

## 1. Product profile

### 1.1 General description

High-voltage, high-speed planar-passivated NPN power switching transistor in a SOT428 (D-PAK) surface mounted package.

### 1.2 Features and benefits

- Low thermal resistance
- Fast switching

### 1.3 Applications

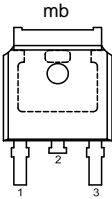
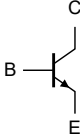
- Electronic lighting ballasts
- DC-to-DC converters
- Inverters
- Motor control systems

### 1.4 Quick reference data

- $V_{CESM} \leq 700 \text{ V}$
- $I_C \leq 4 \text{ A}$
- $P_{tot} \leq 80 \text{ W}$
- $h_{FEsat} = 12.5 \text{ (typ)}$

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	base	 <p style="text-align: center;"><b>SOT428 (D-PAK)</b></p>	 <p style="text-align: center;">sym123</p>
2	collector <a href="#">[1]</a>		
3	emitter		
mb	mounting base; connected to collector		

[1] It is not possible to make a connection to pin 2 of the SOT428 (D-PAK) package.

### 3. Ordering information

Table 2. Ordering information

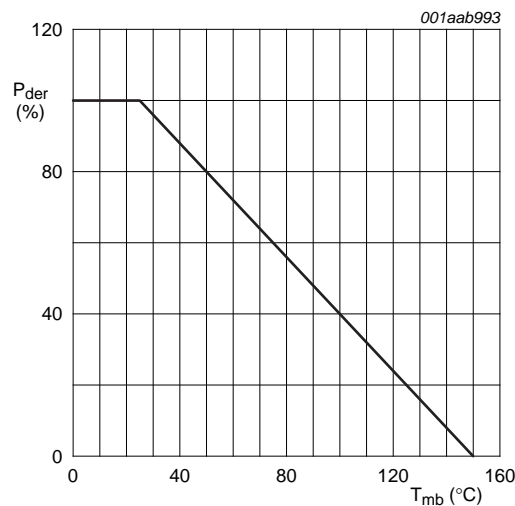
Type number	Package		Version
	Name	Description	
BUJ103AD	D-PAK	plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT428

### 4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CESM}$	peak collector-emitter voltage	$V_{BE} = 0\text{ V}$	-	700	V
$V_{CBO}$	collector-base voltage	open emitter	-	700	V
$V_{CEO}$	collector-emitter voltage	open base	-	400	V
$I_C$	collector current (DC)		-	4	A
$I_{CM}$	peak collector current		-	8	A
$I_B$	base current (DC)		-	2	A
$I_{BM}$	peak base current		-	4	A
$P_{tot}$	total power dissipation	$T_{mb} \leq 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	80	W
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	150	°C



$$P_{der}(\%) = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

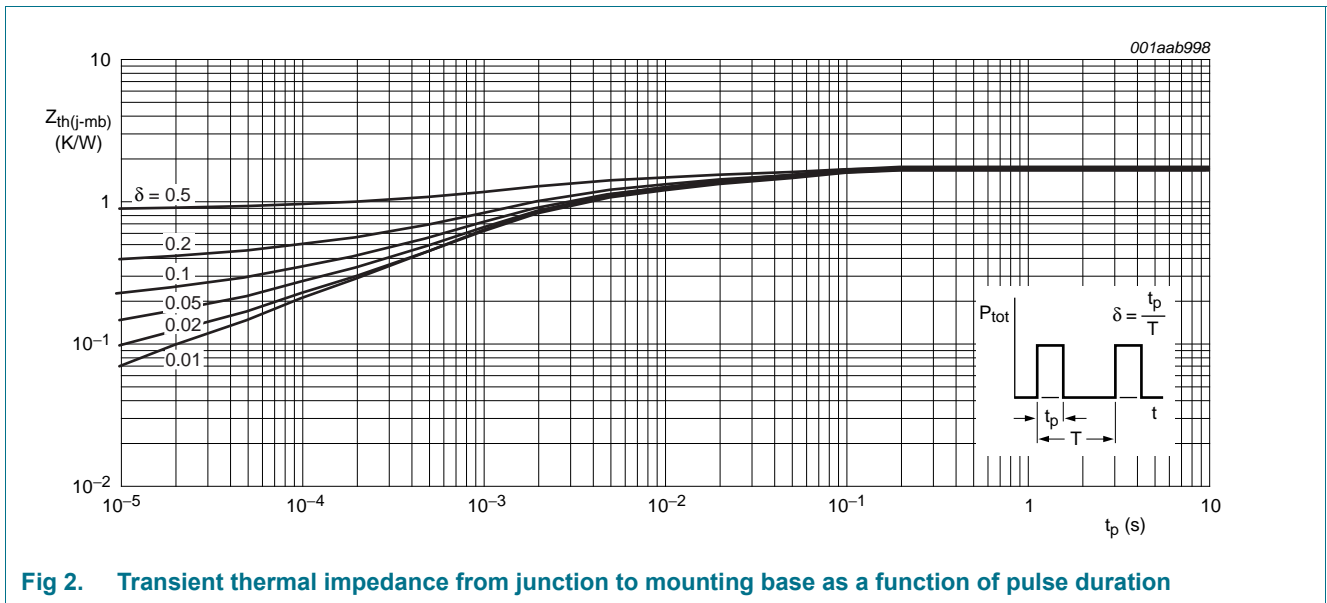
Fig 1. Normalized total power dissipation as a function of mounting base temperature

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 2</a>	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	75	-	K/W

[1] Device mounted on a printed-circuit board; minimum footprint.



**Fig 2. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 5. Characteristics**

$T_{mb} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{CES}$	collector-emitter cut-off current	$V_{BE} = 0\text{ V}; V_{CE} = V_{CESMmax}$	[1]	-	1.0	mA
		$V_{BE} = 0\text{ V}; V_{CE} = V_{CESMmax}; T_j = 125\text{ }^\circ\text{C}$	[1]	-	2.0	mA
$I_{CBO}$	collector-base cut-off current	$V_{BE} = 0\text{ V}; V_{CE} = V_{CESMmax}$	[1]	-	1.0	mA
$I_{CEO}$	collector-emitter cut-off current	$V_{CEO} = V_{CEOMmax} = 400\text{ V}$	[1]	-	0.1	mA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 7\text{ V}; I_C = 0\text{ A}$	-	-	0.1	mA
$V_{CE0sus}$	collector-emitter sustaining voltage	$I_B = 0\text{ A}; I_C = 10\text{ mA}; L = 25\text{ mH}$ ; see <a href="#">Figure 3</a> and <a href="#">4</a>	400	-	-	V
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 3.0\text{ A}; I_B = 0.6\text{ A}$ ; see <a href="#">Figure 10</a>	-	0.25	1.0	V
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 3.0\text{ A}; I_B = 0.6\text{ A}$ ; see <a href="#">Figure 11</a>	-	0.97	1.5	V
$h_{FE}$	DC current gain	$I_C = 1\text{ mA}; V_{CE} = 5\text{ V}$ ; see <a href="#">Figure 9</a>	10	17	32	
		$I_C = 500\text{ mA}; V_{CE} = 5\text{ V}$	13	22	32	

**Table 5. Characteristics ...continued**  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$h_{FEsat}$	DC saturation current gain	$I_C = 2.0\text{ A}$ ; $V_{CE} = 5\text{ V}$	11	16	22	
		$I_C = 3.0\text{ A}$ ; $V_{CE} = 5\text{ V}$	-	12.5	-	

**Dynamic characteristics**

Switching times (resistive load); see [Figure 5](#) and [6](#)

$t_{on}$	turn-on time	$I_{Con} = 2.5\text{ A}$ ; $I_{Bon} = -I_{Boff} = 0.5\text{ A}$ ; $R_L = 75\text{ }\Omega$	-	0.52	0.6	$\mu\text{s}$
$t_{stg}$	storage time		-	2.7	3.3	$\mu\text{s}$
$t_f$	fall time		-	0.3	0.35	$\mu\text{s}$

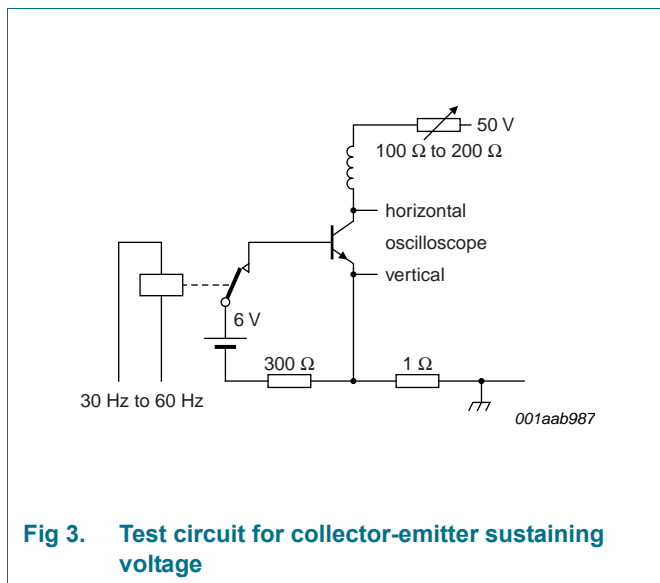
Switching times (inductive load); see [Figure 7](#) and [8](#)

$t_{stg}$	storage time	$I_{Con} = 2\text{ A}$ ; $I_{Bon} = 0.4\text{ A}$ ; $L_B = 1\text{ }\mu\text{H}$ ; $V_{BB} = -5\text{ V}$	-	1.2	1.4	$\mu\text{s}$
$t_f$	fall time		-	30	60	ns

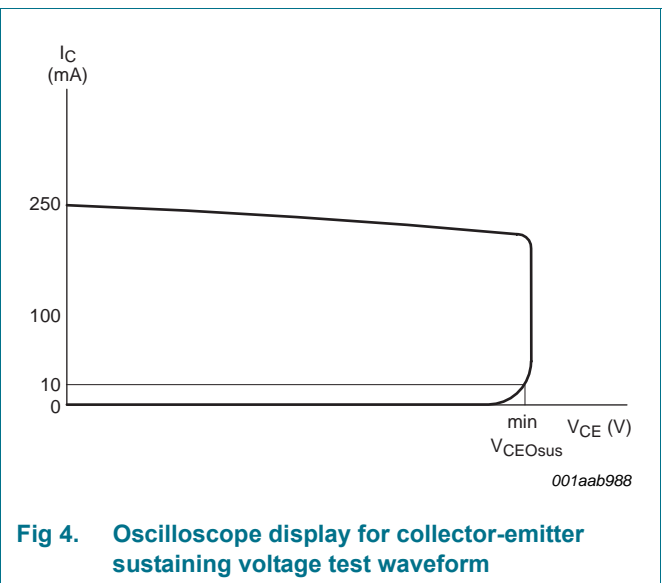
Switching times (inductive load); see [Figure 7](#) and [8](#)

$t_{stg}$	storage time	$I_{Con} = 2\text{ A}$ ; $I_{Bon} = 0.4\text{ A}$ ; $L_B = 1\text{ }\mu\text{H}$ ; $V_{BB} = -5\text{ V}$ ; $T_j = 100\text{ }^{\circ}\text{C}$	-	-	1.8	$\mu\text{s}$
$t_f$	fall time		-	-	120	ns

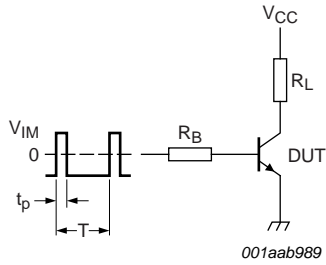
[1] Measured with half sine-wave voltage (curve tracer).



**Fig 3. Test circuit for collector-emitter sustaining voltage**

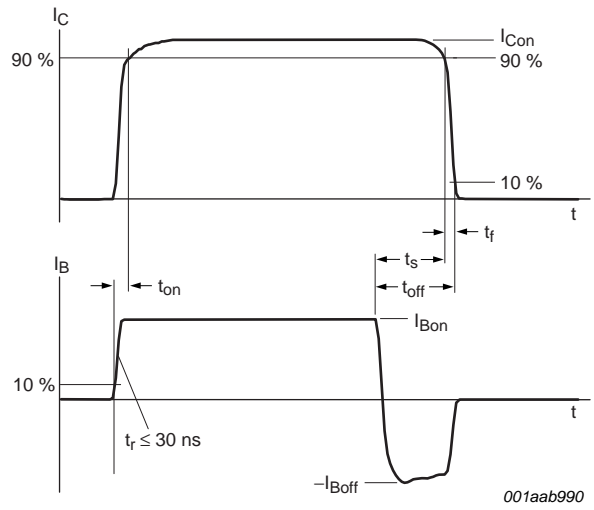


**Fig 4. Oscilloscope display for collector-emitter sustaining voltage test waveform**

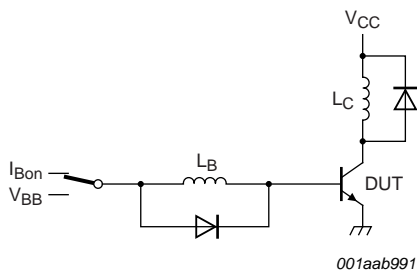


$V_{IM} = -6\text{ V to }+8\text{ V}; V_{CC} = 250\text{ V}; t_p = 20\text{ }\mu\text{s};$   
 $\delta = t_p/T = 0.01.$   
 $R_B$  and  $R_L$  calculated from  $I_{Con}$  and  $I_{Bon}$  requirements.

**Fig 5. Test circuit for resistive load switching**

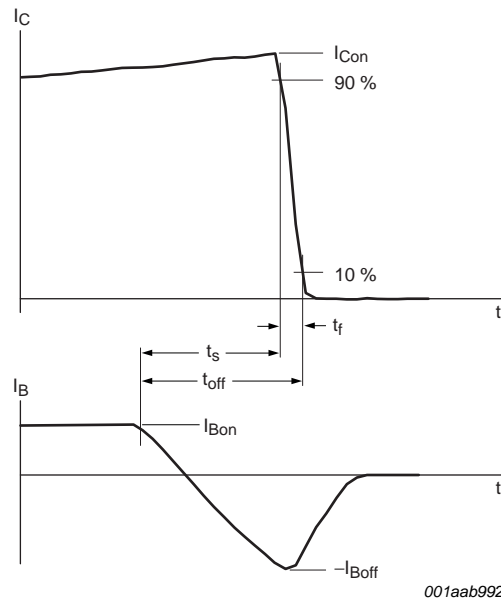


**Fig 6. Switching times waveforms for resistive load**

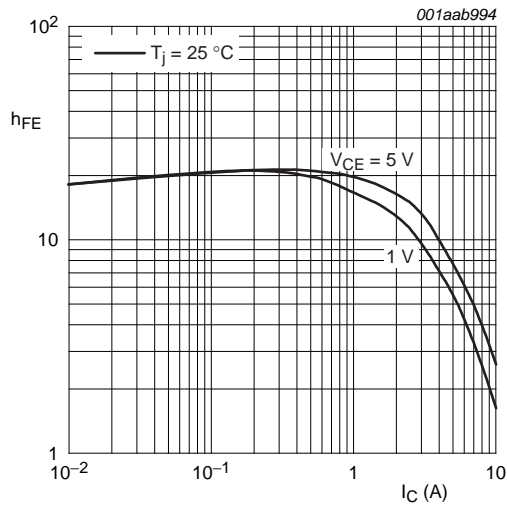


$V_{CC} = 300\text{ V}; V_{BB} = -5\text{ V}; L_C = 200\text{ }\mu\text{H}; L_B = 1\text{ }\mu\text{H}.$

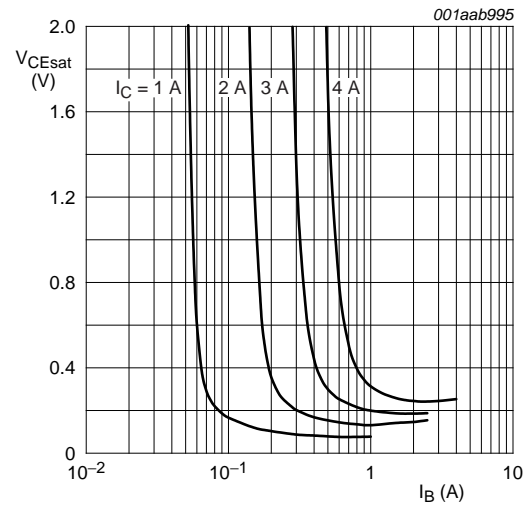
**Fig 7. Test circuit for inductive load switching**



**Fig 8. Switching times waveforms for inductive load**

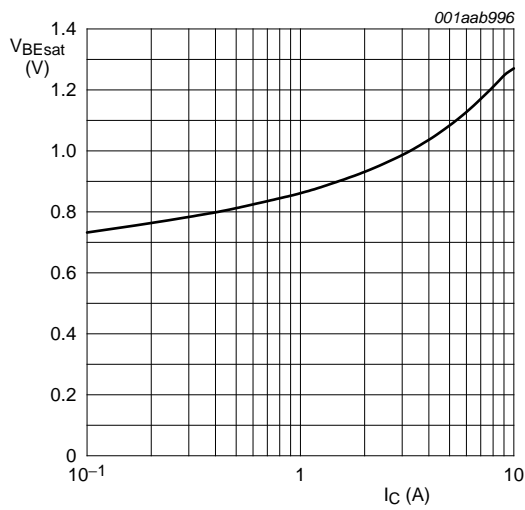


**Fig 9. DC current gain as a function of collector current; typical values**



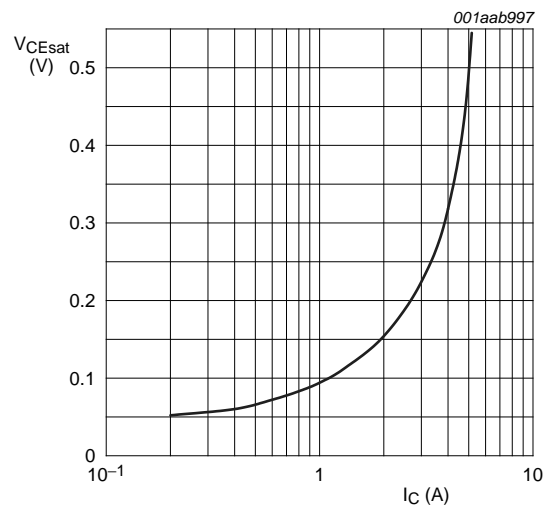
$T_j = 25\text{ }^\circ\text{C}$ .

**Fig 10. Collector-emitter saturation voltage as a function of base current; typical values**



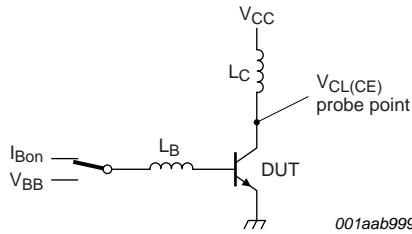
$I_C/I_B = 4$ .

**Fig 11. Base-emitter saturation voltage as a function of collector current; typical values**



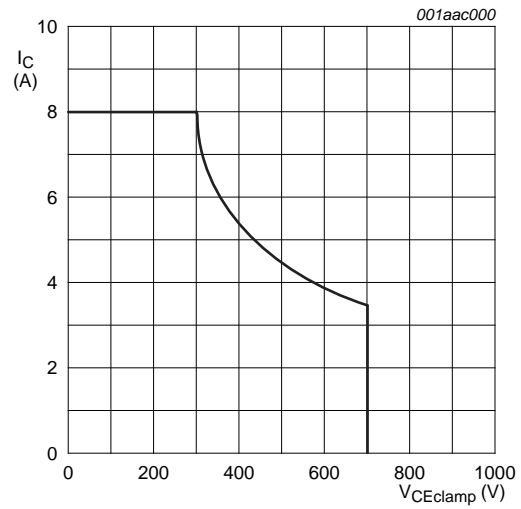
$I_C/I_B = 4$ .

**Fig 12. Collector-emitter saturation voltage as a function of collector current; typical values**



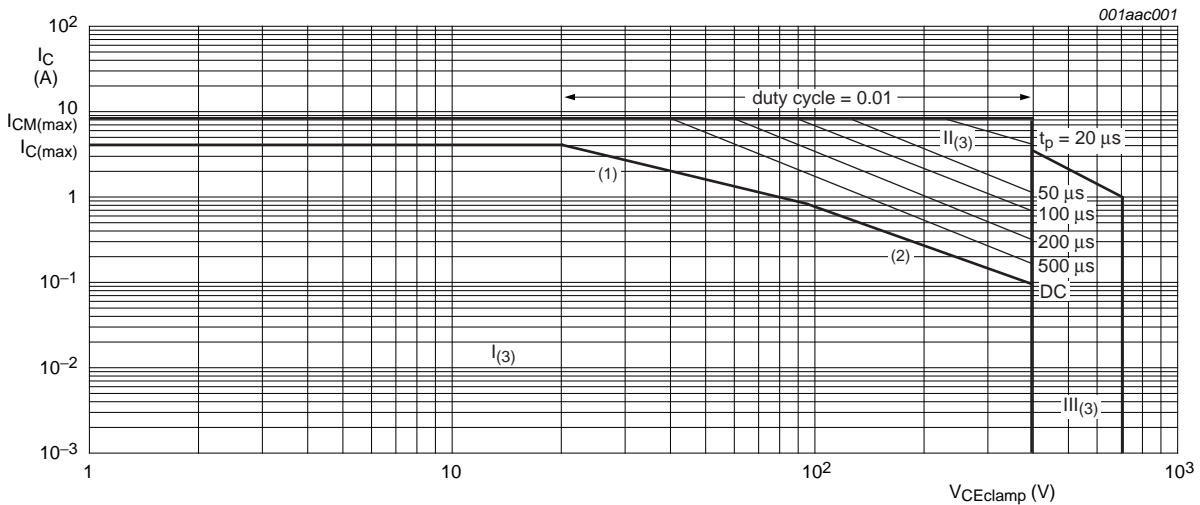
$V_{CEclamp} \leq 1000 \text{ V}$ ;  $V_{CC} = 150 \text{ V}$ ;  $V_{BB} = -5 \text{ V}$ ;  $L_B = 1 \mu\text{H}$ ;  $L_C = 200 \mu\text{H}$ .

**Fig 13. Test circuit for reverse bias safe operating area**



$T_j \leq T_{j(max)}$ .

**Fig 14. Reverse bias safe operating area**



$T_{mb} \leq 25 \text{ }^\circ\text{C}$ ; Mounted with heatsink compound and  $30 \pm 5$  Newton force on the center of the envelope.

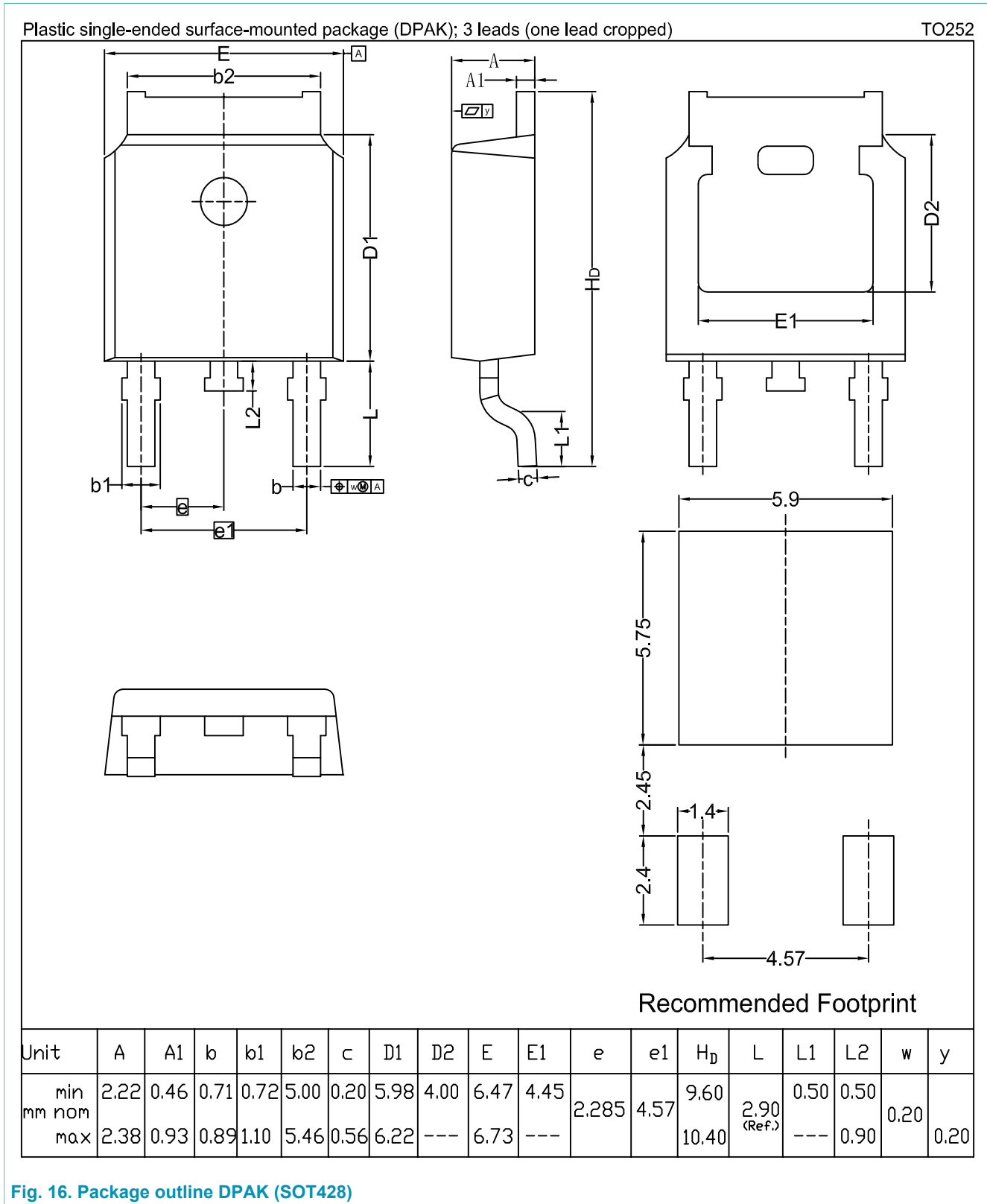
- (1)  $P_{tot}$  maximum and  $P_{tot}$  peak maximum lines.
- (2) Second breakdown limits.
- (3) I = Region of permissible DC operation.  
 II = Extension for repetitive pulse operation.  
 III = Extension during turn-on in single transistor converters provided that  $R_{BE} \leq 100 \Omega$  and  $t_p \leq 0.6 \mu\text{s}$ .

**Fig 15. Forward bias safe operating area**

## 7. Package information

Epoxy meets requirements of UL94 V-0 at  $\frac{1}{8}$  inch.

**8. Package outline**



**Fig. 16. Package outline DPAK (SOT428)**



## 9. Legal information

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