



# BUK964R8-60E

N-channel TrenchMOS logic level FET

29 July 2016

Product data sheet

## 1. General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with VGS(th) rating of greater than 0.5V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

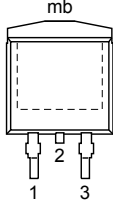
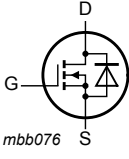
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	60	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	[1]	-	-	100	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	-	234	W
<b>Static characteristics</b>							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>		-	3.78	4.8	mΩ
<b>Dynamic characteristics</b>							
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	20.3	-	nC

[1] Continuous current is limited by package.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>D2PAK (SOT404)</p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK964R8-60E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK964R8-60E	BUK964R8-60E

## 8. Limiting values

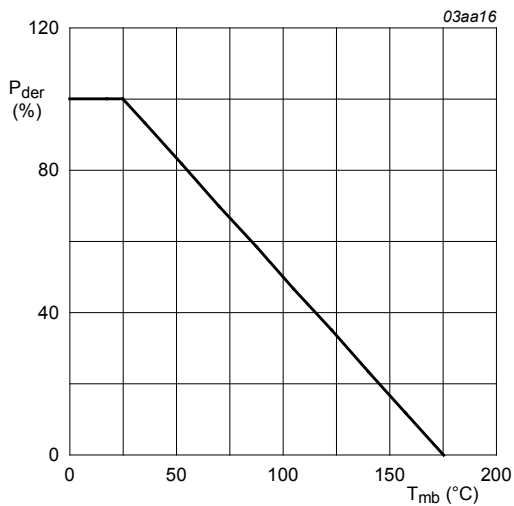
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	60	V	
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V	
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC	-10	10	V	
		$T_j \leq 175\text{ °C}$ ; Pulsed	[1][2]	-15	15	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1	-	234	W	
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 2	[3]	-	100	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 2	[3]	-	100	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 3	-	596	A	
$T_{stg}$	storage temperature		-55	175	°C	

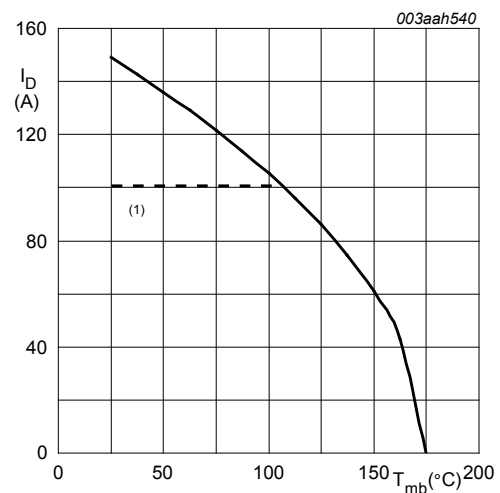
Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[3]	-	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	596	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 60 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped; Fig. 4	[4][5]	-	273	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>
- [3] Continuous current is limited by package.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.



**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



(1) Capped at 100A due to package

**Fig. 2. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 5V$$

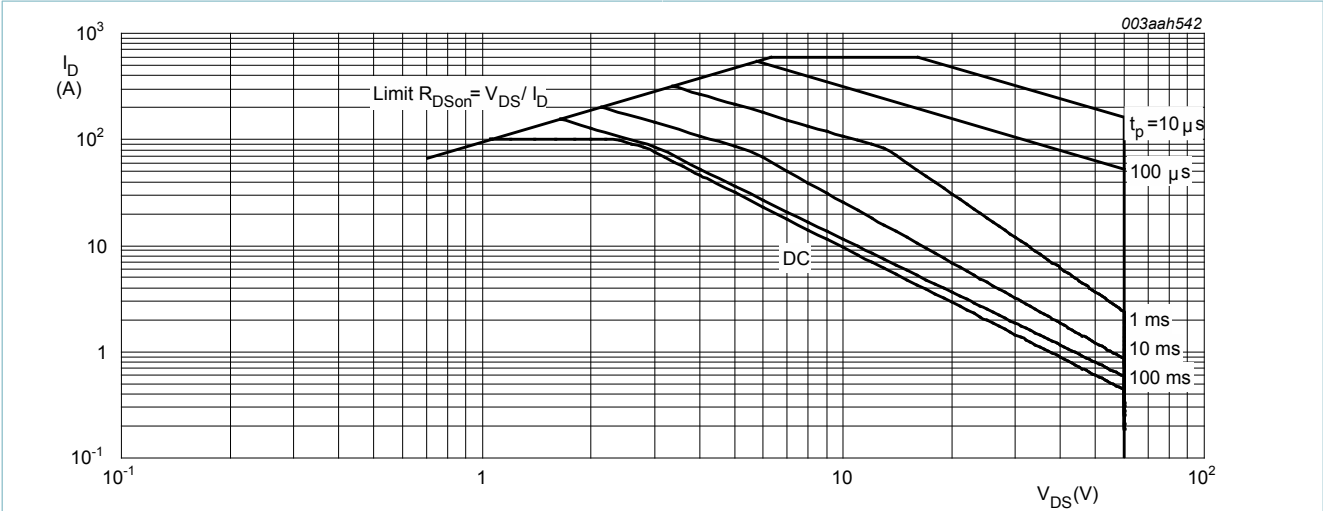


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$ ;  $I_{DM}$  is a single pulse

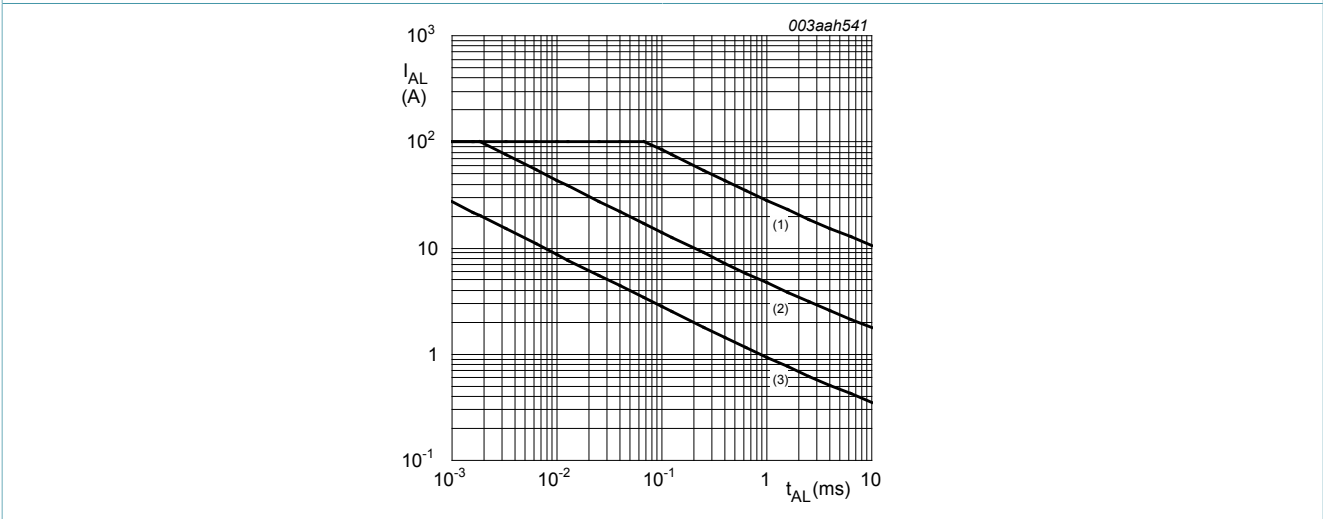


Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_j(init) = 25^\circ C$ ; (2)  $T_j(init) = 150^\circ C$ ; (3) Repetitive Avalanche

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.64	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

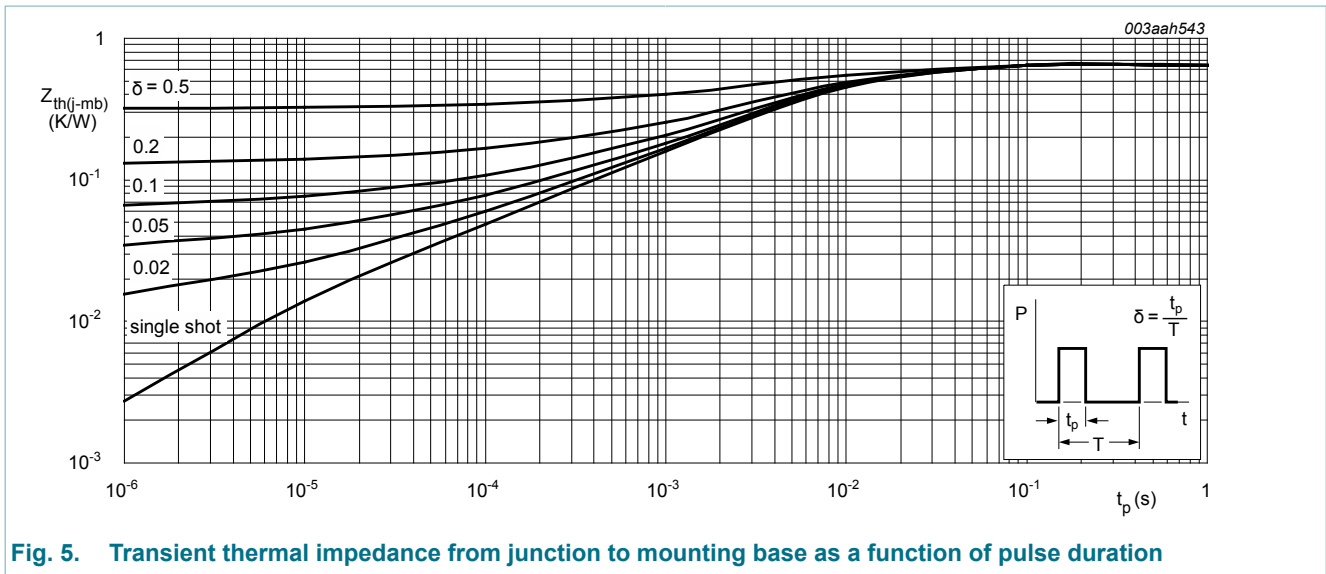


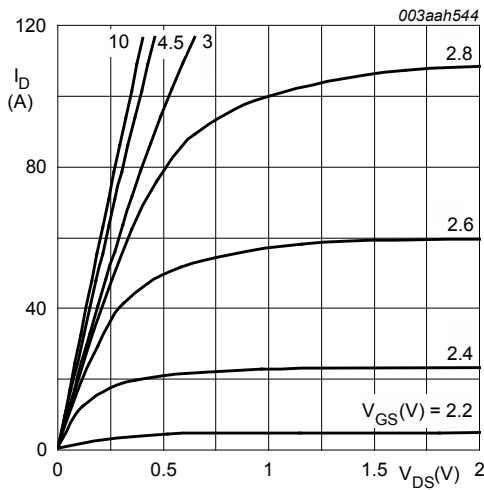
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

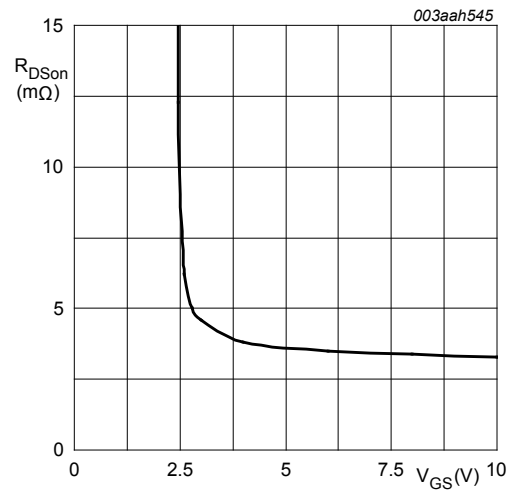
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.05	1	$\mu A$
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	3.78	4.8	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	3.42	4.4	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 11</a>	-	-	10.6	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 5 \text{ V};$ <a href="#">Fig. 13; Fig. 14</a>	-	65	-	nC
$Q_{GS}$	gate-source charge		-	17.5	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{GD}$	gate-drain charge		-	20.3	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 15}$	-	7282	9710	pF
$C_{oss}$	output capacitance		-	607	729	pF
$C_{rss}$	reverse transfer capacitance		-	313	429	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 45\text{ V}; R_L = 1.8\text{ }\Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\text{ }\Omega$	-	36	-	ns
$t_r$	rise time		-	73	-	ns
$t_{d(off)}$	turn-off delay time		-	78	-	ns
$t_f$	fall time		-	68	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 16}$	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}$	-	39	-	ns
$Q_r$	recovered charge		-	56	-	nC



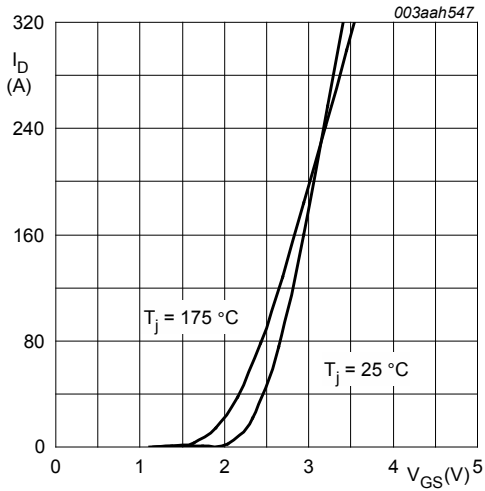
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



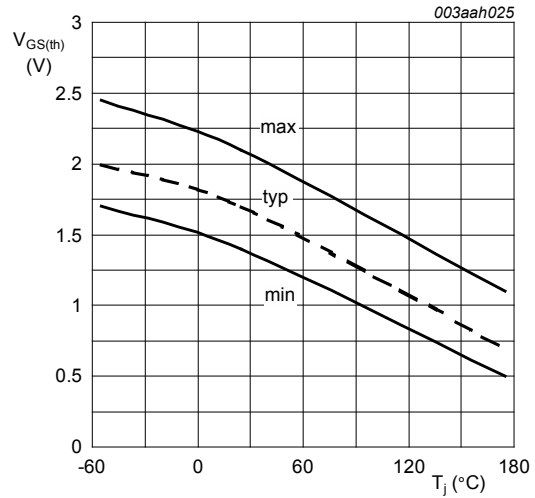
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$



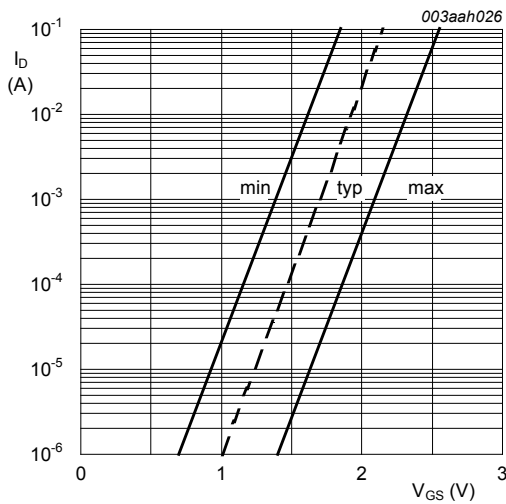
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$



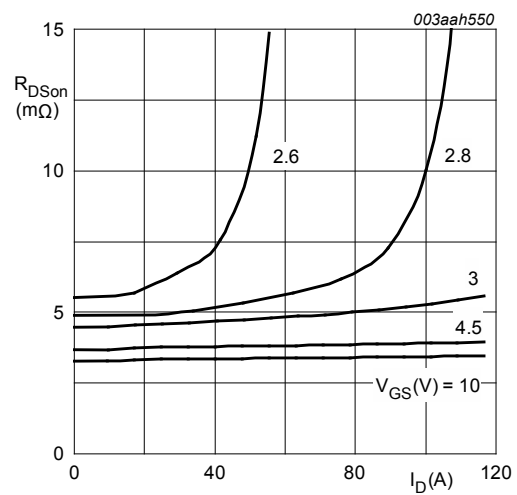
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5V$



$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

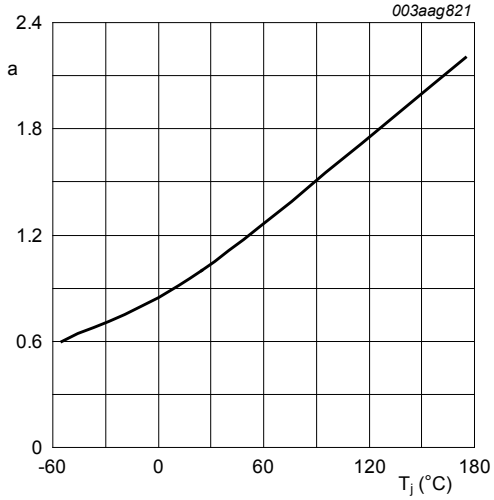


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$



Fig. 13. Gate charge waveform definitions

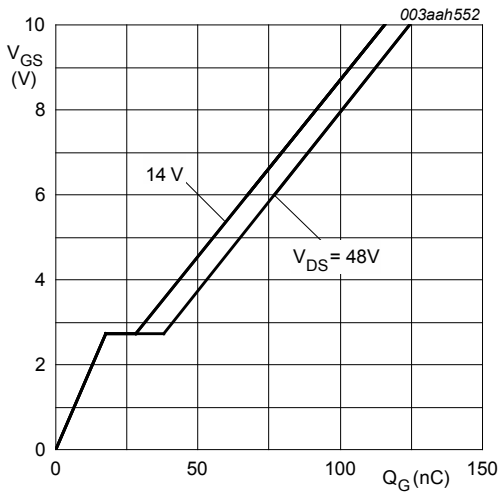


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$

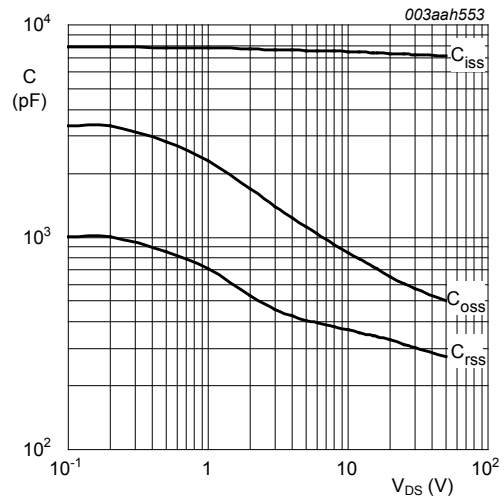
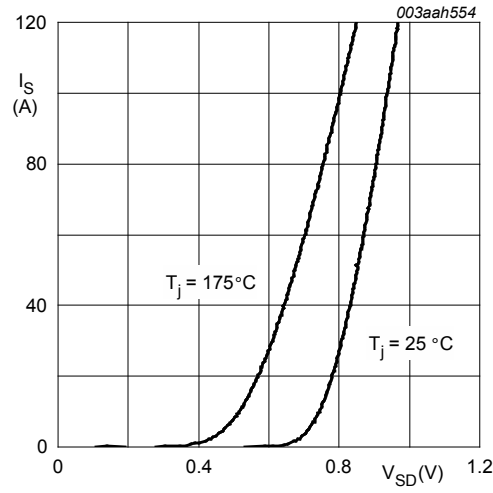


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$



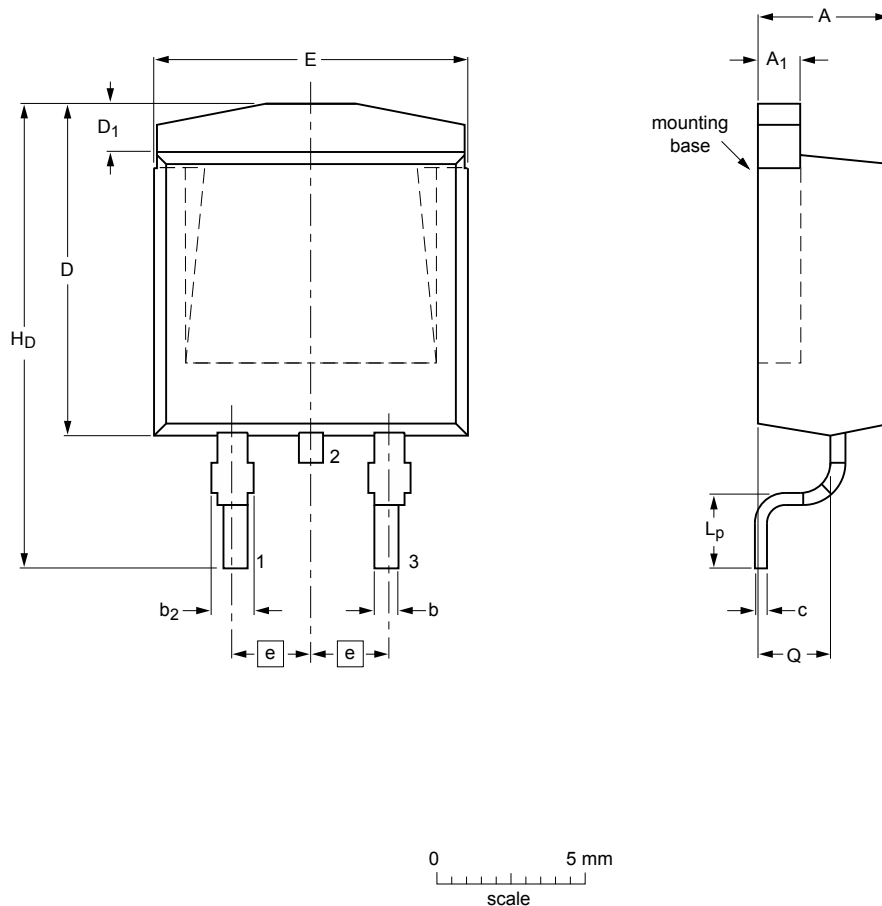


**Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

$$V_{GS} = 0V$$

### 11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	H <sub>D</sub>	L <sub>p</sub>	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 17. Package outline D2PAK (SOT404)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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