

CBTL05024

High performance multiplexer/demultiplexer switch for Thunderbolt applications

Rev. 4 — 27 March 2014

Product data sheet

1. General description

The CBTL05024 is a multiplexer/demultiplexer switch chip optimized to interface the Thunderbolt/MiniDP connector with Thunderbolt systems. It supports 10.3125 Gbit/s Thunderbolt or DisplayPort v1.2 channels.

The TB MUX is a 3 : 1 switch that selects between Thunderbolt data path and DisplayPort v1.2 side-band signals — either DDC or AUX.

The DP MUX is a 2 : 1 switch that selects between DP ML (DisplayPort Main Link) and LS TX/RX signals. Both LSTX and LSRX are the side-band signals for Thunderbolt channel.

This chip also includes HPD and CA_DET buffers for HPD_IN and CA_DET control signals.

CBTL05024 is powered by a 3.3 V supply and it is available in a 3 mm × 3 mm HVQFN24 package with 0.4 mm pitch.

2. Features and benefits

2.1 TB MUX 3 : 1 switch

- This 3 : 1 switch is implemented by two cascaded 2 : 1 switches
 - ◆ The first 2 : 1 10G MUX is controlled by TB_ENA, AUXIO_EN and DP_PD pins
 - ◆ The second 2 : 1 AUX MUX is controlled by CA_DET signal multiplexing of the 720 Mbit/s Differential FAUX (or 1 Mbit/s AUX) and DDC (Direct Display Control) signals
 - ◆ When CA_DET is HIGH, DDC path is selected
- Differential TB channel
 - ◆ Low insertion loss: -1.3 dB at 5 GHz
 - ◆ Low return loss: < -20 dB at 5 GHz
 - ◆ Low ON-state resistance: 8 Ω
 - ◆ Bandwidth: 10 GHz
 - ◆ Low off-state isolation: -20 dB at 5 GHz
 - ◆ Low crosstalk: -36 dB at 5 GHz
 - ◆ Differential input voltage V_{ID} : 1.2 V (maximum)
- Differential AUX channel
 - ◆ Low insertion loss: -1.1 dB at 5 MHz; -1.8 dB at 360 MHz
 - ◆ Low return loss: -18 dB at 5 MHz; -16 dB at 360 MHz



- ◆ Low ON-state resistance: 13 Ω (typical); 16 Ω (maximum)
- ◆ Bandwidth: 3 GHz
- ◆ Low off-state isolation: -80 dB at 5 MHz; -55 dB at 360 MHz
- ◆ Low crosstalk: -26 dB at 2.7 GHz
- ◆ Common-mode input voltage V_{IC} : 0 V to 3.3 V
- ◆ Differential input voltage V_{ID} : 1.4 V (maximum)
- DDC channel
 - ◆ ON-state resistor: 50 Ω (maximum)
 - ◆ 100 kHz 3.3 V voltage swing signal
- Both AUXIO+ and AUXIO- outputs have 85 k Ω (± 20 %) resistors
 - ◆ The 85 k Ω AUXIO- pull-up resistor
 - ◆ The 85 k Ω AUXIO+ pull-down resistor is always present

2.2 DP MUX 2 : 1 switch

- Multiplexes between differential DP ML signal and LSTX/LSRX signals
- The DP ML (DisplayPort Main Link) runs up to HBR2 data rate of 5.4 Gbit/s
- The low speed DC-coupled signals LSTX and LSRX are 3.3 V single-ended signals that operate at 1 Mbit/s
- 5.4 Gbit/s DP-DPMLO path for DP MUX
 - ◆ Low insertion loss for DP-DPMLO path: -1.2 dB at 2.7 GHz
 - ◆ Low return loss for DP-DPMLO path: -15 dB at 2.7 GHz
 - ◆ Low ON-state resistance for DP-DPMLO path: 9 Ω
 - ◆ High bandwidth: 5.5 GHz
 - ◆ Low off-state isolation: -20 dB at 2.7 GHz
 - ◆ Low crosstalk: -25 dB at 2.7 GHz
 - ◆ Common-mode input voltage V_{IC} : 0 V to 3.3 V
 - ◆ Differential input voltage V_{ID} : 1.4 V (maximum)
- LS-DPMLO path for DP MUX
 - ◆ Low insertion loss: single-ended insertion loss (ON) is -1.0 dB at 5 MHz
 - ◆ Low return loss: single-ended return loss (ON) is -20 dB at 5 MHz
 - ◆ Low ON-state resistance: 16 Ω (typical) for $V_{DD} = 3.3$ V
 - ◆ High bandwidth: Single-ended -3 dB bandwidth is 1 GHz
 - ◆ Low off-state isolation: single-ended insertion loss (OFF) is -60 dB at 5 MHz
 - ◆ Low crosstalk: -40 dB at 5 GHz

2.3 General

- The input of the HPD (Hot Plug Detect) buffer is 5 V tolerant
- HPDOOUT and CA_DETOUT buffers
 - ◆ CA_DET input leakage current < 0.1 μ A to prevent driving the 1 M Ω pull-down to a HIGH level
- Integrated LSRX buffer with 1 M Ω pull-down resistor (R1) on the LSRX buffer input
- Integrated 8.75 k Ω pull-up resistor (R4) on the LSTX pin

- When AUXIO_EN = 1, TB_ENA = 0 and DP_PD = 1, the CBTL05024 is in Detect mode
 - ◆ AUXIO+ and AUXIO– of the TB MUX are disabled
 - ◆ LS path is selected in DP MUX
 - ◆ CA_DET and HPD buffers are on
 - ◆ When the CBTL05024 is in Detect mode, this chip consumes < 18 μW
- Patent-pending high bandwidth analog pass-gate technology
- Very low intra-pair differential skew (5 ps typical)
- Back current protection on connector pins (AUXIO+/-, DPMLO+/-, CA_DET and HPD pins)
- All channels support rail-to-rail input voltage
- All CMOS input buffer with hysteresis
- Single 3.3 V ± 10 % power supply
- HVQFN24 3 mm × 3 mm package, 0.4 mm pitch, exposed center pad for thermal relief and electrical ground
- ESD: 2000 V HBM, 1000 V CDM
- Operating temperature range –20 °C to 85 °C

3. Ordering information

Table 1. Ordering information

| Type number | Topside marking | Package | | |
|-------------|-----------------|---------|---|----------|
| | | Name | Description | Version |
| CBTL05024BS | 024 | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3 × 3 × 0.85 mm ^[1] | SOT905-1 |

[1] Maximum package height is 1 mm.

3.1 Ordering options

Table 2. Ordering options

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature |
|-------------|-----------------------|---------|--------------------------------------|------------------------|-------------------------------------|
| CBTL05024BS | CBTL05024BSHP | HVQFN24 | Reel 13" Q2/T3 *standard mark SMD | 6000 | T _{amb} = –20 °C to +85 °C |

4. Block diagram

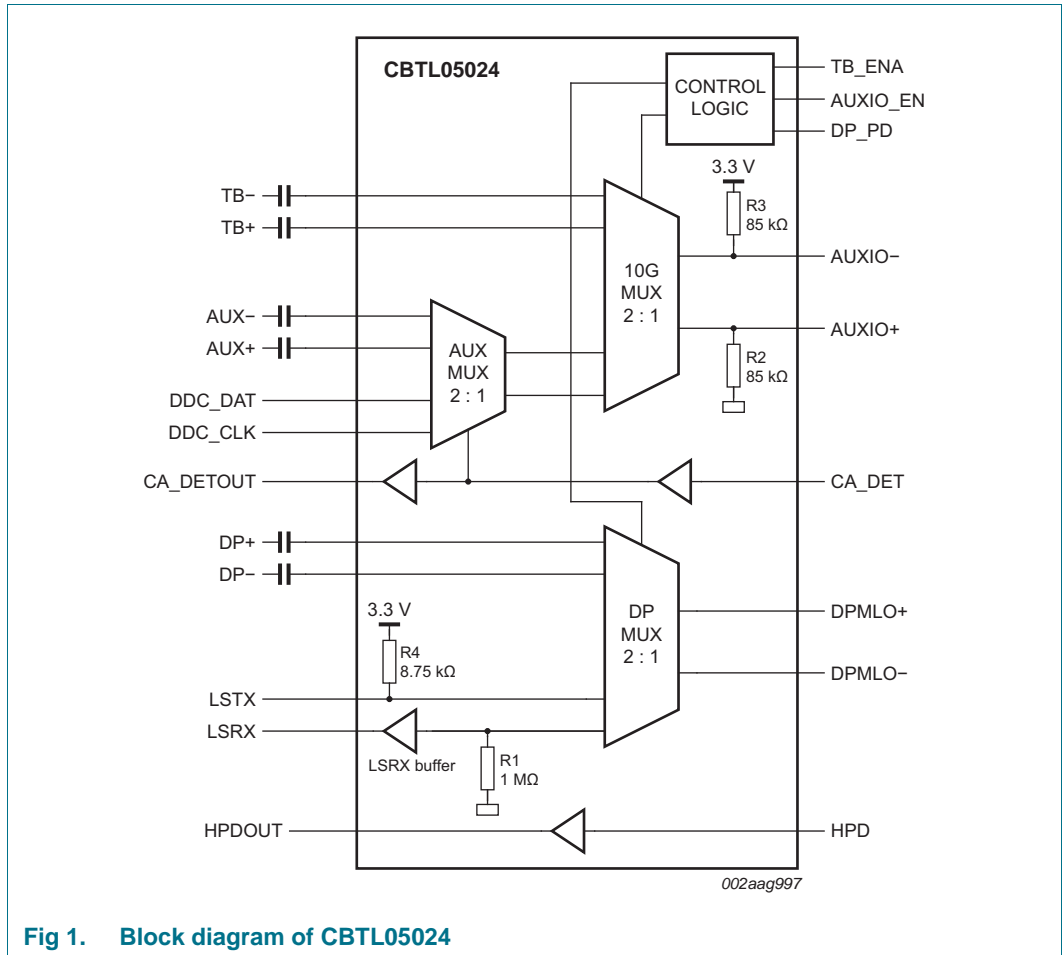
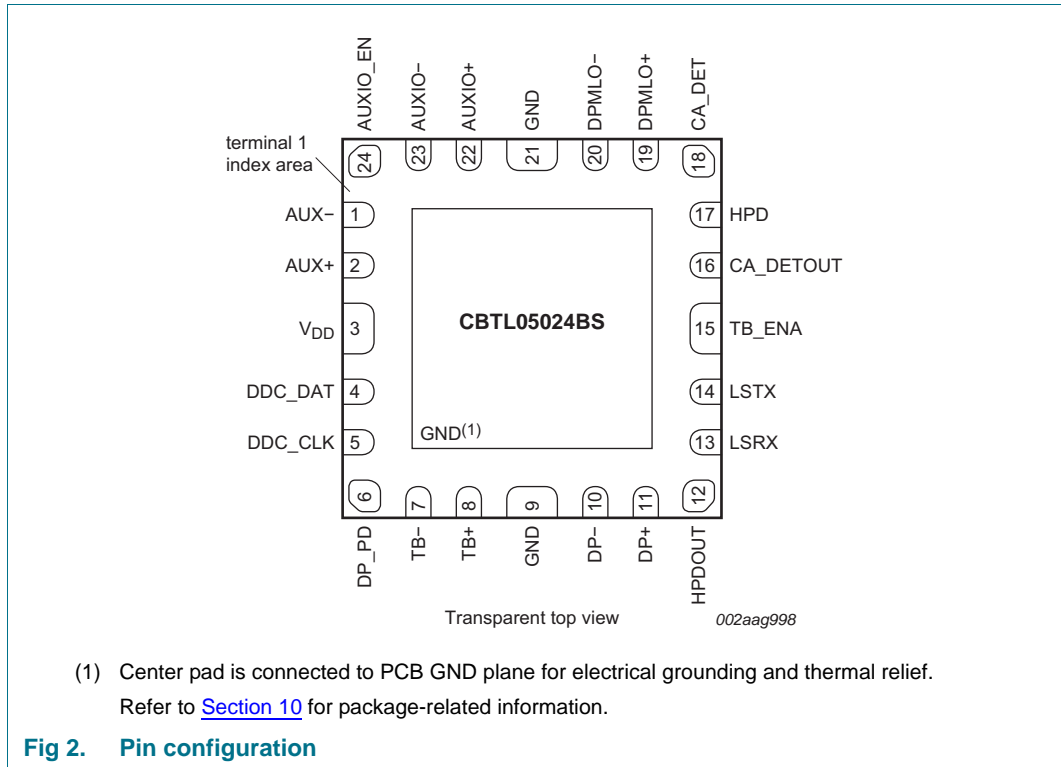


Fig 1. Block diagram of CBTL05024

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 3. Pin description

| Symbol | Pin | Type | Description |
|----------------------------|------------|---------------------|---|
| Data path signals | | | |
| AUX- | 1 | differential I/O | AUX differential signals. The input to this pin must be AC-coupled externally. |
| AUX+ | 2 | differential I/O | |
| TB- | 7 | differential I/O | Thunderbolt differential signals. These output signals must be AC-coupled externally. |
| TB+ | 8 | differential I/O | |
| AUXIO- | 23 | differential I/O | Differential signals for TB MUX. |
| AUXIO+ | 22 | differential I/O | |
| DDC_CLK | 5 | single-ended I/O | Pair of single-ended terminals for DDC clock and data signals. |
| DDC_DAT | 4 | single-ended I/O | |
| DP- | 10 | differential I/O | High-speed differential pair. The input to this pin must be AC-coupled externally. |
| DP+ | 11 | differential I/O | |
| DPMLO- | 20 | differential I/O | Differential signals for DP MUX. |
| DPMLO+ | 19 | differential I/O | |
| LSRX | 13 | single-ended output | Single-ended TB low speed receive signal. |
| LSTX | 14 | single-ended I/O | Single-ended TB low speed transmit signal. |
| Control signals | | | |
| HPDOUT | 12 | CMOS output | Output buffer for HPD. |
| HPD | 17 | CMOS input | HPD input with 5 V tolerance. |
| CA_DET | 18 | CMOS input | When CA_DET = HIGH, DDC_CLK and DDC_DAT is selected. When CA_DET = LOW, AUX path is selected. |
| CA_DETOUT | 16 | CMOS output | 3.3 V CMOS output buffer for CA_DET. |
| TB_ENA | 15 | CMOS input | The control input signal to enable Thunderbolt path for TB MUX. |
| AUXIO_EN | 24 | CMOS input | The control signal for TB MUX. |
| DP_PD | 6 | CMOS input | The control signal for DP MUX. This MUX must work during initial power-up that might have $V_{DD} = 2.3$ V. |
| 3.3 V supply option | | | |
| V_{DD} | 3 | Power | 3.3 V supply. Pin 3 must be connected to system power supply. |
| Ground connections | | | |
| GND | 9, 21 | Ground | Supply ground (0 V). |
| GND | center pad | Ground | The center pad must be connected to GND plane for both electrical grounding and thermal relief. |

6. Functional description

Refer to [Figure 1 “Block diagram of CBTL05024”](#).

The following sections describe the individual block functions and capabilities of the device in more detail.

6.1 Buffer function tables

Table 4. HPD buffer

| HPD input | HPDOUT output |
|-----------|---------------|
| 0 | 0 |
| 1 | 1 |

Table 5. CA_DET buffer

| CA_DET input | CA_DETOUT output |
|--------------|------------------|
| 0 | 0 |
| 1 | 1 |

6.2 AUX MUX function table

Table 6. 2 : 1 AUX MUX function

| CA_DET input | AUXIO |
|--------------|-------|
| 0 | AUX |
| 1 | DDC |

6.3 Operation modes of both DPML MUX and TB MUX

Table 7. Operation modes

| AUXIO_EN | TB_ENA | DP_PD | CA_DET | AUXIO | DPML0 | Modes | R3 | R2 |
|----------|--------|-------|--------|-----------|----------|--------------------------|-----|----|
| 0 | X | 0 | X | 3-state | 3-state | DP Standby mode | ON | ON |
| 0 | X | 1 | X | 3-state | LS | Standby mode | ON | ON |
| 1 | 0 | 0 | 0 | AUX input | DP input | DP mode | ON | ON |
| 1 | 0 | 0 | 1 | DDC | DP input | DP++ mode | ON | ON |
| 1 | 0 | 1 | X | 3-state | LS | Detect mode | ON | ON |
| 1 | 1 | 0 | 1 | TB | DP input | Test mode ^[1] | OFF | ON |
| 1 | 1 | 0 | 0 | 3-state | 3-state | Sleep mode | OFF | ON |
| 1 | 1 | 1 | X | TB | LS | TB mode | OFF | ON |

[1] HPD must be LOW during Test mode.

7. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|------------------|---------------------------------|------------|------|------|------|---|
| V _{DD} | supply voltage | [1] | -0.3 | +4.6 | V | |
| V _I | input voltage | [1] | -0.3 | +5.5 | V | |
| T _{stg} | storage temperature | | -65 | +150 | °C | |
| V _{ESD} | electrostatic discharge voltage | HBM | [2] | - | 2000 | V |
| | | CDM | [3] | - | 1000 | V |

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model – Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[3] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model – Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

8. Recommended operating conditions

Table 9. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------|---|------|-----|-----------------------|------|
| V _{DD} | supply voltage | 3.3 V supply option | 3.0 | 3.3 | 3.6 | V |
| | | initial supply voltage before power supply negotiation done [1] | 2.3 | - | - | V |
| V _I | input voltage | CMOS inputs | -0.3 | - | +5.5 | V |
| | | MUX I/O pins | -0.3 | - | V _{DD} + 0.3 | V |
| T _{amb} | ambient temperature | operating in free air | -20 | - | +85 | °C |

[1] During power supply negotiation only a limited supply voltage is available. The control logic and multiplexers must be in full function with degraded performance. The channel between LSTX/LSRX and DPMLO+/- must work. The initial R_{on} of DP MUX in [Table 14](#) should be < 50 Ω.

9. Characteristics

9.1 Device general characteristics

Table 10. General characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------------------------|---|-----|-------|------|---------|
| I_{DD} | supply current ^[1] | TB mode; $V_{DD} = 3.6$ V | - | 0.25 | 0.35 | mA |
| P_{cons} | power consumption ^[1] | TB mode; $V_{DD} = 3.6$ V; AUXIO_EN = 1, TB_ENA = 1 and DP_PD = 1 | - | 0.825 | 1.26 | mW |
| | | DP or DP++ modes; AUXIO_EN = 1, TB_ENA = 0 and DP_PD = 0 | - | 0.66 | 1.00 | mW |
| | | Sleep or DP Standby modes; (AUXIO_EN = 1, TB_ENA = 1 and CA_DET = DP_PD = 0) for Sleep mode or (AUXIO_EN = 0 and DP_PD = 0) for DP Standby mode | - | 1 | 18 | μ W |
| | | Detect mode; AUXIO_EN = 1, TB_ENA = 0 and DP_PD = 1 | - | 1 | 18 | μ W |
| | | Standby mode; AUXIO_EN = 0, TB_ENA = X and DP_PD = 1 | - | 1 | 18 | μ W |
| $t_{startup}$ | start-up time | supply voltage valid to channel specified operating characteristics | - | 100 | 500 | μ s |
| t_{rcfg} | reconfiguration time | DP_PD, AUXIO_EN, TB_ENA or CA_DET state change to channel specified operating characteristics ^[2] | - | 50 | 100 | μ s |

[1] Do not include current through R4.

[2] Outputs are undefined during reconfiguration, including enable and disable time of the multiplexers.

9.2 3 : 1 TB MUX channel characteristics

Table 11. TB channel of 2 : 1 10G MUX dynamic and static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---------------------------------|---|-----|------|-----|----------|
| DDIL | differential insertion loss | channel is OFF | | | | |
| | | f = 5 GHz | - | -20 | - | dB |
| | | f = 100 MHz | - | -55 | - | dB |
| | | channel is ON | | | | |
| | | f = 5 GHz | - | -1.3 | - | dB |
| | | f = 100 MHz | - | -1 | - | dB |
| DDRL | differential return loss | f = 5 GHz | - | -20 | - | dB |
| | | f = 100 MHz | - | -22 | - | dB |
| DDNEXT | differential near-end crosstalk | adjacent channels are ON | | | | |
| | | f = 5 GHz | - | -18 | - | dB |
| | | f = 2.7 GHz | - | -25 | - | dB |
| | | f = 100 MHz | - | -60 | - | dB |
| | | f = 1 MHz | - | -70 | - | dB |
| R_{on} | ON-state resistance | $V_{DD} = 3.3$ V; $V_I = 3.3$ V; $I_I = 5$ mA | - | 8.5 | 12 | Ω |

Table 11. TB channel of 2 : 1 10G MUX dynamic and static characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|----------------------------|---------------------------|-----|-----|-----------------------|------|
| B _{-3dB} | -3 dB bandwidth | differential | - | 10 | - | GHz |
| t _{PD} | propagation delay | between AUXIO and TB | - | 70 | - | ps |
| t _{sk(dif)} | differential skew time | intra-pair | - | 5 | - | ps |
| V _I | input voltage | TB+/TB- and AUXIO+/AUXIO- | 0 | - | V _{DD} + 0.3 | V |
| V _{ID} | differential input voltage | TB+/TB- and AUXIO+/AUXIO- | - | - | 1.2 | V |

Table 12. AUX - AUXIO channel of AUX MUX dynamic and static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|----------------------------------|---|-----|------|-----------------|------|
| DDIL | differential insertion loss | channel is OFF | | | | |
| | | f = 5 MHz | - | -80 | - | dB |
| | | f = 360 MHz | - | -60 | - | dB |
| | | channel is ON | | | | |
| | | f = 5 MHz | - | -1.1 | - | dB |
| | | f = 360 MHz | - | -1.2 | - | dB |
| DDRRL | differential return loss | f = 5 MHz | - | -19 | - | dB |
| | | f = 360 MHz | - | -18 | - | dB |
| DDNEXT | differential near-end crosstalk | adjacent channels are ON | | | | |
| | | f = 5 GHz | - | -18 | - | dB |
| | | f = 2.7 GHz | - | -25 | - | dB |
| | | f = 100 MHz | - | -60 | - | dB |
| R _{on} | ON-state resistance | adjacent channels are ON | | | | |
| | | f = 5 GHz | - | -18 | - | dB |
| | | f = 2.7 GHz | - | -25 | - | dB |
| | | f = 100 MHz | - | -60 | - | dB |
| R _{on} | ON-state resistance | V _{DD} = 3.3 V; I _I = 10 mA; V _{IC} = 0.9V _{DD} for AUXIO-; V _{IC} = 0.1V _{DD} for AUXIO+ | - | 13 | 16 | Ω |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| B _{-3dB} | -3 dB bandwidth | differential | - | 3 | - | GHz |
| t _{PD} | propagation delay | between AUX and AUXIO | - | 70 | - | ps |
| t _{sk(dif)} | differential skew time | intra-pair | - | 5 | - | ps |
| V _I | input voltage | AUX+/AUX- and AUXIO+/AUXIO- | 0 | - | V _{DD} | V |
| V _{IC} | common-mode input voltage | AUX+/AUX- and AUXIO+/AUXIO- | 0 | - | V _{DD} | V |
| V _{ID} | differential input voltage | AUX+/AUX- and AUXIO+/AUXIO- | - | - | 1.4 | V |
| I _{LIH} | HIGH-level input leakage current | AUX+/AUX- pins; V _{DD} = max; V _I = V _{DD} | - | - | ±1 | μA |
| I _{LIL} | LOW-level input leakage current | AUX+/AUX- pins; V _{DD} = max; V _I = GND | - | - | ±1 | μA |

Table 13. DDC - AUXIO channel of AUX MUX dynamic and static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------------|--|-----|-----|------|------|
| R _{on} | ON-state resistance | V _{DD} = 3.3 V; I _I = 10 mA | - | 35 | 50 | Ω |
| C _{in} | input capacitance | V _{DD} = 3.3 V; V _I = 3.3 V | - | 0.2 | - | pF |
| t _{PD} | propagation delay | between DDC and AUXIO | - | 70 | - | ps |
| I _{LH} | HIGH-level input leakage current | DDC_DAT and DDC_CLK pins; V _{DD} = max; V _I = V _{DD} | - | - | ±1.5 | μA |
| I _{LIL} | LOW-level input leakage current | DDC_DAT and DDC_CLK pins; V _{DD} = max; V _I = GND | - | - | ±1.5 | μA |

9.3 DP MUX channel characteristics

Table 14. Channel dynamic and static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|--|-----|------|-----|------|
| DDIL | differential insertion loss | DP-DPMLO path; channel is OFF | | | | |
| | | f = 2.7 GHz | - | -20 | - | dB |
| | | f = 1.35 GHz | - | -35 | - | dB |
| | | f = 100 MHz | - | -50 | - | dB |
| | | DP-DPMLO path; channel is ON | | | | |
| | | f = 2.7 GHz | - | -1.2 | - | dB |
| | | f = 1.35 GHz | - | -1.1 | - | dB |
| | | f = 100 MHz | - | -0.8 | - | dB |
| α _{il(se)} | single-ended insertion loss | LS-DPMLO path; channel is OFF; f = 5 MHz | - | -60 | - | dB |
| | | LS-DPMLO path; channel is ON; f = 5 MHz | - | -1 | - | dB |
| DDRL | differential return loss | DP-DPMLO path | | | | |
| | | f = 2.7 GHz | - | -15 | - | dB |
| | | f = 100 MHz | - | -20 | - | dB |
| α _{rl(se)} | single-ended return loss | LS-DPMLO path; f = 5 MHz | - | -18 | - | dB |
| DDNEXT | differential near-end crosstalk | adjacent channels are ON | | | | |
| | | f = 5 GHz | - | -18 | - | dB |
| | | f = 2.7 GHz | - | -25 | - | dB |
| | | f = 100 MHz | - | -60 | - | dB |
| | | f = 1 MHz | - | -70 | - | dB |
| R _{on} | ON-state resistance | DP-DPMLO path; V _{DD} = 3.3 V; I _I = 5 mA | - | 9 | 12 | Ω |
| | | LS-DPMLO path; V _{DD} = 3.3 V; I _I = 5 mA | - | 16 | 22 | Ω |
| | | initial ON-state resistance before power supply negotiation done; V _{DD} = 2.3 V; I _I = 5 mA | - | 35 | 50 | Ω |
| | | | | | | |
| B _{-3dB} | -3 dB bandwidth | differential; DP-DPMLO path | - | 5.5 | - | GHz |
| | | single-ended; LS-DPMLO path | - | 1 | - | GHz |
| t _{PD} | propagation delay | between DP+/DP- and DPMLO+/DPMLO- | - | 100 | - | ps |
| t _{sk(dif)} | differential skew time | intra-pair | - | 5 | - | ps |

Table 14. Channel dynamic and static characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------------|--|------|-----|-----------------------|------|
| V _I | input voltage | LSTX/LSRX to DPMLO+/DPMLO- channel | -0.3 | - | V _{DD} + 0.3 | V |
| V _{IC} | common-mode input voltage | DP+/DP- and DPMLO+/DPMLO- | 0 | - | V _{DD} | V |
| V _{ID} | differential input voltage | DP+/DP- to DPMLO+/DPMLO- channel | - | - | 1.4 | V |
| I _{LIH} | HIGH-level input leakage current | DP+/DP- and DPMLO+ pins; V _{DD} = max; V _I = V _{DD} | - | - | ±1 | µA |
| | | DPMLO- pins; V _{DD} = max; V _I = V _{DD} | - | - | ±5 | µA |
| I _{LIL} | LOW-level input leakage current | DP+/DP- and DPMLO+/DPMLO- pins; V _{DD} = max; V _I = GND | - | - | ±1 | µA |

9.4 Control signals characteristics

Table 15. CA_DET input buffer characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------------|--|-----|-----|-----|------|
| V _{IH} | HIGH-level input voltage | | 2 | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I _{LI} | input leakage current | measured with input at V _{IH} = V _{DD} and V _{IL} = 0 V [1] | - | - | 0.1 | µA |

[1] The leakage current on CA_DET pin must not drive the 1 MΩ pull-down to a HIGH level.

Table 16. HPD input buffer characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------------|------------|-----|-----|-----|------|
| V _{IH} | HIGH-level input voltage | | 2 | - | 5 | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.8 | V |

Table 17. TB_ENA, DP_PD or AUXIO_EN input characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------------|--|-----------------------|-----|-----------------------|------|
| V _{IH} | HIGH-level input voltage | CMOS inputs | 0.7 × V _{DD} | - | - | V |
| V _{IL} | LOW-level input voltage | CMOS inputs | - | - | 0.3 × V _{DD} | V |
| I _{LI} | input leakage current | measured with input at V _{IH} = V _{DD} and V _{IL} = 0 V | - | 1 | 10 | µA |

Table 18. CA_DETOUT and HPDOUT output buffer characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|---|-----|-----|-----|------|
| V _{OL} | LOW-level output voltage | I _{OL} = 2 mA; V _{DD} = 3 V | 0 | - | 0.4 | V |
| V _{OH} | HIGH-level output voltage | pull-up voltage; I _{OH} = -2 mA; V _{DD} = 3 V | 2.5 | - | - | V |
| t _{PD} | propagation delay | load capacitance C _L = 5 pF | - | 50 | 100 | ns |

9.5 Integrated LSRX buffer characteristics

Table 19. LSRX buffer characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|----------------------------------|---|------|------|------|------|
| V _{th(LH)} | positive-going threshold voltage | input; V _{DD} = 3.3 V ± 10 % | 0.9 | 1.1 | 1.24 | V |
| | | input; V _{DD} = 2.3 V | 0.8 | 0.9 | 1.02 | V |
| V _{th(HL)} | negative-going threshold voltage | input; V _{DD} = 3.3 V ± 10 % | 0.58 | 0.7 | 0.84 | V |
| | | input; V _{DD} = 2.3 V | 0.5 | 0.57 | 0.63 | V |
| V _{OL} | LOW-level output voltage | I _{OL} = 2 mA; V _{DD} = 3 V | - | 0.2 | 0.4 | V |
| | | I _{OL} = 0.5 mA; V _{DD} = 2.3 V | - | 0.1 | 0.2 | V |
| V _{OH} | HIGH-level output voltage | pull-up voltage; I _{OH} = -2 mA; V _{DD} = 3 V | 2.5 | - | - | V |
| | | pull-up voltage; I _{OH} = -0.5 mA; V _{DD} = 2.3 V | 2.1 | - | - | V |
| t _{PD} | propagation delay | load capacitance C _L = 8 pF | - | 2 | 10 | ns |

9.6 Bias resistor characteristics

Table 20. Characteristics of AUXIO+ pin in DP/DP++ mode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|----------------------|--|-----|-----|-----|------|
| R _{pd} | pull-down resistance | resistor R2; AUXIO_EN = 1, TB_ENA = DP_PD = 0 | 68 | 85 | 102 | kΩ |

Table 21. Characteristics of AUXIO- pin in DP/DP++ mode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------|--|-----|-----|-----|------|
| R _{PU} | pull-up resistance | resistor R3; AUXIO_EN = 1, TB_ENA = DP_PD = 0 | 68 | 85 | 102 | kΩ |

Table 22. Characteristics of DPML0- pin in TB mode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|----------------------|---|-----|-----|-----|------|
| R _{pd} | pull-down resistance | resistor R1; AUXIO_EN = TB_ENA = DP_PD = 1 | 0.8 | 1 | 1.2 | MΩ |

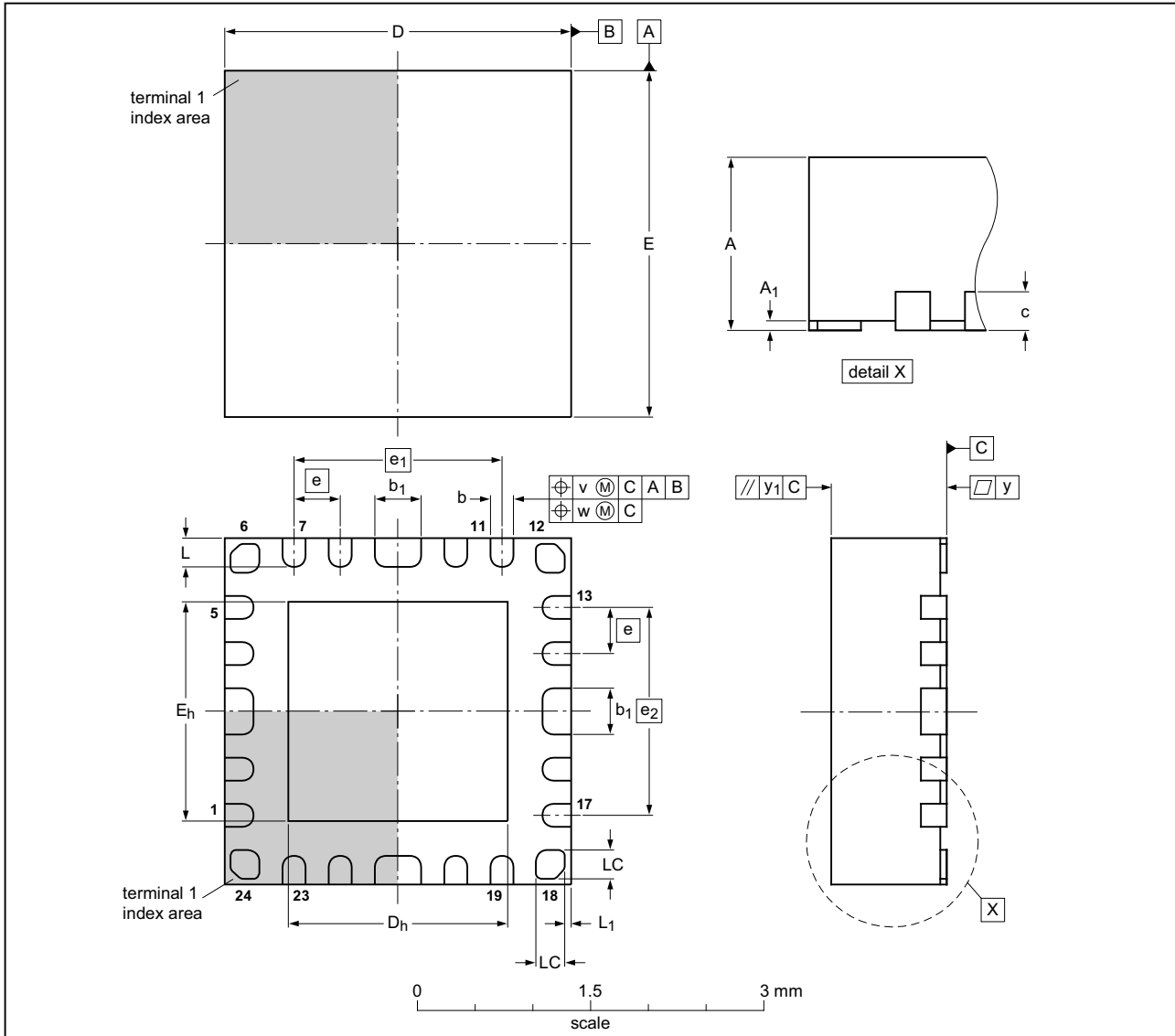
Table 23. Characteristics of LSTX pin

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------|-------------|-----|------|------|------|
| R _{PU} | pull-up resistance | resistor R4 | 7 | 8.75 | 10.5 | kΩ |

10. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3 x 3 x 0.85 mm

SOT905-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A ⁽¹⁾ max | A ₁ | b | b ₁ | c | D ⁽¹⁾ | D _h | E ⁽¹⁾ | E _h | e | e ₁ | e ₂ | L | L ₁ | LC | v | w | y | y ₁ |
|------|-------------------------|----------------|--------------|----------------|-----|------------------|----------------|------------------|----------------|-----|----------------|----------------|--------------|----------------|------------|-----|------|------|----------------|
| mm | 1 | 0.05 0.00 | 0.25 0.15 | 0.45 0.35 | 0.2 | 3.1 2.9 | 2.05 1.75 | 3.1 2.9 | 2.05 1.75 | 0.4 | 1.8 | 1.8 | 0.35 0.15 | 0.1 0.0 | 0.3 0.2 | 0.1 | 0.05 | 0.05 | 0.1 |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|-------|------------------------|----------------------|
| | IEC | JEDEC | JEITA | | |
| SOT905-1 | --- | --- | --- | | 06-03-13 06-03-31 |

Fig 3. Package outline SOT905-1 (HVQFN24)

11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 4](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 24](#) and [25](#)

Table 24. SnPb eutectic process (from J-STD-020D)

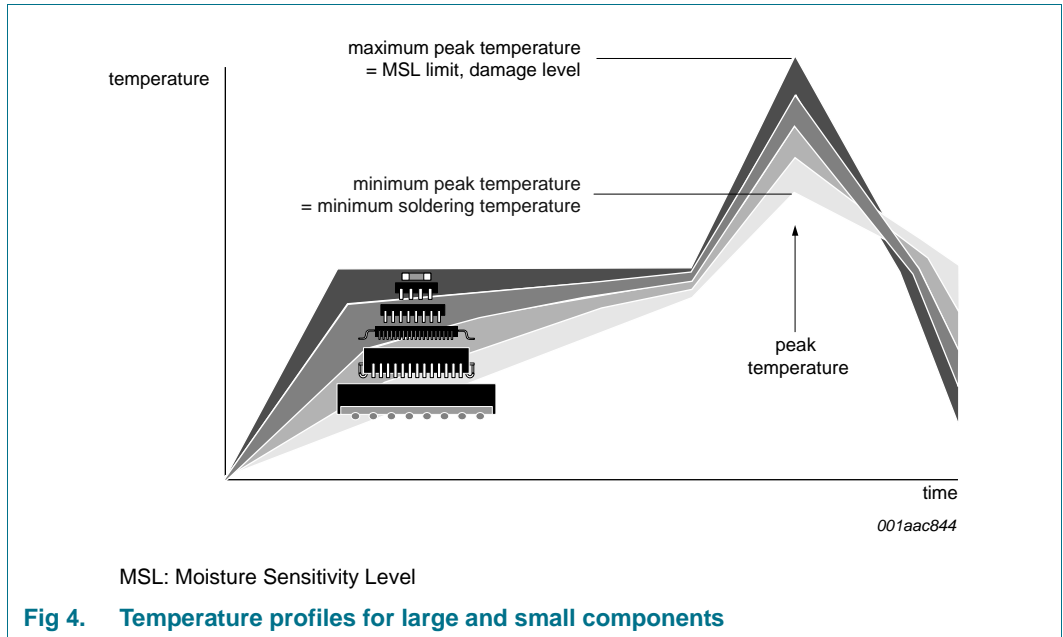
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 25. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 4](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

12. Abbreviations

Table 26. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DP | DisplayPort |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| HPD | Hot Plug Detect |
| I/O | Input/Output |
| MUX | multiplexer |
| PCB | Printed-Circuit Board |

13. Revision history

Table 27. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|--------------------|---------------|---------------|
| CBTL05024 v.4 | 20140327 | Product data sheet | - | CBTL05024 v.3 |
| Modifications: | <ul style="list-style-type: none">The security status of this data sheet has been altered from company confidential to company public. | | | |
| CBTL05024 v.3 | 20131014 | Product data sheet | - | CBTL05024 v.2 |
| CBTL05024 v.2 | 20130715 | Product data sheet | - | CBTL05024 v.1 |
| CBTL05024 v.1 | 20121116 | Product data sheet | - | - |

14. Legal information

14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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