Product data sheet

1. General description

Planar passivated ultra sensitive gate Silicon Controlled Rectifier in a SOT223 surface mountable plastic package.

2. Features and benefits

- Planar passivated for voltage ruggedness and reliability
- Ultra sensitive gate
- Surface mountable package

3. Applications

- Electronic ballasts
- · Safety shut down and protection circuits
- Sensing circuits
- · Smoke detectors
- Switched Mode Power Supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{RRM}	repetitive peak reverse voltage		-	-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \le 114 ^{\circ}\text{C}$; Fig. 1	-	-	0.5	Α
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \le 114 ^{\circ}\text{C}$; Fig. 2; Fig. 3	-	-	0.8	Α
I _{TSM}	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5	-	-	8	Α
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms	-	-	9	Α
T_j	junction temperature		-	-	125	°C
Static chara	cteristics					
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 9$	-	3	12	μA
Dynamic ch	aracteristics					_
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 268 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit	-	150	-	V/µs

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	4	А Ы К
2	Α	anode		G sym037
3	G	gate		symosi
4	mb	mounting base; connected to anode	☐1 ☐2 ☐3 SC-73 (SOT223)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
EC103D1W	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223		

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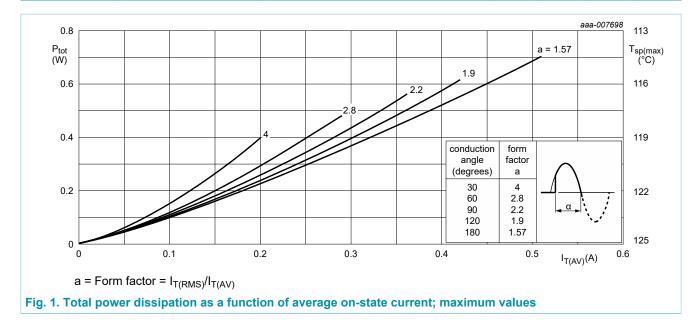
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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	400	V
V_{RRM}	repetitive peak reverse voltage		-	400	V
I _{T(AV)}	average on-state current	half sine wave; T _{sp} ≤ 114 °C; <u>Fig. 1</u>	-	0.5	Α
I _{T(RMS)}	RMS on-state current	half sine wave; T _{sp} ≤ 114 °C; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	8.0	Α
I _{TSM}	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5	-	8	А
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms	-	9	Α
I ² t	I ² t for fusing	t _p = 10 ms; sine-wave pulse	-	0.32	A²s
dl _T /dt	rate of rise of on-state current	$I_T = 2 \text{ A}$; $I_G = 0.01 \text{ A}$; $dI_G/dt = 0.1 \text{ A}/\mu\text{s}$	-	50	A/µs
I _{GM}	peak gate current		-	1	Α
V_{RGM}	peak reverse gate voltage		-	5	V
P _{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	150	°C
T _j	junction temperature		-	125	°C



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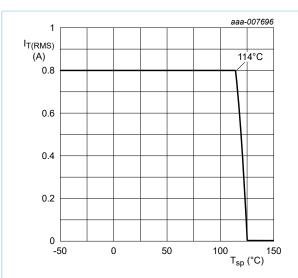


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

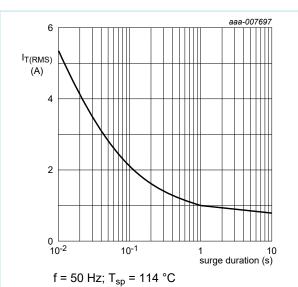


Fig. 3. RMS on-state current as a function of surge duration; maximum values

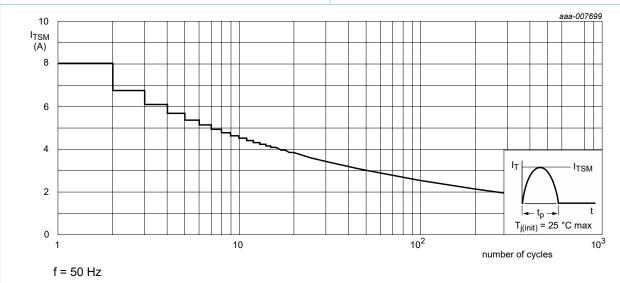
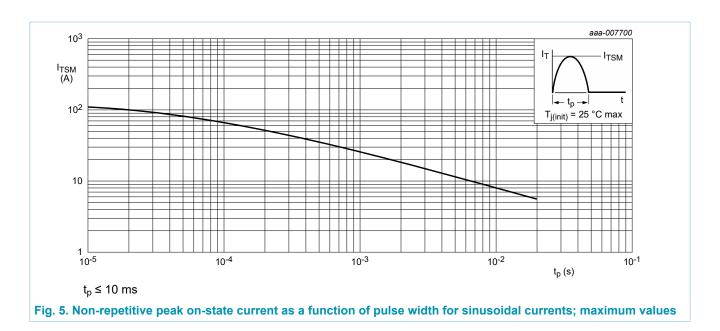


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-sp)}	thermal resistance from junction to solder point	Fig. 6	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to	printed circuit board mounted; minimum pad area; in free air; Fig. 7	-	70	-	K/W
	ambient free air	printed circuit board mounted; minimum footprint; in free air; Fig. 8	-	156	-	K/W

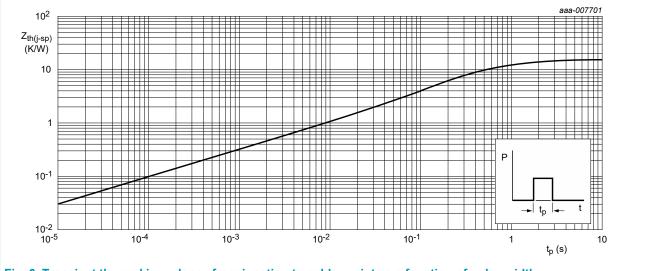
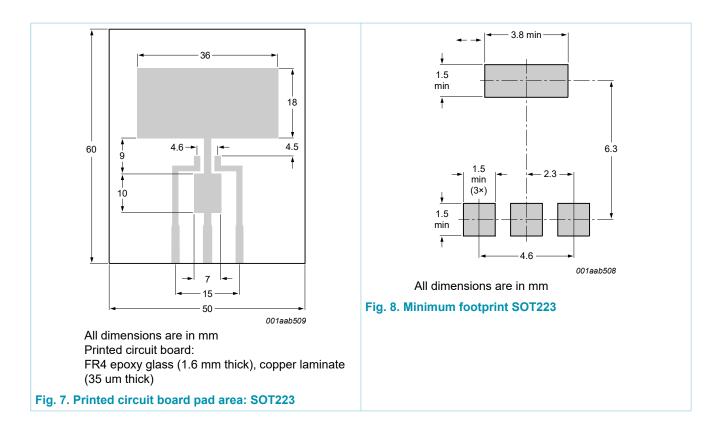


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width

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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics		,			
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 9</u>	-	3	12	μΑ
IL	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 10	-	2	6	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 11</u>	-	2	5	mA
V _T	on-state voltage	I _T = 1 A; T _j = 25 °C; <u>Fig. 12</u>	-	1.2	1.35	V
V _{GT}	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 13	-	0.5	0.8	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 13	0.2	0.3	-	V
I _D	off-state current	V _D = 400 V; T _j = 125 °C	-	0.05	0.1	mA
I _R	reverse current	V _R = 400 V; T _j = 125 °C	-	0.05	0.1	mA
Dynamic ch	naracteristics		'			
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 268 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit	-	150	-	V/µs

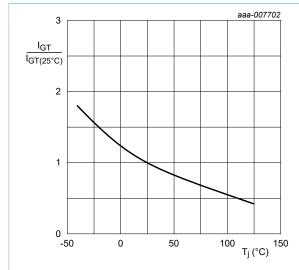


Fig. 9. Normalized gate trigger current as a function of junction temperature

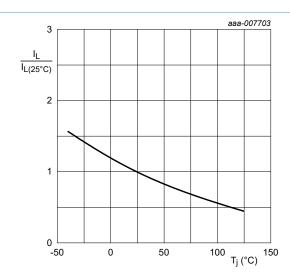


Fig. 10. Normalized latching current as a function of junction temperature

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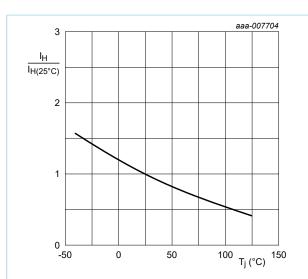
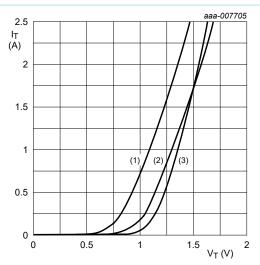


Fig. 11. Normalized holding current as a function of junction temperature



 $V_o = 0.987 \text{ V}; R_s = 0.3125 \Omega$

(1) $T_j = 125$ °C; typical values (2) $T_j = 125$ °C; maximum values

(3) $T_j = 25$ °C; maximum values

Fig. 12. On-state current as a function of on-state voltage

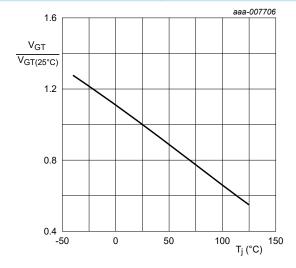
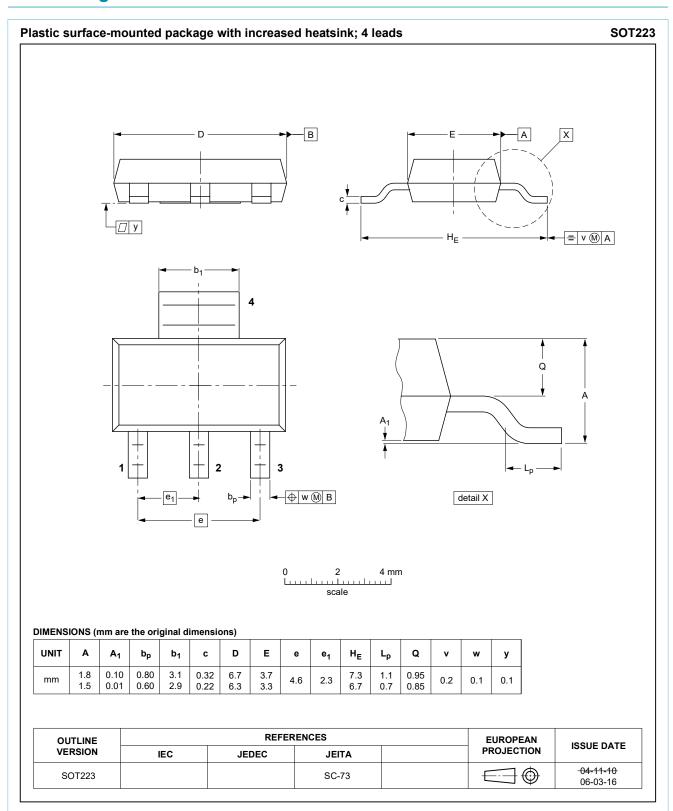


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

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10. Package outline



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11. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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