### **KTFRDMPF1550EVMUG** FRDM-PF1550EVM evaluation board Rev. 2.0 — 7 March 2018

User guide

### 1 FRDM-PF1550EVM



aaa-027028



FRDM-PF1550EVM evaluation board

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### 3 Overview of the PF1550 PMIC development environment

NXP offers a combination of boards that support the evaluation of the PF1550 PMIC.

The FRDM-PF1550EVM boards serve as an evaluation platform that allow users to test and demo designs that incorporate the PF1550 PMIC. The evaluation board contains a preconfigured MC34PF1550 device and provides numerous jumpers and test points that allow users to tailor the evaluation to their needs.

The kit comes with a FRDM-KL25Z already mounted and loaded with compatible microcode. The FRDM-KL25Z's primary function is to control communication between the evaluation board and a PC.

### 4 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state-of-the-art systems.

The tool summary page for FRDM-PF1550EVM is located at <u>http://www.nxp.com/FRDM-PF1550EVM</u>. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, list of (and links to) any related products and a **Get Started** section.

The **Get Started** section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the FRDM-PF1550EVM.

- Go to <a href="http://www.nxp.com/FRDM-PF1550EVM">http://www.nxp.com/FRDM-PF1550EVM</a>.
- On the Overview tab, locate the Jump To navigation feature on the left side of the window.
- Select the Get Started link.
- Review each entry in the **Get Started** section and download an entry by clicking on the title.
- After reviewing the **Overview** tab, visit the other product related tabs for additional information:
  - Documentation: download current documentation
  - Software & Tools: download current hardware and software tools
  - Buy/Parametrics: purchase the product and view the product parametrics

After downloading files, review each file, including the user guide which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

#### 4.1 Kit contents/packing list

The kit contents include:

- Assembled and tested FRDM-PF1550EVM evaluation board in an anti-static bag
- Cable, USB type A male/type mini B male 3 ft
- Quick start guide

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#### 4.2 Required equipment

To use this kit, you need:

- 5.0 V power supply or USB with enough current capability (3.0 A for maximum performance)
- KITPF1550GUI installed on a Windows PC
- Optional voltmeters to measure regulator outputs
- Optional oscilloscope
- Battery pack 3.6 V (Li-ion)

#### 4.3 System requirements

The kit requires the following:

• USB enabled computer running Windows XP, Vista, 7, 8, or 10 (32-bit or 64-bit)

### 5 Getting to know the hardware

#### 5.1 Board overview

The FRDM-PF1550EVM board is an easy-to-use circuit board, allowing the user to exercise all the functions of the PF1550 power management IC.

The FRDM-KL25Z is mounted to the EVB as an integral component and serves as an interface between the KITPF1550GUI and the PF1550 PMIC. The FRDM-KL25Z drives circuitry on the FRDM-PF1550EVM, as well as provides an analog-to-digital convertor (ADC) to allow real-time monitoring of the PF1550 regulator voltages, and display their values in the GUI.

### 5.2 Board features

The board features are as follows:

- PF1550 power management IC
- Integrated FRDM-KL25Z as a communication link between the EVB and a PC
- · One 1.0 Amp ELOAD with configurable current
- NTC Thermistor for temperature measurements (necessary for JEITA compliance)

FRDM-PF1550EVM evaluation board

#### 5.3 Device features

The evaluation board feature the following NXP product:

Table 1.	Fable 1. Device features					
Device	Description	Features				
PF1550	Power management integrated circuit (PMIC) for i.MX 7ULP, i.MX 6SL, 6UL, 6ULL and 6SX processors	<ul> <li>Three adjustable high efficiency buck regulators with 1.0 A per regulator current capability</li> <li>Three adjustable general purpose linear regulators</li> <li>Battery charger (JEITA compliant battery temp. sensing)</li> <li>Input voltage range on VBUSIN: 4.1 V to 6.0 V</li> <li>LDO/switch supply</li> <li>DDR memory reference voltage</li> <li>One time programmable (OTP) memory for device configuration</li> </ul>				

#### 5.3.1 Device description

The PF1550 device populated on board features the A4 OTP. See Table 2.

Register	Pre-programmed OTP configuration – A4 configuration
OTP_VSNVS_VOLT[2:0]	3.0 V
OTP_SW1_VOLT[5:0]	1.1 V
OTP_SW1_PWRUP_SEQ[2:0]	4
OTP_SW2_VOLT[5:0]	1.2 V
OTP_SW2_PWRUP_SEQ[2:0]	3
OTP_SW3_VOLT[5:0]	1.8 V
OTP_SW3_PWRUP_SEQ[2:0]	2
OTP_LDO1_VOLT[4:0]	3.3 V
OTP_LDO1_PWRUP_SEQ[2:0]	1
OTP_LDO2_VOLT[3:0]	3.3 V
OTP_LDO2_PWRUP_SEQ[2:0]	2
OTP_LDO3_VOLT[4:0]	1.8 V
OTP_LDO3_PWRUP_SEQ[2:0]	1
OTP_VREFDDR_PWRUP_SEQ[2:0]	3
OTP_SW1_DVS_ENB	DVS mode
OTP_SW2_DVS_ENB	DVS mode
OTP_LDO1_LS_EN	LDO mode
OTP_LDO3_LS_EN	LDO mode
OTP_SW1_RDIS_ENB	Enabled
OTP_SW2_RDIS_ENB	Enabled
OTP_SW3_RDIS_ENB	Enabled
OTP_SW1_DVSSPEED	12.5 mV step each 4.0 µs
OTP_SW2_DVSSPEED	12.5 mV step each 4.0 µs

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Register	Pre-programmed OTP configuration – A4 configuration
OTP_SWx_EN_AND_STBY_EN	SW1, SW2, SW3 enabled in RUN and STANDBY
OTP_LDOx_EN_AND_STBY_EN	LDO1, LDO2, LDO3, VREFDDR enabled in RUN and STANDBY
OTP_PWRON_CFG	Level sensitive
OTP_SEQ_CLK_SPEED	2 ms time slots
OTP_TGRESET[1:0]	4 secs Global reset timer
OTP_POR_DLY[2:0]	2 ms RESETBMCU power up delay
OTP_UVDET[1:0]	Rising 3.0 V; falling 2.9 V
OTP_I2C_DEGLITCH_EN	I <sup>2</sup> C Deglitch filter disabled
OTP_CHGR_OPER[1:0]	Charger = ON, Linear = ON
OTP_CHGR_TPRECHG	Pre-charge timer = 30 minutes
OTP_CHGR_EOCTIME[2:0]	End-of-charge debounce = 16 secs
OTP_CHGR_FCHGTIME[2:0]	Fast-charge timer disabled
OTP_CHGR_EOC_MODE	Linear ON in the DONE state
OTP_CHGR_CHG_RESTART[1:0]	100 mV below CHGCV
OTP_CHGR_CHG_CC[4:0]	CC = 500 mA
OTP_CHGR_MINVSYS[1:0]	VSYSMIN = 4.3 V
OTP_CHGR_CHGCV[5:0]	CV = 4.2 V
OTP_CHGR_VBUS_LIN_ILIM[4:0]	VBUS ILIM = 1500 mA
OTP_CHGR_VBUS_DPM_REG[2:0]	4.5 V
OTP_CHGR_USBPHYLDO	USBPHY LDO enabled
OTP_CHGR_USBPHY	USBPHY = 3.3 V
OTP_CHGR_ACTDISPHY	USBPHY active discharge enabled

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### 5.4 Board description

Figure 1 describes the main elements on the board.



#### Table 3. Board description

Number	Name	Description
1	1A ELOAD	Electronic load 1.0 A
2	ELOAD CSA	Current sense amplifier for the electronic load
3	PF1550	PF1550 PMIC
4	Analog MUX	Analog multiplexers
5	Battery terminals	Connect battery
6	Thermistor connector	NTC Thermistor (10 k $\Omega$ at 25 °C) connector
7	VBAT CSA	Current sense amplifier for battery current
8	VSYS CSA	Current sense amplifier for VSYS
9	VBUS CSA	Current sense amplifier for VBUSIN
10	VBUS INPUT	USB power supply for the charger
11	ONKEY and PWRON buttons	Buttons connected to the ONKEY and PWRON signals

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### 5.4.1 LED display

The board contains the following LED:



Figure 2. LED locations

#### Table 4. LED locations

LED ID	Description
LED1	Red LED, charge state indicator – behavior of the LED (duty cycle of blinking) is programmable

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### J11 J12 J7 J3 J92 S1 S2 J4 aaa-027031 Figure 3. Jumper and switch locations

Figure 3 shows the location of jumpers and switches on the evaluation board.

Table 5 describes the function and settings for each jumper and switch.

Jumper/Switch	Description	Setting	Connection/Result
S1	ONKEY	Open	Connects ONKEY pin to GND when pressed. Causes wake-up event if configured properly.
S2	PWRON	Open	Connects PWRON pin to GND when pressed. Resets the PMIC device.
J3	5V USB		Power supply for the board (J12 shall be opened)
J4	Pullup configuration	[1-2]	Pullup to VSNVS
		[2-3]	Pullup to VDDIO which is supplied by P3V3 coming from the Freedom board
J7	Battery connection Do not short together	Pin 1	Negative pole of battery
		Pin 2	Positive pole of battery
J11	Thermistor connection	Thermistor connected	Connect NTC thermistor (10 kOhm at 25 °C, example, NXRT15XH103FA1B040)
J12	5V power supply	Open	5V from the J3 (USB) is used
		[1-2]	5V is used from the Freedom board (current is limited)
J92	Battery connection Do not short together	Pin 1	Negative pole of battery
		Pin 2	Positive pole of battery

#### Table 5. Jumper and switch definitions

5.4.2 Jumper and switch definitions

#### 5.4.3 Test point definitions

The following test points provide access to various signals to and from the board.

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#### Table 6. Test point definitions

Test point name	Signal name	Description
TP1	VBUS_PORT	5.0 V power supply (from USB connector J3)
TP2	SW1OUT	Output of the switcher 1
TP3	GND	Ground (next to SW1OUT)
TP4	SW3OUT	Output of the switcher 3
TP5	SW2OUT	Output of the switcher 2
TP6	GND	Ground (next to SW3OUT)
TP7	GND	Ground (next to SW2OUT)
TP19	VSNVS	Output of the VSNVS regulator
TP20	SW1IN	Input of the switcher 1
TP24	VLDO1	Output of the VLDO1 regulator
TP25	SW3IN	Input of the switcher 3
TP29	VLDO2	Output of the VLDO2 regulator
TP30	SW2IN	Input of the switcher 2
TP33	VLDO3	Output of the VLDO3 regulator
TP34	VLD01IN	Input of the VLDO1 regulator
TP35	STANDBY	STANDBY input
TP36	VREFDDR	Output of the VREFDDR regulator
TP37	VLDO2IN	Input of the VLDO2 regulator
TP38	PWRON	PWRON input
TP39	USBPHY	Output of the USBPHY regulator
TP40	VLDO3IN	Input of the VLDO3 regulator
TP41	WDI	Watchdog input from MCU
TP42	LICELL	Coin cell input
TP43	VBATT_SH	Battery voltage (before current shunt)

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Test point name	Signal name	Description
TP44	GND	Ground
TP45	ONKEY	ONKEY push button input
TP46	SDA1	Data signal of the I <sup>2</sup> C-bus
TP47	VINREFDDR	Input of the VREFDDR regulator
TP49	INTB	Interrupt to the MCU
TP50	SCL1	Clock signal of the I <sup>2</sup> C-bus
TP51	GND	Ground
TP52	VSYS_SH	Main input voltage to PMIC and output from charger (after current shunt)
TP53	RESETBMCU	MCU reset signal
TP54	VDDIO	I/O supply voltage of the PMIC
TP59	ELOAD	Electronic load input (connect the tested power supply)
TP63	GND	Ground (next to the electronic load)
TP66	USBPHY	Output of the USBPHY regulator

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#### FRDM-KL25Z Freedom Development Platform 6

The NXP Freedom development platform is a set of software and hardware tools for evaluation and development. It is ideal for rapid prototyping of microcontroller-based applications. The NXP Freedom KL25Z hardware, FRDM-KL25Z, is a simple, yet sophisticated design featuring a Kinetis L Series microcontroller, the industry's first microcontroller built on the ARM<sup>®</sup> Cortex<sup>®</sup>-M0+ core.

#### 6.1 Connecting the FRDM-KL25Z to the board

The FRDM-KL25Z evaluation board was chosen specifically to work with the FRDM-PF1550EVM kit because of its low cost and features. The FRDM-KL25Z board makes use of the USB, built in LEDs and I/O ports available with NXP's Kinetis KL2x family of microcontrollers.

The FRDM-PF1550EVM connects to the FRDM-KL25Z using the four dual row Arduino<sup>™</sup> R3 connectors on the bottom of the board.



Table 7. FRDM-PF1550EVM to FRDM-KL25Z connections						
FRDM-PF1550EVM		F	FRDM-KL25Z		Pin hardware name	
Header	Pin	Header	Pin	FRDM-PF1550EVM	FRDM-KL25Z	Description
J1	1	J1	1	N/C	PTC7	No connection
J1	2	J1	2	INTB	PTA1	Interrupt to the MCU
J1	3	J1	3	N/C	PTC0	No connection
J1	4	J1	4	WDI	PTA2	Watchdog input from MCU
J1	5	J1	5	N/C	PTC3	No connection
J1	6	J1	6	nLDAC	PTD4	DAC configuration signal
J1	7	J1	7	N/C	PTC4	No connection
J1	8	J1	8	RDY/BSY	PTA12	DAC control signal
J1	9	J1	9	N/C	PTC5	No connection

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FRDM-PF1550EVM		FRDM-	<l25z< th=""><th colspan="2">Pin hardware name</th><th></th></l25z<>	Pin hardware name		
Header	Pin	Header	Pin	FRDM-PF1550EVM	FRDM-KL25Z	Description
J1	10	J1	10	MUX_RESETB	PTA4	Multiplexer reset
J1	11	J1	11	N/C	PTC6	No connection
J1	12	J1	12	VDDIO	PTA5	VDDIO Power Supply
J1	13	J1	13	N/C	PTC10	No connection
J1	14	J1	14	SCL2	PTC8	Clock signal of the I <sup>2</sup> C-bus (for additional ICs)
J1	15	J1	15	N/C	PTC11	No connection
J1	16	J1	16	SDA2	PTC9	Data signal of the I <sup>2</sup> C- bus (for additional ICs)
J2	1	J2	1	N/C	PTC12	No connection
J2	2	J2	2	PWRON	PTA13	PWRON input
J2	3	J2	3	N/C	PTC13	No connection
J2	4	J2	4	STANDBY	PTD5	STANDBY input
J2	5	J2	5	N/C	PTC16	No connection
J2	6	J2	6	RESETBMCU	PTD0	MCU Reset signal
J2	7	J2	7	N/C	PTC17	No connection
J2	8	J2	8	VSYS_CSA_ALERT	PTD2	Alert signal from the VSYS's current shunt
J2	9	J2	9	ELOAD_CSA_ALERT	PTA16	Alert signal from the ELOAD's current shunt
J2	10	J2	10	VBAT_CSA_ALERT	PTD3	Alert signal from the VBAT's current shunt
J2	11	J2	11	N/C	PTA17	No connection
J2	12	J2	12	VBUS_CSA_ALERT	PTD1	Alert signal from the VBUS's current shunt
J2	13	J2	13	N/C	PTE31	No connection
J2	14	J2	14	GND	GND	Ground
J2	15	J2	15	N/C	N/C	No connection
J2	16	J2	16	N/C	VREFH	No connection
J2	17	J2	17	N/C	PTD6	No connection
J2	18	J2	18	SDA1	PTE0	Data signal of the I <sup>2</sup> C- bus (PF1550)
J2	19	J2	19	N/C	PTD7	Open
J2	20	J2	20	SCL1	PTE1	Clock signal of the I <sup>2</sup> C-bus (PF1550)
J10	1	J10	1	N/C	PTE20	No connection
J10	2	J10	2	N/C	PTB0	No connection
J10	3	J10	3	N/C	PTE21	No connection
J10	4	J10	4	N/C	PTB1	No connection
J10	5	J10	5	N/C	PTE22	No connection
J10	6	J10	6	2V5_ADC	PTB2	Voltage reference for ADC
J10	7	J10	7	N/C	PTE23	No connection
J10	8	J10	8	ADC_1	PTB3	Analog signal to ADC1

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FRDM-PF1550EVM		FF	FRDM-KL25Z		Pin hardware name	
Header	Pin	Header	Pin	FRDM-PF1550EVM	FRDM-KL25Z	Description
J10	9	J10	9	N/C	PTE29	No connection
J10	10	J10	10	ADC_0	PTC2	Analog signal to ADC0
J10	11	J10	11	N/C	PTE30	No connection
J10	12	J10	12	N/C	PTC1	No connection
J9	1	J9	1	N/C	PTB8	No connection
<b>J</b> 9	2	J9	2	P3V3	SDA_PTD5	3V3 coming from the Freedom board
J9	3	J9	3	N/C	PTB9	No connection
J9	4	J9	4	P3V3	3V3	3V3 coming from the Freedom board
J9	5	J9	5	N/C	PTB10	No connection
<b>J</b> 9	6	J9	6	P3V3	RESET/PTA20	3V3 coming from the Freedom board
J9	7	J9	7	N/C	PTB11	No connection
<b>1</b> 8	8	J9	8	P3V3	3V3	3V3 coming from the Freedom board
J9	9	J9	9	N/C	PTE2	No connection
J9	10	J9	10	P5V_USB	5V	5V coming from the Freedom board
J9	11	J9	11	N/C	PTE3	No connection
J9	12	J9	12	GND	GND	Ground
J9	13	J9	13	N/C	PTE4	No connection
J9	14	J9	14	GND	GND	Ground
J9	15	J9	15	N/C	PTE5	No connection
J9	16	J9	16	NC	P5-9V_VIN	No connection

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### 7 Installing the software and setting up the hardware

#### 7.1 Setup PF1550GUI on your computer

- 1. Download PF1550GUI.zip from <u>http://www.nxp.com/FRDM-PF1550EVM</u>. Choose the 32 or 64 bit version with respect to the system installed on your PC.
- 2. Extract all the files to any desired folder on your PC.
- 3. Plug the evaluation board.
- 4. Launch the GUI (no installation is necessary, GUI can be directly launched by clicking on the file "**PF1550\_GUI.jar**").

# 7.2 Configuring the hardware and using the GUI for control and monitoring



- 1. Apply input voltage to the board.
  - First solution is to use power directly from the FRDM-KL25Z by by connecting J12 jumper. Advantage of this configuration is that you need only one USB port, but this solution may have limited performance (because of the current capability of the USB port).
  - Second possibility is to use power from charger USB input (J3). In this case, keep J12 open. This solution is recommended for higher currents.

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- 2. Plug the mini-USB side of USB cable into the KL25Z USB port on the FRDM-KL25Z board and the other end to an available USB port on the PC.
- 3. Windows automatically installs the necessary drivers. Wait for this to complete.
- 4. Launch the PF1550 GUI.
- 5. In the PF1550 GUI window, click **Scan For Devices** button in the top-left corner. A confirmation message that a valid device is available is logged.

USB Connectio	n				
Vendor ID: Part ID:	0x15A2 0x00D0		Device: PF15	50	
Target Enabled:	<b>V</b>	1	Scan For	Device	s
					*
					Ŧ
Save Log	Clear Lo	g	I2C Address:	80x0	•
				aaa-0	270

- 6. Enable the communication by clicking the **Target Enabled:** checkbox. The window turns from grey to color.
- 7. The GUI installation and hardware setup is now complete.

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### 7.3 Using onboard ELOAD

Onboard electronic load (ELOAD) provides adjustable load current from 0 to 1000 mA in 50 mA steps. The ELOAD is useful for testing supply performance or evaluating a particular PMIC supply rail at a specified load current.

To use the ELOAD, connect a suitable jumper wire (short length with proper gauge) between ELOAD (TP59) and the desired supply VOUT test point. Continuous operation under full load current heats up the EVB. Set the ELOAD back to 0 mA when finished.

Below is an example of a script that demonstrates the use of the ELOAD to test the LDO1 current limit of 150 mA.

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### 7.4 Understanding and using the GUI

#### 7.4.1 GUI structure for PF1550

Figure 7 shows the different components of the GUI.

USB connection status and main log area	PF1550 control tabs
PF1550 GUI	
USB Connection	Switching Supplies Linear Supplies Charger OTF Configuration Miscellaneous Interrupts Script Editor Charge Plot Discharge Plot Functional Registers OTF Registers
UB connection Verdor Do dal-S2 Perdor P1350 Parts: boots of the second o	sextenders Specifie (Lever Specifie (Compering Heredinense) Meredinense), Specifie (Comper Here] (Execting Her
Direct I2C / communication dialog	aaa-027037
Figure 7. GUI components	

#### 7.4.2 GUI panels

When the GUI is launched, it looks for a PF1550 target board connected via the USB cable. If connected, the USB Connection panel displays the Vendor ID: 0x15A2, and Part ID: 0x00D0.

The Main Log window displays messages, example, when the board is connected (PF1550 attached) and when the board was removed (PF1550 removed).

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USB Connection Vendor ID: 0x15A2 Device:	Switching Supplies Linear	Supplies Charger 01	and a second second				
Vendor ID: 0x15A2 Device:			P Configuration Miscellan	eous Interrupts Script Edi	tor Charge Plot Dischar	ge Plot Functional Registers OT	P Registers
	SW1 FUNCT	IONAL	SW2 FUNC	TIONAL			
Part ID: 0x00D0	Vout: •	► 0.6000 V	Vout:	► 0.6000 V	Vin		
Click to Enable Target:	Vstby:	► 0.6000 V	Vstby: 4	► 0.6000 V	የ		
	Vslp: 🔸 🔚	► 0.6000 V	Vslp: 🔫 📃	► 0.6000 V			
*	Supply Enabled:		Supply Enabled:				
	Standby Enabled:		Standby Enabled:		- +	IN SWI	
	LPM Enabled:		LPM Enabled:			VOUT: 0.6000 V FPWM:	DFF ILim = 1.0 A
	OMODE Enabled:		OMODE Enabled:			VSLP: 0.6000 V STDBY: VSLP: 0.6000 V LPM:	OFF
	DVS Speed:	6.250 mV/us	DVS Speed:	6.250 mV/us		DVS: 6.250 mV/us OMODE:	OFF
	DVS Tracking Enabled:		DVS Tracking Enabled:				
	FPWM Enabled:		FPWM Enabled:				
	RDischarge Disabled:		RDischarge Disabled:				
	ILimit: •	▶ 1.0 A	ILimit: • 🔅 💷	+ 1.0 A		SW/2	
		Update		Update	- +	IN SW2	
Save Log Clear Log I2C Address: 0x08 •	SW3 FUNCT	IONAL	ELOAI			VSTBY: 0.6000 V STDBY: VSLP: 0.6000 V LPM: DVS: 6.250 mV/us OMODE:	DFF DFF
	Vout: •	▶ 1.8000 V	Voltage	Current			
Direct I2C Communication	Vstby: •	► 1.8000 V	0.000 V 0	A 000 A			
	Vslp: •	▶ 1.8000 V	EN: DISET: 0	⊻ mA			
I2C Byte Read/Write Mode	Supply Enabled:			Update			·B <b>4</b>
Register: 0x00 Read @ FUNC	Standby Enabled:					IN SW3	
Data: 0x00 Write OTP	LPM Enabled:					VOUT: 1.8000 V FPWM:	DFF ILim = 1.0 A
	OMODE Enabled:					VSTBY: 1.8000 V STDBY:	DFF
Device State	PPWM Enabled:					OMODE:	DFF
	Nuischarge Disabled:						
	itimic •	, 10A					
Ruild: 0.1		Update					

#### Figure 8. GUI startup

Pressing the **Scan For Devices** button attempts to read from each of the eight permissible I<sup>2</sup>C device addresses, and displays the results in the Main Log window. If multiple PMIC devices are detected, the GUI can be configured to communicate with a particular device by selecting the corresponding device address in the I<sup>2</sup>C address list.

Note: The GUI can communicate with only one PMIC device at a time.

<pre>Mark &amp; value &amp; va</pre>	nder ID 0-1552 Device 051550	SW1 FUNCTIONAL	SW2 FUNCTIONAL	
sept Enabled: V Mbp:   Conditionance V Mbp:   V Mbp: 1 2005 V   Sendly Enabled: 1 2005 Finabled:   DVD Enabled: 1 2005 V   V Mbp: 2 20 A   V Mbp: 1 2007 V   V Mbp: 2 20A   V Mbp: 1 2007 V   V Mbp: 1 2007 V <th>art ID: 0x00D0</th> <th>Vout: ( 13875 V</th> <th>Vout: &lt;</th> <th>Vin</th>	art ID: 0x00D0	Vout: ( 13875 V	Vout: <	Vin
See Log Concession       Value       Value </th <th>unet En ablant 💷 Euro Euro Daniana</th> <th>Vetby: 4 1.3875 V</th> <th>Vetby: &lt; III + 1.3500 V</th> <th>Ŷ</th>	unet En ablant 💷 Euro Euro Daniana	Vetby: 4 1.3875 V	Vetby: < III + 1.3500 V	Ŷ
Sund device Mith. #Stream: 0x00       Supply finabled.       Sundy finabled.       Sundy finabled.         Sundy finabled.       Sundy finabled.       Sundy finabled.       Sundy finabled.         OUX00 E finabled.       OUX00 E finabled.       OUX00 E finabled.       Sundy finabled.         Since Log.       DC S Speed.       OUX00 E finabled.       OUX00 E finabled.         Since Log.       DC Address:       OUX00 E finabled.       Finabled.         Since Since       OUX00 E finabled.       Finabled.       Finabled.         Since Log.       DC Finabled.       Finabled.       Finabled.         Since Since       OUX00 E finabled.       Finabled.       Finabled.         Dide Since Since       Finabled.       Finabled.       Finabled.         Since Si	arget chables:	Vslp: ( 1.3875 V	Vslp: <	
Survey Foundated V Survey Founda	ound device with address: 0x08	Supply Enabled:	Supply Enabled:	FB TOTOL
UPM Easlete:       UPM Easlete: <td< th=""><th></th><th>Standby Enabled:</th><th>Standby Enabled:</th><th></th></td<>		Standby Enabled:	Standby Enabled:	
ONODE Facilità     ONODE Facilità       ONODE Facilità     ONODE Facilità       ONODE Facilità     ONODE Facilità       FPMA facilità     Innic 4       Update     Dis Tracing Endeta:       FPMA facilità     Innic 4       Update     Voltage Curret       Voltage Curret     Voltage Curret       Voltage Curret     Voltage Curret       Voltage Curret     Nonce Endeta       PMM facilità     Innic 4       Voltage Curret     Voltage Curret       Voltage Curret     Voltage Curret       Voltage Curret     Voltage Curret       Voltage Curret     PMM facilità       PMM facilità     Innic 4       Voltage Curret     Voltage Curret       Voltage Curret		LPM Enabled:	LPM Enabled:	VOUT: 1.3875 V FPWM: OFF ILim = 2.0 A
D05 Specie:     V 23 Specie:     V		OMODE Enabled:	OMODE Enabled:	VSTBY: 1.3875 V STDBY: ON VSLP: 1.3875 V LPM: OFF
D05 Tacking Evablet     D05 Tacking Evablet       D06 Evablet     FFWA Evablet       Evablet </td <td></td> <td>DVS Speed: 📝 3.125 mV/us</td> <td>DVS Speed: 🕑 3.125 mV/us</td> <td>DVS: 3.125 mV/us OMODE: OFF</td>		DVS Speed: 📝 3.125 mV/us	DVS Speed: 🕑 3.125 mV/us	DVS: 3.125 mV/us OMODE: OFF
FPWM Enable:     FPWM Enable:     FPWM Enable:       Swe Leg:     Cammacizie     Lippine       Swe Leg:     Cammacizie     Lippine       Swe Leg:     Cammacizie     Value:     113000V       Swe Leg:     Cammacizie     Value:     11300V       Value:     11300V     Stable:     Notes       Doi:     Comment     0000 A     Notes       Value:     11300V     Stable:     Notes       Doi:     Comment     Stable:     Notes       Doi:     000     Wate:     1200V       Value:     1200V     Stable:     Notes       Doi:     Comment     Stable:     Notes       Doi:     Stable:     Notes     Notes       Stable:     File     Stable:     Notes		DVS Tracking Enabled:	DVS Tracking Enabled:	
Rotecharge Dualstef:     Image: Standing       Image: Dec Address:     0.000       Serve Log:     Dec Address:       Orient LOC Communication     Variation       Variation     11.0000 V		FPWM Enabled:	FPWM Enabled:	
Save Log     Eckele     * 20 A       Save Log     Communication       Direct I2C Communication     Votage       Votage     * 10000       Votage     * 1		RDischarge Disabled:	RDischarge Disabled:	
Image: Current Opdate     Image: Current Opdate       Sevelog: Cextog: CAddress: 0/08 +     Sovi 110h-C100hdl       Voti: \$\$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$		ILimit:	ILimit: <	SW2 FB 0000
weeteng         Certeng         CAddress         0.000         Fill 4000           Weeting         Center         1.0000         Votes         0.000 A           Direct 12C Communication         Votes         0.000 A         0.000 A           Votes         0.000 A         0.000 A         0.000 A           Votes         0.000 B         0.000 A         0.000 A           Votes         0.000 A         0.000 A         0.000 A <th></th> <th>Update</th> <th>Update</th> <th></th>		Update	Update	
Since Log         Clear Log         CL Address         Out         It is 000         Voits # 0000         It is 000         Voits # 0000 A         It is 000 A         Voits # 0000 A         It is	*			VOUT: 1.3500 V FPWM: OFF ILm = 2.0 A
Note (s)         Carlos (s)         Carlos (s)         Consection           Viste (s)         Vaty (s)         118000 V         Vaty (s)         0000 A           Viste (s)         Vaty (s)         118000 V         00000 A         000           Viste (s)         Carlos (s)         0000 V         00000 A         000           Viste (s)         Supply Enabled:         Vaty (s)         0000 V         00000 A           Viste (s)         Standy Chalted:         Vaty (s)         Vaty (s)         Vaty (s)         Vaty (s)           Device State         OHODE Enabled:         FWM Enabled:         Vaty (s)	Control Charles Decautors 0.02 =	SW3 FUNCTIONAL	ELOAD	VSLP: L3500 V LPM: OFF
Direct I2C Communication         Value         Image: Particular State         Odde         Odd	Save Log Clear Log I2C Address: 0000 +	Vout: + 1.8000 V	Voltage Current	DVS: 3.125 mV/us OMODE: OFF
B2C Dyte Read/Wirke     Mode     Wole     Image: mail and the second stability       Register     0.00     Read     # FINA       Obter     0.00     Write     0.00       Write     0.00     Write     0.00       Detec     0.00     Write     0.00       PMM Endabled     Image: mail and the second stability     0.00       PWM Endabled     Image: mail and the second stability     0.00       StANDBY     Endet the second stability     1.00       Bable 0.1     Update     0.00	lirect I2C Communication	Vstbv: + I.800 V	A 000.0 V 0.000 A	÷
QC Dyle Read Winte         Mode         Supply Enabled         Update           Register         0:00         Read         # FUNC         Standby Chabled         Update           Dete:         0:00         Write         Off         Control (Fabled)         FUNC         Function (Fabled)           Dete:         0:00         Write         Off         FUNC         Function (Fabled)         Funct		Vslp: +	EN: ISET: 0 v mA	
Register:         0.00         Pard         FRUNC         Stonday Dabled:         IN         SW3         LX           Dobi:         0.00         Write:         0.00         Visit:         IN         SW3         LX           Device:         0.00         Write:         IN         SW3         LX         Visit:         No         Visit:         No         SW3         LX         Visit:         SW3         LX         SW3         LX         LX         SW3         LX	C Byte Read/Write Mode	Supply Enabled:		
Data:     0.00     Write     OTP     LPM Enabled:     0.000 Enabled: <t< th=""><th>egister: 0x00 Read @ FUNC</th><th>Standby Enabled:</th><th>opone</th><th>swa in month and</th></t<>	egister: 0x00 Read @ FUNC	Standby Enabled:	opone	swa in month and
OMODE Enabled:     WOULT 12000 V     Prove ON V       Device State     PFWM Enabled:     VUUT 12000 V     VUUT 12000 V       Device State     PFWM Enabled:     VUUT 12000 V     VUUT 12000 V       STANDEY     Line:      20 A       Baste: 0.1     Update	ata: 0x00 Write OTP	LPM Enabled:		IN IN 3,300 V
Device State     FPWM finalshite     VSLP L000 V     LPRA OFF       STANDBY     Link (      OMODEL OFF       Bulke 0.1     Update		OMODE Enabled:		VSTBV: 1.8000 V STDBY: ON
STANDBY Lish: Diskharge Disabled: Diskoharge Diskoharge Disabled: Diskoharge Di		FPWM Enabled:		VSLP: 1.8000 V LPM: OFF
STANDBY Limit: ( ) 20A	levice State	RDischarge Disabled:		OMODE OFF
Bude 0.1 Update	TANDBY	ILimit: 4		=
	uild: 0.1	Update		

#### 7.4.3 Switching Supplies panel

The Switching Supplies panel allows users to adjust the functional parameters of each supply.

```
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```

#### FRDM-PF1550EVM evaluation board



To change supply parameters, click and adjust the desired control. An **UPDATE** button appears whenever a change is made, and pressing the **UPDATE** button writes the change to the PMIC.

**Note:** Multiple changes can be made at a time, and all changes are written when the **UPDATE** button is pressed.

#### 7.4.4 Linear Supplies panel

The Linear Supplies panel allows users to adjust the functional parameters of each linear regulator. To change supply parameters, click and adjust the desired control.

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An **UPDATE** button appears whenever a change is made, and pressing the **UPDATE** button writes the change to the PMIC.

**Note:** Multiple changes can be made at a time, and all changes are written when the **UPDATE** button is pressed.

#### 7.4.5 Charger panel

The charger panel contains all the functions dedicated to the battery charging and monitoring.

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#### 7.4.6 OTP Configuration panel

The OTP Configuration panel allows access and editing of the PF1550 startup parameters.

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MIC CHARGER									
VSTEM SWI SWZ	SW3 LINA UN2				PF15	50 POWER UP	TIMING		
OTP SYSTE	M PARAMETERS								
PWRON Configuration	IT LEVEL SEN	SITIVE	OFF	Vout: 0.6000 V DVS	Ramp: 6.250 us				
Sequencer Clock:	0.5	• ms		SEQ Delay: 0 ms					
Enter Fault Mode	E1		-						
2C Address:	0,408	•							
N Det. Threshold	3.0 V   2.9 V		OFF	Vent: 0.8000 V DVS	Ramp: 6.250 us				
POR Delays	2	→ ms	and a	SEQ Delay: U ma					
leset Timer.	4	• s							
		Updat	1						
			OFF	Veut: 1.8000 V					
				SQ Delay10 mi					
				~					
			OFF	Vout: 0.7500 V					
				sequency: o ms					
				100					
			OFF	Vout: 1.8500 V					
				Sequences and					
				140					
			2010	O SED Dalard mr.					
				and the second					
			211113	6 SEQ Delay: 0 ms					
						2.0			
						TIME (ms)			
			Clear CFG	Load CFG File Load Fr	om PMIC	Save CFG File	Generate Repo	a.	
			Constant State State	a consideration of the same	Construction of Construction o	Antersteinsteinen	Annecio de Societado	054	

#### Figure 13. OTP Configuration panel

Initially, the panel display is greyed out. To populate the panel, press **Edit Configuration**, and select a data source to read from.

The **Load CFG File button** opens the Configuration File Open dialog, and populates the panel with the parameters contained in this file.

The **Update From Target** button loads the OTP configuration data from the target evaluation board.

#### 7.4.7 Miscellaneous panel

The Miscellaneous panel contains general purpose commands and power down sequencing configuration.

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#### 7.4.8 Interrupts panel

The Interrupts panel displays the state of all PF1550 interrupts.



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The **Interrupts** tab displays status, mask, and sense registers for INT0, INT1, INT3, and INT4. Selecting the Poll Interrupts checkbox enables update of this information with period of 500 ms. To activate interrupt, the appropriate mask has to be set. When an interrupt occurs, the appropriate checkbox is selected. Interrupt can be then cleared by unchecking this checkbox.

The state of the PF1550 INTB pin is displayed, and updated asynchronously. Interrupts that are unmasked, causes the INTB pin to go LOW while the interrupt condition exists.

The PF1550 target hardware detects when the INTB pin goes LOW, and sends a message to the GUI to indicate that an interrupt has occurred. The INTB label on the panel flashes until the interrupt condition is cleared.

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#### 7.4.9 Script Editor panel

The Script Editor panel allows the user to write and execute scripts that exercise various functions on the PF1550 PMIC, including setting voltages on the regulators, reading and writing I<sup>2</sup>C addresses, and clearing interrupts. Script commands can be written directly in an editor window. Alternatively, the user can build the scripts by selecting commands from drop-down menus and entering the appropriate values.

The scripts are executed within the **Files:** section of the panel and the results are displayed in the **Script Log** section.

Completed scripts can be saved as text files for later use. Commands can be generated easily.



Figure 16 shows the main elements in the Script Editor panel.

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#### 7.4.10 Charge Plot panel

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#### 7.4.11 Discharge Plot panel

#### 7.4.12 Functional Registers panel

In the Functional Registers panel, clicking on a checkbox immediately sets or clears the corresponding register bit. Key bit-fields in each register are decoded to assist in displaying the actual state of each parameter.

Registers are grouped within each tab by function.

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IISC 1	MISC 2	INT 1 INT 2	SW1 S	V2 SW3	SW PD SEQ	LIN1	LIN2 LIN PE	D SEQ CHG1	CHG2	CHG3 CHG4
DDRESS				COINCEL	L CONTROL					Coincell charging vol. = 1.8 V Coincell charger = disabled
0x30	D7	D6	05 🔳 🕻	14	] D3 [	D2	🗖 D1	🗖 D0	0x00	
PAGEO			CHEN	vcc	DIN3 V	COIN2	VCOIN1	VCOIN0		
DDRESS				POWER	CONTROL 0					Standby pin delay = no delay Standby pin polarity = high RESETBMCU pin delay = no delay
0x58	🗌 D7	🕅 D6	D5	D4	D3	D2	D1	🕅 D0	0x00	UNKEY IOW duration = 4
PAGE 0	TGRST1	TGRST0	PORDLY2	PORDLY1	PORDLYO	STBINV	STBDLV1	STBDLY0		
DDRESS				POWER	CONTROL 1					PWRON debounce = 31.25   31.25 ms ONKEY debounce = 31.25   31.25 ms REGS_DISABLE or Sleep mode = disabled System restart on PWRON low = disabled
0x59	D7	<b>D</b> 6	D5	D4	D3	D2	D1	<b>D</b> 0	0x00	LDO shut down = disabled Turn off via ONKEY = disabled
PAGE 0	OKEYRST	SCP	RST	PONRST	ONKEY1	ONKEYO	PWRON1	PWRON0		UVDET through a ld = 2.0 V L 2.0 V
DDRESS				POWER	CONTROL 2					Low SYS warn. threshold = 3.3 V   3.1 V
0x5A	D7	D6	D5 🔄 D	4 🔳 🖸	13	D2	D1	D0	0x00	
PAGE 0				LOWS	IS1 LOV	VSYS0	UVDET1	UVDET0		
DDRESS				POWER	CONTROL 3					GOIO_SHIP mode = disabled CORE_OFF mode = disabled
0x5B	D7	D6	D5	D4	D3	D2	🗖 D1	D0	0x00	
PAGEO							COREOFF	SHIP		

#### 7.4.13 OTP Registers panel

The OTP Registers panel provides bit-level access to each register.

Sw	/itching Sup	plies Linear Supplies	Charger (	OTP Configuration	on Miscellane	ous Interrupts	Script Editor	Charge Plot	Discharge	Plot Functional Registers OTP Registers	
	MISC SL	JP1 SUP2 CHG1	CHG2	CHG3							
	ADDRESS			OTP PMIC	CONFIGURATIO	0 M 0				Power On Configuration = level sensitive SEQ CLK SPEED = 0.5 ms Enter fault mode = disabled	l
	0x1C	D7 D6	D5	D4	🗂 D3	D2	D1	D0	0x00		
	PAGE 0			P	WRGDEN	CLK	PWRON				
	ADDRESS			OTP PMIC	CONFIGURATIO	DN 1				Reset delay on ONKEY press = 4 POR delay = no delay UV detection threshold = 3.0 V   2.9 V	
1	0x24	D7 D6	🗖 D5	D4	D3	D2	🗖 D1	D0	0x00		
	PAGE 0	UVDET1	UVDET0	PORDLY2	PORDLY1	PORDLYD	TGRST1	TGRST0			
	ADDRESS			OTP PMIC	CONFIGURATIO	DN 2				VREFDDR power up sequence = 0 I2C deglitch = disabled I2C address = 0x08	
1	0x28	D7 D	5 📃 I	D5 🗖 D4	🗖 D3	🕅 D2	🕅 D1	D0	0x00	Ship core off = disabled	
	PAGE 0	COFF I2CA2	I2CA1	I2CA0	12CEN	VREFUP2	VREFUP1	VREFUP0			
1	ADDRESS	S OTP CRC									
	0x37	D7	D6	D5	D4 🗌 D3	🗌 D2	🗌 D1	D0	0x00		
	PAGE 0	CRCLSB									
										aaa-027	'050
-											
F	igure :	20. UTP Re	egistei	rs panel							

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Bits can only be changed after the Edit Configuration has been pressed.

Clicking on a checkbox immediately sets or clears the corresponding register bit. Key bit-fields in each register are decoded to assist in displaying the actual state of each parameter.

Registers are grouped within each tab by function.

While in Edit Configuration (TBB mode), the OTP data import, export, and compare buttons are visible. The buttons function the same as those on the OTP Configuration panel.

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### 8 Schematics, board layout and bill of materials

The board schematics, board layout and bill of materials are available at <u>http://</u>www.nxp.com/FRDM-PF1550EVM on the Overview tab under Get Started.

### 9 References

The following URLs reference related NXP products and application solutions:

NXP.com support pages	Description	URL
FRDM-PF1550EVM	Tool summary page	http://www.nxp.com/FRDM-PF1550EVM
PF1550	Product summary page	http://www.nxp.com/PF1550
FRDM-KL25Z	Freedom Development Platform	http://www.nxp.com/FRDM-KL25Z

### 10 Revision history

<b>Revision histo</b>	Revision history								
Rev	Date	Description							
v.2.0	20180307	<ul> <li>Updated Section 4</li> <li>Deleted Jump start</li> <li>Updated Table 2</li> <li>Updated Table 6</li> <li>Updated Figure 17 and Figure 18</li> </ul>							
v.1.0	20170616	Initial version							

#### FRDM-PF1550EVM evaluation board

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FRDM-PF1550EVM evaluation board

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