

# DATA SHEET

## **74F257A**

Quad 2-line to 1-line selector/multiplexer,  
non-inverting (3-State)

Product specification

1995 Mar 31

IC15 Data Handbook

Philips Semiconductors



**PHILIPS**

# Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State)

## 74F257A

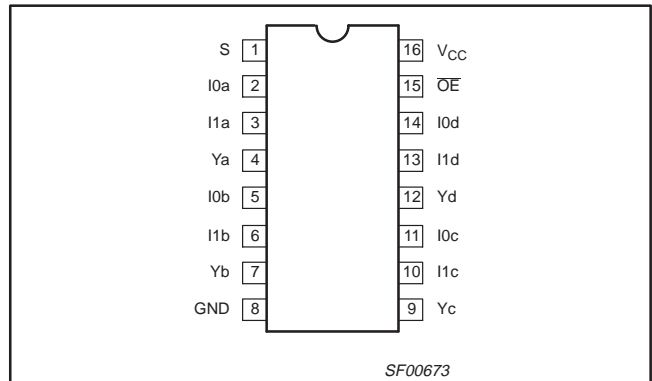
### FEATURES

- Industrial range available (−40°C to +85°C)
- Multifunction capability
- Non-inverting data path
- 3-State outputs
- See 74F258A for inverting version

### DESCRIPTION

The 74F257A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I0a inputs are selected when the common Select input is Low and the I1n inputs are selected when the common Select input is High. Data appears at the outputs in true non-inverted form from the selected inputs. The 74F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the common Select input. Outputs are forced to a high impedance “off” state when the Output Enable ( $\overline{OE}$ ) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum rating if the outputs were tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices were tied together.

### PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F257A	4.3ns	12mA

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE		DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
16-pin plastic DIP	N74F257AN	I74F257AN	SOT38-4
16-pin plastic SO	N74F257AD	I74F257AD	SOT109-1

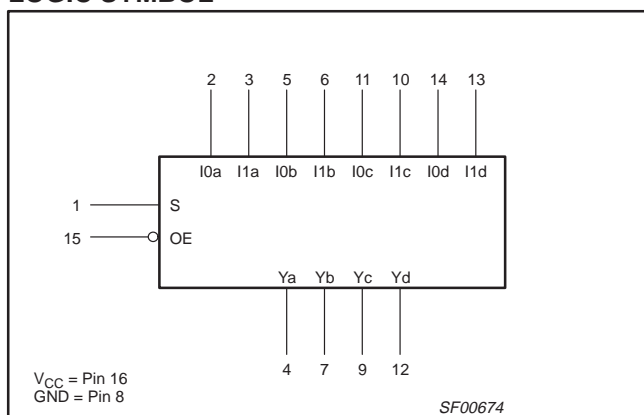
### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0n, I1n	Data inputs	1.0/1.0	20μA/0.6mA
S	Common Select input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20μA/0.6mA
Ya – Yd	Data outputs	150/33	3.0mA/20mA

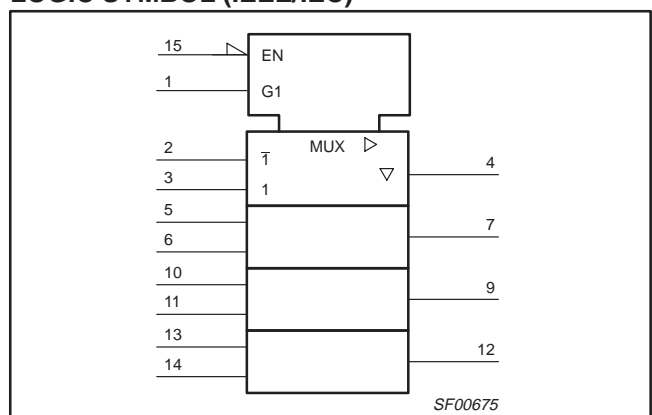
#### NOTE:

One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

### LOGIC SYMBOL



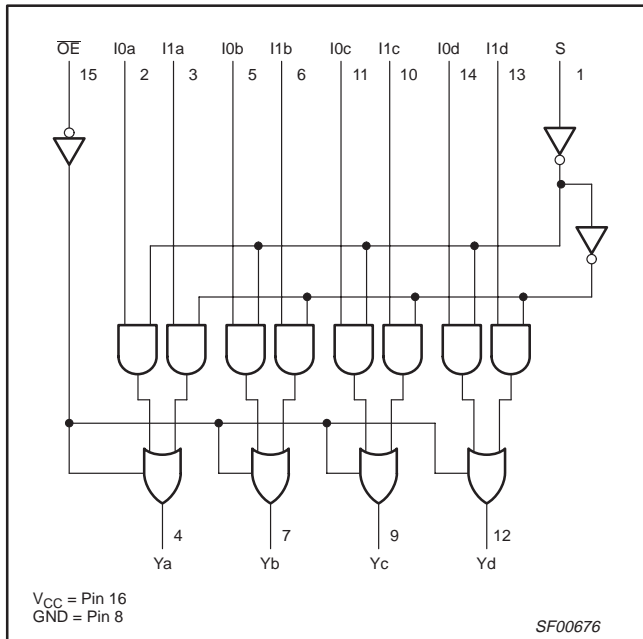
### LOGIC SYMBOL (IEEE/IEC)



# Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State)

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## LOGIC DIAGRAM

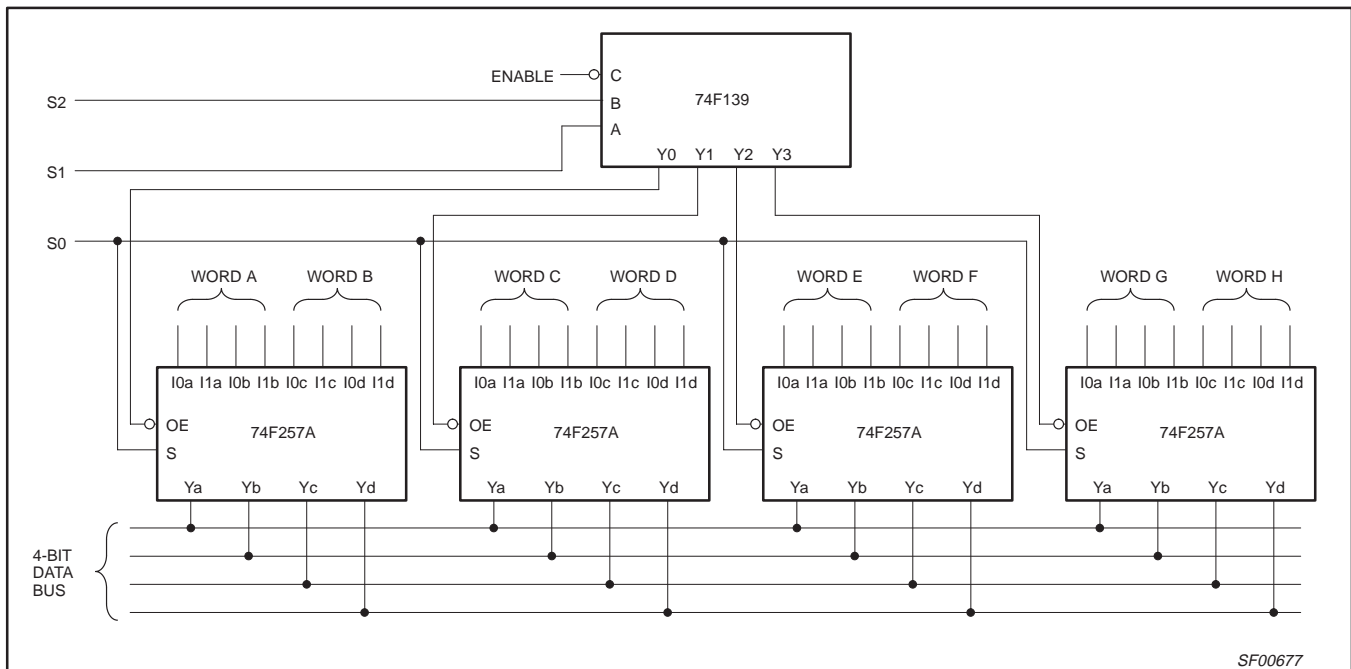


## FUNCTION TABLE

INPUTS				OUTPUT
OE	S	I0	I1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "off" state

## APPLICATION



# Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State)

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## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage		-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage		-0.5 to +7.0	V
I <sub>IN</sub>	Input current		-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state		-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state		48	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-3	mA
I <sub>OL</sub>	Low-level output current			24	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

# Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State)

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.4		V	
			±5%V <sub>CC</sub>	2.7	3.3	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.35	0.50	V
			±5%V <sub>CC</sub>		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-0.6	mA	
I <sub>OZH</sub>	Off state output current, High-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V			50	μA	
I <sub>OZL</sub>	Off state output current, Low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V			-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-60		-150	mA	
I <sub>CC</sub>	Supply current <sup>4</sup> (total)	V <sub>CC</sub> = MAX	I <sub>CCH</sub>		9.0	15.0	mA
			I <sub>CCL</sub>		14.5	22.0	mA
			I <sub>CCZ</sub>		15.0	23.0	mA

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Measure I<sub>CC</sub> with all outputs open and inputs grounded.

## AC ELECTRICAL CHARACTERISTICS

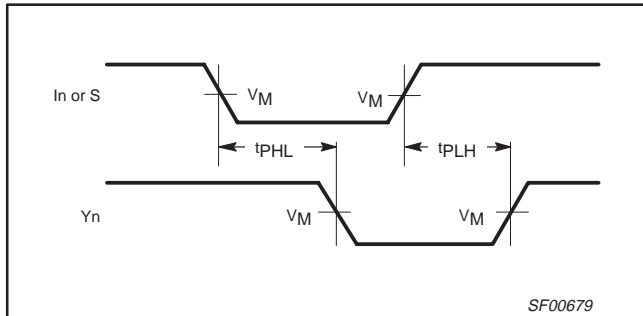
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		T <sub>amb</sub> = -40°C to +85°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to Y <sub>n</sub>	Waveform 1	3.0 2.0	4.5 3.5	6.0 5.0	3.0 2.0	7.0 6.0	3.0 2.0	7.0 7.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S to Y <sub>n</sub>	Waveform 1	5.0 4.0	7.5 5.5	9.5 7.0	5.0 4.0	10.5 8.0	5.0 4.0	10.5 8.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level	Waveform 2 Waveform 3	4.5 4.5	6.5 6.0	7.5 7.5	4.5 4.5	8.5 8.5	4.5 4.5	8.5 8.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.0 6.0	2.0 2.0	6.0 6.0	ns

# Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State)

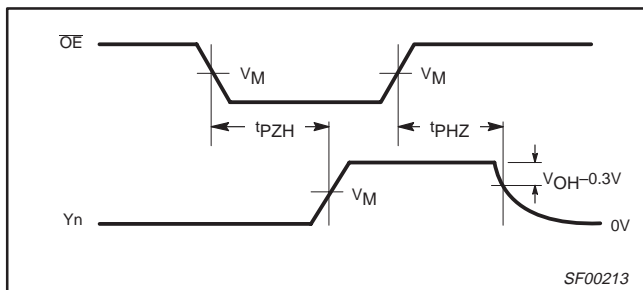
74F257A

## AC WAVEFORMS

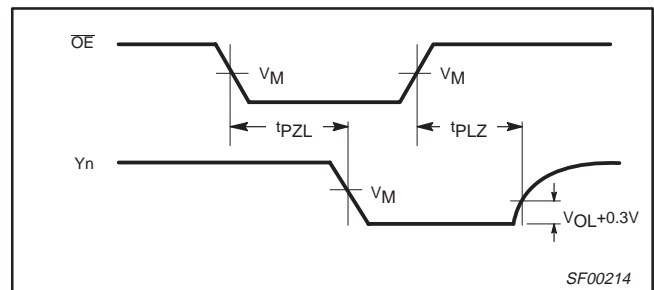
For all waveforms,  $V_M = 1.5V$ .



Waveform 1. Propagation Delay, Data and Select to Output



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**Input Pulse Definition**

INPUT PULSE REQUIREMENTS						
family	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

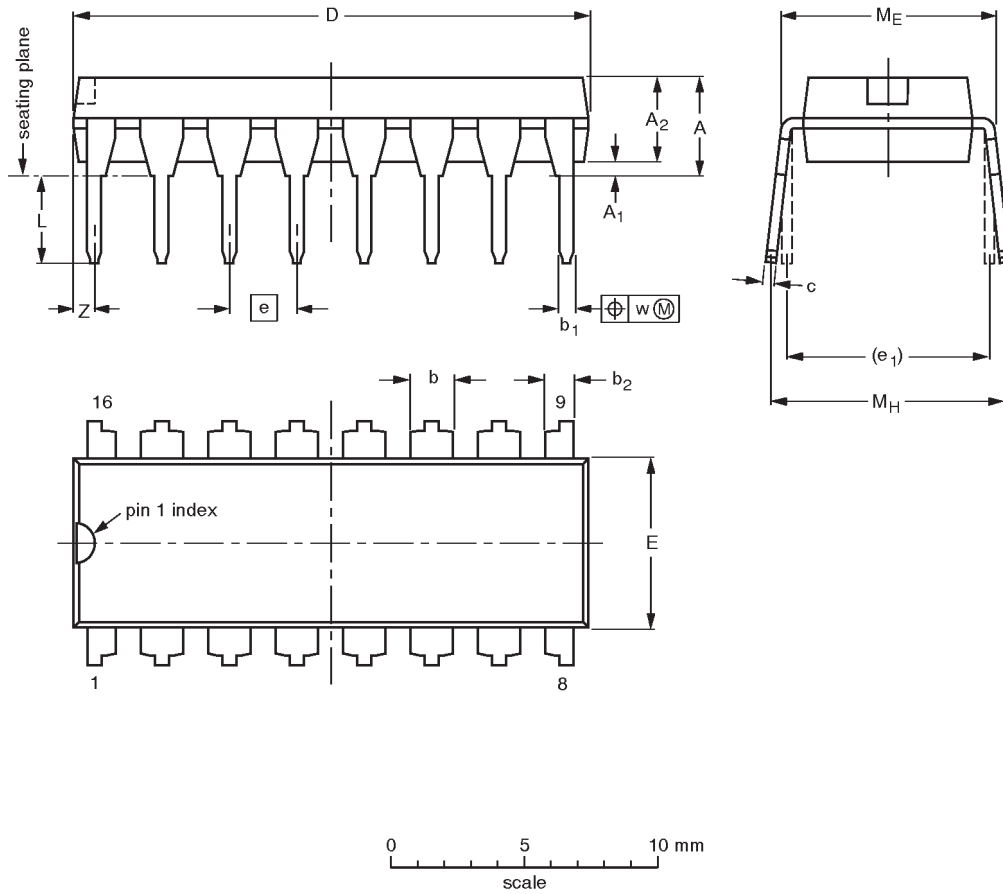
SF00777

Quad 2-line 1-line selector/multiplexer, non-inverting (3-State)

74F257A

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

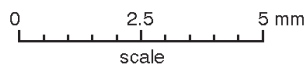
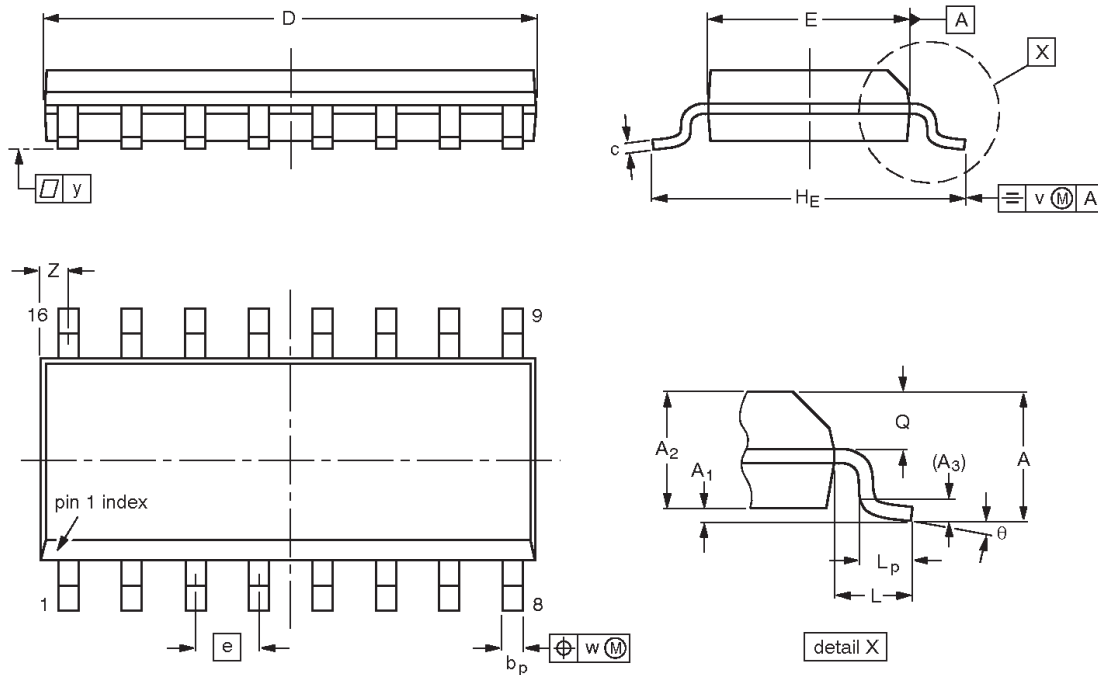
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

Quad 2-line 1-line selector/multiplexer, non-inverting (3-State)

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22



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Quad 2-line 1-line selector/multiplexer, non-inverting (3-State)

74F257A

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**NOTES**

## Quad 2-line 1-line selector/multiplexer, non-inverting (3-State)

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	<b>Full Production</b>	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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**811 East Arques Avenue**  
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**Sunnyvale, California 94088-3409**  
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