**User manual** 



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# 1 Introduction

This document is the user guide for the KITFS85AEEVM evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of FS8500 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS8500 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITFS85AEEVM enables development on FS84/FS85 family of devices. The kit can be connected to the FlexGUI software which allows you to play with registers, try OTP configurations, and burn the part.

This kit is suitable for truck application running at 24 V nominal. It is able to sustain up to 60 V at  $V_{\text{BAT}}.$ 

It is delivered with empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. Burning the OTP three times, gives a good flexibility. The board contains a superset device (MC33FS8530AE0S), allowing tests on all the FS84/ FS85 derivatives.

# 2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <u>http://www.nxp.com</u>.

The information page for KITFS85AEEVM evaluation board is at <u>http://www.nxp.com/</u> <u>KITFS85AEEVM</u>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS85AEEVM evaluation board, including the downloadable assets referenced in this document.

## 2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

# 3 Getting ready

Working with the KITFS85AEEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

#### 3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm

• Jumpers mounted on board

### 3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

• Power supply with a range of 8.0 V to 60 V and a current limit set initially to 1.0 A

## 3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7 or Windows 10

#### 3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at <u>http://www.nxp.com/</u><u>KITFS85AEEVM</u> or from the provided link.

- FlexGUI latest version
- FS85\_FS84\_OTP\_Config.xlsm
- Java installation <a href="https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html">https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</a>

## 4 Getting to know the hardware

The KITFS85AEEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU installed on the board, combined with the FlexGUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signal, like DC/DC switcher node is mapped on test points. Digital signals (SPI, I2C, RSTB, etc.) are accessible through connectors. Pin WAKE1 has a switch to control (Ignition) them. A VBAT switch is available to power On or Off the device.

This board can be operated in Emulation mode or in OTP mode. In emulation mode, as long as the power is supplied, the board configuration stays valid. The OTP mode uses the fused configuration. The device can be fused three times. In OTP mode, the device always starts with the fused configuration, except if the user wants to overwrite OTP configuration using Emulation mode. This board is able to fuse the OTP without any extra tools or board.

## 4.1 Kit overview

The KITFS85AEEVM is a hardware evaluation tool that allows performance test. The FS85xx part soldered on the board can be fused three times (see <u>Section 7.3</u> "Programming the device with an OTP configuration").

An Emulation mode is possible to test as many configurations as needed. The voltage monitoring hardware configuration is done through resistors. Note this configuration can be changed by selecting the appropriate bridges resistors:

• VMON1: assigned to VPRE, 4.1 V

### KITFS85AEEVM evaluation board

- VMON2: assigned to EXT\_MON2, (VMON bridge for 3.3 V input)
- VMON3: assigned to BUCK3, 2.3 V
- VMON4: assigned to EXT\_MON4, (VMON bridge for 5.0 V input)

This configuration can be changed by installing appropriate bridge resistors. This board was designed to sustain up to 10 A total on VPRE. Layout is done using six layer PCB stack up.

The FS84/FS85 family can be evaluated with this board as it is populated with a superset part. The FS84xx supports ASIL B design, while FS85xx supports ASIL D design.

An external LDO provides VDDI2C voltage with a choice of 1.8 V or 3.3 V (default). VDDIO is assigned by default to VDDI2C. From USB voltage, an external DC/DC generates the OTP programming voltage (8.0 V) without any need for an external power supply.

#### 4.1.1 KITFS85AEEVM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE output capability up to 6.0 A (external MOSFET)
- VBUCK1/2 in Standalone (default) or Multiphase mode
- VBUCK3 up to 3.6 A peak
- VBOOST 5.0 V or 5.74 V, up to 400 mA
- LDO1 and LDO2, from 1.1 V to 5.0 V, up to 400 mA
- · Ignition key switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software GUI (access to SPI/I2C bus, IOs, RSTB, FS0B, INTB, Debug, MUX\_OUT, regulators)
- · LEDs that indicate signal or regulator status
- · Support OTP fuse capabilities
- USB connection for register access, OTP emulation and programming

#### 4.1.2 VMON configuration

The VMONx configuration is highly dependent on the use case. This kit is delivered with a default configuration shown in <u>Figure 2</u>.

This configuration supports the following mapping:

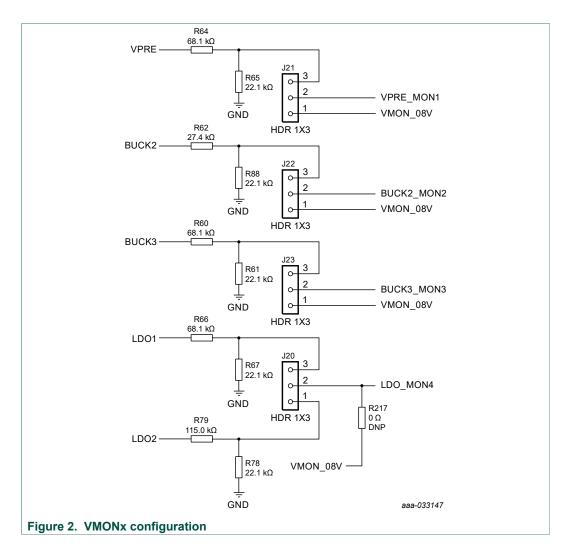
- VPRE, assigned to VMON1; Bridge resistor set for 3.3 V
- BUCK2, assigned to VMON2; Bridge resistor set for 1.8 V
- BUCK3, assigned to VMON3; Bridge resistor set for 3.3 V
- LDO1, assigned to VMON4; Bridge resistor set for 3.3 V
- LDO2, assigned to VMON4; Bridge resistor set for 5.0 V

LDO1 and LDO2 use the same VMON, a reassignment is necessary to monitor both.

Due to the jumpers, VMONx can be tied to a 0.8 V to force a good voltage at pin level. This behaves like hardware disabling and makes debug easy in some cases.

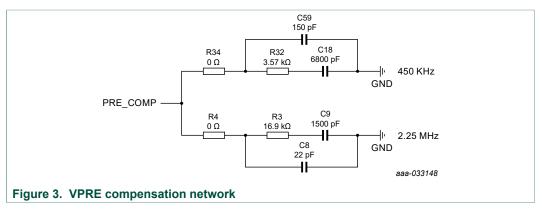
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#### KITFS85AEEVM evaluation board



#### 4.1.3 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 450 kHz. All other VPRE configurations require a new calculation for these components.

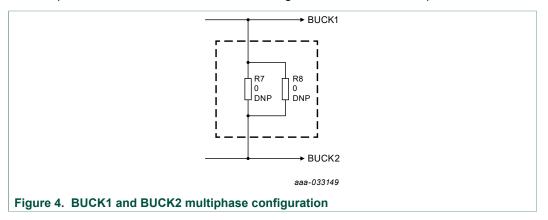


#### KITFS85AEEVM evaluation board

Table 1. Compensation network			
Components	VPRE 450 kHz	VPRE 2.2 MHz	
C18/C9	6.8 nF	1.5 nF	
C59/C8	150 pF	22 pF	
R32/R3	3.57 kΩ	16.9 kΩ	
LPRE	4.7 μH or <b>6.8 μH</b>	<b>1.5 μH</b> , 2.2 μH or 4.7 μH	

#### 4.1.4 BUCK1 and BUCK2 multiphase configuration

The board is designed to work independently with BUCK1 and BUCK2. Due to R7 and R8, it is possible to connect both connectors together and work in multiphase.



#### 4.1.5 SPI/I2C

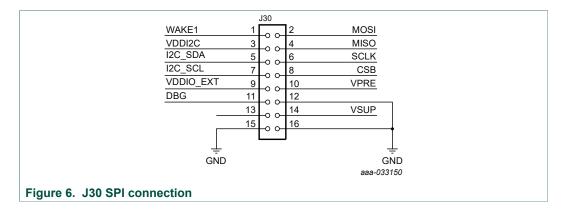
The SPI and I2C buses are connected to KL25Z MCU. The user can use either one or the other. The choice can be done at start of the FlexGUI or at any time after launch (see <u>Section 8 "Using FlexGUI"</u>).

This kit uses a KL25Z MCU to communicate with FlexGUI. However, if the user wants to connect the SPI to another MCU, this is possible. In this case, remove J28 and appropriate jumpers to disconnect the KL25Z MCU (see Figure 5) and connect the external MCU on J30 connector as shown in Figure 6. In addition to this change, make sure that the VDDIO voltage domain is the same on MCU side and SBC side.

[3] RSTb	J28 1 2	RSTb_SH		
[3] FS0b -	3 0 4	FS0b_SH		
[3] MISO →	5 6	MISO_SH		
[3] MISU	7 8	MOSI_SH		
[3] MOSI	9 0 10	SCLK_SH		
[3] SCER -		CSB_SH		
		aaa-032768		
Figure 5. SPI connection to KL25Z	Figure 5. SPI connection to KL25Z			

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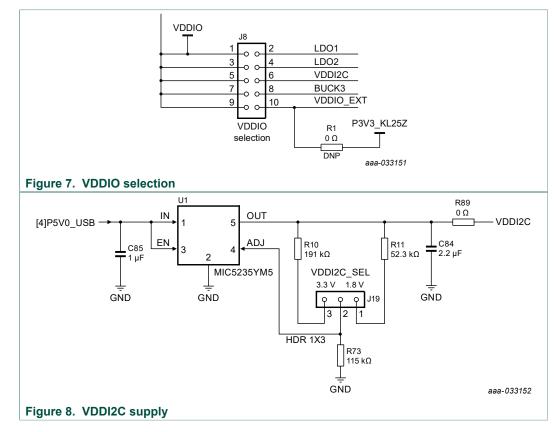
## KITFS85AEEVM evaluation board



## 4.1.6 VDDI2C

As an option, an external LDO is provided to feed VDDI2C. This LDO can also be used to feed VDDIO, which is the default implementation.

The I2C is compatible with 1.8 V or 3.3 V, while VDDIO is compatible with 3.3 V and 5.0 V. For this reason, the LDO default configuration is 3.3 V. The LDO is supplied by 5.0 V coming from the USB.



## 4.2 Device OTP user configuration

It is recommended to learn about OTP before operating with the device. The device has a high level of flexibility due to parameter configuration available in the OTP. This

#### KITFS85AEEVM evaluation board

impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers and the FS85 SoC.

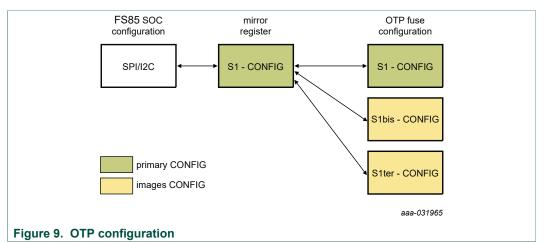
The OTP related operations can be performed either in Emulation mode, where the product uses a given configuration as long as power supply is not switched Off or from OTP fuse content that is valid even after a power down/power up sequence.

#### 4.2.1 OTP and mirrors registers

There are two OTP blocks in the device. One is for the main section, and the other for the fail-safe. During configuration, each of them are using dedicated sectors. The OTP configuration scheme is shown in Figure 9 (same implementation for main and fail-safe).

The device can be fused three times using mirror registers. The user can first load the mirror register content with the desired contents, then decide either to use the device in Emulation mode or to burn the next sector. The first sector to be burned is S1, the second S1bis and the third S1ter. FlexGUI automatically manages the next sector to be burned. It is not possible to revert back to the previous sector. When the user reaches the sector S1ter, there no other possibility for burn, however emulation mode is still available.

**Note:** When device is operating in Emulation mode using configuration from mirror registers, few parameters must be overwritten by SPI/I2C. This concerns regulator TSD behaviors; VPRE slew rate high-side and low-side VBOOST slew rate. See <u>Section 8.4.10 "TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe"</u> for additional details.



At boot, the content of the valid sector is loaded into the Mirror Register Sector 1. The mirror register content is accessible from FlexGUI by using specific SPI/I2C commands. The mirror configuration is managed by the FlexGUI, which eases the access.

#### 4.2.2 OTP hardware implementation

To work in OTP emulation or OTP programming, it is required to start the device in Debug mode.

<u>Figure 10</u> shows the sequence to be followed to enter in Debug mode. The voltage sequence on the kit is done using switches installed on the board, while the OTP registers configuration is managed by the FlexGUI GUI. This is described in detail in the following sections.

KITFS85AEEVM evaluation board

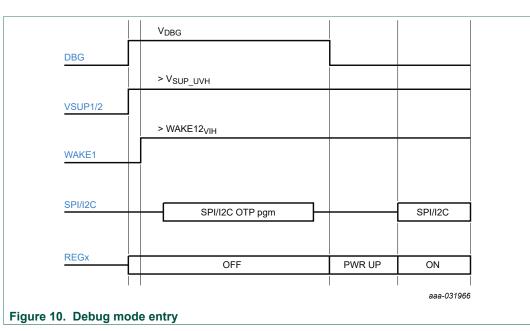
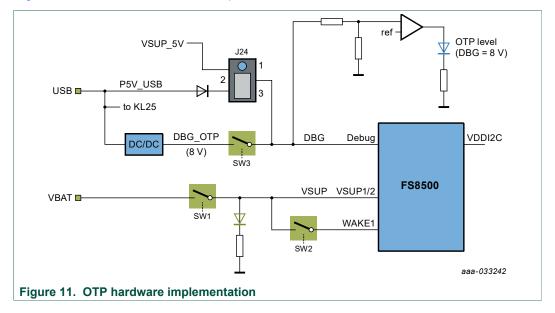


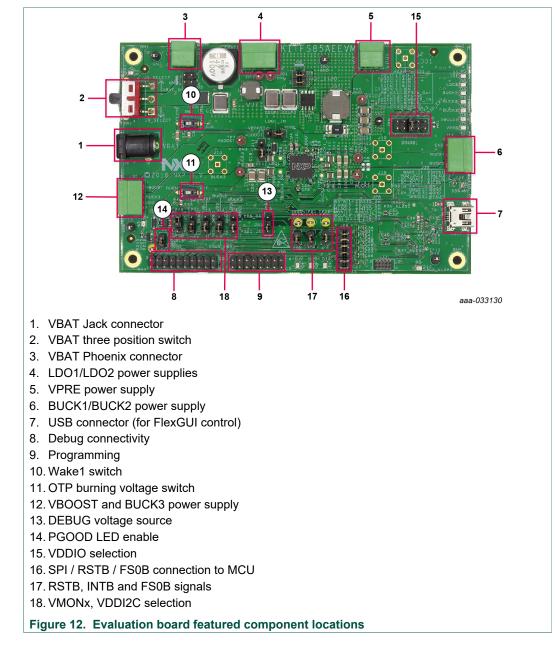
Figure 11 shows the hardware kit implementation.



#### 4.3 Kit featured components

Figure 12 identifies important components on the board and <u>Table 2</u> provides additional details on these components.

### KITFS85AEEVM evaluation board



#### Table 2. Evaluation board board component descriptions

Number	Description
1	VBAT Jack connector
2	<ul> <li>VBAT three position switch</li> <li>Left position: board supplied by Jack connector</li> <li>Middle position: board not supplied</li> <li>Right position: board supplied by Phoenix connector</li> </ul>
3	VBAT Phoenix connector
4	LDO1/LDO2 power supply
5	VPRE power supply
6	BUCK1/BUCK2 power supply

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#### KITFS85AEEVM evaluation board

Number	Description	
7	USB connector (for FlexGUI control)	
8	Debug connectivity. Access to: • VSUP, GND • FOUT/FIN • PGOOD/RSTB/FS0B • FCCUx • WAKE2 • PSYNC, ERRMON, AMUX • VMONx	
9	Programming <ul> <li>SPI bus</li> <li>I2C bus</li> <li>Debug pin</li> <li>VPRE, VSUP, GND</li> </ul>	
10	Wake1 switch	
11	OTP burning voltage switch	
12	VBOOST and BUCK3 power supply	
13	DEBUG voltage source either from USB (recommended) or from VSUP	
14	PGOOD LED indicator (enabled when jumper is plugged)	
15	VDDIO source from device regulators or external sources	
16	SPI, RSTB or FS0B can be disconnected between device and MCU	
17	RSTB, INTB and FS0B signals available here (device pin level)	
18	Allows to select VMON from regulators or a fix 0.8 V VDDI2C can be selected either 1.8 V or 3.3 V	

#### 4.3.1 FS8500/FS8400: Fail-safe system basis chip with multiple SMPS and LDO

#### 4.3.1.1 General description

This device family is part of a global platform FS84 (fit for ASIL B) and FS85 (fit for ASIL D), pin to pin and software compatible. The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard. Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

#### 4.3.1.2 Features

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.

#### KITFS85AEEVM evaluation board

- **Based on part number:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on part number**: low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 2.5 A typical peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10 µA typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

#### 4.3.2 Indicators

The following LEDs are provided as visual output devices for the evaluation board:

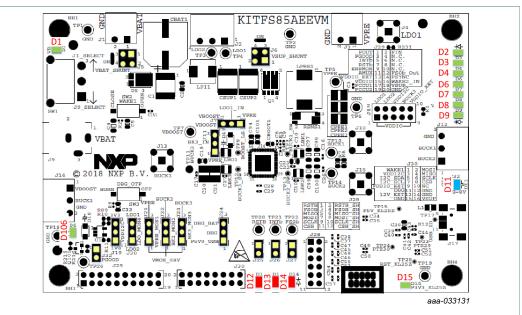


Figure 13. Evaluation board indicator locations

Label	Name	Color	Description	
D1	VBAT	Green	VBAT On	
D2	LDO1	Green	LDO1 On	

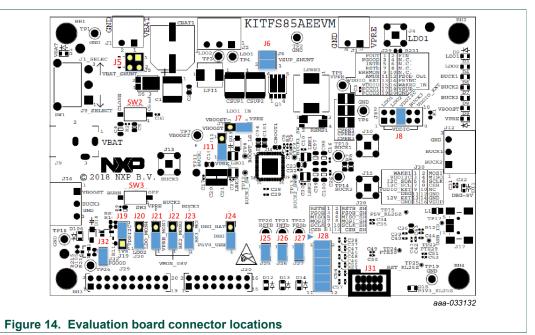
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## KITFS85AEEVM evaluation board

Label	Name	Color	Description
D3	LDO2	Green	LDO2 On
D4	BUCK1	Green	BUCK1 On
D6	BUCK2	Green	BUCK2 On
D7	BUCK3	Green	BUCK3 On
D8	VBOOST	Green	VBOOST On
D9	VPRE	Green	VPRE On
D11	DBG > 8.0 V	Blue	DBG pin voltage > 8.0 V (OTP programming)
D12	RSTB	Red	RSTb asserted (logic level = 0)
D13	INTB	Red	INTB asserted (logic level = 0)
D14	FS0B	Red	FS0B asserted (logic level = 0)
D15	P3V3_KL25	Green	P3V3_KL25 On
D106	PGOOD	Green	PGOOD released

#### 4.3.3 Connectors

Figure 14 shows the location of connectors on the board.



## 4.3.3.1 VBAT connector (J1)

VBAT connects to the board through Phoenix connector (J1).

#### Table 4. V<sub>BAT</sub> Phoenix connector (J1)

Schematic label	Signal name	Description
J1-1	VBAT	Battery voltage supply input
J1-2	GND	Ground

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#### 4.3.3.2 Output power supply connectors

#### Table 5. BUCK1/BUCK2 connector (J14)

Schematic label	Signal name	Description
J14-1	BUCK2	BUCK2 power supply output
J14-2	BUCK1	BUCK1 power supply output
J14-3	GND	Ground

#### Table 6. VBOOST/BUCK3 connector (J16)

Schematic label	Signal name	Description
J16-1	VBOOST	VBOOST output
J16-2	BUCK3	BUCK3 power supply output
J16-3	GND	Ground

#### Table 7. LDO1/LDO2 connector (J2)

Schematic label	Signal name	Description
J2-1	LDO1	LDO1 power supply output
J2-2	LDO2	LDO2 power supply output
J2-3	GND	Ground

#### Table 8. VPRE connector (J3)

Schematic label	Signal name	Description
J3-1	VPRE	VPRE power supply output
J3-2	GND	Ground

## 4.3.3.3 Debug connector (J29)

#### Table 9. Debug connector (J29)

Schematic label	Signal name	Description
J29-1	FOUT	Frequency synchronization output
J29-2	FIN	Frequency synchronization input
J29-3	PGOOD	Power GOOD
J29-4	n.c.	not connected
J29-5	INTB	Interrupt, active low
J29-6	n.c.	not connected
J29-7	RSTB	Reset, active low
J29-8	n.c.	not connected
J29-9	ERRMON	Error monitoring
J29-10	n.c.	not connected
J29-11	AMUX	Analog multiplexer
J29-12	FS0B_Out	Fail-safe, active low
J29-13	VDDIO_EXT	VDDIO external reference

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## KITFS85AEEVM evaluation board

Schematic label	Signal name	Description
J29-14	PSYNC	Power synchronization
J29-15	VDDIO	VDDIO used by FS85
J29-16	WAKE2_IN	Wake2 input
J29-17	FCCU1	Fault collector control unit 1
J29-18	VSUP	VSUP power supply
J29-19	FCCU2	Fault collector control unit 2
J29-20	GND	Ground

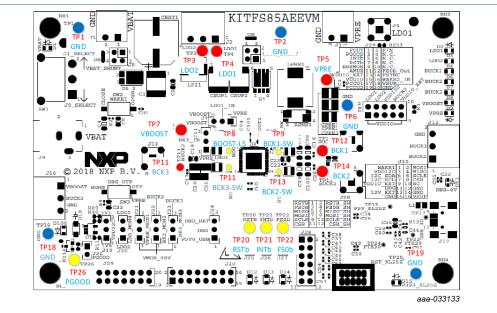
#### 4.3.3.4 Program connector (J30)

Schematic label	Signal name	Description
J30-1	WAKE1	WAKE1 input
J30-2	MOSI	SPI master output slave input
J30-3	VDDI2C	VDDI2C voltage
J30-4	MISO	SPI master input slave output
J30-5	I2C_SDA	I2C serial data
J30-6	SCLK	SPI clock
J30-7	I2C_SCL	I2C serial clock
J30-8	CSB	SPI chip select
J30-9	VDDIO_EXT	VDDIO supplied from external regulator
J30-10	VPRE	VPRE output
J30-11	DBG	Connected to Debug pin
J30-12	GND	Ground
J30-13	n.c.	not connected
J30-14	VSUP	Connected to VSUP pin
J30-15	GND	Ground
J30-16	GND	Ground

## 4.3.4 Test points

The following test points provide access to various signals to and from the board.

## KITFS85AEEVM evaluation board



#### Figure 15. Evaluation board test points

Test point name	Signal name	Description
TP1	GND	Ground
TP2	GND	Ground
TP3	LDO1	LDO1 regulator output
TP4	LDO2	LDO2 regulator output
TP5	VPRE	VPRE DC/DC regulator output
TP6	GND	Ground
TP7	VBOOST	VBOOST DC/DC output
TP8	BOOST_LS	VBOOST low-side switcher
TP9	BUCK1_SW	BUCK1 switcher
TP10	BUCK1	BUCK1 DC/DC regulator output
TP11	BUCK3	BUCK3 DC/DC regulator output
TP12	BUCK3_SW	BUCK3 switcher
TP13	BUCK2_SW	BUCK2 switcher
TP14	BUCK2	BUCK2 DC/DC regulator output
TP19	GND	Ground
TP20	RSTb	Reset
TP21	INTB	Interruption
TP22	FS0B	Fail-safe output
T26	PGOOD	Power GOOD

#### Table 11. Evaluation board test point descriptions

# UM11193 KITFS85AEEVM evaluation board

#### 4.3.5 Jumpers

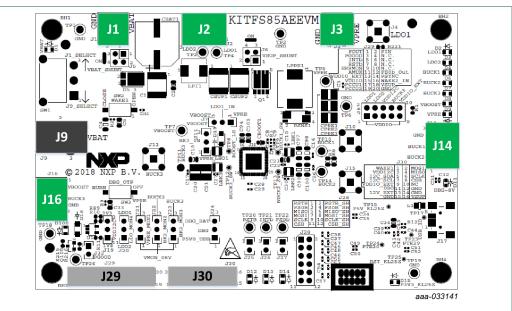


Figure 16. Evaluation board jumper locations

Name	Function	Pin number	Jumper/pin function
J5	VBAT shunt	1-2	Shunt switch SW1 for current > 5.0 A
12	VDAT Shuht	3-4	Shunt switch SW1 for current > 5.0 A
J6	VSUP shunt	1-2	For current measurement (insert amperemeter)
30	VSOF Shull	3-4	For current measurement (insert amperemeter)
J7	LDO1 input	1-2	LDO1_IN connected to VPRE
57		2-3	LDO1_IN connected to VBOOST
		1-2	VDDIO tied to LDO1
		3-4	VDDIO tied to LDO2
J8	VDDIO selection	5-6	VDDIO tied to VDDI2C (provided by external regulators)
		7-8	VDDIO tied to BUCK3
		9–10	VDDIO tied to VDDIO external
J9	VBAT Jack	Jack	Used for VBAT supply using jack connector
J11	BUCK3 input	1-2	BUCK_INQ tied to VPRE
511		2-3	BUCK_INQ tied to VBOOST
J20	VMON4	1-2	VMON4 tied to LDO2
020		2-3	VMON4 tied to LDO1
J21	VMON1	1-2	VMON1 tied to 0.8 V
021		2-3	VMON1 tied to VPRE
J22	VMON2	1-2	VMON2 tied to 0.8 V
022		2-3	VMON2 tied to BUCK2
J23	VMON3	1-2	VMON3 tied to 0.8 V
020	VMUN3	2-3	VMON3 tied to BUCK3

#### Table 12. Evaluation board jumper descriptions

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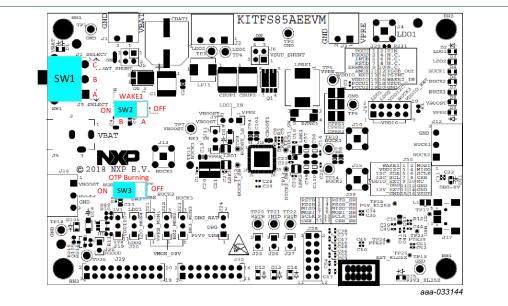
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## KITFS85AEEVM evaluation board

Name	Function	Pin number	Jumper/pin function
104	Debug	1–2	Debug pin tied to P5V0_USB (5.0 V provided by USB connector)
J24	Debug	2-3	Debug pin tied to VBAT (through external protection) Do not use for OTP burning
J25	RSTB	1-2	Reset LED Enabled when jumper is plugged
J26	INTB	1-2	Interrupt LED Enabled when jumper is plugged
J27	FS0B	1–2	FS0B LED Enabled when jumper is plugged
J29	—	—	-
J30	—	—	_
J31	—	—	Use only during board manufacturing
J32	PGOOD	1–2	PGOOD LED Enabled when jumper is plugged

### 4.3.6 Switches



#### Figure 17. Switch locations

#### Table 13. SW3

Position	Function	Description
RIGHT	OTP programming Off	OTP burning not possible
LEFT	OTP programming On	8.0 V on DBG pin allows OTP burning (blue LED turns On to indicate this state)

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#### KITFS85AEEVM evaluation board

Table 14. SW2			
Position	Function	Description	
OFF	WAKE1 open	Wake1 pin not connected to $V_{SUP}$	
ON	WAKE1 closed	Wake1 pin connected to $V_{SUP}$	

#### Table 15. SW1

Position	Function	Description
ТОР	VBAT On	VBAT from J1
MIDDLE	VBAT Off	Board not supplied
BOTTOM	VBAT On	VBAT from J9

#### 4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS85AEEVM evaluation board are available at <u>http://www.nxp.com/KITFS85AEEVM</u>.

## 5 Installing and configuring software and tools

This development kit uses FlexGUI software. FlexGUI software is based on Java JRE.

Preparing the Windows PC workstation consists of three steps.

- 1. Install the appropriate Java SE Runtime Environment (JRE).
- 2. Install Windows 7 FlexGUI driver.
- 3. Install FlexGUI software package.

#### 5.1 Installing the Java JRE

- Download Java JRE (Java SE Runtime Environment), available at <u>http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</u> (8u162 or newer).
- 2. Open the installer and follow the installation instructions.
- 3. Following the successful installation, restart the computer.

#### 5.2 Installing Windows 7 FlexGUI driver

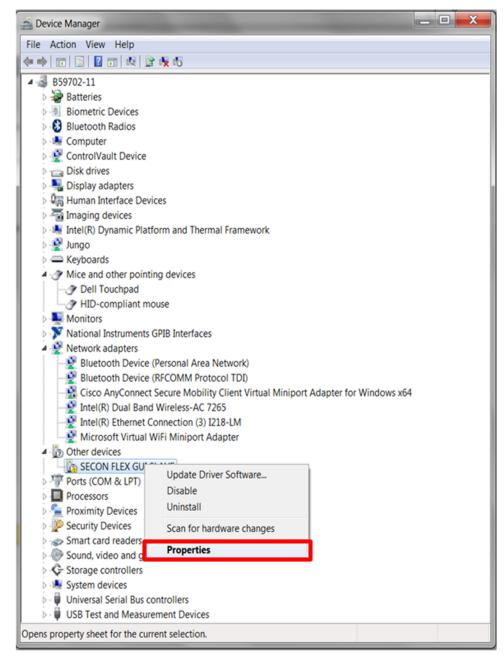
On Windows 7 PCs, a virtual COM port installation is required. Install the Windows 7 FlexGUI driver using the following procedure.

**Note:** On Windows 10, it is not necessary to install virtual com port as Windows 10 uses a generic COM port driver.

- 1. Connect the kit to the computer as described in <u>Section 6 "Configuring the hardware</u> <u>for startup"</u>
- 2. On the Windows PC, open the Device Manager.
- 3. In the **Device Manager** window, right-click on **SECON FLEX GUI SLAVE**, and then select **Properties**.

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aaa-031982

4. In the SECON FLEX GUI SLAVE Properties window, click Update Driver.

## KITFS85AEEVM evaluation board

SECON FLE	X GUI SLAVE Prop	erties X
General	Driver Details	
	SECON FLEX GL	JI SLAVE
	Device type:	Other devices
	Manufacturer:	Unknown
	Location:	Port_#0002.Hub_#0002
The The	e is no driver select	e are not installed. (Code 28) ed for the device information set or element. evice, click Update Driver.
		Update Driver
		Close
		aaa-03198

5. in the Update Software Driver window, select Browse my computer for driver software.

lo	w do you want to search for driver software?	
•	Search automatically for updated driver software Windows will search your computer and the Internet for the latest driver software for your device, unless you've disabled this feature in your device installation settings.	
•	Browse my computer for driver software Locate and install driver software manually.	

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- <complex-block>
  Constant of the series of the seri
- 6. Select Let me pick from a list of device drivers on my computer, and then click Next.

7. Select Ports (COM & LPT) from the list, and then click Next.

Select your device's type	; nom the list be	low.	
Common hardware types:			
Network Client			
Network Protocol			
Retwork Service			
Non-Plug and Play Drivers			
PCMCIA adapters			
Portable Devices			
Ports (COM & LPT)			
Reference of the second			
Processors			=
Proximity Devices			
SBP2 IEEE 1394 Devices			
SD host adapters			
Security Devices			-

8. Click Have Disk.

## KITFS85AEEVM evaluation board

	In the local distance	ligerte.		×
$\bigcirc$	Update Driver Software - SECON Fl	EX GUI SLAVE		
	Select the manufacturer and	vant to install for this hardware. model of your hardware device and then you want to install, click Have Disk.		If you have a
	Manufacturer (Standard port types) Brother Compaq GSM Radio Card NBC Compart GSM Radio Card This driver is digitally signed. Tell me why driver signing is imp	Model Communications Port ECP Printer Port Multiport Communications Port Printer Port	Ha	ave Disk
			Next	Cancel

aaa-031987

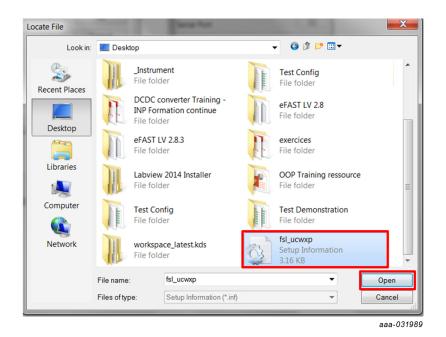
9. Click Browse.

HON NO.	nutrion tuble Properties	X
🕞 👖 Update D	Priver Software - SECON FLEX GUI SLAVE	
Select the o	device driver you want to install for this ha	ardware.
Selec Install From	t the manufacturer and model of your bardware device n Disk	and then click Next. If you
N C	Insert the manufacturer's installation disk, and then make sure that the correct drive is selected below.	OK Cancel
A B	Copy manufacturer's files from:	
	r is digitally signed. <del>Iny driver signing is important</del>	Have Disk
		Next Cancel
		aaa-031988

10.In the Locate File window, locate and select fsl\_ucwxp, and then click Open.

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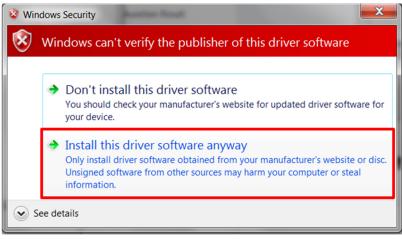


11.In the Install from Disk window, click OK.

Install Fron	n Disk	X
<i>.</i>	Insert the manufacturer's installation disk, and then make sure that the correct drive is selected below.	OK Cancel
	Copy manufacturer's files from: C:\Users\B59702\Desktop	Browse
		aaa-0319

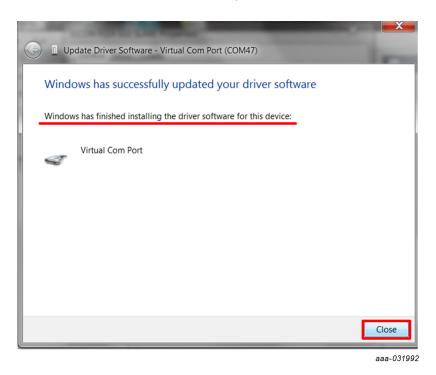
12.If prompted, in the **Windows Security** window, click **Select this driver software anyway**.

#### KITFS85AEEVM evaluation board



aaa-031991

13.Close the window when the installation is complete.



14.In the **Virtual Com Port Properties** window, verify that the device is working properly, and then click **Close**.

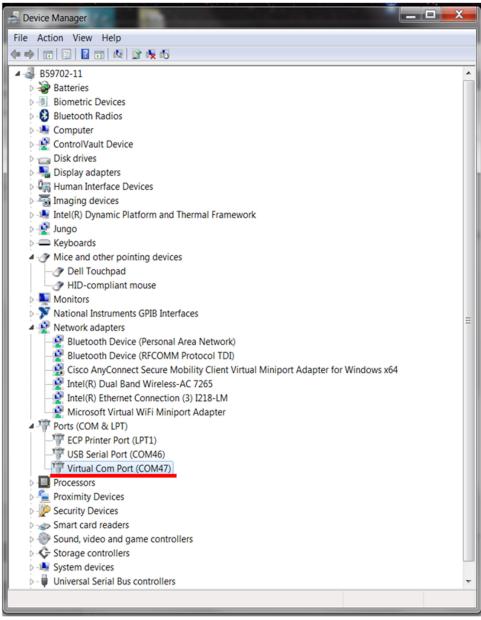
# KITFS85AEEVM evaluation board

Virtual Com Port (COM47) Properties							
General	Driver Details						
1	Virtual Com Port (0	COM47)					
	Device type:	Other devices					
	Manufacturer:	NXP					
	Location:	Port_#0002.Hub_#0002					
	e status device is working pro	operly.					
			~				
		Close	Cancel				

aaa-031993

The Virtual Com Port appears in the Device Manager window.

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aaa-031994

## 5.3 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

- 1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
- 2. Download the latest FlexGUI (32-bit or 64-bit) version, available at <u>http://www.nxp.com/KITFS85AEEVM</u>.
- Extract all the files to a desired location on your PC. FlexGUI is started by running the batch file, \bin\flexgui-app-fs85.bat.

# <figure><figure>

# 6 Configuring the hardware for startup

Figure 18 presents a typical hardware configuration incorporating the development board, power supply and Windows PC workstation.

To configure the hardware and workstation as illustrated in <u>Figure 18</u>, complete the following procedure:

1. Install jumpers for the configuration.

Table 16. Jumper configuration						
Jumper	Configuration					
J24	connect 1-2 (connect 5.0 V on DBG pin from the USB)					

2. Configure switches for the configuration

Table 17. Switch configuration						
Switch	Configuration					
SW1	middle position (VBAT off)					
SW2	open (WAKE1)					
SW3	open (OTP programming off)					

3. Connect the Windows PC USB port to the KITFS85AEEVM development board using the provided USB 2.0 cable.

Set the DC power supply to 12 V and current limit to 1.0 A. With power turned off, attach the DC power supply positive and negative output to KITFS85AEEVM  $V_{BAT}$  Phoenix connector (J1).

- 4. Turn on the power supply.
- 5. Close SW2.

**Note:** At this step, the product is in debug mode and all regulators are turned off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as J24 jumper is removed.

# 7 Using the KITFS85AEEVM evaluation board

This section summarizes the overall setup. Detailed description is provided in the following sections.

Before starting the process, choose the mode you want to run the device.

- In Normal mode, the configuration comes from OTP fuses.
- In Debug mode, you can either use the current configuration from OTP fuse, if any, or use the OTP emulation mode to write in the mirror register.

The Normal mode or Debug mode is defined at startup depending on the DBG pin level.

- Normal mode is set by tying DBG to ground.
- Debug mode is set by setting DBG voltage to 5.0 V.

In OTP emulation, you can overwrite the mirror registers from a given OTP fuse configuration. See <u>Section 4.2.1 "OTP and mirrors registers"</u> and <u>Section 8.3 "Working with the Script editor"</u> to define your configuration.

In OTP fuse configuration, use the configuration fused in the OTP. So, if a valid OTP fuse configuration exists, then it is copied to the mirror registers at startup.

## 7.1 Generating the OTP configuration file

Define and generate your OTP configuration using the excel file *FS85\_FS84\_OTP\_Config.xlsm*. This file allows configuring the device for parameters controlled by the the main state machine and the fail-safe state machine.

**Note:** You can avoid this step by using a trial script (FS85\_UG\_Config.txt) available on the website.

To generate the script:

1. Fill data in the **OTP\_conf\_main\_reg** sheet.

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						OTP_REGISTERS					
egister Name		BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BITO	Data_Bin	Data_H
TP_CFG_VPRE_	14		-				EV[5:0]				
		0	0				0 - 5.0V			00100000	0x20
TP_CFG_VPRE_	2 15		-				SC[5:0]				
		0	0				70mVłµs			00000111	0x07
TP_CFG_VPRE_	3 16	VPREI			OFF[1:0]		SRLS[10]		SRHS[1:0]		
			20m¥	10 - 40ns 11 - PU/PD/300mA 00 - PU/PD/30mA				PD/130mA	10101100	0zA	
P_CFG_BOOST	17	0			VPRE_MODE         Reserved         VBSTV[3:0]           0 - Force PV/M         0         1101 - 5.74V					00001101	0x0
P CFG BOOST	18	BOOSTEN		0 - Force PVM ONTIME[1:0]	0			0.74V		00001101	UZU
P_UFG_BOUST_	18	1 - Enabled					VBSTSC[4:0]			10001100	0x8
	19		OMP[1:0]	00 - 60ns 01100 - 125mV/µ.s				000000	10001100	828	
P_CFG_BOOST_	19			I) VBSTCCOMP[1:0] VBSTILIM[1:0] VBSTSR[1:0] 00-125pF 01-2A 11-500Y/us						820	
P CFG BUCKI	1A	00 - 750	Okohms	00+1	126pF	VBIV[7:0]	- 2A	11+5	Ουνγμε	00000111	Uzt
P_CFG_BOCKI	18					VBIV[7:0] 0001000 - 1.25V				10001000	Ozf
P CFG BUCKI	1B		otp SPARE0[2	0		OPT[1:0]	VBISVI	18.471.01	VB12MULTIPH	10001000	UXC
F_CFG_BOCKI			000_0FARE0[2	.0	VBIINL	• 1µH	11-4		0 - Disabled	00000110	0x4
P CFG BUCK2	1C		000			VB2V[7:0]	1		0 · Disabled	00000110	~~
	- ~~					10110001 - 1.8V				10110001	0xl
P CFG BUCK2	1D		VB2IA	JDOPT[1:0]	BUCK2EN		/ILIM[1:0]	VB3 CTRL RC	VB3 CTRL GM	10110001	
		0	0	0 - 1µH	1 - Enabled	11-	4.5A	0 - Default	0 - Default	00011100	0x
P CFG BUCK3	1E	BUCK3EN	VB3IN	IDOPT[1:0]			VB3V[4:0]				
		1 - Enabled	0	0 - 1µ.H			10101 - 3.3V			10010101	0z
P_CFG_BUCK3_	1F		VB2GMCOMP[2	50]		VB1GMCOMP[2:0]			/ILIM[1:0]		
			100 - 65 GM			100 - 65 GM			4.5A	10010011	0x
TP CFG LDO	20	LDO2ILIM		LD02V[2:0]		LDO1ILIM		LD01V[2:0]			
		0 - 400mA		111 - 5.0V		1 - 150mA		111 - 5.0V		01111111	0x
TP CFG SEQ 1	21				VB2S[2:0]			VB1S[2:0]			
		0	0	000 - E	egulator Start and Stop i	in Slot 0	000 - B	egulator Start and Stop	in Slot 0	00000000	0z
TP CFG SEQ 2	22				LD02S[2:0]			LD01S[2:0]			
		0	0		or does not Start (Enable	d by SPI/I2C)	000 - R	egulator Start and Stop	in Slot 0	00111000	0z
TP_CFG_SEQ_3	23	DVS_BU	CK12[1:0]	DVS_BL	JCK3[1:0]	Tslot		VB3S[2:0]			
		00 - 7.8	lm∀nµs	00 - 10.4	lm∀łµs	0 - 250µs	000 - R	egulator Start and Stop	in Slot 0	00000000	0x
P_CFG_CLOCK	24	•			VPRE_ph[2:0]			CLK_DIV2[2:0]			
		0	0		000 - delay 0		100	divide by 44 - CLK2=45	5KHz	00000100	Øzt
P CFG CLOCK	25				BUCK1_ph[2:0]			VBST ph[2:0]			
		0	0		110 - delay 6			000 - delau 0		00110000	0z
P CFG CLOCK	26				BUCK3 ph[2:0]			BUCK2 ph[2:0]			
		0	0		011 - delay 3			000 - delau 0		00011000	0z
P CFG CLOCK	27	BUCK3 clk sel	BUCK2 clk sel	BUCK1 clk sel	VBST clk sel	VPRE clk sel	PLL_sel	CLK	DIV1[1:0]		
		0 - CLK1	0 · CLK1	0 · CLK1	0 - CLK1	1-CLK2	0 · Disabled		- CLK1=2.22MHz	00001010	8z(
TP CFG SM 1	28						tsd[5:0]				
		0	0	0 - BOOST Shutdown	1-BUCK1Shutdown +		1 BUCK3 Shutdown +	0 - LDO1 Shutdown	0 - LDO2 Shutdown	00010100	0x
TP CFG SM 2	29	· ·	oto SPARE1[2		VPRE off dlu	Autoretru infinite	Autoretru en	PSYNC CFG	PSYNC EN	00010100	
	20		000	~	1-32ms	1 - Enabled	1 · Enabled	0 - 2x FS85	0 - Disabled	00011100	8z1
P CFG VSUP L	2A		000		otp SPARE2[6		1 - Chapleo	0-281300	VSUPCEG	00011100	UXI
r_ora_VSUP_0	2M				0000000	201			0 - 4.9V for Vpre < 4.5V	00000000	Ozt
OTP CFG I2C	2B				000000		M I2CDEV	ADDDI2.01	1 0 - 4.5V ror vpre < 4.5V	00000000	Uzi
OTP_CFG_2C	28	0	0		0		M_12CUEV 0001- Ad			00000001	0x
070 050 OU	00								~	00000001	Uzt
OTP_CFG_OV	2C		-				V V	DDIO_REG_ASSIGN[2	:0]		-
		0	0	0	0	0		100 - BUCK3		00000100	0x0
TP_CFG_DEVID	2D					DeviceID[7:0]					
						00000001				00000001	0z
P_M_S1_CRC_LS	2E					4_S1_CRC_LSB[7:0]					
						ally filled in by Sidence IP				00000000	Ozt
_M_S1_CRC_M	2F					1_S1_CRC_MSB[7:0] allu filled in bu Sidence IP				00000000	0x0

Figure 19. OTP\_conf\_main\_reg spreadsheet example

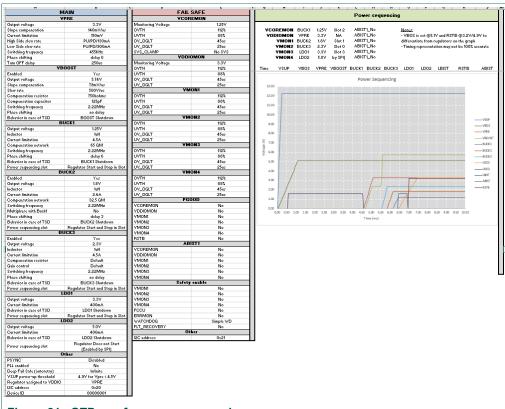
2. Fill data in the OTP\_conf\_failsafe\_reg sheet.



#### Figure 20. OTP\_conf\_failsafe\_reg spreadsheet example

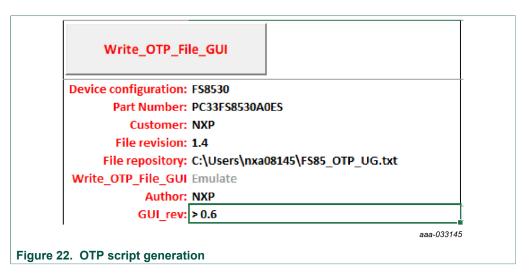
3. See the **OTP\_conf\_summary** sheet to review the complete configuration (main and fail-safe).

#### KITFS85AEEVM evaluation board



#### Figure 21. OTP\_conf\_summary example

 Generate script in the OTP\_conf\_file\_generation sheet. Once the configuration is ready, the user can generate the script file. Go to OTP\_conf\_file\_generation, enter the path in the File repository, and then click Write\_OTP\_File\_GUI.



## 7.2 Working in OTP emulation mode

At startup, the device always uses the content from the mirror register. This content can come from OTP fuse or from configuration written directly in the mirror register. OTP

#### KITFS85AEEVM evaluation board

emulation means that the user can emulate the OTP writing in the mirror register. This allows trials before burning the OTP.

- 1. Configure the hardware. See Section 6 "Configuring the hardware for startup".
- 2. Launch the FlexGUI software.
- 3. Switch to Debug mode:
  - a. Place SW1 in TOP direction (VBAT switched On).
  - b. Close SW2 (WAKE1).

While in Debug mode, all regulators are turned Off.

- 4. Load the mirror registers to work in OTP emulation mode. See <u>Section 8.3 "Working</u> with the <u>Script editor"</u>.
- 5. Unplug jumper J24 1-2 to start the device with the mirror configuration setting.
  - a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
  - b. If the mirror registers are not filled (with a configuration using the Script editor), the currently-programmed OTP fuse configuration is used, if it exists.
  - c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned, and the device will not start up.

As long as initialization phase is not closed by a first good WD\_Answer, the WD does not start and regulators do not stay alive. Also, as long as Debug mode is not exited by writing FS\_STATES:[DBG\_EXIT] bit to 1, the FS0B pin cannot be released.

 Use the FlexGUI software to evaluate the device configured. See <u>Section 8 "Using</u> <u>FlexGUI"</u>.

# 7.2.1 Example script: Closing initialization phase, disabling FCCU monitoring and releasing FS0B

The following script can be used to:

- Disable the WD (simple WD configuration is used here).
- Disable the FCCU monitoring.

On the hardware kit, the FCCU1 is pulled to GND and FCCU2 is pulled to VDDIO, which is detected as error phase by default. Disabling the FCCU by SPI/I2C avoids safety issue at startup.

- · Close the initialization phase.
- Exit the Debug mode.
- Release FS0B pin. This is valid only if WD is activated in OTP. Seven good consecutive WD answers are required to have the FLT\_ERR\_CNTR back to 0. This is one of the conditions to allow FS0B release.

Step	Register name	Value	Description
1	FS_WD_WINDOW	0x0200	WDW_WINDOWS[3:0] = 0x0 => Watchdog disabled
2	FS_NOT_WD_WINDOW	0xF50F	NOT of FS_WD_WINDOW
3	FS_I_SAFE_INPUTS	0x51C6	FCCU_CFG[1:0] = 0x0 => 0x1 => Monitoring by pair FCCU12_FLT_POL[0] = 1 => FCCU1 or 2 = 0 is a fault
4	FS_I_NOT_SAFE_INPUTS	0xAC18	NOT of FS_I_SAFE_INPUTS
5	FS_WD_ANSWER	0x5AB2	1st good WD answer (for simple WD selection in OTP) Close the initialization phase
6	FS_STATES	0x4000	DBG_EXIT[0]=1 => Exit Debug mode

#### Table 18. FS85 starting sequence example

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Step	Register name	Value	Description
7	FS_WD_ANSWER	0x5AB2	2nd good WD answer
8	FS_WD_ANSWER	0x5AB2	3rd good WD answer
9	FS_WD_ANSWER	0x5AB2	4th good WD answer
10	FS_WD_ANSWER	0x5AB2	5th good WD answer
11	FS_WD_ANSWER	0x5AB2	6th good WD answer
12	FS_WD_ANSWER	0x5AB2	7th good WD answer
13	FS_RELEASE_FS0B	0xB2A5	FS0B pin released (pulled to high level)
14	MFLAG2	0x40F1	Clear flags VSUPUV7; VPREUVL, VSUPUVL, WAKE1FLG
15	FS_OVUVREG_STATUS	0x4550	Clear UV status flags

This sequence can be sent using a script built with FlexGUI. See <u>Section 8.3.2 "Script</u> <u>sequence files</u>".

## 7.3 Programming the device with an OTP configuration

The device configuration can be changed three times (see <u>Section 4.2.1 "OTP and</u> <u>mirrors registers"</u>). The programming steps are exactly the same as the OTP emulation mode up to step 6.

Then, the user has to burn the part with FlexGUI. See <u>Section 8.4.8 "OTP programming"</u>. Follow the instructions on the screen to proceed.

## 8 Using FlexGUI

To follow the steps in this section, make sure that the board is connected using the appropriate hardware configuration (see <u>Section 7.2 "Working in OTP emulation mode"</u>).

Note: It is recommended to use the latest version of FlexGUI.

#### 8.1 Starting the FlexGUI application

After FlexGUI is launched with the *flexgui-app.bat* file, the FlexGUI launcher displays available kits.

Communication bus, SPI or I2C can be selected at this level. It is also possible to switch from one to the other using the communication tab from the main panel (see <u>Section 8.2</u> "Establishing the connection between FlexGUI and the hardware").

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FlexGUI Laune					×
Select a kit, or	n board device(s), ta	rget MCU	and USE	interfa	ce.
Kit and Device	s)				
▼ FS85 KITs					
▼ FS85					
▼ ✓ F:	\$8530				
	во				
$\checkmark$	C0				
	nd FS84 evaluation.	us selection			
A kit for FS85 a	SPI or I <sup>2</sup> C h	ous selection			
	SPI or I <sup>2</sup> C h	_	ust loade	d tabs, et	tc.
✓ Advanced Set	SPI or I <sup>2</sup> C b	🔹 🧬 Adj			
✓ Advanced Set Feature Set	SPI or I <sup>2</sup> C b ettings debug-spi	<ul> <li>✓ <sup>6</sup> Adj</li> <li>✓ <sup>1</sup> Che</li> </ul>	ust loade	IW setup	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> </ul>	SPI or I <sup>2</sup> C b ettings debug-spi KL25Z (embedd usb_cdc	<ul> <li>✓ <sup>6</sup> Adj</li> <li>✓ <sup>1</sup> Che</li> </ul>	ust loade eck your H	IW setup	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> </ul>	SPI or I <sup>2</sup> C b ettings debug-spi KL25Z (embedd usb_cdc	<ul> <li>Adj</li> <li>Che</li> <li>Che</li> <li>Che</li> </ul>	ust loade eck your H eck used f	IW setup	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application</li> </ul>	SPI or I <sup>2</sup> C b ettings debug-spi KL25Z (embedd usb_cdc Mode provide sect	<ul> <li>Adj</li> <li>Che</li> <li>Che</li> <li>Che</li> </ul>	ust loade eck your H eck used f	IW setup irmware.	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application</li> <li>Password</li> <li>Launch Privileg</li> </ul>	SPI or I <sup>2</sup> C b ettings debug-spi KL25Z (embedd usb_cdc Mode provide sect	<ul> <li>Adj</li> <li>Che</li> <li>Che</li> <li>Che</li> </ul>	ust loade eck your H eck used f	IW setup irmware.	
<ul> <li>Advanced Set</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application</li> <li>Password</li> <li>Launch Privileg</li> </ul>	SPI or I <sup>2</sup> C b ettings debug-spi KL25Z (embedd usb_cdc Mode provide sect es BAS	<ul> <li>Adj</li> <li>Che</li> <li>Che</li> <li>Che</li> </ul>	ust loade eck your H eck used f	IW setup irmware. evate	

Figure 23. Launcher panel - bus selection

When the configuration is selected, click **OK**.

## 8.2 Establishing the connection between FlexGUI and the hardware

The board must be connected to the USB before establishing a connection.

- Click **Search** to detect the COM port of the board.
- Click Start to enable the connection.

## KITFS85AEEVM evaluation board

5 Still Register map Clocks Regulators	Measurama	inte Internet Flag		ety Dian Safety OTP prog	TestMode Services	ar TastModeMirrors	Main TestModeMi	mm FailSafe				
TM_STATUS1:0x1FJ R: 0x022E												
	gisters Per P	age o 💌	Bit Buttons I	Per une 8 💌 Sol	t by Address 🔽 Uni	form suttons 🔽 Sho	W Bit Position					
TM_STATUS1:0x1FJ R: 0x022E functional		Write Read (	Copy Res	et								
_STATES:0x16] R: 0x4006 TM_STATUS1:0x1FI R: 0x022E												
				W 0x0								
STATES OX 16] R: OXA006 Start		M FLAG	0x00	0	RESERVED	RESERVED	RESERVED	SPUMUCLK	SPUMUREQ	SPLMLCRC	IQC_M_CRC	IQC_M_REQ
STATES OK 16] R: ON ADDE				R 0x0	COMLERR	WU,6	VPRE,0	V80057,6	VBUCK1,6	V8UCK2,6	VBUCK3,6	VLD01_6
TM STATUS1.0x1FI R: 0x022E				K OXO	VLD02_6	ASSERVED	RESERVED	SPILMUCLK	SPUMUREQ	SPUMUCRC	I2C_M_CRC	I2C_M_REQ
STATES:0x16] R: 0xA006					RESERVED			RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
TM_STATUS1.0x1FJ R: 0x022E Search				W 0x0								
STATES:0x16] R: 0x4006 COM Port		M_MODE	0x01		RESERVED	EXT_RIN_DIS	RESERVED	RESERVED	RESERVED	W2D15	W1DIS	GOTOSTBY
TM_STATUS1:0x1FJ R: 0x022E				R 0x0	RESERVED	ALSERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PLL_LOCK_RT
STATES:0x16] R: 0x4006				K OID	EXT_FIN_SEL_RT	RESERVED	MAIN_NORMAL	RESERVED	RESERVED	W2015	WIDIS	RESERVED
TM_STATUS1:0x1F) R: 0x022E					VPRE_PD_DIS	VPDIS	BOOSTOIS	8UCK1DIS	RUCK2DIS	RUCKION	1001015	LDOZDIS
STATES:0x16] R: 0x4006				W 0x0								
TM_STATUS1.0x1FJ R: 0x022E STATES.0x16J R: 0x0206 User mode or Tes	at 📖	M REG_CTRL1	0x02		RESERVED	VPEN	BOOSTEN	BUCKTEN	BUCKZEN	BUCK3EN	LDO1EN	LDO2EN
Mode Selection				R 0x0	VPRE_PD_DIS	ALSERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Mode Selection				K OKO	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
					V8STSRI11	V8575R001	BOOSTTSDCFG	8UCK1TSDCFG	BUCK2TSDCFG	BUCK3TSDCF6	LD01TSDCF6	LDO2TSDCFG
: test-mode 💌 Poll				W 0x0	RESERVED	ALSERVED	RESERVED		VPRESRUSIOI	ALSERVED	VPRESRHSTIT	VPRESRHSIDI
		M_REG_CTRL2	0x03	0				VANTERNIELI				
SPI-routing *				R 0x9	V8STSR[1]	VESTSRIDI	BOOSTTSDCFG	BUCKITSDCFG	BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG
SPI or I2C Switch	1				RESERVED	RESERVED	RESERVED	VPRESRLS[1]	VPRESRLS[0]	RESERVED	VPRESRHS[1]	VPRESRHSJOJ
SPI												
Hz): 5000				W Oxe			RATIO	ANUDZE	AMUXUU	AV(U)(2)	AMUD[1]	AMUNOT
va		M_AMUX	0x04	0								
				R Ox0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
itatus					RESERVED	ALSURVED	RATIO	AMUX[4]	AMU0[3]	AMU0021	AMUR[1]	AMU000
No event					M00_CON#	FOUT_MUX_SEL[3]	FOUT_MUX_SEL[2]	FOUT_MUX_SEL[1]	FOUT_MUX_SEL[0]	FOUT_PHASE[2]	FOUT, PHASE[1]	FOUT_PHASE[0]
No error				W 0x0	FOUT_CLK_SEL	EXT FIN SEL	FINLOW	MOD EN	CUK_TUNE(3)	CUCTUNER	CUCTUNE[1]	CLK_TUNE(0)
No error		M_CLOCK	0x05	0			and the second second					
No error Communication				R 0x0	MOD_CONF	FOUT_MUX_SEL[3]	FOUT_MUX_SEL[2]	FOUT_MUX_SEL[1]	FOUT_MUX_SEU[0]	FOUT, PHASE[2]	FOUT,PHASE[1]	FOUT, PHASE[0]
No error / Status					POUT_CLK_SEL	ASSERVED	FINLOW	MOD_EN	CUK;TUNE[3]	CUC,TUNE[2]	CUK_TUNE[1]	CLK_TUNE[0]
No error							< 1 2	3 1				
							1/3					

#### Figure 24. Main panel

<u>Figure 24</u> shows the mode selection. At first launch, the FlexGUI starts in User mode. The user can then decide to switch to Test mode using the Switch mode drop-down list followed by clicking **Apply**.

The **GUI-Device Status** field checks the connection from MCU to the device. The **ONLINE** status indicates a good connection, while **ERROR** status indicates an issue (e.g. V<sub>SUP</sub> is not provided to the device).

The SPI/I2C communication bus can be changed at any time using the drop-down list. This change is managed by the onboard MCU to communicate with the desired bus.

It is also possible to change the clock frequency using this panel.

Note that in the case of I2C, most of the time, the default address used by the device are 0x20 for main and 0x21 for the fail-safe.

The I2C address is managed differently in Debug and Normal mode

- Debug mode :
  - I2C address when debug mode pin is set to 5.0 V are 0x20 for main and 0x21 for failsafe.
  - The user can change this address in the mirror register. The new address is taken into account only after debug pin is released to 0 V.
- Normal mode:
  - The address is burned in the OTP.

The user can read in which mode the device is operating. It is also possible to switch from user mode to test mode (and vice-versa).

The current operating mode is refreshed periodically by default at FlexGUI startup. This automatic refresh can be disabled by disabling Poll button as shown in <u>Figure 25</u>.

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ſ	FS85			
	Mode			
	Switch Mode:	user-mode	•	Apply
	Current Mode:	user-mode		Poll
				aaa-032771
Figure 25. Disal	oling device mode p	olling		

To move from one mode to the other, select the mode with switch mode drop-down button and click **Apply** to validate. At this time, the current mode is updated at the condition that Poll button is enabled.

## 8.3 Working with the Script editor

The register and OTP emulation can be configured with the script editor. This is particularly useful to try various OTP configurations in Emulation mode.

INFO • 500 🔶 🖌 II 💾			
Iter messages	Device: FS85 *	Commands:	Results:
3> FS85 [FS_MIRRORDATA.0x18] W: 0x00	Alias: No values *	//Device configuration: FS8530	//Device configuration: FS8530
4> FS85 [FS_MIRRORCMD:0x17] W: 0x0119	<ul> <li>Digital pins</li> </ul>	//Sample marking: PC33F58530A0ES //Author: NXP	//Sample marking: PC33FS8530A0ES
> FS85 [FS_OTPCMD:0x18] W: 0x0125	<ul> <li>Analog pins</li> </ul>	//Customer: NXP	//Author: NXP
FS85 (FS_OTPCMD:0x18) W: 0x0124	Registers	//Date: 11/8/2018 //Time: 10:12:14 AM	//Customer: NXP
FS85 [FS_TM_STATUS1:0x2A] R: 0xA0C0	<ul> <li>Mode</li> </ul>	//Imme: to: Lo:14 AM //Generated from FS85_OTP_Mapping file revision: Rev 1.4	//Date: 11/8/2018
FS85 [M_TM_STATUS1:0x1F] R: 0x0022		//Emulate/Program: Emulate	//Time: 10:12:14 AM
FS85 [FS_STATES:0x16] R: 0x4001	Generator     //GUL_rev: > 0.6     //TEST_MODE_ENTRY	//GUI_nev: > 0.6 //TEST_MODE_ENTRY	//Generated from FS85_OTP_Mapping file revision: Rev 1.4
FS85 [M_TM_STATUS1:0x1F] R: 0x0022		SET_MODE:FS85:test-mode	//Emulate/Program: Emulate
FS85 [FS_STATES:0x16] R: 0xA001	Command	//BEGIN MAIN	//GUI_rev: > 0.6
FS85 [M_TM_STATUS1:0x1F] R: 0x0022	Script Editor	//Verify Main Test Mode Entry (expect 0x0022) GET_REG: FS85: M_TestMode: M_TM_STATUS1	//TEST_MODE_ENTRY
FS85 [FS_STATES:0x16] R: 0xA001	Script Editor	//CONFIGURE OTP MIRROR REGISTERS Script Text Editor	OK: set mode = test-mode Script Results
FS85 [M_TM_STATUS1:0x1F] R: 0x0022		str. #dd/stss.M. ofrew.mikinolaufa.acodol str. #dd/stssM.ofrew.mikinolaufa.acodol str. #dd/stssM.ofrew.mikinolaufa.acodor str.#dd/stssM.ofrew.mikinolaufa.acodor str.#dd/stssM.ofrew.mikinolaufa.acits	//BEGIN MAIN
FS85 (FS_STATES:0x16) R: 0xA001			//Verify Main Test Mode Entry (expect 0x0022)
FS85 [M_TM_STATUS1:0x1F] R: 0x0022	Send and Received		OK: read reg. M_TM_STATUS1 = 0x0022
FS85 [FS_STATES:0x16] R: 0xA001	Commands		//CONFIGURE OTP MIRROR REGISTERS
FS85 [M_TM_STATUS1:0x1F] R: 0x0022			OK: write reg. M_MIRRORDATA = 0x0f
FS85 [FS_STATES:0x16] R: 0xA001			OK: write reg. M_MIRRORCMD = 0x0114
5 Pins			OK: write reg. M.MIRRORDATA = 0x07
ode			OK: write reg. M.MIRRORCMD = 0x0115
itch Mode: test-mode *			OK: write reg. M_MIRRORDATA = 0xef
rrent Mode: test-mode			OK: write reg. M. MIRRORCMD = 0x0116
rrent Mode: test-mode			OK: write reg. M_MIRRORDATA = 0x0d
ting: SPI-routing *			OK: write reg. M_MIRRORCMD = 0x0117
SPI1			OK: write reg. M_MIRRORDATA = 0x8c
se SPI			OK: write reg. M MIRRORCMD = 0x0118
quency [kHz]: 5000			OK: write reg. M_MIRRORDATA = 0x07
()			OK: write reg. M_MIRRORCMD = 0x0119
Main Status			OK: write reg. M_MIRRORDATA = 0x64
M_ERR: No failure			OK: write reg. M MIRRORCMD = 0x011a
_G: Event occurred			OK: write reg. M_MIRRORDATA = 0x05
RE_G: Event occurred			OK: write reg. M_MIRRORCMD = 0x011b
OST_G: Event occurred			OK: write reg. M. MIRRORDATA = 0x88
ICK1_G: No event			OK: write reg. M_MIRRORCMD = 0x011c
UCK2_G: No event			OK: write reg. M_MIRRORDATA = 0x1c
UCK3_G: No event		💿 🗠 💾 📄 🚽 😨 Script Execution and Manage	ment
.DO1_G: No event	~		

#### Figure 26. Script Editor

The main subareas of this panel are:

- Send and receive command: displays a summary of commands sent and received from the device
- · Command script editor: builds commands to be sent to the device
- Script text editor: sends a sequence of register configurations from a text file or from command edited directly in this area
- Script results: displays result status of each command sent to the device

#### 8.3.1 Script text editor

Using Script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if needed.

All commands have to follow a specific syntax. The Help menu describes commands available in the script editor and their syntax.

This help page describes commands available in the script editor and their format.

#### List of commands

- SET\_REG: sets value of a selected register.
- READ\_REG: reads value of a selected register.
- SET\_DPIN: sets value of a selected digital pin.
- GET\_DPIN: gets value of a selected digital pin.
- · GET\_APIN: gets value of a selected analog pin. Returned value is in mV.
- PAUSE: shows a dialog with user defined message. The script is paused until the user cofirms the dialog.
- EXIT: stops execution of the script.
- SET\_MODE: sets device mode. List of modes depends on a device.

#### **Command format**

The following table describes command parameters. All paramaters are mandatory.

	lst parameter	2nd parameter	3rd parameter	4th parameter	5th parameter
SET_REG	Device	Reg. set	Reg. name / Reg. address	Reg. value	-
GET_REG	Device	Reg. set	Reg. name / Reg. address	-	-
SET_DPIN	Device	Pin name	Dig. pin value	-	-
GET_DPIN	Device	Pin name	-	-	-
GET_APIN	Device	Pin name	-	-	-
PAUSE	Message	-	-	-	-
EXIT	-	-	-	-	-

Description of command parameters mentioned in the table above:

- Device: device name (alias used in application).
- Reg. set: register set name. Register sets allows to associate registers which have similar function.
- Reg. name: register name as defined in datasheet.
- Reg. address: register address in decimal or hexadecimal (with 0x prefix) format.
- Reg. value: register value in decimal or hexadecimal (with 0x prefix) format.
- Pin name: name of digital or analog pin as defined in device datasheet.
- Dig. pin value: value of digital pin. Allowed strings are 'low' and 'high'.
- Message: a message to be displayed in a dialog. It cannot contain ':' character, which is used as delimiter of
- parameters.
- Mode: name of a device mode.

Figure 27 shows an example to build a command from the panel.

## KITFS85AEEVM evaluation board

	FS85 Script editor					
	Device: FS	\$85	•	Commands:		
	<ul> <li>Digital pins</li> </ul>			SET_REG:FS85:function	al:M_REG_CTRL1:0x0800	
	Analog pins			Comma	and Built	
	<ul> <li>Registers</li> </ul>					
	Operation:	Write reg.	•			
	Reg. set:	functional	•			
	Reg. name/address:	M_REG_CTRL1	•			
	Reg. value:	0x0800				
	Build	 Command			aaa-032336	
Figure 27. B	uild a command	1				

The value 0x0800 is sent to the register M\_REG\_CTRL1 (BUCK2DIS). The user can then send it to the device by clicking the arrow (see <u>Figure 28</u>).

	Send Script	
	aaa-032337	
Figure 28. Send scrip	t	
	Commands:	
	// This command will disable // Regulator BUCK2 SET_REG:FS85:functional:M_REG_CTRL1:0x0800	
Figure 29. Correct for	mat	
	Commands:	
	// This command will disable Regulator BUCK2 SET_REG:FS85:functional:M_REG_CTRL1:0x0800	
Figure 30. Wrong form	nat ("//" missing in second line)	

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### 8.3.2 Script sequence files

The Script editor allows the user to save script sequence files. A script sequence file is text file that contains a set of commands sent to the device in the order they are written, as shown in the following example.

```
// FS85_Release_FS0b
SET_REG:FS85:safety:FS_WD_WINDOW:0x0200
SET_REG:FS85:safety:FS_NOT_WD_WINDOW:0xF50F
SET_REG:FS85:Write_INIT_Safety:FS_I_SAFE_INPUTS:0x51C6
SET_REG:FS85:write_INIT_Safety:FS_I_NOT_SAFE_INPUTS:AC18
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
```

Note: Comments can be added with a // prefix.

## 8.4 Understanding the FS85 workspace

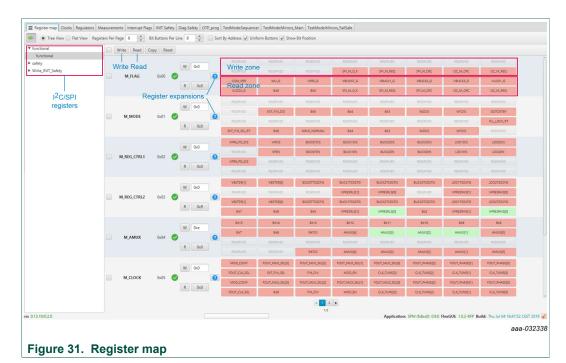
The FS85 workspace consists of several tabs, each dedicated to a specific aspect of device functionality or configuration.

- · Register map
- Clocks
- Regulators
- Measurements
- Interrupt flags
- · INIT safety
- Diag safety
- OTP programming
- TestMode:Sequencer
- TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe

#### 8.4.1 Register map

All SPI/I2C registers can be accessed in write and read mode using this tab.

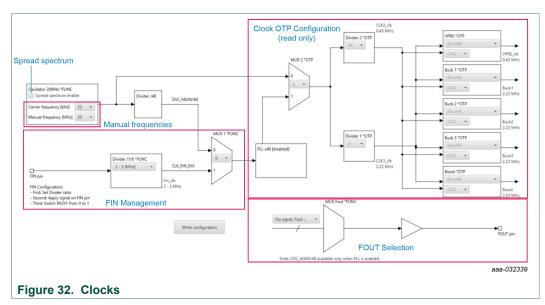
### **KITFS85AEEVM** evaluation board



#### · Register map: allows access to functional register, safety register and write init register which are accessible only during initialization phase

- Read: allows you to read any register either individually or by bank
- Write: allows you to write any register either individually or by bank
- · Register expansion: displays the value of each device parameter

#### 8.4.2 Clocks



This tab allows:

OTP:

• Read current OTP configuration (write operation is not possible). To display the accurate data, the device needs to operate in Test mode.

KITFS85AEEVM evaluation board

SPI/I2C:

- · Configure the device to work with FIN input
- Select the signal to apply on FOUT pin
- Play with manual frequencies and spread spectrum

#### 8.4.3 Regulators

The regulator has two main areas:

- · Low voltage (LV) regulators configuration
- VPRE compensation network calculation

Each regulator can either be enabled or disabled by SPI/I2C. The thermal shutdown behavior can be configured to either shutdown the regulator, or shutdown the regulator and transition to deep fail-safe. The write button applies to the entire table. The VPRE compensation network calculator helps to define the value for VPRE external compensation network.

Low Voltage Regulators						VPRE compensation network calculation
LV	Buck1		LV Buck2	VPRE [V]		
	Disable	-	State in normal mode	Disable	-	VPRE ILIM [mV]
Behavior in case of TSD	Regulator_Shutdown	•	Behavior in case of TSD	Regulator_Shutdown	•	Switching Frequency [KHz]
						Rshunt [mOhm]
LV	Buck3			LDO1		Cout [uF]
itate in normal mode	Disable	-	State in normal mode	Disable	-	Lvpre [uH]
Sehavior in case of TSD	Regulator_Shutdown	•	Behavior in case of TSD	Regulator_Shutdown	•	Rcomp [KOhm] N/A Ccomp [nF] N/A
						Chf [pF] N/A
1	LDO2			VBOOST		Current limit [A] N/A Slope compensation [mV/us] N/A
itate in normal mode	Disable 🔹	•	State in normal mode	Disable	-	siope compensation (invos) 10 A
Behavior in case of TSD	Regulator_Shutdown	•	Behavior in case of TSD	Regulator_Shutdown	-	
		Wri	te			Calculate

#### 8.4.4 Measurements

This tab enables two features:

- Read any of the AMUX signals over time
- Display regulator voltage summary

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## 8.4.5 Interrupt flags

This tab allows you to set or clear flags. It is also possible to mask the interruption.

	Over/under-	-voltage			Over-terr	nperature	
	Status	Clear	Mask		Status	Clear	Mask
VSUP UVH		$\checkmark$	INT_not_mas	sked LDO1 shutdown			INT_not_maske
VSUP UVL		$\checkmark$	INT_not_mas	sked LDO2 shutdown			INT_not_maske
VSUP UV7		$\checkmark$	INT_not_ma	sked BUCK1 shutdown			INT_not_maske
VPRE UVH		$\checkmark$	INT_not_ma	sked BUCK2 shutdown			INT_not_maske
VPRE UVL		$\checkmark$	INT_not_ma	sked BUCK3 shutdown			INT_not_maske
VPRE FB_OV			INT_not_ma	sked VBOOST shutdow	n		INT_not_maske
VBOS UVH		$\checkmark$	INT_not_ma	sked BOS			INT_not_maske
VBOOST UVH		$\checkmark$	INT_not_ma	sked	Write	ead Poll	
VBOOST OV			INT_not_mas	sked			
	Write Read	d Poll					
	Over-cur Status	rrent Clear	Mask		Miscell Status	aneous Clear	Mask
LDO1		Clear		sked			Mask
LDO1 LDO2		Clear	INT_not_ma				Mask
		Clear		sked LDO2 ST			Mask
LDO2		Clear	INT_not_ma	sked LDO2 ST sked BUCK1 ST			Mask
LDO2 BUCK1			INT_not_ma: INT_not_ma: INT_not_ma:	sked LDO2 ST sked BUCK1 ST sked BUCK2 ST			Mask
LDO2 BUCK1 BUCK2		Clear	INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma:	sked LDO2 ST sked BUCK1 ST sked BUCK2 ST sked BUCK3 ST			Mask
LDO2 BUCK1 BUCK2 BUCK3		Clear	INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma:	sked LDO2 ST sked BUCK1 ST sked BUCK2 ST sked BUCK3 ST sked VBOOST ST			Mask INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status (	Clear	INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma:	sked LDO2 ST sked BUCK1 ST sked BUCK2 ST sked BUCK3 ST sked VBOOST ST		Clear	
LDO2 BUCK1 BUCK2 BUCK3 VBOOST		Clear	INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma:	sked LDO2 ST sked BUCK1 ST sked BUCK2 ST sked BUCK3 ST sked VBOOST ST sked WK1 FLG		Clear	INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status (	Clear	INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma:	sked LDO2 ST sked BUCK1 ST sked BUCK2 ST sked BUCK3 ST sked VBOOST ST sked WK1 FLG WK2 FLG		Clear	INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status (	Clear	INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma: INT_not_ma:	sked LDO2 ST sked BUCK1 ST sked BUCK2 ST sked BUCK3 ST vBOOST ST sked WK1 FLG WK2 FLG WK1 RT	Status	Clear	INT_not_maske

### 8.4.6 INIT safety

This tab allows you to manage all registers that can be configured to close the initialization phase. Note that the initialization phase is closed by the first good watchdog refresh before 256 ms timeout.

	Fault impact						
Fault source	Settings	FSOB RSTB		Error counters limit		OV/UV Safe Reacti	on 1
COREMON_OV	No_effect 👻		WD_ERR_LIMIT	6 -	6	VCore ABIST2	No_ABIST
DDIO_OV	No_effect 👻		WD_RFR_LIMIT	6 -	6	VDDIO ABIST2 VMon1 ABIST2	No_ABIST No_ABIST
MON1_OV	No_effect 👻		FLT_ERR_CNT_LIMIT	6 👻	6	VMon2 ABIST2	No_ABIST
MON2_OV	No_effect 👻					VMon3 ABIST2	No_ABIST
MON3_OV	No_effect 👻					VMon4 ABIST2	No_ABIST
MON4_OV	No_effect 👻						
COREMON_UV	FSOB 👻			Safe Inputs		Miscellaneous	
DDIO_UV	FSOB 👻		FCCU pin config	FCCU1_FCCU2_pair *	FCCU1_FCCU2_pair	RSTB pulse duration 10ms	• 10ms
MON1_UV	FSOB 👻	•	FCCU12 polarity FCCU1 polarity		FCCU1_L_FCCU2_H FCCU1_L	Assert RSTB on FS0B short Disable clock monitoring	RESET_asserted Monitoring_activ
MON2_UV	FSOB 👻		FCCU2 polarity		FCCU2_L	Disable clock monitoring Disable 8S timer	Counter_enables
MON3_UV	FSOB 👻		FCCU1 polarity impact	$\checkmark$	FSOB_RSTB		
MON4_UV	FSOB 👻		ERRMON polarity		Negative_edge		
CCU12	FSOB_RSTB -		ERRMON timing config	8ms -	8ms		
CCU1	FSOB_RSTB -						
CCU2	FSOB_RSTB -			Static Voltage Scaling			
RRMON	FSOB_RSTB -		Static voltage scaling	0mV 👻	0mV		
VD_FS_IMPACT	FSOB_RSTB -						
LT_ERR_IMPACT	FSOB_RSTB -						
npact							
lo impact							
	Write Read				Write Rea	d	
							aaa-032

### 8.4.7 Diag safety

The watchdog type configured in the OTP has to be manually selected in the dropdown list to play with the watchdog features. If the user is not aware about the type of watchdog configured in the OTP, it can be found in TestMode:Mirrors\_Failsafe and Miscellaneous tabs.

## KITFS85AEEVM evaluation board

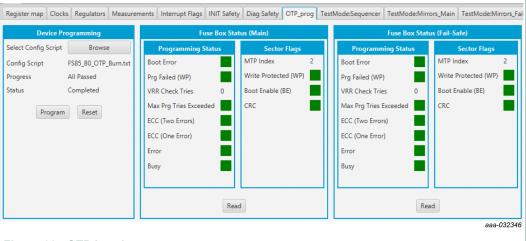
Register map Clocks Regulators Measurements Interrup	t Flags INIT Safety Diag Safet	ty OTP_prog Test	tMode:Sequencer	TestMode:Mirrors_Main T	estMode:Mirrors_F	ailSafe
Safe IO	Diag	j. Safety		IN	TB Mask	
Report PGCOD change         N/V           Report PGCOD event         N/V           Report PGCOD sense         N/V	FCCU12 error FCCU1 error FCCU2 error		N/V N/V	VMON4 OV/UV int. enable VMON3 OV/UV int. enable VMON2 OV/UV int. enable		N/V N/V N/V
Xxternal reset         N/V           SSTB driver         N/V           SSTB sense         N/V	ERRMON acknowledge ERRMON input error ERRMON input status		N/V N/V	VMON1 OV/UV int. enable VDDIO OV/UV int. enable VCOREMON OV/UV int. enab		N/V N/V N/V
ISTB event N/V ISTB diag N/V ISTB request	WD refresh status WD timing SPI CLK status		N/V 8	WD refresh int. enable ERRMON int. enable FCCU2 int. enable FCCU1 int. enable		N/V N/V N/V
S0B driver         N/V           S0B sense         N/V           S0B ding         N/V           S0B request         Image: Solar of the sense           Ioto INIT fail-safe         Image: Solar of the sense	SPI access status SPI CRC status I2C CRC status I2C access status		N/V F N/V N/V N/V	CCO Fint enable		N/V
Write Read	Write	Read		Write	Read	
Watchdog management	OV/L	JV status		Flags	and Status	
Vatchdog Type     Simple_WD        Sood watchdog refresh     WD ANSWER Good       Vad watchdog refresh     WD ANSWER Bad       S0B release     FSRELEASE_FS0B Command       S0B release     FS0B release script       VD_ERE_CN T     VD_REC_NT       UT_ERE_CNT     Disable *       N/V     N/V       VD_W_PERIQD     31.25 *       VDW_RECCVERY     Disable *	YDDIO OV           YDDIO UV           VMON4 OV           YMON4 UV           YMON3 OV           YMON3 UV           YMON2 OV           YMON2 OV           YMON2 UV           YMON2 UV           YMON2 UV           YMON1 OV           YMON1 UV		NV         1           NV         1	Communication error WD refresh error O error Voltage monitoring error ABIST1 status ABIST2 status BIST_OK status Test Mode Activation Status Leave debug mode Debug mode DTP bit corruption NIT register corruption Fail-safe machine state	N/V N/V N/V N/V N/V N/V N/V N/V N/V N/V	
Write Read	Write	Read		Write	Read	
	cript to release FS0b pi rom power-up	n when				
Send right FS_RELEASE_FS0B	register value					
Select the current watchdog OTP config before to use the watchdog management Figure 37. Diag safety						aaa-0323

The FS\_Release\_FS0B command calculates and sends the right secure16-bit word to release FS0B.

A simplified way to release FS0B after power up is to, first, select the right type of watchdog configured in the OTP, then, hit FS0B Release script button. This sends the right sequence to close the initialization sequence, sets the error counter back to 0, then releases FS0B.

## 8.4.8 **OTP** programming

This tab allows you to burn the OTP using a script generated by the excel file OTP configuration (see <u>Section 7.1 "Generating the OTP configuration file "</u>).



#### Figure 38. OTP burning

To set up the hardware before OTP burning, see <u>Section 7.3 "Programming the device</u> with an OTP configuration".

See Figure 38 and follow the steps:

- Browse and load the script file you want to burn. The program button is then available.
- Click Program.

FlexGUI pops up to turn the 8.0 V On, and then turns Off. Note that the blue LED on the board indicates that an 8.0 V voltage is available on the Debug pin. This voltage is used only during the burning process, and should not be applied in any other configuration. At the end of the first OTP programming, the MTP index = 1, WP, BE and CRC flags are green.

The Sector Flags area provides status <u>Table 19</u> provides the state of main flags after a read. This helps to determine how many times the part was burned.

OTP burning step	BE	WP	CRC	MTP Index
OTP not burn Mirrors Empty	Red	Red	Red	1
OTP not Burn Mirrors Filled	Red	Red	Green	1
1	Green	Green	Green	1
2	Green	Green	Green	2
3	Green	Green	Green	3

#### Table 19. OTP burning flag status

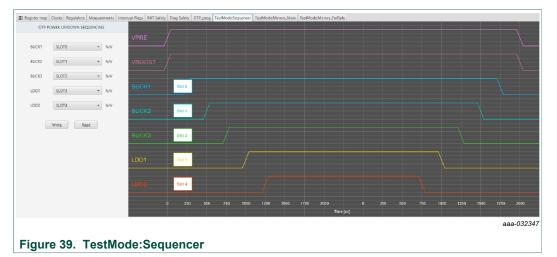
Example shown in Figure 38 corresponds to the OTP burning step 2 from Table 19.

To check if a valid OTP configuration is already burned, switch  $V_{BAT}$  Off, then On, and start the device. The device starts with the OTP configuration.

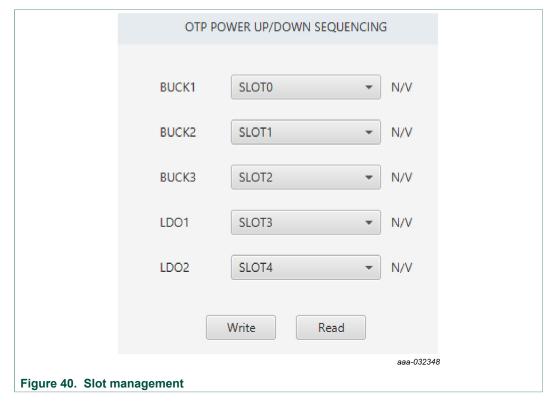
### 8.4.9 TestMode:Sequencer

The sequencer allows you to display the slot configuration for the device. To be able to access this tab, the device has to be in Test mode. The configuration is read from mirror register. It is possible to modify it and update the mirror register.

As an example, the slot sequence is filled at start up with the content of OTP fuses. Then the user can decide to modify any of the configurations coming from the OTP fuse. Note that all these actions are done with Debug pin at 5.0 V and in test mode.



Use the drop-down button (see <u>Figure 40</u>) to select the appropriate slot. The selection configuration can be sent to the device by clicking Write button. The current status can be read by using Read button.



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## 8.4.10 TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe

The TestModeMirrors\_Main and TestModeMirrors\_FailSafe tabs allow access to the OTP main mirrors and fail-safe registers. These tabs are available in Test mode.

Write	e Read		W	rite Read			Write Read	
			Device I2C address	D1	▼ D1			
			Synchronization with 2 devices	Enabled	▼ Enabled			
	Divide10 - Divide10		Synchronization with 1x FS85 or 1x PF8					
	Divide8 • Divide8		Deep Fail-safe autoretry enable	Disabled	<ul> <li>Disabled</li> </ul>	Regulator assigned to VDDIO (C	-	- VPR
	Disabled • Disabled		Deep Fail-safe infinite autoretry enable		<ul> <li>Disabled</li> </ul>	VSUP Under Voltage Threshold		• 6.2)
	стоск			SM			VSUP UV/OV	
Write	e Read		W	rite Read			Write Read	
						Soft start/stop configurability	3.47mV/us	▼ 3.47mV/us
BUCK1 and BUCK2 Soft start/stop configura	7.81mV/us *	7.81mV/us				Regulator behavior in case of	BUCK3 shutdown	▼ BUCK3 shute
Regulator behavior in case of TSD	BUCK1 shutdown + 👻	BUCK1 shutdown +	Regulator behavior in case of TSD	SUCK2 shutdown	BUCK2 shutdown	BUCK3 clock selection	CLK_DIV1	▼ CLK_DIV1
UCK1 clock selection	CLK_DIV1 -	CLK_DIV1	BUCK2 clock selection C	LK_DIV1 -	CLK_DIV1	BUCK3 phase (delay) selection	Delay2	▼ Delay2
BUCK1 phase (delay) selection	Delay2 ~	Delay2	BUCK2 phase (delay) selection	Delay1 -	Delay1	BUCK3 sequencing slot	Slot1	✓ Slot1
BUCK1 sequencing slot	Slot1 -	Slot1	BUCK2 sequencing slot	ilot2 -	Slot2	BUCK3 gain control	1	* 1
8UCK1 Compensation Network	65GM ~	65GM	BUCK2 compensation network 0	) -	0	BUCK3 compensation resistor	Default	▼ Default
BUCK1 & VBUCK2 multiphase operation	Enabled 👻	Enabled	VBUCK2 current limitation 0	, -	0	VBUCK3 current limitation	2.6A	▼ 2.6A
/BUCK1 current limitation	0 ~	0	BUCK2 enable E	nabled 👻	Enabled	BUCK3 inductor selection	1uH	▼ 1uH
BUCK1 inductor selection	1.5uH 👻	1.5uH	BUCK2 inductor selection. 1	uH 👻	1uH	BUCK3 enable	Disabled	<ul> <li>Disabled</li> </ul>
/BUCK1 output voltage	17 👻	17	VBUCK2 output voltage	7	17	VBUCK3 output voltage	2.8V	▼ 2.8V
	BUCK1			BUCK2			BUCK3	
mit								
Write	Read		W	rite Read			Write Read	
			Regulator behavior in case of TSD	BOOST shutdown	▼ BOOST shut			
			BOOST clock selection	CLK_DIV2	<ul> <li>CLK_DIV2</li> </ul>			
/PRE clock selection	CLK_DIV1 +	CLK_DIV1	BOOST phase (delay) selection	Delay1	✓ Delay1			
Delay to turn OFF VPRE at device power down	32ms 👻	32ms	VBOOST Low Side slew rate control	1	▼ 1	Regulator behavior in case o	LDO1 shutdown 👻	LDO1 shutdown
/PRE phase (delay) selection	Delay2 👻	Delay2	VBOOST current limitation	0	• 0	LDO1 sequencing slot	Slot1 ~	Slot1
ligh Side slew rate control	260mA ~	260mA	Compensation Network Capacitor C	1	* 1	VLDO1 output voltage	1.2V -	1.2V
Low Side slew rate control	130mA -	130mA	Compensation Network Resistor Rco	750Kohms	<ul> <li>750Kohms</li> </ul>	VLDO1 current limitation	400mA -	400mA
Current limitation threshold	50mV ~		VBOOST slope compensation	17	* 17	Regulator behavior in case o	LDO2 shutdown + •	
Slope compensation	170mV/us -	170mV/us	BOOST minimum ON time	60ns	<ul> <li>60ns</li> </ul>	LDO2 sequencing slot	Slot2 *	
Dutput voltage	17 *	17	BOOST enable	Disabled	<ul> <li>Disabled</li> </ul>	VLDO2 output voltage	1.2V *	
/PRE mode	VPRE Force PWM +	Force PWM	Output voltage	BOOST 1	<b>v</b> 1	VLDO2 current limitation	LDOs 400mA ~	400mA

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# UM11193

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V	MON1		V	MON2		VI	монз	
Overvoltage threshold [%]	112 👻	112	Overvoltage threshold [%]	112 👻	112	Overvoltage threshold [%]	112 👻	112
Overvoltage Filtering Timing [us]	45 👻	45	Overvoltage Filtering Timing [us]	45 👻	45	Overvoltage Filtering Timing [us]	45 👻	45
Undervoltage threshold [%]	88 💌	88	Undervoltage threshold [%]	88 💌	88	Undervoltage threshold [%]	88 👻	88
Undervoltage Filtering Timing [us]	25 🔹	25	Undervoltage Filtering Timing [us]	25 🔹	25	Undervoltage Filtering Timing [us]	25 🔹	25
Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigne
Assignment to ABIST1		Not_Assigned	Assignment to ABIST1		Not_Assigned	Assignment to ABIST1		Not_Assigne
Monitoring		Disabled	Monitoring		Disabled	Monitoring		Disabled
write	Read		write	Read		write	Read	
V	MON4		v	'DDIO		v	CORE	
Overvoltage threshold [%]	112 🔹	112	Overvoltage threshold [%]	112 -	112	Overvoltage threshold (BUCK1) [%]	112 -	112
Overvoltage Filtering Timing [us]	45 💌	45	Overvoltage Filtering Timing [us]	45 💌	45	Overvoltage Filtering Timing [us]	45 💌	45
Undervoltage threshold [%]	88 👻	88	Undervoltage threshold [%]	88 👻	88	Undervoltage threshold [%]	88 👻	88
Undervoltage Filtering Timing [us]	25 💌	25	Undervoltage Filtering Timing [us]	25 👻	25	Undervoltage Filtering Timing [us]	25 👻	25
Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigne
Assignment to ABIST1		Not_Assigned	Assignment to ABIST1		Not_Assigned	Assignment to ABIST1		Not_Assigne
Monitoring		Disabled	Voltage selection	3.3V -	3.3V	Monitoring voltage (VBUCK1)	1.25V -	1.25V
write	Read		write	Read		write	Read	
		Miscell	aneous					
SVS max value allowed NoSVS	<ul> <li>NoSVS</li> </ul>	RSTB assign	ment to PGOOD	Not_Assigned				
Watchdog monitoring	✓ Enabled	Watchdog n	node Simple_WD	▼ Simple_WD				
ERRMON monitoring	Disabled	FCCU monit	oring	Disabled				
Fault recovery strategy	Disabled	Device I2C a	ddress D0	• D0				
		write	Read					

#### Figure 42. TestMode: Mirrors\_FailSafe

The Read button provides the current status. The Write button changes the configuration in mirror register. This can be useful, for example, to modify few parameters from OTP fuse to start up the board.

## 9 References

- [1] **KITFS85AEEVM** detailed information on this board, including documentation, downloads, and software and tools <u>http://www.nxp.com/KITFS85AEEVM</u>
- [2] **FS8500** product information on FS8500, Safety system basis chip for S32 microcontrollers, ASIL D capable <u>http://www.nxp.com/FS8500</u>
- [3] FS8400 product information on FS8400, Safety system basis chip for S32 microcontrollers, ASIL B capable <u>http://www.nxp.com/FS8400</u>
- [4] FS85\_FS84\_OTP\_Config.xlsm OTP configuration file

## 10 Revision history

Revision	history		
Rev	Date	Description	
v.2.1	20200130	<u>Section 2, Section 3.4, Section 4.4</u> : fixed links (tool summary)	
v.2	20191206	<ul> <li><u>Section 8.1</u>: updated Figure 23</li> <li><u>Section 8.2</u>: updated description and Figure 24</li> <li><u>Section 8.3</u>: updated Figure 26</li> <li><u>Section 8.4.1</u>: updated Figure 28</li> <li><u>Section 8.4.1</u>: updated Figure 31</li> <li><u>Section 8.4.6</u>: updated Figure 32</li> <li><u>Section 8.4.6</u>: updated Figure 36</li> <li><u>Section 8.4.3</u>: updated Figure 33</li> <li><u>Section 8.4.10</u>: updated Figure 41</li> </ul>	
v.1	20190220	Initial version	

### KITFS85AEEVM evaluation board

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