## **UM11157** KITFS85FRDMEVM evaluation board Rev. 3 – 6 December 2019

**User manual** 



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## 1 Introduction

This document is the user guide for the KITFS85FRDMEVM evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of FS8500 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS8500 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITFS85FRDMEVM enables development on FS84/FS85 family of devices. The kit can be connected to the FlexGUI software which allows you to play with registers, try OTP configurations, and burn the part.

It is delivered with empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. The board contains a superset device (MC33FS8530AE0S), allowing tests on all the FS84/FS85 derivatives.

## 2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <u>http://www.nxp.com</u>.

The information page for KITFS85FRDMEVM evaluation board is at <u>http://www.nxp.com/</u> <u>KITFS85FRDMEVM</u>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS85FRDMEVM evaluation board, including the downloadable assets referenced in this document.

## 2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <u>http://community.nxp.com</u>.

## 3 Getting ready

Working with the KITFS85FRDMEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

## 3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm
- · Jumpers mounted on board

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## 3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

• Power supply with a range of 8.0 V to 40 V and a current limit set initially to 1.0 A (maximum current consumption can be up to 6.0 A)

## 3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7 or Windows 10

## 3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at <u>http://www.nxp.com/</u> <u>KITFS85FRDMEVM</u> or from the provided link.

- FlexGUI latest version
- FS85\_FS84\_OTP\_Config.xlsm
- Java installation <u>https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</u>

## 4 Getting to know the hardware

The KITFS85FRDMEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU installed on the board, combined with the FlexGUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signal, like DC/ DC switcher node is mapped on test points. Digital signals (SPI, I2C, RSTB, etc.) are accessible through connectors. Pin WAKE1 pin has a switch to control (Ignition) them. A VBAT switch is available to power On or Off the device.

This board can be operated in Emulation mode or in OTP mode. In emulation mode, as long as the power is supplied, the board configuration stays valid. The OTP mode uses the fused configuration. The device can be fused three times. In OTP mode, the device always starts with the fused configuration, except if the user wants to overwrite OTP configuration using Emulation mode. This board is able to fuse the OTP without any extra tools or board.

## 4.1 Kit overview

The KITFS85FRDMEVM is a hardware evaluation tool that allows performance test. The FS85xx part soldered on the board can be fused three times (see <u>Section 7.3</u> "Programming the device with an OTP configuration").

An Emulation mode is possible to test as many configurations as needed. The voltage monitoring hardware configuration is done through resistors. Note that this configuration can be changed by selecting the appropriate bridge resistors:

- VMON1: assigned to VPRE, 4.1 V
- VMON2: assigned to EXT\_MON2 (VMON bridge for 3.3 V input)

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- VMON3: assigned to BUCK3, 2.3 V
- VMON4: assigned to EXT\_MON4 (VMON bridge for 5.0 V input)

This configuration can be changed by installing appropriate bridge resistors. This board was designed to sustain up to 6.0 A total on  $V_{PRE}$ .

Layout is done using six layer PCB stack up and by following the rules for DC-DC converter layout design. The FS84/FS85 family can be evaluated with this board as it is populated with a superset part. The FS84xx supports ASIL B design, while FS85xx supports ASIL D design.

An external LDO provides VDDI2C voltage with a choice of 1.8 V or 3.3 V (default). VDDIO is assigned by default to VDDI2C. From USB voltage, an external DC-DC generates the OTP programming voltage (8.0 V) without any need for an external power supply.

## 4.1.1 KITFS85FRDMEVM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE output capability up to 6.0 A (external MOSFET)
- VBUCK1/2 in Standalone (default) or Multiphase mode, up to 3.6 A peak
- VBUCK3 up to 3.6 A peak
- VBOOST 5.0 V or 5.74 V, up to 400 mA
- LDO1 and LDO2, from 1.1 V to 5.0 V, up to 400 mA
- · Ignition key switch
- · FS0B external safety pin
- Embedded USB connection for easy connection to software GUI (access to SPI/I2C bus, IOs, RSTB, FS0B, INTB, Debug, MUX\_OUT, regulators)
- · LEDs that indicate signal or regulator status
- Support OTP fuse capabilities
- USB connection for register access, OTP emulation, and programming

### 4.1.2 VMON configuration

The VMONx configuration is highly dependent on the use case. This kit is delivered with a default configuration shown in bold in <u>Table 1</u>. However, the user can assign VMONx differently to address the use case. As an example, VMON1 could be reassigned from VPRE to LDO1 with a wire connected between LDO1 and EXT\_MON1. In this case, the user has to define the right value for R240 which depends on the nominal voltage. As a consequence, the *Resistor to set column* in <u>Table 1</u>, indicates that R11 and R227 resistors have to be removed.

Table 1 defines how to connect VMONx.

#### Table 1. VMONx voltage assignment

The default configuration on the board is indicated in bold.

VMONx inputs	Assignment	Alternate	Nominal voltage	Resistor to set	Resistor value
VMON1	VPRE	-	4.1 V	R11	90.9 kΩ
		VMON_08V	0.8 V	R227	0 Ω
		EXT_MON1	User	R240	User
VMON2	VMON_08V	-	0.8 V	R228	0 Ω
		EXT_MON2	3.3 V	R7	68.1 kΩ

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# UM11157

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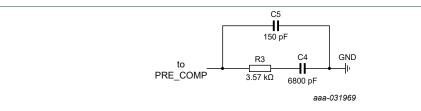
VMONx inputs	Assignment	Alternate	Nominal voltage	Resistor to set	Resistor value
VMON3	BUCK3	-	2.3 V	R38	41.2 kΩ
		VMON_08V	0.8 V	R229	0 Ω
		EXT_MON3	User	R241	User
VMON4	VMON_08V		0.8 V	R230	0 Ω
		EXT_MON4	5.0 V	R40	115 kΩ

VMON\_08V is a fixed voltage at 0.8 V which allows to force the right voltage on VMONx. EXT\_MONx are available from J16 to feed the desired voltage on VMONx (external). In this case, the resistor value from the upper side of the bridge must be defined.

The resistor location is given in *Resistor to set* column in <u>Table 1</u>. *Nominal voltage* column gives the voltage for which VMONx bridge is defined on the board. The bridge low-side resistor is 22.1 k $\Omega$  for each VMON.

## 4.1.3 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 450 kHz. All other VPRE configurations require a new calculation for these components.



#### Figure 2. VPRE compensation network

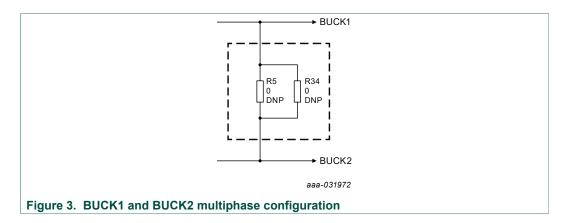
#### Table 2. Compensation network

Components	VPRE 450 kHz	VPRE 2.2 MHz
C4	6.8 nF	1.5 nF
C5	150 pF	22 pF
R3	3.57 kΩ	16.9 kΩ
LPRE	4.7 μH or <b>6.8 μH</b>	<b>1.5 μH</b> , 2.2 μH, or 4.7 μH

### 4.1.4 BUCK1 and BUCK2 multiphase configuration

The board is designed to work independently with BUCK1 and BUCK2. Due to R5 and R34, it is possible to connect both connectors together and work in multiphase.

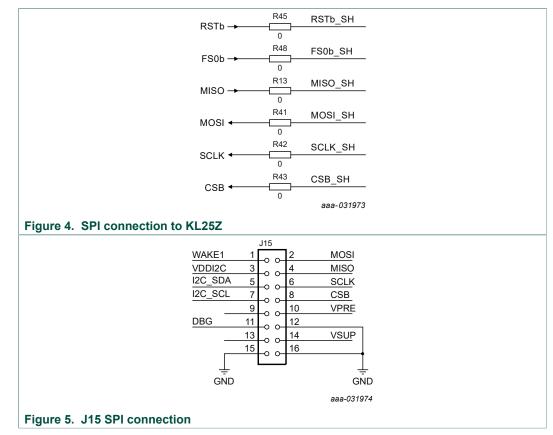
## KITFS85FRDMEVM evaluation board



## 4.1.5 SPI/I2C

The SPI and I2C buses are connected to KL25Z MCU. The user can use either one or the other. The choice can be done at start of the FlexGUI or at any time after launch (see <u>Section 8 "Using FlexGUI"</u>).

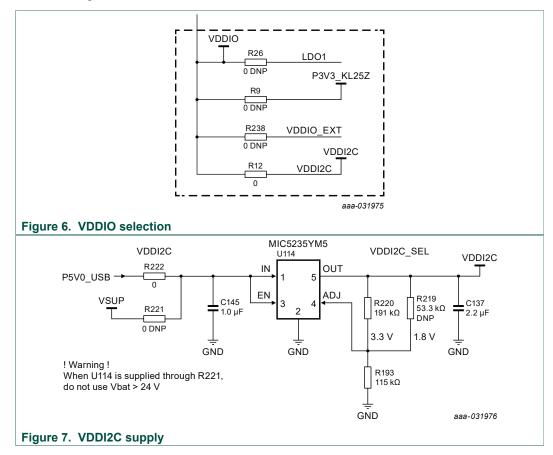
This kit uses a KL25Z MCU to communicate with FlexGUI. It is also possible to connect the SPI to another MCU. In this case, remove R13, R41, R42, and R43 to disconnect the KL25Z MCU (see Figure 4) and connect the external MCU on J15 connector as shown in Figure 5. The external MCU can be connected on J15 connector as shown in Figure 5. In addition to this change, be sure that VDDIO voltage domain is the same on MCU side and SBC side.



## 4.1.6 VDDI2C

An external LDO is provided to feed VDDI2C. This LDO can also be used to feed VDDIO, which is the default implementation.

The I2C is compatible with 1.8 V or 3.3 V, while VDDIO is compatible with 3.3 V and 5.0 V. For this reason, the LDO default configuration is 3.3 V. The LDO is supplied by 5.0 V coming from the USB.

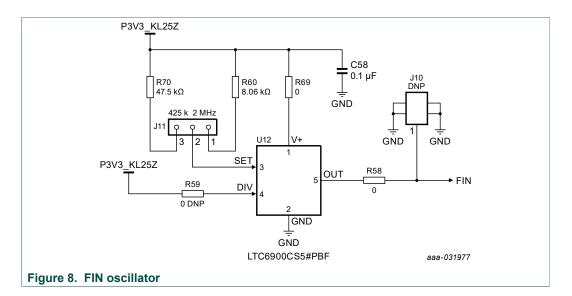


## 4.1.7 FIN external oscillator

In order to ease the FIN evaluation, a standalone oscillator is installed on the board. It supplies either 425 kHz or 2.4 MHz to the FIN input. The configuration is shown in Figure 8.

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## 4.2 Device OTP user configuration

It is recommended to learn about OTP before operating with the device. The device has a high level of flexibility due to parameter configuration available in the OTP. This impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers and the FS85 SoC.

The OTP-related operations can be performed either in Emulation mode, where the product uses a given configuration as long as power supply is not switched Off or from OTP fuse content that is valid even after a power down/power up sequence.

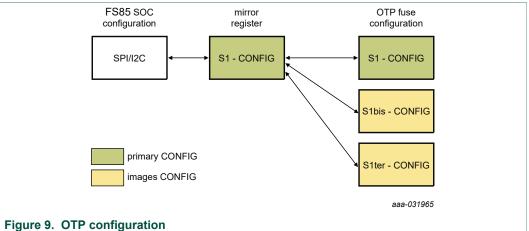
## 4.2.1 OTP and mirrors registers

There are two OTP blocks in the device. One is for the main section, and the other for the fail-safe. During configuration, each of them are using dedicated sectors. The OTP configuration scheme is shown in Figure 9 (same implementation for main and fail-safe).

The device can be fused three times using mirror registers. The user can first load the mirror register content with the desired contents, then decide either to use the device in Emulation mode or to burn the next sector. The first sector to be burned is S1, the second S1bis, and the third S1ter. FlexGUI automatically manages the next sector to be burned. It is not possible to revert to the previous sector. When the user reaches the sector S1ter, there no other possibility for burn, however emulation mode is still available.

**Note:** When device is operating in Emulation mode using configuration from mirror registers, few parameters must be overwritten by SPI/I2C. This concerns regulator TSD behaviors; VPRE slew rate high-side and low-side VBOOST slew rate. See <u>Section 8.4.10 "TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe"</u> for additional details.

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#### Figure 9. OTP configuration

At boot, the content of the valid sector is loaded into the Mirror Register Sector 1. The mirror register content is accessible from FlexGUI by using specific SPI/I2C commands. The mirror configuration is managed by the FlexGUI, which eases the access.

## 4.2.2 OTP hardware implementation

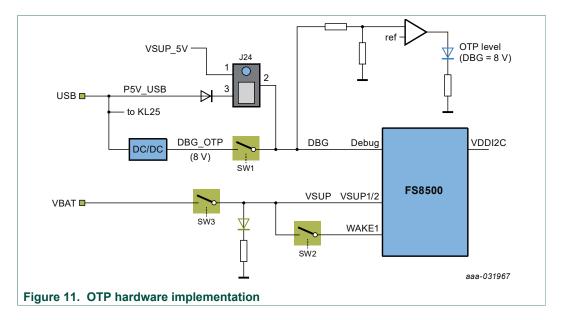
To work in OTP emulation or OTP programming, it is required to start the device in Debug mode.

<u>Figure 10</u> shows the sequence to be followed to enter in Debug mode. The voltage sequence on the kit is done using switches installed on the board, while the OTP registers configuration is managed by the FlexGUI GUI. This is described in detail in the following sections.

	V <sub>DBG</sub>		
DBG			
	> V <sub>SUP_UVH</sub>		
VSUP1/2			
	> WAKE12 <sub>VIH</sub>		
WAKE1			
SPI/I2C	SPI/I2C OTP pgm	]	SPI/I2C
REGx	OFF	PWR UP	ON
			 aaa-031966
e 10. Debug mod	de entry		

Figure 11 shows the hardware kit implementation.

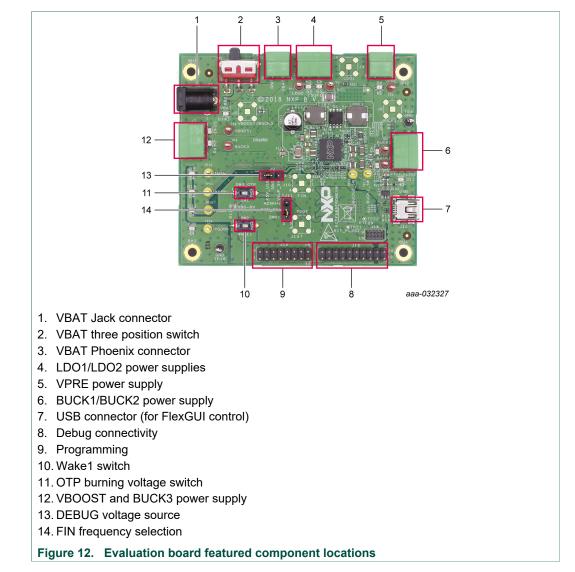
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## 4.3 Kit featured components

Figure 12 identifies important components on the board and <u>Table 3</u> provides additional details on these components.

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#### Table 3. Evaluation board component descriptions

Number	Description	
1	VBAT Jack connector	
2	<ul> <li>VBAT three position switch</li> <li>Left position: board supplied by Jack connector</li> <li>Middle position: board not supplied</li> <li>Right position: board supplied by Phoenix connector</li> </ul>	
3	VBAT Phoenix connector	
4	LDO1/LDO2 power supply	
5	VPRE power supply	
6	BUCK1/BUCK2 power supply	
7	USB connector (for FlexGUI control)	

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Number	Description	
8	Debug connectivity. Access to: • VSUP, GND • FOUT/FIN • PGOOD/RSTB/FS0B • FCCUx • WAKE2 • PSYNC, ERRMON, AMUX • VMONx	
9	Programming <ul> <li>SPI bus</li> <li>I2C bus</li> <li>Debug pin</li> <li>VPRE, VSUP, GND</li> </ul>	
10	WAKE1 switch	
11	OTP burning voltage switch	
12	VBOOST and BUCK3 power supply	
13	Debug voltage source either from USB (recommended) or from VSUP	
14	FIN frequency selection	

## 4.3.1 FS8500/FS8400: Fail-safe system basis chip with multiple SMPS and LDO

### 4.3.1.1 General description

This device family is part of a global platform FS84 (fit for ASIL B) and FS85 (fit for ASIL D), pin to pin and software compatible. The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard. Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

### 4.3.1.2 Features

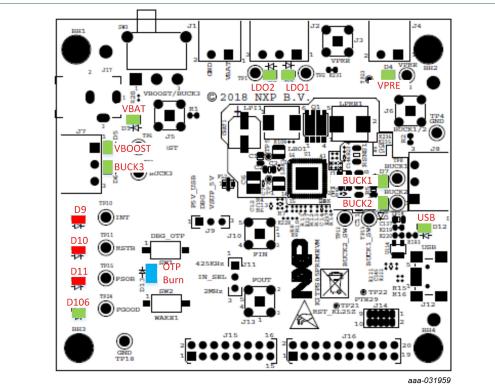
- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- **Based on part number:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on part number**: low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 2.5 A typical peak.

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- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10 µA typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

## 4.3.2 Indicators

The following LEDs are provided as visual output devices for the evaluation board:



#### Figure 13. Evaluation board indicator locations

#### Table 4. Evaluation board indicator descriptions

Label	Name	Color	Description
D1	VBAT	Green	VBAT On
D2	LDO1	Green	LDO1 On
D3	LDO2	Green	LDO2 On

## KITFS85FRDMEVM evaluation board

Label	Name	Color	Description
D4	BUCK1	Green	BUCK1 On
D6	BUCK2	Green	BUCK2 On
D7	BUCK3	Green	BUCK3 On
D8	VBOOST	Green	VBOOST On
D9	VPRE	Green	VPRE On
D12	DBG > 8.0 V	Blue	DBG pin voltage > 8.0 V (OTP programming)
D13	RSTB	Red	RSTB asserted (logic level = 0)
D14	INTB	Red	INTB asserted (logic level = 0)
D15	FS0B	Red	FS0B asserted (logic level = 0)
D16	P3V3_KL25	Green	P3V3_KL25 On

## 4.3.3 Connectors

Figure 14 shows the location of connectors on the board.

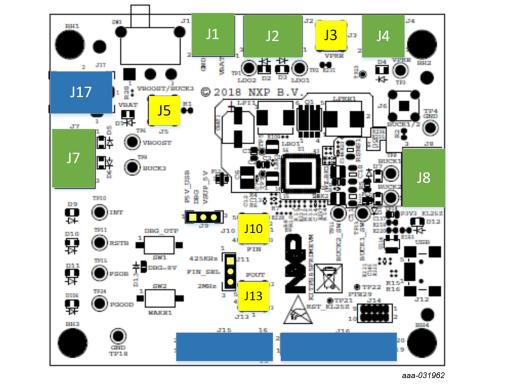


Figure 14. Evaluation board connector locations

## 4.3.3.1 VBAT connector (J1)

VBAT connects to the board through Phoenix connector (J1).

#### Table 5. V<sub>BAT</sub> Phoenix connector (J1)

Schematic label	Signal name	Description
J1-1	VBAT	Battery voltage supply input
J1-2	GND	Ground

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## 4.3.3.2 Output power supply connectors

#### Table 6. BUCK1/BUCK2 connector (J8)

Schematic label	Signal name	Description
J8-1	BUCK2	BUCK2 power supply output
J8-2	BUCK1	BUCK1 power supply output
J8-3	GND	Ground

#### Table 7. VBOOST/BUCK3 connector (J7)

Schematic label	Signal name	Description
J7-1	VBOOST	VBOOST output
J7-2	BUCK3	BUCK3 power supply output
J7-3	GND	Ground

#### Table 8. LDO1/LDO2 connector (J2)

Schematic label	Signal name	Description
J2-1	LDO1	LDO1 power supply output
J2-2	LDO2	LDO2 power supply output
J2-3	GND	Ground

## Table 9. VPRE connector (J4)

Schematic label	Signal name	Description
J4-1	VPRE	VPRE power supply output
J4-2	GND	Ground

## 4.3.3.3 Debug connector (J16)

#### Table 10. Debug connector (J16)

Schematic label	Signal name	Description
J16-1	FOUT	Frequency synchronization output
J16-2	FIN	Frequency synchronization input
J16-3	PGOOD	Power GOOD
J16-4	VMON1_EXT	Voltage monitoring 1, from external reference
J16-5	INTB	Interrupt, active low
J16-6	VMON2_EXT	Voltage monitoring 2, from external reference
J16-7	RSTB	Reset, active low
J16-8	VMON3_EXT	Voltage monitoring 3, from external reference
J16-9	ERRMON	Error monitoring
J16-10	VMON4_EXT	Voltage monitoring 4, from external reference
J16-11	AMUX	Analog multiplexer
J16-12	FS0B_Out	Fail-safe, active low
J16-13	VDDIO_EXT	VDDIO external reference

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Schematic label	Signal name	Description
J16-14	PSYNC	Power synchronization
J16-15	VDDIO	VDDIO used by FS85
J16-16	WAKE2_IN	WAKE2 input
J16-17	FCCU1	Fault collector control unit 1
J16-18	VSUP	VSUP power supply
J16-19	FCCU2	Fault collector control unit 2
J16-20	GND	Ground

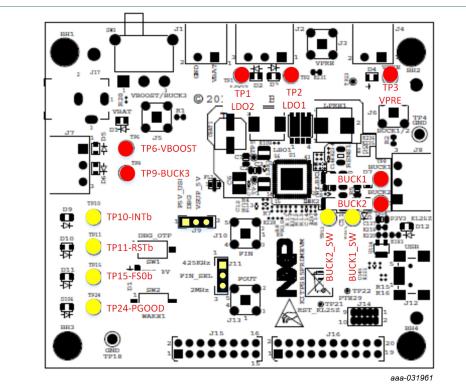
## 4.3.3.4 Program connector (J15)

Schematic label	Signal name	Description
J15-1	WAKE1	WAKE1 input
J15-2	MOSI	SPI master output slave input
J15-3	VDDI2C	VDDI2C voltage
J15-4	MISO	SPI master input slave output
J15-5	I2C_SDA	I2C serial data
J15-6	SCLK	SPI clock
J15-7	I2C_SCL	I2C serial clock
J15-8	CSB	SPI chip select
J15-9	n.c.	not connected
J15-10	VPRE	VPRE output
J15-11	DBG	Connected to Debug pin
J15-12	GND	Ground
J15-13	n.c.	not connected
J15-14	VSUP	Connected to VSUP pin
J15-15	GND	Ground
J15-16	GND	Ground

## 4.3.4 Test points

The following test points provide access to various signals to and from the board.

## KITFS85FRDMEVM evaluation board



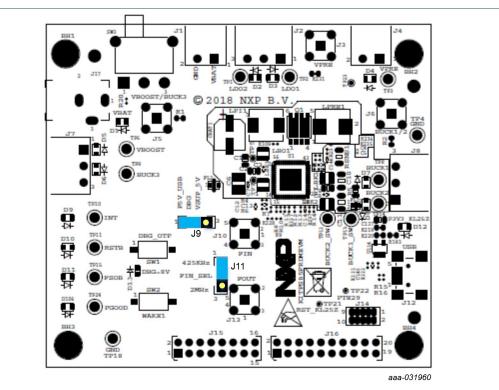
## Figure 15. Evaluation board test points

### Table 12. Evaluation board test point descriptions

Test point name	Signal name	Description
TP1	LDO2	LDO2 regulator output
TP2	LDO1	LDO1 regulator output
TP3	VPRE	VPRE DC/DC regulator output
TP4	GND	Ground
TP6	VBOOST	VBOOS DC/DC output
TP8	BUCK1	BUCK1 DC/DC regulator output
TP9	BUCK3	BUCK3 DC/DC regulator output
TP10	INTB	Interruption signal, active low
TP11	RSTB	Reset signal, active low
TP14	BUCK2	BUCK2 DC/DC regulator output
TP15	FS0B	Fail-safe output, active low
TP18	GND	Ground
TP24	PGOOD	Power GOOD output, active low

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## 4.3.5 Jumpers



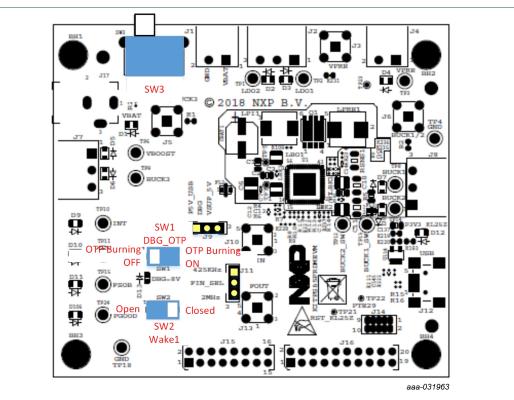
#### Figure 16. Evaluation board jumper locations

#### Table 13. Evaluation board jumper descriptions

Name	Function	Pin number	Jumper/pin function
<b>1</b> 9	VBAT shunt	1-2	DBG voltage produced from VBAT
39	VDAT Shufft	2-3	DBG voltage produced from USB 5.0 V
J11	FIN clock	1-2	FIN set to 2.0 MHz
511	selection	2-3	FIN set to 425 kHz

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## 4.3.6 Switches



#### Figure 17. Switch locations

#### Table 14. SW1

Position	Function	Description
LEFT	OTP programming Off	OTP burning not possible
RIGHT	OTP programming On	8.0 V on DBG pin allows OTP burning (blue LED turns On to indicate this state)

#### Table 15. SW2

Position	Function	Description
OPEN	WAKE1 open	Wake1 pin not connected to $V_{SUP}$
CLOSED	WAKE1 closed	Wake1 pin connected to $V_{SUP}$

## Table 16. SW3

Position	Function	Description
LEFT	VBAT On	VBAT from J17
MIDDLE	VBAT Off	Board not supplied
RIGHT	VBAT On	VBAT from J1

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## 4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS85FRDMEVM evaluation board are available at <u>http://www.nxp.com/KITFS85FRDMEVM</u>.

## 5 Installing and configuring software and tools

This development kit uses FlexGUI software. FlexGUI software is based on Java JRE.

Preparing the Windows PC workstation consists of three steps.

- 1. Install the appropriate Java SE Runtime Environment (JRE).
- 2. Install Windows 7 FlexGUI driver.
- 3. Install FlexGUI software package.

## 5.1 Installing the Java JRE

- 1. Download Java JRE (Java SE Runtime Environment), available at <u>http://</u> <u>www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</u> (8u162 or newer).
- 2. Open the installer and follow the installation instructions.
- 3. Following the successful installation, restart the computer.

## 5.2 Installing Windows 7 FlexGUI driver

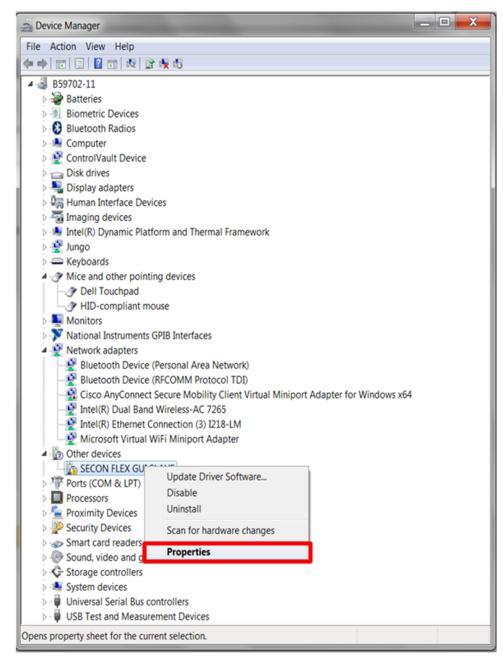
On Windows 7 PCs, a virtual COM port installation is required. Install the Windows 7 FlexGUI driver using the following procedure.

**Note:** On Windows 10, it is not necessary to install virtual com port as Windows 10 uses a generic COM port driver.

- 1. Connect the kit to the computer as described in <u>Section 6 "Configuring the hardware</u> <u>for startup"</u>
- 2. On the Windows PC, open the Device Manager.
- 3. In the **Device Manager** window, right-click on **SECON FLEX GUI SLAVE**, and then select **Properties**.

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aaa-031982

4. In the SECON FLEX GUI SLAVE Properties window, click Update Driver.

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SECON FLE	X GUI SLAVE Prope	erties	x
General	Driver Details		
	SECON FLEX GUI	ISLAVE	
	Device type:	Other devices	
	Manufacturer:	Unknown	
	Location:	Port_#0002.Hub_#0002	
The o	e is no driver selecte	e are not installed. (Code 28) ed for the device information set or element. vice, click Update Driver.	•
		Update Driver	
		Close	ncel
			aaa-031983

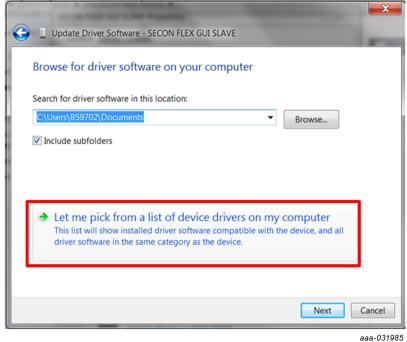
5. in the Update Software Driver window, select Browse my computer for driver software.

lov	v do you want to search for driver software?	
•	Search automatically for updated driver software Windows will search your computer and the Internet for the latest driver software for your device, unless you've disabled this feature in your device installation settings.	
•	Browse my computer for driver software Locate and install driver software manually.	

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 Select Let me pick from a list of device drivers on my computer, and then click Next.



7. Select Ports (COM & LPT) from the list, and then click Next.

Select your device's typ	be from the list bein	OW.	
Common hardware types:			
Network Client			*
Network Protocol			
Service			
Non-Plug and Play Drivers			
PCMCIA adapters			
Portable Devices			
Ports (COM & LPT)			
🖶 Printers			
Processors			=
Proximity Devices			
SBP2 IEEE 1394 Devices			
SD host adapters			
Security Devices			-

8. Click Have Disk.

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	and the film into		ligerte.	L.R.	×
🕒 🧕 Update	Driver Software - S	ECON FL	EX GUI SLAVE		
5	elect the manufact	urer and	vant to install for this har model of your hardware device you want to install, click Have D	and then click Next.	If you have a
Brother Compaq PRC ( III)	turer I port types) GSM Radio Card Iriver is digitally sig ne why driver signir		Model Communications Port ECP Printer Port Multiport Communication Printer Port		ave Disk
				Next	Cancel

aaa-031987

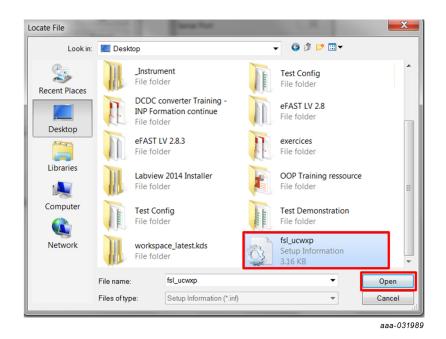
9. Click Browse.

Update Driver Software - SECON FLEX GUI SLAVE	<u> </u>
Select the device driver you want to install for this hardware.	
Select the manufacturer and model of your bardware device and then click I Install From Disk	Vext If you
Insert the manufacturer's installation disk, and then make sure that the correct drive is selected below. Cancel	
A Copy manufacturer's files from: B Browse B This driver is digitally signed.	Disk
Tell me why driver signing is important	DISK
Next	Cancel
	aaa-031988

10.In the Locate File window, locate and select fsl\_ucwxp, and then click Open.

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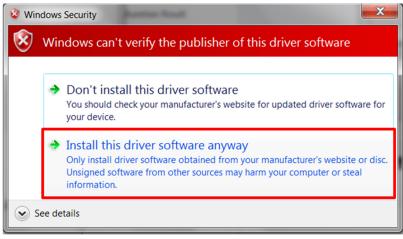
11.In the Install from Disk window, click OK.

Install Fron	n Disk	<b>X</b>
4	Insert the manufacturer's installation disk, and then make sure that the correct drive is selected below.	OK Cancel
	Copy manufacturer's files from: C:\Users\B59702\Desktop	Browse

12.If prompted, in the **Windows Security** window, click **Select this driver software anyway**.

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aaa-031991

13.Close the window when the installation is complete.

Update Driver Software - Virtual Com Port (COM47)	X
Windows has successfully updated your driver software	
Windows has finished installing the driver software for this device:	
Virtual Com Port	
	Close
	aaa-031992

14.In the **Virtual Com Port Properties** window, verify that the device is working properly, and then click **Close**.

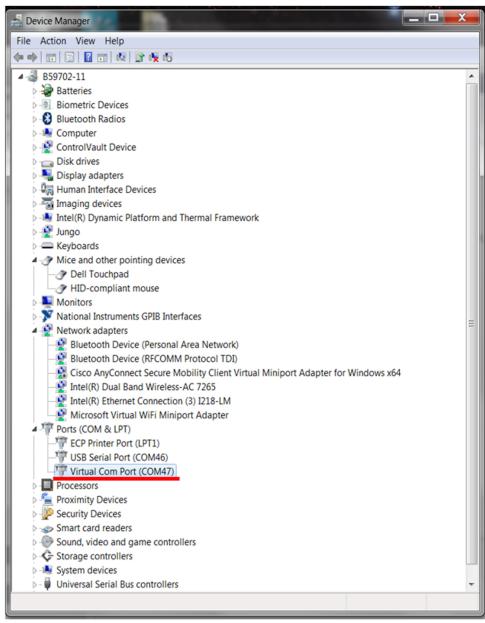
## KITFS85FRDMEVM evaluation board

Virtual Co	om Port (COM47) Pr	operties	×
General	Driver Details		
	Virtual Com Port (	COM47)	
	Device type:	Other devices	
	Manufacturer:	NXP	
	Location:	Port_#0002.Hub_#0002	
	ce status s device is working pr	roperty	
		openy.	
			~
		Close	Cancel

aaa-031993

The Virtual Com Port appears in the Device Manager window.

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aaa-031994

## 5.3 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

- 1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
- 2. Download the latest FlexGUI (32-bit or 64-bit) version, available at <a href="http://www.nxp.com/KITFS85FRDMEVM">http://www.nxp.com/KITFS85FRDMEVM</a>.
- Extract all the files to a desired location on your PC.
   FlexGUI is started by running the batch file, \bin\flexgui-app-fs85.bat.

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# POWER POWER Supply Image: Supply state Supply state Image: Supply state

## 6 Configuring the hardware for startup

Figure 18 presents a typical hardware configuration incorporating the development board, power supply, and Windows PC workstation.

To configure the hardware and workstation as illustrated in <u>Figure 18</u>, complete the following procedure:

1. Install jumpers for the configuration.

Table 17. Jun	nper configuration
Jumper	Configuration
<b>1</b> 9	connect 1-2 (connect 5.0 V on DBG pin from the USB)

2. Configure switches for the configuration.

 Table 18.
 Switch configuration

Switch	Configuration
SW3	middle position (VBAT off)
SW1	open (OTP programming Off)
SW2	open (WAKE1)

- Connect the Windows PC USB port to the KITFS85FRDMEVM development board using the provided USB 2.0 cable.
   Set the DC power supply to 12 V and current limit to 1.0 A. With power turned off, attach the DC power supply positive and negative output to KITFS85FRDMEVM VBAT Phoenix connector (J1).
- 4. Turn on the power supply.
- 5. Close SW2.

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**Note:** At this step, the product is in debug mode and all regulators are turned Off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as J9 jumper is removed.

## 7 Using the KITFS85FRDMEVM evaluation board

This section summarizes the overall setup. Detailed description is provided in the following sections.

Before starting the process, choose the mode you want to run the device.

- In Normal mode, the configuration comes from OTP fuses.
- In Debug mode, you can either use the current configuration from OTP fuse, if any, or use the OTP emulation mode to write in the mirror register.

The Normal mode or Debug mode is defined at startup depending on the DBG pin level.

- Normal mode is set by tying DBG to ground.
- Debug mode is set by setting DBG voltage to 5.0 V.

In OTP emulation, you can overwrite the mirror registers from a given OTP fuse configuration. See <u>Section 4.2.1 "OTP and mirrors registers"</u> and <u>Section 8.3 "Working with the Script editor"</u> to define your configuration.

In OTP fuse configuration, use the configuration fused in the OTP. So, if a valid OTP fuse configuration exists, then it is copied to the mirror registers at startup.

## 7.1 Generating the OTP configuration file

Define and generate your OTP configuration using the excel file *FS85\_FS84\_OTP\_Config.xlsm*. This file allows configuring the device for parameters controlled by the main state machine and the fail-safe state machine.

To generate the script:

1. Fill data in the OTP\_conf\_main\_reg sheet.

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						OTP_REGISTERS					
Register Name		BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BITO	Data_Bin	Data_
TP_CFG_VPRE_	14						EV[5:0]				
		0	0				0 - 5.0V			00100000	0x20
TP_CFG_VPRE_	15		-				SC[5:0]				
		0	0				70mV/µs			00000111	0x0
TP_CFG_VPRE_	16	VPREI	LIM[1:0]	VPRET	OFF[1:0]		SRLS[10]		RHS[1:0]		
		10 - 1;	20mV		40ns	11 - PU/F	D/900mA		PD/130mA	10101100	0zA
TP_CFG_BOOST	17			VPRE_MODE	Reserved		VBST				
		0	0	0 - Force PWM	0		1101 - 1	5.74V		00001101	0z0
P_CFG_BOOST_	18	BOOSTEN		ONTIME[1:0]			VBSTSC[4:0]				
		1 - Enabled		) - 60ns			01100 - 125mV/µs			10001100	0x8
P_CFG_BOOST_	19		OMP[1:0]		:OMP[1:0]		LIM[10]		'SR[1:0]		
		00 - 75	Okohms	00 - 1	125pF		-2A	11 - 51	30V/µ.s	00000111	0z0
P_CFG_BUCK1	1A					VBIV[7:0]					
						0001000 - 1.25V				10001000	Ozt
P_CFG_BUCK1_	1B		otp_SPARE0[2	:0	VBIIND	OPT[1:0]	VBISVI	_IM[1:0]	VB12MULTIPH		
			000		00	ъµН	11 - 4	.5A	0 - Disabled	00000110	Ozt
P_CFG_BUCK2	1C					VB2V[7:0]					
				10000000000		10110001 - 1.8V		1000 0701 57	1 1000 OTDI 211	10110001	0x
P_CFG_BUCK2	1D			IDOPT[1:0]	BUCK2EN		ALIM(1:0)	VB3_CTRL_RC	VB3_CTRL_GM	00011100	Ûx'
P CFG BUCK3	1E	BUCK3EN	0	0 - 1µH JDOPT[1:0]	1 - Enabled	11-	4.5A	0 - Default	0 - Default	00011100	Uz
CFG_BOCK3	15	BUCK3EN 1 - Enabled		100PT[1:0] 0 - 1µH			VB3V[4:0] 10101 - 3.3V			10010101	0z
P CFG BUCK3	1F	1 - Enabled	VB2GMCOMPI			VB1GMCOMP[2:0]	10101 - 3.3 V	UD001	1LIM[1:0]	10010101	UZ
LFG_BOLK3_	· ⊪		100 - 65 GM	20		100 - 65 GM			4.5A	10010011	0x
TP CFG LDO	20	LDO2ILIM	100 - 65 GIVI	LD02V[2:0]		LDOILIM		LD01V[2:0]	4.0M	10010011	UX
JIP_CFG_LDU	20					1-150mA					
		0 - 400mA		111 - 5.0V	100000000	1 - 150mA		111 - 5.0V		01111111	0x
ITP_CFG_SEQ_1	21				VB2S[2:0]			VB1S[2:0]			-
		0	0	000 - F	Regulator Start and Stop i	n Slot 0	000 · R	egulator Start and Stop i	n Slot 0	00000000	Ozt
TP_CFG_SEQ_2	22			444 15 1 1	LD02S[2:0] or does not Start (Enable		000 5	LD015[2:0]	01.0	00111000	0z;
TP CFG SEQ 3	23	DVS BL	U		or does not start (Enable JCK3[1:0]	d by SPirizCj Tslot	000 · R	egulator Start and Stop i VB3SI2:01	n slot u	00111000	UZ.
TP_UFG_SEQ_3	23		UKI2[R0] HmV/µs	DVS_B(	JCKa[£0] HmV/µs	0 - 250as	000 B	egulator Start and Stop i	e Slot 0	00000000	0x0
P CFG CLOCK	24	-		00 - 10.4	VPRE ph[2:0]	0-20005	00011	CLK DIV2[2:0]	11 510( 0	00000000	01
r_cra_clock	24	0	0		000 - delay 0		400	- divide by 44 - CLK2= 455	2011	00000100	Øz
	25				BUCK1 ph[2:0]		100		IK.HZ	00000100	UZ
P_CFG_CLOCK	25							VBST_ph[2:0]		00110000	-
					110 - delay 6			000 - delay 0		00110000	Űz:
P_CFG_CLOCK	26				BUCK3_ph[2:0]			BUCK2_ph[2:0]			-
		0	0		011 - delay 3			000 - delay 0		00011000	Øz
P_CFG_CLOCK	27	BUCK3_clk_sel	BUCK2_clk_sel	BUCK1_clk_sel	VBST_clk_sel	VPRE_clk_sel	PLL_sel		DIV1[1:0]		
		0 - CLK1	0 · CLK1	0 · CLK1	0 - CLK1	1-CLK2	0 - Disabled	10 - divide by 9	- CLK1=2.22MHz	00001010	0z0
TP_CFG_SM_1	28		-				tsd[5:0]				
		0	0		1-BUCK1Shutdown +		1 - BUCK3 Shutdown +	0 - LDO1 Shutdown	0 - LDO2 Shutdown	00010100	0z
TP_CFG_SM_2	29		otp_SPARE1[2	.0	VPRE_off_dly	Autoretry_infinite	Autoretry_en	PSYNC_CFG	PSYNC_EN		
			000		1-32ms	1 - Enabled	1 - Enabled	0 - 2x FS85	0 - Disabled	00011100	Ozi
P_CFG_VSUP_L	2A				otp_SPARE2[6	80]			VSUPCFG		
					0000000				0 - 4.9V for Vpre < 4.5V	00000000	0z
DTP_CFG_I2C	2B						M_I2CDEV				
		0	0	0	0		0001 - Ad			00000001	0x
DTP_CFG_OV	2C	-	-				٧	DDIO REG ASSIGN[2:	0]		
		0	0	0	0	0		100 - BUCK3		00000100	8z6
IP CFG DEVID	2D					DeviceID[7:0]					
	_					00000001				00000001	0z
M SI CRC LS	2E				OTP N	1 S1 CRC LSB[7:0]					34
0_0,0_0					Automatic	ally filled in by Sidence IP				00000000	0z0
M SI CRC M	2F					SI CRC MSB[7:0]				00000000	01
	1 6F					ally filled in by Sidence IP				00000000	0z0

Figure 19. OTP\_conf\_main\_reg spreadsheet example

2. Fill data in the OTP\_conf\_failsafe\_reg sheet.

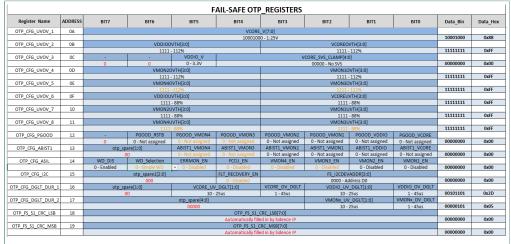
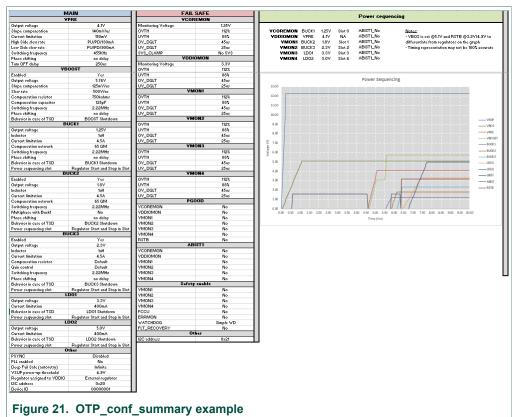


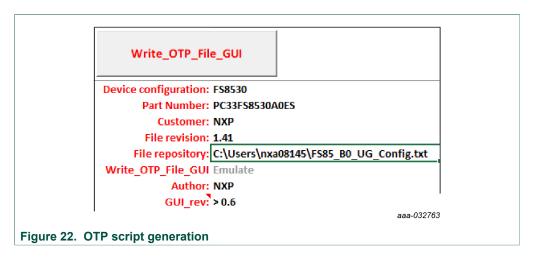
Figure 20. OTP\_conf\_failsafe\_reg spreadsheet example

3. See the **OTP\_conf\_summary** sheet to review the complete configuration (main and fail-safe).

## KITFS85FRDMEVM evaluation board



 Generate script in the OTP\_conf\_file\_generation sheet. Once the configuration is ready, the user can generate the script file. Go to OTP\_conf\_file\_generation, enter the path in the File repository, and then click Write\_OTP\_File\_GUI.



## 7.2 Working in OTP emulation mode

At startup, the device always uses the content from the mirror register. This content can come from OTP fuse or from configuration written directly in the mirror register. OTP emulation means that the user can emulate the OTP writing in the mirror register. This allows trials before burning the OTP.

## KITFS85FRDMEVM evaluation board

- 1. Configure the hardware. See Section 6 "Configuring the hardware for startup".
- 2. Launch the FlexGUI software.
- 3. Switch to Debug mode:
  - a. Place SW3 in the right direction (VBAT switched On).
  - b. Close SW2 (WAKE1).
  - While in Debug mode, all regulators are turned Off.
- 4. Load the mirror registers to work in OTP emulation mode. See <u>Section 8.3 "Working</u> with the <u>Script editor"</u>.
- 5. Unplug jumper J9 1-2 to start the device with the mirror configuration setting.
  - a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
  - b. If the mirror registers are not filled (with a configuration using the Script editor), the currently-programmed OTP fuse configuration is used, if it exists.
  - c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned, and the device will not start up.

As long as initialization phase is not closed by a first good WD\_Answer, the WD does not start and regulators do not stay alive. Also, as long as Debug mode is not exited by writing FS\_STATES:[DBG\_EXIT] bit to 1, the FS0B pin cannot be released.

6. Use the FlexGUI software to evaluate the device configured. See <u>Section 8 "Using</u> <u>FlexGUI"</u>.

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# 7.2.1 Example script: Closing initialization phase, disabling FCCU monitoring, and releasing FS0B

The following script can be used to:

- Disable the WD.
- Disable the FCCU monitoring. On the hardware kit, the FCCU1 is pulled to GND and FCCU2 is pulled to VDDIO. Disabling the FCCU by SPI/I2C avoids safety issue at startup.
- Close the initialization phase.
- Exit the Debug mode.
- Release FS0B pin. This is valid only if WD is activated in OTP. Seven good consecutive WD answers are required to have the FLT\_ERR\_CNTR back to 0. This is one of the conditions to allow FS0B release.

Table 19. FS85 starting sequence example

Step	Register name	Value	Description
1	FS_WD_WINDOW	0x0200	WDW_WINDOWS[3:0] = 0x0 => Watchdog disabled
2	FS_NOT_WD_WINDOW	0xF50F	NOT of FS_WD_WINDOW
3	FS_I_SAFE_INPUTS	0x51C6	FCCU_CFG[1:0] = 0x0 => 0x1 => Monitoring by pair FCCU12_FLT_POL[0] = 1 => FCCU1 or 2 = 0 is a fault
4	FS_I_NOT_SAFE_INPUTS	0xAC18	NOT of FS_I_SAFE_INPUTS
5	FS_WD_ANSWER	0x5AB2	First good WD answer (for simple WD selection in OTP) Close the initialization phase
6	FS_STATES	0x4000	DBG_EXIT[0]=1 => Exit Debug mode
7	FS_WD_ANSWER	0x5AB2	Second good WD answer
8	FS_WD_ANSWER	0x5AB2	Third good WD answer
9	FS_WD_ANSWER	0x5AB2	Fourth good WD answer
10	FS_WD_ANSWER	0x5AB2	Fifth good WD answer
11	FS_WD_ANSWER	0x5AB2	Sixth good WD answer
12	FS_WD_ANSWER	0x5AB2	Seventh good WD answer
13	FS_RELEASE_FS0B	0xB2A5	FS0B pin released (pulled to high level)
14	MFLAG2	0x40F1	Clear flags VSUPUV7; VPREUVL, VSUPUVL, WAKE1FLG
15	FS_OVUVREG_STATUS	0x4550	Clear UV status flags

This sequence can be sent using a script built with FlexGUI. See <u>Section 8.3.2 "Script</u> <u>sequence files"</u>.

## 7.3 Programming the device with an OTP configuration

The device configuration can be changed three times (see <u>Section 4.2.1 "OTP and</u> <u>mirrors registers"</u>). The programming steps are the same as the OTP emulation mode up to step 6.

Then, the user has to burn the part with FlexGUI. See <u>Section 8.4.8 "OTP programming"</u>. Follow the instructions on the screen to proceed.

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## 8 Using FlexGUI

To follow the steps in this section, make sure that the board is connected using the appropriate hardware configuration (see <u>Section 7.2</u> "Working in OTP emulation mode").

Note: It is recommended to use the latest version of FlexGUI.

## 8.1 Starting the FlexGUI application

After FlexGUI is launched with the *flexgui-app.bat* file, the FlexGUI launcher displays available kits.

Communication bus, SPI, or I2C can be selected at this level. It is also possible to switch from one to the other using the communication tab from the main panel (see <u>Section 8.2</u> "Establishing the connection between FlexGUI and the hardware").

NP FlexGUI Laun		
FlexGOI Laun	cher —	
Select a kit, or	n board device(s), target MCU and USB i	nterface.
Kit and Device	(s)	
▼ FS85 KITs		
▼ FS85		
▼ ✓ F	S8530	
	BO	
$\checkmark$	C0	
A Litter FOOE	and FS84 evaluation.	
A KILIOFF585 a		
✓ Advanced S	SPI or I <sup>2</sup> C bus selection	
	SPI or I <sup>2</sup> C bus selection	tabs, etc.
✓ Advanced S	SPI or I <sup>2</sup> C bus selection	
<ul> <li>✓ Advanced S</li> <li>Feature Set</li> </ul>	SPI or I <sup>2</sup> C bus selection debug-spi	V setup.
<ul> <li>Advanced S</li> <li>Feature Set</li> <li>Target MCU</li> </ul>	SPI or I <sup>2</sup> C bus selection debug-spi  KL25Z (embedd Usb_cdc	V setup.
<ul> <li>Advanced S</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> </ul>	SPI or I <sup>2</sup> C bus selection debug-spi  KL25Z (embedd Usb_cdc Mode	V setup.
<ul> <li>Advanced S</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application</li> </ul>	SPI or I <sup>2</sup> C bus selection ettings debug-spi KL25Z (embedd usb_cdc Mode provide secret keywo Elev	V setup. mware.
<ul> <li>Advanced S</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application</li> <li>Password</li> <li>Launch Privileg</li> </ul>	SPI or I <sup>2</sup> C bus selection ettings debug-spi KL25Z (embedd usb_cdc Mode provide secret keywo Elev	V setup. mware.
<ul> <li>Advanced S</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>Application</li> <li>Password</li> <li>Launch Privileg</li> </ul>	SPI or I <sup>2</sup> C bus selection ettings debug-spi KL25Z (embedd usb_cdc Mode provide secret keywo BASIC SPI or I <sup>2</sup> C bus selection & Adjust loaded Check your HV Check used fin Elevent	V setup. mware.
<ul> <li>✓ Advanced S</li> <li>Feature Set</li> <li>Target MCU</li> <li>USB Interface</li> <li>✓ Application</li> <li>Password</li> <li>Launch Privileg</li> </ul>	SPI or I <sup>2</sup> C bus selection debug-spi	V setup. mware. vate

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When the configuration is selected, click **OK**.

## 8.2 Establishing the connection between FlexGUI and the hardware

The board must be connected to the USB before establishing a connection.

- Click **Search** to detect the COM port of the board.
- Click **Start** to enable the connection.

4FO 🔹 500 🚓 😽 🚵 💿 FS85-FS8530.CO Script edito	pr											
er messages		ents Interrupt FL	ags INIT Safe	ty Diag Safety OTP prog	TestModeSequenc	er TestMode:Mirrors	Main TestMode Mi	rrors_FailSafe				
9> FS85 [M_TM_STATUS1:0x1F] R: 0x020E						form Buttons 🗸 Show						
	new negoters per	rage o 💌	Dit DOLLORS P	er one o 💌 🖬 son	by Address [v] on	ionni sottons 🕑 snor	W BIL POSICION					
51> FS85 [M_TM_STATUS1:0x1F] R: 0x022E functional		Write Read	Copy Rese	8								
52> FS85 [FS_STATES.0x16] R: 0x4005 53> FS85 [M. TM. STATUS1.0x1F] R: 0x022E												
in a second second				W 0x0					Second Second			
SV BORS IM TH STATISTOUTE B. 0x0226		M FLAG	0x00			RESERVED	RESERVED	SPUMJCLK	SPUMUREQ	SPUMUCRC	IQC_M_CRC	QC_M_REQ
6× F585 [F5_STATES.0x16] R: 0x4006 Communication	on			R Ox0	COM,ERR	WU,6	VPRE,6	V80057,6	VBUCK1,6	V8UCK2_6	VBUCK3_6	VLD01_6
17> F585 IM TM STATUS1.0x1FI R 0x022E				K OND	VLDO2_G	RESERVED	RESERVED	SPILMLOUK	SPUMUREQ	SPUMUCRC	I2C_M_CRC	I2C_M_REQ
18> F585 [F5_STATES:0x16] R: 0x4005								RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
69> F585 [M_TM_STATUS1.0x1F] R: 0x022E Search				W 0x0								
70> FS85 [FS_STATES:0x16] R: 0x4006 COM Port		M MODE	E 0x01 (	A A	RESERVED	EXT_RIN_DIS	RESERVED	RESERVED	RESERVED	W2DIS	WIDIS	GOTOSTBY
71> F585 [M_TM_STATUS1:0x1F] R: 0x022E					RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PLLLOCK,RT
72> FS85 [FS_STATES:0x16] R: 0xA006				R Ox0	EXT_RIN_SEL_RT	RESERVED	MAIN_NORMAL	RESERVED	RESERVED	W2015	WIDIS	
73> F585 [M_TM_STATUS1:0x1F] R: 0x022E												
74> FS85 [FS_STATES:0x16] R: 0x4006				W 0x0	VPRE_PD_DIS	VPDIS	BOOSTOIS	8UCK1DIS	BUCK2DIS	BUCK3DIS	LOOIDIS	LDOSDIS
75> FS85 [M_TM_STATUS1.0x1F] R: 0x022E	Test	M REG CTRL1	CTRL1 0x02 🥑		RESERVED	VPEN	BOOSTEN	BUCKTEN	BUCKZEN	BUCKIEN	LDO1EN	LDOZEN
		M_REG_CTRE1		-	VPRE_PD_DIS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
sas Pins Mode Selection	on			R 0x0								
Mode												
Switch Mode: test-mode - Poll				W 0x0	V8STSR[1]	VBSTSR(0)	BOOSTTSDCFG	BUCK1TSDCFG	8UCK2TSDCF6	BUCK3TSDCFG	LDO1TSDCF6	LD02TS0CF6
and note					RESERVED	RESERVED	RESERVED	VPRESALS[1]	VPRESRUS[0]	RESERVED	VPRESRHS[1]	VPRESRHS[0]
outing: SPI-routing -		M_REG_CTRL2	0x03	Ø0	V8STSR(1)	VESTSRID	BOOSTTSDCFG	BUCKITSDCFG	BUCK2TSDCFG	BUCKITSDOFG	LDO1TSDCFG	LDO2TSDCFG
• SPI or I2C SV	and a large			R 0x9	RESERVED	RESERVED	RESERVED	VPRESRLSITI	VPRESRLSIOI	RESERVED	VPRESRHS[1]	VPRESRHSIOI
0110112000	witch							(manual)	(manual)		(maximup)	(Friday (1995)
				W Oxe	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Frequency (kHz): 5000				w uxe	RESERVED	RESERVED	RATIO	AMURŞAJ	AMU0(3)	AMUX(2)	AMUX[1]	AMUNIO
Main Status		M_AMUX	0x04	<b>V</b>			RESERVED	RESERVED				RESERVED
				R Ox0			RATIO	AMUXMI	AMUSER	AMUX721	ANUXTI	AMUUUT
Extended Status VLDO2_G: No event							RATIO .	warodal	AMPO(S)	ww00021	www.optil	xwo.(0)
SPI_M_CLK: No error				W 0x0	MOD_CONF	FOUT_MUX_SEL[3]	FOUT_MUX_SEL[2]	FOUT_MUX_SEL[1]	FOUT_MUX_SEL[0]	FOUT_PHASE(2)	FOUT_PHASE[1]	FOUT_PHASE[0]
				W W0	FOUT_CLK_SEL	EXT_FIN_SEL	FIN_DIV	MOD_EN	CLK_TUNE(3)	CUCTUNE(2)	CUC_TUNE[1]	CUC,TUNE(0)
SPI_M_REQ: No error		M_CLOCK	0x05	<b>V</b>	MOD_CONF	FOUT_MUX_SEL[3]	FOUT_MUX_SEU21	FOUT_MUX_SEL[1]	FOUT_MUX_SELIDI	FOUT_PHASE(2)	FOUT_PHASE[1]	FOUT_PHASEIDI
SPI_M_CRC: No error Communicat	tion			R 0x0		ALSERVED	FIN.DV	MOD EN				
2C_M_CRC: No error / Status					FOUT_CLK_SEL				CLK_TUNE[3]	CUC,TUNE[2]	CUC, TUNE[1]	CUK_TUNE[0]
2C_M_REQ: No error							< 1 2	3 🕨				
U: KL25Z (embedded State: CONNECTED Firmware: 0.13.10/02.0							1/3					ild: Thu Oct 03 16:01:2:

#### Figure 24. Main panel

<u>Figure 24</u> shows the mode selection. At first launch, the FlexGUI starts in User mode. The user can then decide to switch to Test mode using the Switch mode drop-down list followed by clicking **Apply**.

The **GUI-Device Status** field checks the connection from MCU to the device. The **ONLINE** status indicates a good connection, while **ERROR** status indicates an issue (for example,  $V_{SUP}$  is not provided to the device).

The SPI/I2C communication bus can be changed at any time using the drop-down list. This change is managed by the onboard MCU to communicate with the desired bus.

It is also possible to change the clock frequency using this panel.

Note that in the case of I2C, most of the time, the default address used by the device are 0x20 for main and 0x21 for the fail-safe.

The I2C address is managed differently in Debug and Normal mode.

- Debug mode:
  - I2C address when debug mode pin is set to 5.0 V are 0x20 for main and 0x21 for failsafe.
  - The user can change this address in the mirror register. The new address is taken into account only after debug pin is released to 0 V.
- Normal mode:
  - The address is burned in the OTP.

The user can read in which mode the device is operating. It is also possible to switch from user mode to test mode (and vice-versa).

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The current mode is refreshed only when Poll button is activated. If required, this has to be done at startup (Poll button is disabled by default). See <u>Figure 25</u>.

	Mode				
	Switch Mo	test	-	Poll	
				aaa-032771	
Figure 25. Disabling	device mode poll	ing			

To move from one mode to the other, select the mode with switch mode drop-down button. If the requested mode is not confirmed by the device (if debug pin is not set, for instance), the drop-down menu switches back to the previous mode.

### 8.3 Working with the Script editor

The register and OTP emulation can be configured with the script editor. This is particularly useful to try various OTP configurations in Emulation mode.

Filter messages	Device: FS85 +	Commands:	Results:	
42> FS85 [FS_MIRRORCMD:0x17] W: 0x0118 43> FS85 [FS_MIRRORDATA:0x18] W: 0x00	Alias: No values	//Device configuration: FS8530	//Device configuration: FS8530	
14> FS85 [FS_MIRRORCMD:0x17] W: 0x0119		//Sample marking: PC31F58530A0ES	//Sample marking: PC33FS8530A0ES	
5> FS85 [FS_0TPCMD.0x18] W: 0x0125	<ul> <li>Digital pins</li> </ul>	//Author: NXP //Cuttomer: NXP	//Author: NXP	
6> FS85 [FS_OTPCMD.0x18] W: 0x0124	<ul> <li>Analog pins</li> </ul>	//Date: 11/8/2018	//Customer: NOP	
7> FS85 IFS TM STATUS1:0v2A1R: 0xA0C0	<ul> <li>Registers</li> </ul>	//Time: 10:12:14 AM //Generated from FS85_OTP_Mapping file revision: Rev 1.4	//Date: 11/8/2018	
4> FS85 [M_TM_STATUS1:0x1F] R: 0x0022	▶ Mode	//Generated from FSE5_DTP_Mapping the revision: Key 1.4 //Emulate/Program:Emulate	//Time: 10:12:14 AM	
5> FS85 [FS_STATES:0x16] R: 0x4001	<ul> <li>Generator</li> </ul>	//GUI_rev: > 0.6	//Generated from FS85_OTP_Mapping file revision: Rev 1	4
6> FS85 [M_TM_STATUS1:0x1F] R: 0x0022		//TEST_MODE_ENTRY SET_MODE/585test-mode	//Emulate/Program: Emulate	
7> FS85 [FS_STATES:0x16] R: 0x4001		//EGIN MAIN	//GUI_rev: > 0.6	
8> FS85 [M_TM_STATUS1.0x1F] R: 0x0022	Command	//Verify Main Test Mode Entry (expect 0x0022)		
69> FS85 [FS_STATES:0x16] R: 0x4001	Script Editor	GET_REG: FS85: M_TestMode: M_TM_STATUS1 //CONFIGURE OTP MIRROR REGISTERS Script Text Editor	//TEST_MODE_ENTRY	Covint Deputte
70> FS85 [M_TM_STATUS1:0x1F] R: 0x0022		//CONFIGURE OTP MIRROR REGISTERS Script Text Editor	OK: set mode = test-mode	Script Results
11> FS85 [FS_STATES:0x16] R: 0x0001		SET_REG:FS85:M_OTP:M_MIRRORCMD:0x0114	//BEGIN MAIN	
12> FS85 [M_TM_STATUS1:0x1F] R: 0x0022	Send and Received	SET_REG/FS85-M_OTP:M_MIRRORDATA.0x0007 SET_REG/FS85-M_OTP:M_MIRRORCMD.0x0115	//Verify Main Test Mode Entry (expect 0x0022)	
12> F585 (M_1M_STATUSTUKTF) K: 0x0022 13> F585 (F5_STATES:0x16) R: 0x4001		SET_REGPS85M_OTP/M_MIRRORCMD0x0115	OK: read reg. M_TM_STATUS1 = 0x0022	
13> FS85 [M_TM_STATUS1.0x1F] R: 0x0022	Commands	SET_REG/S85:M_OTP:M_MIRRORCMD:0x0116	//CONFIGURE OTP MIRROR REGISTERS	
14> FS85 [M_1M_STATUS10X1F] R: 0x0022 15> FS85 [FS_STATES:0x16] R: 0x4001		SET_REG/FS85-M_OTP-M_MIRRORDATA:0x000D SET_REG/FS85-M_OTP-M_MIRRORCMD:0x0117	OK: write reg. M_MIRRORDATA = 0x0f	
	2	SH_RKGISSBM_CTIPM_MIRRORCMATAGOOC SFT_RKGISSBM_CTIPM_MIRRORCMATAGOOC SFT_RKGISSBM_CTIPM_MIRRORCMATAGOOC SFT_RKGISSBM_CTIPM_MIRRORCMATAGOOT SFT_RKGISSBM_CTIPM_MIRRORCMATAGOOT SFT_RKGISSBM_CTIPM_MIRRORCMATAGOOK	OK: write reg. M_MIRRORCMD = 0x0114	
S85 Pins			OK: write reg. M_MIRRORDATA = 0x07	
Mode	â		OK: write reg. M_MIRRORCMD = 0x0115	
Switch Mode: test-mode *			OK: write reg. M_MIRRORDATA = 0xef	
Current Mode: test-mode		SET_REG/S85:M_OTP.M_MIRRORCMD:0x011A	OK: write reg. M_MIRRORCMD = 0x0116	
Current Mode: test-mode		SET_REG/FS85:M_OTP:M_MIRRORDATA:0x0006 SET_REG/FS85:M_OTP:M_MIRRORCMD:0x0118	OK: write reg. M_MIRRORDATA = 0x0d	
Routing: SPI-routing +		SET_REG/S85/M_OTP:M_MIRRORCMU000116 SET_REG/S85/M_OTP:M_MIRRORDATA/0x0088	OK: write reg. M. MIRRORCMD = 0x0117	
		SET_REG/FS85:M_OTP:M_MIRRORCMD:0x011C	OK: write reg. M. MIRRORDATA = 0x8c	
▼ SPI1 Rus: SPI		SET_REG/FS85/M_OTP/M_MIRRORDATA.0x001C SET_REG/FS85/M_OTP/M_MIRRORCMD:0x011D	OK: write reg. M.MIRRORCMD = 0x0118	
		SET_REG/S85:M_OTP:M_MIRRORDATA.0x008E	OK: write reg. M. MIRRORDATA = 0x07	
Frequency (kHz): 5000		SET_REG/FS85:M_OTPIM_MIRRORCMD:0x011E	OK write reg. M_MIRRORCMD = 0x0119	
		SET_REG:FS85.M_OTP.M_MIRRORDATA.0x0093 SET_REG:FS85.M_OTP.M_MIRRORCMD:0x011F	OK: write reg. M_MIRRORDATA = 0x0119 OK: write reg. M_MIRRORDATA = 0x64	
COM_ERR: No failure		SET_REG/S85:M_OTP:M_MIRRORDATA.0x0076		
WU_G: Event occurred		SET_REG/FS85:M_OTP.M_MIRRORCMD:0x0120	OK: write reg. M_MIRRORCMD = 0x011a	
VPRE.G: Event occurred		SET_REG/FS85/M_OTP/M_MIRRORDATA/0x0030 SET_REG/FS85/M_OTP/M_MIRRORCMD/0x0121	OK: write reg. M_MIRRORDATA = 0x05	
VBOOST_G: Event occurred		SET_REGFS85M_OTP:M_MIRRORDATA@x0023	OK: write reg. M_MIRRORCMD = 0x011b	
		SET_REGIFS85:M_OTPIM_MIRRORCMD/0x0122	OK: write reg. M_MIRRORDATA = 0x88	
VBUCK1_G: No event		SET_REG:FS85:M_OTP:M_MIRRORDATA:0x0002 SET_REG:FS85:M_OTP:M_MIRRORCMD:0x0123	OK: write reg. M_MIRRORCMD = 0x011c	
VBUCK2_G: No event		SET. REG/F885M OTP/M MIRRORDATA.0x0004	OK: write reg. M_MIRRORDATA = 0x1c	
VBUCK3_G: No event		💽 ∞ 💾 🖿 🚽 🕘 Script Execution and Management	💾 🛅 🥑 Results manager	nent
VLDO1 G: No event	~			
	ware: 0.13.10/0.2.0			0.9.0 FlexGUI: 1.0.2-RFP Build: Thu Jul 04 18:47:52 CE

The main subareas of this panel are:

- Send and receive command: displays a summary of commands sent and received from the device
- Command script editor: builds commands to be sent to the device
- Script text editor: sends a sequence of register configurations from a text file or from command edited directly in this area
- Script results: displays result status of each command sent to the device

#### 8.3.1 Script text editor

Using Script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if needed.

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All commands have to follow a specific syntax. The Help menu describes commands available in the script editor and their syntax.

This help page describes commands available in the script editor and their format.

#### List of commands

- SET\_REG: sets value of a selected register.
- READ\_REG: reads value of a selected register.
- SET\_DPIN: sets value of a selected digital pin.
- GET\_DPIN: gets value of a selected digital pin.
- GET\_APIN: gets value of a selected analog pin. Returned value is in mV.
- PAUSE: shows a dialog with user defined message. The script is paused until the user cofirms the dialog.
- EXIT: stops execution of the script.
- SET\_MODE: sets device mode. List of modes depends on a device.

#### **Command format**

The following table describes command parameters. All paramaters are mandatory.

	lst parameter	2nd parameter	3rd parameter	4th parameter	5th parameter
SET_REG	Device	Reg. set	Reg. name / Reg. address	Reg. value	-
GET_REG	Device	Reg. set	Reg. name / Reg. address	-	-
SET_DPIN	Device	Pin name	Dig. pin value	-	-
GET_DPIN	Device	Pin name	-	-	-
GET_APIN	Device	Pin name	-	-	-
PAUSE	Message	-	-	-	-
EXIT	-	-	-	-	-

Description of command parameters mentioned in the table above:

- Device: device name (alias used in application).
- Reg. set: register set name. Register sets allows to associate registers which have similar function.
- · Reg. name: register name as defined in datasheet.
- Reg. address: register address in decimal or hexadecimal (with 0x prefix) format.
- Reg. value: register value in decimal or hexadecimal (with 0x prefix) format.
- · Pin name: name of digital or analog pin as defined in device datasheet.
- · Dig. pin value: value of digital pin. Allowed strings are 'low' and 'high'.
- Message: a message to be displayed in a dialog. It cannot contain ':' character, which is used as delimiter of parameters.
- · Mode: name of a device mode.

Figure 27 shows an example to build a command from the panel.

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	FS85 Script editor	•		-
	Device:	FS85	•	Commands:
	<ul> <li>Digital pins</li> </ul>			SET_REG:FS85:functional:M_REG_CTRL1:0x0800
	Analog pins			Command Built
	<ul> <li>Registers</li> </ul>			
	Operation:	Write reg.	•	
	Reg. set:	functional	•	
	Reg. name/address	: M_REG_CTRL1	-	
	Reg. value:	0x0800		
	Bu	 ild Command		aaa-032336
Figure 27. B	uild a comma	nd		

The value 0x0800 is sent to the register M\_REG\_CTRL1 (BUCK2DIS). The user can then send it to the device by clicking the arrow (see <u>Figure 28</u>).

	Send Script	
	aaa-032337	
Figure 28. Send scrip	t	
	Commands:	
	// This command will disable // Regulator BUCK2 SET_REG:FS85:functional:M_REG_CTRL1:0x0800	
Figure 29. Correct for	mat	
	Commands:	
	// This command will disable Regulator BUCK2 SET_REG:FS85:functional:M_REG_CTRL1:0x0800	
Figure 30. Wrong form	nat ("//" missing in second line)	

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#### 8.3.2 Script sequence files

The Script editor allows the user to save script sequence files. A script sequence file is text file that contains a set of commands sent to the device in the order they are written, as shown in the following example.

```
// FS85_Release_FS0b
SET_REG:FS85:safety:FS_WD_WINDOW:0x0200
SET_REG:FS85:safety:FS_NOT_WD_WINDOW:0xF50F
SET_REG:FS85:Write_INIT_Safety:FS_I_SAFE_INPUTS:0x51C6
SET_REG:FS85:Write_INIT_Safety:FS_I_NOT_SAFE_INPUTS:AC18
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
```

Note: Comments can be added with a // prefix.

### 8.4 Understanding the FS85 workspace

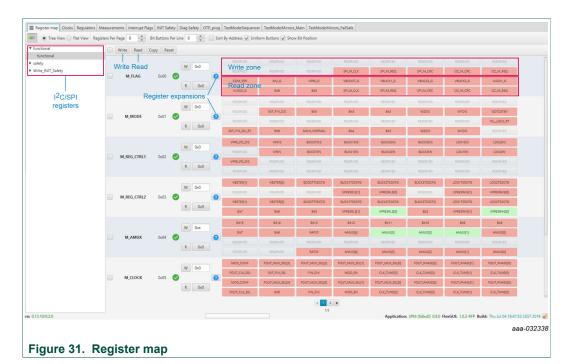
The FS85 workspace consists of several tabs, each dedicated to a specific aspect of device functionality or configuration.

- · Register map
- Clocks
- · Regulators
- Measurements
- Interrupt flags
- · INIT safety
- · Diag safety
- OTP programming
- TestMode:Sequencer
- TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe

#### 8.4.1 Register map

All SPI/I2C registers can be accessed in write and read mode using this tab.

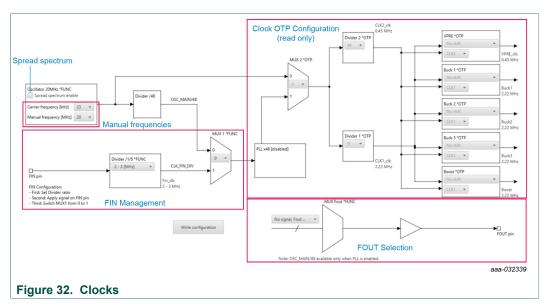
#### KITFS85FRDMEVM evaluation board



# • **Register map**: allows access to functional register, safety register and write init register which is accessible only during initialization phase

- Read: allows you to read any register either individually or by bank
- Write: allows you to write any register either individually or by bank
- Register expansion: displays the value of each device parameter

#### 8.4.2 Clocks



This tab allows:

OTP:

• Read current OTP configuration (write operation is not possible). To display the accurate data, the device must operate in Test mode.

SPI/I2C:

- · Configure the device to work with FIN input
- Select the signal to apply on FOUT pin
- Play with manual frequencies and spread spectrum

#### 8.4.3 Regulators

The regulator has two main areas:

- · Low voltage (LV) regulators configuration
- VPRE compensation network calculation

Each regulator can either be enabled or disabled by SPI/I2C. The thermal shutdown behavior can be configured to either shutdown the regulator, or shutdown the regulator and transition to deep fail-safe. The write button applies to the entire table. The VPRE compensation network calculator helps to define the value for VPRE external compensation network.

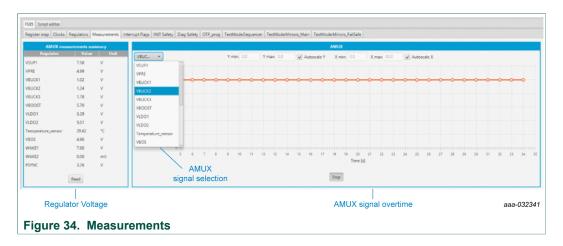
	Low Vo	ltage	Regulators			VPRE compensation network calculation		
LV	Buck1		LV Buck2			VPRE [V]		
	Disable	-	State in normal mode	Disable	-	VPRE ILIM [mV]		
Behavior in case of TSD	Regulator_Shutdown	•	Behavior in case of TSD	Regulator_Shutdown	•	Switching Frequency [KHz]		
						Rshunt [mOhm]		
LV	Buck3			LDO1		Cout [uF]		
itate in normal mode	Disable	-	State in normal mode	Disable	-	Lvpre [uH]		
Sehavior in case of TSD	Regulator_Shutdown	•	Behavior in case of TSD	Regulator_Shutdown	•	Rcomp [KOhm] N/A Ccomp [nF] N/A		
						Chf [pF] N/A		
1	LDO2			VBOOST		Current limit [A] N/A Slope compensation [mV/us] N/A		
itate in normal mode	Disable 🔹	-	State in normal mode	Disable	-	Stope compensation (invos) 10 A		
Behavior in case of TSD	Regulator_Shutdown	•	Behavior in case of TSD	Regulator_Shutdown	-			
		Wri	te			Calculate		

#### 8.4.4 Measurements

This tab enables two features:

- Read any of the AMUX signals over time
- Display regulator voltage summary

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### 8.4.5 Interrupt flags

This tab allows you to set or clear flags. It is also possible to mask the interruption.

	Over/under-v					temperatu		
	Status C	lear	Mask		Stat	us Clear		Mask
VSUP UVH		$\checkmark$	INT_not_mas	ked LDO1 shutdown				INT_not_maske
VSUP UVL	6	$\checkmark$	INT_not_mas	ked LDO2 shutdown				INT_not_maske
VSUP UV7		$\checkmark$	INT_not_mas	ked BUCK1 shutdown				INT_not_maske
VPRE UVH		$\checkmark$	INT_not_mas	ked BUCK2 shutdown				INT_not_maske
VPRE UVL		$\checkmark$	INT_not_mas	ked BUCK3 shutdown				INT_not_maske
VPRE FB_OV			INT_not_masl	ked VBOOST shutdow	n			INT_not_maske
VBOS UVH		$\checkmark$	INT_not_mas	ked BOS				INT_not_maske
VBOOST UVH		V	INT_not_mas	ked	Write	Read	Poll	
VBOOST OV			INT_not_mas	ked	·····	nead		
	Write Read	Poll						
	Over-curr   Status   C	rent lear	Mask			c <mark>ellaneous</mark> 15 Clear		Mask
LDO1		lear	Mask INT_not_masl	ked LDO1 ST				Mask
LDO1 LDO2	Status C	lear	INT_not_masl					Mask
	Status C	lear	INT_not_mas	ked LDO2 ST				Mask
LDO2	Status C	ilear	INT_not_masl INT_not_masl INT_not_masl	ked LDO2 ST ked BUCK1 ST				Mask
LDO2 BUCK1	Status C	ilear	INT_not_masl INT_not_masl INT_not_masl INT_not_masl	ked LDO2 ST ked BUCK1 ST ked BUCK2 ST				Mask
LDO2 BUCK1 BUCK2	Status C		INT_not_mask INT_not_mask INT_not_mask INT_not_mask INT_not_mask	ked LDO2 ST ked BUCK1 ST ked BUCK2 ST ked BUCK3 ST				Mask
LDO2 BUCK1 BUCK2 BUCK3	Status C		INT_not_masl INT_not_masl INT_not_masl INT_not_masl INT_not_masl INT_not_masl	ked LDO2 ST BUCK1 ST ked BUCK2 ST ked BUCK3 ST VBOOST ST				
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status C		INT_not_masi INT_not_masi INT_not_masi INT_not_masi INT_not_masi	ked LDO2 ST BUCK1 ST ked BUCK2 ST ked BUCK3 ST VBOOST ST		us Clear		Mask INT_not_maske INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status C		INT_not_masi INT_not_masi INT_not_masi INT_not_masi INT_not_masi	ked LDO2 ST BUCK1 ST ked BUCK2 ST ked BUCK3 ST VBOOST ST ked WK1 FLG		us Clear		INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status C		INT_not_masi INT_not_masi INT_not_masi INT_not_masi INT_not_masi	ked LDO2 ST BUCK1 ST ked BUCK2 ST ked BUCK3 ST VBOOST ST WK1 FLG WK2 FLG		us Clear		INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status C		INT_not_masi INT_not_masi INT_not_masi INT_not_masi INT_not_masi	ked LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG WK1 RT		us Clear		INT_not_maske

#### 8.4.6 INIT safety

This tab allows you to manage all registers that can be configured to close the initialization phase. The initialization phase is closed by the first good watchdog refresh before 256 ms timeout.

	Fault impact						
Fault source	Settings	FSOB RSTB		Error counters limit		OV/UV Safe Rea	ction 1
COREMON_OV	No_effect 👻		WD_ERR_LIMIT	6 👻	6	VCore ABIST2	No_ABIST
/DDIO_OV	No_effect 👻		WD_RFR_LIMIT	6 -	6	VDDIO ABIST2 VMon1 ABIST2	No_ABIST No_ABIST
MON1_OV	No_effect 👻		FLT_ERR_CNT_LIMIT	6 -	6	VMon1 ABIST2 VMon2 ABIST2	No_ABIST
MON2_OV	No_effect 🔹					VMon3 ABIST2	No_ABIST
MON3_OV	No_effect -					VMon4 ABIST2	No_ABIST
/MON4_OV	No_effect -						
COREMON_UV	FSOB 👻			Safe Inputs		Miscellaneo	us
/DDIO_UV	FSOB 👻		FCCU pin config	FCCU1_FCCU2_pair •	FCCU1_FCCU2_pair	RSTB pulse duration 10ms	▼ 10ms
MON1_UV	FSOB 👻		FCCU12 polarity		FCCU1_L_FCCU2_H	Assert RSTB on FS0B short	RESET_asserted
MON2_UV	FSOB 👻		FCCU1 polarity FCCU2 polarity		FCCU1_L FCCU2_L	Disable clock monitoring Disable 8S timer	Monitoring_activ Counter_enabled
MON3_UV	FSOB -		FCCU1 polarity impact	$\checkmark$	FSOB_RSTB		
/MON4_UV	FSOB -		ERRMON polarity		Negative_edge		
CCU12	FSOB_RSTB -		ERRMON timing config	8ms 👻	8ms		
CCU1	FSOB_RSTB -						
CCU2	FSOB_RSTB -			Static Voltage Scaling			
RRMON	FSOB_RSTB -		Static voltage scaling	0mV 👻	0mV		
VD_FS_IMPACT	FSOB_RSTB -						
LT ERR IMPACT	FSOB_RSTB -						
mpact		_					
lo impact							
	Write Read				Write Rea	d	
							aaa-032

#### 8.4.7 Diag safety

The watchdog type configured in the OTP has to be manually selected in the dropdown list to play with the watchdog features. If the user is not aware about the type of watchdog configured in the OTP, it can be found in TestMode:Mirrors\_Failsafe and Miscellaneous tabs.

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Register map Clocks Regulators Measurements Interr	upt Flags INIT Safety Diag Safety OTP_prog TestMode:Sequence	r TestMode:Mirrors_Main TestMode:Mirrors_FailSafe
Safe IO	Diag. Safety	INTB Mask
Report PGOOD change     N/V       Report PGOOD event     N/V       Report PGOOD sense     N/V       Statemal reset     N/V       RSTB driver     N/V       RSTB diag     N/V       FS08 driver     N/V       FS08 driver     N/V       FS08 dring     N/V       FS08 request     Goto INIT fail-safe	FCCU12 error         N/Y           FCCU1 error         N/Y           FCCU2 error         N/Y           ERRMON acknowledge         ERRMON input status           ERRMON input status         N/Y           ERRMON input status         N/Y           WD refresh status         N/Y           SPI CRC status         N/Y           SPI CRC status         N/Y           I2C CRC status         N/Y           I2C access status         N/Y	VMON4 OV/UV int. enable N/V VMON3 OV/UV int. enable N/V VMON2 OV/UV int. enable N/V VDDIO OV/UV int. enable N/V VDDIO OV/UV int. enable N/V VCOREMON OV/UV int. enable N/V WD refresh int. enable N/V ERRMON int. enable N/V FCCU2 int. enable N/V FCCU2 int. enable N/V
Write Read	Write Read	Write Read
Watchdog management	OV/UV status	Flags and Status
	VCOREMON OV         N/V           VCOREMON UV         N/V           VDIO OV         N/V           VDDIO UV         N/V           VDDIO UV         N/V           VMON4 OV         N/V           VMON4 OV         N/V           VMON4 UV         N/V           VMON3 UV         N/V           VMON3 UV         N/V           VMON2 OV         N/V           VMON1 UV         N/V           Script to release FS0b pin when           from power-up         Nover-up	Communication error N/V WD refresh error N/V IO error N/V Voltage monitoring error N/V ABIST1 status N/V ABIST2 status N/V Est Mode Activation Status N/V Test Mode Activation Status N/V CoTP bit corruption N/V OTP bit corruption N/V Fail-safe machine state N/V Write Read
Select the current watchdog OTP conf before to use the watchdog managem	iguration	aaa-0323

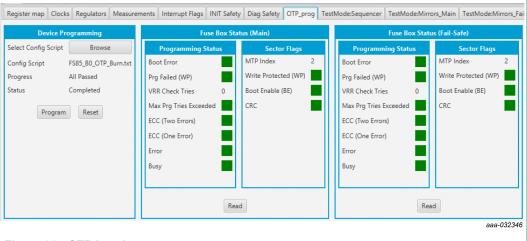
The FS\_Release\_FS0B command calculates and sends the right secure16-bit word to release FS0B.

A simplified way to release FS0B after power up is to, first, select the right type of watchdog configured in the OTP, then, hit FS0B Release script button. This sends the right sequence to close the initialization sequence, sets the error counter back to 0, then releases FS0B.

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### 8.4.8 **OTP** programming

This tab allows you to burn the OTP using a script generated by the excel file OTP configuration (see <u>Section 7.1 "Generating the OTP configuration file "</u>).



#### Figure 38. OTP burning

To set up the hardware before OTP burning, see <u>Section 7.3 "Programming the device</u> with an OTP configuration".

See Figure 38 and follow the steps:

- Browse and load the script file you want to burn. The program button is then available.
- Click Program.

FlexGUI pops up to turn the 8.0 V On, and then turns Off. Note that the blue LED on the board indicates that an 8.0 V voltage is available on the Debug pin. This voltage is used only during the burning process, and should not be applied in any other configuration. At the end of the first OTP programming, the MTP index = 1, WP, BE, and CRC flags are green.

The Sector Flags area provides status <u>Table 20</u> provides the state of main flags after a read. This helps to determine how many times the part was burned.

OTP burning step	BE	WP	CRC	MTP Index
OTP not burn Mirrors Empty	Red	Red	Red	1
OTP not Burn Mirrors Filled	Red	Red	Green	1
1	Green	Green	Green	1
2	Green	Green	Green	2
3	Green	Green	Green	3

#### Table 20. OTP burning flag status

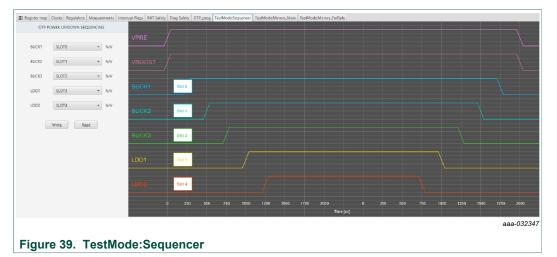
Example shown in Figure 38 corresponds to the OTP burning step 2 from Table 20.

To check if a valid OTP configuration is already burned, switch  $V_{BAT}$  Off, then On, and start the device. The device starts with the OTP configuration.

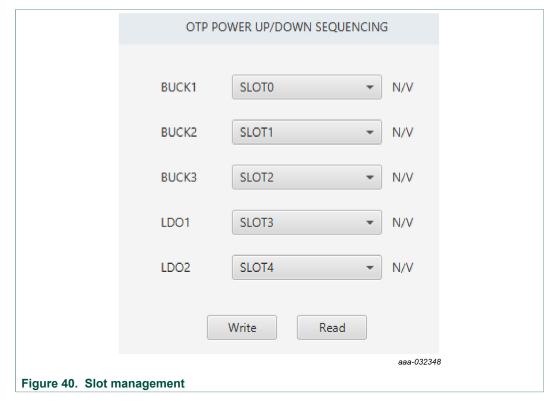
#### 8.4.9 TestMode:Sequencer

The sequencer allows you to display the slot configuration for the device. To be able to access this tab, the device has to be in Test mode. The configuration is read from mirror register. It is possible to modify it and update the mirror register.

As an example, the slot sequence is filled at startup with the content of OTP fuses. Then the user can decide to modify any of the configurations coming from the OTP fuse. Note that all these actions are done with Debug pin at 5.0 V and in test mode.



Use the drop-down button (see <u>Figure 40</u>) to select the appropriate slot. The selection configuration can be sent to the device by clicking Write button. The current status can be read by using Read button.



#### 8.4.10 TestMode:Mirrors\_Main and TestMode:Mirrors\_Failsafe

The TestModeMirrors\_Main and TestModeMirrors\_FailSafe tabs allow access to the OTP main mirrors and fail-safe registers. These tabs are available in Test mode.

In this panel, some parameters are highlighted in red. The red indicates that these parameters are not considered in case of emulation mode (accessible only in debug mode). The user must rewrite by SPI or I2C after startup.

This concerns only:

- VPRE and VBOOST slew rate
- · All regulator behavior in case of TSD

	VPRE			BOOST			LDOs	
VPRE mode	Force PWM 👻	Force PWM	Output voltage	1 *	1	VLDO2 current limitation	400mA 👻	400mA
Dutput voltage	17 ~	17	BOOST enable	Disabled +	Disabled	VLDO2 output voltage	1.2V ×	1.2V
Slope compensation	170mV/us -	170mV/us	BOOST minimum ON time	60ns -	60ns	LDO2 sequencing slot	Slot2 -	Slot2
urrent limitation threshold	50mV ~	50mV	VBOOST slope compensation	17 👻	17	Regulator behavior in case o	LDO2 shutdown + •	LDO2 shutdown
ow Side slew rate control	130mA -	130mA	Compensation Network Resistor Rco	750Kohms 👻	750Kohms	VLDO1 current limitation	400mA ~	400mA
ligh Side slew rate control	260mA -	260mA	Compensation Network Capacitor C	1 *	1	VLDO1 output voltage	1.2V -	1.2V
/PRE phase (delay) selection	Delay2 -	Delay2	VBOOST current limitation	0 ~	0	LDO1 sequencing slot	Slot1 +	Slot1
Delay to turn OFF VPRE at device power down	32ms -	32ms	VBOOST Low Side slew rate control	1 *	1	Regulator behavior in case o	LDO1 shutdown 👻	LDO1 shutdown
/PRE clock selection	CLK_DIV1 -	CLK_DIV1	BOOST phase (delay) selection	Delay1 ~	Delay1			
			BOOST clock selection	CLK_DIV2 -	CLK_DIV2			
			Regulator behavior in case of TSD	BOOST shutdown 👻	BOOST shut			
Writ	e Read		Wr	ite Read			Write Read	
	8UCK1			BUCK2			BUCK3	
BUCK1 output voltage		17	VBUCK2 output voltage 1		17	VBUCK3 output voltage	2.8V	▼ 2.8V
UCK1 inductor selection		1.5uH			1uH	BUCK3 enable	Disabled	<ul> <li>Disabled</li> </ul>
/BUCK1 current limitation	0 -	0	BUCK2 enable En	nabled 👻	Enabled	BUCK3 inductor selection	1uH	▼ 1uH
/BUCK1 & VBUCK2 multiphase operation	Enabled +	Enabled	VBUCK2 current limitation 0	-	0	VBUCK3 current limitation	2.6A	▼ 2.6A
BUCK1 Compensation Network	65GM ~	65GM	BUCK2 compensation network 0	•	0	BUCK3 compensation resistor	Default	▼ Default
BUCK1 sequencing slot	Slot1 -	Slot1	BUCK2 sequencing slot SI	lot2 •	Slot2	BUCK3 gain control	1	* 1
BUCK1 phase (delay) selection	Delay2 -	Delay2	BUCK2 phase (delay) selection D	elay1 -	Delay1	BUCK3 sequencing slot	Slot1	- Slot1
BUCK1 clock selection	CLK_DIV1 -	CLK_DIV1	BUCK2 clock selection C	LK_DIV1 -	CLK_DIV1	BUCK3 phase (delay) selection	Delay2	▼ Delay2
Regulator behavior in case of TSD	BUCK1 shutdown + •	BUCK1 shutdown +	Regulator behavior in case of TSD B	UCK2 shutdown 👻	BUCK2 shutdown	BUCK3 clock selection	CLK_DIV1	· CLK_DIV1
BUCK1 and BUCK2 Soft start/stop configura	7.81mV/us -	7.81mV/us				Regulator behavior in case of	BUCK3 shutdown	· BUCK3 shutd
						Soft start/stop configurability	3.47mV/us	▼ 3.47mV/us
Writ	e Read		Wr	ite Read			Write Read	
	стоск			SM			VSUP UV/OV	
	Disabled • Disabled		Deep Fail-safe infinite autoretry enable		Disabled	VSUP Under Voltage Threshold		
	Divide8 • Divide8		Deep Fail-safe autoretry enable	Disabled -		Regulator assigned to VDDIO (0	-	<ul> <li>VPRI</li> </ul>
-	Divide10 - Divide10		Synchronization with 1x FS85 or 1x PF8					
			Synchronization with 2 devices	Enabled -				
			Device I2C address	D1 -	D1			

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	MON1		VI	MON2		VI	MON3	
Overvoltage threshold [%]	112 -	112	Overvoltage threshold [%]	112 -	112	Overvoltage threshold [%]	112 •	112
Overvoltage Filtering Timing [us]	45 👻	45	Overvoltage Filtering Timing [us]	45 👻	45	Overvoltage Filtering Timing [us]	45 👻	45
Undervoltage threshold [%]	88 👻	88	Undervoltage threshold [%]	88 💌	88	Undervoltage threshold [%]	88 👻	88
Undervoltage Filtering Timing [us]	25 -	25	Undervoltage Filtering Timing [us]	25 💌	25	Undervoltage Filtering Timing [us]	25 👻	25
Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigne
Assignment to ABIST1		Not_Assigned	Assignment to ABIST1		Not_Assigned	Assignment to ABIST1		Not_Assigned
Monitoring		Disabled	Monitoring		Disabled	Monitoring		Disabled
write	Read		write	Read		write	Read	
V	MON4		v	DDIO		V	CORE	
Overvoltage threshold [%]	112 -	112	Overvoltage threshold [%]	112 -	112	Overvoltage threshold (BUCK1) [%]	112 •	112
Overvoltage Filtering Timing [us]	45 💌	45	Overvoltage Filtering Timing [us]	45 -	45	Overvoltage Filtering Timing [us]	45 💌	45
Undervoltage threshold [%]	88 -	88	Undervoltage threshold [%]	88 💌	88	Undervoltage threshold [%]	88 -	88
Undervoltage Filtering Timing [us]	25 👻	25	Undervoltage Filtering Timing [us]	25 👻	25	Undervoltage Filtering Timing [us]	25 💌	25
Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigne
Assignment to ABIST1		Not_Assigned	Assignment to ABIST1		Not_Assigned	Assignment to ABIST1		Not_Assigne
Monitoring		Disabled	Voltage selection	3.3V -	3.3V	Monitoring voltage (VBUCK1)	1.25V -	1.25V
write	Read		write	Read		write	Read	
		Miscel	aneous					
SVS max value allowed NoSVS	✓ NoSVS	RSTB assign	ment to PGOOD	Not_Assigned				
Watchdog monitoring	✓ Enabled	Watchdog n	Simple_WD	<ul> <li>Simple_WD</li> </ul>				
ERRMON monitoring	Disabled	FCCU monit	oring	Disabled				
Fault recovery strategy	Disabled	Device I2C a	ddress D0	• D0				
		write	Read					

#### Figure 42. TestMode: Mirrors\_FailSafe

The Read button provides the status. The Write button changes the configuration in mirror register. This can be useful, for example, to modify few parameters from OTP fuse to start up the board.

## 9 References

[1] **KITFS85FRDMEVM** — detailed information on this board, including documentation, downloads, and software and tools

http://www.nxp.com/KITFS85FRDMEVM

- [2] FS8500 product information on FS8500, Safety system basis chip for S32 microcontrollers, fit for ASIL D http://www.nxp.com/FS8500
- [3] **FS8400** product information on FS8400, Safety system basis chip for S32 microcontroller, fit for ASIL B <u>http://www.nxp.com/FS8400</u>
- [4] **FS85\_FS84\_OTP\_Config.xlsm** OTP configuration file

# 10 Revision history

Revision history		
Rev	Date	Description
v.3	20191206	<ul> <li>Section 8.1: updated Figure 23</li> <li>Section 8.2: updated description and Figure 24, Figure 25</li> <li>Section 8.3: updated Figure 26</li> <li>Section 8.3.1: updated Figure 28</li> <li>Section 8.4.1: updated Figure 31</li> <li>Section 8.4.2: updated Figure 32</li> <li>Section 8.4.6: updated Figure 36</li> <li>Section 7.1: updated OTP_conf_main_reg spreadsheet example</li> <li>Section 8.4.10: updated Figure 41</li> </ul>
v.2	20190220	<ul> <li>Global: reorganized content to match latest template</li> <li><u>Section 7.1</u>: replaced FS85_OTP_Configuration.xls by FS85_FS84_OTP_Config.xlsm</li> <li><u>Section 4.3.5</u>: updated <u>Table 13</u></li> <li><u>Section 6</u>: updated the configuration procedure</li> <li><u>Section 8.4.7</u>: updated <u>Figure 37</u></li> <li><u>Section 8.4.9</u>: updated <u>Figure 39</u> and <u>Figure 40</u></li> <li><u>Section 8.4.10</u>: updated <u>Figure 41</u></li> </ul>
v.1	20181204	Initial version

#### KITFS85FRDMEVM evaluation board

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