KMA310

Programmable angle sensor IC

Rev. 3 — 27 February 2019

Product data sheet

1 General description

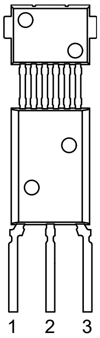
The KMA310 is a single channel magnetic angle sensor. Magnetoresistive (MR) sensor bridges and mixed signal IC are integrated into a single package. The module has integrated filters and is optimized for PCB-less designs. The IC allows user-specific adjustments of angular range, zero angle, and clamping voltages. The settings are stored permanently in a non-volatile memory (NVM). The programmable angle sensor is pre-programmed, pre-calibrated and therefore, ready to use.

2 Features and benefits

- High precision sensor for magnetic angular measurement
- Single package sensor module with integrated filters for improved electromagnetic compatibility (EMC)
- Automotive qualified in accordance with AEC-Q100 Rev-H
- Programmable user adjustments, e.g. zero angle and angular range
- Fail-safe non-volatile memory with write protection using lock bit
- Independent from magnetic field strength above 25 kA/m
- Module ready to use without external components
- Factory calibrated
- Separate temperature sensor and auxiliary analog-to-digital converter (ADC) for input stage supervision
- High temperature range up to 180 °C
- Ratiometric analog output voltage or push pull output stage compliant with SAE J2716 SENT using pulse shaping
- Overvoltage protection up to 18 V
- Power-loss detection
- Programming via one-wire interface (OWI)
- 8 × 12-bit original equipment manufacturer (OEM) code registers for identification (ID)
- ISO 26262 ASIL-C capable, safety element out of context (SEooC)
- Multipoint calibration (MPC) with 17 equidistant or seven free selectable calibration points
- Low latency

3 Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline
1	V_{DD}	supply voltage	
2	GND	ground	
3	OUT/DATA	analog/single edge nibble transmission (SENT) output or data interface	

4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
KMA310	SIL3	plastic single-ended multi-chip package; 6 interconnections; 3 in-line leads	SOT1288-3

5 Functional diagram

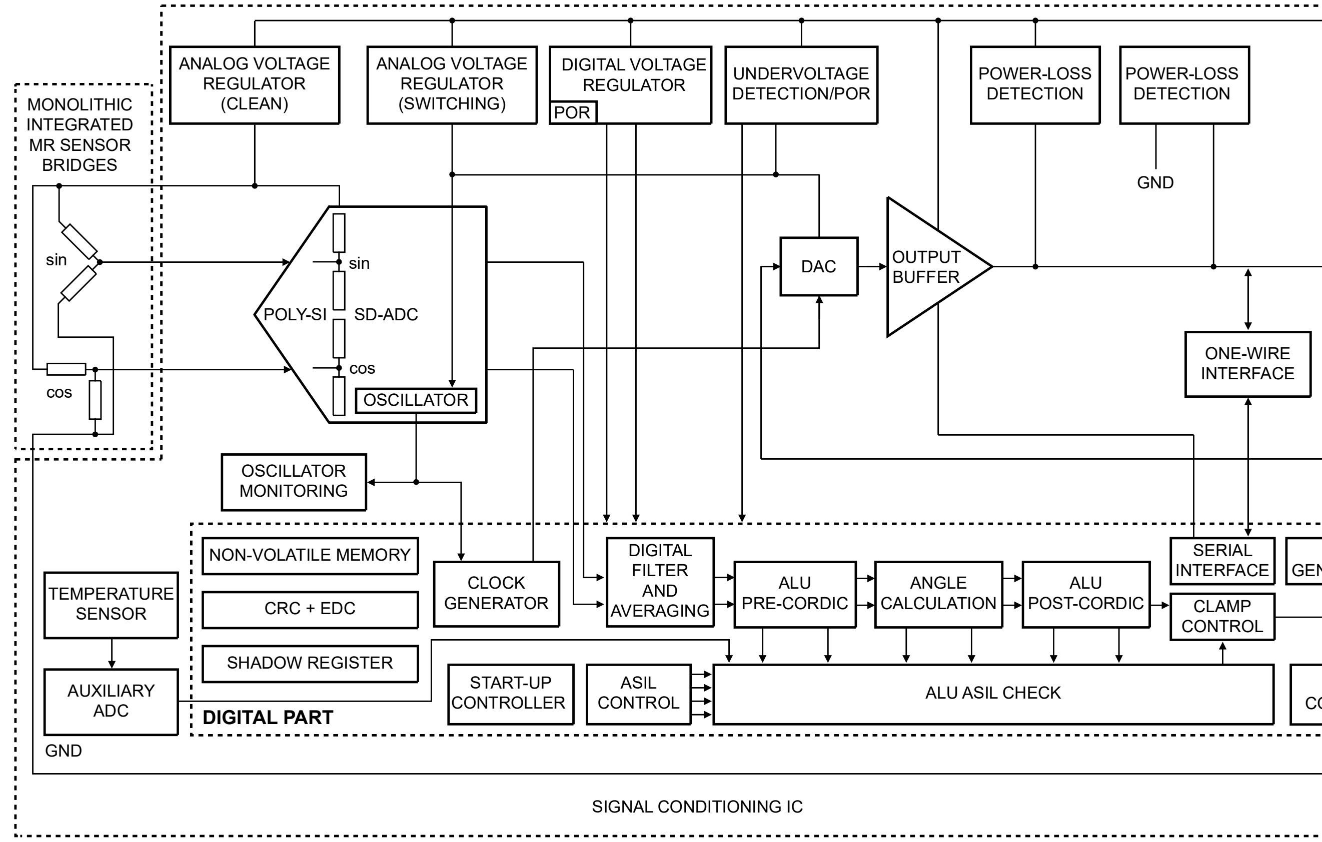


Figure 1. Functional diagram

6 Functional description

The KMA310 converts two orthogonal signals from MR sensor bridges into the digital domain. The angle is calculated using the coordinate rotation digital computer (CORDIC) algorithm. After a digital-to-analog conversion, the analog signal is provided to the output as a linear representation of the angular value or transmitted in a SENT frame compliant to SAE J2716. Zero angle, clamping voltages and angular range are programmable. In addition, eight 12-bit registers are available for customer purposes, such as sample ID.

KMA310 comprises a cyclic redundancy check (CRC) and an error detection and correction (EDC) to ensure a fail-safe operation. If either the supply voltage or the ground line of the mixed signal IC is interrupted, a power-loss detection circuit pulls the output to the remaining connection.

After conversion into the digital domain by an ADC, further processing is done within an on-chip state machine. This state machine controls offset cancelation, calculation of the mechanical angle using the CORDIC algorithm, as well as zero angle and angular range adjustment. The internal digital-to-analog converter (DAC) and the analog output stage are used for conversion of the angle information into an analog output voltage, which is ratiometric to the supply voltage. Alternatively, the output signal can be transmitted digitally in a SENT frame compliant to SAE J2716.

The configuration parameters are stored in a user-programmable non-volatile memory. The OWI (accessible using pin OUT/DATA) is used for accessing the memory. In order to protect the memory content a lock bit can be set. After locking the non-volatile memory, its content cannot be changed anymore.

6.1 Angular measurement directions

The signals of the MR sensor bridges depend only on the direction of the external magnetic field vector H_{ext}, which is applied parallel to the plane of the sensor. In order to obtain a correct output signal, exceed the minimum saturation field strength.

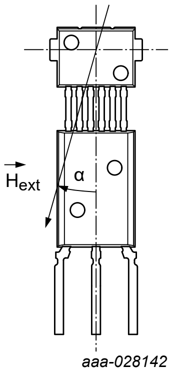


Figure 2. Angular measurement directions

Since the anisotropic MR (AMR) effect is periodic over 180°, the sensor output is also 180°-periodic. The angle is calculated relative to a freely programmable zero angle. The dashed line indicates the mechanical zero degree position.

7 Analog output

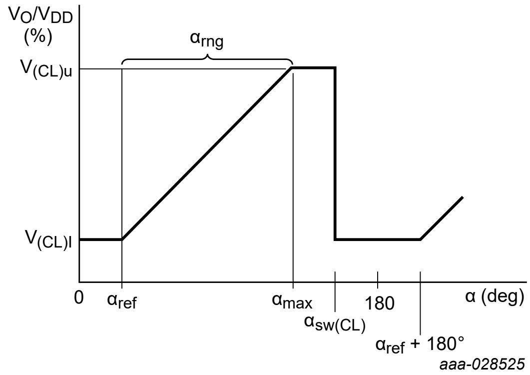
KMA310 provides an analog output signal on pin OUT/DATA (if bit 12 in register SYS_SETTING is set to logic 0; see Table 51). The measured angle α is converted linearly into a value, which is ratiometric to the supply voltage V_{DD}. Either a positive or a negative slope is provided for this purpose.

Table 3 describes the analog output behavior for a positive slope. A magnetic field angle, above the programmed maximum angle α_{max}, but below the clamp switch angle $\alpha_{sw(CL)}$ sets the analog output to the upper clamping voltage. If the magnetic field angle is larger than the clamp switch angle, the analog output switches from upper to lower clamping voltage. If there is a negative slope, the clamping voltages are changed.

Table 3. Analog output behavior for a positive slope

Magnetic field angle	Analog output
$\alpha_{max} < \alpha < \alpha_{sw(CL)}$	$V_{(CL)u}$
$\alpha_{sw(CL)} < \alpha < \alpha_{ref} + 180°$	$V_{(CL)l}$

The analog output voltage range encodes both angular and diagnostic information. A valid angle value is between the upper and lower clamping voltage. If the analog output is in the diagnostic range that is below 4 %V_{DD} or above 96 %V_{DD}, an error condition has been detected. The analog output repeats every 180°.



$\alpha_{max} = \alpha_{ref} + \alpha_{rng}$

Figure 3. Characteristic of the analog output

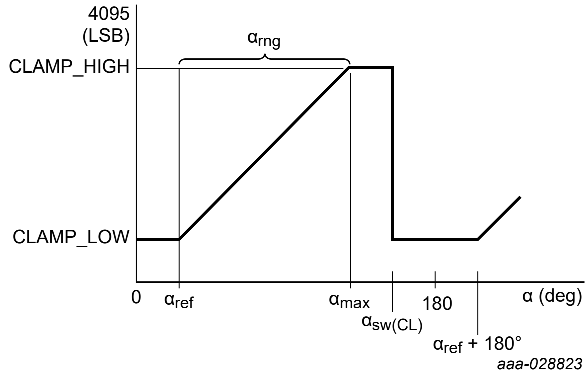
8 Digital output

KMA310 provides a digital output signal on pin OUT/DATA (if bit 12 in register SYS_SETTING is set to logic 1; see Table 51) compliant with the SAE J2716 SENT standard. The measured angle α is converted linearly into a value, which is digital encoded in SENT frames. Either a positive or a negative angular slope characteristic is provided for this purpose.

Table 4 describes the digital output behavior for a positive slope. A magnetic field angle above the programmed maximum angle α_{max} but below the clamp switch angle $\alpha_{sw(CL)}$ sets the output to the upper clamping value. If the magnetic field angle is larger than the clamp switch angle, the output value switches from upper to lower clamping value. If there is a negative slope, the clamping levels are changed.

Table 4. Digital output behavior for a positive slope

Magnetic field angle	Data value
$\alpha_{max} < \alpha < \alpha_{sw(CL)}$	CLAMP_HIGH
$\alpha_{sw(CL)} < \alpha < \alpha_{ref} + 180°$	CLAMP_LOW



$\alpha_{max} = \alpha_{ref} + \alpha_{rng}$

Figure 4. Characteristic of the digital output

8.1 Transmission of sensor messages

KMA310 encodes a 12-bit angular value into a sequence of pulses based on the encoding scheme of the SAE J2716 SENT standard. Data is split into 4-bit nibbles that are encoded in the time-domain as the duration between two falling edges. The message frame is a sequence of 4-bit nibbles (SENT frame). The timebase of the SENT frame is defined in clock ticks with a configurable duration of T_{clk} = 2.7 μs, 3 μs, 4.5 μs, and 6 μs each clock tick. A calibration pulse (SYNC nibble) followed by a STATUS nibble, a constant number of fast channel DATA nibbles, a CRC nibble, and an optional PAUSE pulse define one message frame of a SENT transmission as shown in Figure 5. The KMA310 is compatible with revisions of the SENT specification listed below and supports data formats in accordance with appendix A.1, H.1, A.3, H.4, and H.3.

General SENT specification can be found in:

- SAE J2716 FEB2008 SENT rev 2
- SAE J2716 JAN2010 SENT rev 3
- SAE J2716 APR2016 SENT rev 4

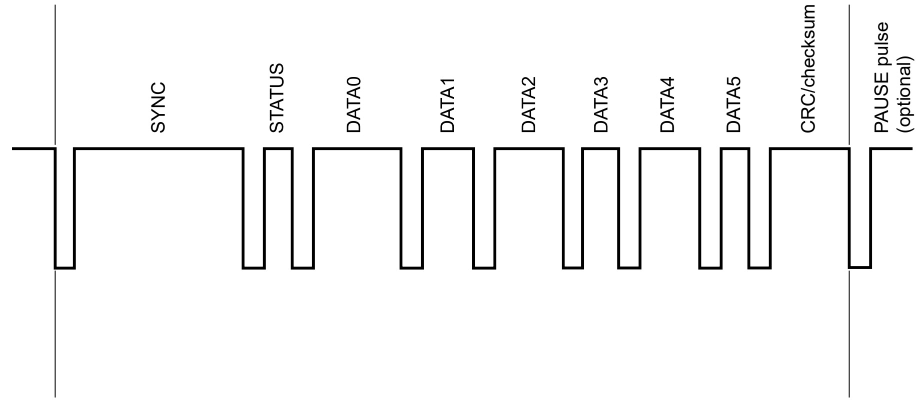


Figure 5. SENT frame

8.2 SYNC nibble

The synchronization and calibration nibble is always 56 clock ticks long. The receiver uses the SYNC nibble to derive the clock tick time from the SENT frame.

8.3 STATUS nibble

The STATUS nibble contains status and slow channel information of the KMA310. Bit 0 reflects the operating mode, i.e. normal or diagnostic mode. Bit 1 is a pre-warning indication and is set while the device is still in normal mode. For a detailed description of the pre-warning bit, see Section 8.11.1.2.

Bit 2 and bit 3 are used for optional slow channel serial data messages using the enhanced serial protocol (ESP), described in Section 8.10.

Table 5. STATUS nibble

Bit	Description
3 [most significant bit (MSB)]	serial data message bit if ESP is enabled, otherwise logic 0
2	serial data message bit if ESP is enabled, otherwise logic 0
1	pre-warning[1] 0b – normal operation 1b – pre-warning condition
0 [least significant bit (LSB)]	operating mode[2] 0b – normal operation 1b – diagnostic condition[3]

[1] Bit 1 can be permanently set to logic 0 via register bit; see Table 51.
[2] Bit 0 can be permanently set to logic 0 via register bit; see Table 51.
[3] Enable the serial data communication for detailed diagnostic information; see Table 14 and Table 15.

8.4 CRC nibble

The CRC nibble contains the 4-bit checksum of the DATA nibbles only. The CRC calculation does not cover the STATUS nibble.

The CRC is calculated using polynomial $x^4 + x^3 + x^2 + 1$ with seed value of 0101b. The KMA310 supports both the legacy CRC defined in SENT SAE J2716 FEB2008 and earlier revisions and the recommended CRC defined in SENT SAE J2716 JAN2010 and later.

The CRC version can be selected via CRC type bit in the SENT_SETTING1 register; see Table 51. CRC in accordance with SAE J2710 JAN2010 is the default configuration.

8.5 PAUSE pulse

A PAUSE pulse can be optionally attached to the SENT frame to generate messages with a constant frame length via register; see Table 51. The frame length depends on the protocol format:

- A.1 and H.1: 239 clock ticks
- A.3 and H.4: 269 clock ticks
- H.3: 196 clock ticks

Additionally, the frame length with PAUSE pulse can be set to 297 clock ticks for all protocol formats via register.

8.6 DATA nibbles

In general, the DATA nibbles contain the fast channel angular value of the device. The DATA nibble content depends on the selected protocol format. KMA310 supports the following different protocol formats as defined in the SAE J2716 SENT specification:

- Single secure sensor format A.3 (rev 3), H.4 (rev 4)
- Dual throttle position sensor format A.1 (rev 3), H.1 (rev 4)
- High-speed 12-bit message format H.3 (rev 4)

A detailed frame format description can be found in the corresponding subsection.

8.7 Single secure sensor formats A.3 and H.4

KMA310 generates the sequence defined in Table 6 repeatedly in accordance with the single secure sensor format defined in SAE J2716 JAN2010 SENT appendix A.3, respectively J2716 APR2016 SENT appendix H.4. DATA nibbles D0 to D2 contain the 12-bit angular value. D3 and D4 reflect the value of an 8-bit loop counter. D5 is an inverted copy of the most significant nibble (MSN) DATA0. The difference between A.3 and H.4 is that A.3 uses the whole 12-bit data range for angular values while H.4 excludes the values 0 and 4089 to 4095 from the angular data range for diagnostic purposes; see Table 7.

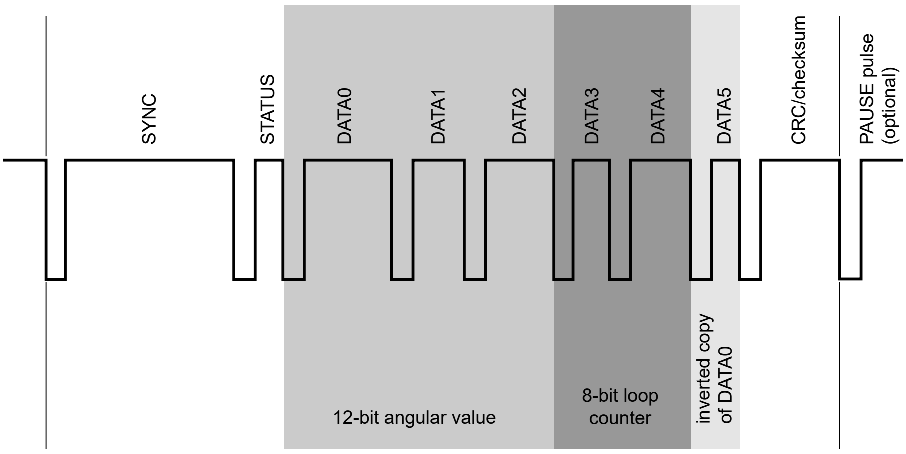


Figure 6. Single secure sensor formats A.3 and H.4

Table 6. Single secure sensor formats A.3 and H.4: frame

SYNC	STATUS	DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	CRC
-	diagnostic and pre-warning	D0[1]	D1	D2[2]	D3[1]	D4[2]	D5	-
-		12-bit angular value			8-bit loop counter		inverted D0	-

[1] MSN.

[2] Least significant nibble (LSN).

DATA nibbles D0 to D2 contain the angular value information in the single secure sensor format. A.3 uses the complete 12-bit data range for angular values while H.4 has reserved values for initialization and diagnostic information.

Table 7. DATA nibbles D0 to D2: angular value

D0[1]	D1	D2[2]	A.3		H.4	
			12-bit value	Angle	12-bit value	Angle/mode
0000	0000	0000	0	0°	0	initialization message
0000	0000	0001			1	0°
:	:	:			:	:
1111	1111	1000			4088	α_{max}
1111	1111	:	:	:	:	reserved
1111	1111	1010			4090	diagnostic mode[3]
1111	1111	:			:	reserved
1111	1111	1111	4095	α_{max}	4095	reserved

[1] MSN.

[2] LSN.

[3] For detailed diagnostic information, the serial data communication can be enabled.

Data nibbles D3 and D4 contain an 8-bit loop counter value with wrap-around common for both protocol formats A.3 and H.4.

Table 8. DATA nibbles D3 and D4: 8-bit loop counter

D3[1]	D4[2]	8-bit loop counter
0000	0000	0
:	:	:
1111	1111	255

[1] MSN.

[2] LSN.

For the single secure sensor format H.4 the clamping levels must be set to the correct values to comply with the SAE J2716 SENT specification: CLAMP_HIGH = 4088, CLAMP_LOW = 1. Otherwise angular values overwrite the reserved data range for diagnostic information.

8.8 Dual throttle position sensor formats A.1 and H.1

The KMA310 generates the sequence defined in Table 9 repeatedly in accordance with the dual throttle position sensor format defined in SAE J2716 JAN2010 SENT appendix A.1 or H.1 defined in SAE J2716 APR2016.

DATA nibbles D0 to D2 contain the 12-bit angular value. DATA nibbles D3 to D5 contain the opposite slope of the same 12-bit angular value while also the order of these DATA nibbles is reversed.

A.1 uses the data range 1 to 4094 for angular values and the values 0 and 4095 for diagnostic information. While H.1 uses data range 1 to 4088 for angular values and 4090 for diagnostic information.

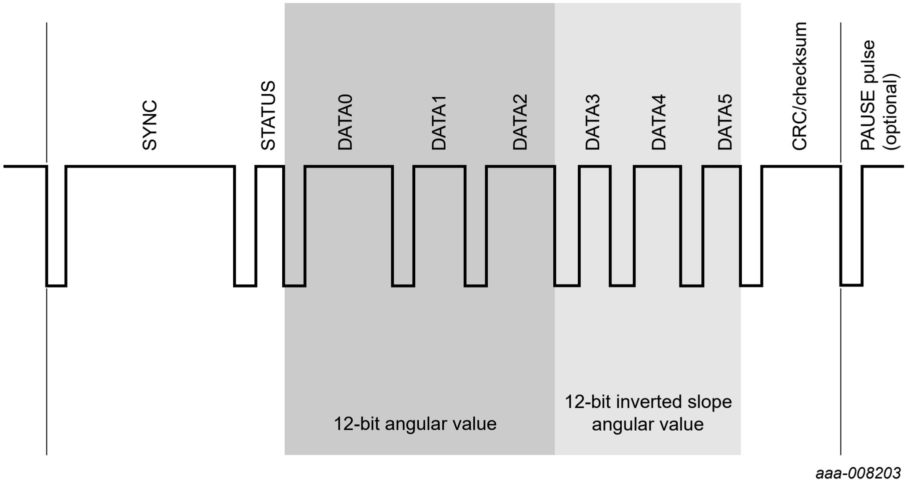


Figure 7. Dual throttle position sensor formats A.1 and H1

Table 9. Dual throttle position sensor formats A.1 and H.1: frame

SYNC	STATUS	DATA0	DATA1	DATA2	DATA3	DATA4	DATA5	CRC
-	diagnostic and pre-warning	D0[1]	D1	D2[2]	D5[2]	D4	D3[1]	-
-		12-bit angular value			12-bit inverted slope angular value			-

[1] MSN.

[2] LSN.

DATA nibbles D0 to D2 contain the angular value information in the dual throttle position sensor formats A.1 and H.1.

Table 10. DATA nibbles D0 to D2: angular value

D0[1]	D1	D2[2]	A.1		H.1	
			12-bit value	Angle	12-bit value	Angle/mode
0000	0000	0000	0	reserved	0	initialization message
0000	0000	0001	1	0°	1	0°
:	:	:			:	:
1111	1111	1000			4088	α_{max}
1111	1111	:	:	:	:	reserved
1111	1111	1010			4090	diagnostic mode[3]
1111	1111	:			:	reserved
1111	1111	1110	4094	α_{max}	4094	reserved
1111	1111	1111	4095	diagnostic mode[3]	4095	reserved

[1] MSN.

[2] LSN.

[3] For detailed diagnostic information, the serial data communication can be enabled.

For the inverted slope angular value in the DATA nibbles D3 to D5 the order of nibbles is also reversed: LSN and MSN.

When a diagnostic condition occurs in A.1 mode, the DATA nibbles D0 to D2 are all set to Fh and DATA nibbles D3 to D5 are all set to 0h. In H.1 mode, the data value of nibbles D0 to D2 is set to 4090 and DATA nibbles D3 to D5 are inverted to diagnostic value 5.

Table 11. DATA nibbles D3 to D5: inverted slope angular value

D5[1]	D4	D3[2]	A.1		H.1	
			12-bit value	Angle	12-bit value	Angle/mode
0000	0000	0000	0	diagnostic mode[3]	0	reserved
0000	0000	0001	1	α_{max}	1	reserved
:	:	:	:	:	:	reserved
0000	0000	0101	:	:	5	diagnostic mode[3]
:	:	:	:	:	:	reserved
0000	0000	0111	:	:	7	α_{max}
:	:	:	:	:	:	:
1111	1111	1110	4094	0°	4094	0°

D5[1]	D4	D3[2]	A.1		H.1	
			12-bit value	Angle	12-bit value	Angle/mode
1111	1111	1111	4095	reserved	4095	initialization message

[1] MSN.
[2] LSN.
[3] For detailed diagnostic information, the serial data communication can be enabled.

For the dual throttle position sensor formats A.1 and H.1, the clamping levels must be set to the correct values to comply with the SAE J2716 SENT specification. A.1: CLAMP_HIGH = 4094, CLAMP_LOW = 1. H.1: CLAMP_HIGH = 4088, CLAMP_LOW = 1. Otherwise angular values overwrite the reserved data range for diagnostic information.

8.9 High-speed 12-bit message format H.3

The KMA310 generates the sequence defined in Table 12 repeatedly in accordance with the high-speed 12-bit message format H.3 defined in SAE J2716 APR2016. This mode realizes almost a doubling of the update rate compared to other modes. The increase of the update rate is achieved by transmitting 12-bit angular data with only four DATA nibbles using only 3 bit of the available 4 bit per nibble. The MSB of each nibble is always zero. Additionally, the clock tick length shall be set to 2.7 µs typically with a maximum variation of ±10 %. The SYNC, STATUS, and CRC nibble and the serial communication are the same as for the other protocol formats.

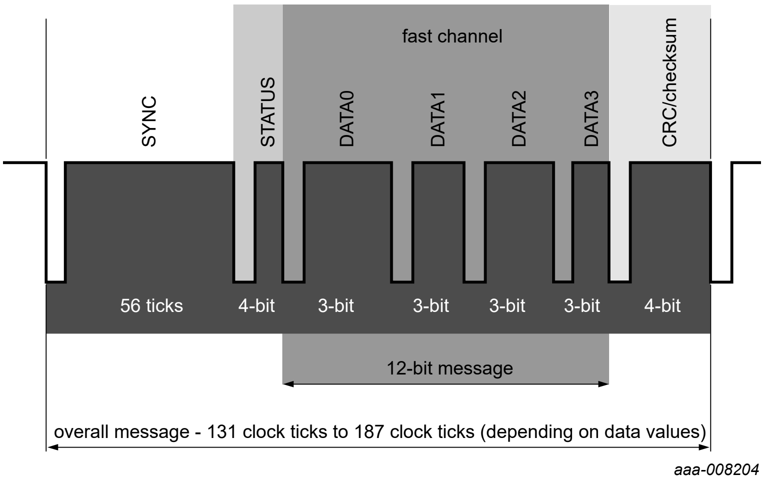


Figure 8. High-speed 12-bit message format frame H.3

Table 12. High-speed 12-bit message format: frame

SYNC	STATUS	DATA0	DATA1	DATA2	DATA3	CRC
-	diagnostic and pre-warning	D0[1]	D1	D2	D3[2]	-
-		12-bit angular value				-

[1] MSN.
[2] LSN.

Table 13. DATA nibbles D0 to D3: angular value

D0[1]	D1	D2	D3[2]	H.3	
				12-bit value	Angle/mode
0000	0000	0000	0000	0	initialization
0000	0000	0000	0001	1	0°
:	:	:	:	:	:
0111	0111	0111	0000	4088	α_{max}
0111	0111	0111	0001	4089	reserved
0111	0111	0111	0010	4090	diagnostic mode[3]
0111	0111	0111	:	:	reserved
0111	0111	0111	0111	4095	reserved

[1] MSN.

[2] LSN.

[3] For detailed diagnostic information, the serial data communication can be enabled.

For the 12-bit high-speed mode H.3, the clamping levels must be set to the correct values to comply with the SAE J2716 SENT specification. CLAMP_HIGH = 4088, CLAMP_LOW = 1. Otherwise angular values overwrite the reserved data range for diagnostic information.

8.10 Enhanced serial data communication

Beside the normal message transmission, also a slow serial data communication is realized using bit 2 and bit 3 of the STATUS nibble. The slow channel message stretches over 18 consecutive SENT frames and contains sensor temperature, supply voltage, diagnostic/status information, and user-programmable messages. These messages comply with the enhanced serial data message format with 8-bit message ID and 12-bit message data described in the SAE J2716 SENT specification. Table 14 shows the serial message cycle that is constantly repeated when enhanced serial data communication is enabled.

Table 14. Serial message schedule

Message number in serial message cycle	8-bit message ID	Definition	Comment
1	01h	diagnostic status code	see Table 15
2	23h	sensor temperature	see Table 21
3	1Ch	supply voltage	see Table 20
4	03h	sensor type	see Table 17
5	29h	sensor ID	see Table 22
6	05h	manufacturer code	see Table 18
7	06h	SENT revision	see Table 19
8	01h	diagnostic status code	see Table 15
9	23h	sensor temperature	see Table 21
10	1Ch	supply voltage	see Table 20
11	90h	OEM code 1	see Table 23

Message number in serial message cycle	8-bit message ID	Definition	Comment
12	91h	OEM code 2	see Table 24
13	92h	OEM code 3	see Table 25
14	93h	OEM code 4	see Table 26
15	94h	OEM code 5	see Table 27
16	95h	OEM code 6	see Table 28
17	96h	OEM code 7	see Table 29
18	97h	OEM code 8	see Table 30

8.10.1 Enhanced serial messages

Table 15. Diagnostic status code message

8-bit ID	12-bit code	Definition	Comment
01h	000h	no error	normal operation
	001h	OOR HIGH[1]	output value above OOR_HIGH register
	002h	OOR LOW[1]	output value below OOR_LOW register
	003h to 019h	reserved	
	020h	undervoltage[1]	V_{DD} below SENT_SETTING2[13:12]
	021h	overvoltage[1]	V_{DD} above SENT_SETTING2[15:14]
	022h	temperature[1]	application-specific integrated circuit (ASIC) temperature above SENT_SETTING2[11:7]
	023h	single-bit error[1]	CTRL1[10]
	024h to 800h	reserved	
	801h to FFFh	automotive safety integrity level (ASIL) error code	see Table 16

[1] If enabled, pre-warning is indicated and bit 1 of STATUS nibble is set.

Table 16. ASIL error code

Bit	Description	Safety mechanism
11 (MSB)	device in diagnostic mode CTRL1[14] (ASIL_STATUS_CODE[11])	-
10	angular range check	SM-12
9	CORDIC range check	SM-11
8	data adder check	SM-10
7	SD-ADC range check	SM-09
6	built-in self-test (BIST) encoding check	SM-08
5	control signal check and BIST completion check	SM-06 and SM-07
4	adjusted angle calculation check	SM-05
3	data conversion check	SM-04
2	data division check	SM-03

Bit	Description	Safety mechanism
1	inverted angle calculation check	SM-02
0 (LSB)	magnetic field conversion check	SM-01

Table 17. SENSOR_TYPE[3:0] – channel 1/2 sensor type message

8-bit ID	12-bit code	Definition	Comment
03h	051h[1]	acceleration pedal position 1 or acceleration pedal position 2	0000b
	052h[1]	acceleration pedal position 1 or secure sensor	0001b
	053h[1]	acceleration pedal position 2 (redundant signal) or secure sensor	0010b
	054h[1]	throttle position 1 or throttle position 2	0011b
	055h[1]	throttle position 1 or secure sensor	0100b
	056h[1]	throttle position 2 (redundant signal) or secure sensor	0101b
	059h[1]	angle position	0110b
	05Ah[1]	angle position or secure sensor	0111b
	062h[2]	angle position (high speed) H.3 protocol format	1000b
	063h[2]	angle position 1 or angle position 2 H.1 protocol format	1001b
	064h[2]	angle position or secure sensor H.4 protocol format	1010b
	066h[2]	reserved for angle position sensors	1011b
	000h	reserved	1101b to 1111b

[1] Compliant with SAE JAN2010 rev 3 only.

[2] Compliant with SAE APR2016 rev 4 only.

Table 18. Manufacturer code message

8-bit ID	12-bit code	Definition	Comment
05h	04Eh	NXP Semiconductors	fix value

Table 19. SENT_REVISION[1:0] – SENT standard revision message

8-bit ID	12-bit code	Definition	Comment
06h	000h	not specified	00b
	002h	FEB2008 rev 2	01b
	003h	JAN2010 rev 3	10b
	004h	APR2016 rev 4	11b

Table 20. Supplementary data channel #3,1: sensor supply voltage

8-bit ID	12-bit code	Definition	Comment
1Ch	000h to 1FFh	9-bit sensor supply voltage	V_{DD} [V] = (digital value [LSB] + 33) / 58
	200h to FFFh	reserved	

Table 21. Supplementary data channel #4,1: sensor temperature value

8-bit ID	12-bit code	Definition	Comment
23h	000h to 0FFh	8-bit sensor temperature	000h: −45 °C to 0FFh: +210 °C
	100h to FFFh	reserved	

Table 22. SENSOR_ID – sensor ID #1 message

8-bit ID	12-bit code	Definition	Comment
29h	000h	sensor ID1	0b
	FFFh	sensor ID2	1b

Table 23. OEM_CODE_1[11:0] – OEM code 1 message

8-bit ID	12-bit code	Definition	Comment
90h	000h to FFFh	OEM code 1	user-programmable data content

Table 24. OEM_CODE_2[11:0] – OEM code 2 message

8-bit ID	12-bit code	Definition	Comment
91h	000h to FFFh	OEM code 2	user-programmable data content

Table 25. OEM_CODE_3[11:0] – OEM code 3 message

8-bit ID	12-bit code	Definition	Comment
92h	000h to FFFh	OEM code 3	user-programmable data content

Table 26. OEM_CODE_4[11:0] – OEM code 4 message

8-bit ID	12-bit code	Definition	Comment
93h	000h to FFFh	OEM code 4	user-programmable data content

Table 27. OEM_CODE_5[11:0] – OEM code 5 message

8-bit ID	12-bit code	Definition	Comment
94h	000h to FFFh	OEM code 5	user-programmable data content

Table 28. OEM_CODE_6[11:0] – OEM code 6 message

8-bit ID	12-bit code	Definition	Comment
95h	000h to FFFh	OEM code 6	user-programmable data content

Table 29. OEM_CODE_7[11:0] – OEM code 7 message

8-bit ID	12-bit code	Definition	Comment
96h	000h to FFFh	OEM code 7	user-programmable data content

Table 30. OEM_CODE_8[11:0] – OEM code 8 message

8-bit ID	12-bit code	Definition	Comment
97h	000h to FFFh	OEM code 8	user-programmable data content

8.11 SENT diagnostic

The SENT standard specifies different methods to transmit diagnostic information. These methods are used in multiple combinations, depending on the SENT revision, protocol format, and device configuration.

8.11.1 STATUS nibble diagnostic

Bit 0 and bit 1 of the STATUS nibble can be used to signal the diagnostic state while the DATA nibbles still contain an angular value at the same time. The CRC nibble does not include the STATUS nibble, thus the receiver do not detect an erroneous STATUS nibble.

8.11.1.1 Diagnostic bit

The device defines bit 0 of the STATUS nibble as diagnostic bit. In case the device is in diagnostic mode the diagnostic bit is set to logic 1.

The diagnostic bit can be disabled and permanently set to logic 0 via the mask STATUS nibble bits in the SENT_SETTING2 register in the non-volatile memory; see Table 51.

8.11.1.2 Pre-warning bit

Bit 1 is a pre-warning indication which is set while the device is still in normal mode, but one of the following conditions occurred:

- The angular value is above the programmed upper out of range (OOR) threshold; see Table 53.
- The angular value is below the programmed lower OOR threshold; see Table 53.
- Corrected single-bit error of the non-volatile memory (EDC); see Section 10.1.
- The temperature is above the programmed temperature threshold; see Table 51.
- Overvoltage: The supply voltage is above the programmed upper voltage threshold; see Table 51.
- Undervoltage: The supply voltage is below the programmed lower voltage threshold; see Table 51.

The pre-warning bit can be disabled and permanently set to logic 0 via the mask STATUS nibble bits in the SENT_SETTING2 register in the non-volatile memory; see Table 51.

8.11.2 Fast channel diagnostic value

Some protocol formats define a reserved data range in the fast channel communication for signaling diagnostic status instead of an angular value in the SENT transmission.

The KMA310 generates a specific diagnostic value instead of an angular value in case the device is in diagnostic mode. The diagnostic value depends on the selected protocol format according to Table 31.

Table 31. Fast channel diagnostic value

Protocol format	Normal mode	Diagnostic mode
A.1	angular value	4095
A.3	angular value	angular value
H.1	angular value	4090
H.3	angular value	4090
H.4	angular value	4090

8.11.3 Enhanced serial protocol diagnostic status code message

Detailed diagnostic and pre-warning information is transmitted in the diagnostic status code message ID 01h of the slow channel message transmission. Therefore, the enhanced serial protocol must be enabled via the ESP bit in the SENT_SETTING1 register in the non-volatile memory; see Table 51. A description of the diagnostic status code message is given in Table 15.

9 Output characteristic

The MPC defines the output transfer characteristic. For this purpose, up to 17 calibration points define the range between programmed reference angle and set maximum angle.

Three different MPC types are available, see Table 51, whereas in each mode either a positive or a negative slope can be programmed. MPC17 and MPC7 enable an improved linearization of the output characteristic.

Furthermore, curve shapes can be customized in accordance with application requirements.

9.1 No MPC mode

No MPC mode refers to the conventional linear output characteristic defined by zero angle (ZERO_ANGLE), angular range (RANGE_DETECTION), clamp switch angle (CLAMP_SWITCH), and clamping levels (CLAMP_LOW and CLAMP_HIGH).

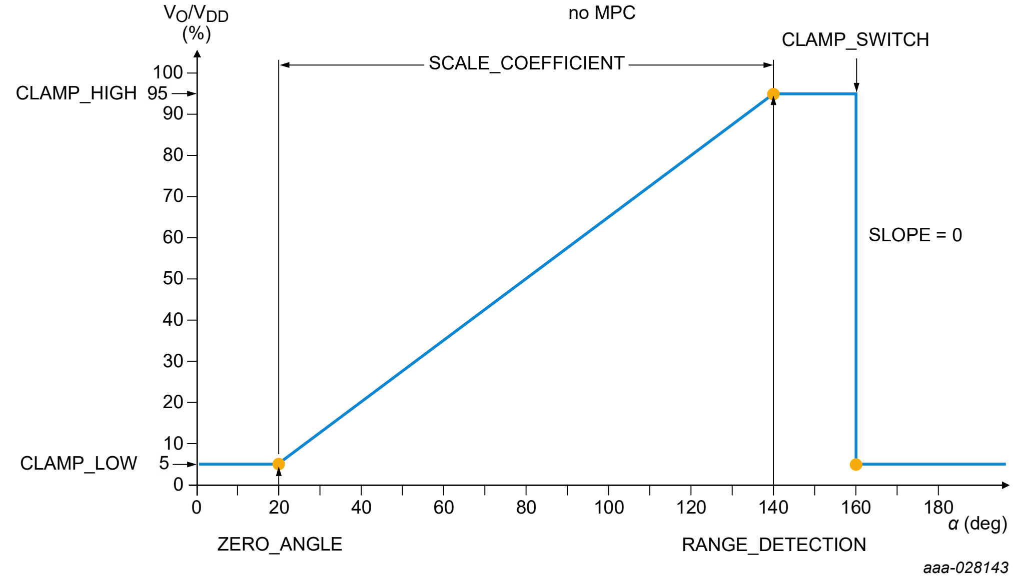


Figure 9. No MPC mode

9.2 MPC17 mode

MPC17 mode enables curve shaping by 17 equidistant calibration points. For this purpose 16 coefficients (MPC_COEFFICIENTn) can be programmed, see Table 52, to set a specific output level for each calibration point.

In this mode, all points are scaling with the angular range to define calibration coefficients at equidistant positions as shown in Figure 10.

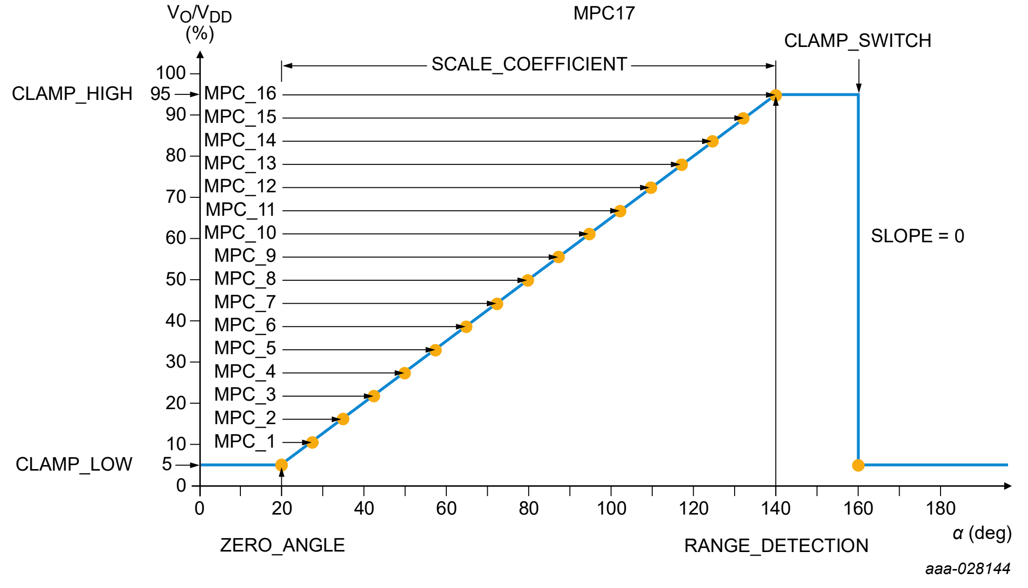


Figure 10. MPC17 mode

9.3 MPC7 mode

MPC7 in contrast provides a set of six freely selectable calibration points defined by angular position (linear Xn), output level (linear Yn), and slope (linear Sn) as shown in Figure 11.

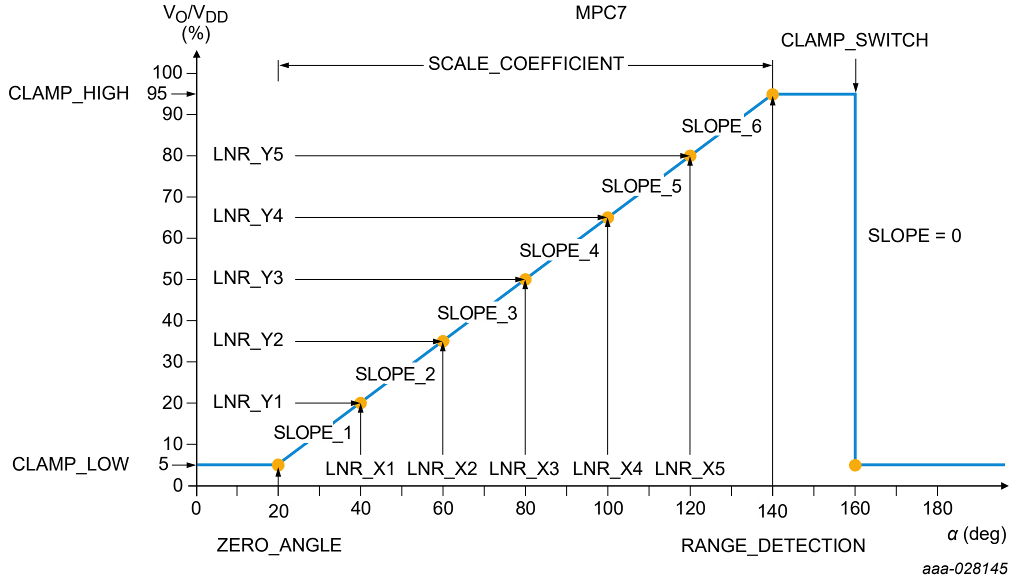


Figure 11. MPC7 mode

10 Diagnostic features

KMA310 provides following diagnostic features. The safety mechanisms supporting functional safety operation are marked with individual numbers SM-xx. Functional risks are only minimized if all safety mechanisms are enabled as in the default configuration. Thus it is not recommended to switch them off individually.

10.1 NVM CRC (SM-20), NVM EDC check (SM-21), and NVM ECC check (SM-22)

The device includes a supervision of the programmed data. At power-on, a CRC of the non-volatile memory is performed (SM-20). The NVM is split into three customer areas with individual CRCs (CRC1, CRC2, and CRC3) and a manufacturer area which is user access restricted and also CRC protected. Furthermore, the memory is protected against bit errors. Every 16-bit data word is saved internally as a 22-bit word for this purpose. The protection logic corrects any single-bit error in a data word (SM-22), while the sensor continues in normal operation mode. Furthermore, the logic detects double-bit error per word and switches the output into diagnostic mode (SM-21).

10.2 Power-loss detection (SM-18) and GND-loss detection (SM-19)

The power-loss detection circuit enables the detection of an interrupted supply or ground line of the mixed signal IC. If there is a power-loss condition, two internal switches in the sensor are closed, connecting the pin of the analog output to the supply voltage and the ground pin.

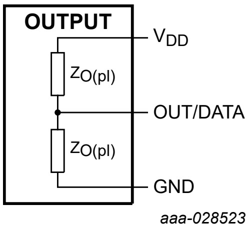


Figure 12. Equivalent output circuit in a power-loss condition

Table 32 describes the power-loss behavior and gives the resulting output voltage depending on the interrupted supply or ground line and the load resistance.

Table 32. Power-loss behavior

Load resistance	Interrupted supply line	Interrupted ground line
$R_{L(ext)} > 5\ k\Omega$	$V_O \leq 4\ \%V_{DD}$	$V_O \geq 96\ \%V_{DD}$

10.3 Supply overvoltage detection (SM-16) and undervoltage detection (SM-17)

If the supply voltage is below the switch-off threshold voltage, a status bit is set and the output goes into diagnostic mode. If the supply voltage is above the overvoltage switch-on threshold voltage, the output switches to diagnostic mode. Table 33 describes the system behavior depending on the voltage range of the supply voltage.

Table 33. System behavior for each output mode

Supply voltage	State	Analog mode	SENT mode
0 V to ≅ 1.8 V	startup power	The output buffer drives an active LOW or is powered down, but the switches of the power-loss detection circuit are not fully opened and set the output to a level between ground and half the supply voltage.	high-ohmic output stage; external pull-up resistor defines output voltage
≅ 1.8 V to V_{POR}	power-on reset	The power-loss charge pump is fully operational and turns the switches of the detection circuit off. The output buffer drives an active LOW and sets the output to the lower diagnostic level. During the reset phase, all circuits are in reset and/or power-down mode.	The output buffer drives an active LOW. During the reset phase, all circuits are in reset and/or power-down mode.
V_{POR} to $V_{th(on)}$ or $V_{th(off)}$	initialization	The digital core and the oscillator are active. After reset, the content of the non-volatile memory is copied into the shadow registers. The output buffer drives an active LOW.	The digital core and the oscillator are active. After reset, the content of the non-volatile memory is copied into the shadow registers. The output buffer drives an active LOW.

Supply voltage	State	Analog mode	SENT mode
$V_{th(on)}$ or $V_{th(off)}$ to minimum V_{DD}	functional operation	All analog circuits are active and the measured angle is available at the analog output. Not all parameters are within the specified limits.	All analog circuits are active and the output is set to HIGH for at least 100 μs before SENT transmission starts. Not all parameters are within the specified limits.
Minimum V_{DD} to maximum V_{DD}	normal operation	All analog circuits are active and the measured angle is available at the analog output. All parameters are within the specified limits.	All analog circuits are active and the measured angle is available at the digital output. All parameters are within the specified limits.
Maximum V_{DD} to $V_{th(ov)}$	functional operation	All analog circuits are active and the measured angle is available at the analog output. Not all parameters are within the specified limits.	All analog circuits are active and the measured angle is available at the digital output. Not all parameters are within the specified limits.
$V_{th(ov)}$ to 18 V	overvoltage	The digital core and the oscillator are active but all other circuits are in power-down mode. The output is set to the lower diagnostic level.	The digital core and the oscillator are active but all other circuits are in power-down mode. The output buffer drives an active LOW.

Table 34 describes the diagnostic behavior and the resulting output voltage depending on the error case. Furthermore the duration and termination condition to enter and leave the diagnostic mode are given, respectively.

Table 34. Diagnostic behavior

Diagnostic condition	Duration	Output	Termination condition
Low voltage	20 μs < t < 120 μs	≤ 4 %V_{DD}	functional or normal operation
Overvoltage	20 μs < t < 120 μs	≤ 4 %V_{DD}	functional or normal operation
Checksum error	n.a.	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]	power-on reset[2]
Double-bit error	n.a.	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]	power-on reset[2]
Power-loss	≤ 2 ms	≤ 4 %V_{DD} or ≥ 96 %V_{DD}; see Table 32	power-on reset

[1] Depending on the diagnostic level setting.

[2] Status bit stays set in command register until power-on reset.

10.4 Oscillator monitoring (SM-13, SM-14 and SM-15)

If the oscillator frequency differs from the target frequency by more than ±30 % or the oscillator stops, status bit 7 of CTRL1 register is set and the output goes into diagnostic mode; see Table 50. If the oscillator frequency differs by more than ±10 %, the SENT timing can violate the SAE J2716 SENT specification.

10.5 Safe assure - ASIL control unit

The ASIL control includes a state machine, which is a 4-bit up-counter that defines time slots. The different time slots are used to trigger dedicated BISTs. To enable or disable the complete ASIL control unit globally, use the BIST bit in ASIL_SETTING register; see Table 51. The NVM register setting enables or disables individually each integrated test.

In case a self-test was performed a ready flag is generated to reset the start test trigger signals. In case no reset signal is found, the output is set to diagnostic mode.

10.5.1 Timing description

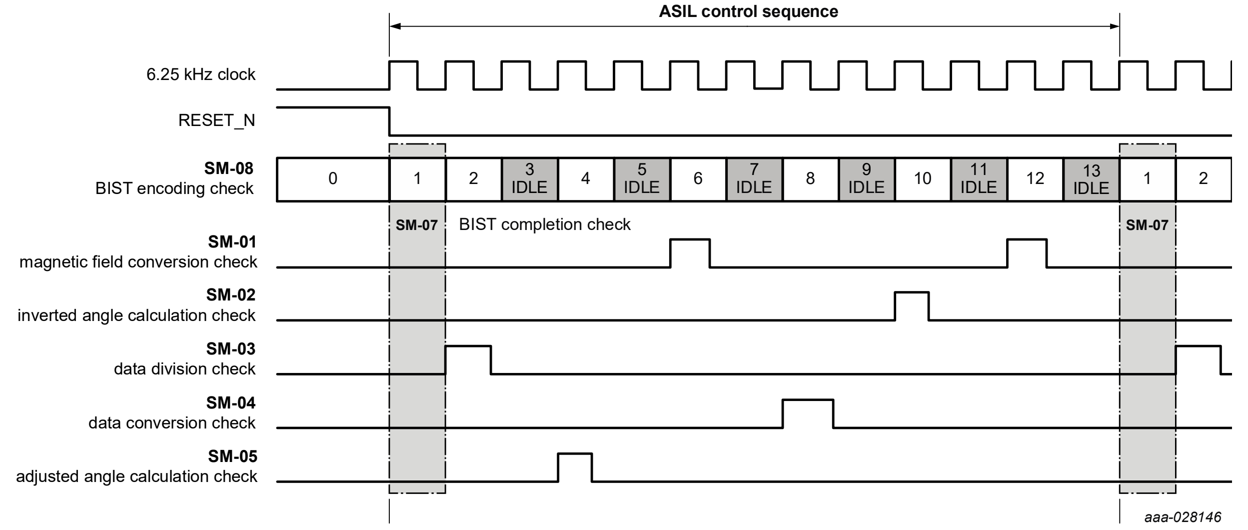


Figure 13. Sequence state register and start flags for integrated self-checks

10.5.2 User selectable BIST

To enable the BISTs SM-01 to SM-06 set the BIST bit in ASIL_SETTING register; see Table 51. User selectable self-tests can be enabled or masked separately as described in the following subsections.

10.5.2.1 Magnetic field conversion check (SM-01)

The output amplitude of an AMR sensor has a strong temperature dependency. This physical effect is used to check the plausibility of the AMR signals. The magnetic field conversion check compares a temperature value, which is based on an on-chip temperature sensor with the temperature information based on the AMR amplitude. In case the magnet is removed, the AMR amplitude goes down, and the magnetic field conversion check indicates this failure mode. Furthermore, this check can be switched off separately with the magnetic field conversion check bit of the ASIL_SETTING register; see Table 51.

In case the on-chip temperature sensor fails, the product goes to diagnostic condition, even if the angle data path is not directly affected from this failure mode.

10.5.2.2 Inverted angle calculation check (SM-02)

The inverted angle calculation check calculates a second internal output angle value. Based on the customer settings the second angle value is an exact inverted copy of the main data path angle. The check compares the sum of both calculated angle values with the sum of both adjusted customer clamping levels. In case the post-CORDIC integrated adder and multiplier are in normal operating mode the result is equal. Furthermore, this check can be switched off separately with the inverted angle calculation check bit of the ASIL_SETTING register; see Table 51.

In case internal post-memory addressing, post-multiplier or post-adder fails, the product goes into diagnostic mode.

10.5.2.3 Data division check (SM-03)

The main data path division module is only used in MPC17 mode. Nevertheless, the integrated data division check uses the same hardware, which is used by the post-CORDIC. This test performs a test division with a known result. To execute the data division check, also the post-adder and the post-memory addressing are used. Furthermore, this check can be switched off separately with the data division check bit of the ASIL_SETTING register; see Table 51.

In case internal post-memory addressing, post-adder or division fails, the product goes into diagnostic mode.

10.5.2.4 Data conversion check (SM-04)

The data conversion check checks the CORDIC module, which is used for all modes. For testing, internal cos and –sin signals are used to calculate an inverted CORDIC angle. The sum of the main data path CORDIC angle and the inverted CORDIC angle must be zero. Furthermore, this check can be switched off separately with the data conversion check bit of the ASIL_SETTING register; see Table 51.

In case internal subblocks of the CORDIC module (shift register, adder, state-controller) fail, the product goes into diagnostic mode.

10.5.2.5 Adjusted angle calculation check (SM-05)

The zero angle corrected CORDIC signal is one of the most important signals within the system. This signal is used for the main data path angle value and for the segment detection for MPC7 and MPC17 mode. The integrated adjusted angle calculation check compares the post-CORDIC zeroed result with a redundant calculated CORDIC zeroed signal. The arithmetic logic unit (ALU) ASIL module performs this redundant calculation. Furthermore, this check can be switched off separately with the adjusted angle calculation check bit of the ASIL_SETTING register; see Table 51.

In case the redundant calculation of the ALU ASIL check fails, the product goes into diagnostic mode, even if the angle data path is not directly affected from this failure mode.

10.5.3 Fixed internal diagnostics

The following internal diagnostics are permanently enabled and automatically executed. The corresponding flags can be masked individually.

10.5.3.1 Control signal check (SM-06)

Checks, if the main data path processing was performed correctly. This status flag can be masked with the mask control signal check bit of the ASIL_SETTING register; see Table 51.

10.5.3.2 BIST completion check (SM-07)

Checks, if all selected self-tests were executed without any errors. In case a failure mode occurs at one selected test, the BIST completion check flag indicates this failure latest after 160 µs.

In case the ASIL control block fails, the product goes into diagnostic mode, even if the angle data path is not directly affected from this failure mode. This status flag can be masked with the mask BIST completion check bit of the ASIL_SETTING register; see Table 51.

10.5.3.3 BIST encoding check (SM-08)

The ASIL control module provides the test sequence number for all implemented self-tests. To prove that this module is running normal, the state register of the ASIL control module is coded with a parity bit to prevent single bit failures.

In case the ASIL control block fails, the product goes into diagnostic mode, even if the angle data path is not directly affected from this failure mode. This status flag can be masked with the mask BIST encoding check bit of the ASIL_SETTING register; see Table 51.

10.5.3.4 SD-ADC range check (SM-09)

The SD-ADC is not using full scale range. Some part is reserved to detect overflows. In case the filter result is larger than 95 % (including the gain factor) the overflow flag is set. This status flag can be masked with the mask SD-ADC range check bit of the ASIL_SETTING register; see Table 51.

10.5.3.5 Data adder check (SM-10)

The pre-CORDIC adder is used for AMR offset cancelation, new AMR offset value calculation, and temperature calculation from the auxiliary ADC. In case overflow occurs, the bit is set. This status flag can be masked with the mask data adder check bit of the ASIL_SETTING register; see Table 51.

10.5.3.6 CORDIC range check (SM-11)

The CORDIC block, which is used for angle calculation, is using internally more than 16 bit. To prevent a wrap-around for unexpected sin/cos input signals, the block has a built-in overflow monitor. In case overflow occurs, a status flag is set. This status flag can be masked with the mask CORDIC range check bit of the ASIL_SETTING register; see Table 51.

10.5.3.7 Angular range check (SM-12)

The clamp control checks the plausibility of the internal status flags coming from the clamp and range detection. In case the clamp switch angle position was detected before the range position, the flag is set. This status flag can be masked with the mask angular range check bit of the ASIL_SETTING register; see Table 51.

10.6 Self-diagnostic overview

Table 35. Self-diagnostic overview

Diagnostic block	Mode	Monitoring interval	Output behavior	
Supply overvoltage detection (SM-16)	always	continuously	≤ 4 %V_{DD}	
Supply undervoltage detection (SM-17)	always	continuously	≤ 4 %V_{DD}	
Power-loss detection (SM-18) (broken V_{DD} wire)	always	continuously	≤ 4 %V_{DD}	
GND-loss detection (SM-19) (broken GND wire)	always	continuously	≥ 96 %V_{DD}	
NVM CRC (SM-20)	startup	-	≤ 4 %V_{DD}	
NVM EDC double-bit error check (SM-21)	NVM read	-	≤ 4 %V_{DD}	
NVM error correcting code (ECC) single-bit error check (SM-22)	NVM read	-	SENT status nibble pre-warning bit	
Magnetic field conversion check (SM-01)	always	1.04 ms	analog:	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]
			SENT ESP:	801h
			ASIL_FLAGS:	0001h
Inverted angle calculation check (SM-02)	always	2.08 ms	analog:	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]
			SENT ESP:	802h
			ASIL_FLAGS:	0002h
Data division check (SM-03)	always	2.08 ms	analog:	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]
			SENT ESP:	804h
			ASIL_FLAGS:	0004h
Data conversion check (SM-04)	always	2.08 ms	analog:	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]
			SENT ESP:	808h
			ASIL_FLAGS:	0008h
Adjusted angle calculation check (SM-05)	always	2.08 ms	analog:	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]
			SENT ESP:	810h
			ASIL_FLAGS:	0010h
Control signal check (SM-06)	always	160 µs	analog:	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]
			SENT ESP:	820h
			ASIL_FLAGS:	0020h
BIST completion check (SM-07)	always	1.25 µs	analog:	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]
			SENT ESP:	820h
			ASIL_FLAGS:	0040h
BIST encoding check (SM-08)	always	1.25 µs	analog:	≤ 4 %V_{DD} or ≥ 96 %V_{DD}[1]
			SENT ESP:	840h
			ASIL_FLAGS:	0080h

Diagnostic block	Mode	Monitoring interval	Output behavior	
SD-ADC range check (SM-09)	always	10 μs	analog:	$\leq 4\ \%V_{DD}$ or $\geq 96\ \%V_{DD}$[1]
			SENT ESP:	880h
			ASIL_FLAGS:	0100h
Data adder check (SM-10)	always	1.25 μs	analog:	$\leq 4\ \%V_{DD}$ or $\geq 96\ \%V_{DD}$[1]
			SENT ESP:	900h
			ASIL_FLAGS:	020h
CORDIC range check (SM-11)	always	160 μs	analog:	$\leq 4\ \%V_{DD}$ or $\geq 96\ \%V_{DD}$[1]
			SENT ESP:	A00h
			ASIL_FLAGS:	0400h
Angular range check (SM-12)	always	160 μs	analog:	$\leq 4\ \%V_{DD}$ or $\geq 96\ \%V_{DD}$[1]
			SENT ESP:	C00h
			ASIL_FLAGS:	0800h
Upper oscillator frequency check (SM-13)	always	continuously	$\leq 4\ \%V_{DD}$	
Lower oscillator frequency check (SM-14)	always	continuously	$\leq 4\ \%V_{DD}$	
Oscillator stuck-at check (SM-15)	always	continuously	$\leq 4\ \%V_{DD}$	

[1] Depending on the diagnostic level setting.

10.7 Self-diagnostic validation support

To validate the correct function of self-diagnostics within the system, enable the self-diagnostic validation support bit 10 in SYS_SETTING register. In case this bit is logic 1 the device shows diagnostic modes based on the content of OEM_CODE1 register; see Table 36. In case this bit is logic 0 the device is in normal operating mode which is the default mode.

Table 36. Self-diagnostic validation support

OEM_CODE1 value	Safety mechanism	Comment
001h	SM-01	magnetic field conversion check
002h	SM-02	inverted angle calculation check
004h	SM-03	data division check
008h	SM-04	data conversion check
010h	SM-05	adjusted angle calculation check
020h	SM-06[1]	control signal check
040h	SM-07[1]	BIST completion check
080h	SM-08[1]	BIST encoding check
100h	SM-09[1]	SD-ADC range check
200h	SM-10[1]	data adder check
400h	SM-11[1]	CORDIC range check
800h	SM-12[1]	angular range check

[1] Disable the corresponding ASIL mask bits in the ASIL_SETTING register.

11 Limiting values

Table 37. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.3	+18	V
V_O	output voltage		−0.3	+18	V
$V_{O(ov)}$	overvoltage output voltage	T_{amb} < 140 °C at t < 1 h [1]	$V_{th(ov)}$	18	V
I_r	reverse current	T_{amb} < 70 °C	-	150	mA
T_{amb}	ambient temperature		−40	+180	°C
$T_{amb(pr)}$	programming ambient temperature		10	70	°C
T_{stg}	storage temperature		−40	+125	°C
t_{diag}	diagnostic time	output voltage level ≤ 4 %V_{DD} or ≥ 96 %V_{DD}	-	100	h
Non-volatile memory					
$t_{ret(D)}$	data retention time	T_{amb} = 50 °C	17	-	year
$N_{endu(W\_ER)}$	write or erase endurance	$T_{amb(pr)}$ = 70 °C	100	-	cycle

[1] Overvoltage on output and supply within the specified operating voltage range.

12 Recommended operating conditions

Table 38. Operating conditions

In a homogenous magnetic field.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	[1]	4.5	5.0	5.5	V
T_{amb}	ambient temperature		−40	-	+180	°C
$T_{amb(pr)}$	programming ambient temperature		10	-	70	°C
H_{ext}	external magnetic field strength		25	-	-	kA/m
Analog						
$R_{L(ext)}$	external load resistance	[2]	5	-	∞	kΩ
$C_{L(ext)}$	external load capacitance	[1][3]	0	-	22	nF
		[3][4]	0	-	6.8	nF
SENT						
$R_{L(ext)}$	external load resistance	[5]	10	-	55	kΩ
$C_{L(ext)}$	external load capacitance	[1][3][6]	0	-	3.5	nF

[1] Normal operation mode.
[2] Power-loss detection is only possible with a load resistance within the specified range connected to the supply or ground line.
[3] Between ground and output.
[4] Command mode.
[5] Pull-up resistance between output and supply.
[6] Without internal load capacitance; part of capacitance is defined as input capacitor inside receiver circuit according to SENT specification; see application information in Section 19.2.

13 Thermal characteristics

Table 39. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		155	K/W

14 Characteristics

Table 40. Mechanical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{lead}	mechanical force to the leads	T_{amb} = 25 °C	-	-	5	N

Table 41. Supply current

Characteristics are valid for the operating conditions, as specified in Section 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog						
I_{DD}	supply current	[1][2]	5	-	10	mA
		[3][4]	-	-	13	mA
$I_{off(ov)}$	overvoltage switch-off current	[5]	-	-	8.5	mA
$I_{O(sc)}$	short-circuit output current	[6]	-	-	30	mA
SENT						
I_{DD}	supply current	[1][2]	5	-	12	mA
		[3][4]	-	-	14	mA
$I_{DD(ripple)}$	ripple supply current	peak-to-peak value	-	1	2	mA
$I_{off(ov)}$	overvoltage switch-off current	[5]	-	-	9.5	mA
$I_{O(sc)}$	short-circuit output current	[6]	-	-	32	mA

[1] Normal operation and diagnostic mode excluding overvoltage and undervoltage within the specified operating supply voltage range.
[2] Without load current at the output.
[3] Normal operation and diagnostic mode over full voltage range up to limiting supply voltage at steady state.
[4] With minimum load resistance at the output.
[5] Diagnostic mode for a supply voltage above the overvoltage threshold voltage up to the limiting supply voltage.
[6] Supply current if the output OUT/DATA is shorted to GND or V_{DD}, respectively.

Table 42. Power-on reset

Characteristics are valid for the operating conditions, as specified in Section 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(on)}$	switch-on threshold voltage	if $V_{DD} > V_{th(on)}$, output switches on	-	4.3	4.45	V
$V_{th(off)}$	switch-off threshold voltage	if $V_{DD} < V_{th(off)}$, output switches off	3.9	4.1	-	V
V_{hys}	hysteresis voltage	$V_{hys} = V_{th(on)} - V_{th(off)}$	0.1	0.2	-	V
V_{POR}	power-on reset voltage	IC is initialized	-	3.3	3.6	V
$V_{th(ov)}$	overvoltage threshold voltage	if $V_{DD} > V_{th(ov)}$, output switches off	6.5	7.5	8	V
$V_{hys(ov)}$	overvoltage hysteresis voltage		0.1	0.3	-	V

Table 43. Performance

Characteristics are valid for the operating conditions, as specified in Section 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta\phi_{lin}$	linearity error	temperature range −40 °C to +180 °C [1][2][3]	−1.2	-	+1.2	deg
		temperature range −40 °C to +160 °C [1][2][3]	−1	-	+1	deg
		temperature range −40 °C to +140 °C [1][2][3]	−0.9	-	+0.9	deg
$\Delta\phi_{temp}$	temperature drift error	temperature range −40 °C to +180 °C [1][2][4][5]	-	-	0.8	deg
		temperature range −40 °C to +160 °C [1][2][4][5]	-	-	0.6	deg
		temperature range −40 °C to +140 °C [1][2][4][5]	-	-	0.5	deg
$\Delta\phi_{temp\|RT}$	temperature drift error at room temperature	temperature range −40 °C to +180 °C [2][4][6]	-	-	0.65	deg
		temperature range −40 °C to +160 °C [2][4][6]	-	-	0.6	deg
		temperature range −40 °C to +140 °C [2][4][6]	-	-	0.5	deg
$\Delta\phi_{hys}$	hysteresis error	referred to input [1][2]	-	-	0.09	deg
$\Delta\phi_{\mu lin}$	microlinearity error	referred to input [1][2]	−0.1	-	+0.1	deg
$\Delta\phi_{ang}$	angular error	temperature range −40 °C to +180 °C [1][2][3][7]	−1.35	-	+1.35	deg
		temperature range −40 °C to +160 °C [1][2][3][7]	−1.2	-	+1.2	deg
		temperature range −40 °C to +140 °C [1][2][3][7]	−1.1	-	+1.1	deg
m_{ang}	slope of angular error	[1][2][7]	-	-	0.04	deg/deg
$Z_{O(pl)}$	power-loss output impedance	impedance to remaining supply line in case of lost supply voltage or lost ground	-	-	210	Ω
Analog						
α_{res}	angle resolution	[5]	-	-	0.04	deg
α_{max}	maximum angle	programmable angular range for $V_{(CL)u} - V_{(CL)l} \geq 80\ \%V_{DD}$ [8]	6	-	180	deg
α_{ref}	reference angle	programmable zero angle [8]	0	-	180	deg
$V_{O(nom)}$	nominal output voltage	at full supply operating range	5 $\%V_{DD}$	-	95 $\%V_{DD}$	V
$V_{O(udr)}$	upper diagnostic range output voltage	[1][9][10]	96 $\%V_{DD}$	-	100 $\%V_{DD}$	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(ldr)}$	lower diagnostic range output voltage	[1][9][10]	0 $\%V_{DD}$	-	4 $\%V_{DD}$	V
$V_{(CL)u}$	upper clamping voltage	[1][10][11]	40 $\%V_{DD}$	-	95 $\%V_{DD}$	V
$V_{(CL)l}$	lower clamping voltage	[1][10][11]	5 $\%V_{DD}$	-	30.5 $\%V_{DD}$	V
$\Delta V_{(CL)}$	clamping voltage variation	deviation from programmed value [1][10]	−0.3 $\%V_{DD}$	-	+0.3 $\%V_{DD}$	V
$V_{n(o)(RMS)}$	RMS output noise voltage	equivalent power noise [1][5]	-	0.4	2.5	mV
SENT						
α_{res}	angle resolution	[12]	-	-	0.044	deg
$V_{n(o)(RMS)}$	RMS output noise voltage	equivalent power noise [13]	-	-	1	LSB
V_{OH}	HIGH-level output voltage	at 0.1 mA DC load current	4.1	-	4.7	V
V_{OL}	LOW-level output voltage	at 0.5 mA DC load current	-	-	0.5	V
$T_{sen(acc)}$	sensor temperature accuracy	[14]	−10	-	+10	°C
$T_{sen(res)}$	sensor temperature resolution	[14]	-	1	-	°C
$V_{sen(acc)}$	sensor voltage accuracy		−250	-	+250	mV
$V_{sen(res)}$	sensor voltage resolution		-	17.5	-	mV

[1] At a low-pass filtered analog output with a cut-off frequency of 0.7 kHz.

[2] Definition of errors is given in Section 15.

[3] Inhomogeneity of an 18 mm diameter disc magnet can increase the linearity error by < 0.1°.

[4] Based on a 3σ standard deviation.

[5] At a nominal output voltage between 5 $\%V_{DD}$ and 95 $\%V_{DD}$ and a maximum angle of α_{max} = 180°.

[6] Room temperature is given for an ambient temperature of 25 °C.

[7] Graph of angular error is shown in Figure 14.

[8] In steps of resolution < 0.0027°.

[9] Activation is dependent on the programmed diagnostic mode.

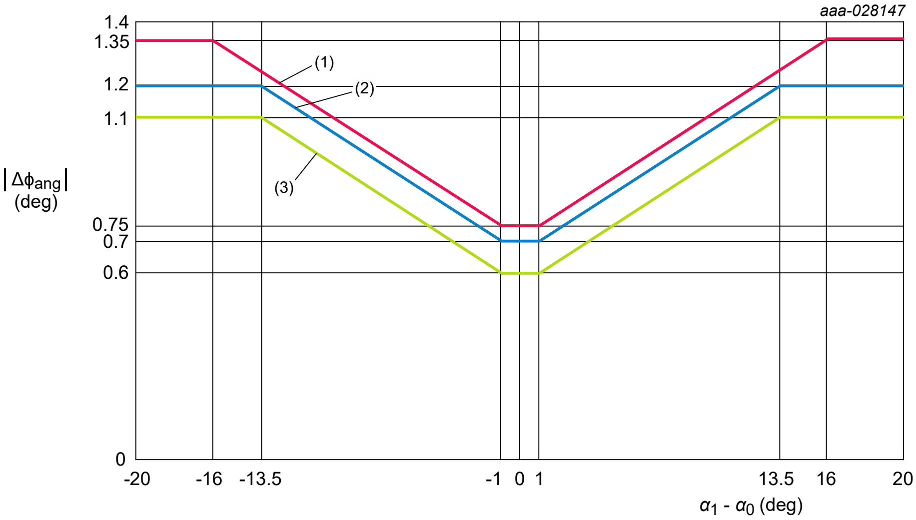
[10] Settling to these values is limited by 0.7 kHz low-pass filtering of analog output.

[11] In steps of 0.02 $\%V_{DD}$.

[12] At a maximum angle of α_{max} = 180°.

[13] Based on 12 bit.

[14] Sensor temperature refers to the on-chip temperature.



1. −40 °C to +180 °C
2. −40 °C to +160 °C
3. −40 °C to +140 °C

Figure 14. Envelope curve for the magnitude of angular error

Table 44. Dynamics

Characteristics are valid for the operating conditions, as specified in Section 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{on}	turn-on time	until first valid result	-	-	1	ms
f_{upd}	update frequency		5.5125	6.25	-	kHz
t_s	settling time	after an ideal mechanical angle step of 45°, until 90 % of the final value is reached [1]	250	400	500	µs
FTTI	fault tolerant time interval	time until the device will go into safe state after internal error occurs [2]	-	-	5	ms
$t_{cmd(ent)}$	enter command mode time	after power-on	20	-	30	ms
$t_{rec(ov)}$	overvoltage recovery time	after overvoltage	-	-	1	ms
SENT						
f_{upd}	update frequency	[3]	1.2	-	2.2	kHz
T_{clk}	clock period	SENT clock tick time = 2.7 µs [4]	2.4	2.67	3	µs
		SENT clock tick time = 3 µs	2.7	3	3.3	µs
		SENT clock tick time = 4.5 µs	3.6	4.5	5.4	µs
		SENT clock tick time = 6 µs	4.8	6	7.2	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{jit}	jitter time	variation of maximum nibble time (6σ) compared to the expected time derived from the calibration pulse				
		T_{clk} = 2.7 μs	-	-	0.09	μs
		T_{clk} = 3 μs	-	-	0.1	μs
		T_{clk} = 4.5 μs	-	-	0.15	μs
		T_{clk} = 6 μs	-	-	0.2	μs
t_f	fall time	from 3.8 V to 1.1 V output level				
		slope time: 00b; T_{clk} = 2.7 μs	4.1	5.3	6.5	μs
		slope time: 01b; T_{clk} = 3 μs	4.1	5.3	6.5	μs
		slope time: 10b; T_{clk} = 4.5 μs	6.1	7.1	9.75	μs
		slope time: 11b; T_{clk} = 6 μs	8.2	10.7	13	μs
t_r	rise time	from 1.1 V to 3.8 V output level				
		slope time: 00b; T_{clk} = 2.7 μs	5.2	7.1	8.7	μs
		slope time: 01b; T_{clk} = 3 μs	5.2	7.1	8.7	μs
		slope time: 10b; T_{clk} = 4.5 μs	10.3	14.2	17.4	μs
		slope time: 11b; T_{clk} = 6 μs	15.5	21.3	26.1	μs
t_{stab}	stabilization time	output level below 1.39 V (LOW) or above 3.8 V (HIGH)				
		T_{clk} = 2.7 μs	6	-	-	μs
		T_{clk} = 3 μs	6	-	-	μs
		T_{clk} = 4.5 μs	9	-	-	μs
		T_{clk} = 6 μs	12	-	-	μs

[1] The mechanical angle step is not synchronized with the SENT frame. Thus the worst case settling time is extended with the length of a complete SENT frame.

[2] Refers to analog output; additional information including times for digital output is provided in the safety manual.

[3] SENT update rate at T_{clk} = 3 μs, 6 DATA nibbles, and no PAUSE pulse.

[4] 12 bit fast mode.

Table 45. Digital interface

Characteristics are valid for the operating conditions, as specified in Section 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		80 $\%V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	20 $\%V_{DD}$	V
V_{OH}	HIGH-level output voltage	I_O = 2 mA	80 $\%V_{DD}$	-	-	V
V_{OL}	LOW-level output voltage	I_O = 2 mA	-	-	20 $\%V_{DD}$	V
I_{od}	overdrive current	absolute value for overdriving the output buffer	-	-	20	mA
t_{start}	start time	LOW level before rising edge [1]	5	-	-	µs
t_{stop}	stop time	HIGH level before falling edge	5	-	-	µs
T_{bit}	bit period	the load capacitance limits the minimum period	10	-	100	µs
ΔT_{bit}	bit period deviation	deviation between received clock and sent clock	$0.8T_{bit}$	$1T_{bit}$	$1.2T_{bit}$	µs
t_{w0}	pulse width 0		$0.175T_{bit}$	$0.25T_{bit}$	$0.375T_{bit}$	µs
t_{w1}	pulse width 1		$0.625T_{bit}$	$0.75T_{bit}$	$0.825T_{bit}$	µs
t_{to}	time-out time	communication reset guaranteed after maximum t_{to}	250	-	-	µs
$t_{tko(slv)}$	slave takeover time	duration of LOW level for slave takeover	1	-	5	µs
$t_{tko(mas)}$	master takeover time	duration of LOW level for master takeover	$0T_{bit}$	-	$0.5T_{bit}$	µs
t_{prog}	programming time	for a single memory address	20	-	-	ms

[1] In SENT mode, the OUT/DATA pin must be kept HIGH for at least t_{to} before sending the initial command sequence to enter the command mode.

Table 46. Internal capacitances

Characteristics are valid for the operating conditions, as specified in Section 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{block}	blocking capacitance	[1][2]	100	200	300	nF
C_L	load capacitance	[1]	1.1	2.2	3.3	nF

[1] Measured at 1 MHz.

[2] Total capacitance between V_{DD} and GND.

15 Definition of errors

15.1 General

Angular measurement errors by the device result from linearity errors, temperature drift errors, and hysteresis errors. Figure 15 shows the output signal of an ideal sensor, where the measured angle ϕ_{meas} corresponds ideally to the magnetic field angle α. This curve represents the angle reference line $\phi_{ref}(\alpha)$ with a slope of 0.5 $\%V_{DD}$/degree and 22.75 LSB/degree for SENT mode respectively.

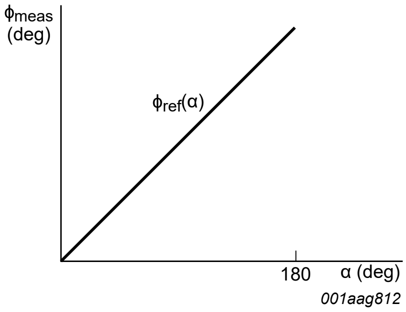


Figure 15. Definition of the reference line

The angular range is set to α_{max} = 180° and the clamping voltages are programmed to $V_{(CL)l}$ = 5 $\%V_{DD}$ and $V_{(CL)u}$ = 95 $\%V_{DD}$ for a valid definition of errors.

15.2 Hysteresis error

The device output performs a positive (clockwise) rotation and negative (counter clockwise) rotation over an angular range of 180° at a constant temperature.
The maximum difference between the angles defines the hysteresis error $\Delta\phi_{hys}$.

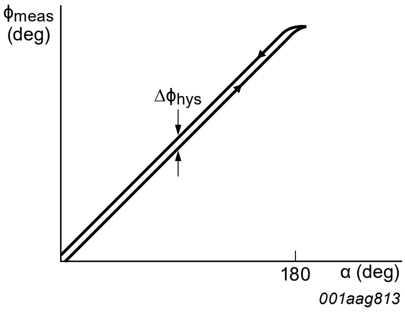


Figure 16. Definition of the hysteresis error

Equation (1) gives the mathematical description for the hysteresis value $\Delta\phi_{hys}$:

$$\Delta\phi_{hys}(\alpha) = |\phi_{meas}(\alpha \to 180°) - \phi_{meas}(\alpha \to 0°)| \qquad (1)$$

15.3 Linearity error

The device output signal deviation from a best straight line $\Delta\phi_{BSL}$, with the same slope as the reference line, is defined as linearity error. The magnetic field angle is varied at fixed temperatures for measurement of this linearity error. The output signals deviation from the best straight line at the given temperature is the linearity error $\Delta\phi_{lin}$. It is a function of the magnetic field angle α and the temperature of the device T_{amb}.

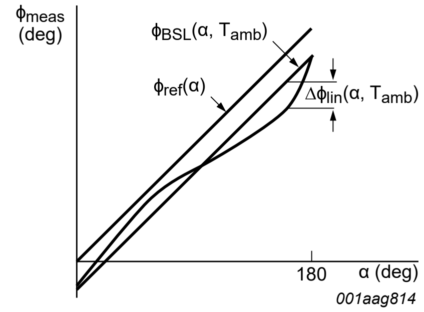


Figure 17. Definition of the linearity error

15.4 Microlinearity error

α is the magnetic field angle. If Δα = 1°, the microlinearity error $\Delta\phi_{lin}$ is the device output deviation from 1°.

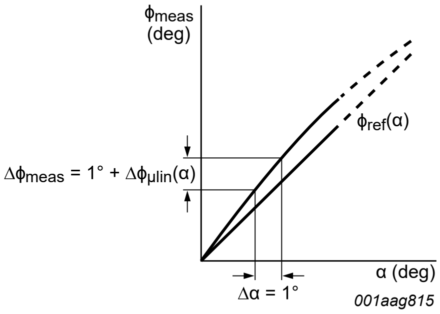


Figure 18. Definition of the microlinearity error

15.5 Temperature drift error

The temperature drift $\Delta\phi_{temp}$ is defined as the envelope over the deviation of the angle versus the temperature range. It is considered as the pure thermal effect.

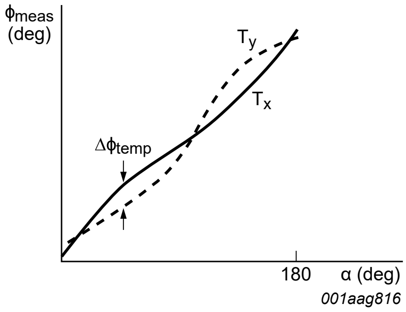


Figure 19. Definition of the temperature drift error

Equation (2) gives the mathematical description for temperature drift value $\Delta\phi_{temp}$:

$$\Delta\phi_{temp}(\alpha) = |\phi_{meas}(\alpha, T_x) - \phi_{meas}(\alpha, T_y)| \tag{2}$$

With:

T_x: temperature for maximum ϕ_{meas} at angle α

T_y: temperature for minimum ϕ_{meas} at angle α

The deviation from the value at room temperature $\Delta\phi_{temp|RT}$ describes the temperature drift of the angle, compared to the value, which the sensor provides at room temperature:

$$\Delta\phi_{temp|RT}(\alpha, T_{amb}) = |\phi_{meas}(\alpha, T_{amb}) - \phi_{meas}(\alpha, T_{RT})| \tag{3}$$

With:

T_{RT}: room temperature (25 °C)

15.6 Angular error

The angular error $\Delta\phi_{ang}$ is the difference between mechanical angle and sensor output during a movement from α_0 to α_1. Here α_0 and α_1 are arbitrary angles within the angular range. The customer initially programs the angle measurement at α_0 at room temperature and zero hour upon production. The angle measurement at α_1 is made at any temperature within the ambient temperature range:

$$\Delta\phi_{ang} = (\phi_{meas}(\alpha_1, T_{amb}) - \phi_{meas}(\alpha_0, T_{RT})) - (\alpha_1 - \alpha_0) \tag{4}$$

With:

α_0, α_1: arbitrary mechanical angles within the angular range

$\phi_{meas}(\alpha_0, T_{RT})$: programmed angle at α_0, T_{RT} = 25 °C and zero hour upon production

$\phi_{meas}(\alpha_1, T_{amb})$: the sensor measures angle at α_1 and any temperature within T_{amb}

This error comprises non-linearity and temperature drift related to the room temperature.

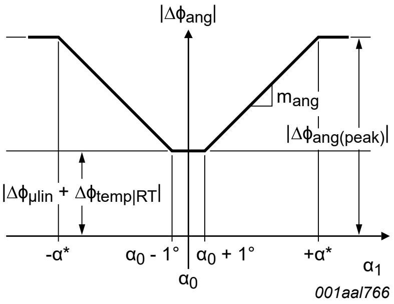


Figure 20. Envelope curve for the magnitude of angular error

Figure 20 shows the envelope curve for the magnitude of angular error $|\Delta\phi_{ang}|$ versus α_1 for all angles α_0 and all temperatures T_{amb} within the ambient temperature range. If α_1 is in the range of ±1° around α_0, $|\Delta\phi_{ang}|$ has its minimum. Here only the microlinearity error $\Delta\phi_{\mu lin}$ and the temperature drift related to the room temperature $|\Delta\phi_{temp|RT}|$ occurs. If α_1 deviates from α_0 by more than 1° in either direction, $|\Delta\phi_{ang}|$ can increase. Slope m_{ang} defines the gradient.

Equation (5) to Equation (8), express the angular error:

For $|\alpha_1 - \alpha_0| \leq 1°$

$$|\Delta\phi_{ang}| = |\Delta\phi_{\mu lin} + \Delta\phi_{temp|RT}| \tag{5}$$

For $1° < |\alpha_1 - \alpha_0| < \alpha^*$

$$|\Delta\phi_{ang}| = |\Delta\phi_{\mu lin} + \Delta\phi_{temp|RT}| + m_{ang} \times (|\alpha_1 - \alpha_0| - 1°) \tag{6}$$

For $|\alpha_1 - \alpha_0| \geq \alpha^*$

$$|\Delta\phi_{ang}| = \sqrt{(\Delta\phi_{lin})^2 + (\Delta\phi_{temp|RT})^2} \tag{7}$$

With:

$$\alpha^* = \frac{|\Delta\phi_{ang(peak)}| - |\Delta\phi_{\mu lin} + \Delta\phi_{temp|RT}|}{m_{ang}} + \alpha_0 + 1° \tag{8}$$

16 Programming

16.1 General description

The device provides an OWI to enable programming of the device which uses pin OUT/DATA bidirectionally.

In general the device runs in analog or SENT mode, the normal operation mode. The embedded programming data configures this mode. After a power-on reset once time t_{on} has elapsed, it starts. In this mode, the magnetic field angle is converted into the corresponding output voltage.

A second mode, the command mode enables programming. In this mode, the customer can adjust all required parameters (for example zero angle and angular range) to meet the application requirements. Data is stored in the non-volatile memory. After changing the contents of the memory, recalculate and write the checksum (see Section 16.4).

In order to enter the command mode keep pin OUT/DATA HIGH for at least t_{to} and send a specific command sequence after a power-on reset and during the time slot $t_{cmd(ent)}$. The external source used to send the command sequence must overdrive the output buffer of the device. In doing so, it provides current I_{od}.

During communication, the KMA310 is always the slave and the external programming hardware is always the master. Figure 21 illustrates the structure of the OWI data format.

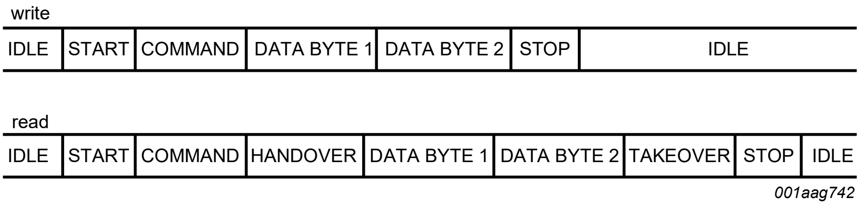


Figure 21. OWI data format

The master provides the start condition, which is a rising edge after a LOW level. Then a command byte which can be either a read or a write command is sent. Depending on the command, the master or the slave has to send the data immediately after the command sequence. If there is a read command, an additional handover or takeover bit is inserted before and after the data bytes. The master must close each communication with a stop condition. If the slave does not receive a rising edge for a time longer than t_{to}, a timeout condition occurs. The bus is reset to the idle state and waits for a start condition and a new command. This behavior can be used to synchronize the device regardless of the previous state.

All communication is based on this structure (see Figure 21), even for entering the command mode. The customer can access the non-volatile memory, CTRL1, and SIGNATURE registers (described in Section 16.5). Only a power-on reset leaves the command mode. A more detailed description of the programming is given in the next sections.

16.2 Timing characteristics

As described in the previous section, a start and stop condition is necessary for communication. The LOW-level duration before the rising edge of the start condition

]

is defined as t_{start}. The HIGH-level duration after the rising edge of the stop condition is defined as t_{stop}. These parameters, together with all other timing characteristics are shown in Table 45.

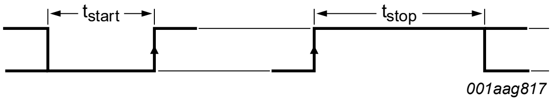


Figure 22. OWI start and stop condition

Figure 23 shows the coding of a single bit with a HIGH level of V_{IH} and a LOW level of V_{IL}. Here the pulse width t_{w1} or t_{w0} represents a logic 1 or a logic 0 of a full bit period T_{bit}, respectively.

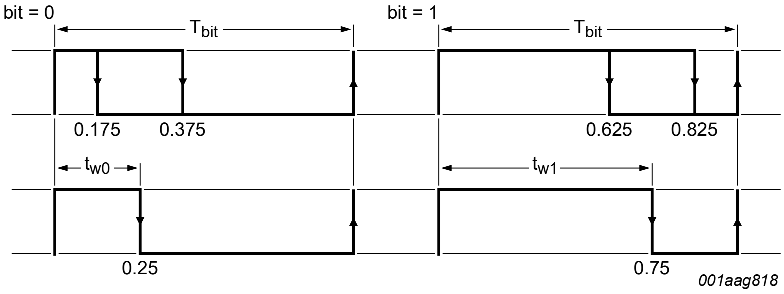


Figure 23. OWI timing

16.3 Sending and receiving data

The master has to control the communication during sending or receiving data. The command byte defines the address and type of command the master requests. Read commands need an additional handover or takeover bit. Insert this bit before and after the two data bytes (see Figure 21). However, the OWI is a serial data transmission, whereas the MSB is sent at first.

Table 47. Format of command byte

7	6	5	4	3	2	1	0
CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

Table 48. Command byte description

Bit	Symbol	Description
7 to 1	CMD[7:1]	address bits
0	CMD0	0 = write
		1 = read

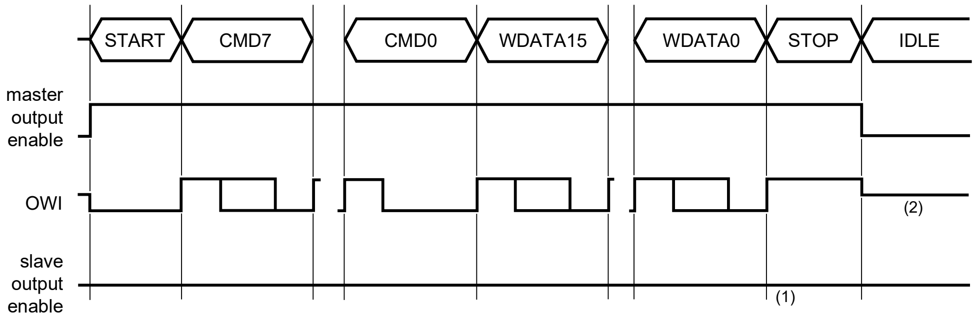
A more detailed description of all customer accessible registers is given in Section 16.5. Both default value and the complete command including the address and write or read request are also listed.

16.3.1 Write access

To write data to the non-volatile memory, perform the following procedure for write access:

1. Start condition: The master drives a rising edge after a LOW level
2. Command: The master sends a write command (CMD0 = 0)
3. Data: The master sends two data bytes
4. Stop condition: The master drives a rising edge after a LOW level

Figure 24 shows the write access of the digital interface. The signal OWI represents the data on the bus from the master or slave. The signals: master output enable and slave output enable indicate when the master or the slave output is enabled or disabled, respectively.



1. Missing rising edges generate a timeout condition and the written data is ignored.
2. If the master does not drive the bus, the bus-pull defines the bus.

Figure 24. OWI write access

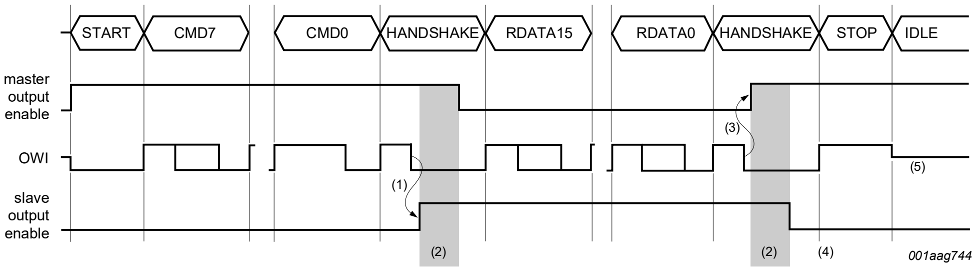
Note: As already mentioned in Section 16.1, use the write procedure to enter the command mode. If command mode is not entered, communication is not possible and the sensor operates in normal operation mode. After changing an address, the time t_{prog} must elapse before changing another address. After changing the contents of the non-volatile memory, recalculate and write the checksum (see Section 16.4).

16.3.2 Read access

To read data from the sensor, perform the following procedure:

1. Start condition: The master drives a rising edge after a LOW level
2. Command: The master sends a read command (CMD0 = 1)
3. Handover: The master sends a handover bit that is a logic 0 and disables the output after a three-quarter bit period
4. Takeover: The slave drives a LOW level after the falling edge for $t_{tko(slv)}$
5. Data: The slave sends two data bytes
6. Handover: The slave sends a handover bit that is a logic 0 and disables the output after a three-quarter bit period
7. Takeover: The master drives a LOW level after the falling edge for $t_{tko(mas)}$
8. Stop condition: The master drives a rising edge after a LOW level

Figure 25 shows the read access of the digital interface. The signal OWI represents the data on the bus from the master or slave. The signals: master output enable and slave output enable indicate when the master or the slave output is enabled or disabled, respectively.



1. Duration of LOW level for slave takeover $t_{tko(slv)}$.
2. The master output enable and the slave output enable overlap, because both drive a LOW level. However this behavior ensures the independency from having a pull-up or pull-down on the bus. In addition, it improves the EMC robustness, because all levels are actively driven.
3. Duration of LOW level for master takeover $t_{tko(mas)}$.
4. If the master does not take over, the pull-up generates the stop condition. Otherwise a timeout is generated if there is a pull-down and the slave waits for a rising edge as start condition.
5. If the master does not drive the bus, the bus-pull defines the bus.

Figure 25. OWI read access

16.3.3 Entering the command mode

After a power-on reset, the sensor provides a time slot $t_{cmd(ent)}$ for entering the command mode. Send a specific command sequence (see Figure 26). If command mode is not entered, the sensor starts in the normal operation mode. If the sensor stays in the diagnostic mode, the master can write the signature without a power-on reset.

During the command mode sequence, the output is enabled. The external programming hardware has to overdrive the output with current I_{od}. If command mode is activated, the output is disabled and pin OUT/DATA operates as a digital interface.

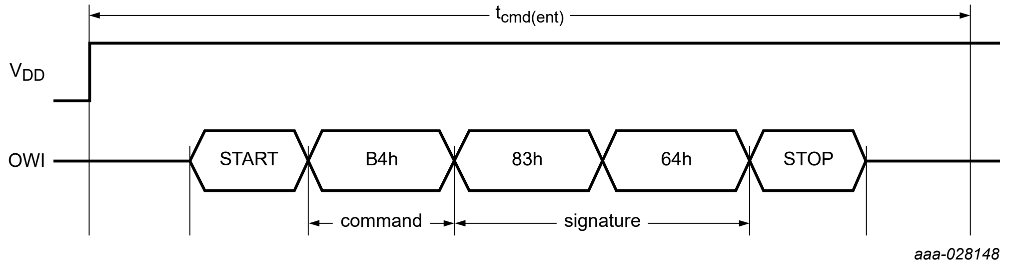


Figure 26. OWI command mode procedure

16.4 Cyclic redundancy check

As mentioned in Section 10.1, there is an individual 8-bit checksum for each non-volatile memory area. Bit 8 of the CTRL1 register indicates a checksum error of customer area 1, 2 or 3 as well as the manufacturer area of the NVM including the traceability registers. Generate the CRC with the MSB of the data word first over all corresponding addresses in increasing order for the corresponding memory area, to calculate the checksums.

Read out all registers of the non-volatile memory area for calculating the checksum. The LSB contains the previous checksum and must be overwritten with 0h before the calculation can be started.

The generator polynomial for the calculation of the checksum is:

$$G(x) = x^8 + x^2 + x + 1 \quad (9)$$

With a seed value of AAh and the data bits are XOR at the x^8 point.

16.4.1 Software example in C++

```
#include "stdafx.h"
#include "conio.h"
unsigned int calculate_crc(unsigned int crc, unsigned int
 data_word)
{
const unsigned int gpoly = 0x107;   // generator polynomial
for (int i = 15; i >= 0; i--)
{
crc <<= 1;
crc |= (int) ((data_word & (1u<<i))>>i);
if (crc & 0x0100) crc ^= gpoly;
}
return crc;
}
int main(void)
{
unsigned int crc;
// data sequence of customer area 1
unsigned int data_word[] = {0x0000, 0x0100, 0x1300, 0x1000,
 0x1FFE, 0xFFFF, 0x1200, 0x0000, 0x0099, 0x0F89, 0x80FA,
 0x00BE};
// seed value
crc = 0xAA;
printf("Seed value\n0x%02X\n\n", crc);
// number of registers
unsigned int N = sizeof(data_word)/sizeof(unsigned int);
// 8 LSBs are reserved for checksum and must be filled with 0
data_word[N - 1] = data_word[N - 1] & 0xFF00;
// calculate checksum over all addresses
printf("Address\t\tValue\n");
for (unsigned int i = 0; i <= N - 1; i++)
{
printf("0x%02X\t\t0x%04X\n", i, data_word[i]);
crc = calculate_crc(crc, data_word[i]);
}
printf("\nChecksum for customer area 1\n0x%02X", crc);
_getch();
return 0;
}
```

The checksum of this data sequence is B3h.

16.5 Registers

16.5.1 Signatures

The command mode can be entered with different signatures with different access rights to the non-volatile memory regions. Table 49 shows the level of access for the different regions of the non-volatile memory depending on the signature used.

Table 49. Signatures

Signature	Value	Command registers	Customer area 1	Customer area 2	Customer area 3	Traceability register
A (OEM)	7253h	R/W	-/-	-/-	R/W	-/-
B (tier 1)	8364h	R/W	R/W	R/W	R/W	R/-

16.5.2 Command registers

To enter the command mode, write the signature given in Table 49 into the specific register using the OWI. Do this procedure as described in Section 16.3.3, with a write command, the signature follows it, but after a power-on reset and not later than $t_{cmd(ent)}$.

Table 50. Command registers

Command write/read	Register	Bit	Access	Description
B0h/B1h	CTRL1	15	R	diagnostic error detected
		14	R	diagnostic error detected in data path
		13	R/W	force diagnostic mode off (no signaling) 0b – enable 1b – disable
		12	R	low voltage detected
		11	R	high voltage detected
		10	R	single-bit error of non-volatile memory detected and corrected
		9	R	double-bit error of non-volatile memory detected
		8	R	checksum error of customer area 1, 2 or 3 detected
		7	R	oscillator frequency out of range detected
		6	R	voltage above programmed threshold detected
		5	R	voltage below programmed threshold detected
		4	R	temperature above programmed threshold detected
		3	W	undefined[1]
		2	R	command mode signature A (OEM) detected
		1	R	command mode signature B (tier 1) detected
		0	R	reserved

Command write/read	Register	Bit	Access	Description
B2h/B3h	ASIL_FLAGS	15 to 13	R	type number 000b – KMA310 001b – KMA320 010b – KMA321 011b – reserved 100b – reserved 101b – reserved 110b – KMZ80 111b – reserved
		12	R/W	reserved
		11	R	BIST completion check (SM-07)
		10	R	angular range check (SM-12)
		9	R	CORDIC range check (SM-11)
		8	R	SD-ADC range check (SM-09)
		7	R	BIST encoding check (SM-08)
		6	R	data adder check (SM-10)
		5	R	control signal check (SM-06)
		4	R	adjusted angle calculation check (SM-05)
		3	R	data conversion check (SM-04)
		2	R	data division check (SM-03)
		1	R	inverted angle calculation check (SM-02)
		0	R	magnetic field conversion check (SM-01)
B4h/B5h	SIGNATURE	15 to 0	W	write signature to enter command mode; see Section 16.3.3

[1] Undefined: write as zero for default, returns any value when read.

16.5.3 Non-volatile memory registers

The device includes several internal registers which are used for customization and identification.

The initial signature allows read access to all areas but only write access to customer registers. Write accesses to reserved areas are ignored. Since these registers are implemented as non-volatile memory cells, writing to the registers needs a specific time t_{prog} after each write access to complete.

As there is no check for the programming time, make sure that no other accesses to the non-volatile memory are made during the programming cycle. Do not address the non-volatile memory during the time t_{prog}.

Note: To calculate the corresponding checksum, read out all register addresses.

Table 51. Customer area 1

Command write/read	Register	Bit	Description	Default MSB/LSB
00h/01h	ZERO_ANGLE	15 to 0	mechanical zero degree position; see Table 55	00h/00h

Command write/read	Register	Bit	Description	Default MSB/LSB
02h/03h	CLAMP_LOW	15 to 13	undefined[1]	01h/00h
		12 to 0	lower clamping level; see Table 56	
04h/05h	CLAMP_HIGH	15 to 13	undefined[1]	13h/00h
		12 to 0	upper clamping level; see Table 57	
06h/07h	SCALE_COEFFICIENT	15 to 0	scale coefficient LSB; see Table 58	10h/00h
08h/09h	CLAMP_SWITCH	15 to 13	undefined[1]	1Fh/FEh
		12 to 1	clamp switch angle; see Table 59	
		0	scale coefficient MSB; see Table 59	
0Ah/0Bh	RANGE_DETECTION	15 to 0	range detection angle; see Table 60	FFh/FFh
0Ch/0Dh	CLAMP_RANGE	15 to 13	undefined[1]	12h/00h
		12 to 0	clamp range; see Table 61	
0Eh/0Fh	SYS_SETTING	15 and 14	undefined[1]	00h/00h
		13	reserved[2]	
		12	output mode 0b – analog (default) 1b – SENT	
		11	reserved[2]	
		10	self-diagnostic validation support[3]	
		9 to 6	undefined[1]	
		5	reserved[2]	
		4 and 3	MPC type 00b – MPC17 (default) 01b – MPC7 10b – no MPC 11b – undefined	
		2 and 1	diagnostic mode 00b – active LOW (default) 01b – active HIGH 1Xb – reserved	
		0	slope; slope of output curve 0b – rising (default) 1b – falling	

Command write/read	Register	Bit	Description	Default MSB/LSB
10h/11h	SENT_SETTING1	15 to 12	sensor type; see Table 62	00h/99h
		11	CRC type 0b – recommended (default) 1b – legacy	
		10	PAUSE pulse enable[3] the frame length depends on the protocol format; see Section 8.5	
		9	frame length[3] constant frame length of 297 clock ticks for all protocol formats	
		8	ESP[3]	
		7 to 5	set protocol format; see Table 63	
		4 and 3	SENT revision 00b – not specified 01b – FEB20008 rev 2 10b – JAN2010 rev 3 11b – APR2016 rev 4 (default)	
		2	sensor ID 0b – sensor ID1 (default) 1b – sensor ID2	
		1 and 0	clock tick time 00b – 2.7 μs 01b – 3 μs (default) 10b – 4.5 μs 11b – 6 μs	

Command write/read	Register	Bit	Description	Default MSB/LSB
12h/13h	SENT_SETTING2	15 and 14	upper voltage threshold 00b – off (default) 01b – 5.25 V 10b – 5.50 V 11b – 5.75 V	0Fh/89h
		13 and 12	lower voltage threshold 00b – off (default) 01b – 4.75 V 10b – 4.50 V 11b – 4.25 V	
		11 to 7	temperature threshold; see Table 64	
		6	temperature warning[3]	
		5	single-bit error and CRC2 warning[3]	
		4	supply monitor warning[3]	
		3 and 2	mask STATUS nibble bit 0 and bit 1 00b – STATUS nibble bit 0 and bit 1 enabled 01b – STATUS nibble bit 1 enabled bit 0 disabled 10b – STATUS nibble bit 1 disabled bit 0 enabled (default) 11b – STATUS nibble bit 0 and bit 1 disabled	
		1 and 0	slope time 00b – for T_{clk} = 2.7 μs 01b – for T_{clk} = 3 μs (default) 10b – for T_{clk} = 4.5 μs 11b – for T_{clk} = 6 μs	
14h/15h	ASIL_SETTING	15	BIST[4]	80h/FAh
		14	mask angular range check (SM-12)[3]	
		13	mask CORDIC range check (SM-11)[3]	
		12	mask SD-ADC range check (SM-09)[3]	
		11	mask BIST encoding check (SM-08)[3]	
		10	mask BIST completion check (SM-07)[3]	
		9	mask data adder check (SM-10)[3]	
		8	mask control signal check (SM-06)[3]	
		7	adjusted angle calculation check (SM-05)[4]	
		6	data conversion check (SM-04)[4]	
		5	data division check (SM-03)[4]	
		4	inverted angle calculation check (SM-02)[4]	
		3	magnetic field conversion check (SM-01)[4]	
		2 to 0	reserved; write as 010b	
16h/17h	CRC1	15 to 8	undefined[1]	00h/B3h
		7 to 0	CRC for customer area 1; see Section 16.4	

[1] Undefined: write as zero for default, returns any value when read.
[2] Reserved: write as zero for default.
[3] Bit allocation: 0b – disabled (default); 1b – enabled.
[4] Bit allocation: 0b – disabled; 1b – enabled (default).

Table 52. Customer area 2

Command write/read	Register	Bit	Description	Default MSB/LSB
20h/21h	MPC_COEFFICIENT1	15 to 0	MPC coefficient 1 or linear X1	08h/00h
22h/23h	MPC_COEFFICIENT2	15 to 0	MPC coefficient 2 or linear X2	10h/00h
24h/25h	MPC_COEFFICIENT3	15 to 0	MPC coefficient 3 or linear X3	18h/00h
26h/27h	MPC_COEFFICIENT4	15 to 0	MPC coefficient 4 or linear X4	20h/00h
28h/29h	MPC_COEFFICIENT5	15 to 0	MPC coefficient 5 or linear X5	28h/00h
2Ah/2Bh	MPC_COEFFICIENT6	15 to 0	MPC coefficient 6 or linear Y1	30h/00h
2Ch/2Dh	MPC_COEFFICIENT7	15 to 0	MPC coefficient 7 or linear Y2	38h/00h
2Eh/2Fh	MPC_COEFFICIENT8	15 to 0	MPC coefficient 8 or linear Y3	40h/00h
30h/31h	MPC_COEFFICIENT9	15 to 0	MPC coefficient 9 or linear Y4	48h/00h
32h/33h	MPC_COEFFICIENT10	15 to 0	MPC coefficient 10 or linear Y5	50h/00h
34h/35h	MPC_COEFFICIENT11	15 to 0	MPC coefficient 11 or linear S1	58h/00h
36h/37h	MPC_COEFFICIENT12	15 to 0	MPC coefficient 12 or linear S2	60h/00h
38h/39h	MPC_COEFFICIENT13	15 to 0	MPC coefficient 13 or linear S3	68h/00h
3Ah/3Bh	MPC_COEFFICIENT14	15 to 0	MPC coefficient 14 or linear S4	70h/00h
3Ch/3Dh	MPC_COEFFICIENT15	15 to 0	MPC coefficient 15 or linear S5	78h/00h
3Eh/3Fh	MPC_COEFFICIENT16	15 to 0	MPC coefficient 16 or linear S6	80h/00h
40h/41h	CRC2	15	LOCK1; irreversible write protection of customer area 1 and customer area 2 1b – enabled	00h/8Ch
		14 to 8	undefined[1]	
		7 to 0	CRC for customer area 2; see Section 16.4	

[1] Undefined: write as zero for default, returns any value when read.

Table 53. Customer area 3

Command write/read	Register	Bit	Description	Default MSB/LSB
50h/51h	OOR_ LOW	15 to 12	undefined[1]	00h/00h
		11 to 0	lower OOR threshold	
52h/53h	OOR_HIGH	15 to 12	undefined[1]	0Fh/FFh
		11 to 0	upper OOR threshold	
54h/55h	OEM_CODE1	15 to 12	OEM code 7 bits 11 to 8	00h/00h
		11 to 0	OEM code 1	

Command write/read	Register	Bit	Description	Default MSB/LSB
56h/57h	OEM_CODE2	15 to 12	OEM code 7 bits 7 to 4	00h/00h
		11 to 0	OEM code 2	
58h/59h	OEM_CODE3	15 to 12	OEM code 7 bits 3 to 0	00h/00h
		11 to 0	OEM code 3	
5Ah/5Bh	OEM_CODE4	15 to 12	OEM code 8 bits 11 to 8	00h/00h
		11 to 0	OEM code 4	
5Ch/5Dh	OEM_CODE5	15 to 12	OEM code 8 bits 7 to 4	00h/00h
		11 to 0	OEM code 5	
5Eh/5Fh	OEM_CODE6	15 to 12	OEM code 8 bits 3 to 0	00h/00h
		11 to 0	OEM code 6	
60h/61h	CRC3	15	LOCK2; irreversible write protection of customer area 3 1b – enabled	00h/B2h
		14 to 8	undefined[1]	
		7 to 0	CRC for customer area 3; see Section 16.4	

[1] Undefined: write as zero for default, returns any value when read.

Table 54. Traceability register

Command write/read	Register	Bit	Access	Description
A0h/A1h	IDENTIFIER1	15 to 0	R	5 × 16 bit unique device identifier code for traceability located in manufacturer area of NVM
A2h/A3h	IDENTIFIER2	15 to 0	R	
A4h/A5h	IDENTIFIER3	15 to 0	R	
A6h/A7h	IDENTIFIER4	15 to 0	R	
A8h/A9h	IDENTIFIER5	15 to 0	R	

Table 55. ZERO_ANGLE – mechanical zero degree position bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

$$\mathrm{ZERO\_ANGLE} = \frac{180^\circ - \text{mechanical zero degree position}}{180^\circ} \times 2^{16} \qquad (10)$$

Examples:

- Mechanical zero degree position 0° = 0000h (default)
- Mechanical zero degree position 10° = F1C7h
- Mechanical zero degree position 45° = C000h

Table 56. CLAMP_LOW – lower clamping level bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	U[1]	U[1]	U[1]	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

[1] Undefined: write as zero for default; returns any value when read.

$$\text{CLAMP\_LOW} = \frac{\text{lower clamping level}}{100\ \%} \times 5120 \tag{11}$$

Values 0 to 255 are reserved. It is not permitted to use such values.

Examples:

- Lower clamping level 5 %V_{DD} = 0100h (default)
- Lower clamping level 10 %V_{DD} = 0200h
- SENT A.3 format lower clamping level = 000h
- SENT A.1, H.1, H.3, H.4 format lower clamping level = 001h

Table 57. CLAMP_HIGH – upper clamping level bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	U[1]	U[1]	U[1]	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

[1] Undefined: write as zero for default; returns any value when read.

$$\text{CLAMP\_HIGH} = \frac{\text{upper clamping level}}{100\ \%} \times 5120 \tag{12}$$

Values 4865 to 5120 are reserved. It is not permitted to use such values.

Examples:

- Upper clamping level 90 %V_{DD} = 1200h
- Upper clamping level 95 %V_{DD} = 1300h (default)
- Upper clamping level 100 %V_{DD} = 1400h (reserved)
- SENT A.1 format upper clamping level = FFEh
- SENT A.3 format upper clamping level = FFFh
- SENT H.1, H.3, H.4 format upper clamping level = FF8h

Table 58. SCALE_COEFFICIENT – least significant bits of scale coefficient bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	2^4[1]	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}

[1] See CLAMP_SWITCH register for MSB of scale coefficient.

$$\text{SCALE\_COEFFICIENT} = \frac{180°}{\text{angular range}} \times 2^{12} \tag{13}$$

Examples:

- Angular range 30° = 6000h
- Angular range 90° = 2000h
- Angular range 180° = 1000h (default)

Table 59. CLAMP_SWITCH – clamp switch angle bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	U[1]	U[1]	U[1]	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^5[2]

[1] Undefined: write as zero for default; returns any value when read.

[2] MSB of scale coefficient.

$$\text{CLAMP\_SWITCH} = \frac{180° + \text{angular range}}{2} \times \frac{2^{12}}{180°} \tag{14}$$

Examples:

- Angular range 40° → CLAMP_SWITCH = 110° = 9C7h
- Angular range 90° → CLAMP_SWITCH = 135° = C00h
- Angular range 180° → CLAMP_SWITCH = 180° = FFFh (default)

Table 60. RANGE_DETECTION – range detection angle bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

$$\text{RANGE\_DETECTION} = \frac{\text{angular range}}{180°} \times 2^{16} \tag{15}$$

Examples:

- Angular range 30° = 2AABh
- Angular range 90° = 8000h
- Angular range 180° = 0000h (default)

Table 61. CLAMP_RANGE – clamp range bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	U[1]	U[1]	U[1]	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

[1] Undefined: write as zero for default; returns any value when read.

$$\text{CLAMP\_RANGE} = \text{CLAMP\_HIGH} - \text{CLAMP\_LOW} \tag{16}$$

Examples:

- Clamp range 80 %V_{DD} = 1000h
- Clamp range 90 %V_{DD} = 1200h (default)
- Clamp range 95 %V_{DD} = 1300h

Table 62. SENSOR_TYPE

SENSOR_TYPE	12-bit code	Definition
0000b (default)	051h[1]	acceleration pedal position 1 or acceleration pedal position 2
0001b	052h[1]	acceleration pedal position 1 or secure sensor
0010b	053h[1]	acceleration pedal position 2 (redundant signal) or secure sensor
0011b	054h[1]	throttle position 1 or throttle position 2
0100b	055h[1]	throttle position 1 or secure sensor
0101b	056h[1]	throttle position 2 (redundant signal) or secure sensor
0110b	059h[1]	angle position
0111b	05Ah[1]	angle position or secure sensor
1000b	062h[2]	angle position (high speed) H.3 protocol format
1001b	063h[2]	angle position 1 or angle position 2 H.1 protocol format
1010b	064h[2]	angle position or secure sensor H.4 protocol format
1011b	066h[2]	reserved for angle position sensors
1101b to 1111b	000h	reserved

[1] Compliant with SAE JAN2010 rev 3 only.
[2] Compliant with SAE APR2016 rev 4 only.

Table 63. PROTOCOL_FORMAT

PROTOCOL_FORMAT	Protocol	Description	SENT revision
000b	A.1	dual throttle position sensor	JAN2010 rev 3
001b	A.3	single secure sensor	JAN2010 rev 3
010b	H.1	dual throttle position sensor[1]	APR2016 rev 4
011b	H.3	high-speed 12-bit fast channel	APR2016 rev 4
100b (default)	H.4	single secure sensor[2]	APR2016 rev 4

[1] This format uses the same data mapping as the A.1 protocol but excludes the reserved diagnostic values from the data range as defined in APR2016 rev 4 specification.
[2] This format uses the same data mapping as the A.3 protocol but excludes the reserved diagnostic values from the data range as defined in APR2016 rev 4 specification.

Table 64. TEMPERATURE_THRESHOLD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	[1]		[2]		2^4	2^3	2^2	2^1	2^0	[3]	[4]	[5]	[6]		[7]	

[1] Upper voltage threshold.
[2] Lower voltage threshold.
[3] Temperature warning.
[4] Single-bit error and CRC2 warning.
[5] Supply monitor warning.
[6] Mask STATUS nibble bit 0 and bit 1.
[7] Slope time.

$$\text{TEMPERATURE\_THRESHOLD} = \frac{\text{temperature threshold} + 45\ ^{\circ}\text{C}}{8\ ^{\circ}\text{C}} \tag{17}$$

Examples:

- Temperature threshold −45 °C = 0h
- Temperature threshold 75 °C = Fh
- Temperature threshold 203 °C = 1Fh (default)

17 Electromagnetic compatibility

EMC is verified in an independent and certified test laboratory.

17.1 Emission (CISPR25)

Tests according to CISPR 25 were fulfilled.

17.1.1 Conducted radio disturbance

Test of the device according to CISPR 25, third edition (2008-03), Chapter 6.2.

Classification level: 5.

17.1.2 Radiated radio disturbance

Test of the device according to CISPR 25, third edition (2008-03), Chapter 6.4.

Classification level: 5 (without addition of 6 dB in FM band).

17.2 Radiated disturbances (ISO 11452-1 fourth edition [2015-06], ISO 11452-2, ISO 11452-4 and ISO 11452-5)

The common understanding of the requested function is that an effect is tolerated as described in Table 65 during the disturbance. The reachable values are setup-dependent and differ from the final application.

Table 65. Failure condition for radiated disturbances and electrical transient transmission

Parameter	Comment	Min	Max	Unit
Variation of output signal in analog output mode	value measured relative to the output at test start	-	±0.9 %V_{DD}	V
Variation of angular value in digital output mode	value measured relative to the output at test start	-	±1.8	deg
SENT sequence	allowed sequentially failing frames	-	2	frame
SENT transmission	allowed failing frames within 100 following frames	-	3	frame

17.2.1 Absorber lined shielded enclosure

Tests according to ISO 11452-2, second edition (2004-11), were fulfilled.

Test level: 200 V/m; extended up to 4 GHz.

State: A.

17.2.2 Bulk-current injection

Tests according to ISO 11452-4, fourth edition (2011-12), were fulfilled.

Test level: 200 mA.

State: A.

17.2.3 Strip line

Tests according to ISO 11452-5, second edition (2002-04), were fulfilled.

Test level: 200 V/m; extended up to 1 GHz.

State: A.

17.2.4 Immunity against mobile phones

Tests according to ISO 11452-2, second edition (2004-11), were fulfilled.

State: A.

Definition of global system for mobile (GSM) communications signal:

- Pulse modulation: per GSM specification (217 Hz; 12.5 % duty cycle)
- Modulation grade: ≥60 dB
- Sweep: linear 800 MHz to 3 GHz
- Antenna polarization: vertical, horizontal
- Field strength: 200 V/m during on-time [calibration in continuous wave (CW)]

In deviation of ISO 11452-2, a GSM signal instead of an AM signal was used.

17.3 Electrical transient transmission (ISO 7637-3 second edition [2007-07])

The common understanding of the requested function is that an effect is tolerated as described in Table 65 during the disturbance.

17.3.1 Capacitive coupling

Tests according to ISO 7637-3 were fulfilled.

Test level: IV (for 12 V electrical system).

Classification level: B for pulse fast a, B for pulse fast b.

17.3.2 Inductive coupling

Tests according to ISO 7637-3 were fulfilled.

Test level: IV (for 12 V electrical system).

Classification level for analog mode: A for positive and negative pulses assuming returning to output voltage level before stress of ±0.9 %V_{DD} within 1 ms otherwise B.

Classification level for digital mode: A for positive and negative pulses assuming a start of a new SENT frame within 1 ms is allowed otherwise B.

18 Electrostatic discharge

18.1 Human body model (AEC-Q100-002)

The KMA310 is protected up to 8 kV, according to the human body model at 100 pF and 1.5 kΩ. This protection is ensured at all pins and interconnects between package bodies.

Classification level: H3B.

18.2 Human metal model (ANSI/ESD SP5.6-2009)

The KMA310 is protected up to 8 kV, according to the human metal model at 150 pF and 330 Ω inside the ESD gun. This test utilizes waveforms of the IEC 61000-4-2 standard on component level. Apply the contact discharge in an unsupplied state at pins OUT/DATA and V_{DD} referred to GND which is connected directly to the ground plane.

Test setup: A.

Test level: 5.

18.3 Machine model (AEC-Q100-003 legacy)

The KMA310 is protected up to 400 V, according to the machine model. This protection is ensured at all pins and interconnects between package bodies.

Classification level: M4.

All pins of KMA310 have latch-up protection.

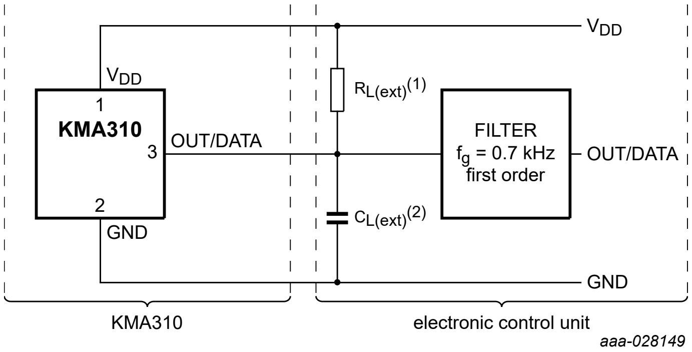
18.4 Charged-device model (AEC-Q100-011)

The KMA310 is protected up to 750 V, according to the charged-device model. This protection is ensured at all pins and interconnects between package bodies.

Classification level: C4.

19 Application information

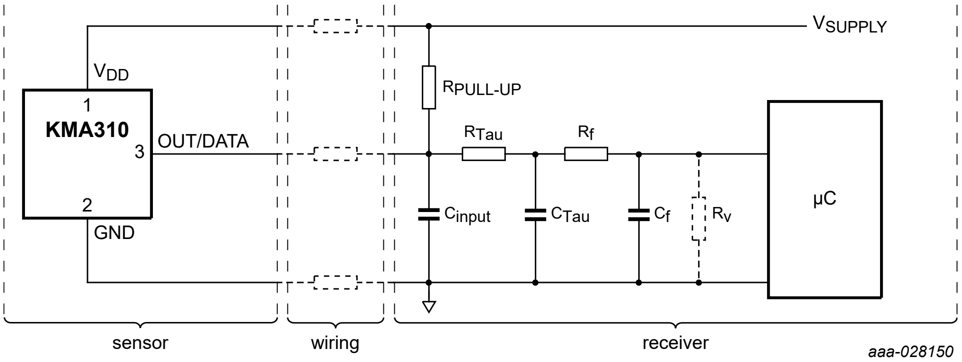
19.1 Analog output



1. Power-loss detection is only possible with a load resistance within the specified range connected to supply or ground line.
2. The load capacitance between ground and output can be used to improve the electromagnetic immunity of the device. A blocking capacitance to suppress noise on the supply line of the device is integrated into the package and thus not required externally.

Figure 27. Application information for analog output of KMA310

19.2 Digital output



KMA310 with receiver load according to figure 6.3.2-2 (recommended SENT system interface circuit topology J2716) of SAE J2716 APR2016 SENT without additional external components near KMA310

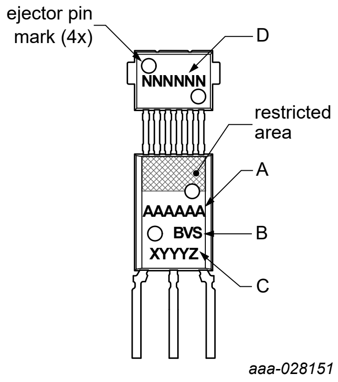
Figure 28. Application information for digital output of KMA310

20 Test information

20.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits, and is suitable for use in automotive applications.

21 Marking



A: leading letters of product name

B: additional marking

- B: burn-in information (0: without burn-in; 1: with burn-in)
- V: IC version
- S: development status (X: development; C: validated; blank: released)

C: manufacturing and date code

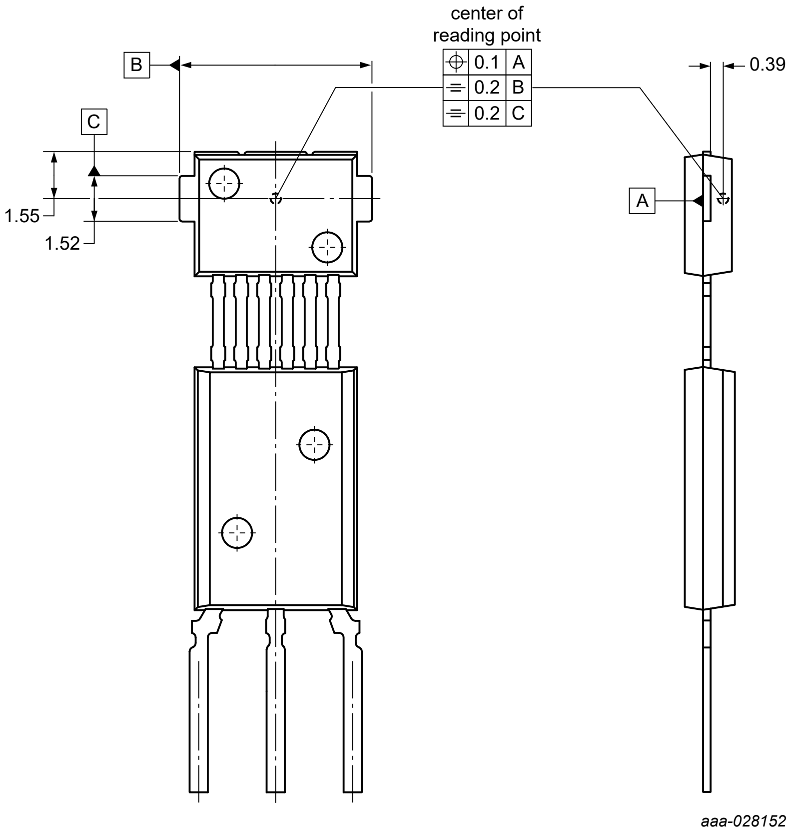
- X: manufacturing code; (m: Manila)
- YYY: day of year
- Z: year of production (last figure)

D: batch number

Figure 29. Marking

22 Package information

22.1 Reading point position



Dimensions in mm

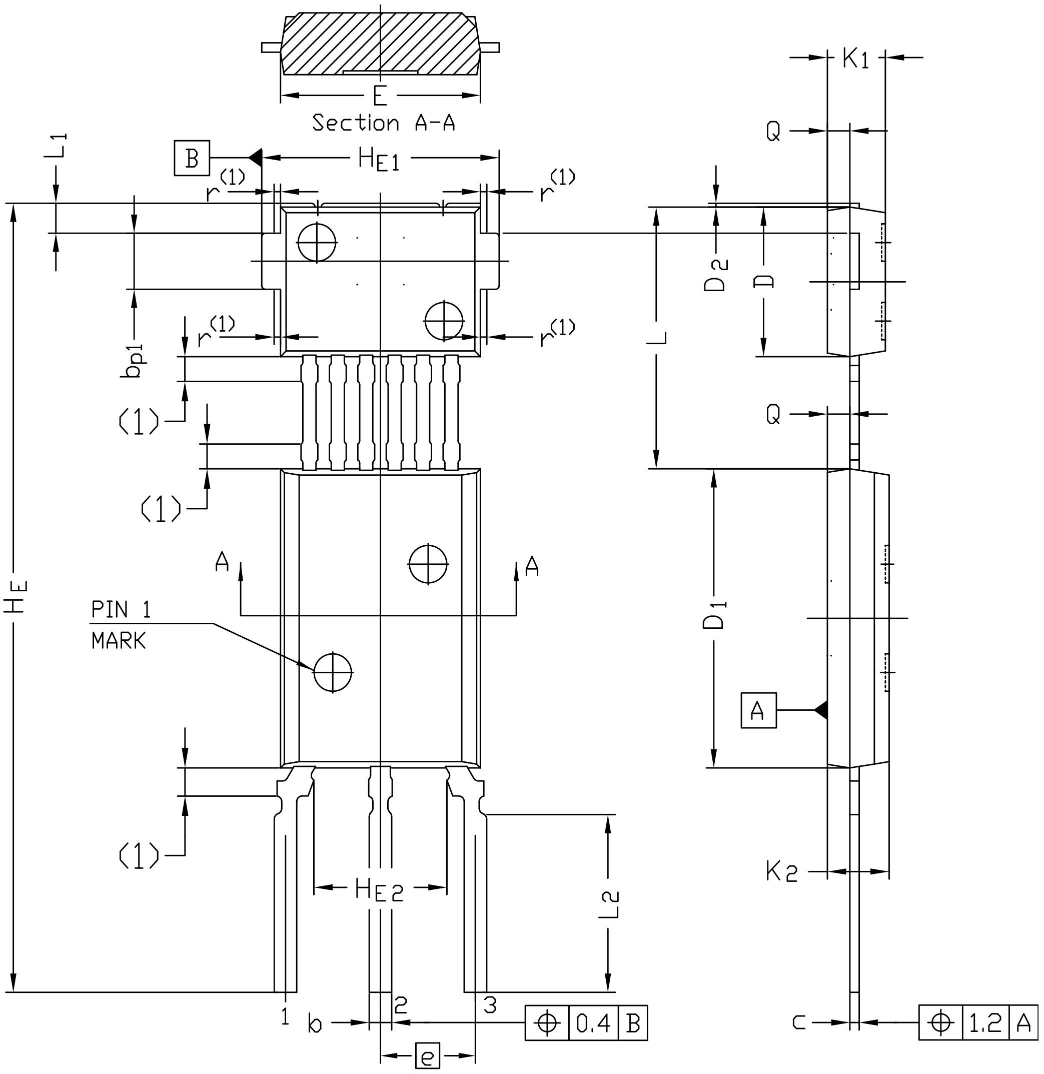
Figure 30. Reading point position

22.2 Terminals

Lead frame material: CuZr with 99.9 % Cu and 0.1 % Zr.

Lead frame plating: 100 % Sn.

23 Package outline



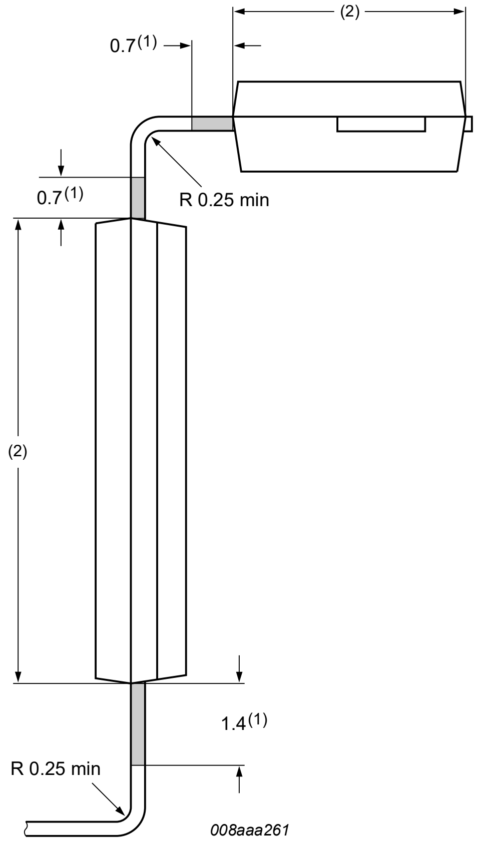
UNIT	b	bp1	c	D	D1	D2	e	E	HE	HE1	HE2	K1	K2	L	L1	L2	Q	r
min	0.55	1.47	0.24	3.9	7.9	0.05	2.54	5.25	21.0	6.32	3.45	1.45	1.55	6.9	0.75	4.75	0.55	--
max	0.65	1.57	0.30	4.1	8.1	0.15		5.45	21.4	6.42	--	1.65	1.75	7.1	0.85	--	0.65	0.17

Note

1. Terminal within this zone is uncontrolled

Figure 31. Package outline SOT1288-3 (SIL3)

24 Handling information



Dimensions in mm

1. No bending allowed.
2. Plastic body and interface plastic body - leads: application of bending forces not allowed.

Figure 32. Bending recommendation

25 Soldering

The solderability qualification is according to AEC-Q100 Rev-H. Recommended soldering process for leaded devices is wave soldering. The maximum soldering temperature is 260 °C for maximum 5 s. Device terminals are compatible with laser and electrical welding. The package is reflow capable.

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26 Abbreviations

Table 66. Abbreviations

Acronym	Description
ADC	analog-to-digital converter
AEC	automotive electronics council
ALU	arithmetic logic unit
AMR	anisotropic MR
ANSI	american national standards institute
ASIC	application-specific integrated circuit
ASIL	automotive safety integrity level
BIST	built-in self-test
CORDIC	coordinate rotation digital computer
CRC	cyclic redundancy check
CW	continuous wave
DAC	digital-to-analog converter
ECC	error correcting code
EDC	error detection and correction
EMC	electromagnetic compatibility
ESD	electrostatic discharge
ESP	enhanced serial protocol
GSM	global system for mobile
ID	identification
LSB	least significant bit
LSN	least significant nibble
MPC	multipoint calibration
MR	magnetoresistive
MSB	most significant bit
MSN	most significant nibble
NVM	non-volatile memory
OEM	original equipment manufacturer
OOR	out of range
OWI	one-wire interface
PCB	printed-circuit board
POR	power-on reset
SENT	single edge nibble transmission

27 Revision history

Table 67. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
KMA310 v.3	20190227	Product data sheet	-	KMA310 v.2
Modifications:	• Table 59: updated • Equation (14): example for angular range 45° changed to 40° and value changed to 9C7h • Figure 30: updated • Figure 31: updated			
KMA310 v.2	20180704	Product data sheet	-	KMA320 v.1
Modifications:	• Section 2: updated • Figure 16: updated			
KMA310 v.1	20180222	Product data sheet	-	-

28 Legal information

28.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Contents

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