



LPC12D27

32-bit ARM Cortex-M0 microcontroller; 128 kB flash and 8 kB SRAM; 40 segment x 4 LCD driver

Rev. 1 — 20 September 2011

Product data sheet

1. General description

The LPC12D27 are ARM Cortex-M0 based microcontrollers for embedded applications featuring a high level of integration and low power consumption. The ARM Cortex-M0 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration.

The LPC12D27 is a dual-chip module consisting of a LPC1227 single-chip microcontroller combined with a PCF8576D Universal LCD driver in a low-cost 100-pin package. The LCD driver provides 40 segments and supports from one to four backplanes. Display overhead is minimized by an on-chip display RAM with auto-increment addressing.

The LPC12D27 operate at CPU frequencies of up to 45 MHz and include 128 kB of flash memory and 8 kB of data memory.

The peripheral complement of the LPC1227 microcontroller includes a micro DMA controller, one Fast-mode Plus I²C interface, one SSP interface, two UARTs, four general purpose timers, a 10-bit ADC, two comparators, and up to 40 general purpose I/O pins.

Remark: For a functional description of the LPC1227 microcontroller see the *LPC122x data sheet*. For a detailed description of the LCD driver see the *PCF8576D data sheet*. Both data sheets are available at <http://www.nxp.com/microcontrollers>

2. Features and benefits

- LCD driver
 - ◆ 40 segments.
 - ◆ One to four backplanes.
 - ◆ On-chip display RAM with auto-increment addressing.
- Processor core
 - ◆ ARM Cortex-M0 processor, running at frequencies of up to 45 MHz (one wait state from flash) or 30 MHz (zero wait states from flash). The LPC12D27 have a high score of over 45 in CoreMark CPU performance benchmark testing, equivalent to 1.51/MHz.
 - ◆ ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
 - ◆ Serial Wire Debug (SWD).
 - ◆ System tick timer.
- Memory
 - ◆ 8 kB SRAM.
 - ◆ 128 kB on-chip flash programming memory.



- ◆ In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- ◆ Includes ROM-based 32-bit integer division routines.
- Clock generation unit
 - ◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
 - ◆ 12 MHz Internal RC (IRC) oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
 - ◆ PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
 - ◆ Clock output function with divider that can reflect the system oscillator clock, IRC clock, main clock, and Watchdog clock.
 - ◆ Real-Time Clock (RTC).
- Digital peripherals
 - ◆ Micro DMA controller with 21 channels.
 - ◆ CRC engine.
 - ◆ Two UARTs with fractional baud rate generation and internal FIFO. One UART with RS-485 and modem support and one standard UART with IrDA.
 - ◆ SSP/SPI controller with FIFO and multi-protocol capabilities.
 - ◆ I²C-bus interface supporting full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode. I²C-bus pins have programmable glitch filter.
 - ◆ Up to 40 General Purpose I/O (GPIO) pins with programmable pull-up resistor, open-drain mode, programmable digital input glitch filter, and programmable input inverter.
 - ◆ Programmable output drive on all GPIO pins. Four pins support high-current output drivers.
 - ◆ All GPIO pins can be used as edge and level sensitive interrupt sources.
 - ◆ Four general purpose counter/timers with four capture inputs and four match outputs (32-bit timers) or two capture inputs and two match outputs (16-bit timers).
 - ◆ Windowed WatchDog Timer (WWDt), IEC-60335 Class B certified.
- Analog peripherals
 - ◆ One 8-channel, 10-bit ADC.
 - ◆ Two highly flexible analog comparators. Comparator outputs can be programmed to trigger a timer match signal or can be used to emulate 555 timer behavior.
- Power
 - ◆ Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
 - ◆ Processor wake-up from Deep-sleep mode via start logic using 12 port pins.
 - ◆ Processor wake-up from Deep-power down and Deep-sleep modes via the RTC.
 - ◆ Brownout detect with three separate thresholds each for interrupt and forced reset.
 - ◆ Power-On Reset (POR).
 - ◆ Integrated PMU (Power Management Unit).
- Unique device serial number for identification.
- 3.3 V power supply.
- Available as 100-pin LQFP package.

3. Applications

- White goods
- Portable medical devices
- Lighting control
- Thermostats
- Alarm systems

4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|--------------------|---------|---|----------|
| | Name | Description | Version |
| LPC12D27FBD100/301 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |

4.1 Ordering options

Table 2. Ordering options for LPC12D27

| Type number | Flash | Total SRAM | UART RS-485 | I ² C/ FM+ | SSP | ADC channels | Package |
|--------------------|--------|------------|-------------|-----------------------|-----|--------------|---------|
| LPC12D27FBD100/301 | 128 kB | 8 kB | 1 | 1 | 1 | 8 | LQFP100 |

5. Block diagram

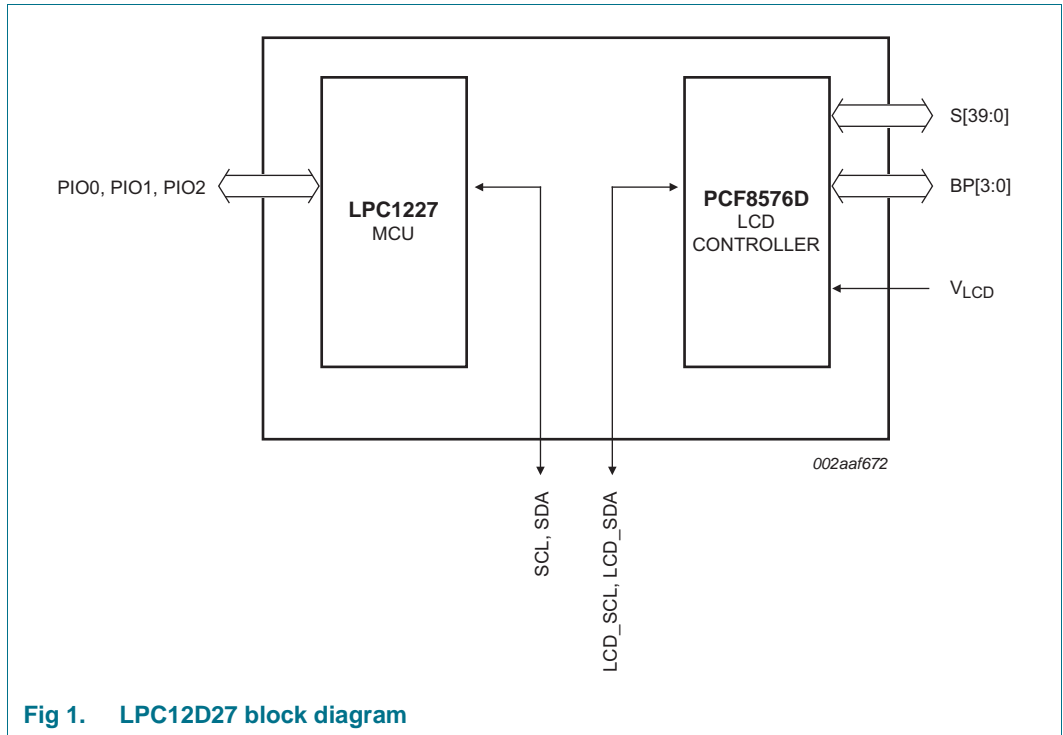


Fig 1. LPC12D27 block diagram

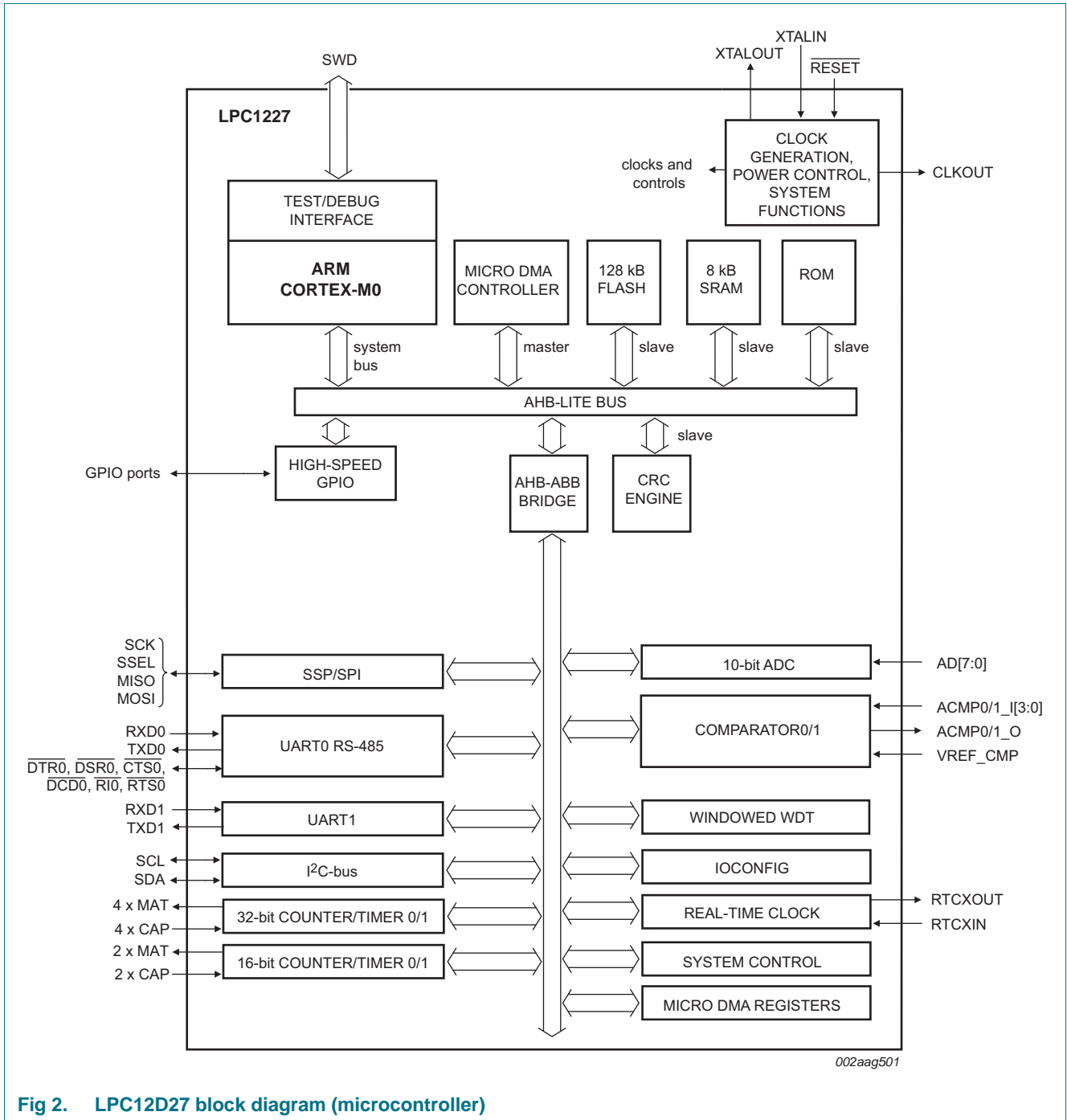
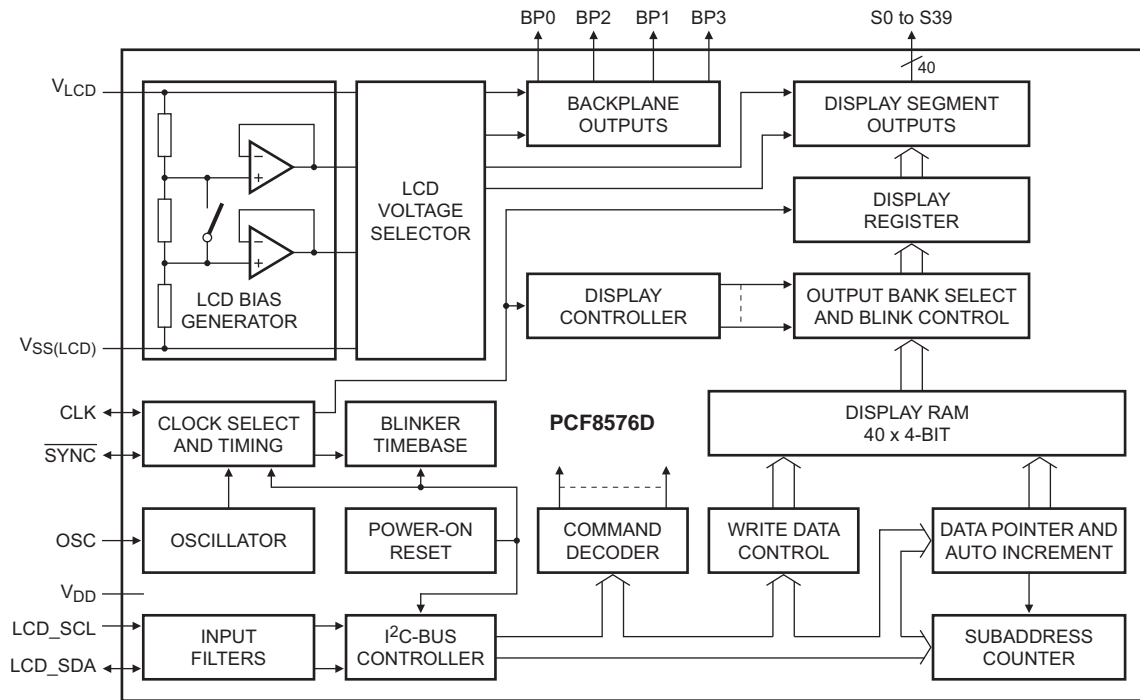


Fig 2. LPC12D27 block diagram (microcontroller)



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Fig 3. LCD display controller block diagram

6. Pinning information

6.1 Pinning

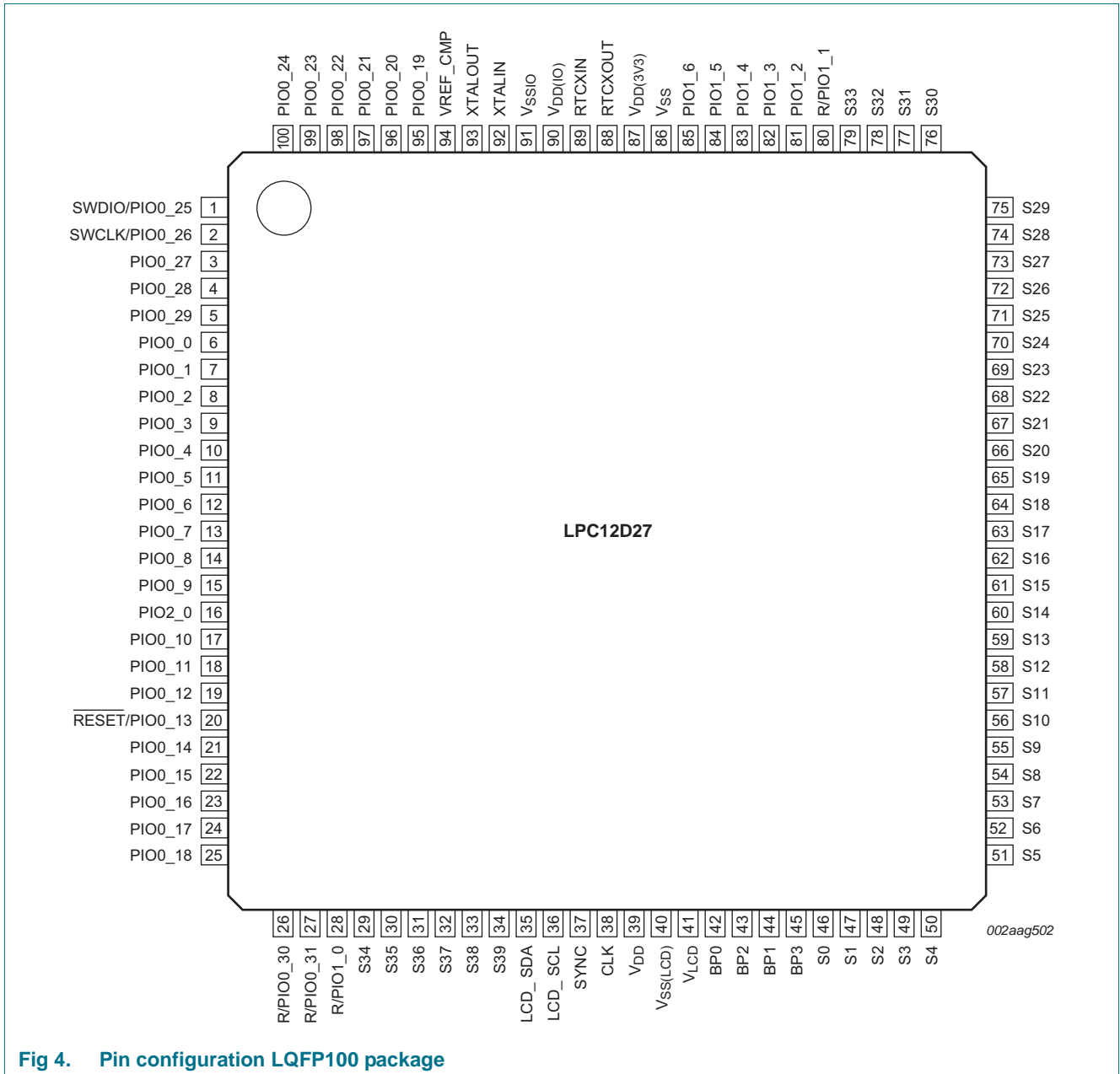


Fig 4. Pin configuration LQFP100 package

6.2 Pin description

All pins except the supply pins and the LCD pins can have more than one function as shown in [Table 3](#). The pin function is selected through the pin's IOCON register in the IOCONFIG block. The multiplexed functions include the counter/timer inputs and outputs, the UART receive, transmit, and control functions, and the serial wire debug functions.

For each pin, the default function is listed first together with the pin's reset state.

Table 3. LPC12D27 LQFP100 pin description

| Symbol | Pin | Start logic input | Reset state [1] | Type | Description |
|---|------------------------|-------------------|---------------------------------|------|--|
| Microcontroller pins | | | | | |
| PIO0_0 to PIO0_31 | | | | I/O | Port 0 — Port 0 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block. |
| PIO0_0/ $\overline{\text{RTS0}}$ | 6 [2] | yes | I; PU | I/O | PIO0_0 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | O | $\overline{\text{RTS0}}$ — Request To Send output for UART0. |
| PIO0_1/RXD0/ CT32B0_CAP0/ CT32B0_MAT0 | 7 [2] | yes | I; PU | I/O | PIO0_1 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | I | RXD0 — Receiver input for UART0. |
| | | | | I | CT32B0_CAP0 — Capture input, channel 0 for 32-bit timer 0. |
| | | | | O | CT32B0_MAT0 — Match output, channel 0 for 32-bit timer 0. |
| PIO0_2/TXD0/ CT32B0_CAP1/ CT32B0_MAT1 | 8 [2] | yes | I; PU | I/O | PIO0_2 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | O | TXD0 — Transmitter output for UART0. |
| | | | | I | CT32B0_CAP1 — Capture input, channel 1 for 32-bit timer 0. |
| | | | | O | CT32B0_MAT1 — Match output, channel 1 for 32-bit timer 0. |
| PIO0_3/ $\overline{\text{DTR0}}$ / CT32B0_CAP2/ CT32B0_MAT2 | 9 [2] | yes | I; PU | I/O | PIO0_3 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | O | $\overline{\text{DTR0}}$ — Data Terminal Ready output for UART0. |
| | | | | I | CT32B0_CAP2 — Capture input, channel 2 for 32-bit timer 0. |
| | | | | O | CT32B0_MAT2 — Match output, channel 2 for 32-bit timer 0. |
| PIO0_4/ CT32B0_CAP3/ CT32B0_MAT3 | 10 [2] | yes | I; PU | I/O | PIO0_4 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | I | DSR0 — Data Set Ready input for UART0. |
| | | | | I | CT32B0_CAP3 — Capture input, channel 3 for 32-bit timer 0. |
| | | | | O | CT32B0_MAT3 — Match output, channel 3 for 32-bit timer 0. |
| PIO0_5/ $\overline{\text{DCD0}}$ | 11 [2] | yes | I; PU | I/O | PIO0_5 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | I | $\overline{\text{DCD0}}$ — Data Carrier Detect input for UART0. |

Table 3. LPC12D27 LQFP100 pin description ...continued

| Symbol | Pin | Start logic input | Reset state | Type | Description |
|---|-------------------|-------------------|-------------|------|--|
| PIO0_6/ $\overline{\text{RI0}}$ / CT32B1_CAP0/ CT32B1_MAT0 | 12 ^[2] | yes | I; PU | I/O | PIO0_6 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | I | $\overline{\text{RI0}}$ — Ring Indicator input for UART0. |
| | | | | I | CT32B1_CAP0 — Capture input, channel 0 for 32-bit timer 1. |
| | | | | O | CT32B1_MAT0 — Match output, channel 0 for 32-bit timer 1. |
| PIO0_7/ $\overline{\text{CTS0}}$ / CT32B1_CAP1/ CT32B1_MAT1 | 13 ^[2] | yes | I; PU | I/O | PIO0_7 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | I | $\overline{\text{CTS0}}$ — Clear To Send input for UART0. |
| | | | | I | CT32B1_CAP1 — Capture input, channel 1 for 32-bit timer 1. |
| | | | | O | CT32B1_MAT1 — Match output, channel 1 for 32-bit timer 1. |
| PIO0_8/RXD1 /CT32B1_CAP2/ CT32B1_MAT2 | 14 ^[2] | yes | I; PU | I/O | PIO0_8 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | I | RXD1 — Receiver input for UART1. |
| | | | | I | CT32B1_CAP2 — Capture input, channel 2 for 32-bit timer 1. |
| | | | | O | CT32B1_MAT2 — Match output, channel 2 for 32-bit timer 1. |
| PIO0_9/TXD1/ CT32B1_CAP3/ CT32B1_MAT3 | 15 ^[2] | yes | I; PU | I/O | PIO0_9 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | O | TXD1 — Transmitter output for UART1. |
| | | | | I | CT32B1_CAP3 — Capture input, channel 3 for 32-bit timer 1. |
| | | | | O | CT32B1_MAT3 — Match output, channel 3 for 32-bit timer 1. |
| PIO0_10/SCL | 17 ^[3] | yes | I; IA | I/O | PIO0_10 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | I/O | SCL — I ² C-bus clock input/output. |
| PIO0_11/SDA/ CT16B0_CAP0/ CT16B0_MAT0 | 18 ^[3] | yes | I; IA | I/O | PIO0_11 — General purpose digital input/output pin. Also serves as wake-up pin from Deep-sleep mode. |
| | | | | I/O | SDA — I ² C-bus data input/output. |
| | | | | I | CT16B0_CAP0 — Capture input, channel 0 for 16-bit timer 0. |
| | | | | O | CT16B0_MAT0 — Match output, channel 0 for 16-bit timer 0. |
| PIO0_12/CLKOUT/ CT16B0_CAP1/ CT16B0_MAT1 | 19 ^[7] | no | I; PU | I/O | PIO0_12 — General purpose digital input/output pin. A LOW level on this pin in during reset starts the ISP command handler. High-current output driver. |
| | | | | O | CLKOUT — Clock out pin. |
| | | | | I | CT16B0_CAP1 — Capture input, channel 0 for 16-bit timer 0. |
| | | | | O | CT16B0_MAT1 — Match output, channel 1 for 16-bit timer 0. |
| $\overline{\text{RESET}}$ /PIO0_13 | 20 ^[4] | no | I; PU | I | $\overline{\text{RESET}}$ — External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. |
| | | | | I/O | PIO0_13 — General purpose digital input/output pin. |
| PIO0_14/SCK | 21 ^[2] | no | I; PU | I/O | PIO0_14 — General purpose digital input/output pin. |
| | | | | I/O | SCK — Serial clock for SSP. |

Table 3. LPC12D27 LQFP100 pin description ...continued

| Symbol | Pin | Start logic input | Reset state | Type | Description |
|--|--------------------|-------------------|-------------|------|---|
| PIO0_15/SSEL/ CT16B1_CAP0/ CT16B1_MAT0 | 22 ^[2] | no | I; PU | I/O | PIO0_15 — General purpose digital input/output pin. |
| | | | | I/O | SSEL — Slave select for SSP. |
| | | | | I | CT16B1_CAP0 — Capture input, channel 0 for 16-bit timer 1. |
| | | | | O | CT16B1_MAT0 — Match output, channel 0 for 16-bit timer 1. |
| PIO0_16/MISO/ CT16B1_CAP1/ CT16B1_MAT1 | 23 ^[2] | no | I; PU | I/O | PIO0_16 — General purpose digital input/output pin. |
| | | | | I/O | MISO — Master In Slave Out for SSP. |
| | | | | I | CT16B1_CAP1 — Capture input, channel 1 for 16-bit timer 1. |
| | | | | O | CT16B1_MAT1 — Match output, channel 1 for 16-bit timer 1. |
| PIO0_17/MOSI | 24 ^[2] | no | I; PU | I/O | PIO0_17 — General purpose digital input/output pin. |
| | | | | I/O | MOSI — Master Out Slave In for SSP. |
| PIO0_18/SWCLK/ CT32B0_CAP0/ CT32B0_MAT0 | 25 ^[2] | no | I; PU | I/O | PIO0_18 — General purpose digital input/output pin. |
| | | | | I | SWCLK — Serial wire clock, alternate location. |
| | | | | I | CT32B0_CAP0 — Capture input, channel 0 for 32-bit timer 0. |
| | | | | O | CT32B0_MAT0 — Match output, channel 0 for 32-bit timer 0. |
| PIO0_19/ACMP0_I0/ CT32B0_CAP1/ CT32B0_MAT1 | 95 ^[5] | no | I; PU | I/O | PIO0_19 — General purpose digital input/output pin. |
| | | | | I | ACMP0_I0 — Input 0 for comparator 0. |
| | | | | I | CT32B0_CAP1 — Capture input, channel 1 for 32-bit timer 0. |
| | | | | O | CT32B0_MAT1 — Match output, channel 1 for 32-bit timer 0. |
| PIO0_20/ACMP0_I1/ CT32B0_CAP2/ CT32B0_MAT2 | 96 ^[5] | no | I; PU | I/O | PIO0_20 — General purpose digital input/output pin. |
| | | | | I | ACMP0_I1 — Input 1 for comparator 0. |
| | | | | I | CT32B0_CAP2 — Capture input, channel 2 for 32-bit timer 0. |
| | | | | O | CT32B0_MAT2 — Match output, channel 2 for 32-bit timer 0. |
| PIO0_21/ACMP0_I2/ CT32B0_CAP3/ CT32B0_MAT3 | 97 ^[5] | no | I; PU | I/O | PIO0_21 — General purpose digital input/output pin. |
| | | | | I | ACMP0_I2 — Input 2 for comparator 0. |
| | | | | I | CT32B0_CAP3 — Capture input, channel 3 for 32-bit timer 0. |
| | | | | O | CT32B0_MAT3 — Match output, channel 3 for 32-bit timer 0. |
| PIO0_22/ACMP0_I3 | 98 ^[5] | no | I; PU | I/O | PIO0_22 — General purpose digital input/output pin. |
| | | | | I | ACMP0_I3 — Input 3 for comparator 0. |
| PIO0_23/ ACMP1_I0/ CT32B1_CAP0/ CT32B1_MAT0 | 99 ^[5] | no | I; PU | I/O | PIO0_23 — General purpose digital input/output pin. |
| | | | | I | ACMP1_I0 — Input 0 for comparator 1. |
| | | | | I | CT32B1_CAP0 — Capture input, channel 0 for 32-bit timer 1. |
| | | | | O | CT32B1_MAT0 — Match output, channel 0 for 32-bit timer 1. |
| PIO0_24/ACMP1_I1/ CT32B1_CAP1/ CT32B1_MAT1 | 100 ^[5] | no | I; PU | I/O | PIO0_24 — General purpose digital input/output pin. |
| | | | | I | ACMP1_I1 — Input 1 for comparator 1. |
| | | | | I | CT32B1_CAP1 — Capture input, channel 1 for 32-bit timer 1. |
| | | | | O | CT32B1_MAT1 — Match output, channel 1 for 32-bit timer 1. |

Table 3. LPC12D27 LQFP100 pin description ...continued

| Symbol | Pin | Start logic input | Reset state | Type | Description |
|--|-------------------|-------------------|-------------|------|---|
| SWDIO/ACMP1_I2/ CT32B1_CAP2/ CT32B1_MAT2/PIO0_25 | 1 ^[5] | no | I; PU | I/O | SWDIO — Serial wire debug input/output, default location. |
| | | | | I | ACMP1_I2 — Input 2 for comparator 1. |
| | | | | I | CT32B1_CAP2 — Capture input, channel 2 for 32-bit timer 1. |
| | | | | O | CT32B1_MAT2 — Match output, channel 2 for 32-bit timer 1. |
| SWCLK/ ACMP1_I3/ CT32B1_CAP3/ CT32B1_MAT3/PIO0_26 | 2 ^[6] | no | I; PU | I/O | SWCLK — Serial wire clock, default location. |
| | | | | I | ACMP1_I3 — Input 3 for comparator 1. |
| | | | | I | CT32B1_CAP3 — Capture input, channel 3 or 32-bit timer 1. |
| | | | | O | CT32B1_MAT3 — Match output, channel 3 for 32-bit timer 1. |
| PIO0_27/ACMP0_O | 3 ^[7] | no | I; PU | I/O | PIO0_27 — General purpose digital input/output pin (high-current output driver). |
| | | | | O | ACMP0_O — Output for comparator 0. |
| PIO0_28/ACMP1_O/ CT16B0_CAP0/ CT16B0_MAT0 | 4 ^[7] | no | I; PU | I/O | PIO0_28 — General purpose digital input/output pin (high-current output driver). |
| | | | | O | ACMP1_O — Output for comparator 1. |
| | | | | I | CT16B0_CAP0 — Capture input, channel 0 for 16-bit timer 0. |
| PIO0_29/ROSC/ CT16B0_CAP1/ CT16B0_MAT1 | 5 ^[7] | no | I; PU | I/O | PIO0_29 — General purpose digital input/output pin (high-current output driver). |
| | | | | I/O | ROSC — Relaxation oscillator for 555 timer applications. |
| | | | | I | CT16B0_CAP1 — Capture input, channel 1 for 16-bit timer 0. |
| | | | | O | CT16B0_MAT1 — Match output, channel 1 for 16-bit timer 0. |
| R/PIO0_30/AD0 | 26 ^[5] | no | I; PU | I | R — Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | | I/O | PIO0_30 — General purpose digital input/output pin. |
| | | | | I | AD0 — A/D converter, input 0. |
| R/PIO0_31/AD1 | 27 ^[5] | no | I; PU | I | R — Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | | I/O | PIO0_31 — General purpose digital input/output pin. |
| | | | | I | AD1 — A/D converter, input 1. |
| PIO1_0 to PIO1_6 | | | | I/O | Port 1 — Port 1 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block. Pins PIO1_7 through PIO1_31 are not available. |
| R/PIO1_0/AD2 | 28 ^[5] | no | I; PU | O | R — Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | | I/O | PIO1_0 — General purpose digital input/output pin. |
| | | | | I | AD2 — A/D converter, input 2. |

Table 3. LPC12D27 LQFP100 pin description ...continued

| Symbol | Pin | Start logic input | Reset state | Type | Description |
|--|-------------------|-------------------|---------------------------------|------|--|
| R/PIO1_1/AD3 | 80 ^[5] | no | I; PU | I | R — Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | | I/O | PIO1_1 — General purpose digital input/output pin. |
| | | | | I | AD3 — A/D converter, input 3. |
| PIO1_2/SWDIO/AD4 | 81 ^[5] | no | I; PU | I/O | PIO1_2 — General purpose digital input/output pin. |
| | | | | I/O | SWDIO — Serial wire debug input/output, alternate location. |
| | | | | I | AD4 — A/D converter, input 4. |
| PIO1_3/AD5/WAKEUP | 82 ^[6] | no | I; PU | I/O | PIO1_3 — General purpose digital input/output pin. |
| | | | | I | AD5 — A/D converter, input 5. |
| | | | | I | WAKEUP — Deep power-down mode wake-up pin. |
| PIO1_4/AD6 | 83 ^[5] | no | I; PU | I/O | PIO1_4 — General purpose digital input/output pin. |
| | | | | I | AD6 — A/D converter, input 6. |
| PIO1_5/AD7/ CT16B1_CAP0/ CT16B1_MAT0 | 84 ^[5] | no | I; PU | I/O | PIO1_5 — General purpose digital input/output pin. |
| | | | | I | AD7 — A/D converter, input 7. |
| | | | | I | CT16B1_CAP0 — Capture input, channel 0 for 16-bit timer 1. |
| | | | | O | CT16B1_MAT0 — Match output, channel 0 for 16-bit timer 1. |
| PIO1_6/CT16B1_CAP1/ CT16B1_MAT1 | 85 ^[2] | no | I; PU | I/O | PIO1_6 — General purpose digital input/output pin. |
| | | | | I | CT16B1_CAP1 — Capture input, channel 1 for 16-bit timer 1. |
| | | | | O | CT16B1_MAT1 — Match output, channel 1 for 16-bit timer 1. |
| PIO2_0 | | | | I/O | Port 2 — Port 2 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 through PIO2_31 are not available. |
| PIO2_0/CT16B0_CAP0/ CT16B0_MAT0 | 16 ^[2] | no | I; PU | I/O | PIO2_0 — General purpose digital input/output pin. |
| | | | | I | CT16B0_CAP0 — Capture input, channel 0 for 16-bit timer 0. |
| | | | | O | CT16B0_MAT0 — Match output, channel 0 for 16-bit timer 0. |
| RTCXIN | 89 | - | - | - | Input to the 32 kHz oscillator circuit. |
| RTCXOUT | 88 | - | - | - | Output from the 32 kHz oscillator amplifier. |
| XTALIN | 92 | - | - | - | Input to the system oscillator circuit and internal clock generator circuits. |
| XTALOUT | 93 | - | - | - | Output from the system oscillator amplifier. |
| VREF_CMP | 94 | - | - | - | Reference voltage for comparator. |
| V _{DD(I/O)} | 90 | - | - | - | Input/output supply voltage. |
| V _{DD(3V3)} | 87 | - | - | - | 3.3 V supply voltage to the internal regulator and the ADC. Also used as the ADC reference voltage. |
| V _{SSIO} | 91 | - | - | - | Ground. |
| V _{SS} | 86 | - | - | - | Ground. |
| LCD display pins | | | | | |
| S0 | 46 | - | V _{LCD} ^[8] | O | LCD segment output. |
| S1 | 47 | - | V _{LCD} ^[8] | O | LCD segment output. |

Table 3. LPC12D27 LQFP100 pin description ...continued

| Symbol | Pin | Start logic input | Reset state [1] | Type | Description |
|--------|-----|-------------------|--------------------------------------|------|-----------------------|
| S2 | 48 | - | V _{LCD} [8] | O | LCD segment output. |
| S3 | 49 | - | V _{LCD} [8] | O | LCD segment output. |
| S4 | 50 | - | V _{LCD} [8] | O | LCD segment output. |
| S5 | 51 | - | V _{LCD} [8] | O | LCD segment output. |
| S6 | 52 | - | V _{LCD} [8] | O | LCD segment output. |
| S7 | 53 | - | V _{LCD} [8] | O | LCD segment output. |
| S8 | 54 | - | V _{LCD} [8] | O | LCD segment output. |
| S9 | 55 | - | V _{LCD} [8] | O | LCD segment output. |
| S10 | 56 | - | V _{LCD} [8] | O | LCD segment output. |
| S11 | 57 | - | V _{LCD} [8] | O | LCD segment output. |
| S12 | 58 | - | V _{LCD} [8] | O | LCD segment output. |
| S13 | 59 | - | V _{LCD} [8] | O | LCD segment output. |
| S14 | 60 | - | V _{LCD} [8] | O | LCD segment output. |
| S15 | 61 | - | V _{LCD} [8] | O | LCD segment output. |
| S16 | 62 | - | V _{LCD} [8] | O | LCD segment output. |
| S17 | 63 | - | V _{LCD} [8] | O | LCD segment output. |
| S18 | 64 | - | V _{LCD} [8] | O | LCD segment output. |
| S19 | 65 | - | V _{LCD} [8] | O | LCD segment output. |
| S20 | 66 | - | V _{LCD} [8] | O | LCD segment output. |
| S21 | 67 | - | V _{LCD} [8] | O | LCD segment output. |
| S22 | 68 | - | V _{LCD} [8] | O | LCD segment output. |
| S23 | 69 | - | V _{LCD} [8] | O | LCD segment output. |
| S24 | 70 | - | V _{LCD} [8] | O | LCD segment output. |
| S25 | 71 | - | V _{LCD} [8] | O | LCD segment output. |
| S26 | 72 | - | V _{LCD} [8] | O | LCD segment output. |
| S27 | 73 | - | V _{LCD} [8] | O | LCD segment output. |
| S28 | 74 | - | V _{LCD} [8] | O | LCD segment output. |
| S29 | 75 | - | V _{LCD} [8] | O | LCD segment output. |
| S30 | 76 | - | V _{LCD} [8] | O | LCD segment output. |
| S31 | 77 | - | V _{LCD} [8] | O | LCD segment output. |
| S32 | 78 | - | V _{LCD} [8] | O | LCD segment output. |
| S33 | 79 | - | V _{LCD} [8] | O | LCD segment output. |
| S34 | 29 | - | V _{LCD} [8] | O | LCD segment output. |
| S35 | 30 | - | V _{LCD} [8] | O | LCD segment output. |
| S36 | 31 | - | V _{LCD} [8] | O | LCD segment output. |
| S37 | 32 | - | V _{LCD} [8] | O | LCD segment output. |
| S38 | 33 | - | V _{LCD} [8] | O | LCD segment output. |
| S39 | 34 | - | V _{LCD} [8] | O | LCD segment output. |
| BP0 | 42 | - | V _{LCD} [8] | O | LCD backplane output. |

Table 3. LPC12D27 LQFP100 pin description ...continued

| Symbol | Pin | Start logic input | Reset state | Type | Description |
|----------------------|-----|-------------------|----------------------|------|---|
| BP1 | 44 | - | V _{LCD} [8] | O | LCD backplane output. |
| BP2 | 43 | - | V _{LCD} [8] | O | LCD backplane output. |
| BP3 | 45 | - | V _{LCD} [8] | O | LCD backplane output. |
| LCD_SDA | 35 | - | [8] | I/O | I ² C-bus serial data input/output. |
| LCD_SCL | 36 | - | [8] | I/O | I ² C-bus serial clock input. |
| SYNC | 37 | - | [8] | I/O | Cascade synchronization input/output. |
| CLK | 38 | - | [8] | I/O | External clock input/output. |
| V _{DD} | 39 | - | - | - | 1.8 V to 5.5 V power supply: Power supply voltage for the PCF8576D. |
| V _{SS(LCD)} | 40 | - | - | - | LCD ground. |
| V _{LCD} | 41 | - | - | - | LCD power supply: LCD voltage. |

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled.

[2] Digital I/O pin; default: pull-up enabled, no hysteresis.

[3] I²C-bus pins; 5 V tolerant; open-drain; default: no pull-up/pull-down, no hysteresis.

[4] Digital I/O pin with RESET function; default: pull-up enabled, no hysteresis.

[5] Digital I/O pin with analog function; default: pull-up enabled, no hysteresis.

[6] Digital I/O pin with analog function and WAKEUP function; default: pull-up enabled, no hysteresis.

[7] High-drive digital I/O pin; default: pull-up enabled, no hysteresis.

[8] See [Section 7.2.3](#).

7. Functional description

7.1 LPC1227 microcontroller

See the *LPC122x data sheet* for a detailed functional description of the LPC1227 microcontroller.

7.2 LCD driver

See the *PCF8576 data sheet* for a detailed functional description of the PCF8576D LCD driver.

7.2.1 General description

The PCF8576D is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCF8576D communicates via the two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes). Please refer to *PCF8576D data sheet* for electrical data.

7.2.2 Functional description

The PCF8576D is a versatile peripheral device interfacing the LPC1227 microcontroller with a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

The possible display configurations of the PCF8576D depend on the number of active backplane outputs required. A selection of display configurations is shown in [Table 4](#). The integration of the LPC1227 microcontroller with the PCF8576D is shown in [Figure 1](#).

Table 4. Selection of display configurations

| Number of Backplanes | Segments | Digits/Characters | | |
|----------------------|----------|-------------------|------------|---------------------|
| | | 7-segment | 14-segment | Dot matrix/Elements |
| 4 | 160 | 20 | 10 | 160 (4 × 40) |
| 3 | 120 | 15 | 7 | 120 (3 × 40) |
| 2 | 80 | 10 | 5 | 64 (2 × 40) |
| 1 | 40 | 5 | 2 | 40 (1 × 40) |

7.2.3 Reset state of the LCD controller and pins

After power-on, the LCD controller resets to the following starting conditions:

- All backplane and segment outputs are set to V_{LCD} .
- The selected drive mode is 1:4 multiplex with 1/3 bias.
- Blinking is switched off.
- Input and output bank selectors are reset.
- The I²C-bus interface is initialized.
- The data pointer and the subaddress counter are cleared (set to logic 0).
- The display is disabled.

Remark: Do not transfer data on the I²C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2.4 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider consisting of three impedances connected in series between V_{LCD} and $V_{SS(LCD)}$. The middle resistor can be bypassed to provide a 1/2 bias voltage level for the 1:2 multiplex configuration. The LCD voltage can be temperature compensated externally using the supply to pin V_{LCD} .

7.2.5 Oscillator

7.2.5.1 Internal clock

The internal logic of the PCF8576D and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin $V_{SS(LCD)}$. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCF8576Ds in the system that are connected in cascade.

7.2.6 Timing

The PCF8576D timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCF8576D in the system is maintained by the synchronization signal at pin $\overline{\text{SYNC}}$. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency (f_{fr}) is a fixed division of the clock frequency (f_{clk}) from either the internal or an external clock: $f_{\text{fr}} = f_{\text{clk}}/24$.

7.2.7 Display register

A display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs, and each column of the display RAM.

7.2.8 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display latch. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.2.9 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.

In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities.

In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.2.10 Display RAM

The display RAM is a static 40×4 -bit RAM which stores LCD data. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. For details, see *PCF8576D data sheet*.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|---------------------------------------|---|----------------------|-------|------------------|
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | | 3.0 | 3.6 | V |
| $V_{DD(I/O)}$ | input/output supply voltage | | 3.0 | 3.6 | V |
| V_I | input voltage | on all digital pins | ^[2] -0.5 | +3.6 | V |
| | | on pins PIO0_10 and PIO0_11 (I ² C-bus pins) | 0 | 5.5 | V |
| I_{DD} | supply current | per supply pin | ^[3] - | 100 | mA |
| I_{SS} | ground current | per ground pin | ^[3] - | 100 | mA |
| I_{latch} | I/O latch-up current | $-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125\text{ }^\circ\text{C}$ | - | 100 | mA |
| T_{stg} | storage temperature | | ^[4] -65 | +150 | $^\circ\text{C}$ |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | - | 1.5 | W |
| V_{ESD} | electrostatic discharge voltage | human body model; all pins | ^[5] -8000 | +8000 | V |

[1] The following applies to the limiting values:

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor.

9. Thermal characteristics

9.1 Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD} . The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 6. Thermal characteristics

$V_{DD} = 3.0\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C unless otherwise specified.}$

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|---|-------------------------------|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | JEDEC test board; no air flow | - | 61 | - | °C/W |
| | | LQFP64 package | | | | |
| | | LQFP48 package | | 86 | - | °C/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | JEDEC test board | - | 19 | - | °C/W |
| | | LQFP64 package | | | | |
| | | LQFP48 package | | 36 | - | °C/W |
| $T_{j(max)}$ | maximum junction temperature | | - | - | 150 | °C |

10. Static characteristics

Table 7. Static characteristics

$T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---|-----------------------------|--|---|--------------------|---------------|---------------|
| $V_{DD(I/O)}$ | input/output supply voltage | on pin $V_{DD(I/O)}$ | 3.0 | 3.3 | 3.6 | V |
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | | 3.0 | 3.3 | 3.6 | V |
| I_{DD} | supply current | Active mode; $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ °C}$; code while(1){} executed from flash | | | | |
| | | all peripherals disabled: | | | | |
| | | CCLK = 12 MHz | - | 4.6 | - | mA |
| | | CCLK = 24 MHz | - | 9 | - | mA |
| | | CCLK = 33 MHz | - | 12.2 | - | mA |
| | | all peripherals enabled: | | | | |
| | | CCLK = 12 MHz | - | 6.6 | - | mA |
| | | CCLK = 24 MHz | - | 10.9 | - | mA |
| | | CCLK = 33 MHz | - | 14.1 | - | mA |
| | | Sleep mode; $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ °C}$; all peripherals disabled | | | | |
| | | CCLK = 12 MHz | - | 1.8 | - | mA |
| | | CCLK = 24 MHz | - | 3.3 | - | mA |
| | | CCLK = 33 MHz | - | 4.4 | - | mA |
| | | Deep-sleep mode; $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ °C}$ | - | 30 | - | μA |
| | | Deep power-down mode; $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ °C}$ | - | 720 | - | nA |
| Normal-drive output pins (Standard port pins, RESET) | | | | | | |
| I_{IL} | LOW-level input current | $V_I = 0\text{ V}$; | - | - | 100 | nA |
| I_{IH} | HIGH-level input current | $V_I = V_{DD(I/O)}$; | - | - | 100 | nA |
| I_{OZ} | OFF-state output current | $V_O = 0\text{ V}$; $V_O = V_{DD(I/O)}$; | - | - | 100 | nA |
| V_I | input voltage | pin configured to provide a digital function | [2] [3] [4] 0 | - | $V_{DD(I/O)}$ | V |
| V_O | output voltage | output active | 0 | - | $V_{DD(I/O)}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD(I/O)}$ | - | - | V |

Table 7. Static characteristics ...continued
T_{amb} = -40 °C to +85 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|---|--|---------------------------------------|--------------------|------------------------|------|
| V _{IL} | LOW-level input voltage | | - | - | 0.3V _{DD(IO)} | V |
| V _{hys} | hysteresis voltage | | - | 0.4 | - | V |
| V _{OH} | HIGH-level output voltage | low mode; I _{OH} = -2 mA | V _{DD(IO)} - 0.4 | - | - | V |
| | | high mode; I _{OH} = -4 mA | V _{DD(IO)} - 0.4 | - | - | V |
| V _{OL} | LOW-level output voltage | low mode; I _{OL} = 2 mA | - | - | 0.4 | V |
| | | high mode; I _{OL} = 4 mA | - | - | 0.4 | V |
| I _{OH} | HIGH-level output current | low mode; V _{OH} = V _{DD(IO)} - 0.4 V | -2 | - | - | mA |
| | | high mode; V _{OH} = V _{DD(IO)} - 0.4 V | -4 | - | - | mA |
| I _{OL} | LOW-level output current | low mode; V _{OL} = 0.4 V | 2 | - | - | mA |
| | | high mode; V _{OL} = 0.4 V | 4 | - | - | mA |
| I _{OHS} | HIGH-level short-circuit output current | V _{OH} = 0 V | ^[5] - | - | -45 | mA |
| I _{OLS} | LOW-level short-circuit output current | V _{OL} = V _{DDA} | ^[5] - | - | 50 | mA |
| I _{pu} | pull-up current | V _I = 0 V | -50 | -80 | -100 | μA |
| High-drive output pins (PIO0_27, PIO0_28, PIO0_29, PIO0_12) | | | | | | |
| I _{IL} | LOW-level input current | V _I = 0 V; | - | - | 100 | nA |
| I _{IH} | HIGH-level input current | V _I = V _{DD(IO)} ; | - | - | 100 | nA |
| I _{OZ} | OFF-state output current | V _O = 0 V; V _O = V _{DD(IO)} ; | - | - | 100 | nA |
| V _I | input voltage | pin configured to provide a digital function | ^{[2][3]} 0 ^[4] | - | V _{DD(IO)} | V |
| V _O | output voltage | output active | 0 | - | V _{DD(IO)} | V |
| V _{IH} | HIGH-level input voltage | | 0.7V _{DD(IO)} | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.3V _{DD(IO)} | - |
| V _{hys} | hysteresis voltage | | - | - | - | V |
| V _{OH} | HIGH-level output voltage | low mode; I _{OH} = -20 mA | V _{DD(IO)} - 0.7 | - | - | V |
| | | high mode; I _{OH} = -28 mA | V _{DD(IO)} - 0.7 | - | - | V |
| V _{OL} | LOW-level output voltage | low mode; I _{OL} = 12 mA | - | - | 0.4 | V |
| | | high mode; I _{OL} = 18 mA | - | - | 0.4 | V |

Table 7. Static characteristics ...continued
 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|--|--|------------------|--------------------|-----------------|---------------|
| I_{OH} | HIGH-level output current | low mode; $V_{OH} = V_{DD(IO)} - 0.7$ | 20 | - | - | mA |
| | | high mode; $V_{OH} = V_{DD(IO)} - 0.7$ | 28 | - | - | mA |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4\text{ V}$ low mode | 12 | - | - | mA |
| | | high mode | 18 | - | - | mA |
| I_{OLS} | LOW-level short-circuit output current | $V_{OL} = V_{DD}$ | ^[5] - | - | - | mA |
| I_{pu} | pull-up current | $V_I = 0\text{ V}$ | -50 | -80 | -100 | μA |
| I²C-bus pins (PIO0_10 and PIO0_11) | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD(IO)}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{DD(IO)}$ | V |
| V_{hys} | hysteresis voltage | | - | $0.05V_{DD(IO)}$ | - | V |
| V_{OL} | LOW-level output voltage | $I_{OLS} = 20\text{ mA}$ | - | - | 0.4 | V |
| I_{LI} | input leakage current | $V_I = V_{DD(IO)}$ | ^[6] - | 2 | 4 | μA |
| | | $V_I = 5\text{ V}$ | - | 10 | 22 | μA |
| C_i | capacitance for each I/O pin | on pins PIO0_10 and PIO0_11 | - | - | 8 | pF |
| Oscillator pins | | | | | | |
| $V_{i(xtal)}$ | crystal input voltage | see Section 12.1 | 0 | 1.8 | 1.95 | V |
| $V_{o(xtal)}$ | crystal output voltage | | 0 | 1.8 | 1.95 | V |

- [1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
 [2] Including voltage on outputs in 3-state mode.
 [3] $V_{DD(3V3)}$ and $V_{DD(IO)}$ supply voltages must be present.
 [4] 3-state outputs go into 3-state mode when $V_{DD(IO)}$ is grounded.
 [5] Allowed as long as the current limit does not exceed the maximum current allowed by the device.
 [6] To V_{SS} .

10.1 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb} = 25\text{ °C}$ and $V_{DD(3V3)} = 3.3\text{ V}$.

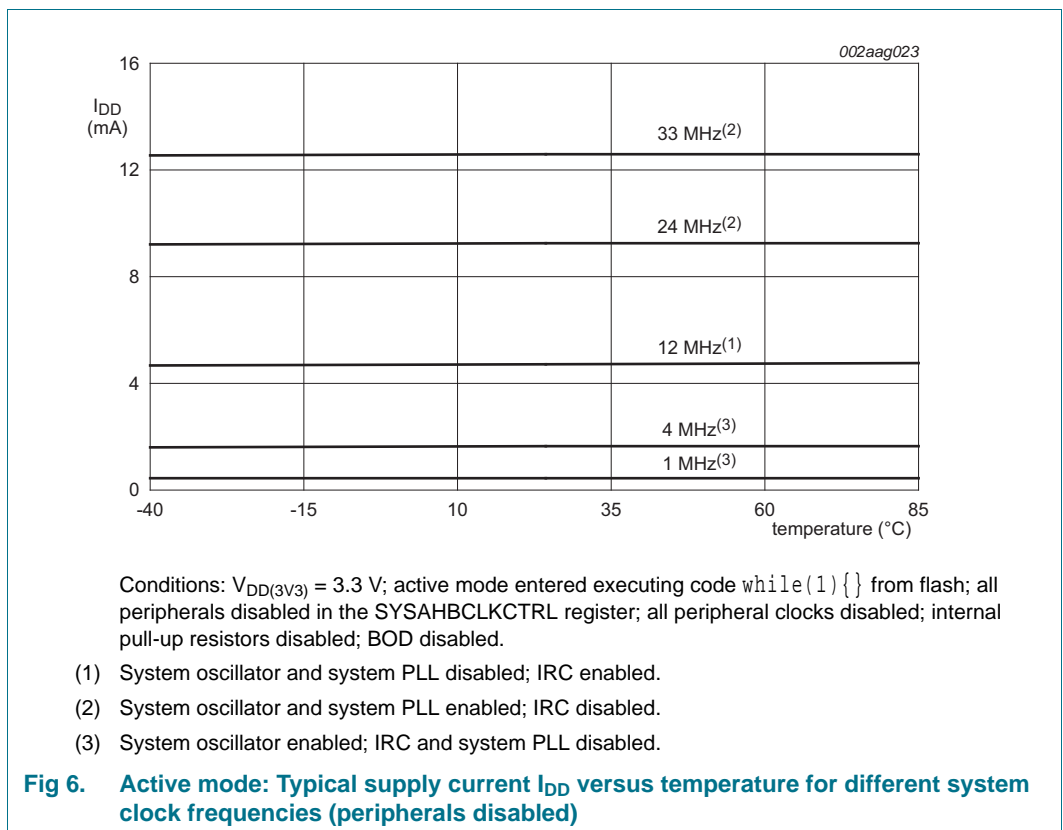
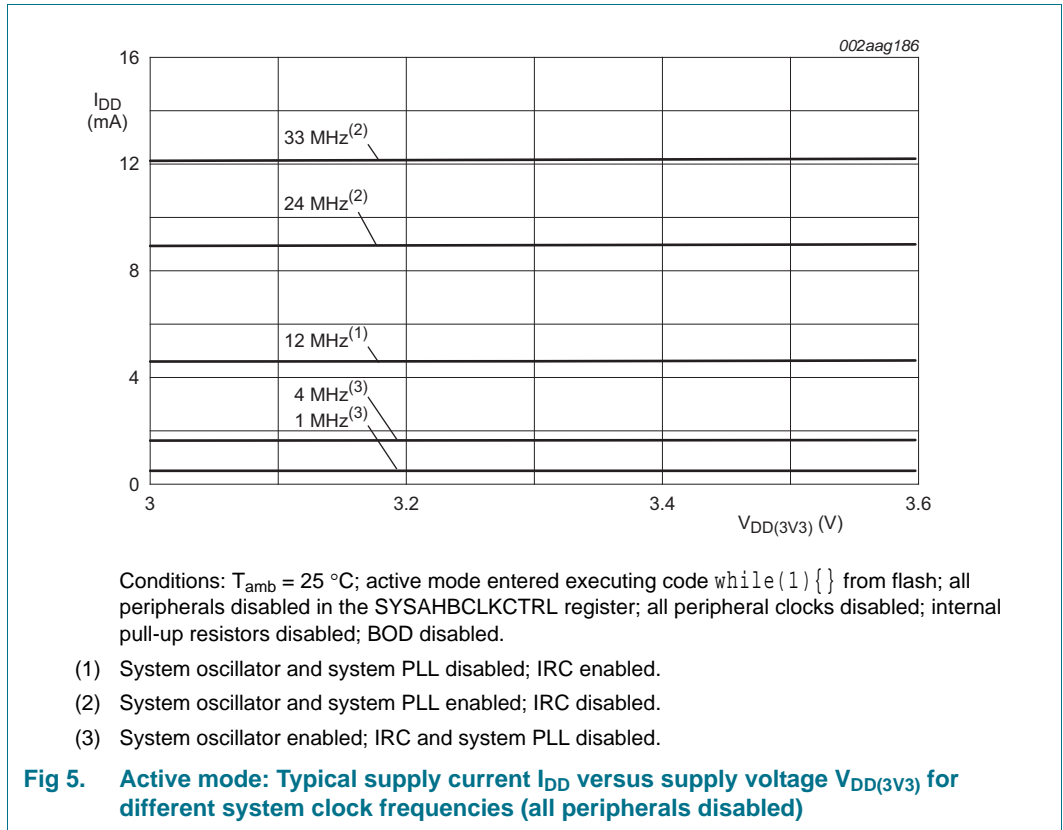
Table 8. Peripheral power consumption

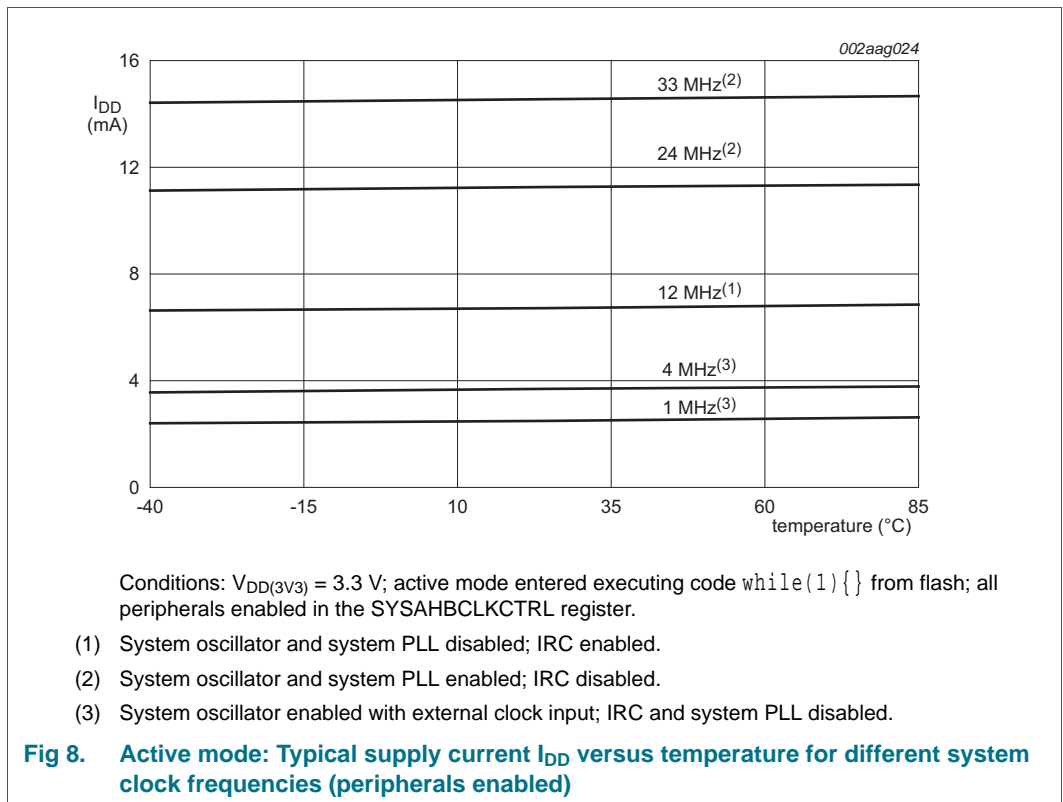
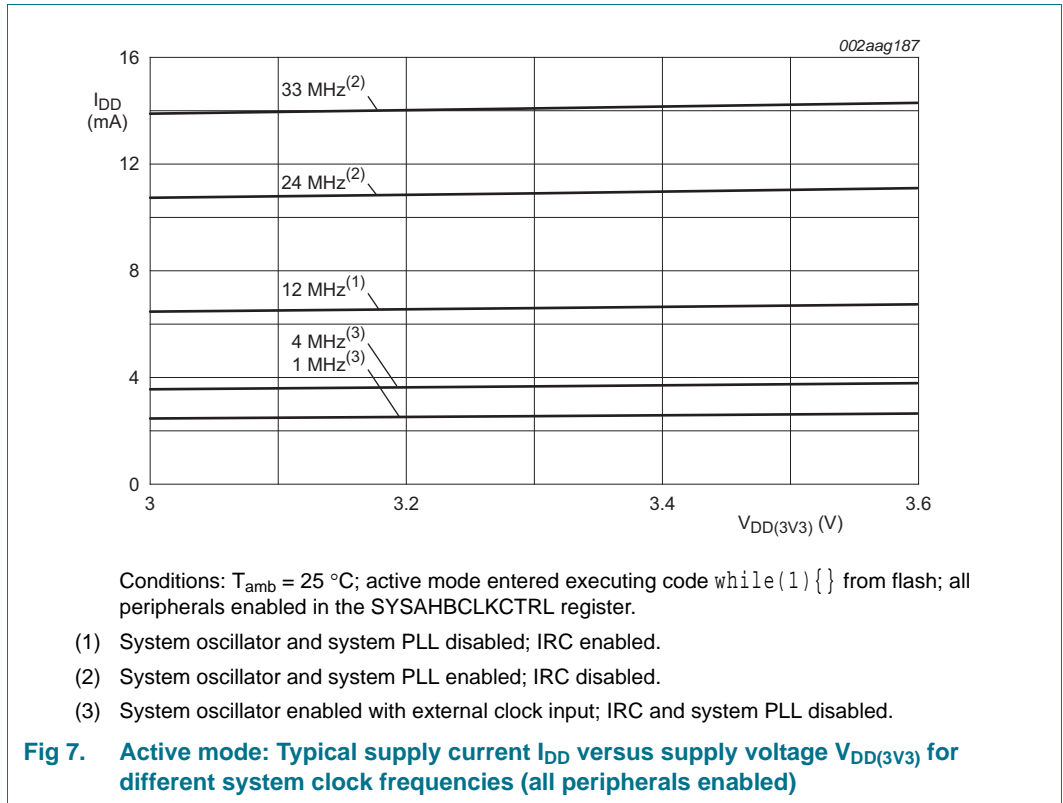
| Peripheral | Typical current consumption I_{DD} in mA | Frequency independent | | | |
|--|--|--------------------------------------|-----------|--------------------------------|------|
| | | 24 MHz system oscillator + PLL | IRC + PLL | 12 MHz system oscillator | IRC |
| IRC | 0.29 | - | - | - | - |
| PLL (PLL output frequency = 24 MHz) | 1.87 | - | - | - | - |
| WDosc (WDosc output frequency = 500 kHz) | 0.25 | - | - | - | - |
| BOD | 0.06 | - | - | - | - |
| Analog comparator 0/1 | - | 0.05 | 0.05 | 0.03 | 0.02 |
| ADC | - | 1.86 | 1.85 | 1.61 | 1.61 |
| CRC engine | - | 0.04 | 0.04 | 0.02 | 0.02 |
| 16-bit timer 0 (CT16B0) | - | 0.09 | 0.09 | 0.04 | 0.04 |
| 16-bit timer 1 (CT16B1) | - | 0.09 | 0.09 | 0.04 | 0.04 |
| 32-bit timer 0 (CT32B0) | - | 0.08 | 0.08 | 0.04 | 0.04 |
| 32-bit timer 1 (CT32B1) | - | 0.08 | 0.08 | 0.04 | 0.04 |
| GPIO0 | - | 0.34 | 0.34 | 0.17 | 0.17 |
| GPIO1 | - | 0.34 | 0.34 | 0.17 | 0.17 |
| GPIO2 | - | 0.36 | 0.37 | 0.18 | 0.18 |
| I2C | - | 0.09 | 0.09 | 0.05 | 0.05 |
| IOCON | - | 0.09 | 0.10 | 0.05 | 0.05 |
| RTC | - | 0.10 | 0.10 | 0.05 | 0.05 |
| SSP | - | 0.30 | 0.29 | 0.15 | 0.15 |
| UART0 | - | 0.52 | 0.51 | 0.26 | 0.26 |
| UART1 | - | 0.52 | 0.51 | 0.26 | 0.26 |
| DMA | - | 0.18 | 0.18 | 0.09 | 0.09 |
| WWDT | - | 0.06 | 0.06 | 0.03 | 0.03 |

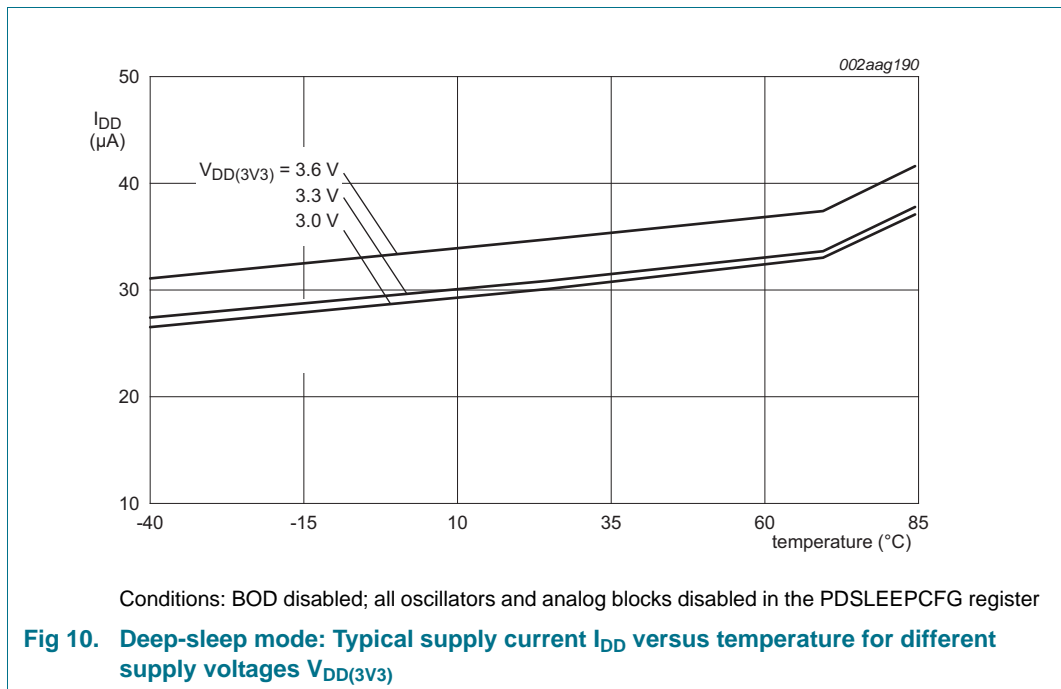
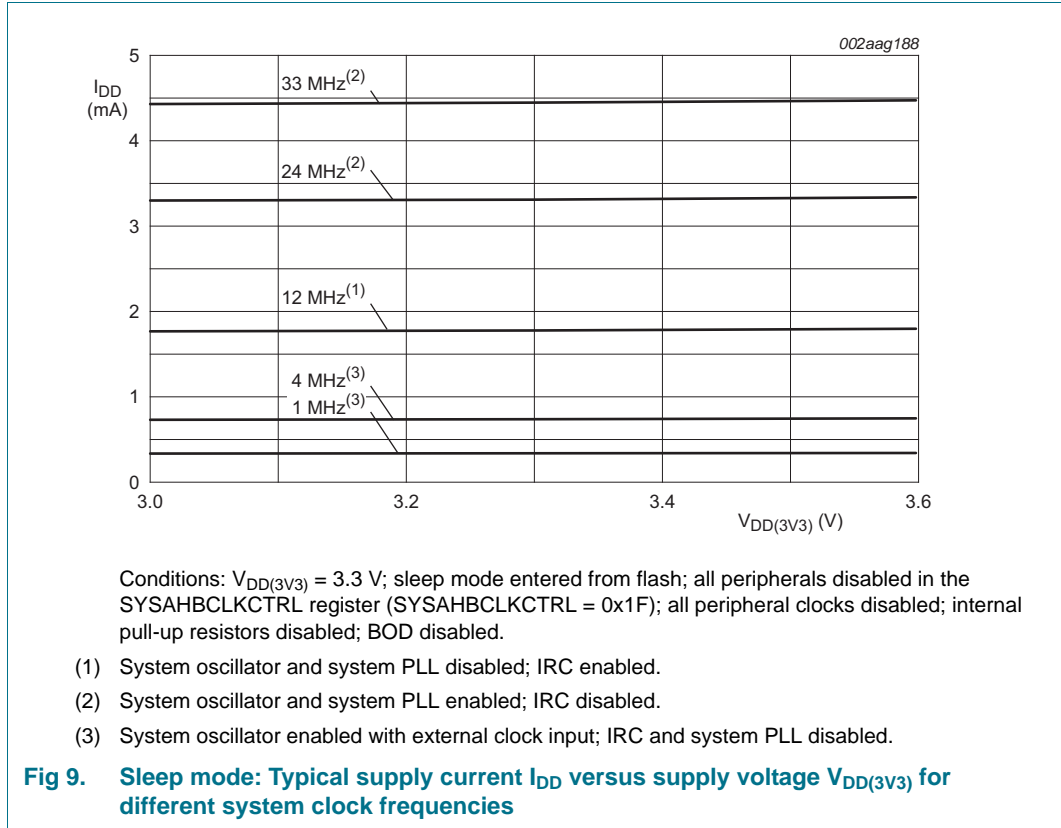
10.2 Power consumption

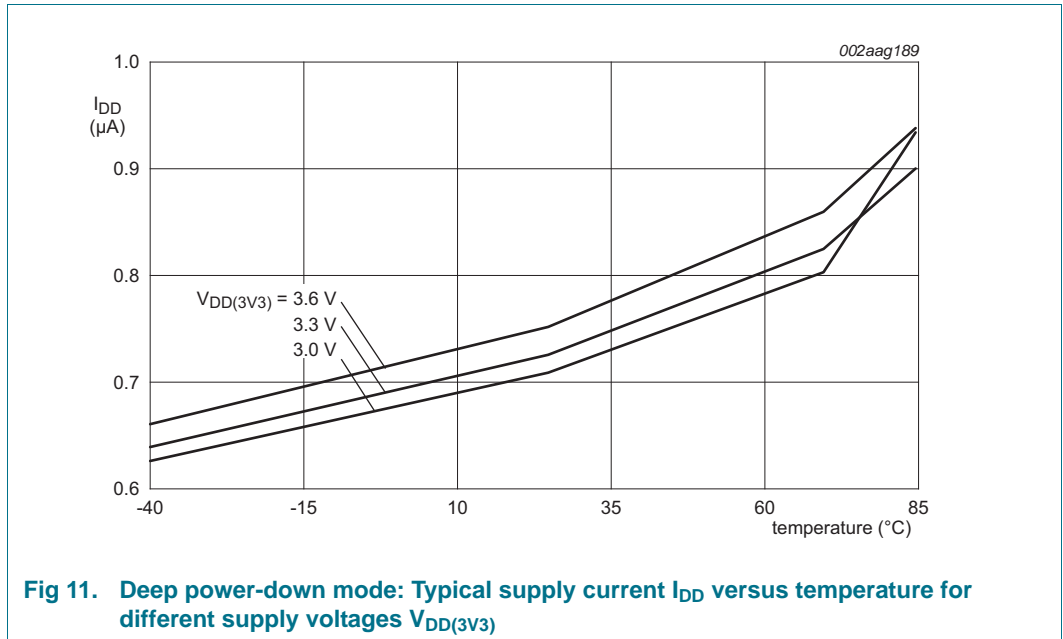
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC122x user manual*):

- Active mode: all GPIO pins set to input with external pull-up resistors.
- Sleep and Deep-sleep modes: all GPIO pins set to output driving LOW.
- Deep power-down mode: all GPIO pins set to input with external pull-up resistors.

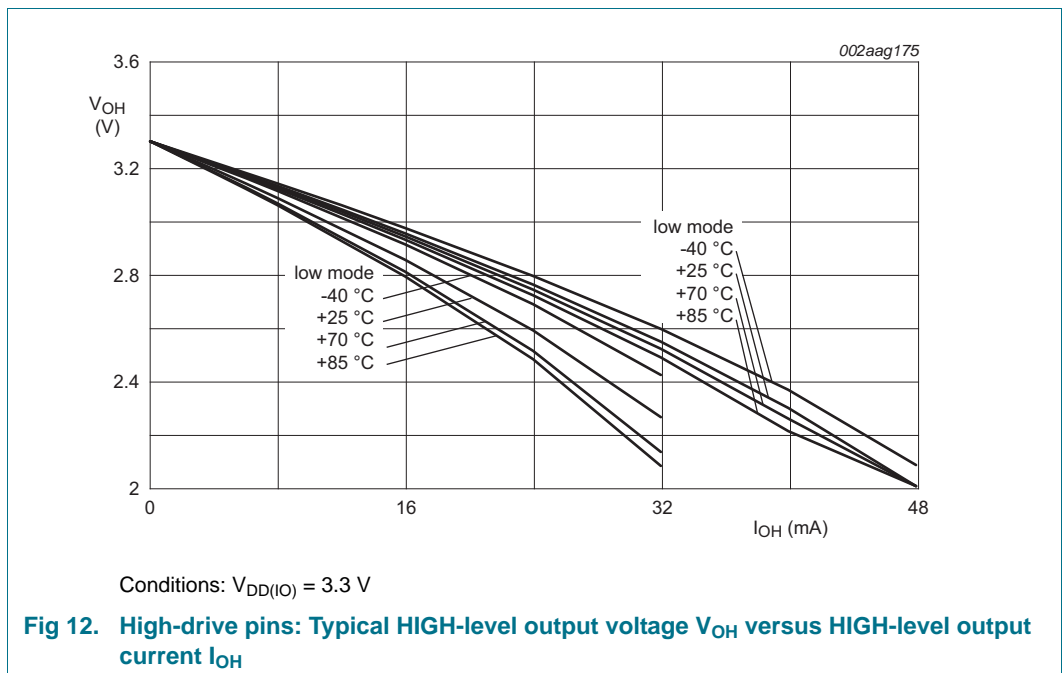


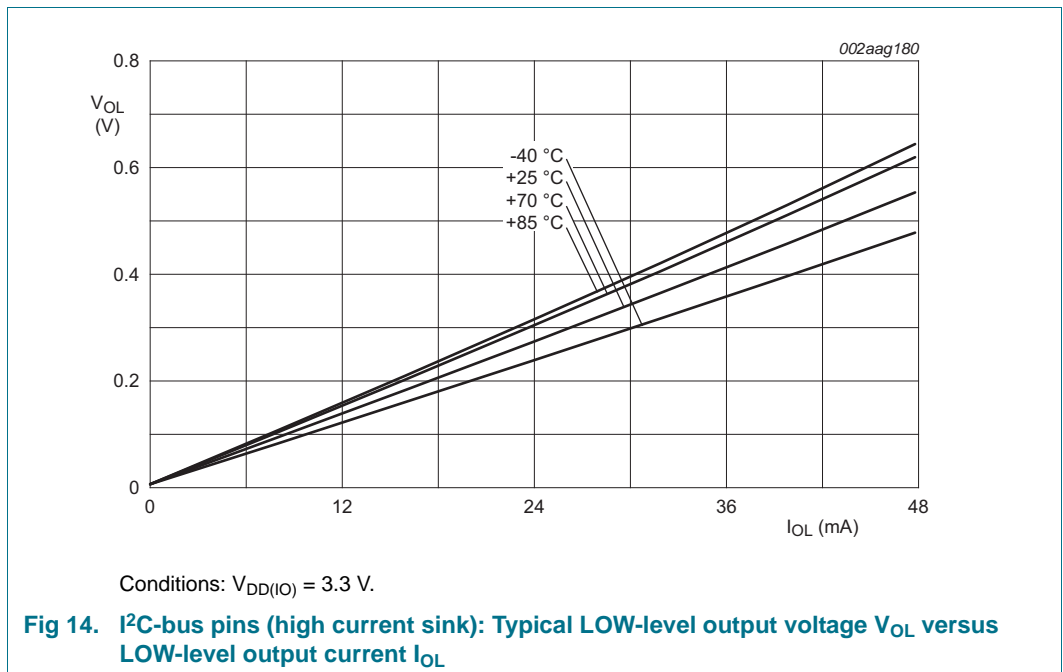
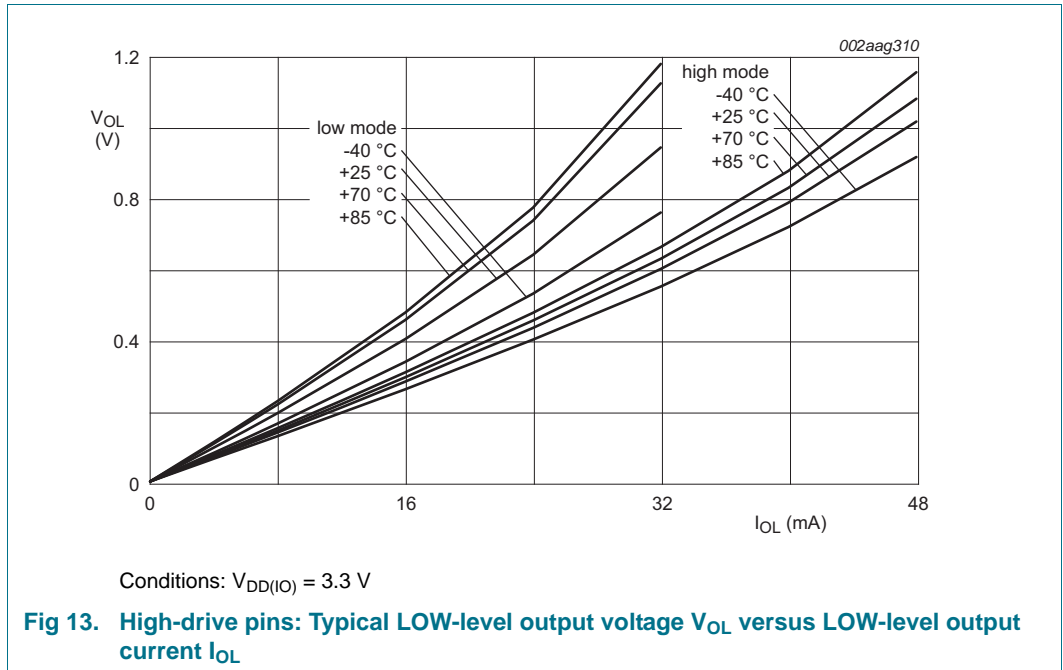


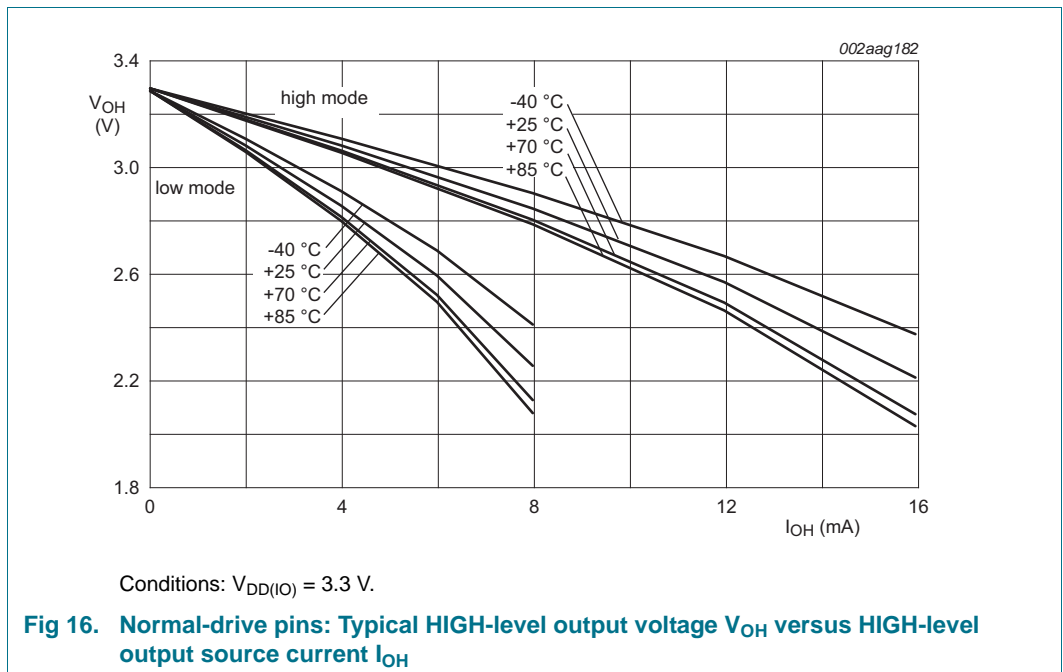
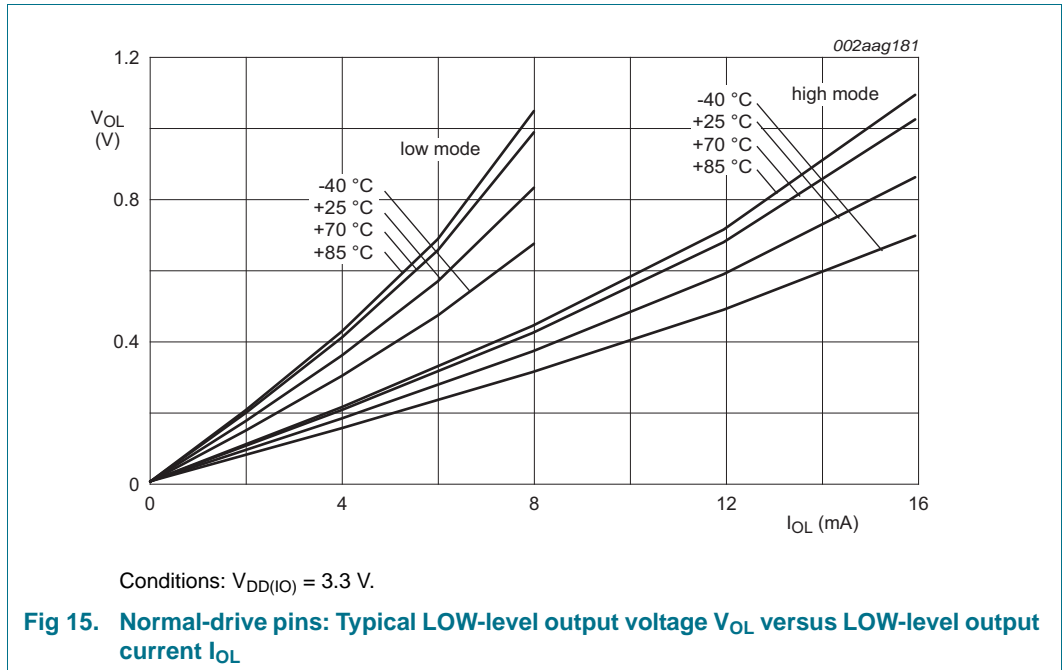


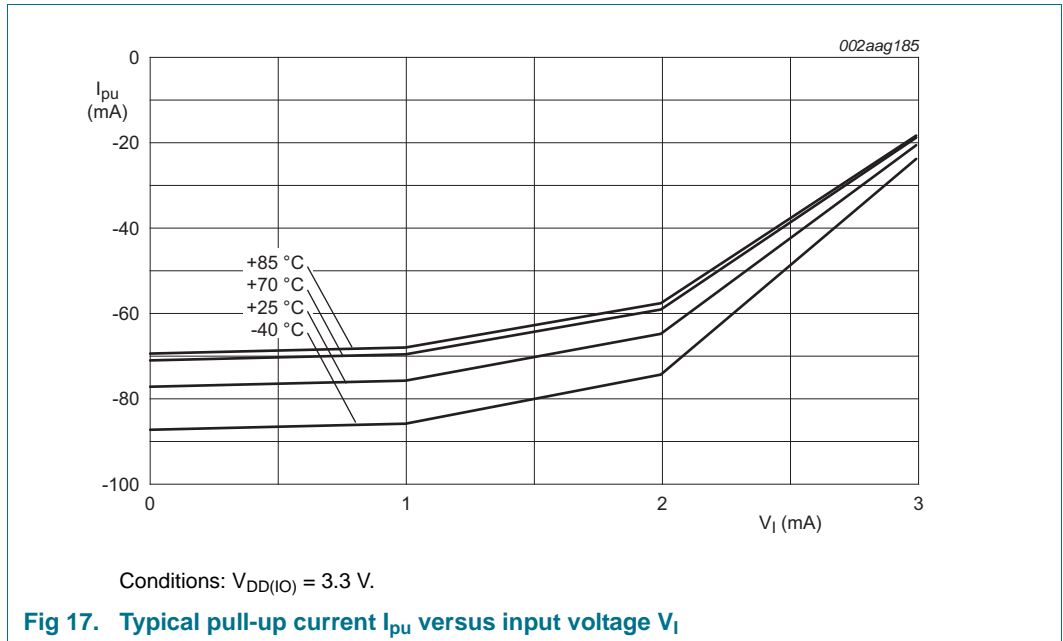


10.3 Electrical pin characteristics









10.4 ADC characteristics

Table 9. ADC static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified; ADC frequency 9 MHz, $V_{DD(3V3)} = 3.0\text{ V}$ to 3.6 V .

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--------------|------------------------------|---|-----|--------------------|---------------|-----------|
| V_{IA} | analog input voltage | | 0 | - | $V_{DD(3V3)}$ | V |
| C_{ia} | analog input capacitance | | - | - | 1 | pF |
| E_D | differential linearity error | [2] [3] [4] | - | - | ± 1 | LSB |
| $E_{L(adj)}$ | integral non-linearity | [2] [5] | - | - | ± 2.5 | LSB |
| E_O | offset error | [2] [6] | - | - | ± 1 | LSB |
| E_G | gain error | [2] [7] | - | - | ± 3 | LSB |
| E_T | absolute error | [2] [8] | - | - | ± 3 | LSB |
| $f_{c(ADC)}$ | ADC conversion frequency | | - | - | 257 | kHz |
| R_i | input resistance | [9] [10] | - | - | 3.9 | $M\Omega$ |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Conditions: $V_{SS} = 0\text{ V}$, $V_{DD(3V3)} = 3.3\text{ V}$.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 18](#).

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 18](#).

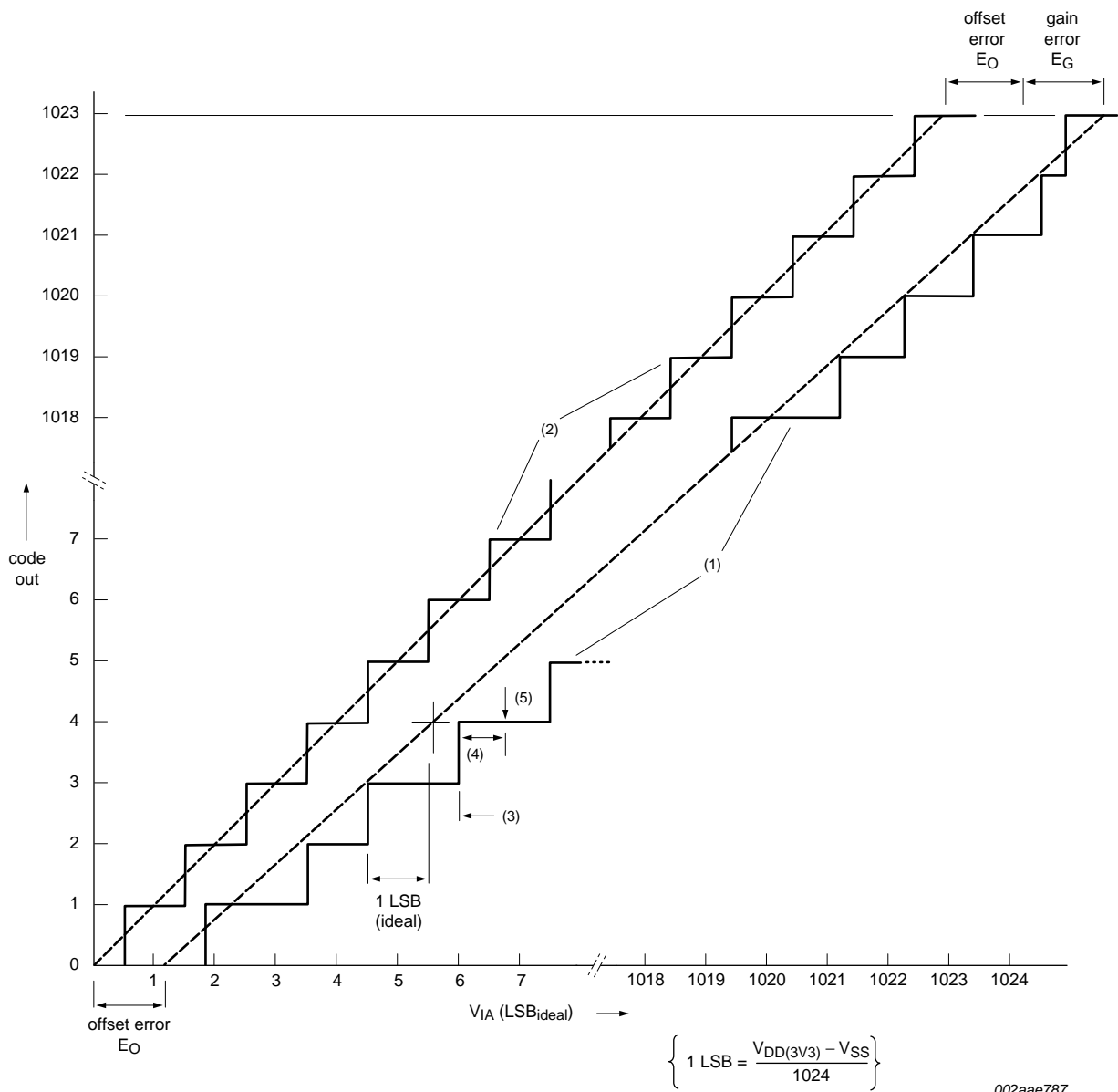
[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 18](#).

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 18](#).

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 18](#).

[9] $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum sampling frequency $f_s = 257\text{ kHz}$ and analog input capacitance $C_{ia} = 1\text{ pF}$.

[10] Input resistance R_i depends on the sampling frequency f_s : $R_i = 1 / (f_s \times C_{ia})$.



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- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E_D).
- (4) Integral non-linearity ($E_{L(adj)}$).
- (5) Center of a step of the actual transfer curve.

Fig 18. ADC characteristics

10.5 BOD static characteristics

Table 10. BOD static characteristics^[1]

$T_{amb} = 25\text{ }^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-------------------|-------------------|-----|------|-----|------|
| V_{th} | threshold voltage | interrupt level 1 | | | | |
| | | assertion | - | 2.25 | - | V |
| | | de-assertion | - | 2.39 | - | V |
| | | interrupt level 2 | | | | |
| | | assertion | - | 2.54 | - | V |
| | | de-assertion | - | 2.67 | - | V |
| | | interrupt level 3 | | | | |
| | | assertion | - | 2.83 | - | V |
| | | de-assertion | - | 2.93 | - | V |
| | | reset level 1 | | | | |
| | | assertion | - | 2.04 | - | V |
| | | de-assertion | - | 2.18 | - | V |
| | | reset level 2 | | | | |
| | | assertion | - | 2.34 | - | V |
| | | de-assertion | - | 2.47 | - | V |
| | | reset level 3 | | | | |
| | | assertion | - | 2.62 | - | V |
| | | de-assertion | - | 2.76 | - | V |

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC122x user manual*.

11. Dynamic characteristics

11.1 Power-up ramp conditions

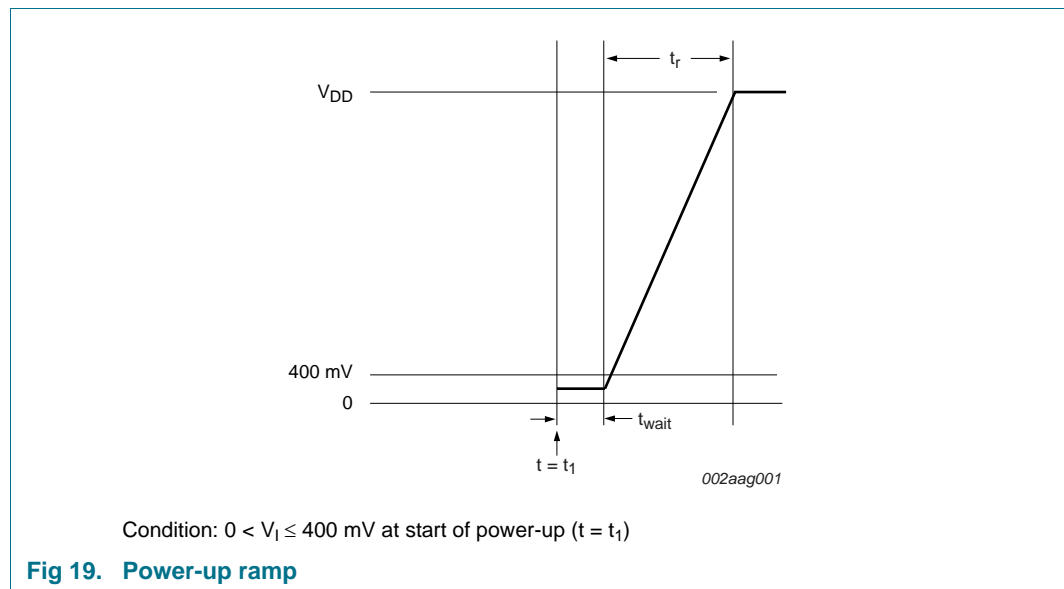
Table 11. Power-up characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|---------------|---|-----------|-----|-----|---------------|
| t_r | rise time | at $t = t_1$: $0 < V_1 \leq 400\text{ mV}$ | [1] 0 | - | 500 | ms |
| t_{wait} | wait time | | [1][2] 12 | - | - | μs |
| V_1 | input voltage | at $t = t_1$ on pin V_{DD} | 0 | - | 400 | mV |

[1] See [Figure 19](#).

[2] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.



11.2 Flash memory

Table 12. Dynamic characteristics: flash memory

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD(3V3)}$ over specified ranges.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|------------------|---------------------------------|-----------|-----|---------------|
| t_{er} | erase time | for one page (512 byte) | [1] - | 20 | ms |
| | | for one sector (4 kB) | [1] | 162 | ms |
| | | for all sectors; mass erase | [1] - | 20 | ms |
| t_{prog} | programming time | one word (4 bytes) | [1] - | 49 | μs |
| | | four sequential words | [1] - | 194 | μs |
| | | 128 bytes (one row of 32 words) | [1] - | 765 | μs |
| N_{endu} | endurance | | [2] 20000 | - | cycles |
| t_{ret} | retention time | | 10 | - | years |

[1] Erase and programming times are valid over the lifetime of the device (minimum 20000 cycles).

[2] Number of program/erase cycles.

11.3 External clock

Table 13. Dynamic characteristics: external clock

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD(3V3)}$ over specified ranges.[1]

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---------------|----------------------|------------|--------------------------|--------|------|------|
| f_{osc} | oscillator frequency | | 1 | - | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | 40 | - | 1000 | ns |
| t_{CHCX} | clock HIGH time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| t_{CLCX} | clock LOW time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| t_{CLCH} | clock rise time | | - | - | 5 | ns |
| t_{CHCL} | clock fall time | | - | - | 5 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

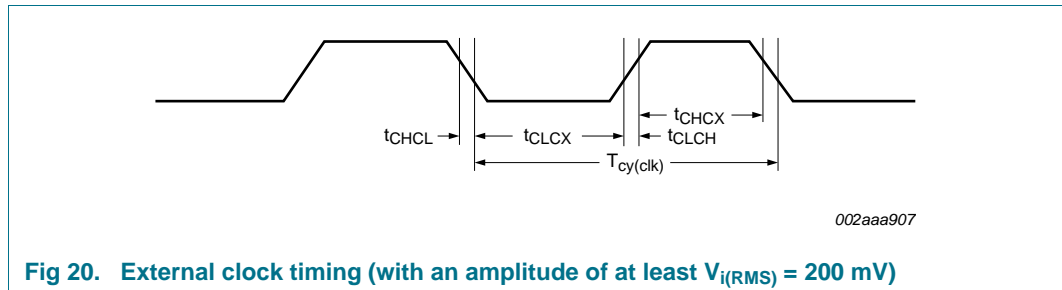


Fig 20. External clock timing (with an amplitude of at least $V_{i(RMS)} = 200\text{ mV}$)

11.4 Internal oscillators

Table 14. Dynamic characteristics: internal oscillators

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD(3V3)}$ over specified ranges.^[1]

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit |
|---------------|----------------------------------|------------|-------|--------------------|-------|------|
| $f_{osc(RC)}$ | internal RC oscillator frequency | - | 11.88 | 12 | 12.12 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

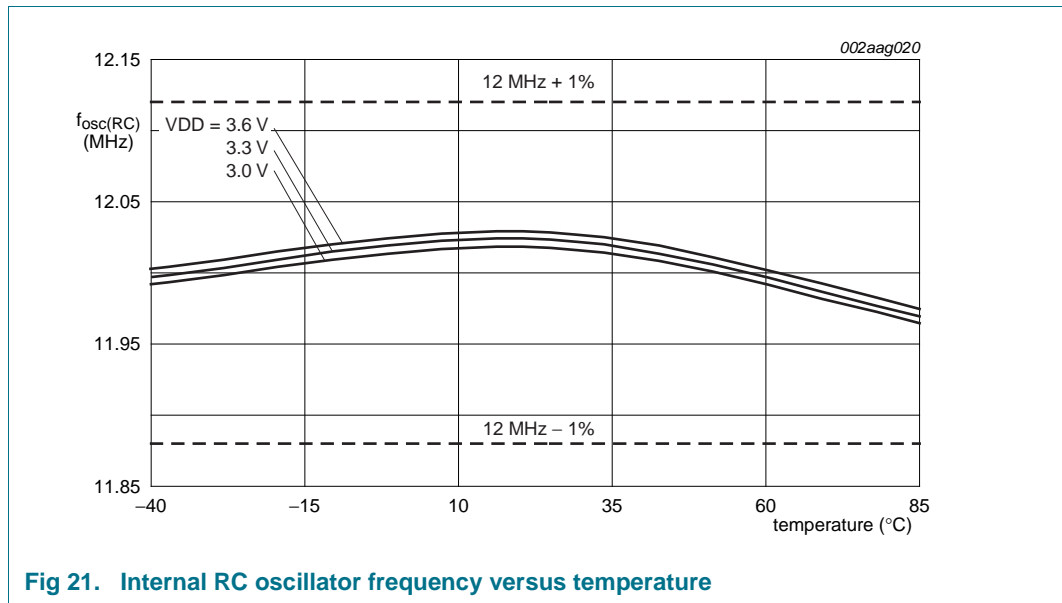


Fig 21. Internal RC oscillator frequency versus temperature

Table 15. Dynamic characteristics: Watchdog oscillator

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit | |
|----------------|-------------------------------|--|--------|--------------------|------|------|-----|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; | [2][3] | - | 7.8 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register | [2][3] | - | 1700 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$) is $\pm 40\%$.

[3] See the *LPC122x user manual*.

11.5 I²C-busTable 16. Dynamic characteristics: I²C-bus pins $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$. [1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--|-----------------------------|-----------------------|-----|---------------|
| f_{SCL} | SCL clock frequency | Standard-mode | 0 | 100 | kHz |
| | | Fast-mode | 0 | 400 | kHz |
| | | Fast-mode Plus | 0 | 1 | MHz |
| t_f | fall time [2][3][4][5] | of both SDA and SCL signals | - | 300 | ns |
| | | Standard-mode | | | |
| | | Fast-mode | $20 + 0.1 \times C_b$ | 300 | ns |
| $t_{HD;DAT}$ | data hold time [6][2][7] | Fast-mode Plus | - | 120 | ns |
| | | Standard-mode | 4.7 | - | μs |
| | | Fast-mode | 1.3 | - | μs |
| t_{HIGH} | HIGH period of the SCL clock | Fast-mode Plus | 0.5 | - | μs |
| | | Standard-mode | 4.0 | - | μs |
| | | Fast-mode | 0.6 | - | μs |
| $t_{SU;DAT}$ | data set-up time [8][9] | Fast-mode Plus | 0.26 | - | μs |
| | | Standard-mode | 0 | - | μs |
| | | Fast-mode | 0 | - | μs |
| $t_{SU;DAT}$ | data set-up time [8][9] | Standard-mode | 250 | - | ns |
| | | Fast-mode | 100 | - | ns |
| | | Fast-mode Plus | 50 | - | ns |

- [1] Parameters are valid over operating temperature range unless otherwise specified.
- [2] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}(\text{min})$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- [3] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.
- [4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f .
- [5] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- [6] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
- [7] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
- [8] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
- [9] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT} = 250\text{ ns}$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(\text{max})} + t_{SU;DAT} = 1000 + 250 = 1250\text{ ns}$ (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

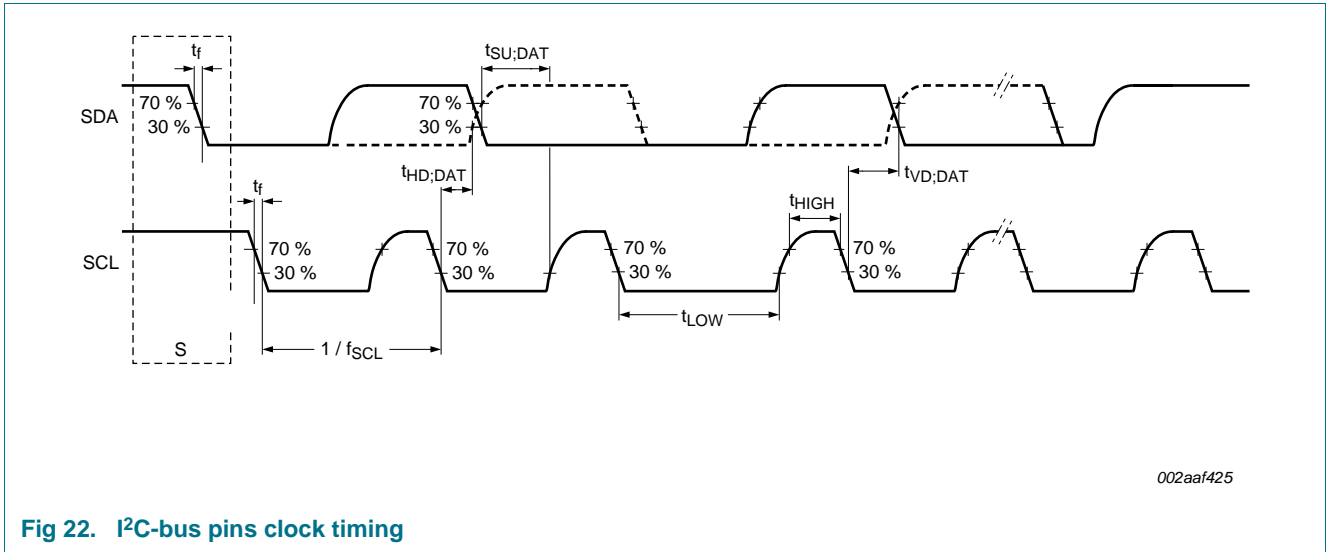


Fig 22. I²C-bus pins clock timing

12. Application information

12.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i = 100$ pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

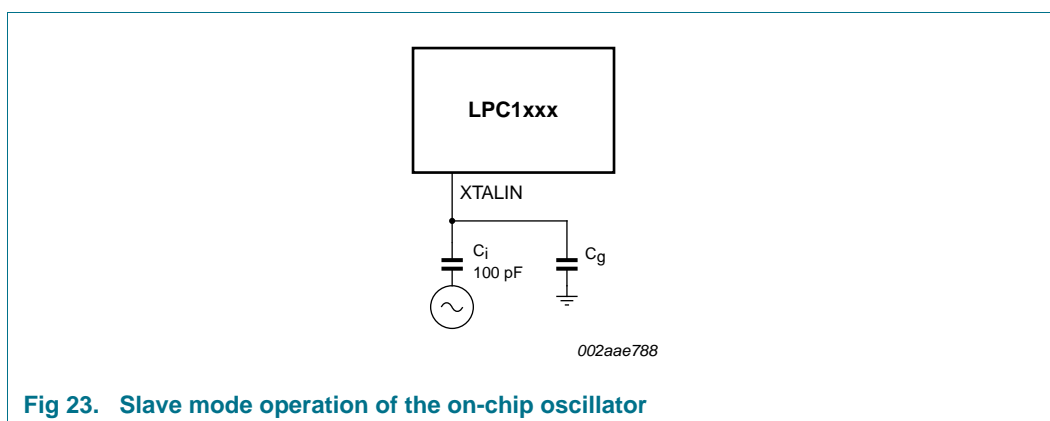


Fig 23. Slave mode operation of the on-chip oscillator

12.2 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1} , C_{x2} , and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

12.3 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1227FBD64/301 in [Table 17](#).

Table 17. ElectroMagnetic Compatibility (EMC) for part LPC1227FBD64/301 (TEM-cell method)

$V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ °C}$.

| Parameter | Frequency band | System clock = | | | Unit |
|---|------------------|----------------|--------|--------|------------|
| | | 12 MHz | 24 MHz | 33 MHz | |
| Input clock: IRC (12 MHz) | | | | | |
| maximum peak level | 150 kHz - 30 MHz | -4.2 | -3.8 | -6.4 | dB μ V |
| | 30 MHz - 150 MHz | 7.3 | 5.4 | 9 | dB μ V |
| | 150 MHz - 1 GHz | 16.4 | 20.1 | 23.4 | dB μ V |
| IEC level ^[1] | - | M | L | L | - |
| Input clock: crystal oscillator (12 MHz) | | | | | |
| maximum peak level | 150 kHz - 30 MHz | -4.8 | -4 | -6.6 | dB μ V |
| | 30 MHz - 150 MHz | 6.9 | 5.6 | 10 | dB μ V |
| | 150 MHz - 1 GHz | 16.3 | 20.3 | 22.3 | dB μ V |
| IEC level ^[1] | - | M | L | L | - |

[1] IEC levels refer to *Appendix D in the IEC61967-2 Specification*.

13. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm

SOT407-1

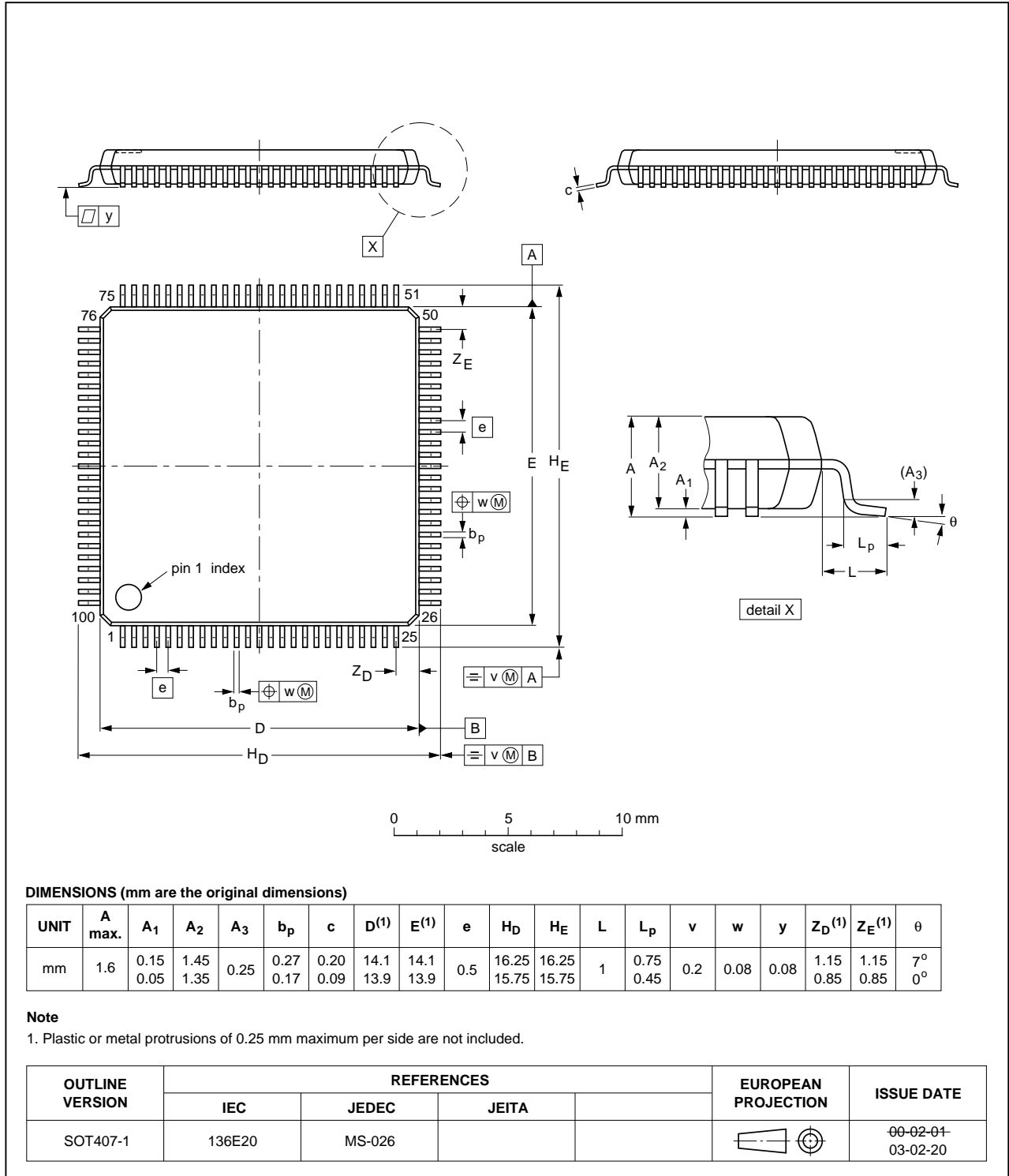


Fig 24. Package outline LQFP100

14. Soldering

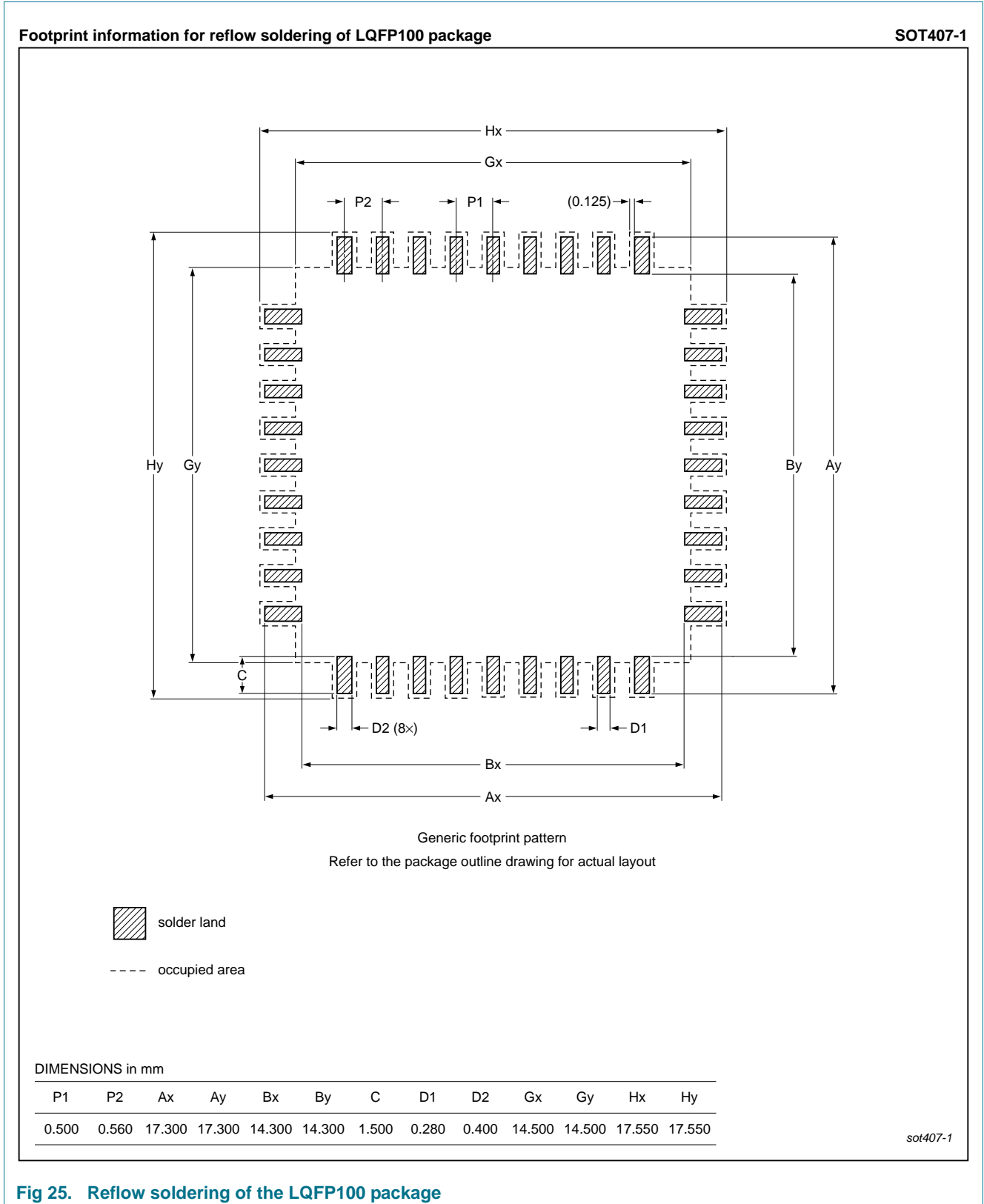


Fig 25. Reflow soldering of the LQFP100 package

15. References

- [1] *LPC122x data sheet*, <http://www.nxp.com/microcontrollers>
- [2] *PCF8576D data sheet*, <http://www.nxp.com/microcontrollers>

16. Revision history

Table 18. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------|--------------|--------------------|---------------|------------|
| LPC12D27 v.1 | 20110920 | Product data sheet | - | - |

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|-----------------------------------|-------------------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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