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LS1012A

QorIQ LS1012A Data Sheet

Features

- LS1012A contains one 64-bit Arm® Cortex®-A53 core processor with the following capabilities:
  - 256 kB L2 cache w/ECC
  - Neon SIMD Co-processor
  - Arm v8 Cryptography Extensions
  - Single-threaded cores with 32 KB L1 data cache and 32 KB L1 instruction cache, and both Neon and Precision Floating Point module support
- One 16-bit DDR3L SDRAM memory controller
  - Up to 1.0 GT/s
  - Supports 16-bit operation (no ECC support)
  - Support for x8 and x16 devices
- Packet Forwarding Engine (PFE)
- Cryptography acceleration (SEC)
- Three SerDes lanes
  - Two SerDes PLLs supported for usage by any SerDes data lane
  - Support for up to 6 Gbit/s operation
- Ethernet Interfaces supported by PFE
  - Two quad-speed Ethernet MACs supporting 2.5G, 1G, 100M, 10M
  - Support for RGMII, SGMII, 2.5G SGMII
  - Energy efficient Ethernet support (802.3 az)
- High-speed peripheral interfaces
  - One PCIe 2.0 controller, supporting x1 operation
  - One Serial ATA (SATA 3.0) controller
  - One USB 3.0/2.0 controller with integrated PHY
  - One USB 2.0 controller with ULPI interface
- Additional peripheral interfaces
  - One Quad Serial Peripheral Interface (QSPI) controller for serial Flash
  - One Serial Peripheral Interface (SPI) controller
  - Two enhanced secure digital host controllers (SD, SDIO, eMMC)
  - Two I2C controllers
  - One 16550 compliant DUART (two UART interfaces)
  - General Purpose IO (GPIO)
  - Two Flextimers
  - Five Synchronous Audio Interfaces (SAI)
- QorIQ Platform's Trust Architecture
- Debug supporting run control, data acquisition, high-speed trace, and performance/event monitoring
- Pre-boot loader (PBL) provides pre-boot initialization and RCW loading capabilities
- Single-source clocking solution enabling generation of core, platform, DDR, SerDes, and USB clocks from a single external crystal and internal crystal oscillator
- 211 FC-LGA package, 9.6 mm x 9.6 mm

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1 Overview

The LS1012A processor features an advanced 64-bit Arm® Cortex®-A53 processor core with ECC-protected L1 and L2 cache memories along with datapath acceleration and network, peripheral interfaces required for networking, wireless infrastructure, and general-purpose embedded applications.

This figure shows the block diagram of the chip.

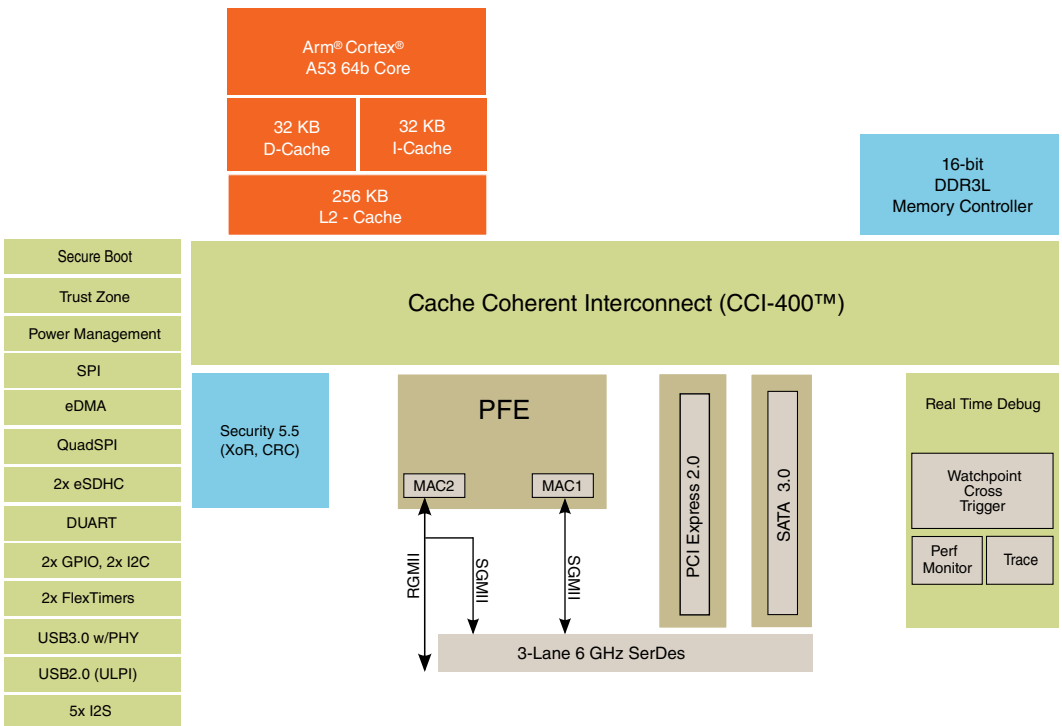

Figure 1. LS1012A block diagram

2 Pin assignments

This section describes the ball map diagram and pin list table for LS1012A.

2.1 211 LGA ball layout diagrams

This figure shows the complete view of the LS1012A LGA ball map diagram. Figure 3, Figure 4, Figure 5, and Figure 6 show quadrant views.

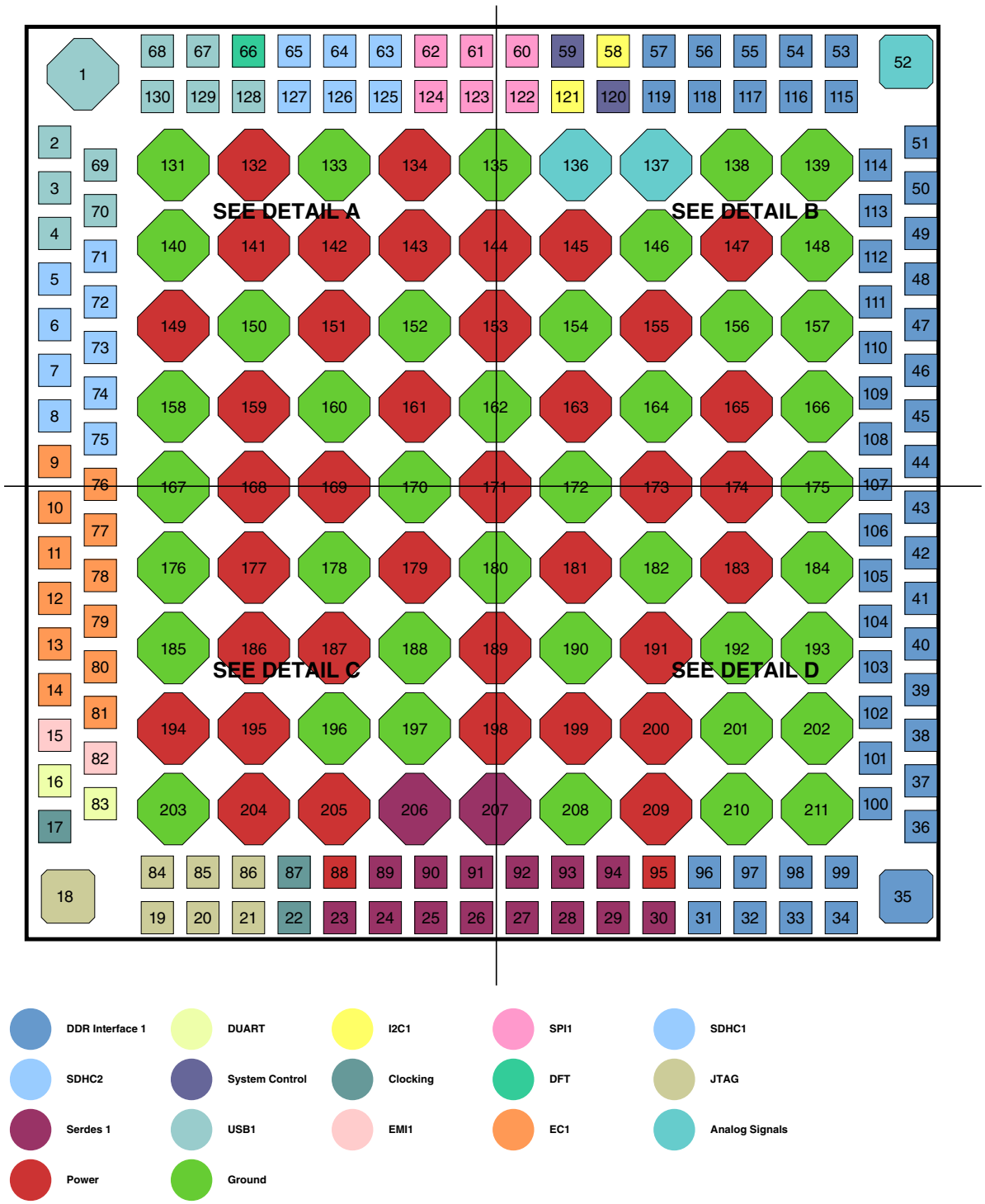

Figure 2. Complete LGA Map for the LS1012A

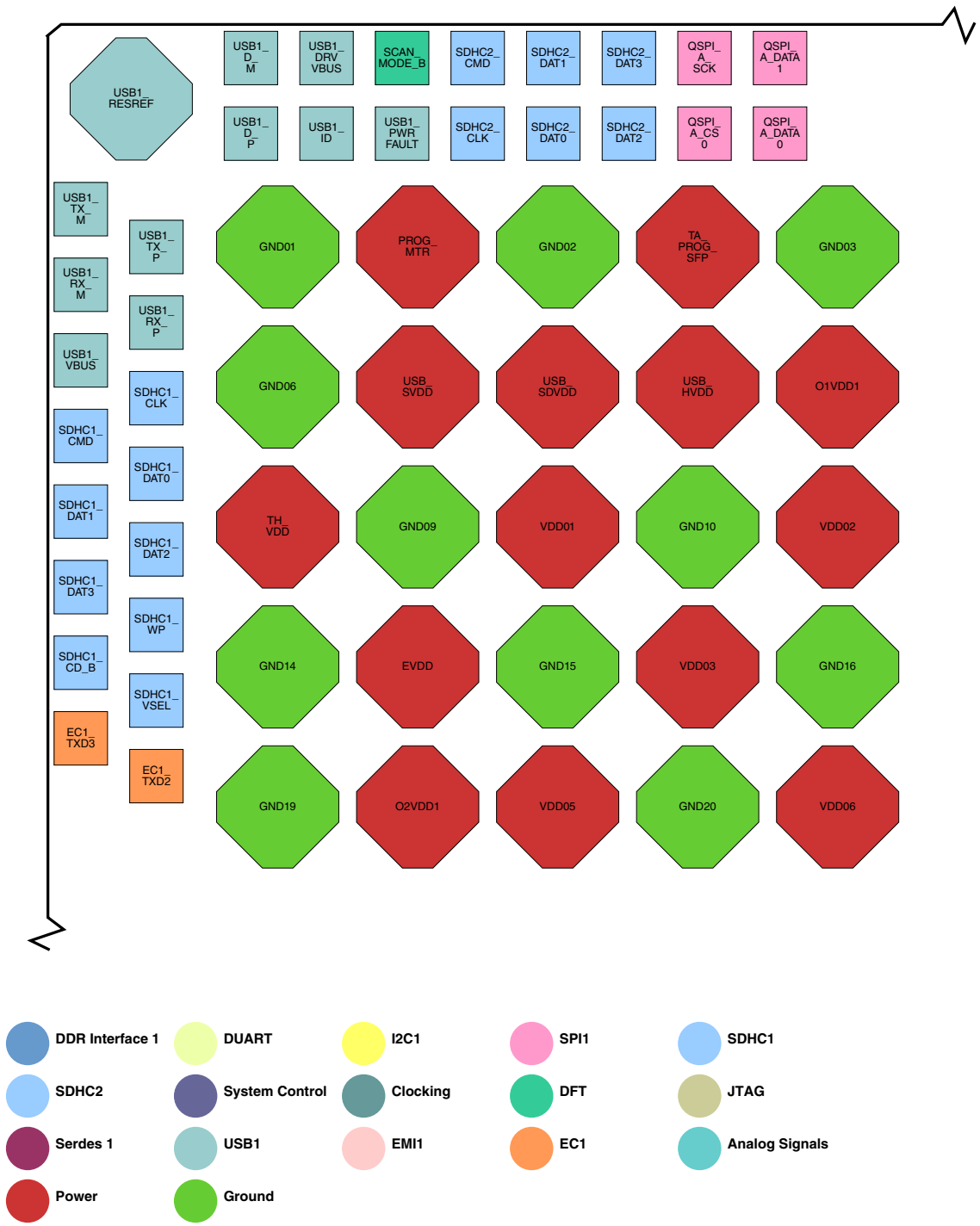

Figure 3. Detail A

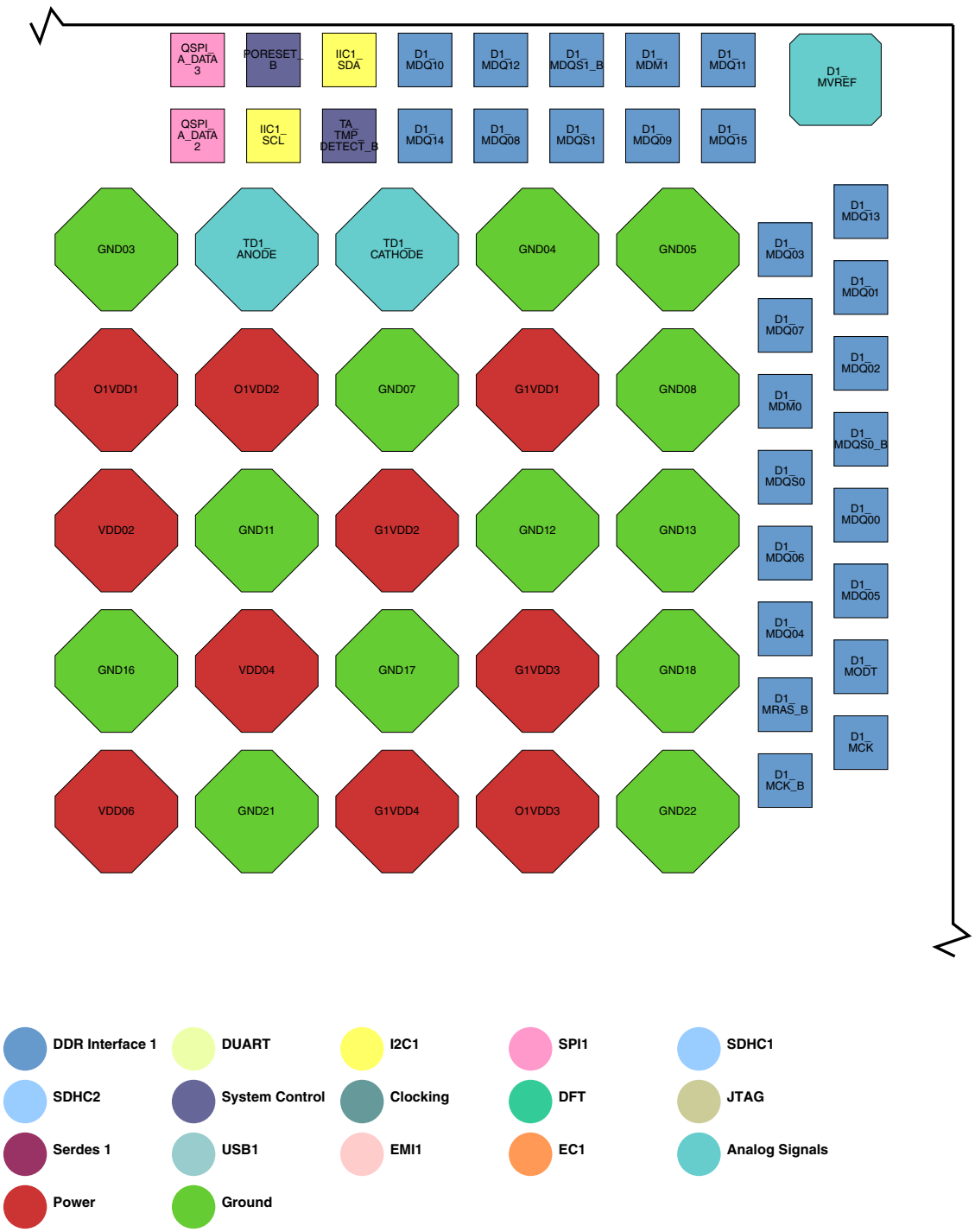

Figure 4. Detail B

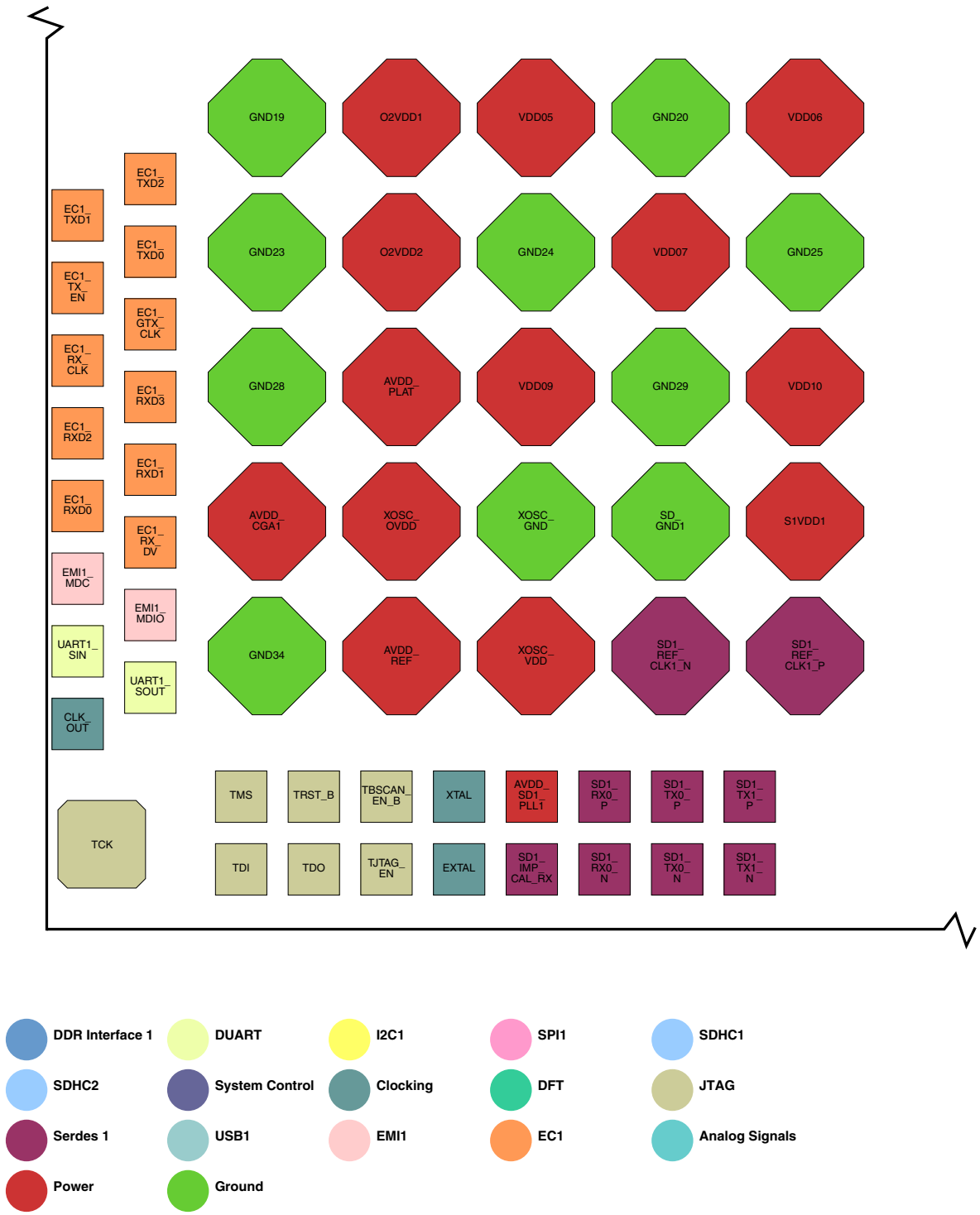

Figure 5. Detail C

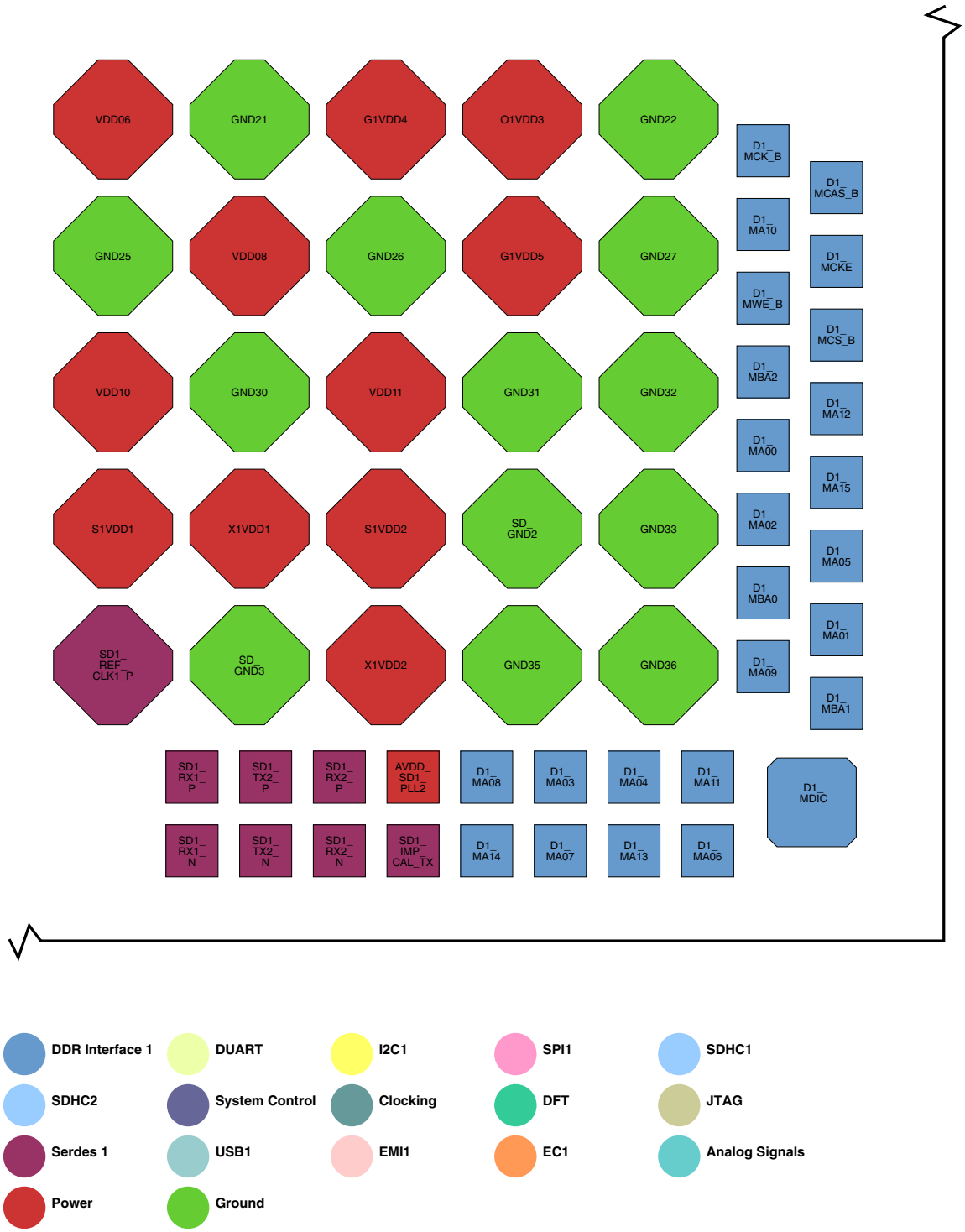

Figure 6. Detail D

2.2 Pinout list

This table provides the pinout listing for the LS1012A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	103	O	$G1V_{DD}$	---
D1_MA01	Address	37	O	$G1V_{DD}$	---
D1_MA02	Address	102	O	$G1V_{DD}$	---
D1_MA03	Address	97	O	$G1V_{DD}$	---
D1_MA04	Address	98	O	$G1V_{DD}$	---
D1_MA05	Address	38	O	$G1V_{DD}$	---
D1_MA06	Address	34	O	$G1V_{DD}$	---
D1_MA07	Address	32	O	$G1V_{DD}$	---
D1_MA08	Address	96	O	$G1V_{DD}$	---
D1_MA09	Address	100	O	$G1V_{DD}$	---
D1_MA10	Address	106	O	$G1V_{DD}$	---
D1_MA11	Address	99	O	$G1V_{DD}$	---
D1_MA12	Address	40	O	$G1V_{DD}$	---
D1_MA13	Address	33	O	$G1V_{DD}$	---
D1_MA14	Address	31	O	$G1V_{DD}$	---
D1_MA15	Address	39	O	$G1V_{DD}$	---
D1_MBA0	Bank Select	101	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	36	O	$G1V_{DD}$	---
D1_MBA2	Bank Select	104	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe	43	O	$G1V_{DD}$	---
D1_MCK	Clock	44	O	$G1V_{DD}$	---
D1_MCKE	Clock Enable	42	O	$G1V_{DD}$	2
D1_MCK_B	Clock Complement	107	O	$G1V_{DD}$	---
D1_MCS_B	Chip Select	41	O	$G1V_{DD}$	---
D1_MDIC	Driver Impedence Calibration	35	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	112	O	$G1V_{DD}$	---
D1_MDM1	Data Mask	54	O	$G1V_{DD}$	---
D1_MDQ00	Data	47	IO	$G1V_{DD}$	---
D1_MDQ01	Data	50	IO	$G1V_{DD}$	---
D1_MDQ02	Data	49	IO	$G1V_{DD}$	---
D1_MDQ03	Data	114	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ04	Data	109	IO	$G1V_{DD}$	---
D1_MDQ05	Data	46	IO	$G1V_{DD}$	---
D1_MDQ06	Data	110	IO	$G1V_{DD}$	---
D1_MDQ07	Data	113	IO	$G1V_{DD}$	---
D1_MDQ08	Data	118	IO	$G1V_{DD}$	---
D1_MDQ09	Data	116	IO	$G1V_{DD}$	---
D1_MDQ10	Data	57	IO	$G1V_{DD}$	---
D1_MDQ11	Data	53	IO	$G1V_{DD}$	---
D1_MDQ12	Data	56	IO	$G1V_{DD}$	---
D1_MDQ13	Data	51	IO	$G1V_{DD}$	---
D1_MDQ14	Data	119	IO	$G1V_{DD}$	---
D1_MDQ15	Data	115	IO	$G1V_{DD}$	---
D1_MDQS0	Data Strobe	111	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	48	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	117	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	55	IO	$G1V_{DD}$	---
D1_MODT	On Die Termination	45	O	$G1V_{DD}$	2
D1_MRAS_B	Row Address Strobe	108	O	$G1V_{DD}$	---
D1_MWE_B	Write Enable	105	O	$G1V_{DD}$	---
DUART					
UART1_SIN/GPIO1_01	Receive Data	16	I	$O2V_{DD}$	1
UART1_SOUT/GPIO1_00/ cfg_eng_use	Transmit Data	83	O	$O2V_{DD}$	1, 4, 23
UART2_CTS_B/**TMS**/ GPIO1_09/SAI5_TX_SYNC/ SAI5_RX_SYNC	Clear to send	84	I	$O2V_{DD}$	1
UART2_RTS_B/**TDI**/ GPIO1_07/SAI5_TX_DATA/ SAI5_RX_DATA	Request to send	19	O	$O2V_{DD}$	1
UART2_SIN/**TCK**/GPIO1_06	Receive Data	18	I	$O2V_{DD}$	1
UART2_SOUT/**TDO**/ GPIO1_08	Transmit Data	20	O	$O2V_{DD}$	1
IIC1					
IIC1_SCL/GPIO1_02/ FTM1_CH0	Serial Clock	121	IO	$O1V_{DD}$	7, 8
IIC1_SDA/GPIO1_03/ FTM2_CH0	Serial Data	58	IO	$O1V_{DD}$	7, 8
IIC2					
IIC2_SCL/**QSPI_A_DATA2**/ GPIO1_13	Serial Clock	122	IO	$O1V_{DD}$	7, 8

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IIC2_SDA/**QSPI_A_DATA3**/ GPIO1_14/RESET_REQ_B	Serial Data	60	IO	$O1V_{DD}$	7, 8
QSPI					
QSPI_A_CS0/GPIO1_05/ cfg_sysclk_sel	QSPI Chip Select	124	O	$O1V_{DD}$	1, 4, 31
QSPI_A_DATA0/GPIO1_11/ cfg_eng_use2	QSPI DATA 0	123	IO	$O1V_{DD}$	1, 4, 23
QSPI_A_DATA1/GPIO1_12/ cfg_func_backup	QSPI DATA 1	61	IO	$O1V_{DD}$	1, 4
QSPI_A_DATA2/GPIO1_13/ IIC2_SCL	QSPI DATA 2	122	IO	$O1V_{DD}$	6
QSPI_A_DATA3/GPIO1_14/ IIC2_SDA/RESET_REQ_B	QSPI DATA 3	60	IO	$O1V_{DD}$	6
QSPI_A_SCK/GPIO1_04	QSPI Clock	62	O	$O1V_{DD}$	1, 5
Serial Peripheral Interface					
SPI_CLK/**SDHC2_CLK**/ GPIO1_29/FTM2_CH3/ SAI1_TX_DATA	SPI Clock	127	O	$O1V_{DD}$	1, 5
SPI_CS0_B/**SDHC2_DAT0**/ GPIO1_25/FTM1_CH3/ SAI1_RX_SYNC	Chip Select 0	126	O	$O1V_{DD}$	1
SPI_CS1_B/**SDHC2_DAT1**/ GPIO1_26/FTM2_CH2/ SAI1_TX_BCLK	Chip Select 1	64	O	$O1V_{DD}$	1
SPI_CS2_B/**SDHC2_DAT2**/ GPIO1_27/FTM1_CH2/ SAI1_TX_SYNC	Chip Select 2	125	O	$O1V_{DD}$	1
SPI_MISO/**SDHC2_DAT3**/ GPIO1_28/FTM2_CH1/ SAI1_RX_BCLK	Master in slave out	63	I	$O1V_{DD}$	1
SPI_MOSI/**SDHC2_CMD**/ GPIO1_24/FTM1_CH1/ SAI1_RX_DATA	Master out slave in	65	O	$O1V_{DD}$	1
eSDHC 1					
SDHC1_CD_B/GPIO1_21	SDHC Card Detect (active-low)	8	I	$O2V_{DD}$	1, 22
SDHC1_CLK/GPIO1_20	Host to Card Clock	71	O	EV_{DD}	1, 5
SDHC1_CMD/GPIO1_15	Command/Response	5	IO	EV_{DD}	28
SDHC1_DAT0/GPIO1_16	Data	72	IO	EV_{DD}	28
SDHC1_DAT1/GPIO1_17	Data	6	IO	EV_{DD}	28
SDHC1_DAT2/GPIO1_18	Data	73	IO	EV_{DD}	28
SDHC1_DAT3/GPIO1_19	Data	7	IO	EV_{DD}	28
SDHC1_VSEL/GPIO1_23	SDHC Voltage Select	75	O	$O2V_{DD}$	1
SDHC1_WP/GPIO1_22	SDHC Write Protect	74	I	$O2V_{DD}$	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
eSDHC 2					
SDHC2_CLK/GPIO1_29/ FTM2_CH3/SAI1_TX_DATA/ SPI_CLK	Host to Card Clock	127	O	$O1V_{DD}$	1, 5
SDHC2_CMD/GPIO1_24/ FTM1_CH1/SAI1_RX_DATA/ SPI_MOSI	Command/Response	65	IO	$O1V_{DD}$	29
SDHC2_DAT0/GPIO1_25/ FTM1_CH3/SAI1_RX_SYNC/ SPI_CS0_B	Data	126	IO	$O1V_{DD}$	29
SDHC2_DAT1/GPIO1_26/ FTM2_CH2/SAI1_TX_BCLK/ SPI_CS1_B	Data	64	IO	$O1V_{DD}$	29
SDHC2_DAT2/GPIO1_27/ FTM1_CH2/SAI1_TX_SYNC/ SPI_CS2_B	Data	125	IO	$O1V_{DD}$	29
SDHC2_DAT3/GPIO1_28/ FTM2_CH1/SAI1_RX_BCLK/ SPI_MISO	Data	63	IO	$O1V_{DD}$	29
System Control					
ASLEEP/**USB1_PWRFAULT**/ GPIO2_01	ASLEEP	128	O	$O1V_{DD}$	1
PORESET_B	Power On Reset	59	I	$O1V_{DD}$	19, 21
RESET_REQ_B/**CLK_OUT**/ GPIO1_31/cfg_rcw_src	Reset Request	17	O	$O2V_{DD}$	1, 4, 30
RESET_REQ_B/ **QSPI_A_DATA3**/GPIO1_14/ IIC2_SDA	Reset Request	60	O	$O1V_{DD}$	1
TA_TMP_DETECT_B/ GPIO2_17	Tamper Detect	120	I	$O1V_{DD}$	---
Clocking					
CLK_OUT/GPIO1_31/ cfg_rcw_src/RESET_REQ_B	Output clock	17	O	$O2V_{DD}$	1, 4
EXTAL	25 MHz Crystal/Clock Input	22	I	$XOSC\_OV_{DD}$	---
XTAL	Crystal Osc output	87	O	$XOSC\_OV_{DD}$	24
DFT					
SCAN_MODE_B	Reserved	66	I	$O1V_{DD}$	10, 21
JTAG					
TBSCAN_EN_B/GPIO1_30/ FTM_EXTCLK	An IEEE 1149.1 JTAG compliance enable pin. 0: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL. 1: JTAG connects to	86	I	$O2V_{DD}$	21, 26

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
	DAP controller for the ARM core debug.				
TCK/GPIO1_06/UART2_SIN	Test Clock	18	I	$O2V_{DD}$	---
TDI/GPIO1_07/ UART2_RTS_B/ SAI5_TX_DATA/ SAI5_RX_DATA	Test Data In	19	I	$O2V_{DD}$	9
TDO/GPIO1_08/ UART2_SOUT	Test Data Out	20	O	$O2V_{DD}$	---
TJTAG_EN	Selection for JTAG IOs	21	I	$O2V_{DD}$	20, 21
TMS/GPIO1_09/ UART2_CTS_B/ SAI5_TX_SYNC/ SAI5_RX_SYNC	Test Mode Select	84	I	$O2V_{DD}$	9
TRST_B/GPIO1_10/ SAI5_TX_BCLK/ SAI5_RX_BCLK	Test Reset	85	I	$O2V_{DD}$	9
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	23	I	$S1V_{DD}$	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	30	I	$X1V_{DD}$	16
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	206	I	$S1V_{DD}$	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	207	I	$S1V_{DD}$	---
SD1_RX0_N	SerDes Receive Data (negative)	24	I	$S1V_{DD}$	---
SD1_RX0_P	SerDes Receive Data (positive)	89	I	$S1V_{DD}$	---
SD1_RX1_N	SerDes Receive Data (negative)	27	I	$S1V_{DD}$	---
SD1_RX1_P	SerDes Receive Data (positive)	92	I	$S1V_{DD}$	---
SD1_RX2_N	SerDes Receive Data (negative)	29	I	$S1V_{DD}$	---
SD1_RX2_P	SerDes Receive Data (positive)	94	I	$S1V_{DD}$	---
SD1_TX0_N	SerDes Transmit Data (negative)	25	O	$X1V_{DD}$	---
SD1_TX0_P	SerDes Transmit Data (positive)	90	O	$X1V_{DD}$	---
SD1_TX1_N	SerDes Transmit Data (negative)	26	O	$X1V_{DD}$	---
SD1_TX1_P	SerDes Transmit Data (positive)	91	O	$X1V_{DD}$	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_TX2_N	SerDes Transmit Data (negative)	28	O	$X1V_{DD}$	---
SD1_TX2_P	SerDes Transmit Data (positive)	93	O	$X1V_{DD}$	---
USB PHY					
USB1_DRVVBUS/GPIO2_00	USB PHY Digital signal - Drive VBUS	67	O	$O1V_{DD}$	1
USB1_D_M	USB PHY Data Minus	68	IO	-	---
USB1_D_P	USB PHY Data Plus	130	IO	-	---
USB1_ID	USB PHY ID Detect	129	I	-	---
USB1_PWRFAULT/ GPIO2_01/ASLEEP	USB PHY Digital signal - Power Fault	128	I	$O1V_{DD}$	1
USB1_RESREF	USB PHY Impedance Calibration	1	IO	-	27
USB1_RX_M	USB PHY SS Receive Data (negative)	3	I	-	---
USB1_RX_P	USB PHY SS Receive Data (positive)	70	I	-	---
USB1_TX_M	USB PHY SS Transmit Data (negative)	2	O	-	---
USB1_TX_P	USB PHY SS Transmit Data (positive)	69	O	-	---
USB1_VBUS	USB PHY VBUS	4	I	-	---
USB 2.0 ULPI					
USB2_CLK/**EC1_TX_EN**/ GPIO2_06/SAI2_TX_SYNC	USB Clock	11	I	$O2V_{DD}$	1
USB2_D0/**EC1_TXD3**/ GPIO2_02/SAI4_TX_DATA/ SAI4_RX_DATA	USB Data	9	IO	$O2V_{DD}$	---
USB2_D1/**EC1_TXD2**/ GPIO2_03/SAI3_TX_DATA/ SAI3_RX_DATA	USB Data	76	IO	$O2V_{DD}$	---
USB2_D2/**EC1_TXD1**/ GPIO2_04/SAI2_TX_DATA	USB Data	10	IO	$O2V_{DD}$	---
USB2_D3/**EC1_TXD0**/ GPIO2_05/SAI2_RX_DATA	USB Data	77	IO	$O2V_{DD}$	---
USB2_D4/**EC1_GTX_CLK**/ GPIO2_07/SAI2_TX_BCLK	USB Data	78	IO	$O2V_{DD}$	---
USB2_D5/**EC1_RX_CLK**/ GPIO2_13/SAI4_TX_SYNC/ SAI4_RX_SYNC	USB Data	12	IO	$O2V_{DD}$	---
USB2_D6/**EC1_RXD3**/ GPIO2_09/SAI2_RX_SYNC	USB Data	79	IO	$O2V_{DD}$	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB2_D7/**EC1_RXD2**/ GPIO2_10/SAI2_RX_BCLK	USB Data	13	IO	$O2V_{DD}$	---
USB2_DIR/**EC1_RX_DV**/ GPIO2_14/SAI4_TX_BCLK/ SAI4_RX_BCLK	USB Direction	81	I	$O2V_{DD}$	1
USB2_NXT/**EC1_RXD1**/ GPIO2_11/SAI3_TX_SYNC/ SAI3_RX_SYNC	USB ULPI next data	80	I	$O2V_{DD}$	1
USB2_STP/**EC1_RXD0**/ GPIO2_12/SAI3_TX_BCLK/ SAI3_RX_BCLK	USB ULPI stop	14	O	$O2V_{DD}$	1
Ethernet Management Interface 1					
EMI1_MDC/GPIO2_15	Management Data Clock	15	O	$O2V_{DD}$	1, 5
EMI1_MDIO/GPIO2_16	Management Data In/Out	82	IO	$O2V_{DD}$	---
Ethernet Controller 1					
EC1_GTX_CLK/GPIO2_07/ SAI2_TX_BCLK/USB2_D4	Transmit Clock Out	78	O	$O2V_{DD}$	1
EC1_RXD0/GPIO2_12/ SAI3_TX_BCLK/ SAI3_RX_BCLK/USB2_STP	Receive Data	14	I	$O2V_{DD}$	1
EC1_RXD1/GPIO2_11/ SAI3_TX_SYNC/ SAI3_RX_SYNC/USB2_NXT	Receive Data	80	I	$O2V_{DD}$	1
EC1_RXD2/GPIO2_10/ SAI2_RX_BCLK/USB2_D7	Receive Data	13	I	$O2V_{DD}$	1
EC1_RXD3/GPIO2_09/ SAI2_RX_SYNC/USB2_D6	Receive Data	79	I	$O2V_{DD}$	1
EC1_RX_CLK/GPIO2_13/ SAI4_TX_SYNC/ SAI4_RX_SYNC/USB2_D5	Receive Clock	12	I	$O2V_{DD}$	1
EC1_RX_DV/GPIO2_14/ SAI4_TX_BCLK/ SAI4_RX_BCLK/USB2_DIR	Receive Data Valid	81	I	$O2V_{DD}$	1
EC1_TXD0/GPIO2_05/ SAI2_RX_DATA/USB2_D3	Transmit Data	77	O	$O2V_{DD}$	1
EC1_TXD1/GPIO2_04/ SAI2_TX_DATA/USB2_D2	Transmit Data	10	O	$O2V_{DD}$	1
EC1_TXD2/GPIO2_03/ SAI3_TX_DATA/ SAI3_RX_DATA/USB2_D1	Transmit Data	76	O	$O2V_{DD}$	1
EC1_TXD3/GPIO2_02/ SAI4_TX_DATA/ SAI4_RX_DATA/USB2_D0	Transmit Data	9	O	$O2V_{DD}$	1
EC1_TX_EN/GPIO2_06/ SAI2_TX_SYNC/USB2_CLK	Transmit Enable	11	O	$O2V_{DD}$	1, 14

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
Analog Signals					
D1_MVREF	SSTL Reference Voltage	52	-	$G1V_{DD}/2$	---
TD1_ANODE	Thermal diode anode	136	IO	-	17
TD1_CATHODE	Thermal diode cathode	137	IO	-	17
General Purpose Input/Output					
GPIO1_00/**UART1_SOUT**/ cfg_eng_use	General Purpose Input/Output	83	O	$O2V_{DD}$	1, 4, 23
GPIO1_01/**UART1_SIN**	General Purpose Input/Output	16	IO	$O2V_{DD}$	---
GPIO1_02/**IIC1_SCL**/ FTM1_CH0	General Purpose Input/Output	121	IO	$O1V_{DD}$	---
GPIO1_03/**IIC1_SDA**/ FTM2_CH0	General Purpose Input/Output	58	IO	$O1V_{DD}$	---
GPIO1_04/**QSPI_A_SCK**	General Purpose Input/Output	62	O	$O1V_{DD}$	1, 5
GPIO1_05/**QSPI_A_CS0**/ cfg_sysclk_sel	General Purpose Input/Output	124	O	$O1V_{DD}$	1, 4, 31
GPIO1_06/**TCK**/UART2_SIN	General Purpose Input/Output	18	IO	$O2V_{DD}$	---
GPIO1_07/**TDI**/ UART2_RTS_B/ SAI5_TX_DATA/ SAI5_RX_DATA	General Purpose Input/Output	19	IO	$O2V_{DD}$	---
GPIO1_08/**TDO**/ UART2_SOUT	General Purpose Input/Output	20	IO	$O2V_{DD}$	---
GPIO1_09/**TMS**/ UART2_CTS_B/ SAI5_TX_SYNC/ SAI5_RX_SYNC	General Purpose Input/Output	84	IO	$O2V_{DD}$	---
GPIO1_10/**TRST_B**/ SAI5_TX_BCLK/ SAI5_RX_BCLK	General Purpose Input/Output	85	IO	$O2V_{DD}$	---
GPIO1_11/**QSPI_A_DATA0**/ cfg_eng_use2	General Purpose Input/Output	123	O	$O1V_{DD}$	1, 4, 23
GPIO1_12/**QSPI_A_DATA1**/ cfg_func_backup	General Purpose Input/Output	61	O	$O1V_{DD}$	1, 4
GPIO1_13/**QSPI_A_DATA2**/ IIC2_SCL	General Purpose Input/Output	122	IO	$O1V_{DD}$	---
GPIO1_14/**QSPI_A_DATA3**/ IIC2_SDA/RESET_REQ_B	General Purpose Input/Output	60	IO	$O1V_{DD}$	---
GPIO1_15/**SDHC1_CMD**	General Purpose Input/Output	5	IO	EV_{DD}	---
GPIO1_16/**SDHC1_DAT0**	General Purpose Input/Output	72	IO	EV_{DD}	---
GPIO1_17/**SDHC1_DAT1**	General Purpose Input/Output	6	IO	EV_{DD}	---
GPIO1_18/**SDHC1_DAT2**	General Purpose Input/Output	73	IO	EV_{DD}	---
GPIO1_19/**SDHC1_DAT3**	General Purpose Input/Output	7	IO	EV_{DD}	---
GPIO1_20/**SDHC1_CLK**	General Purpose Input/Output	71	O	EV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO1_21/**SDHC1_CD_B**	General Purpose Input/Output	8	IO	$O2V_{DD}$	22
GPIO1_22/**SDHC1_WP**	General Purpose Input/Output	74	IO	$O2V_{DD}$	---
GPIO1_23/**SDHC1_VSEL**	General Purpose Input/Output	75	O	$O2V_{DD}$	---
GPIO1_24/**SDHC2_CMD**/ FTM1_CH1/SAI1_RX_DATA/ SPI_MOSI	General Purpose Input/Output	65	IO	$O1V_{DD}$	---
GPIO1_25/**SDHC2_DAT0**/ FTM1_CH3/SAI1_RX_SYNC/ SPI_CS0_B	General Purpose Input/Output	126	IO	$O1V_{DD}$	---
GPIO1_26/**SDHC2_DAT1**/ FTM2_CH2/SAI1_TX_BCLK/ SPI_CS1_B	General Purpose Input/Output	64	IO	$O1V_{DD}$	---
GPIO1_27/**SDHC2_DAT2**/ FTM1_CH2/SAI1_TX_SYNC/ SPI_CS2_B	General Purpose Input/Output	125	IO	$O1V_{DD}$	---
GPIO1_28/**SDHC2_DAT3**/ FTM2_CH1/SAI1_RX_BCLK/ SPI_MISO	General Purpose Input/Output	63	IO	$O1V_{DD}$	---
GPIO1_29/**SDHC2_CLK**/ FTM2_CH3/SAI1_TX_DATA/ SPI_CLK	General Purpose Input/Output	127	O	$O1V_{DD}$	1, 5
GPIO1_30/**TBSCAN_EN_B**/ FTM_EXTCLK	General Purpose Input/Output	86	IO	$O2V_{DD}$	21, 26
GPIO1_31/**CLK_OUT**/ cfg_rcw_src/RESET_REQ_B	General Purpose Input/Output	17	O	$O2V_{DD}$	1, 4
GPIO2_00/**USB1_DRVVBUS**	General Purpose Input/Output	67	O	$O1V_{DD}$	---
GPIO2_01/ **USB1_PWRFAULT**/ASLEEP	General Purpose Input/Output	128	IO	$O1V_{DD}$	---
GPIO2_02/**EC1_TXD3**/ SAI4_TX_DATA/ SAI4_RX_DATA/USB2_D0	General Purpose Input/Output	9	IO	$O2V_{DD}$	---
GPIO2_03/**EC1_TXD2**/ SAI3_TX_DATA/ SAI3_RX_DATA/USB2_D1	General Purpose Input/Output	76	IO	$O2V_{DD}$	---
GPIO2_04/**EC1_TXD1**/ SAI2_TX_DATA/USB2_D2	General Purpose Input/Output	10	IO	$O2V_{DD}$	---
GPIO2_05/**EC1_TXD0**/ SAI2_RX_DATA/USB2_D3	General Purpose Input/Output	77	IO	$O2V_{DD}$	---
GPIO2_06/**EC1_TX_EN**/ SAI2_TX_SYNC/USB2_CLK	General Purpose Input/Output	11	IO	$O2V_{DD}$	---
GPIO2_07/**EC1_GTX_CLK**/ SAI2_TX_BCLK/USB2_D4	General Purpose Input/Output	78	IO	$O2V_{DD}$	---
GPIO2_09/**EC1_RXD3**/ SAI2_RX_SYNC/USB2_D6	General Purpose Input/Output	79	IO	$O2V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_10/**EC1_RXD2**/ SAI2_RX_BCLK/USB2_D7	General Purpose Input/Output	13	IO	$O2V_{DD}$	---
GPIO2_11/**EC1_RXD1**/ SAI3_TX_SYNC/ SAI3_RX_SYNC/USB2_NXT	General Purpose Input/Output	80	IO	$O2V_{DD}$	---
GPIO2_12/**EC1_RXD0**/ SAI3_TX_BCLK/ SAI3_RX_BCLK/USB2_STP	General Purpose Input/Output	14	IO	$O2V_{DD}$	---
GPIO2_13/**EC1_RX_CLK**/ SAI4_TX_SYNC/ SAI4_RX_SYNC/USB2_D5	General Purpose Input/Output	12	IO	$O2V_{DD}$	---
GPIO2_14/**EC1_RX_DV**/ SAI4_TX_BCLK/ SAI4_RX_BCLK/USB2_DIR	General Purpose Input/Output	81	IO	$O2V_{DD}$	---
GPIO2_15/**EMI1_MDC**	General Purpose Input/Output	15	O	$O2V_{DD}$	1, 5
GPIO2_16/**EMI1_MDIO**	General Purpose Input/Output	82	IO	$O2V_{DD}$	---
GPIO2_17/ **TA_TMP_DETECT_B**	General Purpose Input/Output	120	I	$O1V_{DD}$	---
Power-On-Reset Configuration					
cfg_eng_use/**UART1_SOUT**/ GPIO1_00	Power-on-Reset Configuration	83	I	$O2V_{DD}$	1, 4, 23
cfg_eng_use2/ **QSPI_A_DATA0**/GPIO1_11	Power-on-Reset Configuration	123	I	$O1V_{DD}$	1, 4, 23
cfg_func_backup/ **QSPI_A_DATA1**/GPIO1_12	backup	61	I	$O1V_{DD}$	1, 4
cfg_rcw_src/**CLK_OUT**/ GPIO1_31/RESET_REQ_B	Power-on-Reset Configuration	17	I	$O2V_{DD}$	1, 4
cfg_sysclk_sel/**QSPI_A_CS0**/ GPIO1_05	Power-on-Reset Configuration	124	I	$O1V_{DD}$	1, 4, 31
Frequency Timer Module 1					
FTM1_CH0/**IIC1_SCL**/ GPIO1_02	Channel 0	121	IO	$O1V_{DD}$	---
FTM1_CH1/**SDHC2_CMD**/ GPIO1_24/SAI1_RX_DATA/ SPI_MOSI	Channel 1	65	IO	$O1V_{DD}$	---
FTM1_CH2/**SDHC2_DAT2**/ GPIO1_27/SAI1_TX_SYNC/ SPI_CS2_B	Channel 2	125	IO	$O1V_{DD}$	---
FTM1_CH3/**SDHC2_DAT0**/ GPIO1_25/SAI1_RX_SYNC/ SPI_CS0_B	Channel 3	126	IO	$O1V_{DD}$	---
FTM_EXTCLK/ **TBSCAN_EN_B**/GPIO1_30	External Clock	86	I	$O2V_{DD}$	1, 21, 26
Frequency Timer Module 2					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM2_CH0/**IIC1_SDA**/ GPIO1_03	Channel 0	58	IO	$O1V_{DD}$	---
FTM2_CH1/**SDHC2_DAT3**/ GPIO1_28/SAI1_RX_BCLK/ SPI_MISO	Channel 1	63	IO	$O1V_{DD}$	---
FTM2_CH2/**SDHC2_DAT1**/ GPIO1_26/SAI1_TX_BCLK/ SPI_CS1_B	Channel 2	64	IO	$O1V_{DD}$	---
FTM2_CH3/**SDHC2_CLK**/ GPIO1_29/SAI1_TX_DATA/ SPI_CLK	Channel 3	127	O	$O1V_{DD}$	1, 5
Synchronous Audio Interfaces					
SAI1_RX_BCLK/ **SDHC2_DAT3**/GPIO1_28/ FTM2_CH1/SPI_MISO	SAI Receive Clock	63	I	$O1V_{DD}$	1
SAI1_RX_DATA/ **SDHC2_CMD**/GPIO1_24/ FTM1_CH1/SPI_MOSI	SAI Receive Data	65	I	$O1V_{DD}$	1
SAI1_RX_SYNC/ **SDHC2_DAT0**/GPIO1_25/ FTM1_CH3/SPI_CS0_B	SAI Receive Sync	126	IO	$O1V_{DD}$	---
SAI1_TX_BCLK/ **SDHC2_DAT1**/GPIO1_26/ FTM2_CH2/SPI_CS1_B	SAI Transmit Clock	64	I	$O1V_{DD}$	1
SAI1_TX_DATA/**SDHC2_CLK**/ GPIO1_29/FTM2_CH3/ SPI_CLK	SAI Transmit Data	127	O	$O1V_{DD}$	1, 5
SAI1_TX_SYNC/ **SDHC2_DAT2**/GPIO1_27/ FTM1_CH2/SPI_CS2_B	SAI Transmit Sync	125	IO	$O1V_{DD}$	---
SAI2_RX_BCLK/**EC1_RXD2**/ GPIO2_10/USB2_D7	SAI Receive Clock	13	I	$O2V_{DD}$	1
SAI2_RX_DATA/**EC1_TXD0**/ GPIO2_05/USB2_D3	SAI Receive Data	77	I	$O2V_{DD}$	1
SAI2_RX_SYNC/**EC1_RXD3**/ GPIO2_09/USB2_D6	SAI Receive Sync	79	IO	$O2V_{DD}$	---
SAI2_TX_BCLK/ **EC1_GTX_CLK**/GPIO2_07/ USB2_D4	SAI Transmit Clock	78	I	$O2V_{DD}$	1
SAI2_TX_DATA/**EC1_TXD1**/ GPIO2_04/USB2_D2	SAI Transmit Data	10	O	$O2V_{DD}$	1
SAI2_TX_SYNC/**EC1_TX_EN**/ GPIO2_06/USB2_CLK	SAI Transmit Sync	11	IO	$O2V_{DD}$	---
SAI3_RX_BCLK/**EC1_RXD0**/ GPIO2_12/SAI3_TX_BCLK/ USB2_STP	SAI Receive Clock	14	I	$O2V_{DD}$	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SAI3_RX_DATA/**EC1_TXD2**/ GPIO2_03/SAI3_TX_DATA/ USB2_D1	SAI Receive Data	76	I	$O2V_{DD}$	1
SAI3_RX_SYNC/**EC1_RXD1**/ GPIO2_11/SAI3_TX_SYNC/ USB2_NXT	SAI Receive Sync	80	IO	$O2V_{DD}$	---
SAI3_TX_BCLK/**EC1_RXD0**/ GPIO2_12/SAI3_RX_BCLK/ USB2_STP	SAI Transmit Clock	14	I	$O2V_{DD}$	1
SAI3_TX_DATA/**EC1_TXD2**/ GPIO2_03/SAI3_RX_DATA/ USB2_D1	SAI Transmit Data	76	O	$O2V_{DD}$	1
SAI3_TX_SYNC/**EC1_RXD1**/ GPIO2_11/SAI3_RX_SYNC/ USB2_NXT	SAI Transmit Sync	80	IO	$O2V_{DD}$	---
SAI4_RX_BCLK/**EC1_RX_DV**/ GPIO2_14/SAI4_TX_BCLK/ USB2_DIR	SAI Receive Clock	81	I	$O2V_{DD}$	1
SAI4_RX_DATA/**EC1_TXD3**/ GPIO2_02/SAI4_TX_DATA/ USB2_D0	SAI Receive Data	9	I	$O2V_{DD}$	1
SAI4_RX_SYNC/ **EC1_RX_CLK**/GPIO2_13/ SAI4_TX_SYNC/USB2_D5	SAI Receive Sync	12	IO	$O2V_{DD}$	---
SAI4_TX_BCLK/**EC1_RX_DV**/ GPIO2_14/SAI4_RX_BCLK/ USB2_DIR	SAI Transmit Clock	81	I	$O2V_{DD}$	1
SAI4_TX_DATA/**EC1_TXD3**/ GPIO2_02/SAI4_RX_DATA/ USB2_D0	SAI Transmit Data	9	O	$O2V_{DD}$	1
SAI4_TX_SYNC/ **EC1_RX_CLK**/GPIO2_13/ SAI4_RX_SYNC/USB2_D5	SAI Transmit Sync	12	IO	$O2V_{DD}$	---
SAI5_RX_BCLK/**TRST_B**/ GPIO1_10/SAI5_TX_BCLK	SAI Receive Clock	85	I	$O2V_{DD}$	1
SAI5_RX_DATA/**TDI**/ GPIO1_07/UART2_RTS_B/ SAI5_TX_DATA	SAI Receive Data	19	I	$O2V_{DD}$	1
SAI5_RX_SYNC/**TMS**/ GPIO1_09/UART2_CTS_B/ SAI5_TX_SYNC	SAI Receive Sync	84	IO	$O2V_{DD}$	---
SAI5_TX_BCLK/**TRST_B**/ GPIO1_10/SAI5_RX_BCLK	SAI Transmit Clock	85	I	$O2V_{DD}$	1
SAI5_TX_DATA/**TDI**/ GPIO1_07/UART2_RTS_B/ SAI5_RX_DATA	SAI Transmit Data	19	O	$O2V_{DD}$	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SAI5_TX_SYNC/**TMS**/ GPIO1_09/UART2_CTS_B/ SAI5_RX_SYNC	SAI Transmit Sync	84	IO	$O2V_{DD}$	---
Power and Ground Signals					
GND01	GND - SoC Common ground	131	---	---	---
GND02	GND - SoC Common ground	133	---	---	---
GND03	GND - SoC Common ground	135	---	---	---
GND04	GND - SoC Common ground	138	---	---	---
GND05	GND - SoC Common ground	139	---	---	---
GND06	GND - SoC Common ground	140	---	---	---
GND07	GND - SoC Common ground	146	---	---	---
GND08	GND - SoC Common ground	148	---	---	---
GND09	GND - SoC Common ground	150	---	---	---
GND10	GND - SoC Common ground	152	---	---	---
GND11	GND - SoC Common ground	154	---	---	---
GND12	GND - SoC Common ground	156	---	---	---
GND13	GND - SoC Common ground	157	---	---	---
GND14	GND - SoC Common ground	158	---	---	---
GND15	GND - SoC Common ground	160	---	---	---
GND16	GND - SoC Common ground	162	---	---	---
GND17	GND - SoC Common ground	164	---	---	---
GND18	GND - SoC Common ground	166	---	---	---
GND19	GND - SoC Common ground	167	---	---	---
GND20	GND - SoC Common ground	170	---	---	---
GND21	GND - SoC Common ground	172	---	---	---
GND22	GND - SoC Common ground	175	---	---	---
GND23	GND - SoC Common ground	176	---	---	---
GND24	GND - SoC Common ground	178	---	---	---
GND25	GND - SoC Common ground	180	---	---	---
GND26	GND - SoC Common ground	182	---	---	---
GND27	GND - SoC Common ground	184	---	---	---
GND28	GND - SoC Common ground	185	---	---	---
GND29	GND - SoC Common ground	188	---	---	---
GND30	GND - SoC Common ground	190	---	---	---
GND31	GND - SoC Common ground	192	---	---	---
GND32	GND - SoC Common ground	193	---	---	---
GND33	GND - SoC Common ground	202	---	---	---
GND34	GND - SoC Common ground	203	---	---	---
GND35	GND - SoC Common ground	210	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND36	GND - SoC Common ground	211	---	---	---
XOSC_GND	Oscillator GND	196	---	---	---
SD_GND1	Serdes1 core logic GND	197	---	---	---
SD_GND2	Serdes1 core logic GND	201	---	---	---
SD_GND3	Serdes1 core logic GND	208	---	---	---
O1VDD1	General OVDD I/O supply	144	---	$O1V_{DD}$	---
O1VDD2	General OVDD I/O supply	145	---	$O1V_{DD}$	---
O1VDD3	General OVDD I/O supply	174	---	$O1V_{DD}$	---
O2VDD1	General OVDD I/O supply	168	---	$O2V_{DD}$	---
O2VDD2	General OVDD I/O supply	177	---	$O2V_{DD}$	---
XOSC_OVDD	XTAL IO and Oscillator supply	195	---	$XOSC\_OV_{DD}$	---
XOSC_VDD	XOSC_PLL 0.9V supply	205	---	$XOSC\_V_{DD}$	---
EVDD	eSDHC supply - switchable	159	---	EV_{DD}	---
G1VDD1	DDR supply	147	---	$G1V_{DD}$	---
G1VDD2	DDR supply	155	---	$G1V_{DD}$	---
G1VDD3	DDR supply	165	---	$G1V_{DD}$	---
G1VDD4	DDR supply	173	---	$G1V_{DD}$	---
G1VDD5	DDR supply	183	---	$G1V_{DD}$	---
S1VDD1	SerDes1 core logic supply	198	---	$S1V_{DD}$	---
S1VDD2	SerDes1 core logic supply	200	---	$S1V_{DD}$	---
X1VDD1	SerDes1 transceiver supply	199	---	$X1V_{DD}$	---
X1VDD2	SerDes1 transceiver supply	209	---	$X1V_{DD}$	---
PROG_MTR	Reserved	132	---	PROG_MTR	15
TA_PROG_SFP	SFP Fuse Programming Override supply	134	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	149	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	151	---	V_{DD}	---
VDD02	Supply for cores and platform	153	---	V_{DD}	---
VDD03	Supply for cores and platform	161	---	V_{DD}	---
VDD04	Supply for cores and platform	163	---	V_{DD}	---
VDD05	Supply for cores and platform	169	---	V_{DD}	---
VDD06	Supply for cores and platform	171	---	V_{DD}	---
VDD07	Supply for cores and platform	179	---	V_{DD}	---
VDD08	Supply for cores and platform	181	---	V_{DD}	---
VDD09	Supply for cores and platform	187	---	V_{DD}	---
VDD10	Supply for cores and platform	189	---	V_{DD}	---
VDD11	Supply for cores and platform	191	---	V_{DD}	---
AVDD_CGA1	A53 Core Cluster Group A PLL1 1.8V supply	194	---	AVDD_CGA1	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
AVDD_PLAT	Platform PLL 1.8V supply	186	---	AVDD_PLAT	---
AVDD_REF	XOSC PLL supply	204	---	AVDD_REF	---
AVDD_SD1_PLL1	SerDes1 PLL 1 supply	88	---	AVDD_SD1_PLL1	---
AVDD_SD1_PLL2	SerDes1 PLL 2 supply	95	---	AVDD_SD1_PLL2	---
USB_HVDD	USB 3.3V High Supply	143	---	USB_HV_{DD}	---
USB_SDVDD	USB Analog and digital HS supply	142	---	USB_SDV_{DD}	---
USB_SVDD	USB Analog and digital SS supply	141	---	USB_SV_{DD}	---

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

3. Must be grounded through a 240 ohms resistor.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation.

11. This pin requires a 200Ω ± 1% pull-up to respective power-supply.

14. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

15. These pins must be pulled to ground (GND).

16. This pin requires a 698Ω ± 1% pull-up to respective power-supply.

17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

19. PORESET_B should be asserted zero during the JTAG Boundary scan operation, and is required to be controllable on board.

20. To use JTAG interface this pin must be pulled up by 2K-10K Ohms to O2VDD, else pull to GND.

21. This pin will not be tested using JTAG Boundary scan operation.

22. While PORESET_B is asserted, this pin must be pulled up to O2VDD through a weak pull-up resistor (4.7 Kohm) and SD card detect signal should be tri-stated.

23. In external clock oscillator mode, cfg_eng_use and cfg_eng_use2 power-on-reset configuration pins should be pulled high.

24. This pin should be tied to GND in external clock oscillator mode.

26. In normal operation, this pin must be pulled high to O2VDD with 4.7 Kohm.

27. This pin should be grounded through a 200 Ohm ± 1% 100ppm/°C precision resistor.

28. Recommend that a weak pull-up resistor (10-20 kΩ) be placed on this pin to the respective power supply.

29. Recommend that a weak pull-up resistor (10-100 kΩ) be placed on this pin to the respective power supply.

30. RESET_REQ_B is multiplexed on this pin in the LS1012A Rev 2.0 only.

31. Config signal cfg_sysclk_sel/QSPI_A_CS0 should be pulled down during reset when LS1012A is clocked from external oscillator. Most of the flash devices enter into debug mode if CS is pulled low during reset. Hence, pull down resistance connected at cfg_sysclk_sel pin should be isolated from chip select signal of flash device during reset cycle.

Warning

See **"Connection Recommendations in QorIQ LS1012A Design Checklist *(AN5192)*"** for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section provides the AC and DC electrical specifications for the LS1012A processor. The device is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other electrical characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings for the LS1012A device.

Table 2. Absolute maximum ratings[1]

Parameter	Symbol	Max Value	Unit	Notes
Supply for core and platform	V_{DD}	-0.3 to 0.97	V	
Platform PLL supply voltage	AV_{DD_PLAT}	-0.3 to 1.98	V	
Core cluster group A PLL1 supply	AV_{DD_CGA1}	-0.3 to 1.98	V	
XOSC PLL 1.35 V supply	AV_{DD_REF}	-0.3 to 1.48	V	
SerDes1 PLL 1 supply	$AV_{DD\_SD1\_PLL1}$	-0.3 to 1.48	V	
SerDes1 PLL 2 supply	$AV_{DD\_SD1\_PLL2}$	-0.3 to 1.48	V	
I2C, GPIO1, GPIO2, FTM1, FTM2, QSPI, SAI1, SPI, eSDHC2, PORESET_B, Tamper detect, USB1, ASLEEP	$O1V_{DD}$	-0.3 to 1.98	V	-
UART1, UART2, GPIO1, GPIO2, SDHC1_CD_B, SDHC1_WP, SDHC1_VSEL, CLK_OUT, EC1, SAI[2-5], JTAG, EMI1, USB2	$O2V_{DD}$	-0.3 to 1.98	V	-
SDHC1_CMD, SDHC_DAT[3:0], SDHC_CLK, GPIO1	EV_{DD}	-0.3 to 1.98 -0.3 to 3.63	V	-
DDR3L DRAM I/O voltage	$G1V_{DD}$	-0.3 to 1.48	V	-
XTAL IO and Oscillator supply	$XOSC\_OV_{DD}$	-0.3 to 1.98	V	-
XOSC PLL 0.9 V	$XOSC\_V_{DD}$	-0.3 to 0.97	V	-
SerDes transceiver core and reciever power supply	$S1V_{DD}$	-0.3 to 0.97	V	-
Pad power supply for SerDes transmitter	$X1V_{DD}$	-0.3 to 1.48	V	-
Fuse Programming	TA_PROG_SFP	-0.3 to 1.98	V	
Thermal Monitor Unit Supply	TH_V_{DD}	-0.3 to 1.98	V	-
USB PHY Transceiver supply voltage	USB_HV_{DD}	-0.3 to 3.63	V	4
	USB_SDV_{DD}	-0.3 to 0.97	V	5

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Parameter	Symbol	Max Value	Unit	Notes
	USB_SV_{DD}	-0.3 to 0.97	V	6
Storage junction temperature range	T_{stg}	-55 to 150	°C	-
Notes: Refer next table for applicable notes.				

Table 3. Absolute maximum ratings for input signal voltage levels[1]

Interface Input signals	Symbol	Max DC V_input range	Max undershoot and overshoot voltage range	Unit	Notes
DDR3L DRAM signals	MV_{IN}	GND to ($G1V_{DD}$ x 1.05)	-0.3 to ($G1V_{DD}$ x 1.1)	V	2, 3, 8
DDR3L DRAM reference	$D1\_MV_{REF}$	GND to ($G1V_{DD}$/2 x 1.05)	-0.3 to ($G1V_{DD}$/2 x 1.1)	V	2, 3
I2C, GPIO1, GPIO2, FTM1, FTM2, QSPI, SAI1, SPI, eSDHC2, PORESET_B, Tamper detect, USB1, ASLEEP	$O1V_{IN}$	GND to ($O1V_{DD}$ x 1.1)	-0.3 to ($O1V_{DD}$ x 1.15)	V	2, 3
UART1, UART2, GPIO1, GPIO2, SDHC1_CD_B, SDHC1_WP, SDHC1_VSEL, CLK_OUT, EC1, SAI[2-5], JTAG, EMI1, USB2.0 ULPI, FTM_EXTCLK	$O2V_{IN}$	GND to ($O2V_{DD}$ x 1.1)	-0.3 to ($O2V_{DD}$ x 1.15)	V	2, 3
SDHC1_CMD, SDHC_DAT[3:0], SDHC_CLK, GPIO1	EV_{IN}	GND to (EV_{DD} x 1.1)	-0.3 to (EV_{DD} x 1.15)	V	2, 3
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers	$S1V_{IN}$	GND to ($S1V_{DD}$ x 1.05)	-0.3 to ($S1V_{DD}$ x 1.1)	V	2, 3
USB PHY Transceiver signals	USB_HV_{IN}	GND to (USB_HV_{DD} x 1.05)	-0.3 to (USB_HV_{DD} x 1.15)	V	2, 3
	USB_SV_{IN}	GND to (USB_SV_{DD} x 1.1)	-0.3 to (USB_SV_{DD} x 1.15)	V	2, 3

Notes:

1. Functional operating conditions are given in Recommended operating conditions. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. **Caution:** (G1, O1, O2, E)V_{IN}, USB_HV_{IN}, USB_SV_{IN}, and D1_MVREF must not exceed Max DC V_input range. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. **Caution:** (G1, O1, O2, E)V_{IN}, USB_HV_{IN}, USB_SV_{IN}, and D1_MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

4. Transceiver supply for USBPHY.

5. Analog and Digital HS supply for USBPHY.

6. Analog and Digital SS supply for USBPHY.

7. Exposing device to Absolute Maximum Ratings conditions for long periods of time may affect reliability or cause permanent damage

8. Typical DDR interface uses ODT enabled mode. For test purposes with ODT off mode, simulation should be done first so as to ensure that the overshoot signal level at the input pin does not exceed $G1V_{DD}$ by more than 10%. The Overshoot/ Undershoot period should comply with JEDEC standards

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for the LS1012A processor. Proper device operation outside these conditions is not guaranteed.

Table 4. Recommended operating conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply for core and platform		V_{DD}	0.9 ± 30 mV	V	-
Platform PLL supply voltage		AV_{DD_PLAT}	1.8 ± 90 mV	V	6
Core cluster group A PLL1 supply		AV_{DD_CGA1}	1.8 ± 90 mV	V	6
Oscillator PLL supply		AV_{DD_REF}	1.35 ± 67 mV	V	6
SerDes1 PLL 1 supply		$AV_{DD\_SD1\_PLL1}$	1.35± 67 mV	V	
SerDes1 PLL 2 supply		$AV_{DD\_SD1\_PLL2}$	1.35± 67 mV	V	
I2C, GPIO1, GPIO2, FTM1, FTM2, QSPI, SAI1, SPI, eSDHC2, PORESET_B, Tamper detect, USB1, ASLEEP		$O1V_{DD}$	1.8± 90 mV	V	-
UART1, UART2, GPIO1, GPIO2, CLK_OUT, EC1, SAI[2-5], JTAG, EMI1, USB2, FTM_EXTCLK, SDHC1_CD_B, SDHC1_WP, SDHC1_VSEL		$O2V_{DD}$	1.8± 90 mV	V	-
SDHC1_CMD, SDHC_DAT[3:0], SDHC_CLK, GPIO1		EV_{DD}	1.8± 90 mV 3.3± 165 mV	V	-
DDR3L DRAM I/O voltage		$G1V_{DD}$	1.35± 67 mV	V	-
XTAL IO and oscillator supply		$XOSC\_OV_{DD}$	1.8± 90 mV	V	-
XOSC PLL 0.9 V		$XOSC\_V_{DD}$	0.9± 30 mV	V	-
SerDes transceiver core and reciever power supply		$S1V_{DD}$ (LS1012A Rev1.0)	0.9 + 30 mV 0.9 - 30 mV	V	-
		$S1V_{DD}$ (LS1012A Rev2.0)	0.9 + 50 mV 0.9 - 30 mV	V	-
Pad power supply for SerDes transmitter		$X1V_{DD}$	1.35± 67 mV	V	-
Fuse Programming		TA_PROG_SFP	1.8 ± 90 mV	V	1
Thermal Monitor Unit Supply		TH_V_{DD}	1.8 ± 90 mV	V	-
USB PHY Transceiver supply voltage		USB_HV_{DD}	3.3 ± 165 mV	V	3
		USB_SDV_{DD} (LS1012A Rev 1.0)	0.9 + 30 mV 0.9 - 30 mV	V	4
		USB_SDV_{DD} (LS1012A Rev 2.0)	0.9 + 50 mV 0.9 - 30 mV	V	4
		USB_SV_{DD} (LS1012A Rev 1.0)	0.9 + 30 mV 0.9 - 30 mV	V	5
		USB_SV_{DD} (LS1012A Rev 2.0)	0.9 + 50 mV 0.9 - 30 mV	V	5
Input voltage[3]	DDR3L DRAM signals	MV_{IN}	GND to $G1V_{DD}$	V	-
	DDR3L DRAM reference	MV_{REF}	$G1V_{DD}/2$ ± 2%	V	-

Table continues on the next page...

Table 4. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
	I2C, GPIO1, GPIO2, FTM1, FTM2, QSPI, SAI1, SPI, eSDHC2, PORESET_B, Tamper detect, USB1, ASLEEP	$O1V_{IN}$	GND to $O1V_{DD}$	V	-
	UART1, UART2, GPIO1, GPIO2, CLK_OUT, EC1, SAI[2-5], JTAG, EMI1, USB2, FTM_EXTCLK, SDHC1_CD_B, SDHC1_WP, SDHC1_VSEL	$O2V_{IN}$	GND to $O2V_{DD}$	V	-
	SDHC1_CMD, SDHC_DAT[3:0], SDHC_CLK, GPIO1	EV_{IN}	GND to EV_{DD}	V	-
	Main power supply for the internal circuitry of SerDes and pad power supply for SerDes receivers	$S1V_{IN}$	GND to $S1V_{DD}$	V	-
PHY transceiver signals	USB transceiver supply for USB PHY	USB_HV_{IN}	GND to $USBn\_HV_{DD}$	V	
	Analog and digital HS supply for USB PHY	USB_SV_{IN}	0.3 to USB_SV_{DD}	V	
Operating Temperature range	Normal Operation	T_A, T_J	T_A= 0 (min) to T_J= 105 (max)	°C	-
	Extended temperature	T_A, T_J	T_A = -40 (min) to T_J = 105 (max)	°C	-
	Secure Boot Fuse Programming	T_A, T_J	T_A= 0 (min) to T_J= 105 (max)	°C	

Notes:

1. TA_PROG_SFP must be supplied 1.8 V and the device must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, TA_PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power up sequencing.

2. $(O1, O2, E, S1V)_{IN}$ may overshoot or undershoot to the voltages and maximum duration shown in Figure 7.

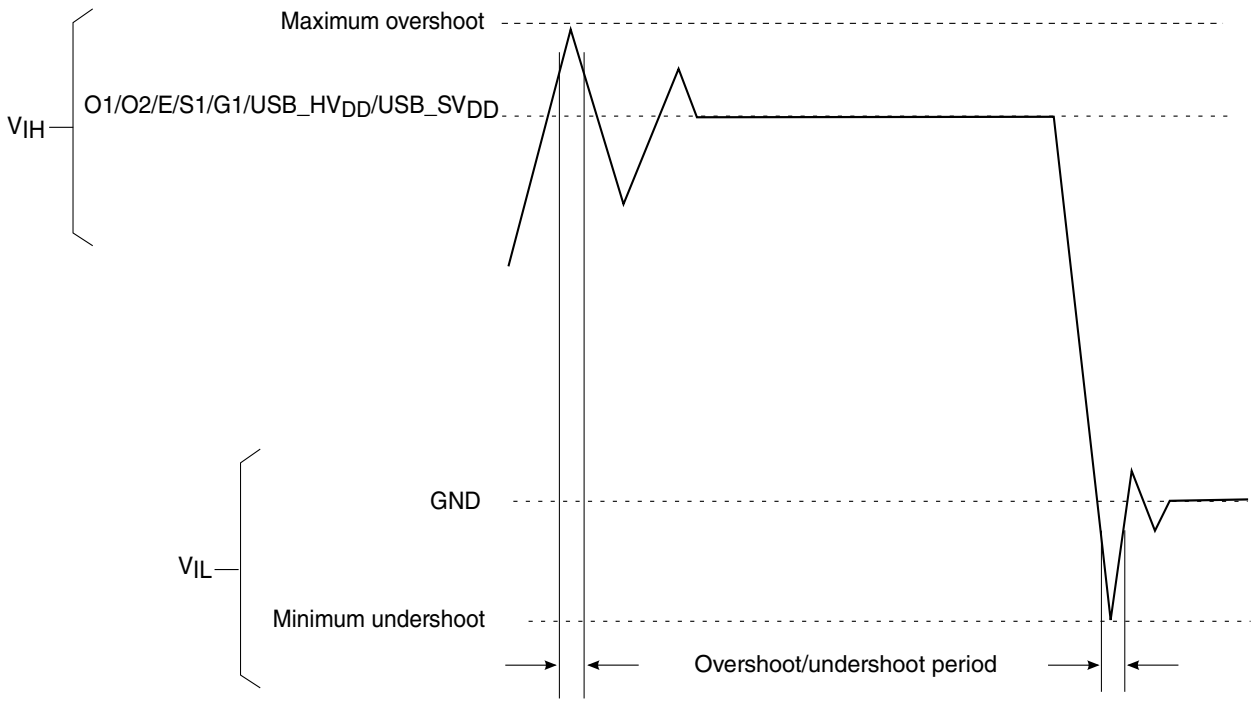
3. Transceiver supply for USB PHY.

4. Analog and Digital HS supply for USBPHY.

5. Analog and Digital SS supply for USBPHY.

6. AV_{DD_PLAT}, AV_{DD_CGA1} and AV_{DD_REF} are measured at the input to the filter and not at the pin of the device. Refer to *QorIQ LS1012A Design Checklist* (AN5192) for more details.

Figure 7 shows the undershoot and overshoot voltages at the interfaces of the chip.



Notes:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 0.8 ns.

Figure 7. Overshoot/Undershoot voltage for $O1V_{DD}$/$O2V_{DD}$/$G1V_{DD}$/$S1V_{DD}$/EV_{DD}/ USB_HV_{DD}/USB_SV_{DD}

The core and platform voltages must always be provided at nominal 0.9 V. See Table 4 for the actual recommended core voltage. The voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 4. The input voltage threshold scales with respect to the associated I/O supply voltage. On V_{DD}, EV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied MVREF*n* signal (nominally set to $G1V_{DD}/2$) as is appropriate for the electrical signaling standard. The DDR DQS receivers cannot be operated in a single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This table provides information about the characteristics of the output driver strengths.

NOTE

The values are preliminary estimates.

Table 5. Output drive capability

Driver type	Output impedance (Ω)			(Nominal) supply voltage	Notes
	Min	Typ	Max		
I2C, GPIO, FTM, QSPI, SAI, SPI, SDHC1_WP, SDHC1_VSEL, eSDHC2, USB, ULPI, ASLEEP, UART, GPIO, CLK_OUT, EC1, JTAG, EMI1	30	45	60	$O1/O2V_{DD}$ = 1.8 V	1
eSDHC1 signals: SDHC1_CMD, SDHC1_DAT[3:0], SDHC1_CLK	40	55	75	EV_{DD} = 1.8 V	1
	45	65	90	EV_{DD} = 3.3 V	1
DDR3L signals	-	48	-	$G1V_{DD}$ = 1.35 V	1
Notes 1. The drive strength of the interface in half-strength mode is at T_j = 105 °C and at $G1V_{DD}$ (min).					

3.1.4 General AC timing specifications

This table lists the AC timing specifications for the sections that are not covered under the specific interface sections.

Table 6. AC Timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Input signal rise and fall times	t_R/t_F	-	5	ns	1
1. Rise time refers to the signal transitions from 10% to 90% of supply and fall time refers to the signal transitions from 90% to 10% of supply.					

3.2 Power up sequencing

The power up sequencing requires that the power rails be applied in a specific sequence in order to ensure proper device operation. The requirements for power up are as follows:

1. $O1V_{DD}$, $O2V_{DD}$, EV_{DD}, $G1V_{DD}$, USB_HV_{DD}, $XOSC\_OV_{DD}$, AV_{DD_PLAT}, AV_{DD_CGA1}, AV_{DD_REF}, $AV_{DD\_SD1\_PLL1}$, $AV_{DD\_SD1\_PLL2}$, $X1V_{DD}$, TH_V_{DD}.
   - The PORESET_B input must be driven asserted and held during this step.
2. V_{DD}, $XOSC\_V_{DD}$, $S1V_{DD}$, USB_SDV_{DD}, USB_SV_{DD}.
   - The 3.3 V (USB_HV_{DD}) in Step 1 and 0.9 V (USB_SDV_{DD} and USB_SV_{DD}) in Step 2 supplies can power up in any sequence provided all these USB supplies ramp up within 95 ms with respect to each other.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

Negate the PORESET_B input when the required assertion/hold time meets the specifications listed in Table 12.

NOTE

The ramp rate requirements should meet the parameters listed in Table 11.

Warning

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

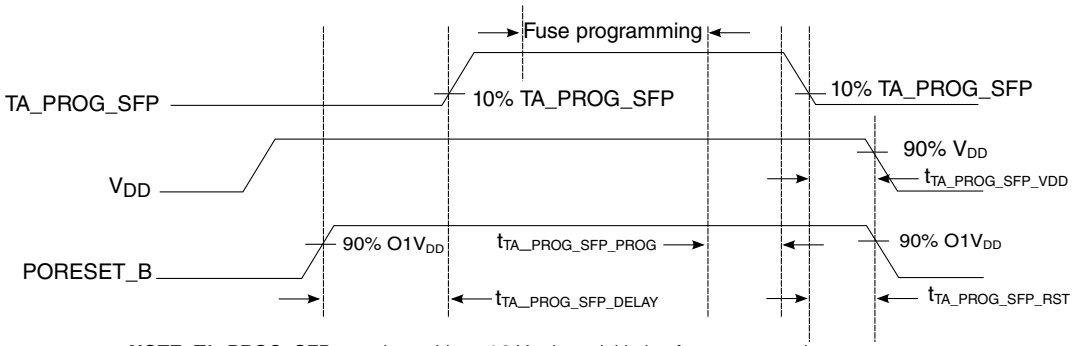
For the secure boot fuse programming, use the following steps:

1. After negation of PORESET_B, drive TA_PROG_SFP = 1.8 V after a required minimum delay per Table 7.
2. After fuse programming is complete, it is required to return TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 7. See Security fuse processor for additional details.

Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

This figure shows the TA_PROG_SFP timing diagram.



NOTE: TA_PROG_SFP must be stable at 1.8 V prior to initiating fuse programming.

Figure 8. TA_PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 7. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{TA\_PROG\_SFP\_DELAY}$	0.8	—	µs	1
$t_{TA\_PROG\_SFP\_PROG}$	0	—	µs	2
$t_{TA\_PROG\_SFP\_VDD}$	0	—	µs	3
$t_{TA\_PROG\_SFP\_RST}$	0	—	µs	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% $O1V_{DD}$ to 10% TA_PROG_SFP ramp up.

2. Delay required from fuse programming completion to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is complete, it is required to return TA_PROG_SFP = GND.

3. Delay required from TA_PROG_SFP ramp-down complete to V_{DD} ramp-down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before V_{DD} reaches 90% V_{DD}.

4. Delay required from TA_PROG_SFP ramp-down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% $O1V_{DD}$.

5. Only six secure boot fuse programming events are permitted per lifetime of a device.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per the requirements in Power up sequencing, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Power up sequencing.

3.4 Power characteristics

This table provides the power dissipations of the V_{DD} supply and SerDes supplies ($S1V_{DD}$) for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 8. Core power dissipation

Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Power mode	Junction temp. (°C)	V_{DD} power (W)	$S1V_{DD}$ power (W)	Total core and platform power (W)[1]	Notes
1000	250	1000	0.9	0.9	Typ-50	65	0.665	0.32	0.985	6
					Typical		0.94	0.32	1.26	2
					Thermal	85	1.14	0.32	1.46	5
					Maximum		1.2	0.32	1.52	3, 4
					Thermal	105	1.35	0.32	1.67	5
					Maximum		1.4	0.32	1.72	3, 4
800	250	1000	0.9	0.9	Typ-50	65	0.62	0.32	0.94	6
					Typical		0.85	0.32	1.17	2
					Thermal	85	1.05	0.32	1.37	5
					Maximum		1.11	0.32	1.43	3, 4
					Thermal	105	1.26	0.32	1.58	5
					Maximum		1.31	0.32	1.63	3, 4
600	250	1000	0.9	0.9	Typ-50	65	0.59	0.32	0.91	6
					Typical		0.82	0.32	1.14	2
					Thermal	85	1.02	0.32	1.34	5
					Maximum		1.06	0.32	1.38	3, 4
					Thermal	105	1.23	0.32	1.55	5
					Maximum		1.28	0.32	1.60	3, 4

Notes:

1. Combined power of V_{DD}, and $S1V_{DD}$ with DDR controller and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Dhrystone running with activity factor of 90% and executing DMA on the platform at 100% activity factor.

3. The maximum power assumes Dhrystone running with activity factor of 100% and executing DMA on the platform at 115% activity factor.

Table 8. Core power dissipation

Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Power mode	Junction temp. (ºC)	V_{DD} power (W)	$S1V_{DD}$ power (W)	Total core and platform power (W)[1]	Notes
4. The maximum power is provided for power supply design sizing. 5. Thermal power assumes Dhrystone running with activity factor of 90% and executing DMA on the platform at 100% activity factor. 6. Typ-50 power assumes Dhrystone running with activity factor of 50% and executing DMA on the platform at 50% activity factor.										

3.4.1 Low power mode saving estimation

Refer to this table for low power mode savings.

Table 9. Low power mode savings, 0.9 V, 65C[1, 2, 3]

Mode	Core Frequency = 1000 MHz	Core Frequency = 800 MHz	Core Frequency = 600 MHz	Units	Comments
PW15	0.11	0.09	0.07	W	Saving realized moving from run to PW15 state. Arm in STANDBYWFI/WFE
LPM20	0.20	0.16	0.12	W	Saving realized moving from PW15 to LPM20 state.
Notes: 1. Power for VDD only 2. Typical power assumes Dhrystone running with activity factor of 80% 3. Typical power based on nominal process distribution for this device.					

3.5 I/O power dissipation

The following table shows all the estimated I/O power supply values based on simulation.

Table 10. I/O power supply estimated values

Interface	Parameter	Symbol	Typical	Unit	Notes
DDR3L	1000 MT/s data rate	$G1V_{DD}$ (1.35 V)	314	mW	1, 2
PCI Express	x1, 2.5 GT/s	$X1V_{DD}$ (1.35 V)	80	mW	1, 4, 7
	x1, 5 GT/s		80		

Table continues on the next page...

Table 10. I/O power supply estimated values (continued)

Interface	Parameter	Symbol	Typical	Unit	Notes
SGMII	x1, 1.25 Gbaud	$X1V_{DD}$ (1.35 V)	77	mW	1, 4, 7
	x2, 1.25 Gbaud		127		
	x1, 3.125 Gbaud		80		
	x2, 3.125 Gbaud		132		
SATA (per port)	6.0 Gbps	$X1V_{DD}$ (1.35 V)	74	mW	1, 4, 7
PFE	RGMII	$O2V_{DD}$ (1.8 V)	21	mW	1, 3
eSDHC1		EV_{DD} (3.3 V)	17	mW	1, 3
		EV_{DD} (1.8 V)	11		
eSDHC2		$O1V_{DD}$ (1.8 V)	11	mW	1, 3
USB1	x1 Super speed mode	USB_HV_{DD} (3.3 V)	46	mW	1, 3
		USB_SV_{DD} (0.9 V)	37		
		USB_SDV_{DD} (0.9 V)	4		
USB1	x1 High speed mode	USB_HV_{DD} (3.3 V)	79	mW	1, 3
		USB_SV_{DD} (0.9 V)	0.31		
		USB_SDV_{DD} (0.9 V)	4.9		
USB2.0 ULPI		$O2V_{DD}$ (1.8 V)	18	mW	1, 3
SPI		$O1V_{DD}$ (1.8 V)	10	mW	1, 3
I2C		$O2V_{DD}$ (1.8 V)	6	mW	1, 3
DUART		$O2V_{DD}$ (1.8 V)	9	mW	1, 3
SAI		$O1V_{DD}$ (1.8 V)	34	mW	1, 3
FlexTimer		$O2V_{DD}$ (1.8 V)	18	mW	1, 3
GPIO	x8	3.3 V	5	mW	1, 3, 5
		1.8 V	3		
System control		$O1V_{DD}$ (1.8 V)	1	mW	1, 3
PLL core and system		AV_{DD}_CGA1, AV_{DD}_PLAT(1.8 V)	20	mW	1, 3
Oscillator PLL supply		AV_{DD}_REF(1.35 V)	26	mW	1, 3
PLL SerDes		$AV_{DD}\_SD1\_PLL1$, $AV_{DD}\_SD1\_PLL2$ (1.35 V)	50	mW	1, 3
PROG_SFP		PROG_SFP (1.8 V)	173	mW	1, 6
TH_V_{DD}		TH_V_{DD} (1.8 V)	5	mW	1
$XOSC\_OV_{DD}$		$XOSC\_OV_{DD}$ (1.8V)	2	mW	1, 3
QSPI		$O1V_{DD}$ (1.8 V)	10	mW	1, 3
JTAG		$O2V_{DD}$ (1.8 V)	11	mW	1, 3

1. The typical values are estimates and based on simulations at nominal recommended voltage for the I/O power supply and assuming at 105°C junction temperature.

2. Typical DDR power numbers are based on 40% utilization.

3. Assuming 15 pF total capacitance load per pin.

Table 10. I/O power supply estimated values

Interface	Parameter	Symbol	Typical	Unit	Notes
4. The total power numbers of $X1V_{DD}$ is dependent on customer application use case. This table lists all the SerDes configurations possible for the device. To get the $X1V_{DD}$ power numbers, the user should add the combined lanes to match to the total SerDes lanes used, not simply multiply the power numbers by the number of lanes. 5. GPIOs are supported on $O1V_{DD}$, $O2V_{DD}$, and EV_{DD} power rails. 6. The maximum power requirement is during programming. No active power beyond leakage levels should be drawn and the supply must be grounded when not programming. 7. When combination of SerDes-based protocols (PCI Express, SGMII, or SATA) are used, the $X1V_{DD}$ power obtained by adding the power numbers reported in the separate rows of this table for the individual protocols may be more than the actual power consumption. The $X1V_{DD}$ power consumption will not exceed 182 mW (typical) for the configuration PCI Express x1 5 GT/s + SGMII 1.25 GBaud + SATA 6.0 Gbps.					

3.6 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 11. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (except for V_{DD} and USB_HV_{DD})	-	25	V/ms	1,2
Required ramp rate V_{DD}	0.06	25	V/ms	2,3
USB_HV_{DD}	-	26.7	V/ms	1,2
Note: 1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 mV to 500 mV is the most critical as this range might falsely trigger the ESD circuitry. 2. Over full recommended operating temperature range (see Table 4). 3. The minimum ramp rate of V_{DD} is required to ensure proper start up of XOSC.				

3.7 RESET initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. Table 12 provides the RESET initialization AC timing specifications.

Table 12. RESET initialization timing specifications

Parameter	Min	Max	Unit	Notes
Required assertion time of PORESET_B after V_{DD} is stable	100	-	ms	1
Maximum rise/fall time of PORESET_B	-	8	ns	1, 3
Input hold time for all POR configurations with respect to negation of PORESET_B	16	-	ns	2, 3
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of PORESET_B	-	40	ns	2, 3

Note:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. POR configurations must be driven asserted before the core and platform power supplies are powered up.
3. Time is mentioned assuming that SYSCLK is 125 MHz.
4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.8 Input clocks

There are two clocking modes supported on the LS1012A processor:

1. Using a 25MHz on board crystal also called Crystal based clocking.

   This requires a 25 MHz crystal onboard which provides a 25 MHz sinusoidal input to the SoC (EXTAL, XTAL) I/O's.

2. Using a clock source which generates 25MHz single-ended square wave.

   This requires a 25 MHz clock source onboard which provides a 25 MHz square wave input to the SoC (EXTAL) I/O. Connect XTAL to ground.

The tables below list the input specifications for crystals and external clock oscillator.

Table 13. Input specifications for crystals [4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Crystal fundamental frequency	Fxtal		25		MHz	
Frequency tolerance	Fctol	-50 ppm		+50 ppm	-	1, 2, 5
Equivalent Series Resistance	ESR		40	60	Ohms	
Load Capacitance	Cload			18	pF	3
Pin capacitance of EXTAL, XTAL	C_{EXTAL} / C_{XTAL}	3	3.2	3.4	pF	

Table continues on the next page...

Table 13. Input specifications for crystals [4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
1. Frequency tolerance is a function of total capacitance loading the crystal. This total load capacitance includes the load capacitors as well as the capacitive load of the board and device pins. To maintain a desired frequency tolerance, the load capacitance specified by the crystal manufacturer may need to be adjusted to accommodate these stray capacitances. 2. To maintain the required system frequency tolerance, it is necessary to select a crystal with an appropriate initial frequency tolerance as well as low frequency variation across temperature and frequency aging. The frequency tolerance is the summation of initial frequency tolerance, frequency variation across temperature and frequency variation due to ageing. 3. To minimize the impact of capacitance variation across temperature, a load capacitor with zero drift across temperature (for example, NP0 ceramic capacitors) may be necessary. 4. The power sequencing requirements must be followed for proper startup operation. 5. All the output signals and clocks will have the same frequency tolerance as the input clock. User may choose input frequency tolerance based on the system requirements. For example: • GTX_CLK of RGMII requires ±50ppm • PCIe requires ±300 ppm (without spread spectrum) • USB requires ±300ppm						

Table 14. Input DC specifications for external clock oscillator/generator

Parameter	Symbol	Min	Typ	Max	Units	Notes
Vin input high	V_{IH}	1.2			Volts	
Vin input low	V_{IL}			0.4	Volts	

Table 15. Input AC specifications for external clock oscillator/generator

Parameter	Symbol	Min	Typ	Max	Units	Notes
Frequency tolerance	Fotol	-50 ppm		+50 ppm	-	1, 2
Clock duty cycle	ClkDutyCycle	40%		60%	-	
Clock input slew rate		0.36		4	V/ns	1
Random phase jitter (1 sigma in RMS) in 10 kHz – 3 MHz frequency band	Rj			1.5	ps-RMS	
Total jitter (pk-pk) in 150 kHz – 15 MHz frequency band at BER of 10 -12	Tj			50	ps -PP	
1. The slew rate is measured from V_{IL} to V_{IH}. 2. All the output signals and clocks will have the same frequency tolerance as the input clock. User may choose input frequency tolerance based on the system requirements. For example: • GTX_CLK of RGMII requires ±50ppm • PCIe and TX_CLK requires ±300 ppm (without spread spectrum) • SATA requires ±350 ppm • USB requires ±300ppm • SGMII requires ±100 ppm						

3.9 DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3L SDRAM controller interface. Note that the required $G1V_{DD}$(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

3.9.1 DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 16. DDR3L SDRAM interface DC electrical characteristics [1, 8]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREFn	0.49 x $G1V_{DD}$	0.51 x $G1V_{DD}$	V	2, 3, 4
Input high voltage	V_{IH}	MVREFn + 0.115	$G1V_{DD}$	V	5
Input low voltage	V_{IL}	GND	MVREFn - 0.115	V	5
I/O leakage current	I_{OZ}	-100	100	µA	7

Notes:

1. $G1V_{DD}$ is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREFn is expected to be equal to 0.5 x $G1V_{DD}$ and to track $G1V_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREFn may not exceed the MVREFn DC level by more than ± 1% of $G1V_{DD}$ (that is, ± 13.5 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREFn with a min value of MVREFn - 0.04 and a max value of MVREFn + 0.04. V_{TT} should track variations in the DC level of MVREFn.
4. The voltage regulator for MVREFn must meet the specifications stated in Table 17.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Refer to the IBIS model for the complete output IV curve characteristics.
7. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ $G1V_{DD}$.
8. For recommended operating conditions, see Table 4.

This table provides the current draw characteristics for MVREFn.

Table 17. Current draw characteristics for MVREFn

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3L SDRAM for MVREFn	I_{MVREFn}	-	200	µA	-

Notes:

1. For recommended operating conditions, see Table 4.

3.9.2 DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3L memories. Note that the required $G1V_{DD}$(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

3.9.2.1 DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 18. DDR3L SDRAM interface input AC timing specifications[3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ	t_{CISKEW}	-	-	ps	1
1000 MT/s data rate		-170	170		1
Tolerated Skew for MDQS-MDQ	t_{DISKEW}	-	-		-
1000 MT/s data rate		-300	300		2

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

3. For recommended operating conditions, see Table 4.

This figure shows the DDR3L SDRAM interface input timing diagram.

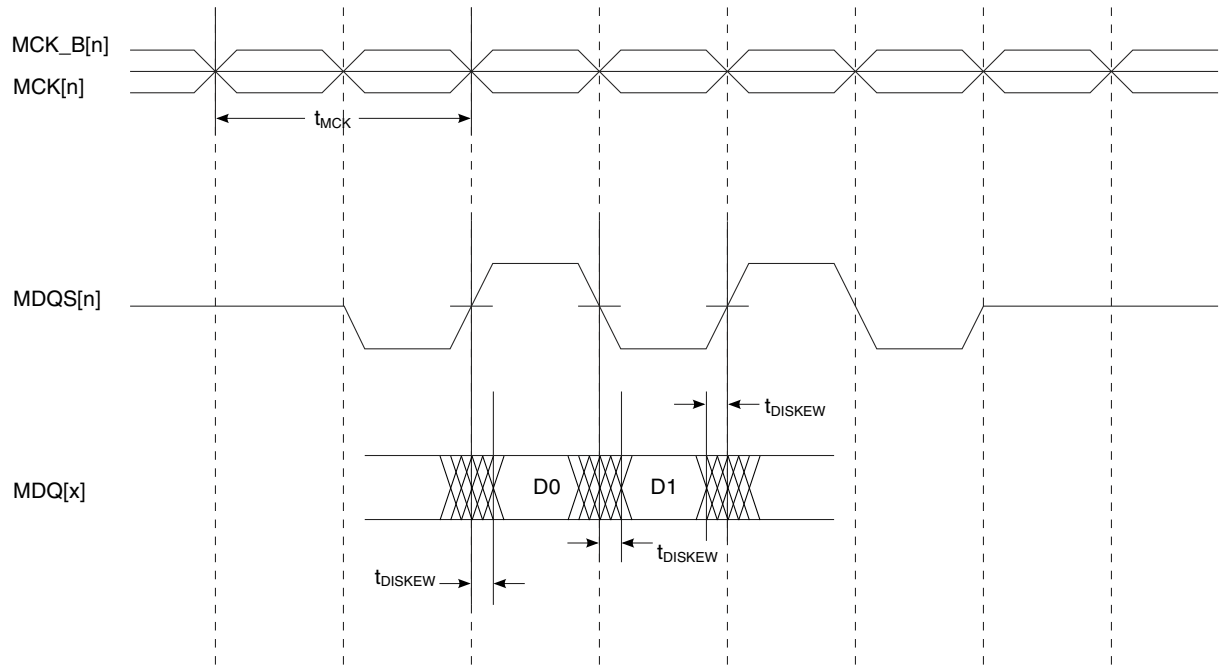


Figure 9. DDR3L SDRAM interface input timing diagram

3.9.2.2 DDR3L SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR3L SDRAM interface.

Table 19. DDR3L SDRAM interface output AC timing specifications[6]

Parameter	Symbol1	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2	2	ns	2
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	-	-		3
1000 MT/s data rate		0.665	-		3
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	-	-		3
1000 MT/s data rate		0.744	-		3
MCK to MDQS Skew	t_{DDKHMH}	-	-		4
1000MT/s data rate		-0.245	0.245		4
MDQ/MDM output data eye	$t_{DDKXDEYE}$	-	-	ns	5
1000 MT/s data rate		0.6	-		5
MDQS preamble	t_{DDKHMP}	0.9 x t_{MCK}	-	ns	-
MDQS postamble	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	-	

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS}

Table 19. DDR3L SDRAM interface output AC timing specifications[6]

Parameter	Symbol1	Min	Max	Unit	Notes
symbolizes DDR timing (DD) for the time tMCK memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, tDDKLDX symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time. 2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals. 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MDM/MDQS. 4. Note that t_{DDKHMH} follows the symbol conventions described in Note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). 5. This value can be determined by the maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor. 6. For recommended operating conditions, see Table 4.					

NOTE

For the ADDR/CMD/CNTL setup and hold specifications in Table 19, it is assumed that memory clock is delayed by 1/2 applied cycle.

This figure shows the SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

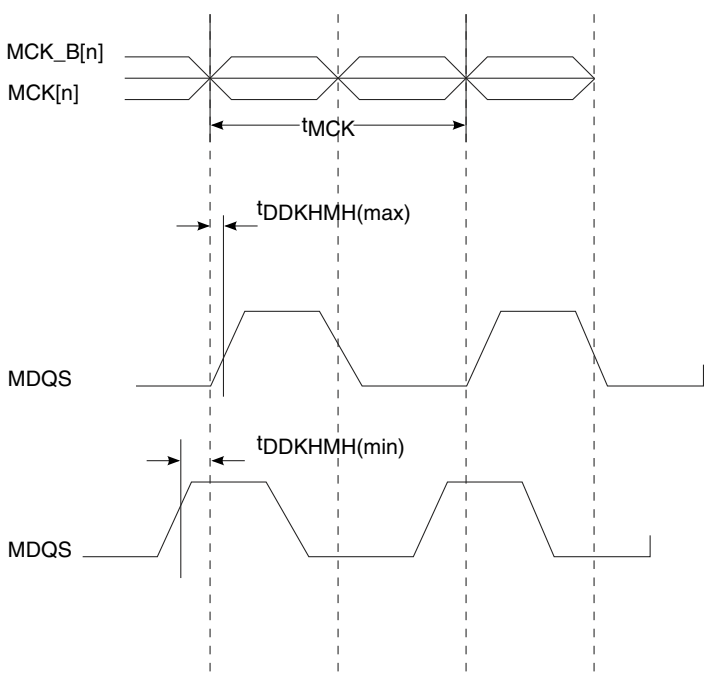


Figure 10. t_{DDKHMH} timing diagram

This figure shows the SDRAM output timing diagram.

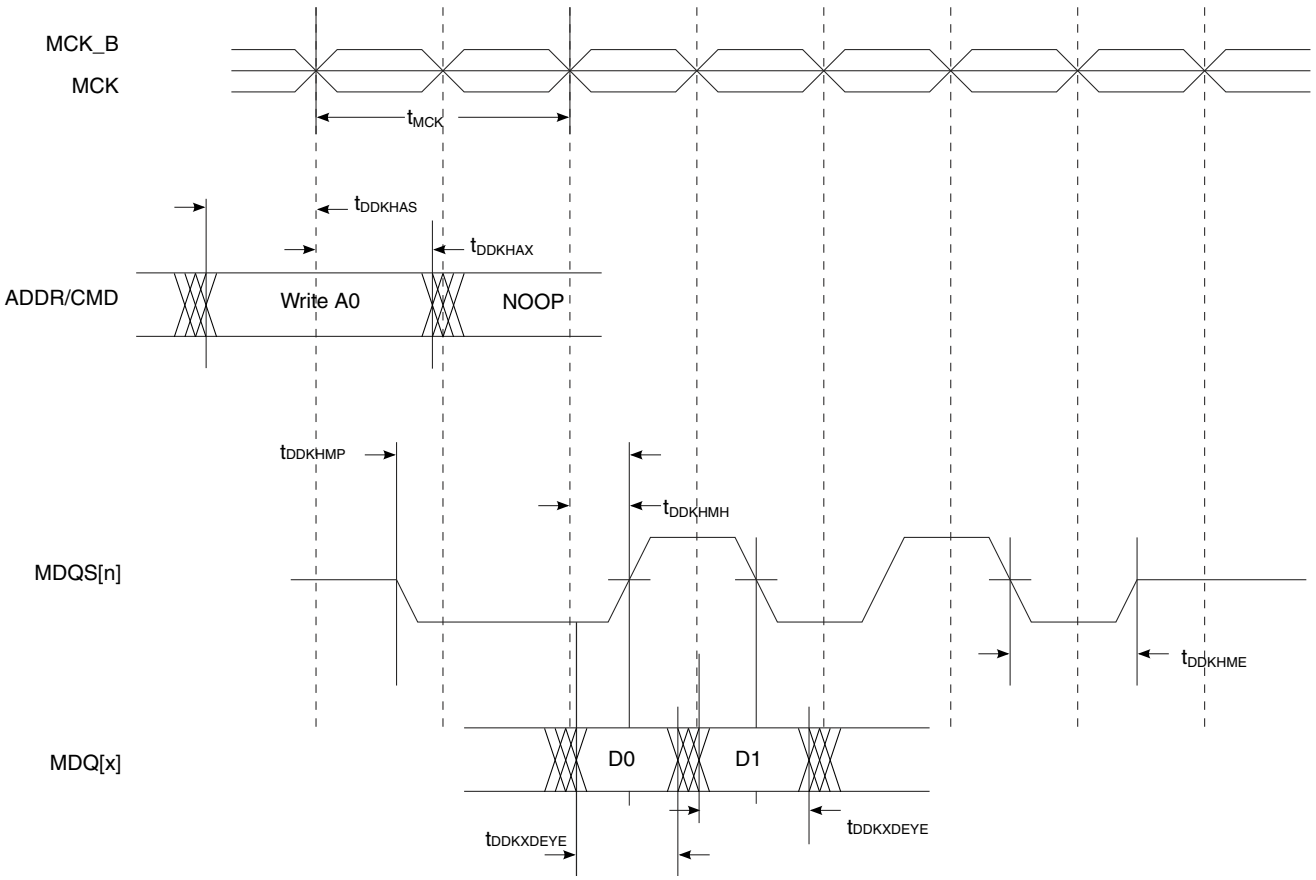


Figure 11. DDR3L output timing diagram

3.10 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

3.10.1 DUART DC electrical characteristics

Table below provides the DC electrical characteristics for the DUART interface.

Table 20. DUART DC electrical characteristics ($O2V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $O2V_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.3 x $O2V_{DD}$	V	1
Input current ($O2V_{IN}$ = 0 V or $O2V_{IN}$ = $O2V_{DD}$)	I_{IN}	-	±50	μA	2
Output high voltage ($O2V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage ($O2V_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Table continues on the next page...

Table 20. DUART DC electrical characteristics ($O2V_{DD}$ = 1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Note: 1. The minimum V_{IL} and the maximum V_{IH} values are based on the respective minimum and maxium $O2V_{IN}$ values found in Table 4. 2. The symbol represents the input voltage of the supply. It is referenced in Table 4. 3. For recommended operating conditions, see Table 4.					

3.10.2 DUART AC timing specifications

Table below provides the AC timing specifications for the DUART interface.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1
Maximum baud rate	f_{CCB}/16	baud	1, 2
Oversample rate	16	-	3
Notes: 1. f_{CCB} refers to the internal platform clock. 2. The actual attainable baud rate is limited by the latency of interrupt processing. 3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each at 16^{th} sample. 4. For recommended operating conditions, see Table 4.			

3.11 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.11.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface. This device has two eSDHC interfaces. Out of the two, eSDHC2 supports only 1.8 V voltage levels.

Table 22. eSDHC interface DC electrical characteristics EV_{DD} = 3.3 V)[2]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	-	0.7 x EV_{DD}	-	V	1

Table continues on the next page...

Table 22. eSDHC interface DC electrical characteristics EV_{DD} = 3.3 V)[2] (continued)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input low voltage	V_{IL}	-	-	0.25 x EV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = -100 µA at EV_{DD} min	0.75 x EV_{DD}	-	V	-
Output low voltage	V_{OL}	I_{OL} = 100 µA at EV_{DD} min	-	0.125 x EV_{DD}	V	-

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum EV_{IN} values found in Table 4.
2. The DC electrical characteristics are based on recommended operating conditions with EV_{DD} = 3.3 V.

Table 23. eSDHC interface DC electrical characteristics O1/O2/EV_{DD} = 1.8 V)[2]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	-	0.7 x OV_{DD}	-	V	1
Input low voltage	V_{IL}	-	-	0.3 x OV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = -2 mA at OV_{DD} min	OV_{DD} - 0.45	-	V	-
Output low voltage	V_{OL}	I_{OL} = 2 mA at OV_{DD} min	-	0.45	V	-

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum OV_{IN} values found in Table 4.
2. The DC electrical characteristics are based on recommended operating conditions for 1.8 V.
3. Replace OV_{DD} with EV_{DD}, $O1V_{DD}$ or $O2V_{DD}$ as applicable.

3.11.2 eSDHC AC timing specifications

This section provides the AC timing specifications.

This table provides the eSDHC AC timing specifications as defined in Figure 12, Figure 13, and Figure 14.

Table 24. eSDHC AC timing specifications (high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency: SD/SDIO (full-speed/high-speed mode) eMMC (full-speed/high-speed mode)	f_{SHSCK}	0	25/50 26/52	MHz	2, 4
SDHC_CLK clock low time (full-speed/high-speed mode)	t_{SHSCKL}	10/7	-	ns	4

Table continues on the next page...

Table 24. eSDHC AC timing specifications (high-speed mode)[6] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock high time (full-speed/high-speed mode)	t_{SHSCKH}	10/7	-	ns	4
SDHC_CLK clock rise and fall times	$t_{SHSCKR/}$ t_{SHSCKF}	-	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK	$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK	$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC high-speed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. In the full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-26MHz for an eMMC device. In the high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an eMMC device .

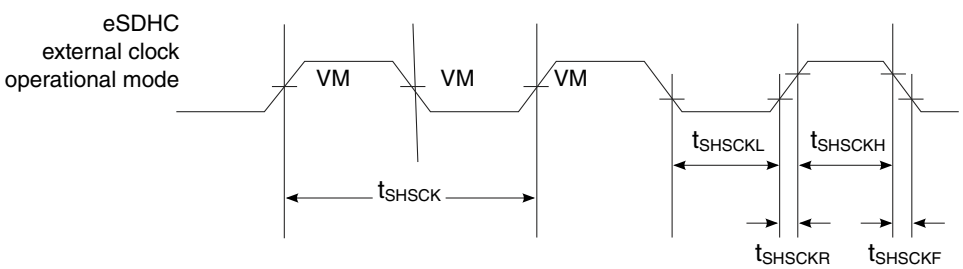
3. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.

4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.

5. The parameter values apply to both the full-speed and the high-speed modes.

6. Th AC timing specifications are based on the recommended operating conditions with $O1/O2V_{DD}$=1.8 V and EV_{DD}= 3.3 V.

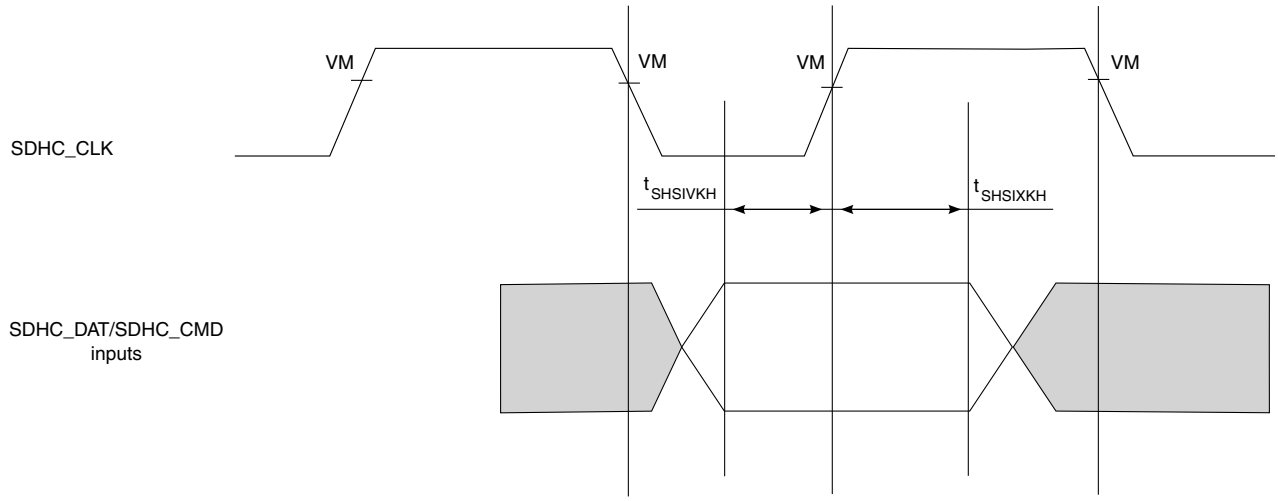
This figure provides the eSDHC clock input timing diagram.



VM = Midpoint voltage ($O1/O2V_{DD}/2$)

Figure 12. eSDHC clock input timing diagram

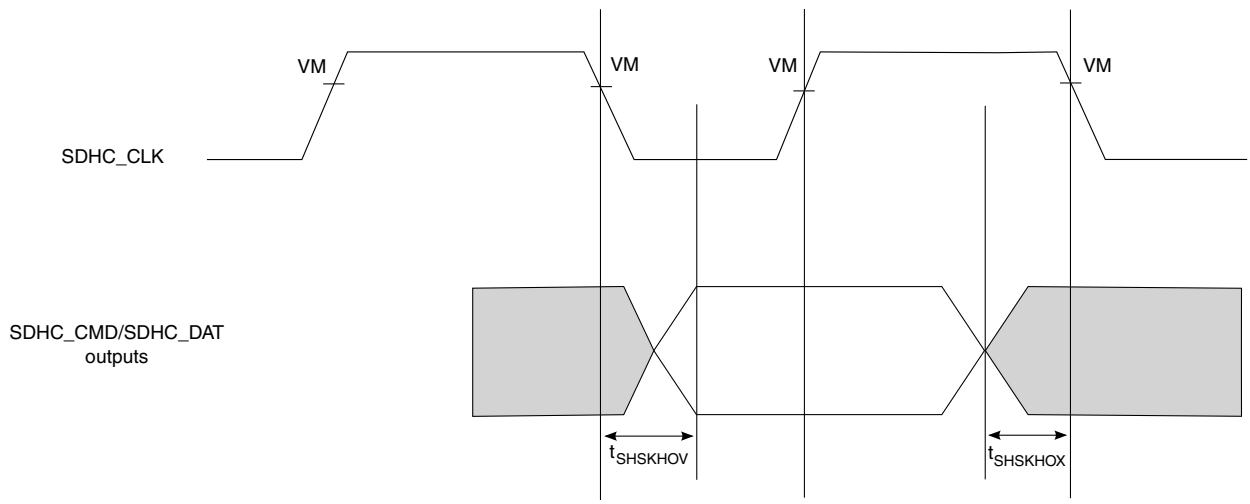
This figure provides the input AC timing diagram for high-speed mode.



VM = Midpoint Voltage ($O1/O2V_{DD}/2$)

Figure 13. eSDHC high-speed mode input AC timing diagram

This figure provides the output AC timing diagram for high-speed mode.



VM = Midpoint Voltage ($O1/O2V_{DD}/2$)

Figure 14. eSDHC high-speed mode output AC timing diagram

Table 25. eSDHC AC timing specifications (SDR 50 mode)[3]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHCK}	0	100	MHz	-
SDHC_CLK duty cycle	-	44	56	%	-
SDHC_CLK clock rise and fall times	t_{SHCKR}/ t_{SHCKF}	-	2	ns	1

Table continues on the next page...

Table 25. eSDHC AC timing specifications (SDR 50 mode)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	t_{SHKHOX}	1.7	-	ns	2,1
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	t_{SHKHOV}	-	6.2	ns	2,1
Input data window	t_{SHIDV}	0.35	-	Unit Interval	
Oversampling clock	F_{samp_clk}	-	1000	MHz	

Notes:

1. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF.
2. The values are based on without a voltage translator.
3. The AC timing specifications are based on the recommended operating conditions with $EV_{DD}/O1V_{DD} = 1.8$ V.

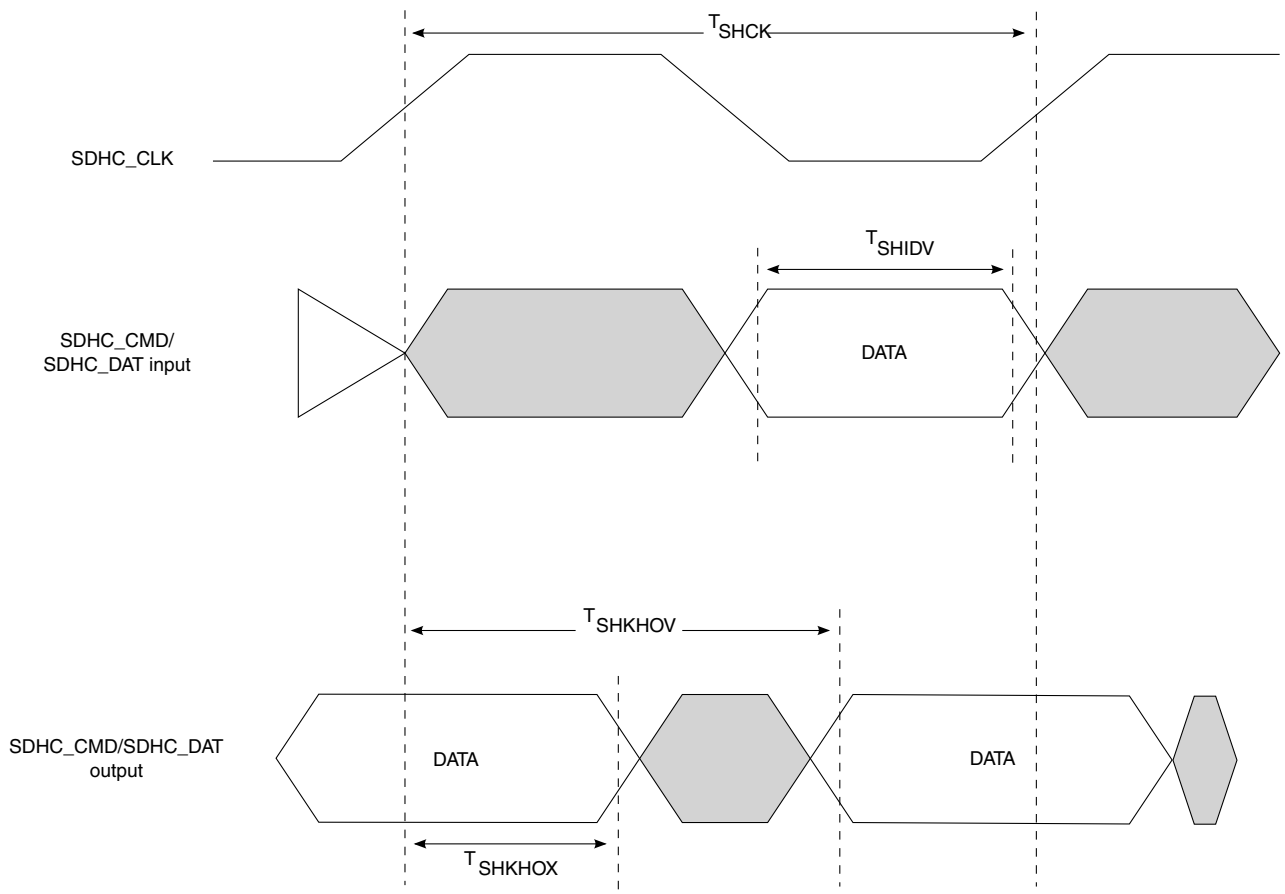


Figure 15. eSDHC SDR50 mode timing diagram

This table provides the eSDHC AC timing specifications for DDR50/eMMC DDR mode.

Table 26. eSDHC AC timing specifications (DDR50/eMMC DDR)[3]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHCK}	-	-	MHz	-
SD/SDIO DDR50 mode			41.67		
eMMC DDR mode			41.67		
SDHC_CLK duty cycle	-	47.5	52.5	%	-
SDHC_CLK clock rise and fall times	t_{SHCKR}/	-	-	ns	1
SD/SDIO DDR50 mode	t_{SHCKF}		4.79		2
eMMC DDR mode			2		
Input setup times: SDHC_DATx to SDHC_CLK	$t_{SHDIVKH}$	-	-	ns	1
SD/SDIO DDR50 mode		1.795			2
eMMC DDR mode		1.89			3
Input hold times: SDHC_DATx to SDHC_CLK	$t_{SHDIXKH}$	-	-	ns	1
SD/SDIO DDR50 mode		1.2			2
eMMC DDR mode		1.18			3
Output hold time: SDHC_CLK to SDHC_DATx valid	$t_{SHDKHOX}$	-	-	ns	1
SD/SDIO DDR50 mode		1.7			2
eMMC DDR mode		3.42			
Output delay time: SDHC_CLK to SDHC_DATx valid	$t_{SHDKHOV}$	-	-	ns	1
SD/SDIO DDR50 mode			8.19		2
eMMC DDR mode			8.79		
Input setup times: SDHC_CMD to SDHC_CLK	$t_{SHCIVKH}$	-	-	ns	1
SD/SDIO DDR50 mode		6.59			2
eMMC DDR mode		6.74			3
Input hold times: SDHC_CMD to SDHC_CLK	$t_{SHCIXKH}$	-	-	ns	1
SD/SDIO DDR50 mode		1.2			2
eMMC DDR mode		1.18			3
Output hold time: SDHC_CLK to SDHC_CMD valid	$t_{SHCKHOX}$	-	-	ns	1
SD/SDIO DDR50 mode		1.7			2
eMMC DDR mode		3.92			
Output delay time: SDHC_CLK to SDHC_CMD valid	$t_{SHCKHOV}$	-	-	ns	1
SD/SDIO DDR50 mode			17.15		2
eMMC DDR mode			19.84		

Notes:

1. C_{CARD} ≤ 10pF, (1 card).
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD}$ ≤ 20pF for eMMC, ≤ 25pF for Input Data of DDR50, ≤ 30pF for Input CMD of DDR50.
3. Round trip board delay should not be greater than 2.4ns.
4. The AC timing specifications are based on the recommended operating conditions with $EV_{DD}/O1V_{DD}$ = 1.8 V.

This figure provides the eSDHC DDR50/eMMC DDR mode input AC timing diagram.

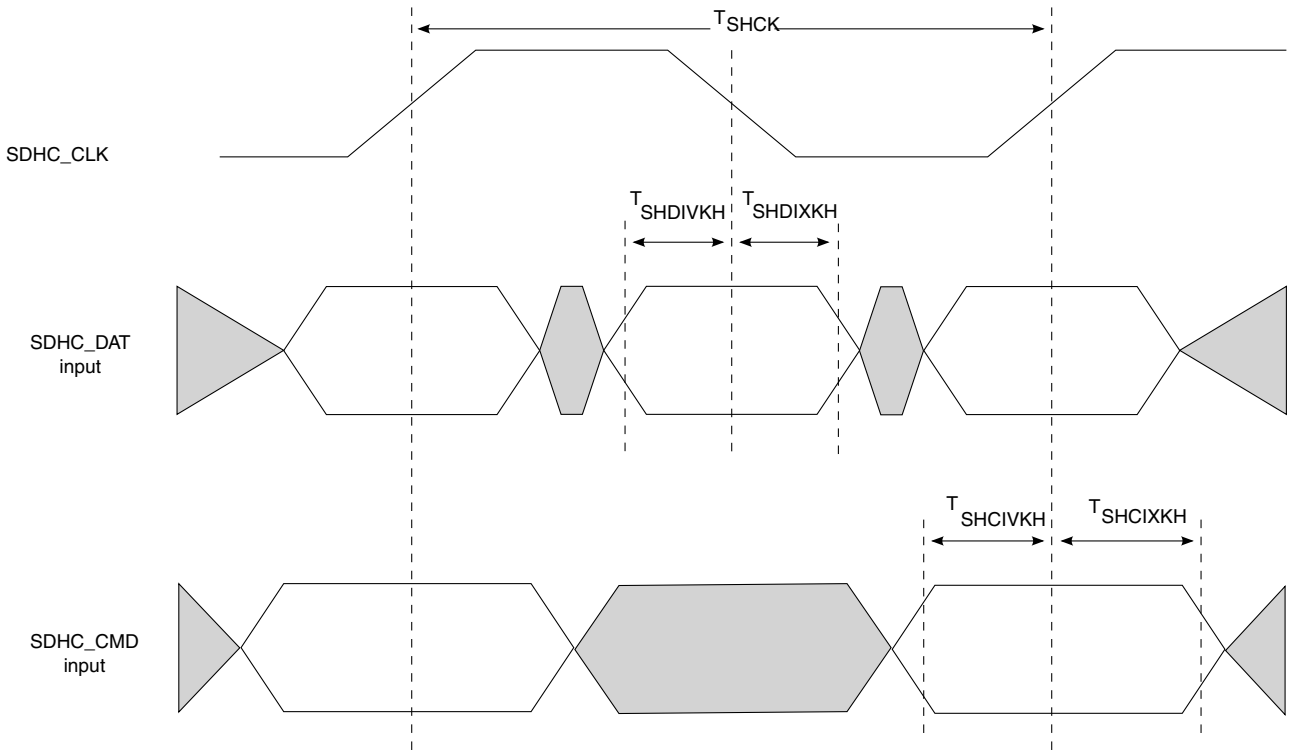


Figure 16. eSDHC DDR50/eMMC DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/eMMC DDR mode output AC timing diagram.

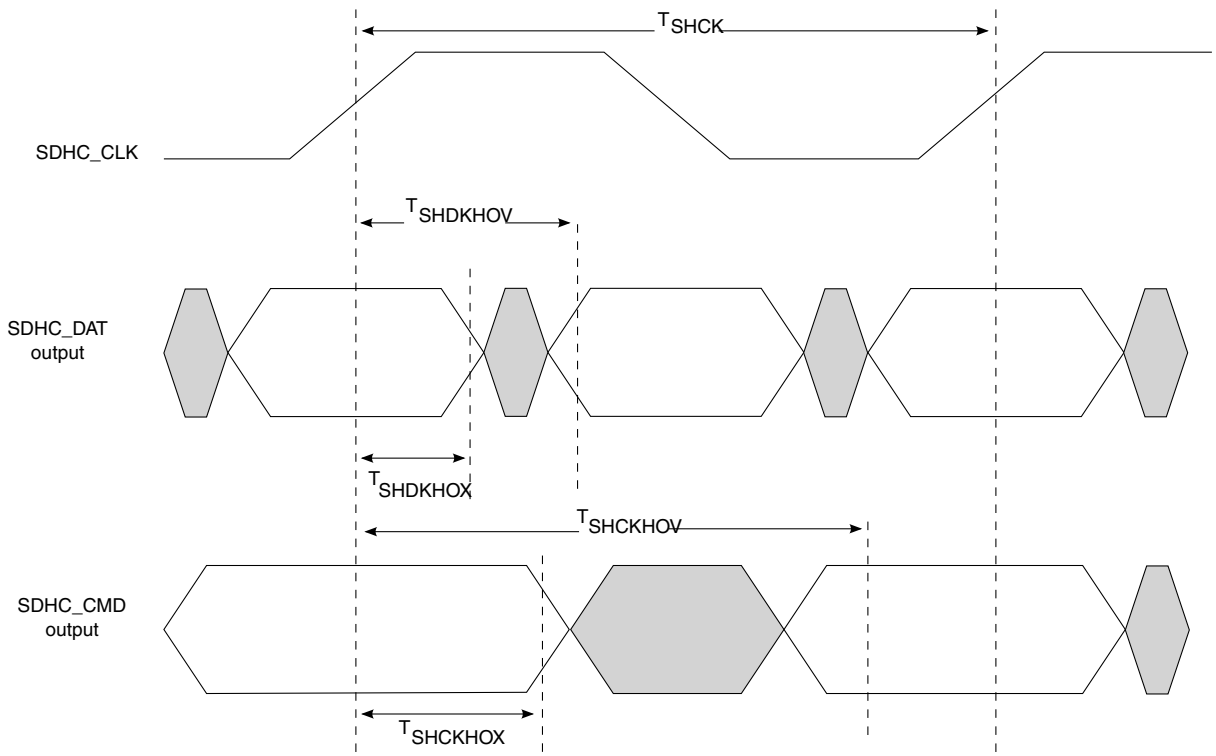


Figure 17. eSDHC DDR50/eMMC DDR mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR104 / eMMC HS200.

Table 27. eSDHC AC timing specifications (SDR104 / eMMC HS200)

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHCK}	-	125	MHz	-
SD/SDIO SDR104 mode			125		
eMMC HS200 mode					
SDHC_CLK duty cycle	-	44	56	%	-
SDHC_CLK clock rise and fall times	t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	t_{SHKHOX}	-	-	ns	1
SD/SDIO SDR104 mode		1.9			
eMMC HS200 mode		1.9			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	t_{SHKHOV}	-	-	ns	1
SD/SDIO SDR104 mode			5.6		
eMMC HS200 mode			5.6		
Input data window (UI)	t_{SHIDV}	-	-	Unit Interval	1
SD/SDIO SDR104 mode		0.5			
eMMC HS200 mode		0.475			
Notes:					

Table 27. eSDHC AC timing specifications (SDR104 / eMMC HS200)

Parameter	Symbol[1]	Min	Max	Unit	Notes
1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15$ pF.					
2. The AC timing specifications are based on the recommended operating conditions with $EV_{DD}/O1V_{DD} = 1.8$ V.					

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

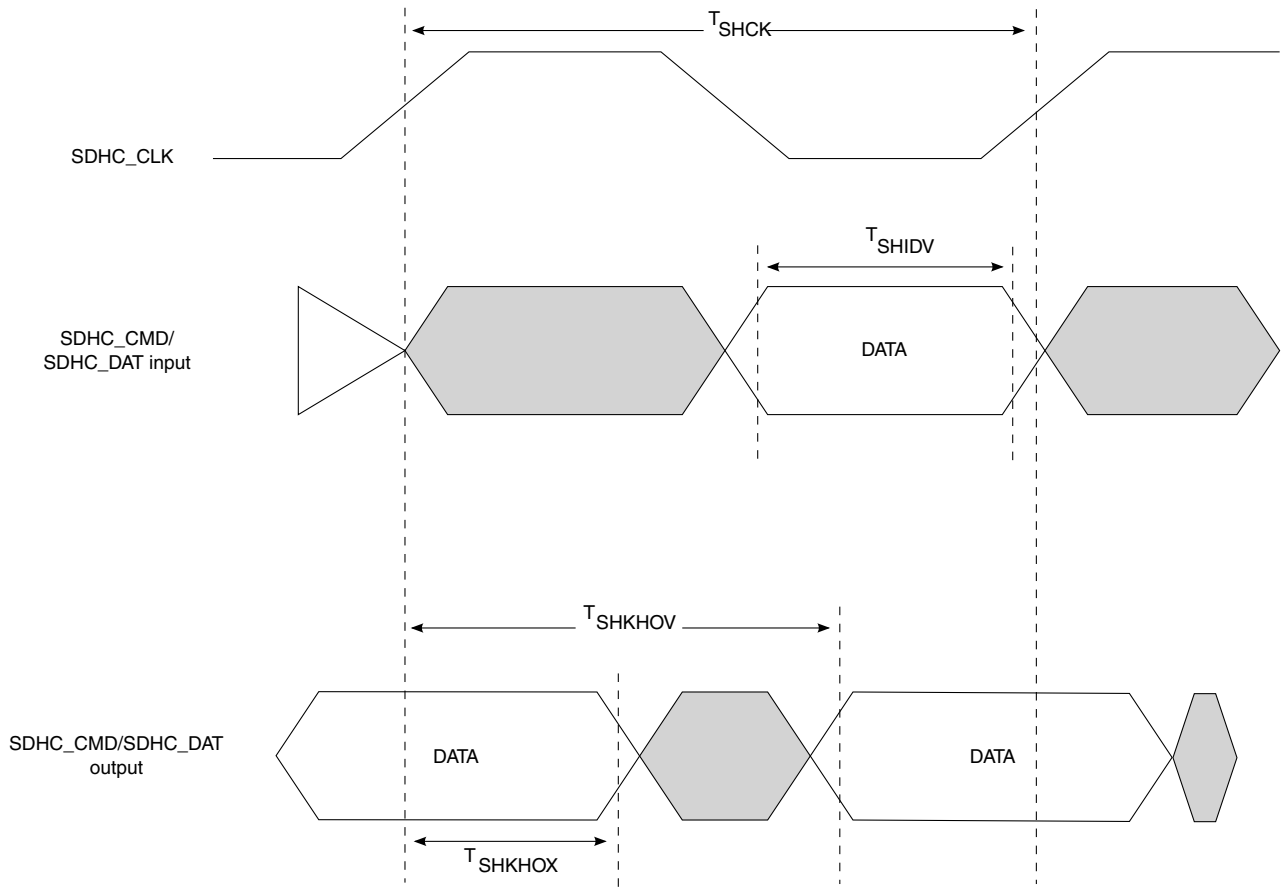


Figure 18. eSDHC SDR104/HS200 mode timing diagram

3.12 PFE (Ethernet Interface)

This section provides the AC and DC electrical characteristics for the PFE triple speed Ethernet 10/100/1000 controller and MII management.

3.12.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interface at $O2V_{DD}$ = 1.8 V.

Table 28. RGMII DC electrical characteristics ($O2V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $O2V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $O2V_{DD}$	V	1
Input current ($O2V_{IN}$ = 0 V or $O2V_{IN}$ = $O2V_{DD}$)	I_{IN}	—	±50	μA	2
Output high voltage ($O2V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	-
Output low voltage ($O2V_{DD}$= min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	-

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the minimum and maximum $O2V_{IN}$ values found in Table 4.
2. The symbol $O2V_{IN}$, in this case, represents the $O2V_{IN}$ symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.12.2 RGMII AC timing specifications

This table presents the RGMII timing specifications.

Table 29. RGMII AC timing specifications

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	-	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	-
Rise time (20%-80%)	t_{RGTR}	-	-	0.54	ns	7
Fall time (20%-80%)	t_{RGTF}	-	-	0.54	ns	7

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that the PC board design requires clocks to be routed such that an additional trace delay greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

Table 29. RGMII AC timing specifications

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
5. The frequency of RX_CLK (input) should not exceed the frequency of GTX_CLK (output) by more than 300 ppm.						
6. For recommended operating conditions, see Table 4.						
7. Applies to inputs and outputs.						

This figure shows the RGMII AC timing and multiplexing diagrams.

NOTE

NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

This figure shows the RGMII AC timing and multiplexing diagram.

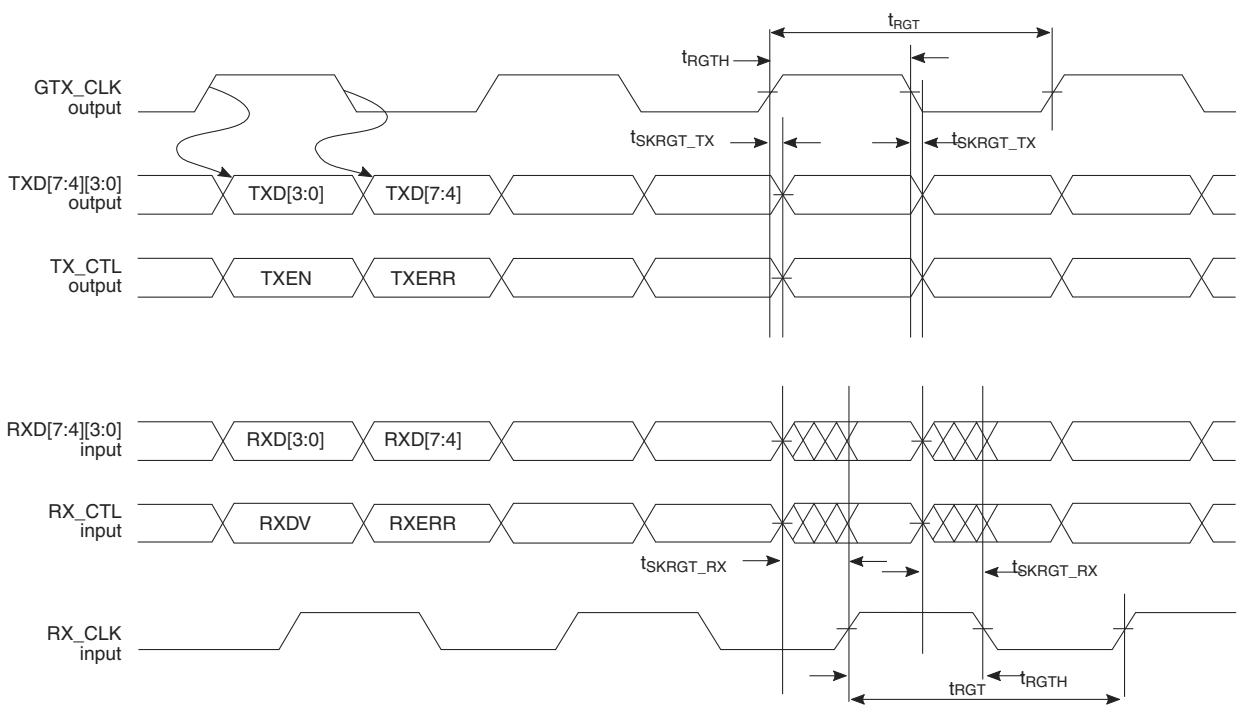


Figure 19. RGMII AC timing and multiplexing diagram

3.13 EMI1 management

This section provides the DC and AC electrical characteristics for EMI1 management.

3.13.1 EMI1 management DC electrical characteristics

The MDC and MDIO are defined to operate at a supply voltage of 1.8 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 30. EMI1 management DC electrical characteristics ($O2V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7*$O2V_{DD}$	-	V	-
Input low voltage	V_{IL}	-	0.3*$O2V_{DD}$	V	-
Input current ($O2V_{IN}$ = 0 V, $O2V_{IN}$ = $O2V_{DD}$)	I_{IN}	-	±50	μA	1
Output high voltage ($O2V_{DD}$ = Min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage ($O2V_{DD}$ = Min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Note:

1. The symbol $V_{IN,}$ in this case, represents the $O2V_{IN}$ symbol referenced in Table 4.

2. The DC electrical characteristics are based on recommended operating conditions with $O2V_{DD}$ = 1.8 V

3.13.2 EMI1 management AC timing specifications

This table provides the EMI1 management AC timing specifications.

Table 31. EMI1 management AC timing specifications

Parameter	$Symbol_1$	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	-	-	2.5	MHz	
MDC clock pulse width high	t_{MDCH}	160	-	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	(Y+1) x t_{enet_clk} - 3	-	(Y+1) x t_{enet_clk} + 3	ns	2, 3, 4
MDIO to MDC setup time	t_{MDDVKH}	8	-	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	0	-	-	ns	-

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the tMDC clock reference (K) going to the high (H) state or setup time.

2. t_{enet_clk} is the Ethernet clock period (4ns).

3. The AC timing specifications are based on recommended operating conditions with $O2V_{DD}$ = 1.8 V ± 5%.

4. The value of Y = 5. .

This figure shows the EMI1 management interface timing diagram.

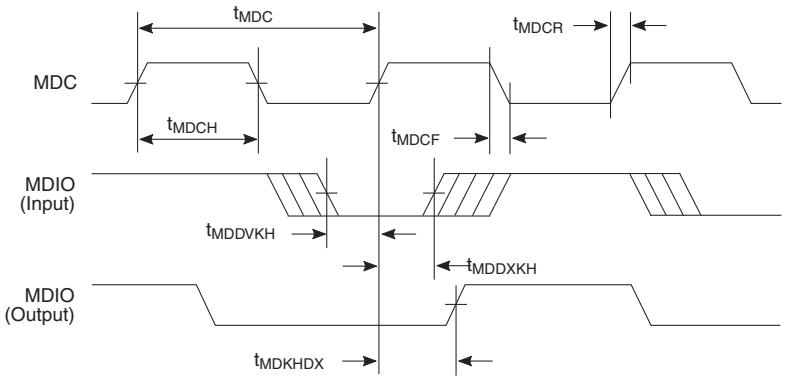


Figure 20. EMI1 management interface timing diagram

3.14 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

3.14.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for the GPIO interface when operating at EV_{DD} = 3.3 V supply.

Table 32. GPIO DC electrical characteristics (EV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x EV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x EV_{DD}	V	1
Input current (EV_{IN} = 0 V or EV_{IN} = EV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the minimum and maximum EV_{IN} respective values found in Table 4.
2. The symbol EV_{IN} represents the input voltage of the supply. It is referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the GPIO interface when operating at O1/O2/EV_{DD} = 1.8 V supply.

Table 33. GPIO DC electrical characteristics ($O1/O2/EV_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	0.7 x $O1/O2/EV_{DD}$	-	V	1
Low-level input voltage	V_{IL}	-	0.3 x $O1/O2/EV_{DD}$	V	1
Input current ($O1/O2/EV_{IN}$ = 0 V or $O1/O2/EV_{IN}$ = $O1/O2/EV_{DD}$)	I_{IN}	-	±50	μA	2
High-level output voltage ($O1/O2/EV_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Low-level output voltage ($O1/O2/EV_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the minimum and maximum $O1/O2/EV_{IN}$ respective values found in Table 4.

2. The symbol $O1/O2/EV_{IN}$ represents the input voltage of the supply. It is referenced in Table 4.

3. For recommended operating conditions, see Table 4.

3.14.2 GPIO AC timing specifications

Table below provides the GPIO input and output AC timing specifications.

Table 34. GPIO Input AC timing specifications

Parameter	Symbol	Min	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least tPIWID to ensure proper operation.

2. For recommended operating conditions, see Table 4

Figure below provides the AC test load for the GPIO.

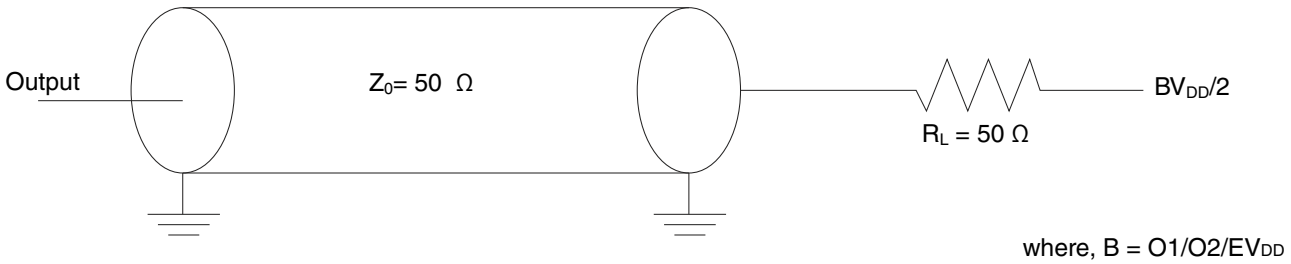


Figure 21. GPIO AC test load

3.15 SAI/I²S interface

This section describes the DC and AC electrical characteristics for the SAI/I²S interface. There are SAI/I²S pins on various power supplies in this device.

3.15.1 SAI/I²S DC electrical characteristics

This table provides the SAI/I²S DC electrical characteristics when $O1/O2V_{DD}$ = 1.8 V.

Table 35. SAI/I²S DC electrical characteristics ($O1/O2V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $O1/O2V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $O1/O2V_{DD}$	V	1
Input current ($O1/O2V_{IN}$ = 0 V or $O1/O2V_{IN}$ = $O1/O2V_{DD}$)	I_{IN}	—	±50	μA	2
Output high voltage ($O1/O2V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	-
Output low voltage ($O1/O2V_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	-

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum $O1/O2V_{IN}$ values found in Table 4.
2. The symbol $O1/O2V_{IN}$ represents the $O1/O2V_{IN}$ symbols referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.15.2 SAI/I²S AC timing specifications

This section provides the AC timings for the synchronous audio interface (SAI) in slave (clocks input) modes.

This table provides the SAI timing in slave mode.

Table 36. Slave mode SAI timing

Parameter	Symbol	Min	Max	Unit
SAIn_TX_BCLK/SAIn_RX_BCLK cycle time (input)	t_{SAIC}	20	-	ns
SAIn_TX_BCLK/SAIn_RX_BCLK pulse width high/low (input)	$t_{SAIL/tSAIH}$	35%	65%	BCLK period
SAIn_RX_SYNC input setup before SAIn_RX_BCLK	$t_{SAISFSVKH}$	10	-	ns
SAIn_RX_SYNC input hold after SAIn_RX_BCLK	$t_{SAISFSXKH}$	2.1	-	ns
SAIn_TX_BCLK to SAIn_TX_DATA / SAIn_TX_SYNC output valid	$t_{SAISLOV}$	-	20	ns
SAIn_TX_BCLK to SAIn_TX_DATA/ SAIn_TX_SYNC output invalid	$t_{SAISLOX}$	0	-	ns
SAIn_RX_DATA setup before SAIn_RX_BCLK	$t_{SAISVKH}$	10	-	ns
SAIn_RX_DATA hold after SAIn_RX_BCLK	$t_{SAISXKH}$	2.1	-	ns

This figure shows the SAI timing in slave modes.

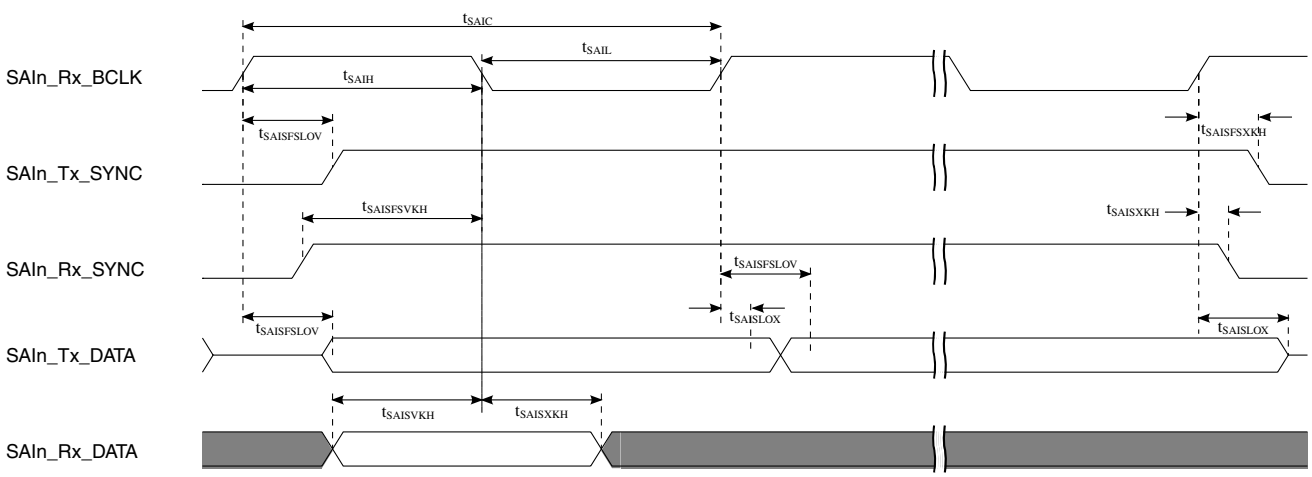


Figure 22. SAI timing — slave modes

3.16 Flextimer interface

This section describes the DC and AC electrical characteristics for the Flextimer interface. There are Flextimer pins on various power supplies in this device.

3.16.1 Flextimer DC electrical characteristics

This table provides the DC electrical characteristics for Flextimer pins operating at $O1V_{DD}$ = 1.8 V.

Table 37. Flextimer DC electrical characteristics ($O1V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $O1V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $O1V_{DD}$	V	1
Input current (V_{IN} = 0 V or V_{IN} = $O1V_{DD}$)	I_{IN}	—	±50	μA	2
Output high voltage ($O1V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($O1V_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum $O1V_{IN}$ values found in Table 4.
2. The symbol V_{IN}, in this case, represents the $O1V_{IN}$ symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.16.2 Flextimer AC timing specifications

This table provides the Flextimer AC timing specifications.

Table 38. Flextimer AC timing specifications[2]

Parameter	Symbol	Min	Unit	Notes
Flextimer inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. Flextimer inputs and outputs are asynchronous to any visible clock. Flextimer outputs should be synchronized before use by any external synchronous logic. Flextimer inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. For recommended operating conditions, see Table 4.

This figure provides the AC test load for the Flextimer.

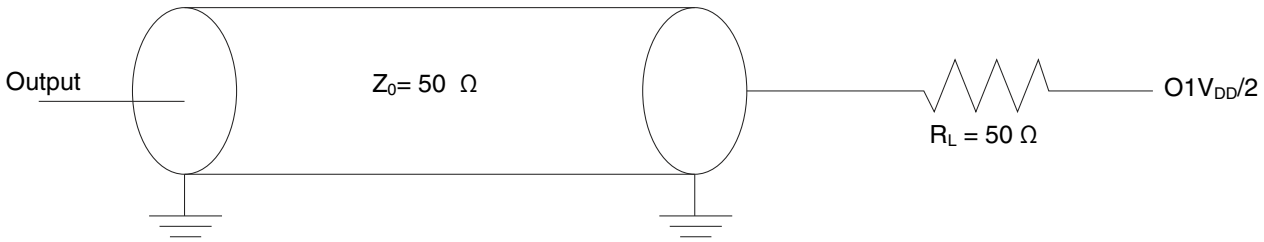


Figure 23. Flextimer AC test load

3.17 USB 2.0 ULPI interface

This section provides the AC and DC electrical specifications for the USB 2.0 interface.

3.17.1 USB 2.0 DC electrical characteristics

This table provides the DC electrical characteristics for the USB 2.0 interface when operating at $O2V_{DD}$ = 1.8 V.

Table 39. USB 2.0 DC electrical characteristics ($O2V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	$O2V_{DD}$ - 0.425	-	V	1
Input low voltage	V_{IL}	-	0.3 x $O2V_{DD}$	V	1
Input current ($O1/O2V_{IN}$ = 0 V or $O1/O2V_{IN}$ = $O1/O2V_{DD}$)	I_{IN}	-	±50	μA	2
Output high voltage ($O1/O2V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage ($O1/O2V_{DD}$= min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

NOTE:

1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum $O2V_{IN}$ values found in Table 4.

2. The symbol $O2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 4.

3. For recommended operating conditions, see Table 4.

3.17.2 USB 2.0 AC timing specifications for ULPI mode

This table provides the general timing parameters of the USB 2.0 interface for ULPI mode.

Table 40. USB general timing parameters (ULPI mode only)[1,6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	-	ns	2, 4, 5
Input setup to USB clock-all inputs	t_{USIVKH}	4	-	ns	2, 4, 5
Input hold to USB clock-all inputs	t_{USIXKH}	1	-	ns	2, 4, 5
USB clock to output valid-all outputs	t_{USKHOV}	-	7	ns	2, 4, 5
Output hold from USB clock-all outputs	t_{USKHOX}	1	-	ns	2, 4, 5
USB clock slew rate		0.5	-	V/ns	

NOTE:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.

2. All timings are with reference to the USB clock.

4. Input timings are measured at the pin.

5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

6. When switching the data pins from outputs to inputs using the pin, the output timings will be violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per ULPI specifications.

7. For recommended operating conditions, Table 4.

Figure 24 and Figure 25 provide the USB AC test load and signals, respectively.

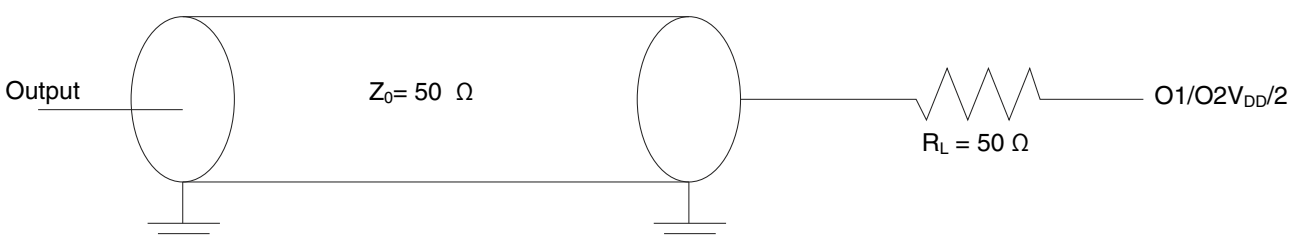


Figure 24. USB AC test load

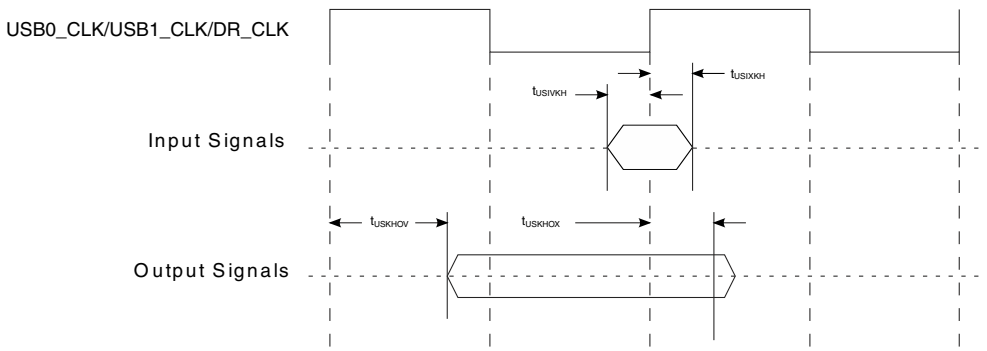


Figure 25. USB Signals

Table below provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 41. USB_CLK_IN AC timing specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Frequency range	Steady state	$f_{USB\_CLK\_IN}$	59.97	60	60.03	MHz
Clock frequency tolerance	-	t_{CLK_TOL}	-0.05	0	0.05	%
Reference clock duty cycle	Measured at rising edge and/or falling edge at /2	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second-order, high-pass filter of 500-kHz bandwidth	t_{CLK_PJ}	-	-	200	ps
USB clock slew rate		-	0.5	-	-	V/ns

3.18 USB 3.0 interface

This section describes the DC and AC electrical specifications for the USB 3.0 interface.

3.18.1 USB 3.0 PHY transceiver supply DC voltage

This table provides the DC electrical characteristics for the USB 3.0 interface when operating at USB_HV_{DD} = 3.3 V.

Table 42. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Table continues on the next page...

Table 42. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Notes: 1. The minimum $V_{IL}$and maximum V_{IH} values are based on the respective minimum and maximum USB_HV_{IN} values found in Table 4. 2. The symbol USB_HV_{IN}, in this case, represents the USB_HV_{IN} symbol referenced in Table 4. 3. For recommended operating conditions, see Table 4.					

3.18.2 USB 3.0 DC electrical characteristics

This table provides the USB 3.0 transmitter DC electrical characteristics at package pins.

Table 43. USB 3.0 transmitter DC electrical characteristics[1]

Characteristic	Symbol	Min	Nom	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800	1000	1200	$mV_{p\text{-}p}$
Low power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400	—	1200	$mV_{p\text{-}p}$
Tx de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3	—	4	dB
Differential impedance	Z_{diffTX}	72	100	120	Ω
Tx common mode impedance	$R_{TX\text{-}DC}$	18	—	30	Ω
Absolute DC common mode voltage between U1 and U0	$T_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$	—	—	200	mV
DC electrical idle differential output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0	—	10	mV
Note: 1. For recommended operating conditions, see Table 4.					

This table provides the USB 3.0 receiver DC electrical characteristics at the Rx package pins.

Table 44. USB 3.0 receiver DC electrical characteristics

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
Differential Rx input impedance	$R_{RX\text{-}DIFF\text{-}DC}$	72	100	120	Ω	—
Receiver DC common mode impedance	$R_{RX\text{-}DC}$	18	—	30	Ω	—
DC input CM input impedance for V > 0 during reset or power down	ZRX-HIGH-IMP-DC	25 K	—	—	Ω	—
LFPS detect threshold	$VRX\text{-}IDLE\text{-}DET\text{-}DC\text{-}DIFF_{pp}$	100	—	300	mV	1
Note:						

Table 44. USB 3.0 receiver DC electrical characteristics

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
1. Below the minimum is noise. Must wake up above the maximum.						

3.18.3 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at the Tx package pins.

Table 45. USB 3.0 transmitter AC timing specifications[1]

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Speed	—	—	5.0	—	Gb/s	—
Transmitter eye	t_{TX-Eye}	0.625	—	—	UI	—
Unit interval	UI	199.94	—	200.06	ps	2
AC coupling capacitor	AC coupling capacitor	75	—	200	nF	—
Note: 1. For recommended operating conditions, see Table 4. 2. UI does not account for SSC-caused variations.						

This table provides the USB 3.0 receiver AC timing specifications at Rx package pins.

Table 46. USB 3.0 receiver AC timing specifications[1]

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Unit interval	UI	199.94	—	200.06	ps	2
Notes: 1. For recommended operating conditions, see Table 4. 2. UI does not account for SSC-caused variations.						

3.18.4 USB 3.0 LFPS specifications

This table provides the key LFPS electrical specifications at the transmitter.

Table 47. LFPS electrical specifications at the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Period	tPeriod	20	—	100	ns	—

Table continues on the next page...

Table 47. LFPS electrical specifications at the transmitter (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Peak-to-peak differential amplitude	$V_{TX-DIFF-PP-LFPS}$	800	—	1200	mV	—
Rise/fall time	$t_{RiseFall2080}$	—	—	4	ns	1
Duty cycle	Duty cycle	40	—	60	%	1

Note:

1. Measured at compliance TP1. See Figure 26 for details.

This figure shows the Tx normative setup with reference channel as per USB 3.0 specifications.

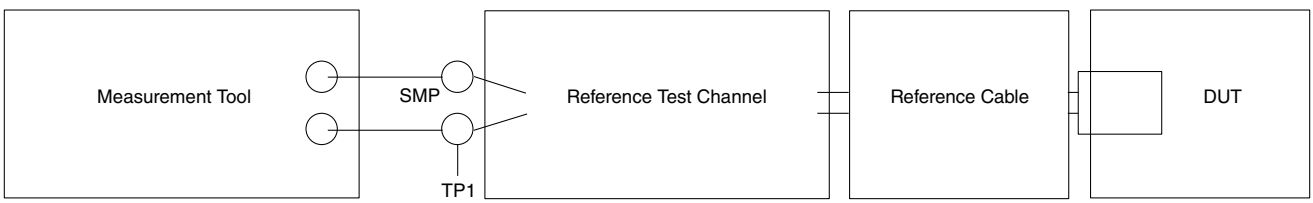


Figure 26. Tx normative setup

3.19 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SGMII and Serial ATA (SATA) data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.19.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

The figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 27 shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

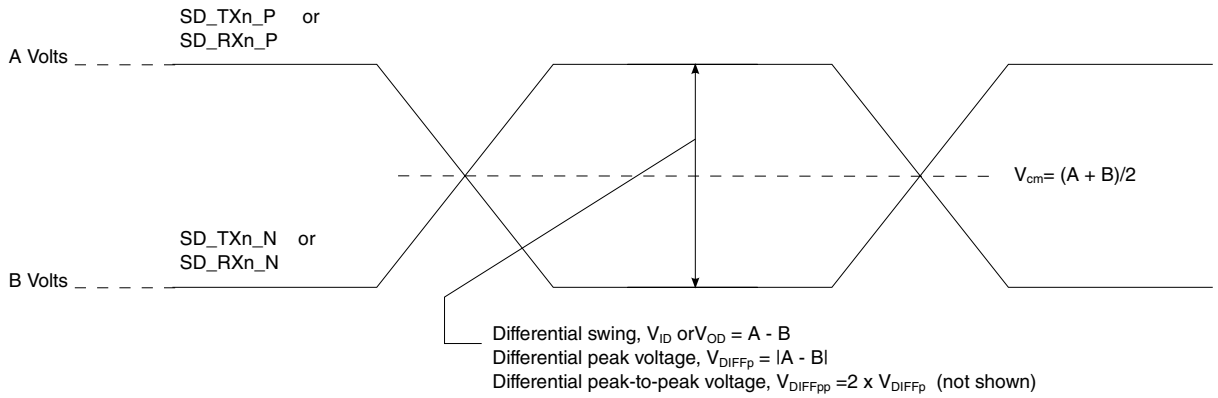


Figure 27. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage,V_{OD}(or Differential Output Swing):

The differential output voltage (or swing) of the transmitter,V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TXn\_P} - V_{SD\_TXn\_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing):

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RXn\_P} - V_{SD\_RXn\_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage,V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_P, for example) from the non-inverting signal (SD_TX*n*_N, for example)

within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 32 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn\_P} + V_{SD\_TXn\_N}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these ouputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV_{p-p}.

3.19.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal phase-locked loop (PLL) whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK1_P and SD1_REF_CLK1_N.

SerDes may be used for various combinations of the following IP block based on the RCW configuration field SRDS_PRTCLn:

- SGMII (1.25 Gbaud or 3.125 Gbaud)
- PCIe (2.5 GT/s, 5 GT/s)
- SATA (1.5 Gbps, 3.0 Gbps, and 6.0 Gbps)

The following sections describe the SerDes reference clock requirements and provide application information.

3.19.2.1 SerDes spread-spectrum clock source recommendations

SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are designed to work with spread-spectrum clocking for the PCI Express protocol only with the spreading specification defined in Table 48. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The SerDes transmitter does not support spread-spectrum clocking for the SATA protocol. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

Spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum-supported protocols. For example, if spread-spectrum clocking is desired on a SerDes reference clock for the PCI Express protocol and the same reference clock is used for any other protocol, such as SATA or SGMII because of the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

This table provides the source recommendations for SerDes spread-spectrum clocking.

Table 48. SerDes spread-spectrum clock source recommendations [1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	-0.5	%	2

Notes:

1. At recommended operating conditions. See Table 4.
2. Only down-spreading is allowed.

3.19.2.2 SerDes reference clock receiver characteristics

The figure shows a receiver reference diagram of the SerDes reference clocks.

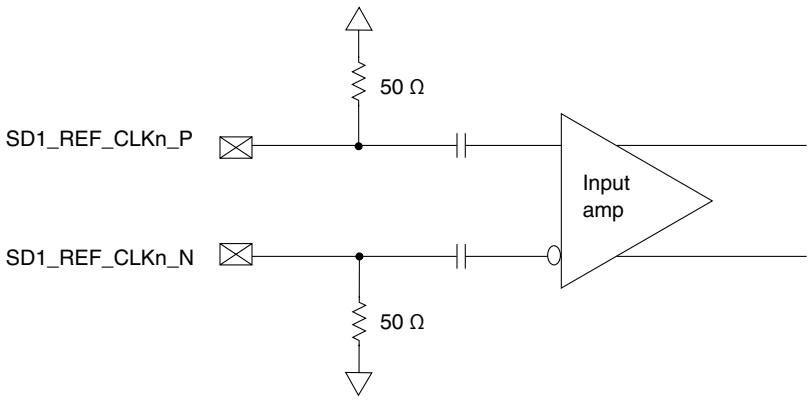


Figure 28. Receiver of SerDes reference clock

The characteristics of the clock signals are as follows:

- The SerDes receiver's core power supply voltage requirements (SV_{DD}) are as specified in Table 4.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SDn_REF_CLK_P and SDn_REF_CLK_N are internally AC-coupled differential inputs as shown in Figure 28. Each differential clock input (SDn_REF_CLK_P or SDn_REF_CLK_N) has on-chip 50-Ω termination to SD_GND1 followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SD_GND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK_P and SD*n*_REF_CLK_N inputs cannot drive 50 Ω to SD_GND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.19.2.3 DC level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. The figure shows the SerDes reference clock input requirement for DC-coupled connection scheme.

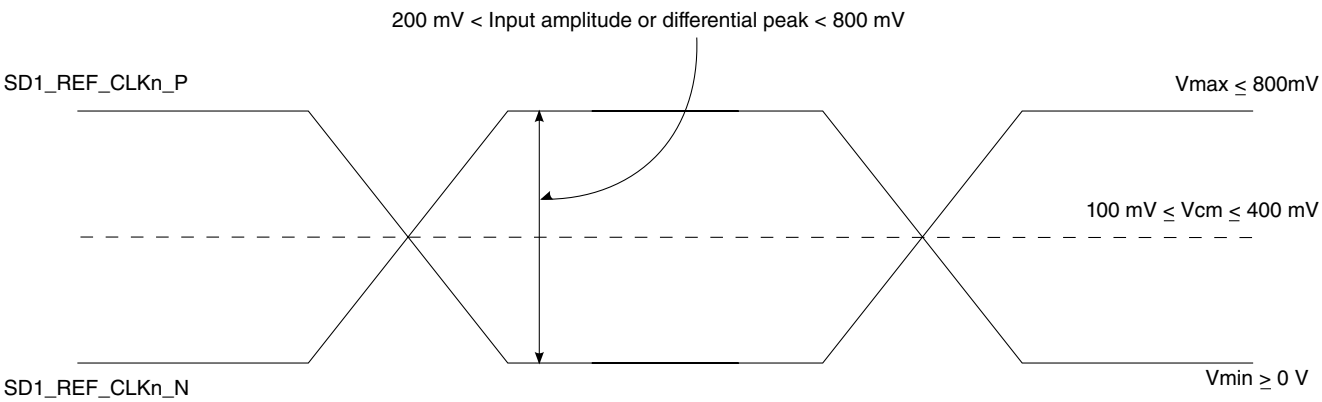


Figure 29. Differential reference clock input DC requirements (external DC-coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SD_GND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage SD_GND.
  - The figure shows the SerDes reference clock input requirement for AC-coupled connection scheme.

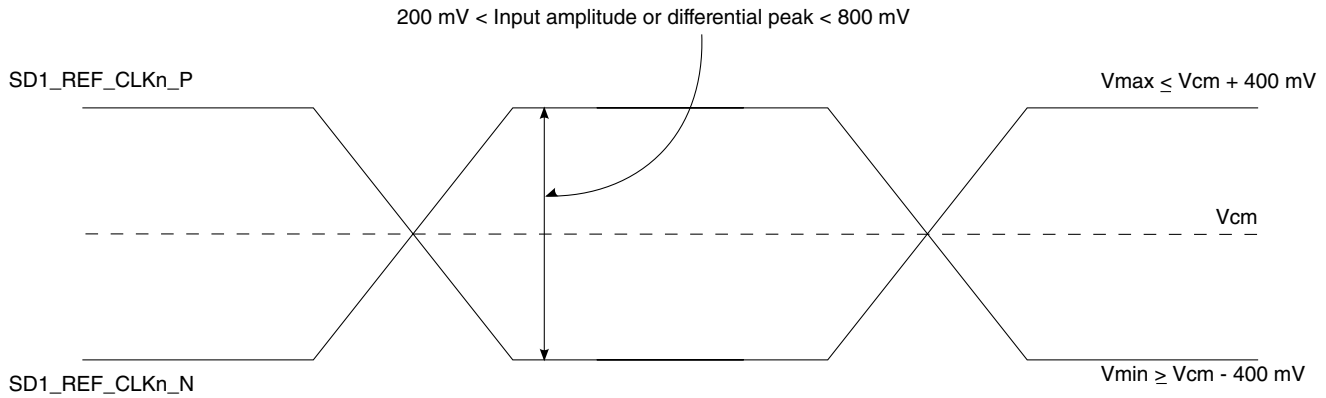


Figure 30. Differential reference clock input DC requirements (external AC-coupled)

- Single-ended mode
  - The reference clock can also be single-ended. The SD*n*_REF_CLK_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with SD*n*_REF_CLK_N either left unconnected or tied to ground.
  - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD*n*_REF_CLK_N) through the same source impedance as the clock input (SD*n*_REF_CLK_P) in use.
  - The SD*n*_REF_CLK_P input average voltage must be between 200 and 400 mV. The figure shows the SerDes reference clock input requirement for single-ended signaling mode.

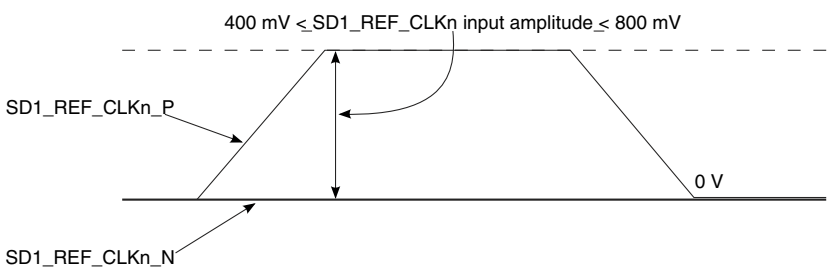


Figure 31. Single-ended reference clock input DC requirements

3.19.2.4 AC requirements for SerDes reference clocks

This table provides the AC requirements for the SerDes reference clocks for protocols running at data rates up to 6 Gbit/s.

This includes PCI Express (2.5 GT/s and 5 GT/s), SGMII (1.25 Gbaud and 3.125 Gbaud), and SATA (1.5 Gbps, 3.0 Gbps, and 6.0 Gbps). The SerDes reference clocks need to be verified by the customer's application design.

Table 49. SD1_REF_CLK_P and SD1_REF_CLK_N input clock requirements (SV_{DD} = 0.9 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N frequency range	t_{CLK_REF}	—	100/125	—	MHz	2
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-300	—	300	ppm	3
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-100	—	100	ppm	4
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	6
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	—	—	3	ps RMS	7
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	—	—	3.1	ps RMS	7
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N rising/ falling edge rate	t_{CLKRR}/t_{CLKFR}	0.6	—	4	V/ns	9
Differential input high voltage	V_{IH}	150	—	—	mV	5
Differential input low voltage	V_{IL}	—	—	-150	mV	5
Rising edge rate (SD*n*_REF_CLK*n*_P) to falling edge rate (SD*n*_REF_CLK*n*_N) matching	Rise-Fall Matching	—	—	20	%	10, 11

Notes:

1. For recommended operating conditions, see Table 4.

2. **Caution:** Only 100 and 125 have been tested. In-between values do not work correctly with the rest of the system.

3. For PCI Express (2.5 GT/s and 5 GT/s).

4. For SGMII and 2.5G SGMII.

5. Measurement taken from differential waveform.

6. Limits from PCI Express CEM Rev 2.0.

7. For PCI Express 5 GT/s, per PCI Express base specification Rev 3.0.

9. Measured from -150 mV to +150 mV on the differential waveform (derived from SD*n*_REF_CLK*n*_P minus SD*n*_REF_CLK*n*_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 32.

10. Measurement taken from single-ended waveform.

11. Matching applies to rising edge for SD*n*_REF_CLK*n*_P and falling edge rate for SD*n*_REF_CLK*n*_N. It is measured using a ±75 mV window centered on the median cross point where SD*n*_REF_CLK*n*_P rising meets SD*n*_REF_CLK*n*_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK*n*_P must be compared to the fall edge rate of SD*n*_REF_CLK*n*_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 33.

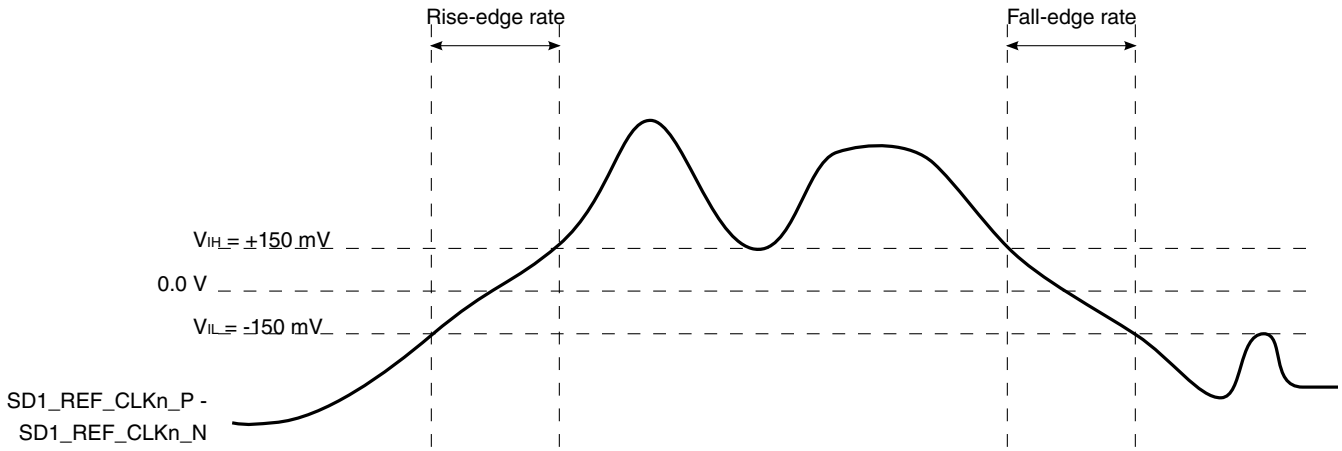


Figure 32. Differential measurement points for rise and fall time

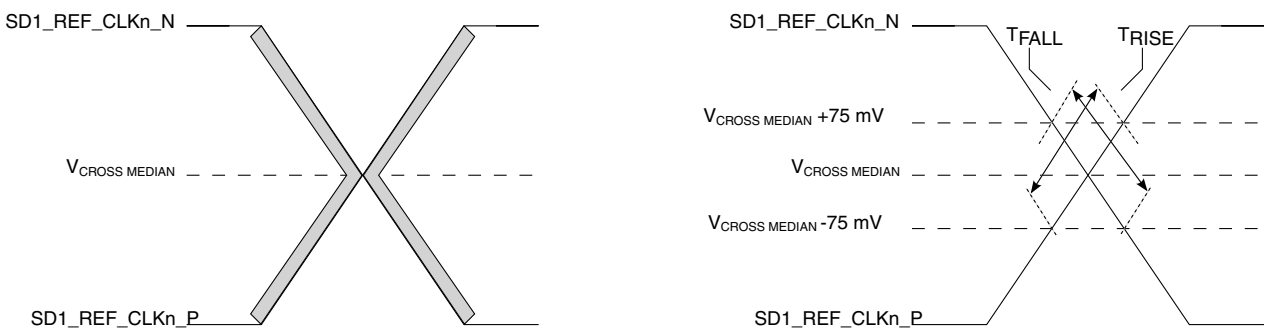


Figure 33. Single-ended measurement points for rise and fall time matching

3.19.3 SerDes transmitter and receiver reference circuits

The figure shows the reference circuits for the SerDes data lane's transmitter and receiver.

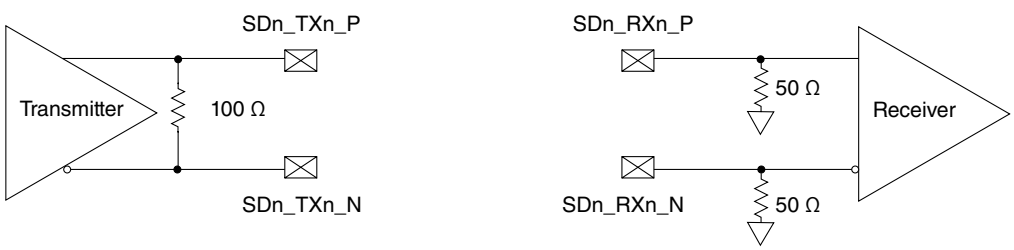


Figure 34. SerDes transmitter and receiver reference circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage :

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface

Note that external AC-coupling capacitor is required for the above serial transmission protocols per the protocol's standard requirements.

3.19.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.19.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.19.4.2 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.19.4.2.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 50. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Table continues on the next page...

Table 50. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35 V)[1] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Notes: 1. For recommended operating conditions, see Table 4.						

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 51. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states
Notes: 1. For recommended operating conditions, see Table 4.						

3.19.4.2.2 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 52. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications ($S1V_{DD}$ = 0.9 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.

Table continues on the next page...

Table 52. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications ($S1V_{DD}$ = 0.9 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 4.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 53. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications ($S1V_{DD}$ = 0.9 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Table continues on the next page...

Table 53. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications ($S1V_{DD}$ = 0.9 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes: 1. Measured at the package pins with a test load of 50 Ω to GND on each pin. 2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port. 3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground. 4. For recommended operating conditions, see Table 4.						

3.19.4.3 PCI Express AC physical layer specifications

This section describes the AC specifications for the physical layer of PCI Express on this device.

3.19.4.3.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 54. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all

Table continues on the next page...

Table 54. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
						edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Test and measurement load and measured over any 250 consecutive transmitter UIs.

2. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

4. For recommended operating conditions, see Table 4.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 55. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. See Note 1.
Transmitter deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI	-
Transmitter RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Test and measurement load and measured over any 250 consecutive transmitter UIs.

2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

3. For recommended operating conditions, see Table 4.

3.19.4.3.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 56. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Test and measurement load must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

4. For recommended operating conditions, see Table 4.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 57. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note:

1. For recommended operating conditions, see Table 4.

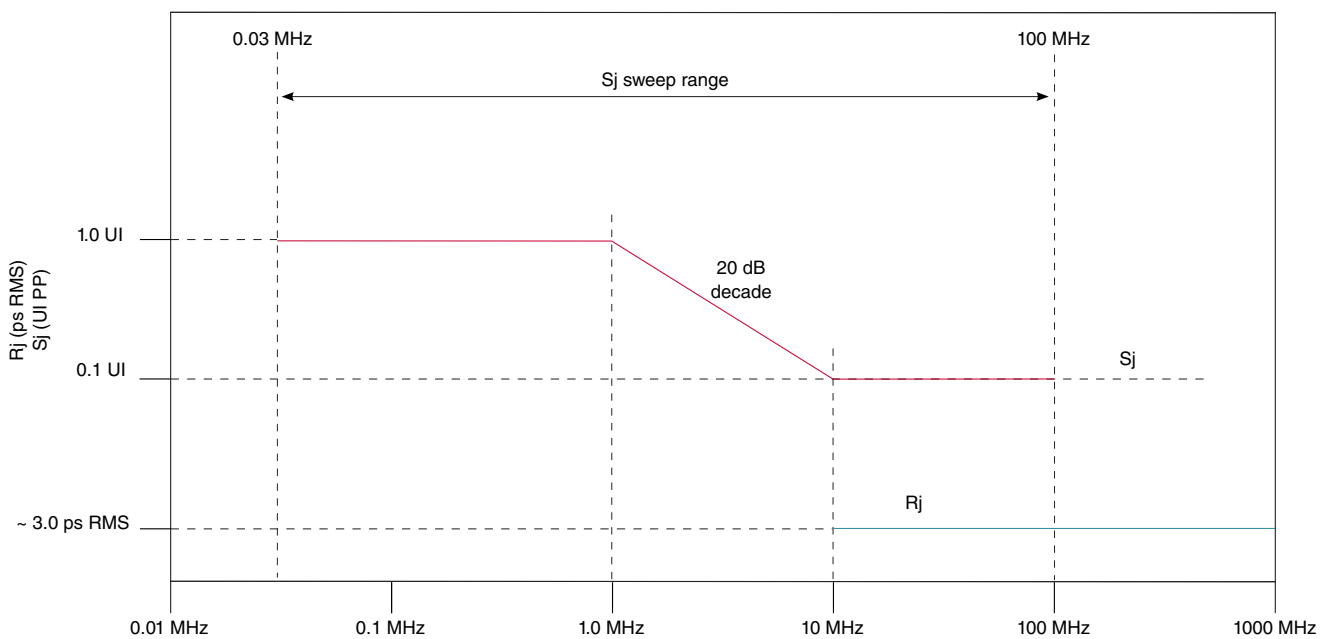


Figure 35. Swept sinusoidal jitter mask

3.19.4.4 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/ board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

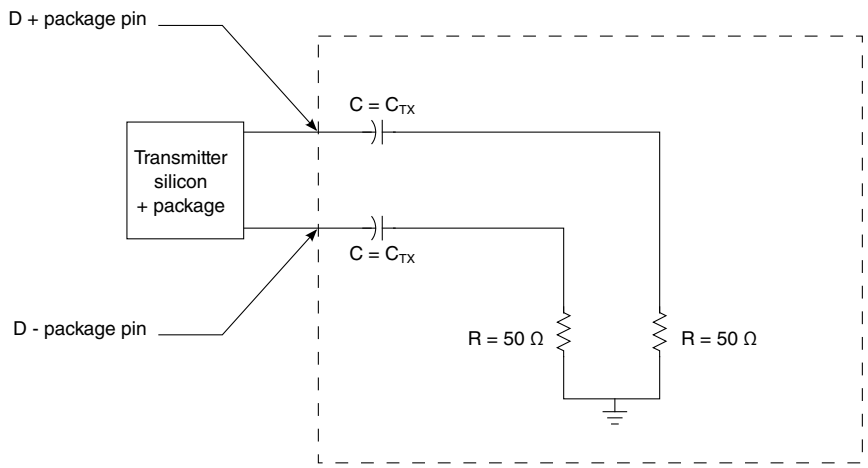


Figure 36. Test and measurement load

3.19.5 TX_CLK

The TX_CLK is AC-coupled 100 MHz differential clock output from the SerDes interface. TX_CLK uses Tx pair of SerDes lane. The Rx pair of the lane remains unused when this option is selected through RCW[SRDS_PRTCL]. For guidelines on termination of the RX pair, see the application note titled *QorIQ LS1012A Design Checklist* (AN5192).

3.19.5.1 TX_CLK DC specifications

This table shows the DC specifications for TX_CLK

Table 58. TX_CLK DC specifications (X1V_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p}$ = 2 x | V_{TX-D+} - V_{TX-D-} |
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance

Table continues on the next page...

Table 58. TX_CLK DC specifications ($X1V_{DD}$ = 1.35 V)[1] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. For recommended operating conditions, see Table 4.

3.19.5.2 TX_CLK AC specifications

This table lists the AC specifications for the TX_CLK output.

Table 59. TX_CLK AC specifications ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Clock frequency	f_{CLK}	99.97	100	100.03	MHz	2
Clock duty cycle	t_{CLK_DUTY}	40	50	60	%	
Max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	2
Total clock jitter at 10^{-6} BER (peak-to-peak jitter)	t_{CLK_TJ}	—	—	86	ps	2
10 kHz to 1.5 MHz RMS jitter	$t_{CLK-LF-RMS}$	—	—	3	ps	2
1.5 MHz to Nyquist RMS jitter	$t_{CLK-HF-RMS}$	—	—	3.1	ps	2
AC coupling capacitor	C_{TX}	75	—	200	nF	

Notes:

1. For recommended operating conditions, see Table 4.
2. Limits from PCI Express CEM Rev 2.0.
3. PCIe compatible driver has been used to generate the pattern for TX_CLK output.

3.19.6 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the SATA interface.

3.19.6.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.19.6.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission.

Table 60. Gen1i/1m 1.5 G transmitter DC specifications ($X1V_{DD}$ = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Notes:

1. Terminated by 50 Ω load.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 61. Gen 2i/2m 3 G transmitter DC specifications ($X1V_{DD}$ = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	—	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Notes:

1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 62. Gen 3i transmitter DC specifications ($S1V_{DD}$ = 0.9 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	240	—	900	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Notes:

1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 4.

3.19.6.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 63. Gen1i/1m 1.5 G receiver input DC specifications ($S1V_{DD}$ = 0.9 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 64. Gen2i/2m 3 G receiver input DC specifications ($S1V_{DD}$ = 0.9 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the Gen 3i differential receiver input DC characteristics for the SATA interface.

Table 65. Gen 3i receiver input DC specifications ($S1V_{DD}$ = 0.9 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	1000	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	200	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

3.19.6.2 SATA AC timing specifications

This section describes the SATA AC timing specifications.

3.19.6.2.1 AC requirements for SATA REF_CLK

This table provides the AC requirements for the SATA reference clock. These requirements must be guaranteed by the customer's application design.

Table 66. SATA reference clock input requirements[6]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLK1_P/SD1_REF_CLK1_N frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD1_REF_CLK1_P/SD1_REF_CLK1_N clock frequency tolerance	t_{CLK_TOL}	-350	—	+350	ppm	—
SD1_REF_CLK1_P/SD1_REF_CLK1_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD1_REF_CLK1_P/SD1_REF_CLK1_N cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD1_REF_CLK1_P/SD1_REF_CLK1_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50	—	+50	ps	2, 3, 4

Notes:

1. **Caution:** Only 100 and 125 MHz have been tested. All the intermediate values do not work correctly with the rest of the system.
2. At RefClk input.
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}.
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
5. Measurement taken from differential waveform.
6. For recommended operating conditions, see Table 4.

3.19.6.2.2 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 67. Gen 1i/1m 1.5 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.

Table 67. Gen 1i/1m 1.5 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
2. For recommended operating conditions, see Table 4.						

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 68. Gen 2i/2m 3 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1
Notes: 1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern. 2. For recommended operating conditions, see Table 4.						

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 69. Gen 3i transmitter AC specifications ($S1V_{DD}$ = 0.9 V)

Parameter	Symbol	Min	Typ	Max	Units
Speed	—	—	6.0	—	Gbps
Total jitter before and after compliance interconnect channel	J_T	—	—	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p
Unit interval	UI	166.6083	166.6667	167.5583	ps

3.19.6.2.3 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 70. Gen 1i/1m 1.5 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_RXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ250UI}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.
2. For recommended operating conditions, see Table 4.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 71. Gen 2i/2m 3 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.
2. For recommended operating conditions, see Table 4.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission The AC timing specifications do not include RefClk jitter.

Table 72. Gen 3i receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Total jitter after compliance interconnect channel	J_T	—	—	0.60	UI p-p	1
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p	1
Unit interval: 6.0 Gb/s	UI	166.6083	166.6667	167.5583	ps	—

Notes:

1. Measured at the receiver.
2. The AC specifications do not include RefClk jitter.

3.19.7 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 37, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 34.

3.19.7.1 SGMII clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N

When operating in SGMII mode, a SerDes reference clock is required. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.19.7.2 SGMII DC electrical characteristics

This section describes the electrical characteristics for the SGMII interface.

3.19.7.2.1 SGMII and SGMII 2.5G transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TX*n*_P and SD1_TX*n*_N)as shown in Figure 38.

Table 73. SGMII DC transmitter electrical characteristics ($X1V_{DD}$ = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3, 5] ($X1V_{DD-Typ}$ at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	LNmTECR0[AMP_RED]=0b000000
		293.8	459.0	665.6		LNmTECR0[AMP_RED]=0b000001
		266.9	417.0	604.7		LNmTECR0[AMP_RED]=0b000011
		240.6	376.0	545.2		LNmTECR0[AMP_RED]=0b000010
		213.1	333.0	482.9		LNmTECR0[AMP_RED]=0b000110
		186.9	292.0	423.4		LNmTECR0[AMP_RED]=0b000111
		160.0	250.0	362.5		LNmTECR0[AMP_RED]=0b010000

Table continues on the next page...

Table 73. SGMII DC transmitter electrical characteristics ($X1V_{DD}$ = 1.35 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:

1. This does not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD\_TXn\_P} - V_{SD\_TXn\_N}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.
3. The $|V_{OD}|$ value shown in the Typ column is based on the condition of X1VDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn_P and SDn_TXn_N.
4. For recommended operating conditions, see Table 4.
5. Example amplitude reduction setting for SGMII on lane A: LNaTECR0[AMP_RED] = 0b000001 for an output differential voltage of 459 mV typical.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

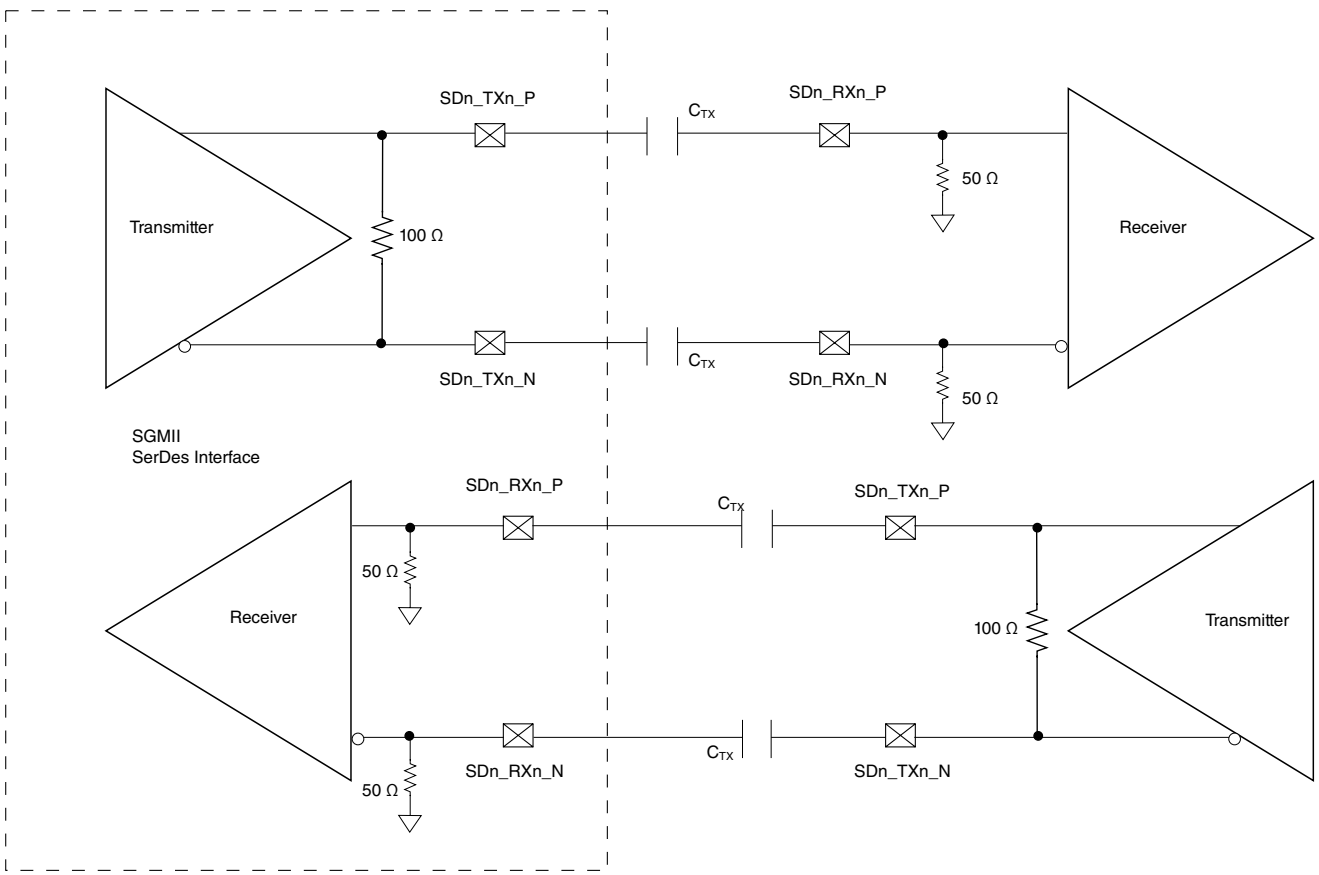


Figure 37. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

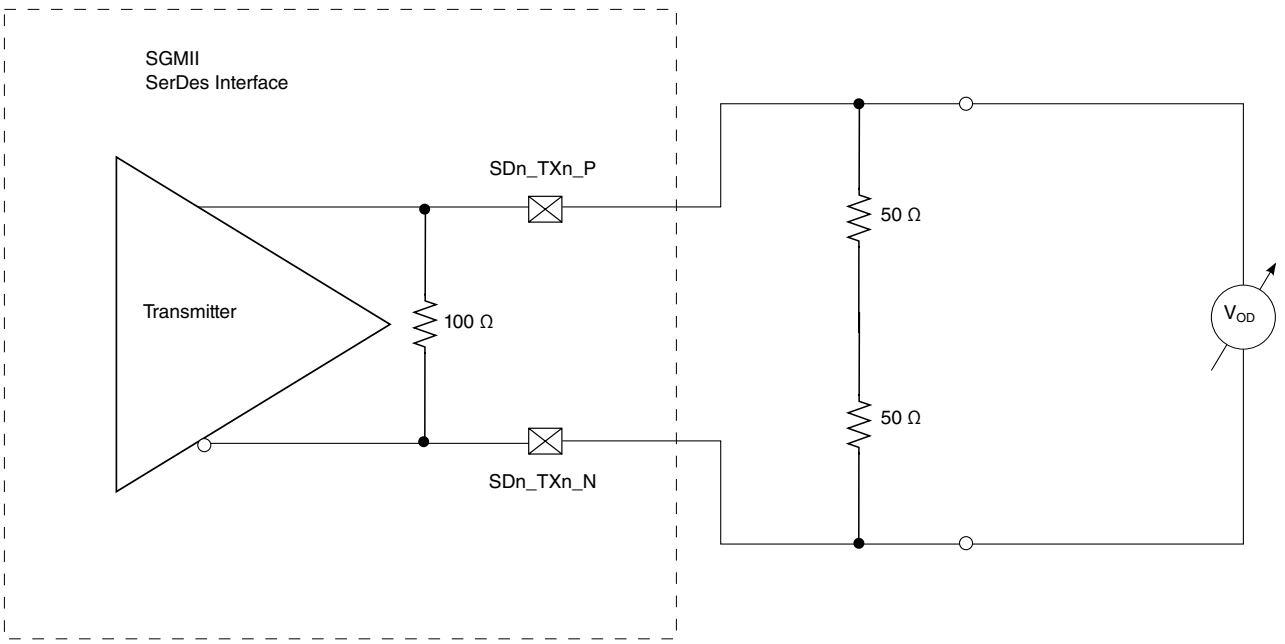


Figure 38. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5G transmitter DC electrical characteristics for 3.125 GBaud.

Table 74. SGMII 2.5G transmitter DC electrical characteristics ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	
Output impedance (differential)	R_O	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 4.						

3.19.7.2.2 SGMII and SGMII 2.5G DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 75. SGMII DC receiver electrical characteristics ($S1V_{DD}$ = 0.9V)[4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	REIDL_TH = 001	$V_{RX\_DIFFp\text{-}p}$	100	-	1200	mV	2, 5
	REIDL_TH = 100		175	-			
Loss of signal threshold	REIDL_TH = 001	V_{LOS}	30	-	100	mV	3, 5
	REIDL_TH = 100		65	-	175		

Table continues on the next page...

Table 75. SGMII DC receiver electrical characteristics ($S1V_{DD}$ = 0.9V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express DC physical layer receiver specifications, for further explanation.
4. For recommended operating conditions, see Table 4.
5. The REIDL_TH shown in the table refers to the chip's SRDSxLNmGCR1[REIDL_TH] bit field.

This table defines the SGMII 2.5G receiver DC electrical characteristics for 3.125 GBaud.

Table 76. SGMII 2.5G receiver DC timing specifications ($S1V_{DD}$ = 0.9V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\_DIFFp\text{-}p}$	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. For recommended operating conditions, see Table 4.

3.19.7.3 SGMII AC timing specifications

This section describes the AC timing specifications for the SGMII interface.

3.19.7.3.1 SGMII and SGMII 2.5G transmit AC timing specifications

This table provides the SGMII and SGMII 2.5G transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 77. SGMII transmit AC timing specifications[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	-	-	0.17	UI p-p	-
Total jitter	JT	-	-	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Table continues on the next page...

Table 77. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AC coupling capacitor	C_{TX}	10	-	200	nF	3

Notes:

1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
2. See Figure 1 for single frequency sinusoidal jitter measurements.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.
4. For recommended operating conditions, see Table 4.

3.19.7.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

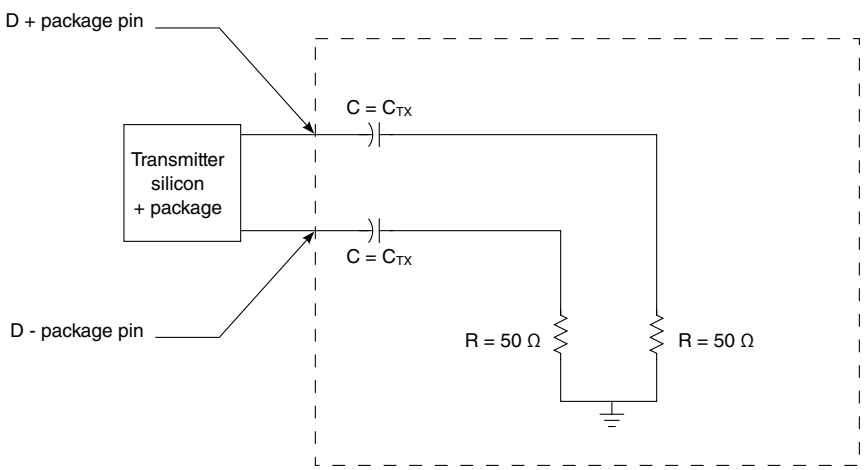


Figure 39. SGMII AC test/measurement load

3.19.7.3.3 SGMII and SGMII 2.5G receiver AC timing Specification

This table provides the SGMII and SGMII 2.5G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 78. SGMII Receive AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1

Table continues on the next page...

Table 78. SGMII Receive AC timing specifications[3] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error ratio	BER	-	-	10^{-12}	-	-
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver

2.Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of the figure given below. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

3. For recommended operating conditions, see Table 4.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

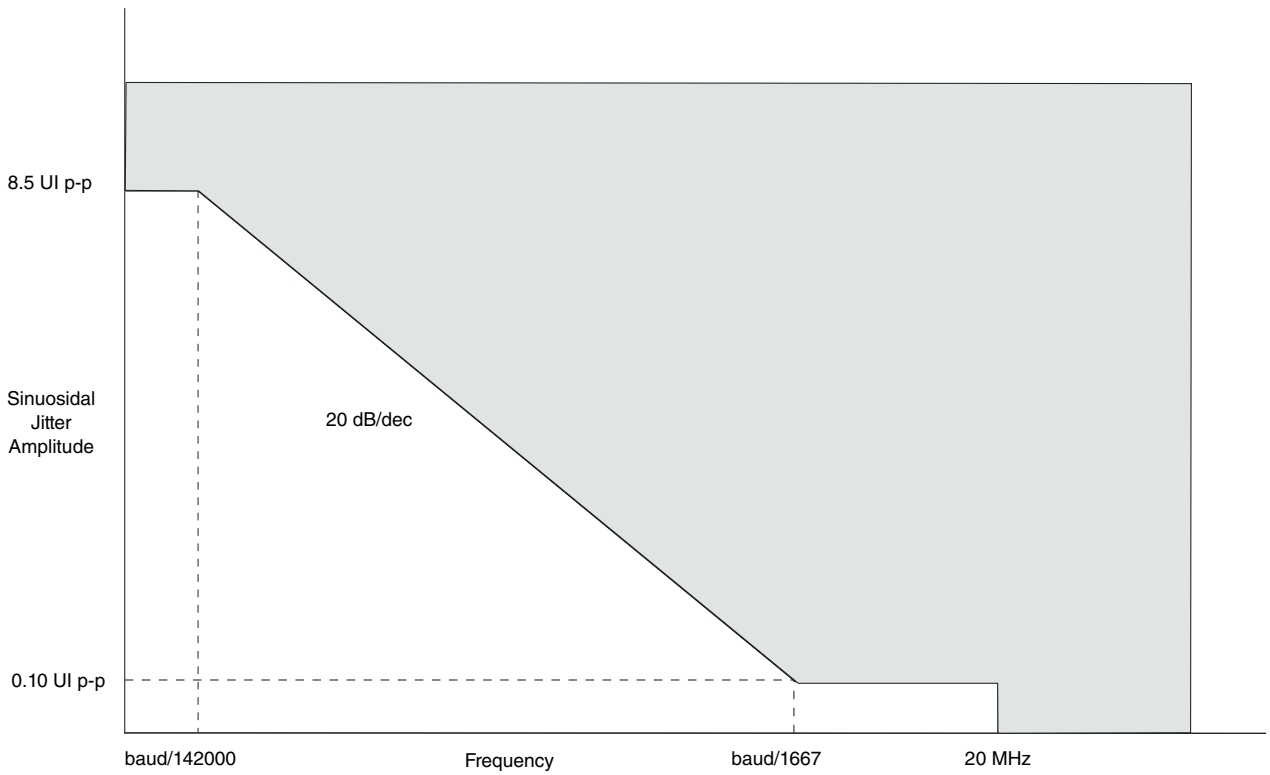


Figure 40. Single-frequency sinusoidal jitter limits

3.20 I2C

This section describes the DC and AC electrical characteristics for the I2C interfaces.

3.20.1 I2C DC electrical characteristics

Table below provides the DC electrical characteristics for the I2C interfaces when operating at $O1V_{DD}$ = 1.8 V.

Table 79. I2C DC electrical characteristics ($O1V_{DD}$ = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $O1V_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.3 x $O1V_{DD}$	V	1
Output low voltage ($O1V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	0	0.2 x $O1V_{DD}$	V	-
Pulse width of spikes that must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between 0.1 x $O1V_{DD}$ and 0.9 x $O1V_{DD}$ (max)	I_I	-10	10	μA	3
Capacitance for each I/O pin	C_I	-	10	pF	-

Notes:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $O1V_{IN}$ values found in Table 4.
2. Refer to the *QorIQ LS1012A Reference Manual* for information about the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if $O1V_{DD}$ is switched off.
4. For recommended operating conditions, see Table 4.

3.20.2 I2C AC timing specifications

This table provides the AC timing specifications for the I2C interfaces.

Table 80. I2C AC timing specifications

Parameter		Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency		f_{I2C}	0	400	kHz	2
Low period of the SCL clock		t_{I2CL}	1.3	-	μs	-
High period of the SCL clock		t_{I2CH}	0.6	-	μs	-
Setup time for a repeated START condition		t_{I2SVKH}	0.6	-	μs	-
Hold time (repeated) START condition (after this period, the first clock pulse is generated)		t_{I2SXKL}	0.6	-	μs	-
Data setup time		t_{I2DVKH}	100	-	ns	-
Data input hold time	CBUS compatible masters	t_{I2DXKL}	-	-	μs	3
	I^2C bus devices		0	-		
Data output delay time		t_{I2OVKL}	-	0.9	μs	4
Setup time for STOP condition		t_{I2PVKH}	0.6	-	μs	-
Bus free time between a STOP and START condition		t_{I2KHDX}	1.3	-	μs	-

Table continues on the next page...

Table 80. I2C AC timing specifications (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 x O1V_{DD}	-	V	-
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 x O1V_{DD}	-	V	-
Capacitive load for each bus line	C_b	-	400	pF	-

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I_2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

2. The requirements for I^2C frequency calculation must be followed. *See Determining the I2C Frequency Divider Ratio for SCL (AN2919).*"

3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I^2C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, *see Determining the I2C Frequency Divider Ratio for SCL (AN2919)* .

4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

5. For recommended operating conditions, see Table 4.

This figure provides the AC test load for the I^2C.

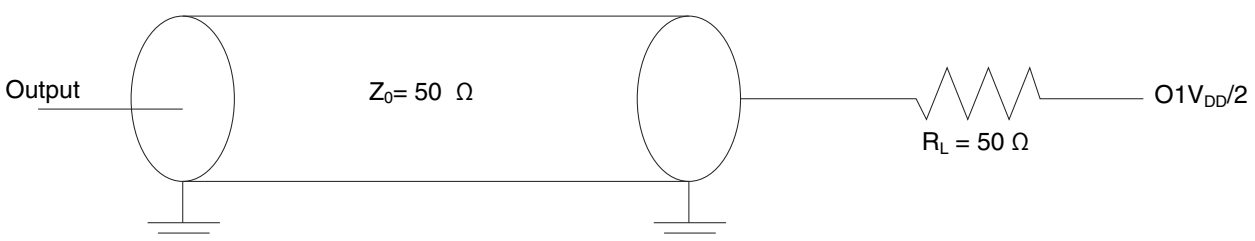


Figure 41. I^2C AC test load

This figure shows the AC timing diagram for the I^2C bus.

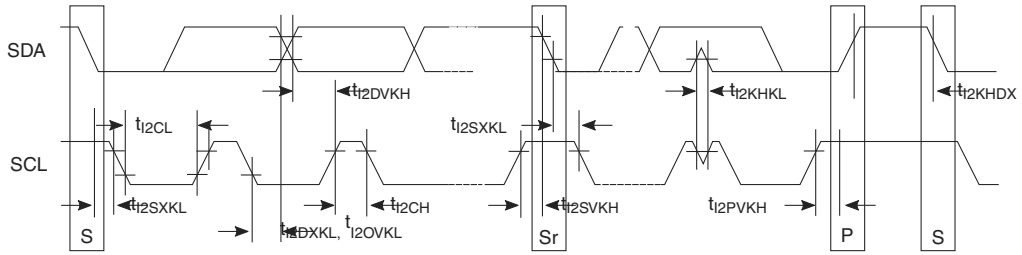


Figure 42. I²C Bus AC timing diagram

3.21 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.21.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 81. JTAG DC electrical characteristics ($O2V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $O2V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $O2V_{DD}$	V	1
Input current ($O2V_{IN}$ = 0 V or $O2V_{IN}$ = $O2V_{DD}$)	I_{IN}	—	-100 / +50	µA	2
Output high voltage ($O2V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($O2V_{DD}$ = min, I_{OL}= 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum $O2V_{IN}$ values found in Table 4.
2. The symbol V_{IN}, in this case, represents the $O2V_{IN}$ symbol found in Table 4.
3. For recommended operating conditions, see Table 4.

3.21.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in the following figures.

Table 82. JTAG AC timing specifications

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	-
JTAG external clock cycle time	t_{JTG}	30	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	-
TRST_B assert time	t_{TRST}	25	-	ns	2
Input setup times	t_{JTDVKH}	4	-	ns	-
Input hold times	t_{JTDXKH}	10	-	ns	-
Output valid times				ns	3
Boundary-scan data	t_{JTKLDV}	-	15		
TDO		-	10		
Output hold times	t_{JTKLDX}	0	-	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. TRST_B is an asynchronous level sensitive signal. The set-up time is for test purposes only.

3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

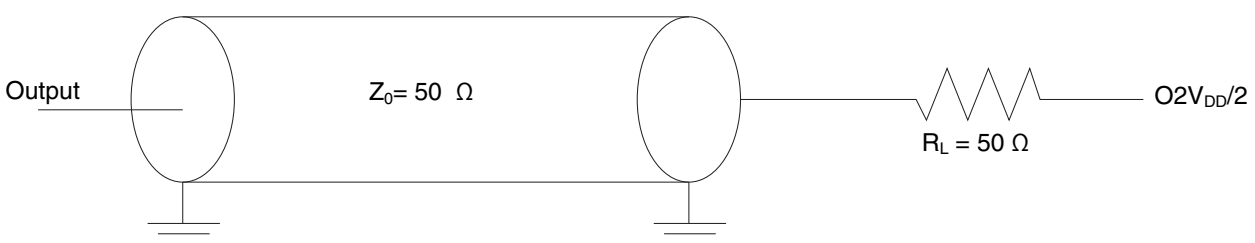


Figure 43. AC test Load for the JTAG interface

This figure provides the JTAG clock input timing diagram.

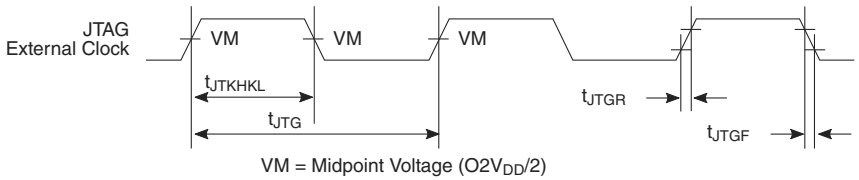


Figure 44. JTAG clock input timing diagram

This figure provides the TRST timing diagram.

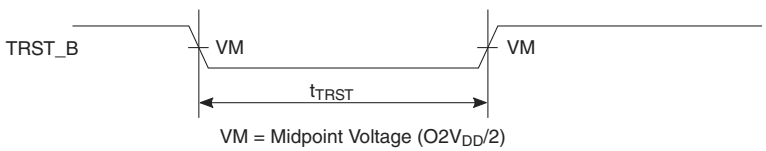


Figure 45. TRST_B timing diagram

This figure provides the boundary-scan timing diagram.

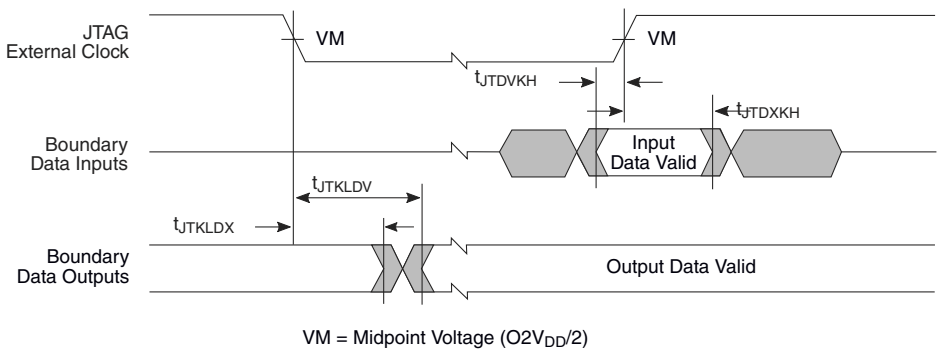


Figure 46. Boundary-Scan timing diagram

3.22 SPI interface

This section describes the DC and AC electrical characteristics for the SPI interface.

3.22.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface operating at $O1V_{DD}$ = 1.8 V.

Table 83. SPI DC electrical characteristics ($O1V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $O1V_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.3 x $O1V_{DD}$	V	1

Table continues on the next page...

Table 83. SPI DC electrical characteristics ($O1V_{DD}$ = 1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0 V or V_{IN} = $O1V_{DD}$)	I_{IN}	—	±50	μA	2
Output high voltage ($O1V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($O1V_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum $O1V_{IN}$ values found in Table 4.

2. The symbol V_{IN}, in this case, represents the $O1V_{IN}$ symbol referenced in Table 4.

3. For recommended operating conditions, see Table 4.

3.22.2 SPI AC timing specifications

This table provides the SPI timing specifications.

Table 84. SPI AC timing specifications

Parameter	Symbol	Condition	Min	Max	Unit	Notes
SCK Clock Pulse Width	t_{SDC}	—	40%	60%	t_{SCK}	
CS to SCK Delay	t_{CSC}	Master	tp*2 -5	—	ns	1, 2
After SCK Delay	t_{ASC}	Master	tp*2 -1	—	ns	1, 3
Data Setup Time for Inputs	t_{NIIVKH}	Master	9	—	ns	
Data Hold Time for Inputs	t_{NIIXKH}	Master	0	—	ns	
Data Valid (after SCK edge) for Outputs	t_{NIKHOV}	Master	—	5	ns	
Data Hold Time for Outputs	t_{NIKHOX}	Master	0	—	ns	

Notes:

1. tp represent the time period for platform clock.

2. Refer the CTARx register in QorIQ LS1012ARM for more details. The tCSC = tp*(Delay Scaler Value)*CTARx[PCSSCK] -5.0, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the tCSC = tp*4*3-5.0 when CTARx[PCSSCK] = 0b01, CTARx[CSSCK]=0b0001.

3. Refer the CTARx register in QorIQ LS1012ARM for more details. The tASC = tp*(Delay Scaler Value)*CTARx[PASC] -1.0, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the tASC = tp*8*3-1.0 when CTARx[PASC] = 0b01, CTARx[ASC]=0b0010.

This figure shows the SPI timing master when CPHA = 0.

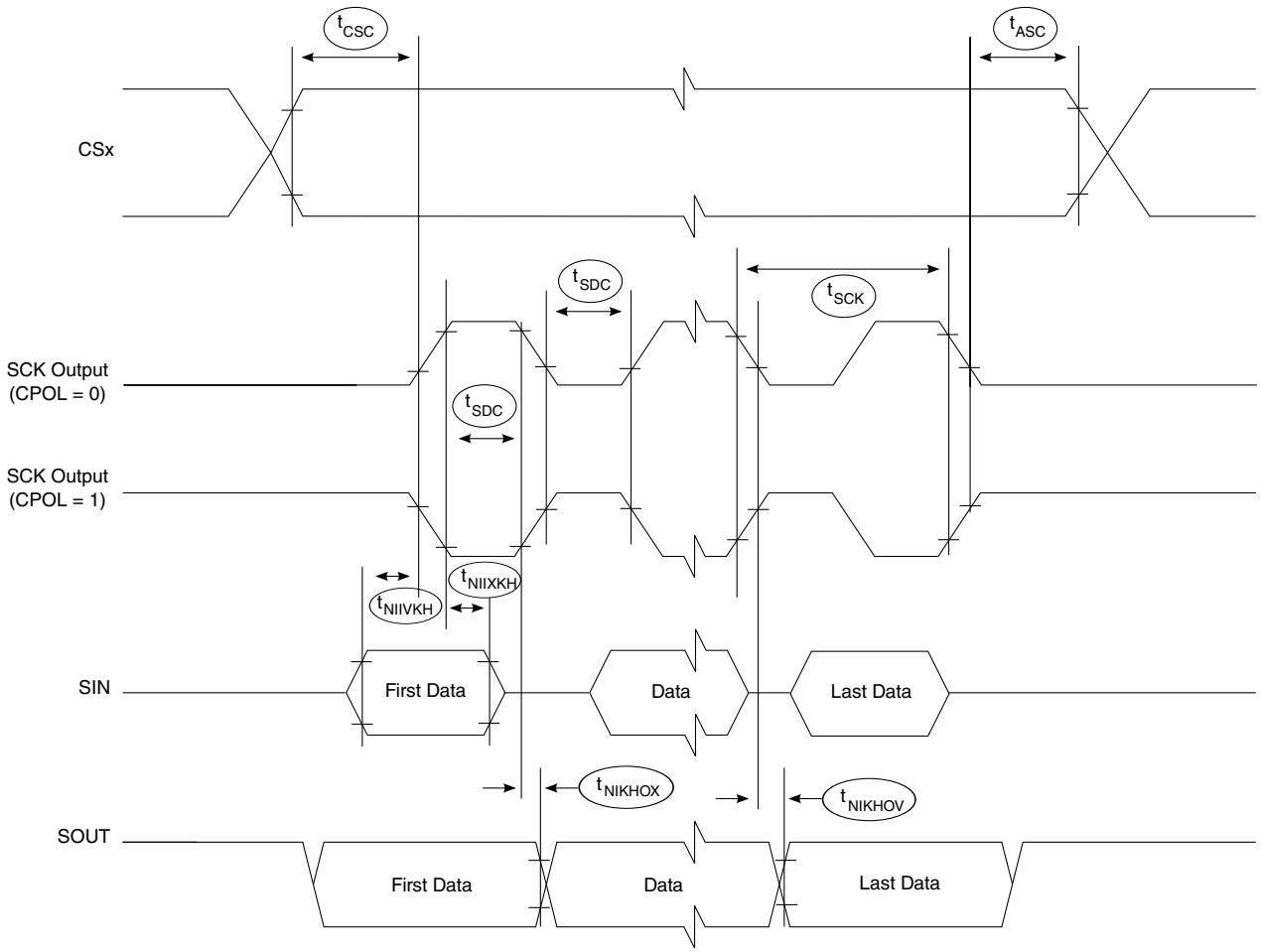


Figure 47. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

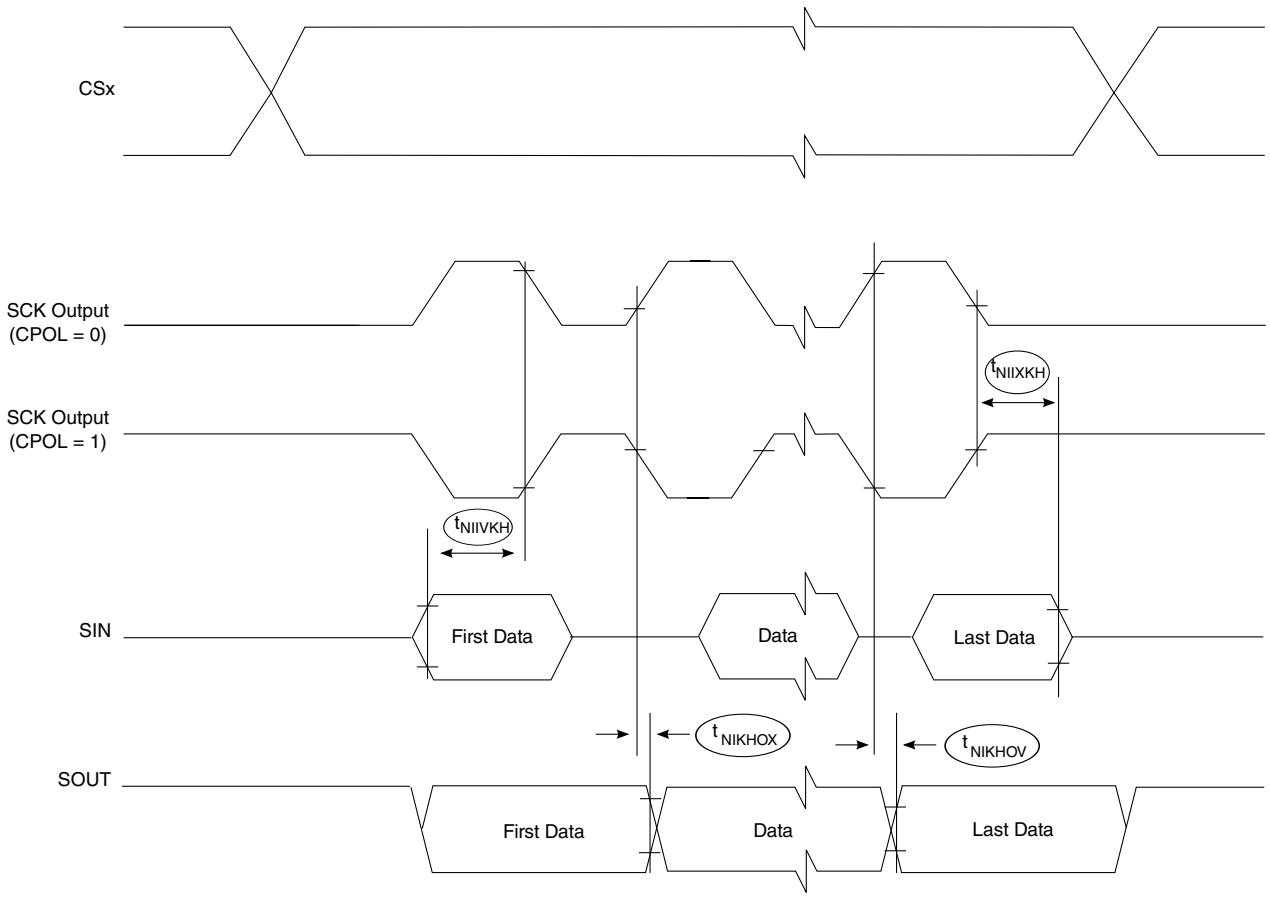


Figure 48. SPI timing master, CPHA = 1

3.23 QuadSPI interface

This section describes the DC and AC electrical characteristics for the QuadSPI interface.

3.23.1 QuadSPI DC electrical characteristics

This table provides the DC electrical characteristics for the QuadSPI interface operating at $O1V_{DD}$ = 1.8 V.

Table 85. QuadSPI DC electrical characteristics ($O1V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $O1V_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.3 x $O1V_{DD}$	V	1

Table continues on the next page...

Table 85. QuadSPI DC electrical characteristics ($O1V_{DD}$ = 1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current ($O1V_{IN}$ = 0 V or $O1V_{IN}$ = $O1V_{DD}$)	I_{IN}	-	±50	μA	2
Output high voltage ($O1V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage ($O1V_{DD}$= min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max values found in Table 4.
2. The symbol V_{IN}, in this case, represents the $O1V_{IN}$ symbol referenced in Table 4.
3. At recommended operating conditions with $O1V_{DD}$=1.8 V. For detailed recommended operating conditions, see Table 4.

3.23.2 QuadSPI AC timing specifications

This section describes the QuadSPI timing specifications in Single data rate (SDR) mode. All data is based on a negative edge data launch and a positive edge data capture for the flash device. Double data rate (DDR)/Double trasfer rate (DTR) mode is not supported.

3.23.2.1 QuadSPI timing SDR mode

This table provides the QuadSPI input and output timing in SDR mode.

Table 86. SDR mode QuadSPI input and output timing

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency	F_{SCK}	—	83.3	MHz	
Clock rise/fall time	T_{RISE}/T_{FALL}	1	—	ns	
CS output hold time	$t_{NIKHOX2}$	-3.4+j*T	—	ns	1, 2
CS output delay	$t_{NIKHOV2}$	-3.5+k*T	—	ns	1, 3
Setup time for incoming data	t_{NIIVKH}	3.8	—	ns	
Hold time requirement for incoming data	t_{NIIXKH}	1	—	ns	
Output data delay	t_{NIKHOV}	—	2.7	ns	
Output data hold	t_{NIKHOX}	-2.7	—	ns	

Notes:

1. T represents the clock period.
2. j represents qSPI_FLSHCR[TCSH].

Table 86. SDR mode QuadSPI input and output timing

Parameter	Symbol	Min	Max	Unit	Notes
3. k depends on qSPI_FLSHCR[TCSS].					

This figure shows the QuadSPI AC timing in SDR mode.

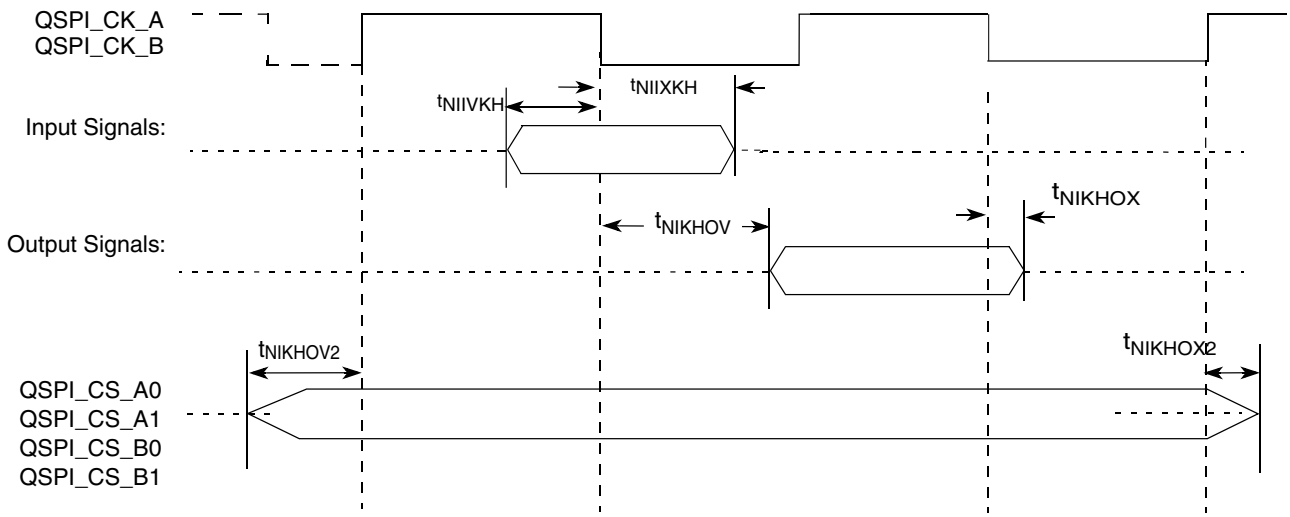


Figure 49. QuadSPI AC timing — SDR mode

3.23.3 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC-coupled operation is supported.

3.23.3.1 1000Base-KX DC electrical characteristics

3.23.3.1.1 1000Base-KX Transmitter DC Specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TXn_P and SD1_TXn_N).

Table 87. 1000Base-KX Transmitter DC Specifications

Parameter	Symbols	Min	Typ	Max	Units	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800	-	1600	mV	1
Differential resistance	T_{RD}	80	100	120	ohm	-

Table continues on the next page...

Table 87. 1000Base-KX Transmitter DC Specifications (continued)

Parameter	Symbols	Min	Typ	Max	Units	Notes
Notes: 1. LNmTECR0[AMP_RED]=00_0000. 2. For recommended operating conditions, see Recommended operating conditions.						

3.23.3.1.2 1000Base-KX Receiver DC Specifications

Table below provides the 1000Base-KX receiver DC timing specifications.

Table 88. 1000Base-KX Receiver DC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Input differential voltage	$V_{RX-DIFFp-p}$	-	-	1600	mV	1
Differential resistance	T_{RDIN}	80	-	120	ohm	-
Notes: 1. For recommended operating conditions, see Recommended operating conditions.						

3.23.3.2 1000Base-KX AC electrical characteristics

3.23.3.2.1 1000Base-KX Transmitter AC Specifications

Table below provides the 1000Base-KX transmitter AC specification.

Table 89. 1000Base-KX Transmitter AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated High Probability Jitter/ Random Jitter	$T_{UHPJ}T_{RJ}$	-	-	0.15	UI p-p	-
Deterministic Jitter	T_{DJ}	-	-	0.10	UI p-p	-
Total Jitter	T_{TJ}	-	-	0.25	UI p-p	1
Notes: 1. Total jitter is specified at a BER of 10^{-12}. 2. For recommended operating conditions, see Recommended operating conditions.						

3.23.3.2.2 1000Base-KX Receiver AC Specifications

Table below provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

Table 90. 1000Base-KX Receiver AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Receiver Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Random Jitter	R_{RJ}	-	-	0.15	UI p-p	1
Sinusoidal Jitter, maximum	R_{SJ-max}	-	-	0.10	UI p-p	2
Total Jitter	R_{TJ}	-	-	See Note 3	UI p-p	2

Notes:

1. Random jitter is specified at a BER of 10^{-12}.
2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.
3. Per IEEE 802.3ap-clause 70.
4. The AC specifications do not include Refclk jitter.
5. For recommended operating conditions, see Recommended operating conditions.

4 Hardware design considerations

4.1 Clock ranges

This section provides the clocking specifications for the processor core, platform, and memory.

Table 91. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency		Unit
	Min	Max	
Core cluster group PLL frequency (LS1012A Rev 2.0 only)	600	1000	MHz
Core cluster group PLL frequency	600	800	MHz
Platform clock frequency	250	250	MHz
Memory Bus Clock Frequency (DDR3L)	500	500	MHz

5 Thermal characteristics

Table 92 provides the package thermal characteristics of the LS1012A.

Table 92. Package thermal characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	52.7	°C/W
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	27.2	°C/W
Junction-to-ambient, Moving Air (at 1 m/s)	Single layer board (1s)	$R_{\theta JMA}$	40.7	°C/W
Junction-to-ambient, Moving Air (at 1 m/s)	Four layer board (2s2p)	$R_{\theta JMA}$	22.0	°C/W
Junction-to-board	Four layer board (2s2p)	$R_{\theta JB}$	10.7	°C/W
Junction-to-case (Top)	-	$R_{\theta JCtop}$	6	°C/W
Junction-to-Mold-top	-	$R_{\theta JMT}$	4.4	°C/W

Notes:

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-2A.
2. Junction-to-Ambient, Moving Air Thermal Resistance determined per JEDEC JESD51-6.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Thermal test board meets JEDEC specification for this package (JESD51-9). Thermal vias are incorporated in 2s2p test board in accordance to JESD51-9 guidelines.
5. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
6. Junction-to-Mold Top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the mold top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.

5.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

5.2 Temperature diode

The chip has temperature diodes that can be used to monitor its temperature by using some external temperature monitoring devices (such as ADT7481A™).

The following are the specifications of the chip's on-board temperature diode:

- Operating range: 10 - 230 μA
- Ideality factor over temperature range 85° C to 105° C, n = 1.006 ± 0.003, with approximate error ± 1° C and error under ± 3° C for temperature range 0° C to 85° C.

5.3 Thermal management information

This section describes the thermal management information for the molded flip-chip, land grid array (FC-LGA) package for air-cooled applications. Heat extraction from the package is primarily dependant on the attached cooling solution, board attributes and ambient/environmental conditions around the package. When an effective cooling solution is attached to the topside of the package, a significant amount of heat will extracted in that direction. If there is no cooling solution attached to the package, the primary heat loss path will be through the package lands to the motherboard. The FCLGA package is designed with a unique LGA map where ground and power pins are clustered in the centre of the package, under the die shadow area. This feature allows for effective heat transfer to the motherboard. The need for heat sinks or any cooling solution ultimately depends on the use condition and system environment. This figure illustrates a typical heat transfer paths and thermal resistances that is associated with this package.

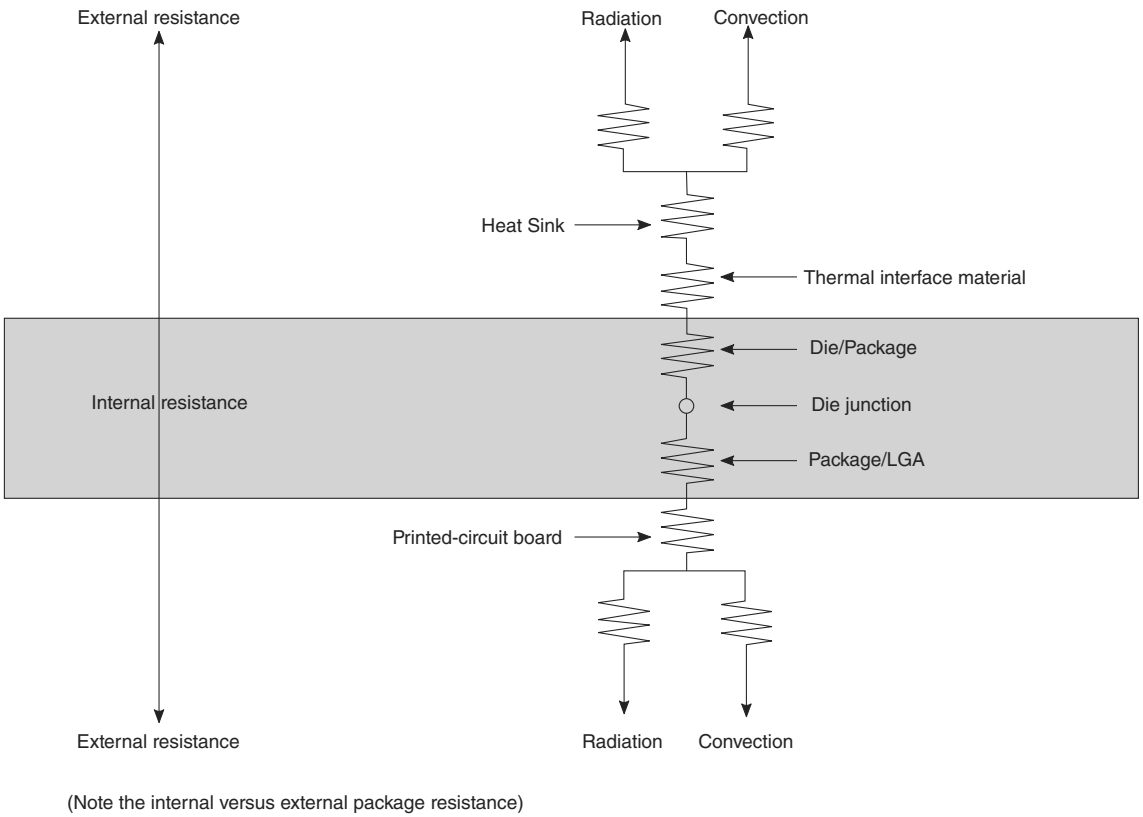


Figure 50. Package with heat sink mounted to a printed-circuit board

5.3.1 Bare package heat transfer

This section describes a scenario where there is no heat sink or cooling solution attached on the top side of the package. Bulk of the heat generated in the die will be channelled to the PC board through the package substrate and land grid array. The land grid array of this package is designed to facilitate routing of all dual-row perimeter pins on the top metal layer of the PC board using standard design rules. This enables placement of copper planes in the internal and bottom layers of a four layer PC board for thermal dissipation, power and ground. The PC board drawing in Figure 51 illustrates this. The PC board's power/ground plated through holes (PTH) or via will channel heat from the package to the PC board's internal copper planes. The centrally positioned ground and power pins under the die shadow (that is, the heat source) area significantly aids this mode of heat transfer.

5.3.2 Heat sink and thermal interface materials

A topside heat sink may or may not be needed for the molded FC-LGA depending on use case and environmental conditions. The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink should be attached to the printed circuit board with the spring force centred over package. This spring force should not exceed 40 Newtons.

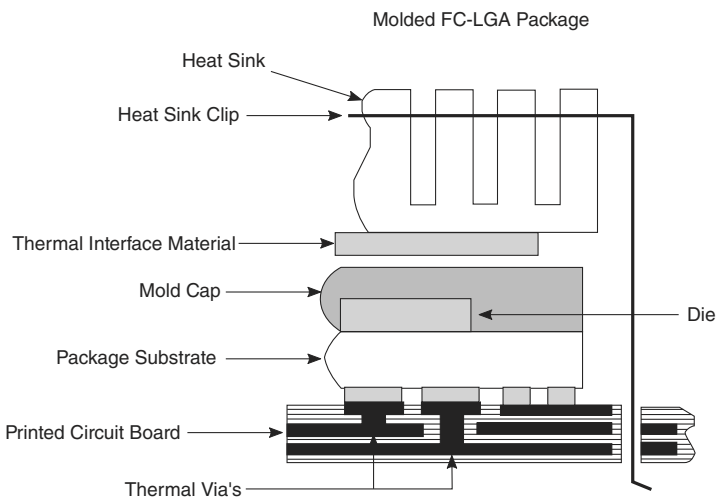


Figure 51. Package exploded, cross-sectional view - molded FC-LGA

The system thermal engineer can choose among several types of commercially-available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly and cost.

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board.

5.3.3 Gap filler thermal pads

In a scenario where there is a lack of volumetric space or headroom above the package for a heat sink, gap filler thermal pads can be used to fill the space between the package and the structure above it. Usually, this structure is the inner chassis skin but may also be

a wide metal heat spreader shared by multiple packages on the same side of the PC board. Gap filler thermal pads are essentially a thicker form of thermal interface material with thicknesses ranging from 0.25 to 5 mm. The presence of the thermal pads will facilitate heat transfer from the top side of the package thus aiding in package temperature reduction. There are many commercially available materials that should be selected based on the target thickness and thermal conductivity that best suits the use application.

6 Package information

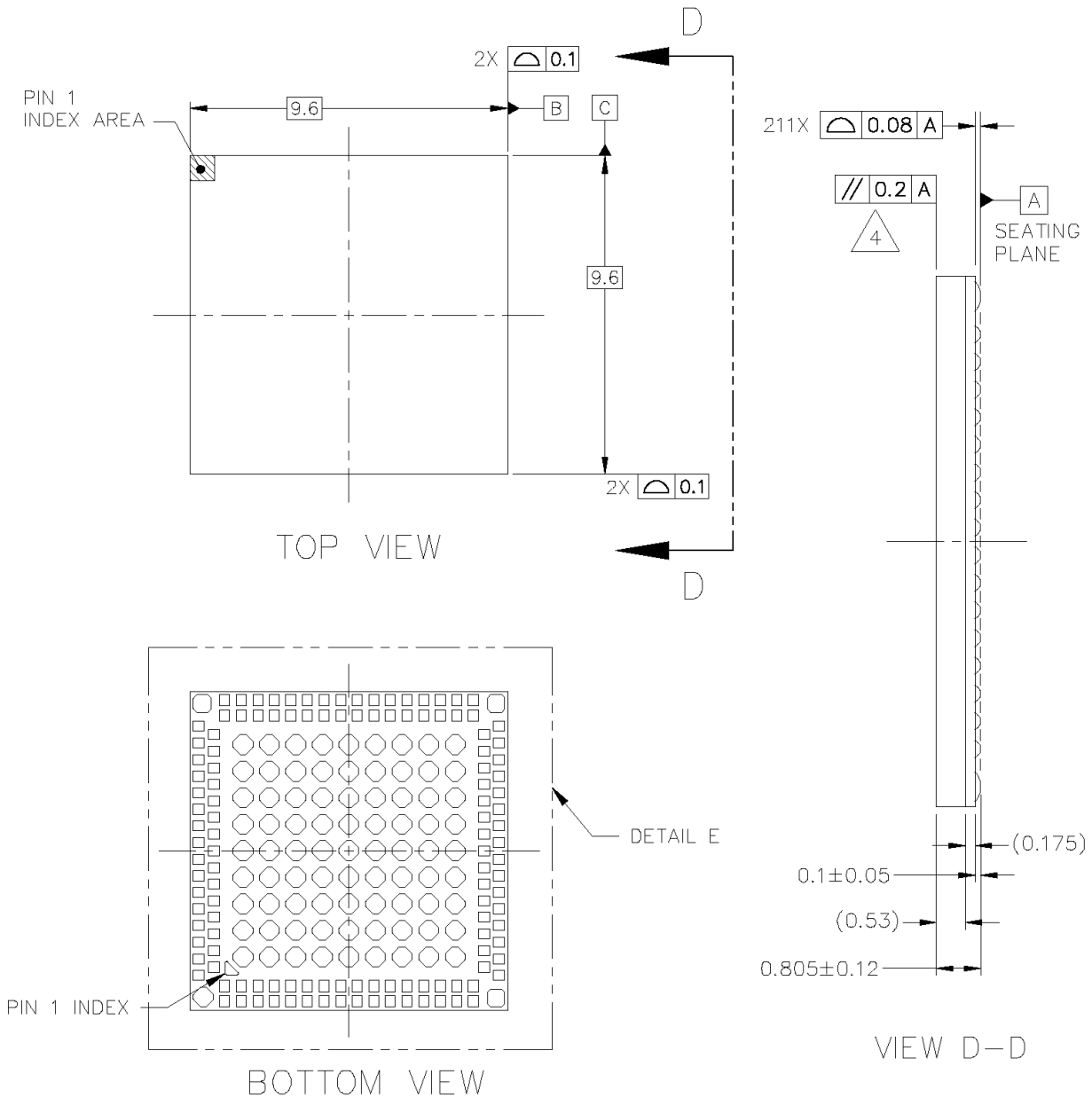
6.1 Package parameters for the LS1012A device

The package type is 9.6 mm x 9.6 mm molded FC-LGA. The package parameters are as follows:

Package	9.6 mm x 9.6 mm molded FC-LGA
Pitch	0.5 mm
Solder Alloy composition	SAC 305 (96.5/3.0/0.5)
Interconnects	211

6.2 Mechanical dimensions of the LS1012A device

The following figure shows the mechanical dimensions and bottom surface nomenclature of the chip.



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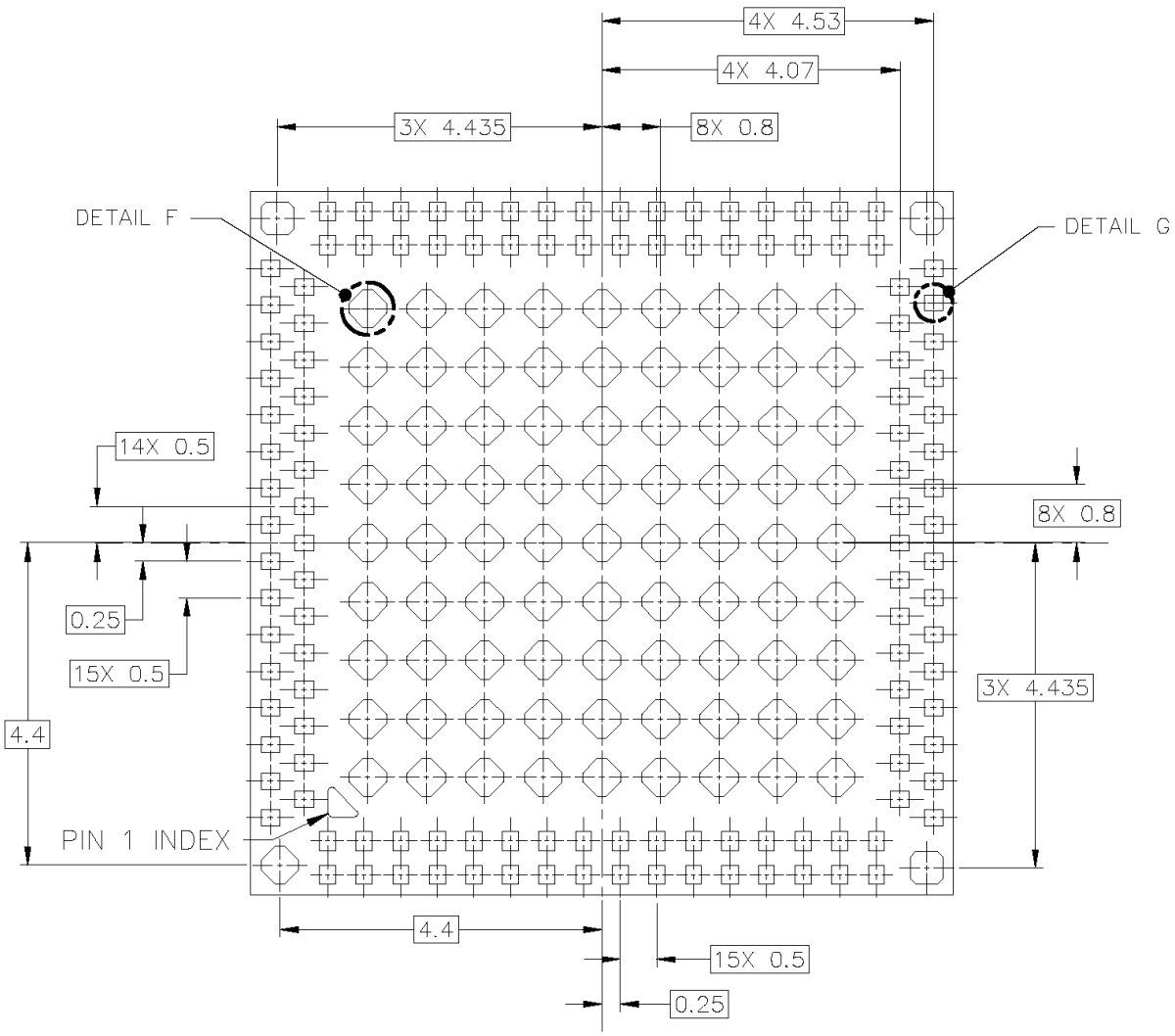
TITLE: FC LGA, 9.6 X 9.6 X 0.805 PKG, 0.5 MM PITCH, 211 I/O	DOCUMENT NO: 98ASA00988D	REV: C
	STANDARD: NON-JEDEC	
	SOT1868-1	06 DEC 2018



BOTTOM VIEW
DETAIL E
SOLDER MASK OPENING

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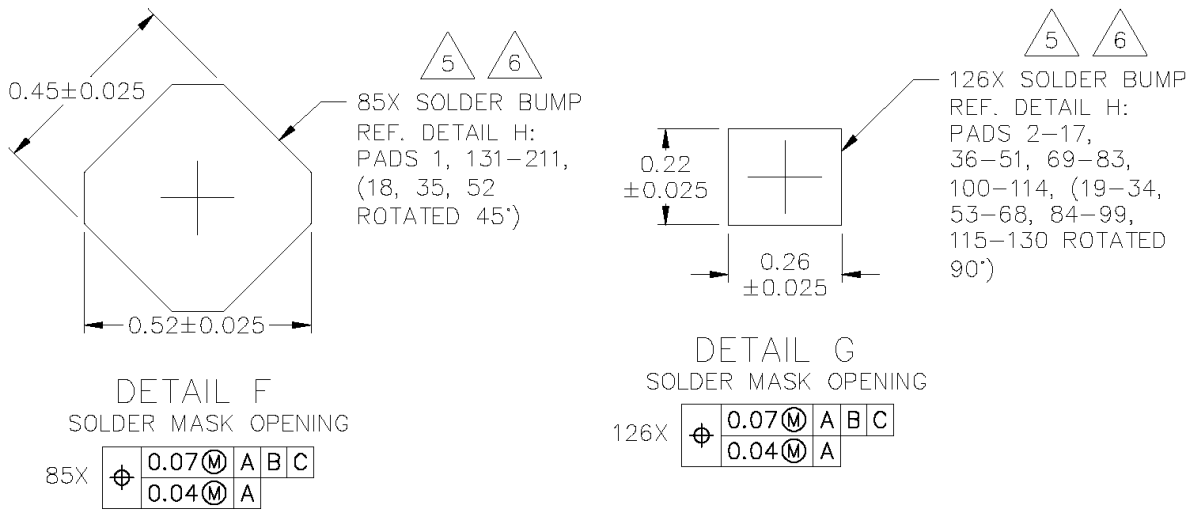
	STANDARD: NON-JEDEC	
	SOT1868-1	06 DEC 2018



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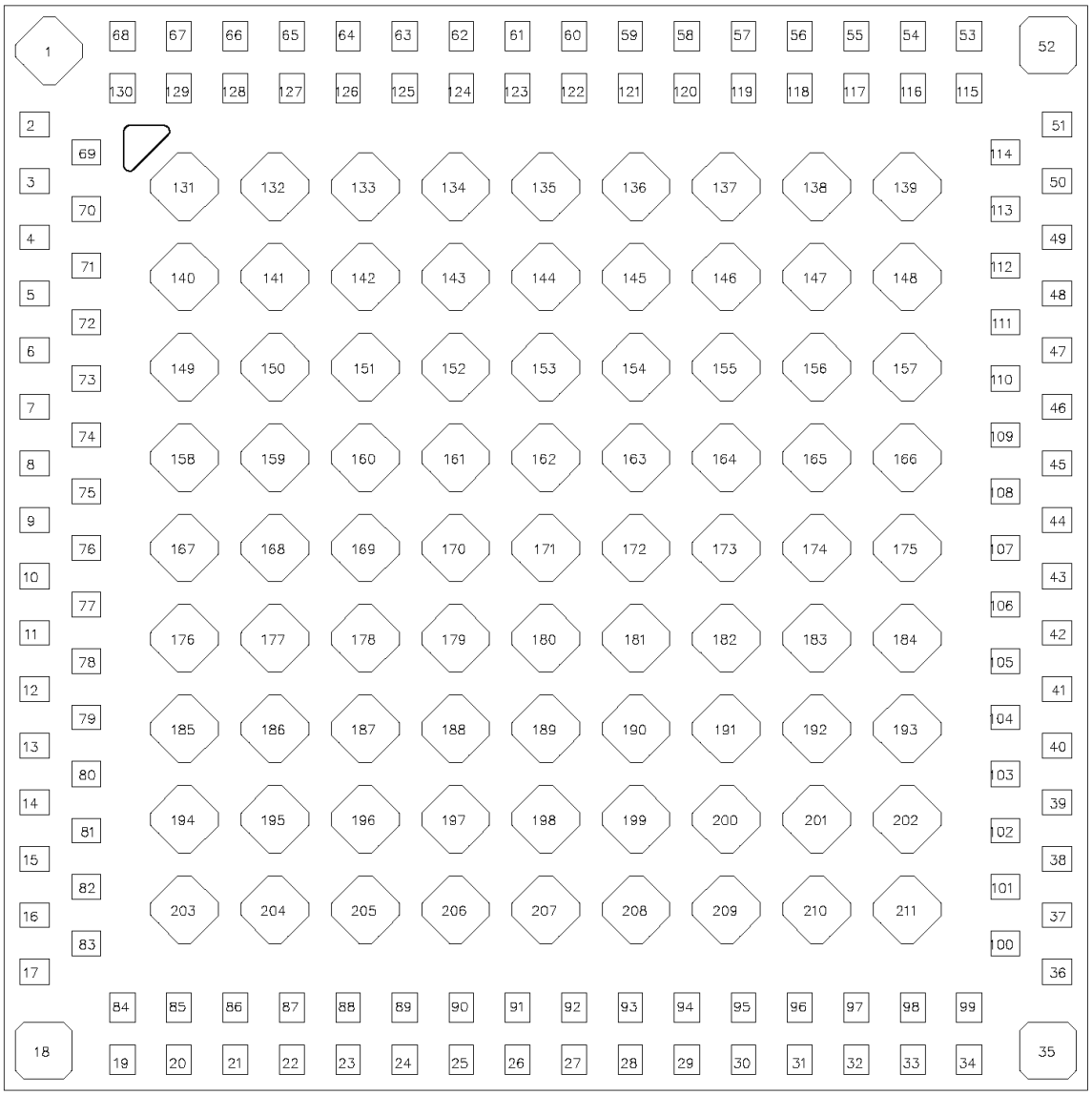
	STANDARD: NON–JEDEC	
	SOT1868–1	06 DEC 2018



DETAIL H
LGA PAD NUMBERS
(VIEWED FROM TOP THROUGH PACKAGE)

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	STANDARD: NON-JEDEC	
	SOT1868-1	06 DEC 2018

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
4. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
5. MAXIMUM SOLDER BUMP SHAPE MEASURED PARALLEL TO DATUM A.
6. EXPOSED COPPER IS NOT ALLOWED ON THE LGA PAD.

Figure 52. Mechanical dimensions of the FC-LGA

7 Security fuse processor

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin per Power up sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of six fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Power up sequencing. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 4.

NOTE

Users not implementing the QorIQ platform's Trust Architecture features should connect TA_PROG_SFP to GND.

8 Ordering information

This table provides the NXP QorIQ platform part numbering nomenclature.

8.1 Part numbering nomenclature

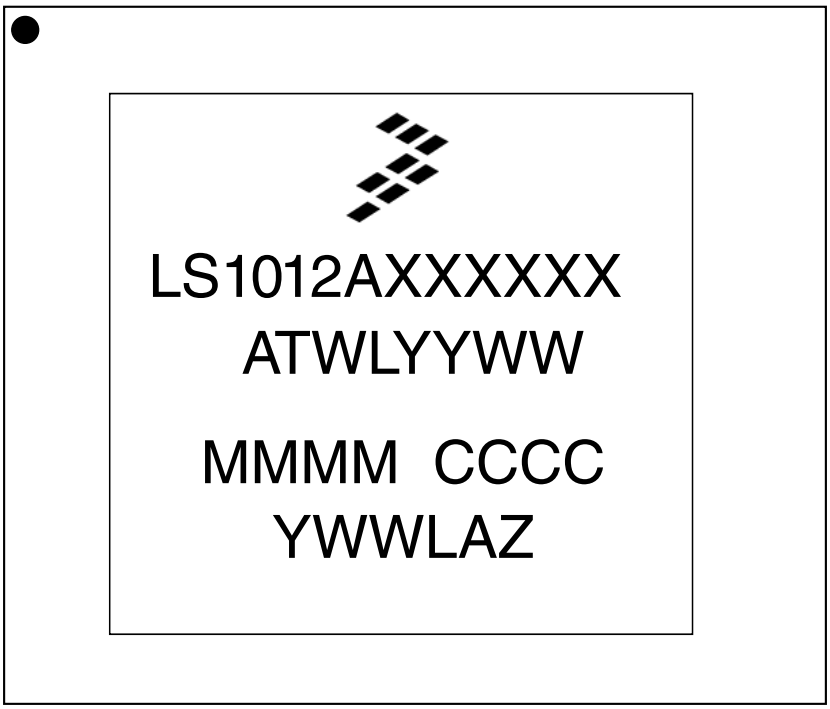
This table provides the NXP QorIQ platform part numbering nomenclature.

Table 93. Part numbering nomenclature

p	ls	n	nn	n	A	X	e	x	c	d	r
Qual status	Generation	Performance Level	Number of Virtual cores	Unique ID	Core Type	Temperature Range	Encryption	Package Type	CPU Speed[1]	DDR Data Rate	Die Revision
P="Sampling" Blank="Qual"	LS	1	01	2	A = Arm	S = Standard temp X = Extended temp	E = Export controlled crypto hardware enabled N = Export controlled crypto hardware disabled	7 = LGA	K = 1000 MHz H = 800 MHz E = 600 MHz	K = 1000 MHz	B = Rev 2.0 A = Rev 1.0
1. CPU speed of 1000 MHz is applicable for the LS1012A Rev 2.0 only.											

8.2 Part marking

Parts are marked as in the example shown in this figure.



Legend:
LS1012AXXXXXX is the orderable part number
ATWLYYWW is the test traceability code
MMMM is the mask number
CCCC is the country code
YWWLAZ is the assembly traceability code

Figure 53. Part marking for FC-LGA chip LS1012A

9 Revision history

The following table provides revision history for this document.

Table 94. Document revision history

Rev. Number	Date	Substantive Change(s)
2	01/2019	• Updated output low voltage in Table 79 • Updated QuadSPI AC timing specifications • Updated output data delay and output data hold in Table 86 • Updated output data delay and output data hold in Figure 49 • Updated t_{CSC} and t_{ASC} timing parameters in Table 84

Table continues on the next page...

Table 94. Document revision history (continued)

Rev. Number	Date	Substantive Change(s)
		• Updated cursor position of t_{RGHT} inFigure 19 • Updated section Temperature diode • Updated Mechanical dimensions of the LS1012A device • Updated CS output delay in Table 86

1	01/2018	• Added note 31 in Pinout list
		• Added section 1000Base-KX interface
		• Updated maximum value from 500 to 200 in Table 17
		• Changed the title of section 3.5 from "Preliminary IO value" to I/O power dissipation
		• Changed the S1VDD, USB_SDVDD, and USB_SVDD voltage tolerance values from +30mV to +50mV in Table 4
		• Updated Table 93 for LS1012A Rev 2.0
		• Updated Table 9 for 1000 MHz
		• Updated notes in Table 3
		• Updated Table 8 for 1000 MHz
		• Changed 10 ms to 95 ms in Power up sequencing
		• Updated Table 4 for LS1012A Rev 2.0
		• Updated Table 81 for maximum input current.
		• Updated Table 91 for 1000 MHz. and removed the Notes column.
		• Updated Pinout list for the following:
		  • The RESET_REQ_B pin is additionally multiplexed with CLK_OUT
		  • Updated notes 2, 11 and 16
		  • Added note 28 to SDHC1_CMD, SDHC1_DAT0, SDHC1_DAT1, SDHC1_DAT2, and SDHC1_DAT3
		  • Added note 29 to SDHC2_CMD, SDHC2_DAT0, SDHC2_DAT1, SDHC2_DAT2, and SDHC2_DAT3
		  • Updated the pin type of D1_MVREF

0	01/2017	Initial public release

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