QorIQ LS1088A Reference Design Board Reference Manual

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Chapter 1
Introduction

The LS1088A Reference Design Board (RDB) is a high-performance-computing hardware and software development platform that supports the LS1088A QorIQ™ Architecture processor series, as well as the footprint-compatible LS1043A. The board is lead-free and RoHS-compliant. Boards can be ordered using the part numbers shown in the table below.

Table 1-1. Ordering Information

Board	Ordering Information	Description
LS1088ARDB	LS1088ARDB-PA	Standard

NOTE

> Throughout this document, descriptions of LS1088ARDB features will also apply to a board using the LS1043A, unless otherwise noted. The term "RDB" applies to all boards equally.

Developers using the LS1088ARDB can perform standard debugging tasks, such as:

- Upload and run code
- Set breakpoints
- Display memory and registers
- Connect and incorporate proprietary hardware into target systems using the LS1088A as a host processor
- Use the RDB as a demonstration tool

The board support package (BSP) is provided with the system and includes support for U-Boot and the Linux operating system.

The figure below shows the LS1088A processor block diagram.

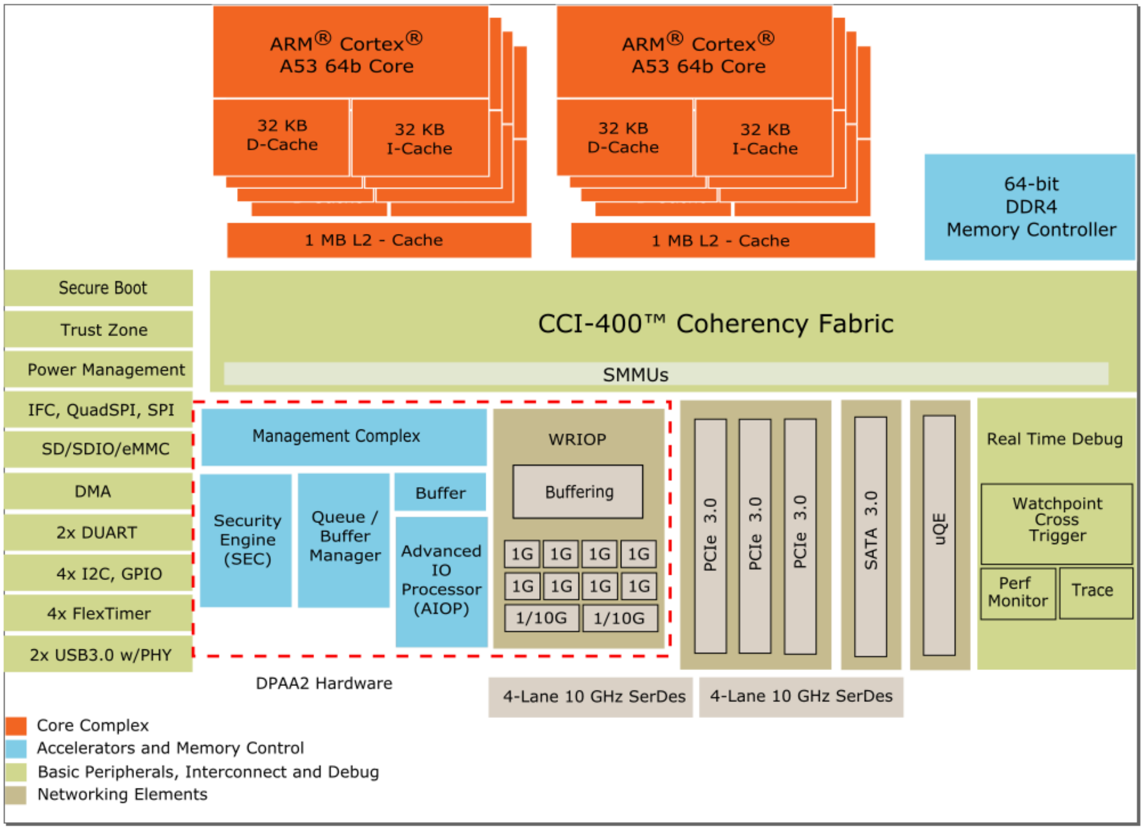

ARM® Cortex® A53 64b Core
32 KB D-Cache
32 KB I-Cache
1 MB L2 - Cache
ARM® Cortex® A53 64b Core
32 KB D-Cache
32 KB I-Cache
1 MB L2 - Cache
64-bit DDR4 Memory Controller
Secure Boot
Trust Zone
Power Management
IFC, QuadSPI, SPI
SD/SDIO/eMMC
DMA
2x DUART
4x I2C, GPIO
4x FlexTimer
2x USB3.0 w/PHY
CCI-400™ Coherency Fabric
SMMUs
Management Complex
Security Engine (SEC)
Queue / Buffer Manager
Buffer
Advanced IO Processor (AIOP)
WRIOP
Buffering
1G
1G
1G
1G
1G
1G
1G
1G
1/10G
1/10G
DPAA2 Hardware
PCIe 3.0
PCIe 3.0
PCIe 3.0
SATA 3.0
uQE
4-Lane 10 GHz SerDes
4-Lane 10 GHz SerDes
Real Time Debug
Watchpoint Cross Trigger
Perf Monitor
Trace
Core Complex
Accelerators and Memory Control
Basic Peripherals, Interconnect and Debug
Networking Elements

Figure 1-1. LS1088A processor block diagram

1.1 Related documents

The table below lists the additional documents that you can refer to, for more information on the LS1088ARDB or LS1043ARDB.

Some of these documents may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1-2. Related documents

Document	Description
LS1088ARDB Quick Start Guide	Describes the LS1088ARDB hardware kit, and lists the settings required to connect switches, connectors, jumpers, push buttons, and LEDs to the peripheral devices.
LS1088A Integrated QorIQ LS Series Processor Family Reference Manual	Provides a detailed description of the LS1088A QorIQ LS Series processor and of some of its features like memory mapping, serial interfaces, power supply, chip features, and clock information.
LS1088A QorIQ LS Series Advanced Multicore Processor Data Sheet	Contains LS1088A information on Pin assignments, Electrical characteristics, Hardware design, considerations, Package information, and Ordering information.

Table continues on the next page...

Table 1-2. Related documents (continued)

Document	Description
LS1088A Chip Errata	Lists the details of all known silicon errata for LS1088A.
LS1043A Integrated QorIQ LS Series Processor Family Reference Manual	Provides a detailed description of the LS1043A QorIQ LS Series processor and of some of its features like memory mapping, serial interfaces, power supply, chip features, and clock information.
LS1043A QorIQ LS Series Advanced Multicore Processor Data Sheet	Contains LS1043A information on Pin assignments, Electrical characteristics, Hardware design, considerations, Package information, and Ordering information.
LS1043A Chip Errata	Lists the details of all known silicon errata for LS1043A.

1.2 Acronyms

The following table lists the acronyms used in the document.

Table 1-3. Acronyms

Term	Meaning
ATX	Advanced Technology Extended (power supply)
BRDCFG	Board Configuration
COP	Common On-Chip Processor
CSR	Control Status Register
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
ECC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable ROM
EMI	ElectroMagnetic Interference
eMMC	Embedded Multi Media Card
eSDHC	Enhanced Secure Digital High Capacity Card
FCM	NAND Flash Control Machine
Fman	Frame Manager
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
GPIO	General Purpose In/Out
HRESET	Hard Reset
I2C	Inter-Integrated Circuit Multi-Master Serial Computer Bus
IPL	Initial Program Load
JTAG	Joint Test Access Group (IEEE® Std. 1149.1™)
LBMAP	Local Bus Map
LED	Light-emitting Diode
LSB	Least Significant Bit

Table continues on the next page...

Table 1-3. Acronyms (continued)

Term	Meaning
MMC	Multi-media Card
MSB	Most Significant Bit
PLL	Phased Lock Loop
ppm	Parts per Million
RCW	Reset Configuration Word
RGMII	Reduced General Media Independent Interface
ROM	Read Only Memory
RTC	Real-time Clock
SATA	Serial Advanced Technology Attachment
SCL/SCLK	Serial Clock
SD	Secure Digital Card
SDHC	Secure Digital High Capacity
SDREFCLK	SerDes Reference Clock
SerDes (SRDS)	Serializer/Deserializer; for example PEX, XAUI, SGMII, SATA, sRIO, AURORA, and XFI
SGMII	Serial Gigabit Media Independent Interface
SMB	Subminiature Version B Connector
SPI	Serial Peripheral Interface Flash
SRAM	Static Random Access Memory
SYSCLK	System Clock
TAP	Test Access Port; for example, USB TAP or ETH TAP
UART	Universal Asynchronous Receiver/Transmitter
uDIMM	Unbuffered Dual In-Line Memory Module Form Factor
USB	Universal Serial Bus

1.3 Features

The following table lists the features of the LS1088ARDB.

Table 1-4. LS1088ARDB features

Feature	Specification	Description
Processor Support	Core Processors	8x 64-bit ARM A53 cores • up to 1.8 GHz • 2MB L2 Cache • Neon SIMD
	HighSpeed Serial Ports (SerDes)	8 (LS1088A) or 4 (LS1043A) lanes, up to 10.3125 GHz SerDes PCIe connectors supporting: • Slot 1: x1 miniPCIe (LS1088A only)

Table continues on the next page...

Table 1-4. LS1088ARDB features (continued)

Feature	Specification	Description
		• Slot 2: x1 miniPCIe • Slot 3: x1 PCIe (LS1088A only) Slot3 supports two PCIe card configurations: Horizontal Configuration: using the right-angle PCIe adapter. Only half-height, half-length PCIe cards are supported in the horizontal card orientation. Vertical Configuration: Either half-height or full-height, half-length PCIe cards supported in vertical card orientation. This orientation requires that the chassis lid be removed. In addition, the two miniPCIe connectors (Slot1 and Slot2) can be combined to support a single PCIe x2 configuration such as Quantenna Wi-Fi card.
		One SATA connector (LS1088A only). Eight RJ45 connectors for Ethernet 100M/1G support (LS1088A only). Four RJ45 connectors for Ethernet 100M/1G support (LS1043A only). One RJ45 for Ethernet 10G support. One SFP+ cage for XFI support (LS1088A only).
	DDR	One DDR4 uDIMM/RDIMM connector featuring: • 72-bits (8-bits ECC) • four chip-selects • speeds up to 2133MT/s The supplied DDR4 memory module is: • 8GB • 72-bit • dual rank • 2100MT/s
	1588	Supported off-board through header.
	USB 3.0	High-speed USB 3.0 ports: • Configurable to Host or OTG modes via jumper. • USB1 is a type-A connector. • USB2 is a micro-AB connector. • All ports support independently-controlled power supplies.
	IFC	Supports QSPI: • 2 devices up to 64MB. • SPI/QSPI memory emulation. • Boot device may be selected among QSPI devices or emulator. Supports NAND: • 2GB memory • 8b • ECC support CPLD connection for BCSRs
	eSDHC	SD slots supporting:

Table continues on the next page...

Table 1-4. LS1088ARDB features (continued)

Feature	Specification	Description
		- external cards - UHS-1 modes: SDR12, SDR25, SDR50, SDR104, DDR50. On-board eMMC supporting: - 8GB memory - HS-200 + DDR modes.
	TDM	Supports TDM riser for E1/T1 telephony connections.
	I2C	I2C1 used for on-board device programming. I2C2/I2C3/I2C4 used as alternate functions.
	DUART (2/channel)	One DB9 D-Type connector (P1) with dual UART port connection. UART3/UART4 supported through DB9 split connectors.
	SATA	One SATA connector (LS1088A only)
	Package	1396-pin, Flip-Chip PBGA of 37x37mm 1.0mm pitch Socket and heatsink included.
System Logic	CPLD	Manages the following: - system reset sequencing - system clock speed selections - processor configuration - QSPI device mapping. Implements QixMin: a subset of the Qixis registers for system control and monitoring. General fault monitoring and logging Runs from ATX-PS hot power rails, allowing operation while system is off.
Clocks	SYSCLK	Fixed at 100 MHz.
	DIFF_SYSCLK	Fixed at 100 MHz.
	DDRCLK	Fixed at 100 MHz.
	SerDes1	Lanes 0 & 1: Fixed at 156.25 MHz for: - XFI Lanes 2 & 3: Fixed at 100 MHz for: - QSGMII
	SerDes2	Lanes 0-3: Fixed at 100.00 MHz for: - PCI Express - SATA (LS1088A only)
	Ethernet	Supports 125 MHz Ethernet clock for 1588
	RTC	Supports 32kHz Real Time Clock input
Power Supplies	VDD GVDD OVDD etc.	Power: - 1.0V for USB Core - 1.8V for PROG_SFP and PROG_MTR (POVDD) - 1.8V and 3.3V standby for CPLD - 1.35 XVDD - 1.0V SVDD - 1.8V for General, UART, IC I/O - 1.8V for USB HVDD

Table 1-4. LS1088ARDB features

Feature	Specification	Description
		• VTT/VREF for DDR4 • 1.8 for eSPI • 3.3V eSDHC • 1.0V for Secure monitor (TA_BB)

1.4 LS1088ARDB Block Diagram

The figure below shows the LS1088ARDB block diagram

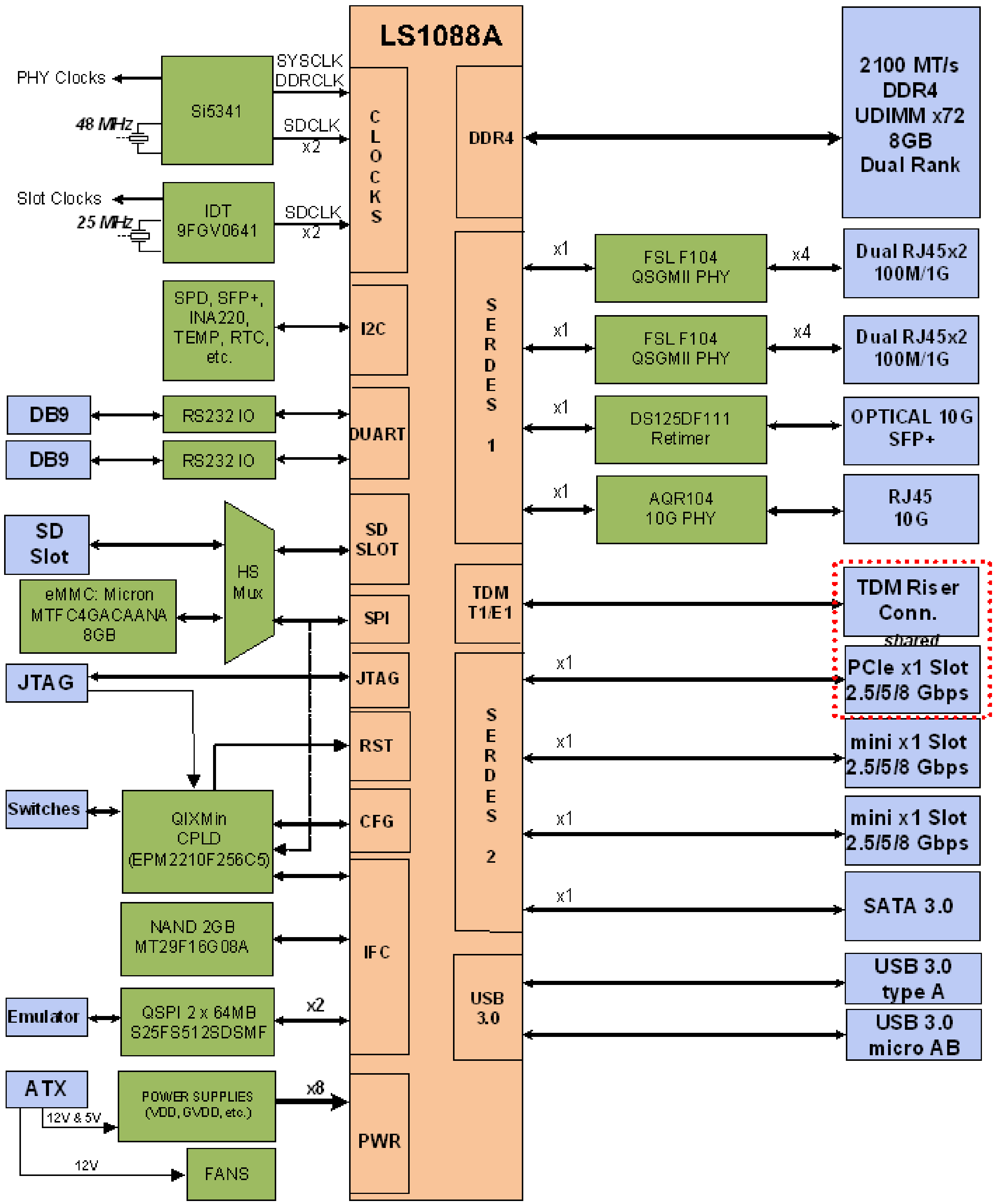

LS1088A
PHY Clocks
Si5341
48 MHz
SYSCLK
DDRCLK
SDCLK
x2
Slot Clocks
IDT
9FGV0641
25 MHz
SDCLK
x2
CLOCKS
DDR4
2100 MT/s
DDR4
UDIMM x72
8GB
Dual Rank
SPD, SFP+, INA220, TEMP, RTC, etc.
I2C
DB9
RS232 IO
DB9
RS232 IO
DUART
SD Slot
HS Mux
eMMC: Micron MTFC4GACAANA 8GB
SD SLOT
SPI
JTAG
JTAG
RST
Switches
QIXMin CPLD (EPM2210F256C5)
CFG
NAND 2GB MT29F16G08A
IFC
Emulator
QSPI 2 x 64MB S25FS512SDSMF
x2
ATX
12V & 5V
POWER SUPPLIES (VDD, GVDD, etc.)
x8
PWR
12V
FANS
SERDES 1
x1
FSL F104 QSGMII PHY
x4
Dual RJ45x2 100M/1G
x1
FSL F104 QSGMII PHY
x4
Dual RJ45x2 100M/1G
x1
DS125DF111 Retimer
OPTICAL 10G SFP+
x1
AQR104 10G PHY
RJ45 10G
TDM T1/E1
TDM Riser Conn.
shared
SERDES 2
x1
PCIe x1 Slot 2.5/5/8 Gbps
x1
mini x1 Slot 2.5/5/8 Gbps
x1
mini x1 Slot 2.5/5/8 Gbps
x1
SATA 3.0
USB 3.0
USB 3.0 type A
USB 3.0 micro AB

Figure 1-2. LS1088ARDB block diagram

1.5 Differences between LS1088ARDB and LS1043ARDB

The LS1088ARDB also supports LS1043A silicon. The following table summarizes the differences when LS1043A silicon is used.

Table 1-5. Board differences

Feature	Connectivity
F104 #1 (100M/1G ports 4..7)	The F104 (PHY2) connected to SerDes 1 Lane 3 ("A") is not usable, and its 4 Ethernet ports (ETH4 to ETH7) are not usable. The F104 (PHY1) on SerDes 1 Lane 2 ("B") is usable, as are its four Ethernet ports (ETH0 to ETH3).
EMI1	The F104 for SerDes 1 Lane 3 (“A”) is present and accessible at addresses 0x0C to 0x0F; software must ignore these addresses during initialization.
MAC Assignment	The LS1043 assigns MACs to Ethernet ports in a different order. Refer to the SerDes section for the complete table.

1.6 LS1088ARDB Board Drawing

The figure below shows the floor plan and escape routing of the LS1088ARDB.

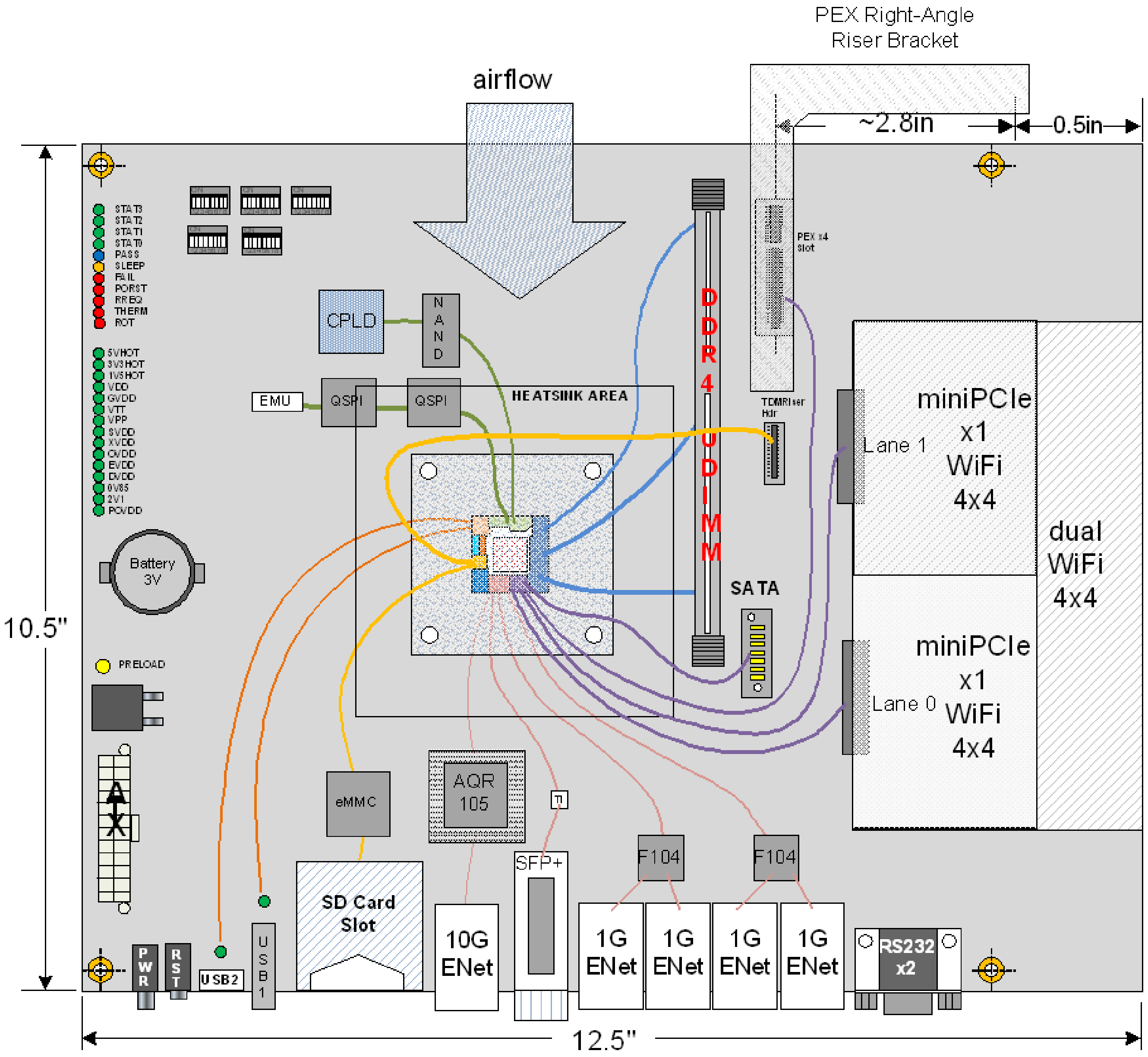

PEX Right-Angle
Riser Bracket
airflow
~2.8in
0.5in
STAT3
STAT2
STAT1
STAT0
PASS
SLEEP
FAIL
PORST
RREQ
THERM
ROT
5VHOT
3V3HOT
1V5HOT
VDD
GVDD
VTT
VPP
SVDD
XVDD
OVDD
EVDD
DVDD
0V85
2V1
POVDD
CPLD
NAND
EMU
QSPI
QSPI
HEATSINK AREA
DDR4 UDIMM
PEX x4
Slot
TDMRiser
Hdr
SATA
miniPCIe
x1
WiFi
4x4
Lane 1
dual
WiFi
4x4
miniPCIe
x1
WiFi
4x4
Lane 0
Battery
3V
10.5"
PRELOAD
ATX
eMMC
AQR
105
SD Card
Slot
SFP+
F104
F104
10G
ENet
1G
ENet
1G
ENet
1G
ENet
1G
ENet
RS232
x2
PWR
RST
USB2
USB1
12.5"

Figure 1-3. LS1088ARDB board drawing

Chapter 2
Functional Description

The LS1088ARDB architecture is primarily determined by the LS1088A QorIQ LS Series Architecture processor, with the need to evaluate the LS1088A processor features and to test its ability to deliver an easily usable off-the-shelf software development platform.

The remaining sections of this chapter cover important features of the system in more detail.

Table 2-1. Architecture sections

Section	Link
Power Supplies	Power Supplies
Clocks	Clocks
DDR Memory	DDR Memory
SerDes	SerDes (Serializer/Deserializer)
EMI Interfaces	EMI - Ethernet Management Interface
Flash Interface	Integrated Flash Controller (IFC)
SDHC Interface	Secure Digital Host Controller (SDHC)
SPI Interface	Serial Peripheral Interface (SPI)
USB Interfaces	USB Interfaces
I2C Ports	I2C Ports
Interrupts	Interrupts
System Controller	System Controller
TDM Interface	TDM Interface
Thermal Management	Thermal Management
JTAG Port	JTAG Port
Serial Ports	Serial Ports (DUART)
Ethernet Controllers	Ethernet (ETH) Controller Interface
IEEE-1588 PTP	IEEE 1588™ PTP Support
GPIO	GPIO Access

2.1 Power Supplies

The LS1088ARDB provides all the voltages necessary for the correct operation of LS1088A device, the DDR4 uDIMM, F104 PHYs, and numerous other peripherals. All power is derived from an external power supply which supplies bulk +5V, +12V, as well as +5V standby power.

The ATX-compatible supply is managed by the system controller CPLD and drives the power supplies shown in th figures below.

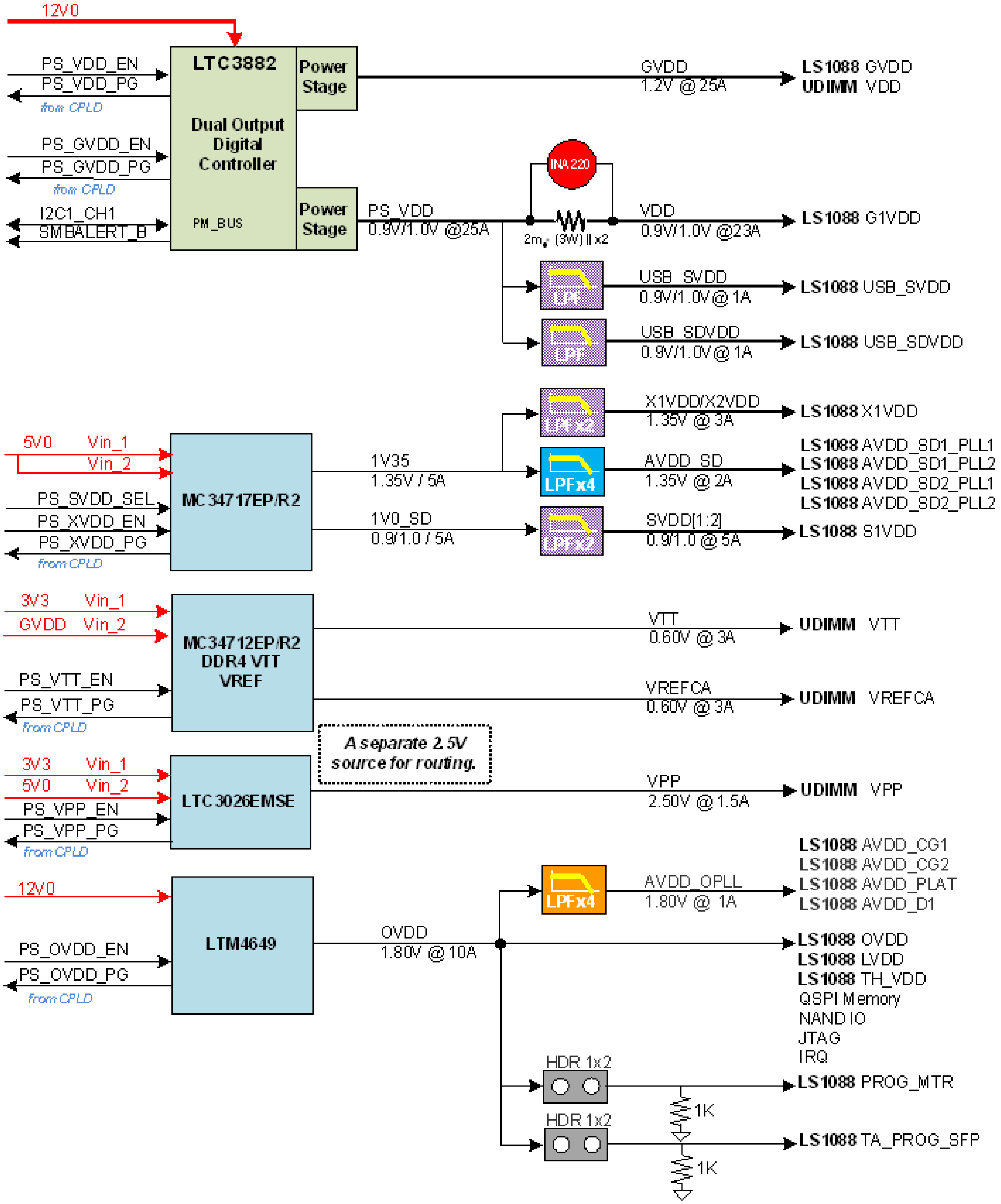

12V0
PS_VDD_EN
PS_VDD_PG
from CPLD
PS_GVDD_EN
PS_GVDD_PG
from CPLD
I2C1_CH1
SMBALERT_B
LTC3882
Dual Output
Digital
Controller
PM_BUS
Power
Stage
Power
Stage
GVDD
1.2V @ 25A
LS1088 GVDD
UDIMM VDD
INA220
PS_VDD
0.9V/1.0V @25A
2m (3W) || x2
VDD
0.9V/1.0V @23A
LS1088 G1VDD
LPF
USB_SVDD
0.9V/1.0V @ 1A
LS1088 USB_SVDD
LPF
USB_SDVDD
0.9V/1.0V @ 1A
LS1088 USB_SDVDD
5V0
Vin_1
Vin_2
PS_SVDD_SEL
PS_XVDD_EN
PS_XVDD_PG
from CPLD
MC34717EP/R2
1V35
1.35V / 5A
1V0_SD
0.9/1.0 / 5A
LPFx2
X1VDD/X2VDD
1.35V @ 3A
LS1088 X1VDD
LPFx4
AVDD_SD
1.35V @ 2A
LS1088 AVDD_SD1_PLL1
LS1088 AVDD_SD1_PLL2
LS1088 AVDD_SD2_PLL1
LS1088 AVDD_SD2_PLL2
LPFx2
SVDD[1:2]
0.9/1.0 @ 5A
LS1088 S1VDD
3V3
Vin_1
GVDD
Vin_2
PS_VTT_EN
PS_VTT_PG
from CPLD
MC34712EP/R2
DDR4 VTT
VREF
VTT
0.60V @ 3A
UDIMM VTT
VREFCA
0.60V @ 3A
UDIMM VREFCA
A separate 2.5V
source for routing.
3V3
Vin_1
5V0
Vin_2
PS_VPP_EN
PS_VPP_PG
from CPLD
LTC3026EMSE
VPP
2.50V @ 1.5A
UDIMM VPP
12V0
PS_OVDD_EN
PS_OVDD_PG
from CPLD
LTM4649
OVDD
1.80V @ 10A
LPFx4
AVDD_OPLL
1.80V @ 1A
LS1088 AVDD_CG1
LS1088 AVDD_CG2
LS1088 AVDD_PLAT
LS1088 AVDD_D1
LS1088 OVDD
LS1088 LVDD
LS1088 TH_VDD
QSPI Memory
NAND IO
JTAG
IRQ
HDR 1x2
LS1088 PROG_MTR
1K
HDR 1x2
LS1088 TA_PROG_SFP
1K

Figure 2-1. LS1088ARDB power supplies

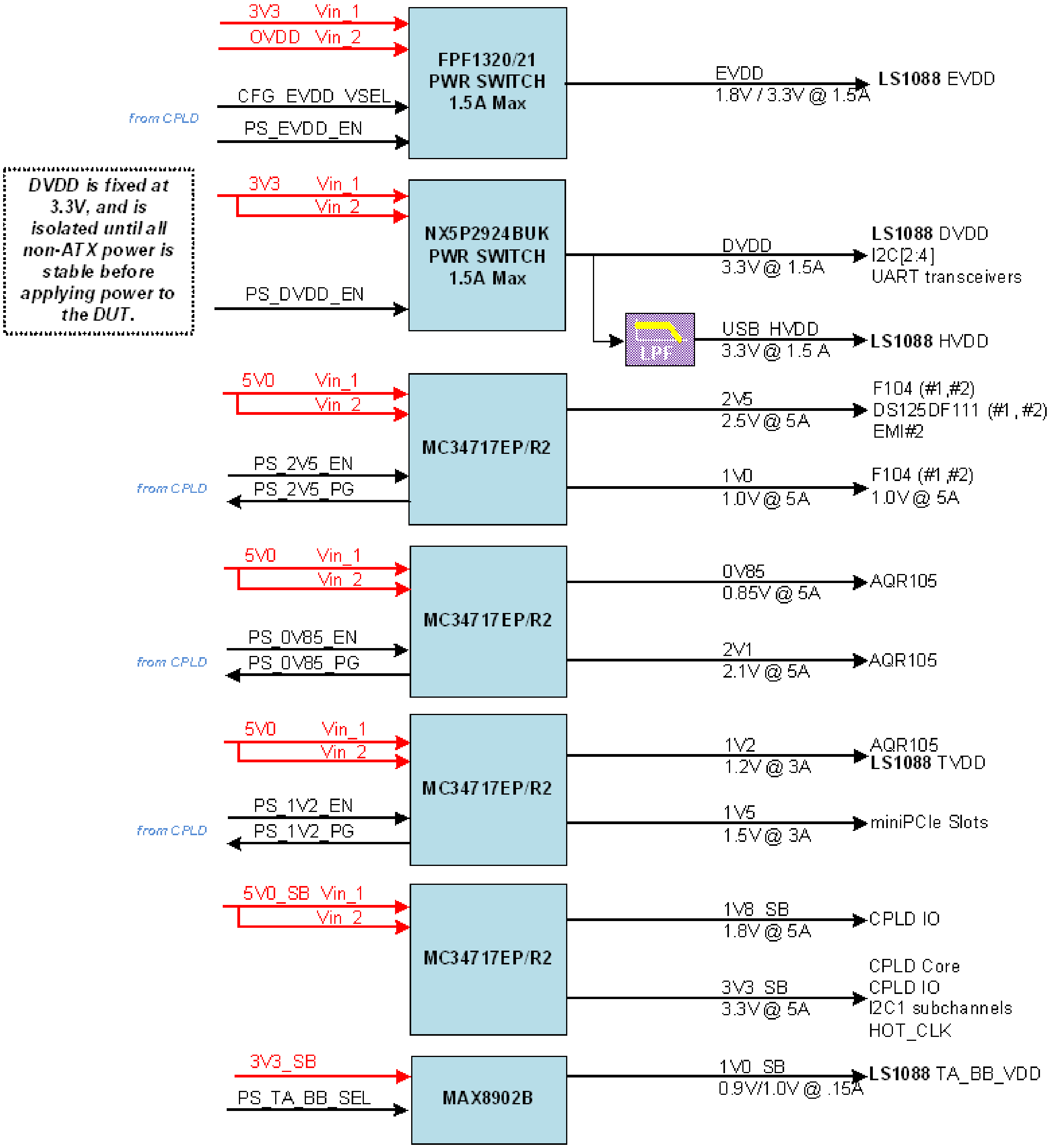

3V3 Vin_1
OVDD Vin_2
CFG_EVDD_VSEL
from CPLD
PS_EVDD_EN
FPF1320/21
PWR SWITCH
1.5A Max
EVDD
1.8V / 3.3V @ 1.5A
LS1088 EVDD
DVDD is fixed at 3.3V, and is isolated until all non-ATX power is stable before applying power to the DUT.
3V3 Vin_1
Vin_2
PS_DVDD_EN
NX5P2924BUK
PWR SWITCH
1.5A Max
DVDD
3.3V @ 1.5A
LS1088 DVDD
I2C[2:4]
UART transceivers
LPF
USB_HVDD
3.3V @ 1.5 A
LS1088 HVDD
5V0 Vin_1
Vin_2
PS_2V5_EN
from CPLD
PS_2V5_PG
MC34717EP/R2
2V5
2.5V @ 5A
F104 (#1,#2)
DS125DF111 (#1, #2)
EMI#2
1V0
1.0V @ 5A
F104 (#1,#2)
1.0V @ 5A
5V0 Vin_1
Vin_2
PS_0V85_EN
from CPLD
PS_0V85_PG
MC34717EP/R2
0V85
0.85V @ 5A
AQR105
2V1
2.1V @ 5A
AQR105
5V0 Vin_1
Vin_2
PS_1V2_EN
from CPLD
PS_1V2_PG
MC34717EP/R2
1V2
1.2V @ 3A
AQR105
LS1088 TVDD
1V5
1.5V @ 3A
miniPCIe Slots
5V0_SB Vin_1
Vin_2
MC34717EP/R2
1V8_SB
1.8V @ 5A
CPLD IO
3V3_SB
3.3V @ 5A
CPLD Core
CPLD IO
I2C1 subchannels
HOT_CLK
3V3_SB
PS_TA_BB_SEL
MAX8902B
1V0_SB
0.9V/1.0V @ .15A
LS1088 TA_BB_VDD

Figure 2-2. LS1088ARDB power supplies (continued)

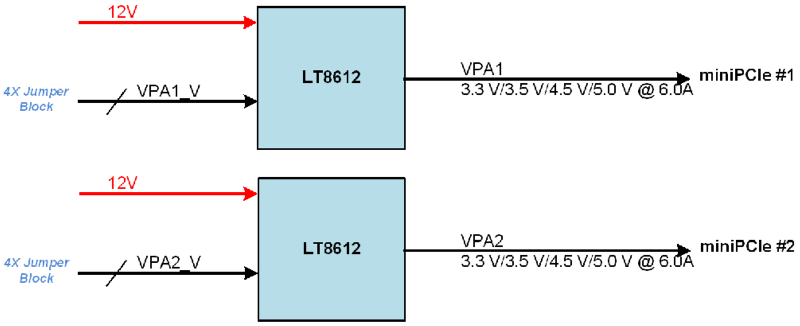

12V
LT8612
4X Jumper Block
VPA1_V
VPA1
3.3 V/3.5 V/4.5 V/5.0 V @ 6.0A
miniPCIe #1
12V
LT8612
4X Jumper Block
VPA2_V
VPA2
3.3 V/3.5 V/4.5 V/5.0 V @ 6.0A
miniPCIe #2

Figure 2-3. LS1088ARDB power supplies (continued)

Note that several power supplies have on-board low-pass filters, to prevent board switching noise from coupling into sensitive analog supplies. The following figure shows the filters used.

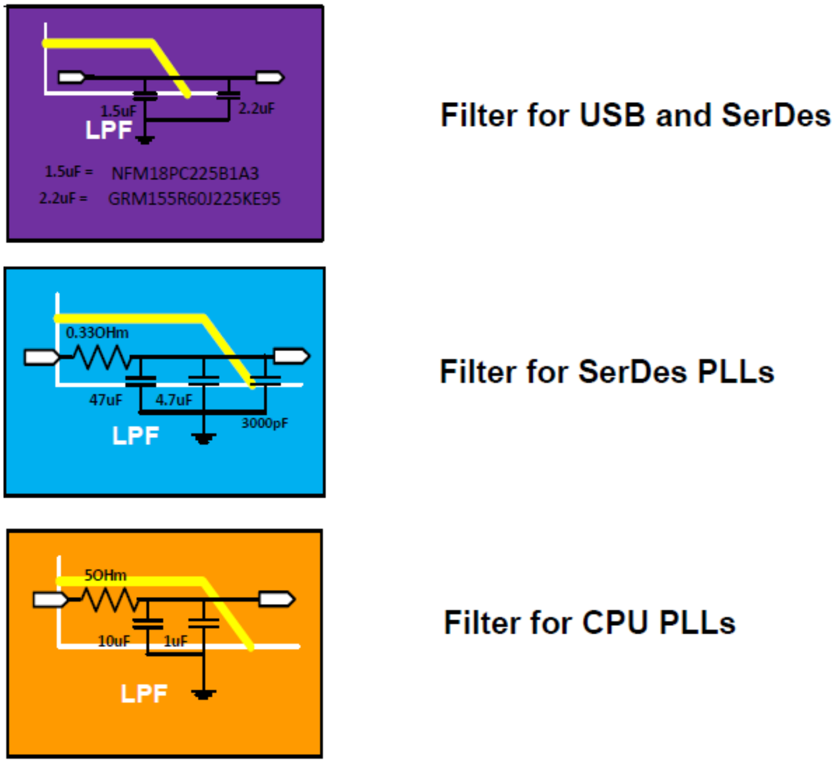

1.5uF
2.2uF
LPF
1.5uF = NFM18PC225B1A3
2.2uF = GRM155R60J225KE95
Filter for USB and SerDes
0.33OHm
47uF
4.7uF
3000pF
LPF
Filter for SerDes PLLs
5OHm
10uF
1uF
LPF
Filter for CPU PLLs

Figure 2-4. LS1088ARDB power filtering

2.1.1 Primary Power Supply

The primary power for the LS1088ARDB is an external ATX12V/EPS12V power supply (PC ATX-PS < 300W).

Table 2-2. Primary power supply

Power Supply	Description	
External ATX12V PS	Vin	90 - 264VAC
	Fin Frequency	50 - 60 Hz
	Iin	< 8.5A @100VAC, 4A @240VAC
	Power Good	Power-on delay time of 100 ~ 500ms
	Temperature Range	Operating: 0° ~ 50°C on full load
	Relative Humidity	20~ 80%

Table 2-3. ATX12V/EPS12 power supply characteristics

Group	Outputs					Units
VOLTAGE	+3.3	+5	+12	-12	+5 (SB)	V
MAX. LOAD	17	18	24	0.3	2.5	A
MIN. LOAD	0.5	1	2	0	0.1	A
REGULATION	±5	±5	±5	±10	±5	%
RIPPLE and NOISE	60	60	120	120	50	mV
CAPACITIVE LOAD	10000	10000	10000	330	10000	uF

2.1.2 Secondary Power Supplies

The table below lists the secondary power supply devices. These supplies are derived from the ATX PSU and are used to power various on-board devices. A few are on all the time, while most others are enabled and disabled in a particular order as controlled by the CPLD.

Table 2-4. Secondary Power Supplies

Supply	Specifications	Vendor/ Device	Vendor	Description
VDD	0.90/1.00/1.025V 25A +/-0.5% accuracy	LTC3882 (controller #1)	Linear Tech	Supplies power to the LS1088A cores. DC-DC converter that produces: NOTE: Filtered VDD power is also supplied to the USB code (USB_SVDD and USB_SDVDD).
G1VDD	1.20 V 25A	LTC3882 (controller #2)		Supplies power to the LS1088A DDR controller and to the DDR memories. NOTE: Only DDR4 is supported, so GVDD is fixed at 1.20V.
X1VDD	1.35 V 5 A	MC34717EP/R2 (controller #1)	Freescale	Supplies power to the LS1088A SerDes IO drivers. NOTE: Filtered XVDD also powers: AVDD_SD1_PLL1

Table continues on the next page...

Table 2-4. Secondary Power Supplies (continued)

Supply	Specifications	Vendor/ Device	Vendor	Description
				AVDD_SD1_PLL2 AVDD_SD2_PLL1 AVDD_SD2_PLL2
S1VDD	0.90/1.00 5 A	(controller #2		Supplies power to the LS1088A SerDes core logic. NOTE: S1VDD level must be 0.9V if VDD is 0.9V.
VTT	0.6V 3A	MC34717EP/R2 (controller #1)	Freescale	Supplies power to the uDIMM DDR4 memory termination power.
VREFCA	0.6V 10mA	(controller #2		Supplies power to the uDIMM DDR4 memory IO switching level.
VPP	2.5 V 1.5 A	LTC3026EMSE	Linear Tech	Regulator that produces DDR4 reference voltage.
OVDD	1.80 V 10 A	LTM4649	Linear Tech	Supplies power to the LS1088A OVDD (IFC, etc.) IO drivers. NOTE: OVDD also powers: LVDD TH_VDD NOTE: Filtered OVDD also powers: AVDD_CGA1 AVDD_CGA2 AVDD_PLAT AVDD_D1 NOTE: Jumper-enabled OVDD also powers: PROG_MTR TA_PROG_SFP These fuse-programming jumpers are normally removed.
EVDD	1.80 V or 3.3 V 1.5 A	FPF1320	NXP	SDHC IO Power. NOTE: EVDD can change between 1.8V and 3.3V on command of the SDHC IP block for certain board configurations. NOTE: The FPF1320 is a power switch, not a power supply. OVDD is the source of 1.8V power.
DVDD	3.3 V 1.5 A	NX5P2924BUK	NXP	Switched power for general 3.3V. DVDD also supplies power to the little-used LVDD rail and filtered power for the USB_HVDD rail.

Table continues on the next page...

Table 2-4. Secondary Power Supplies (continued)

Supply	Specifications	Vendor/ Device	Vendor	Description
				Note: The “NX5P” is an power switch, not a supply, and is used to isolate the LS1088 and peripherals from power until all previous rails are stable. ATX +3.3V is the power source.
2V5	2.50 V 5.0 A	MC34717EP/R2 (controller #1)	Freescale	Power supply fo r F104
1V0	1.00 V 5.0 A	(controller #2		Powe r supply fo r F104
0V85	0.85 V 5.0 A	MC34717EP/R2 (controller #1)	Freescale	Powerr supply for Aquantia AQR105
2V1	2.10 V 5.0 A	(controller #2		Power supply for Aquantia AQR105
1V2	1.20 V 3.0 A	MC 347 1 7EP/R2 (controlle r #1)	Freescale	Power supply for Aquantia AQR105
1V5	1.50 V 3.0 A	(controller #2)		Power supply for miniPCIe cards
VPA1	3.3 / 3.5 / 4.5 / 5.0 6.0A	L T8 612	Line ar T ech	Power supply for WiFi card #1 power amplifier
VPA2	3.3 / 3.5 /4.5 / 5.0 6.0A	L T8 612	Line ar T ech	Power supply for WiFi card #2 power amplifier
3V3_SB	3.3 V 5.0 A	MC34717EP/R2 (controller #1)	Freescale	Standby (“hot”) power for the system controller CPLD core and IO
1V8_SB	1.8 V 5.0 A	(controller #2)		Standby (“hot”) power for the system controller CPLD IO
1V0_SB	0.9 / 1.0 V 150 mA	NCP571SN10T1G	NXP	Power supply for TA_BB_VDD (tamper detection block) NOTE: Must follow SVDD setting.

2.1.3 Power Sequencing

When AC power is available to the ATX power supply, “standby” power is generated to the system controller. Thereafter it is able to control and configure the system as needed.

The power switch, accessible from the front panel, will cause the system controller to enable the ATX supply for the 3.3V, 5V and 12V power supplies. Additionally, a configuration switch (“AUTO_ON”) causes the system controller to keep the LS1088ARDB powered up as long as AC power is available.

After the ATX power supply is stable, the system controller enables the remaining power supplies in the sequence described the table below.

Table 2-5. Power supply sequencing

Time	Event	Details
Initial	AC power applied	90 - 264VAC
Initial + 100ms	+5V STANDBY stable	
Wait for power switch OR detected SW_AUTO = 1.		
t + 0 ms	Assert PS_ON_B	ATX power (+5V, +3.3V, +12V) ramps up.
t + 100 ms	Detect ATX_PWRGD	ATX power stable.
t + 110 ms	Enable Tier #1	Drive “Power Enable” to: DVDD OVDD 1V5 2V5 0V85 1V2 2V1 VPA1 VPA2
t + 210 ms	Tier #1 Stable	All tier 1 supplies report “Power Good”. If not, stall.
t + 220 ms	Enable Tier #2	Drive “Power Enable” to: VDD XVDD
t + 320 ms	Tier #2 Stable	All tier 2 supplies report “Power Good”. If not, stall.
t + 330 ms	Enable Tier #3	Drive “Power Enable” to: VPP
t + 430 ms	Tier #3 Stable	All tier 3 supplies report “Power Good”. If not, stall.
t + 440 ms	Enable Tier #4	Drive “Power Enable” to: GVDD VTT
t + 540 ms	Tier #4 Stable	All tier 4 supplies report “Power Good”. If not, stall.
t +550 ms	Exit power sequence	

2.1.4 Auxiliary Power Supplies

In addition to the above power supplies, there are additional supplies provided that are neither managed nor sequenced.

2.1.4.1 VBAT

3V is supplied to the real-time clock and to the tamper-detect circuitry using a CR2032 lithium coin cell.

2.1.4.2 POVDD

POVDD supplies power to the device for fuse programming (to disable internal functions). This power is enabled through a jumper.

NOTE

> Ensure that POVDD is disabled unless it is specifically required to be enabled.

2.2 Clocks

The LS1088ARDB provides all the required clocks for the processor as well as other devices. The following figure shows the overall clock architecture.

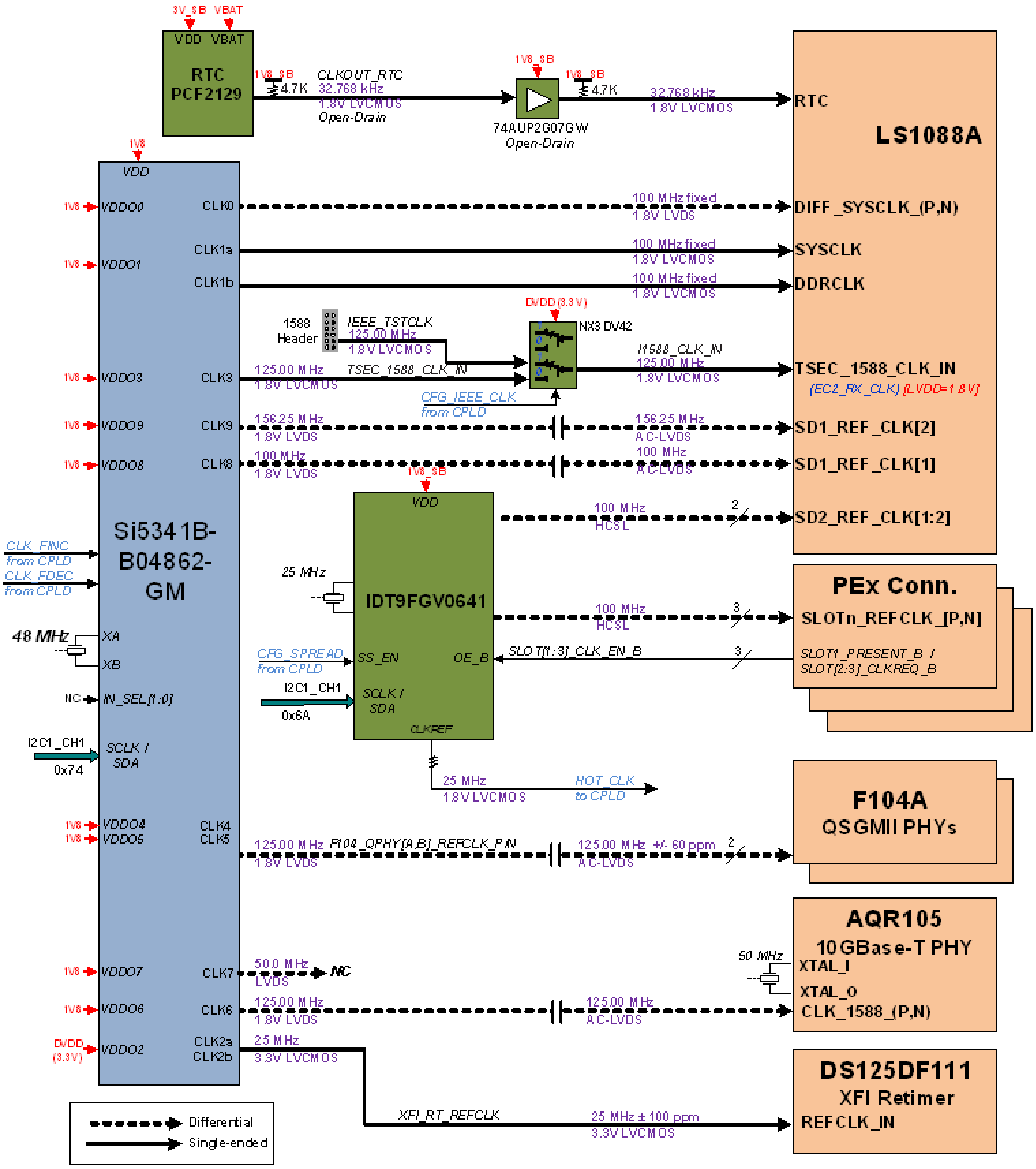

3V_SB
VBAT
VDD VBAT
RTC
PCF2129
1V8_SB
4.7K
CLKOUT_RTC
32.768 kHz
1.8V LVCMOS
Open-Drain
1V8_SB
74AUP2G07GW
Open-Drain
1V8_SB
4.7K
32.768 kHz
1.8V LVCMOS
RTC
LS1088A
1V8
VDD
1V8 VDDO0
CLK0
100 MHz fixed
1.8V LVDS
DIFF_SYSCLK_(P,N)
CLK1a
100 MHz fixed
1.8V LVCMOS
SYSCLK
1V8 VDDO1
CLK1b
100 MHz fixed
1.8V LVCMOS
DDRCLK
DVDD (3.3 V)
1588 Header
IEEE_TSTCLK
125.00 MHz
1.8V LVCMOS
NX3DV42
1V8 VDDO3
CLK3
125.00 MHz
1.8V LVCMOS
TSEC_1588_CLK_IN
I1588_CLK_IN
125.00 MHz
1.8V LVCMOS
TSEC_1588_CLK_IN
(EC2_RX_CLK) [LVDD=1.8V]
CFG_IEEE_CLK
from CPLD
1V8 VDDO9
CLK9
156.25 MHz
1.8V LVDS
156.25 MHz
AC-LVDS
SD1_REF_CLK[2]
1V8 VDDO8
CLK8
100 MHz
1.8V LVDS
100 MHz
AC-LVDS
SD1_REF_CLK[1]
1V8_SB
VDD
100 MHz
HCSL
2
SD2_REF_CLK[1:2]
CLK_FINC
from CPLD
CLK_FDEC
from CPLD
Si5341B-
B04862-
GM
25 MHz
IDT9FGV0641
100 MHz
HCSL
3
PEx Conn.
SLOTn_REFCLK_[P,N]
48 MHz
XA
XB
CFG_SPREAD
from CPLD
SS_EN
OE_B
SLOT[1:3]_CLK_EN_B
3
SLOT1_PRESENT_B /
SLOT[2:3]_CLKREQ_B
I2C1_CH1
0x6A
SCLK /
SDA
NC
IN_SEL[1:0]
CLKREF
I2C1_CH1
0x74
SCLK /
SDA
25 MHz
1.8V LVCMOS
HOT_CLK
to CPLD
F104A
QSGMII PHYs
1V8 VDDO4
1V8 VDDO5
CLK4
CLK5
125.00 MHz
1.8V LVDS
F104_QPHY[A,B]_REFCLK_P,N
125.00 MHz +/- 60 ppm
AC-LVDS
2
AQR105
10GBase-T PHY
50 MHz
XTAL_I
XTAL_O
CLK_1588_(P,N)
1V8 VDDO7
CLK7
50.0 MHz
LVDS
NC
1V8 VDDO6
CLK6
125.00 MHz
1.8V LVDS
125.00 MHz
AC-LVDS
DVDD (3.3V)
VDDO2
CLK2a
CLK2b
25 MHz
3.3V LVCMOS
DS125DF111
XFI Retimer
REFCLK_IN
XFI_RT_REFCLK
25 MHz ± 100 ppm
3.3V LVCMOS
Differential
Single-ended

Figure 2-5. Clock architecture

All the clocks are fixed frequency, and most are produced by the SiliconLabs Si5341B (or a buffered copy of its outputs) or the IDT IDT9FGV0641. The following table summarizes the specifications of each clock and the component that provides it.

Table 2-6. Clock devices and specifications

Clock	Destination	Frequency	Specifications	Device
DIFF_SYSCLK_[P,N]	CPU	100.0 MHz	DIFF 1.8V LVDS ±150 ps jitter, pk.	Si5341B Clk0 output.
SYSCLK	CPU	100.0 MHz	SE 1.8V-LVCMOS ±150 ps jitter, pk.	Si5341B Clk1A output.
DDRCLK	CPU	100.0 MHz	SE 1.8V-LVCMOS ±150 ps jitter, pk.	Si5341B Clk1B output.
SD1_REF_CLK1_[P,N]	CPU	100.0 MHz	DIFF AC-LVDS 42 ps jitter, pk.	Si5341B Clk8 output.
SD1_REF_CLK2_[P,N]	CPU	156.25 MHz	DIFF AC-LVDS 42 ps jitter, pk.	Si5341B Clk9 output.
SD2_REF_CLK1_[P,N] SD2_REF_CLK2_[P,N] SLOT1_REFCLK_[P,N] SLOT2_REFCLK_[P,N] SLOT3_REFCLK_[P,N]	CPU	100.0 MHz	DIFF DC-HCSL 86 ps jitter, pk.	IDT9FGV0641 buffer outputs Slot clock outputs are gated with presence detect.
F104A_REFCLK_[P,N] F104B_REFCLK_[P,N]	F104A F104B	125.0 MHz	DIFF AC-LVDS ±60 ppm <100 ps jitter rms	Si5341B Clk4 and Clk5 outputs.
AQR105_CLK_[P,N]	AQR105	50.0 MHz	Crystal	
AQR105_CLK1588_[P,N]	AQR105	125.0 MHz	DIFF AC-LVDS ±60 ppm	Si5341B Clk6 output.
XFI_RT_REFCLK[1:2]	DS125DS111	25.0 MHz	SE 1.8V-LVCMOS ±100 ppm	Si5341B Clk2a output.
TSEC_1588_CLK_IN	CPU	125.0 MHz	SE 1.8V-LVCMOS <250 ps jitter	Si5341B Clk3 output. May be replaced with external clock via IEEE header.
HOT_CLK	CPLD	25.0 MHz	SE 1.8V-LVCMOS	IDT9FGV0641 reference output. (Hot-powered and hot-enabled)
RTC	CPU	32.768 kHz	SE 1.8V-LVCMOS	1.8V_SB-powered copy of RTC output.

2.3 DDR Memory

The LS1088ARDB supports the single memory controller of the device. The following features are supported:

- One 288-pin JEDEC DDR4 DIMM connector supporting single and dual rank industry-standard, uDIMM or RDIMM modules
- 64-bit data

- 8-bit ECC
- Speeds up to 2133 MT/s
- Four chip-selects per slot.
- Support for x4, x8 and x16 DDR4 memory devices
- Memory interface includes all necessary termination and IO power
- Memory signals are routed in order to achieve maximum performance on the bus.

The default uDIMM supplied with the system is a dual rank, 8GByte, 64-bit with ECC operating at the full 2133MT/s data rate.

NOTE

The LS1088ARDB board supports all types, ranks, and speeds of uDIMM’s. Freescale cannot validate all combinations available in the market; therefore, the system is shipped with a representative uDIMM.

The following figure shows the DDR memory architecture

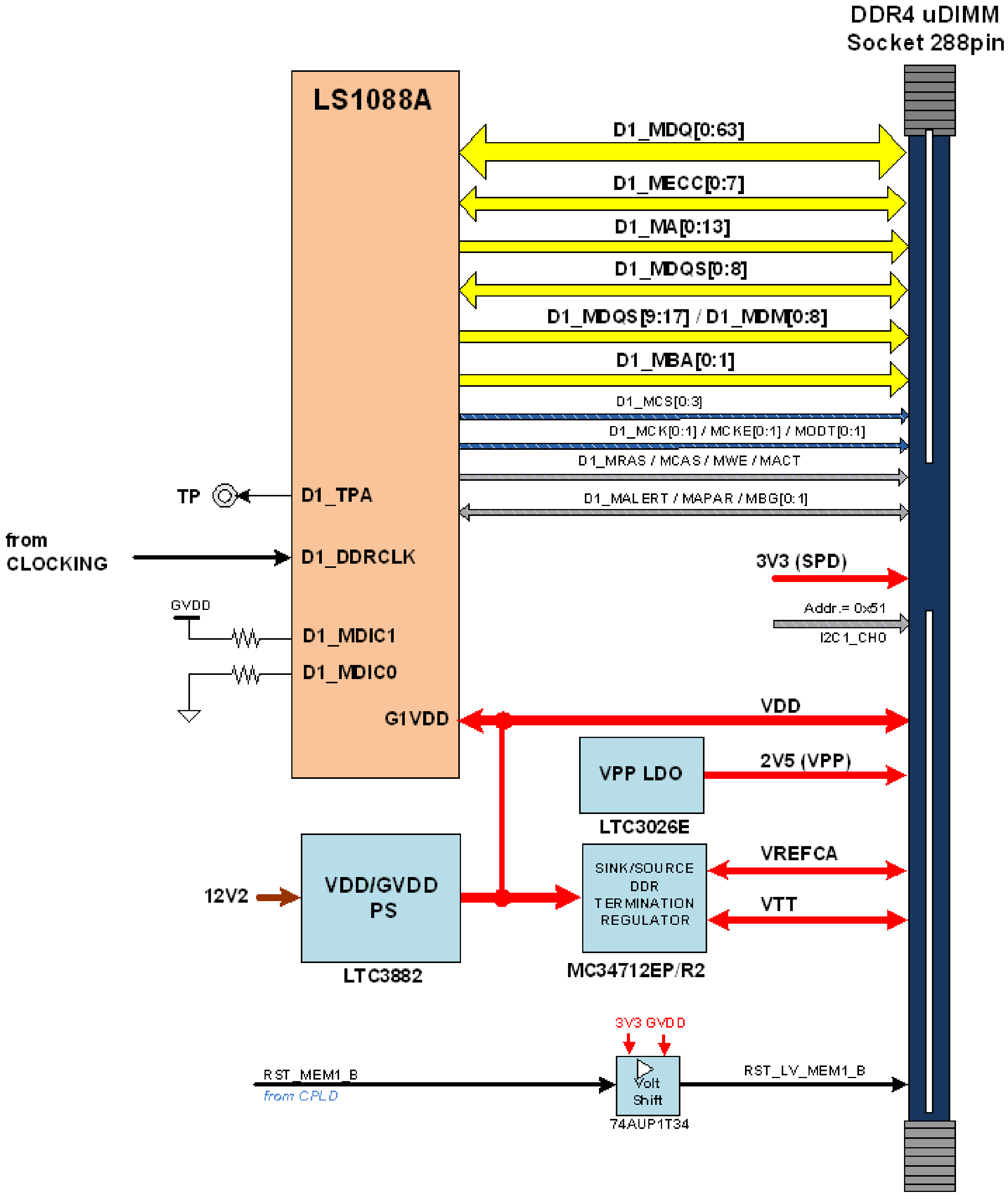

DDR4 uDIMM
Socket 288pin
LS1088A
D1_MDQ[0:63]
D1_MECC[0:7]
D1_MA[0:13]
D1_MDQS[0:8]
D1_MDQS[9:17] / D1_MDM[0:8]
D1_MBA[0:1]
D1_MCS[0:3]
D1_MCK[0:1] / MCKE[0:1] / MODT[0:1]
D1_MRAS / MCAS / MWE / MACT
D1_MALERT / MAPAR / MBG[0:1]
TP
D1_TPA
from
CLOCKING
D1_DDRCLK
GVDD
D1_MDIC1
D1_MDIC0
G1VDD
3V3 (SPD)
Addr.= 0x51
I2C1_CH0
VDD
VPP LDO
2V5 (VPP)
LTC3026E
12V2
VDD/GVDD
PS
LTC3882
SINK/SOURCE
DDR
TERMINATION
REGULATOR
MC34712EP/R2
VREFCA
VTT
3V3 GVDD
RST_MEM1_B
from CPLD
Volt
Shift
74AUP1T34
RST_LV_MEM1_B

Figure 2-6. LS1088ARDB DDR interface

2.3.1 DDR power

The LS1088ARDB power supply blocks provide the voltages shown in the table below specifically for the DDR4 subsystem. Refer to the power section for further details.

Table 2-7. DDR power supplies

Voltage Name	Voltage	Current	NOTE
GVDD	1.2 V	<= 10A	DDR socket and processor IO power.
VREFCA1	0.6 V	>= 10mA	DDR socket CA reference voltage
VTT1	0.6 V	<= 3A	DDR socket termination zsupply
VPP1	2.5 V	<= 1.5 A	DDR socket boosted drive supply.

2.3.2 Compatible DDR4 modules

The LS1088ARDB DDR interface works with any JEDEC-compliant, 288-pin, DDR4 uDIMM or RDIMM (registered) module.

The following table lists uDIMM modules that are tested and confirmed with the LS1088A DDR controller.

Table 2-8. Validated DDR4 modules

Manufacturer	Part Number	Size (GB)	Ranks	ECC?	Max Data Rate	Verified
Micron	MTA18ASF1G72AZ-2G3B1	8	Dual	Yes	2133 MT/s	Yes

The data transfer rate is 2100 MT/s to accomodate both the available bin parts (refer to the HW specification) and to use a100 MHz SYSCLK. 2133 MT/s is possible but requires special binned silicon and altered RCW/software.

2.4 SerDes (Serializer/Deserializer)

The LS1088A SerDes block supports several protocols, which on the LS1088ARDB are assigned to dedicated functions, as shown in the able below.

Table 2-9. SerDes Assignments

SerDes Block	Lane	Connectivity	Ports	Restrictions
1	3 / “A”	Freescale F104 Quad PHY #2 100M / 1G	4x 100M/1G RJ45 MagJacks ETH4..ETH7	LS1088A only
	2 / “B”	Freescale F104 Quad PHY #1 100M/1G	4x 100M/1G RJ45 MagJacks ETH0..ETH3	
	1 / “C”	TI DS125DF111 Retimer 10G optical	SFP+ Fiber Transceiver Cage ETH8	LS1088A only
	0 / “D”	Aquantia AQR105 10G copper	1x 10G RJ45 MagJack ETH9	
2	0 / “A”	PCIExpress (Gen1/2/3) x1	miniPCIe connector Slot 1	LS1088A only LS1043A does not support Gen3
	1 / “B”	PCIExpress (Gen1/2/3) x1	miniPCIe connector Slot 2	LS1043A does not support Gen3
	2 / “C”	PCIExpress (Gen1/2/3) x1	PCIExpress x4 Connector[1] Slot 3	LS1088A only
	3 / “D”	SATA	SATA Header.	When SATA is enabled, PCIExpress is limited to Gen1/2.

1. A 4x connector is used for mechanical stability; only 1x lanes are used.

The following figure shows the SerDes 1 and 2 connectivity for the LS1088ARDB.

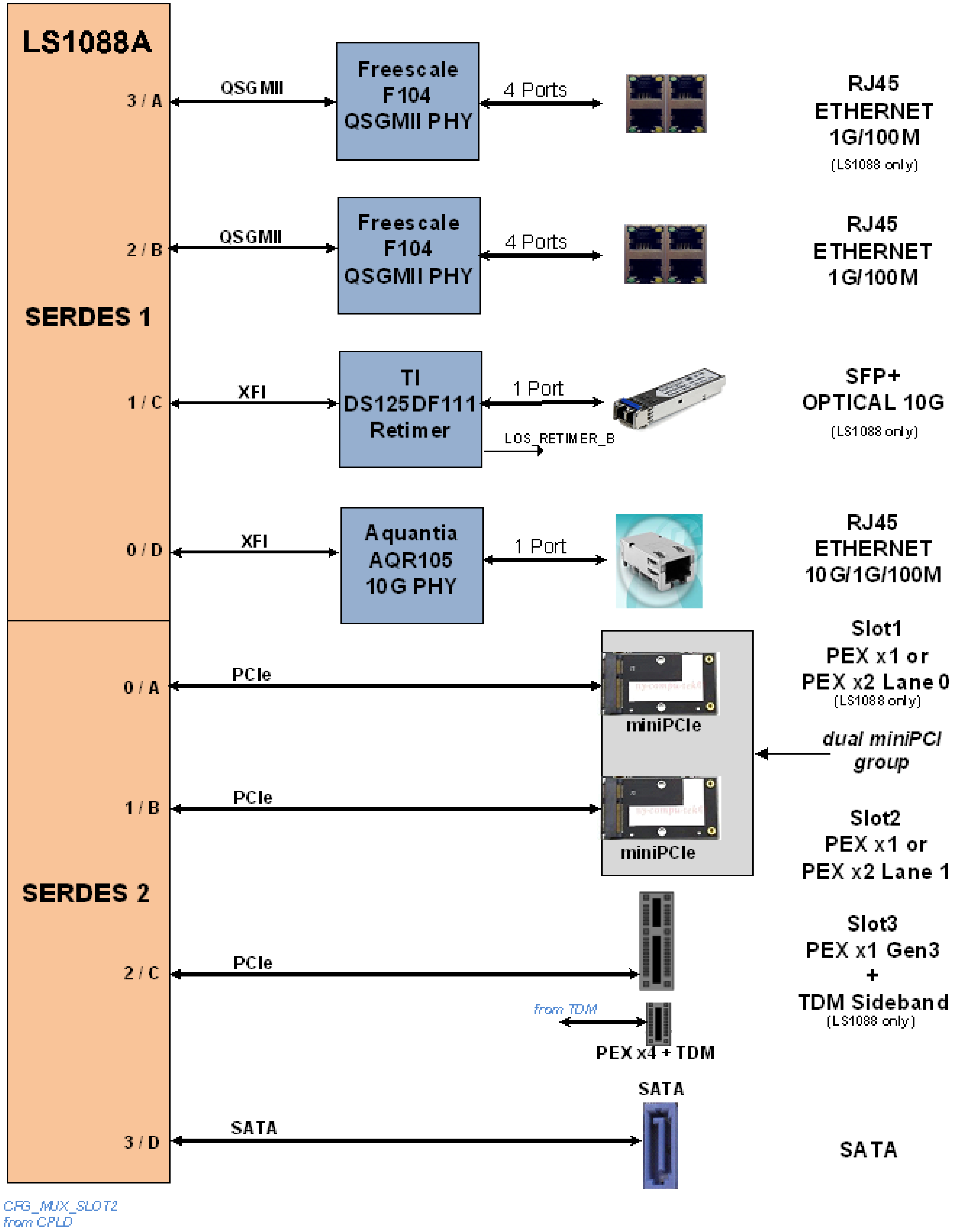

LS1088A
3 / A
QSGMII
Freescale F104 QSGMII PHY
4 Ports
RJ45 ETHERNET 1G/100M
(LS1088 only)
2 / B
QSGMII
Freescale F104 QSGMII PHY
4 Ports
RJ45 ETHERNET 1G/100M
SERDES 1
1 / C
XFI
TI DS125DF111 Retimer
1 Port
LOS_RETIMER_B
SFP+ OPTICAL 10G
(LS1088 only)
0 / D
XFI
Aquantia AQR105 10G PHY
1 Port
RJ45 ETHERNET 10G/1G/100M
0 / A
PCIe
miniPCIe
Slot1
PEX x1 or
PEX x2 Lane 0
(LS1088 only)
dual miniPCI group
1 / B
PCIe
miniPCIe
Slot2
PEX x1 or
PEX x2 Lane 1
SERDES 2
2 / C
PCIe
from TDM
PEX x4 + TDM
Slot3
PEX x1 Gen3
+
TDM Sideband
(LS1088 only)
3 / D
SATA
SATA
SATA
CFG_MUX_SLOT2
from CPLD

Figure 2-7. SerDes connectivity

2.4.1 MAC Assignment

The LS1088A associates MACs with Ethernet ports as shown in the table below. Note that MAC assignments differ for the LS1043A device.

Table 2-10. Ethernet MAC Assignment

Ethernet Port	MAC (LS1088A)	MAC (LS1043A)
ETH0	MAC7	MAC1
ETH1	MAC8	MAC2
ETH2	MAC9	MAC5
ETH3	MAC10	MAC6
ETH4	MAC3	(Unavailable)
ETH5	MAC4	
ETH6	MAC5	
ETH7	MAC6	
XFI1 (SFP)	MAC1	
XFI2 (RJ45)	MAC2	

2.4.2 miniPCIe Wi-Fi Card Support

The two miniPCIe cards support standard PCIe cards, as well as Wi-Fi cards available from a variety of vendors. Most of these cards use several reserved pins to power the RF amplifier, yet few have the same voltage requirements, so the LS1088ARDB uses a jumper block to select one of four VPA (power amplifier) voltages.

The following table describes how the reserved pins are used.

Table 2-11. miniPCIe reserved pin use

Pins	miniPCIe Standard	Wi-Fi Card Definition	Used by
37	Reserved	Ground	Quantenna QSR10GU Quantenna QSR1000
39 41	Reserved	3.3V	Quantenna QSR10GU Quantenna QSR1000
43	Reserved	Ground	Quantenna QSR10GU Quantenna QSR1000
45 47 49	Reserved	VPA	Quantenna QSR10GU Qualcomm CUS238 Qualcomm CUS239

Table continues on the next page...

Table 2-11. miniPCIe reserved pin use (continued)

Pins	miniPCIe Standard	Wi-Fi Card Definition	Used by
			Qualcomm CUS240 Qualcomm CUS260 Celeno CL2400
51	Reserved	VPA	Quantenna QSR10GU Qualcomm CUS238 Qualcomm CUS239 Qualcomm CUS240 Qualcomm CUS260 Celeno CL2400
		W_DISABLE2#	Quantenna QSR10GU Quantenna QSR1000

Note that pin 51 is not consistently defined, so a jumper on the LS1088ARDB allows support of either type.

NOTE

Be sure to double-check the card requirements and voltage jumper settings closely to prevent damage to the card!

NOTE

If using Wi-Fi/Cellular cards not listed in this document, be sure to check the pinout closely. NXP Semiconductors cannot warranty the use of unvalidated Wi-Fi cards.

The following table summarizes the Wi-Fi cards supported and the jumper configuration each requires.

Table 2-12. Wi-Fi card support

Name	VPA Requirement	Jumper Settings	Description
Quantenna QSR10GU 8x8 5G+2.4G	5V	J78: Install 1-2 J25: Install 1-2 J23: Install 2-3 AND J80: Install 1-2 J79: Install 1-2 J81: Install 1-2	Dual miniPCIe (uses both slots). Both VPA supplies must be set the same! This card uses VPA on miniPCIe1 pin 51 but W_DISABLE2# on miniPCIe2 pin 51.
Qualcomm CUS238 4x4 5G	3.5V	miniPCIe #1 (J42): J78: Install 1-2	

Table continues on the next page...

Table 2-12. Wi-Fi card support (continued)

Name	VPA Requirement	Jumper Settings	Description
		J25: Install 5-6 J23: Install 1-2 miniPCIe #2 (J45): J80: Install 1-2 J79: Install 5-6 J81: Install 1-2	
Qualcomm CUS239 4x4 5G	5V	miniPCIe #1 (J42): J78: Install 1-2 J25: Install 1-2 J23: Install 1-2 miniPCIe #2 (J45): J80: Install 1-2 J79: Install 1-2 J81: Install 1-2	
Qualcomm CUS240 4x4 2.4G	3.3V	miniPCIe #1 (J42): J78: Install 1-2 J25: Install 7-8 J23: Install 1-2 miniPCIe #2 (J45): J80: Install 1-2 J79: Install 7-8 J81: Install 1-2	
Qualcomm CUS260 4x4 2.4G	4.5V	miniPCIe #1 (J42): J78: Install 1-2 J25: Install 3-4 J23: Install 1-2 miniPCIe #2 (J45): J80: Install 1-2 J79: Install 3-4 J81: Install 1-2	
Quantenna CSR1000 4x4 5G	n/a	miniPCIe #1 (J42): J78: Remove 1-2 J23: Install 2-3 miniPCIe #2 (J45): J80: Remove 1-2 J81: Install 2-3	This card does not use the reserved pins, but instead receives 3.3V VPA power using a cable to the ATX power supply.

Table continues on the next page...

Table 2-12. Wi-Fi card support (continued)

Name	VPA Requirement	Jumper Settings	Description
Celeno CL2400 4x4 5G	5V	miniPCIe #1 (J42): J78: Install 1-2 J25: Install 1-2 J23: Install 1-2 miniPCIe #2 (J45): J80: Install 1-2 J79: Install 1-2 J81: Install 1-2	
no card/ non-Wi-Fi Card	0.0V	miniPCIe #1 (J42): J78: Remove 1-2 J23: Install 2-3 miniPCIe #2 (J45): J80: Remove 1-2 J81: Install 2-3	If a non-Wi-Fi card is used, remove jumper J78 and/or J80 to disable VPA1/VPA2.

2.4.3 SerDes Configuration

In general, because each SerDes lane connects to a dedicated function, with fixed clock rates, no SerDes programming is required other than conventional PHY setup or PCIExpress enumeration. One exception is the retimer on SerDes 1 lane “C”; these retimers default to CPRI rates and need to be programmed before use. To automate this, the self-initialization feature of the DS125DF111 is used. On reset, each device in turn copies its register settings from the 128B (or larger) EEPROM connected to the retimer I2C channel. When completed, the devices are ready to use.

The following figure shows how the retimer is connected to a storage EEPROM.

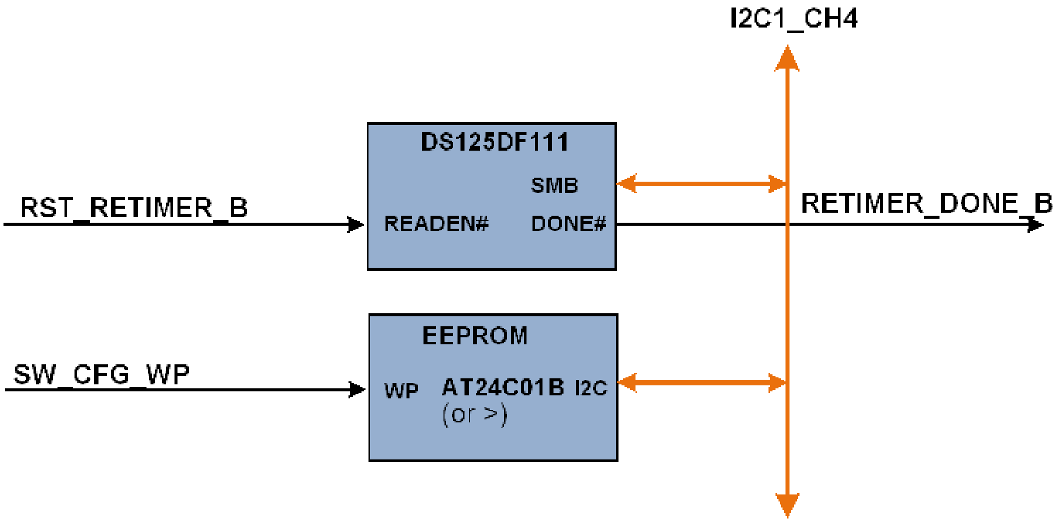


Figure 2-8. Retimer Self-Initialization

NOTE

Access to the Retimer I2C channel should be avoided for 1 (qty) * 128B * 10 b/B* 10us/b, which is less than 0.1s. Normal U-Boot startup times do not occur faster than this, and even then, I2C access is directed elsewhere (DDR I2C SPD EEPROMs), so contention is unlikely.

NOTE

Early-access boards will likely not have this EEPROM programmed, so initial bring-up software will have to do so, using the following process:

On reset, write the values in the table below to program the Retimer.

Table 2-13. DS125DF111 Retimer Programming

I2C Address	Address	Value	Notes
77	0x0D	0x0D	Program I2C mux to connect to I2C_CH5 (where the Retimer is located).
0x18	0xFF	0x0C	Send writes to Channel A (TX) and B (RX).
	0x60	0x00	
	0x61	0xB0	
	0x62	0x90	
	0x63	0xB3	
	0x64	0xCD	

Note that the Retimer can be programmed even if not in use, so it is safe to always program it, even if XFI is not being used.

2.5 EMI - Ethernet Management Interface

The LS1088ARDB has two EMI interfaces to control PHY transceivers.

EMI #1 operates at LVDD (1.8V) levels. The signals are bi-directionally shifted to 2.5V for compatibility with the Freescale F104 PHY. While the LS1088A LVDD power could be powered with 2.5V and eliminate the bidirectional buffer, no other 2.5V power is required for the processor, so this simple device allows power plane optimization.

EMI #2 is used with the AQR105 10G PHY. TVDD is powered with 1.2V and IO pins are pulled up to that level.

The following figure shows the PHY device connections.

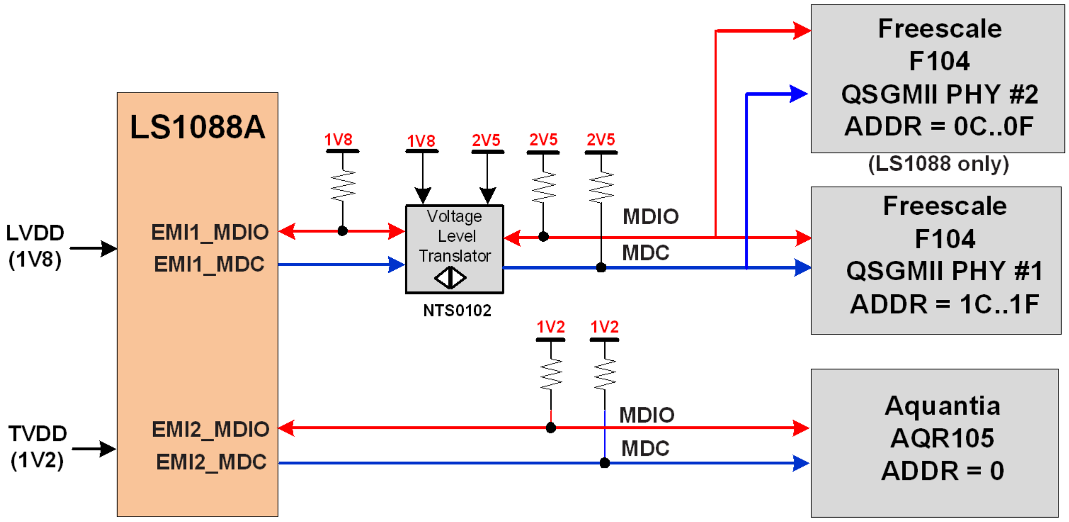

LS1088A
LVDD
(1V8)
TVDD
(1V2)
EMI1_MDIO
EMI1_MDC
EMI2_MDIO
EMI2_MDC
1V8
1V8
2V5
2V5
2V5
Voltage
Level
Translator
NTS0102
MDIO
MDC
1V2
1V2
MDIO
MDC
Freescale
F104
QSGMII PHY #2
ADDR = 0C..0F
(LS1088 only)
Freescale
F104
QSGMII PHY #1
ADDR = 1C..1F
Aquantia
AQR105
ADDR = 0

Figure 2-9. EMI interfaces

2.6 Integrated Flash Controller (IFC)

The LS1088ARDB supports serial memory, parallel memory and general IO over the IFC interface, with the following features:

- Primary QSPI boot image
- Secondary (recovery) QSPI boot image
- ONFI 2.2-compatible NAND flash
- Off-board SPI/QSPI emulation support
- Legacy GPCM access to QixMin registers

The following figure shows the IFC block diagram.

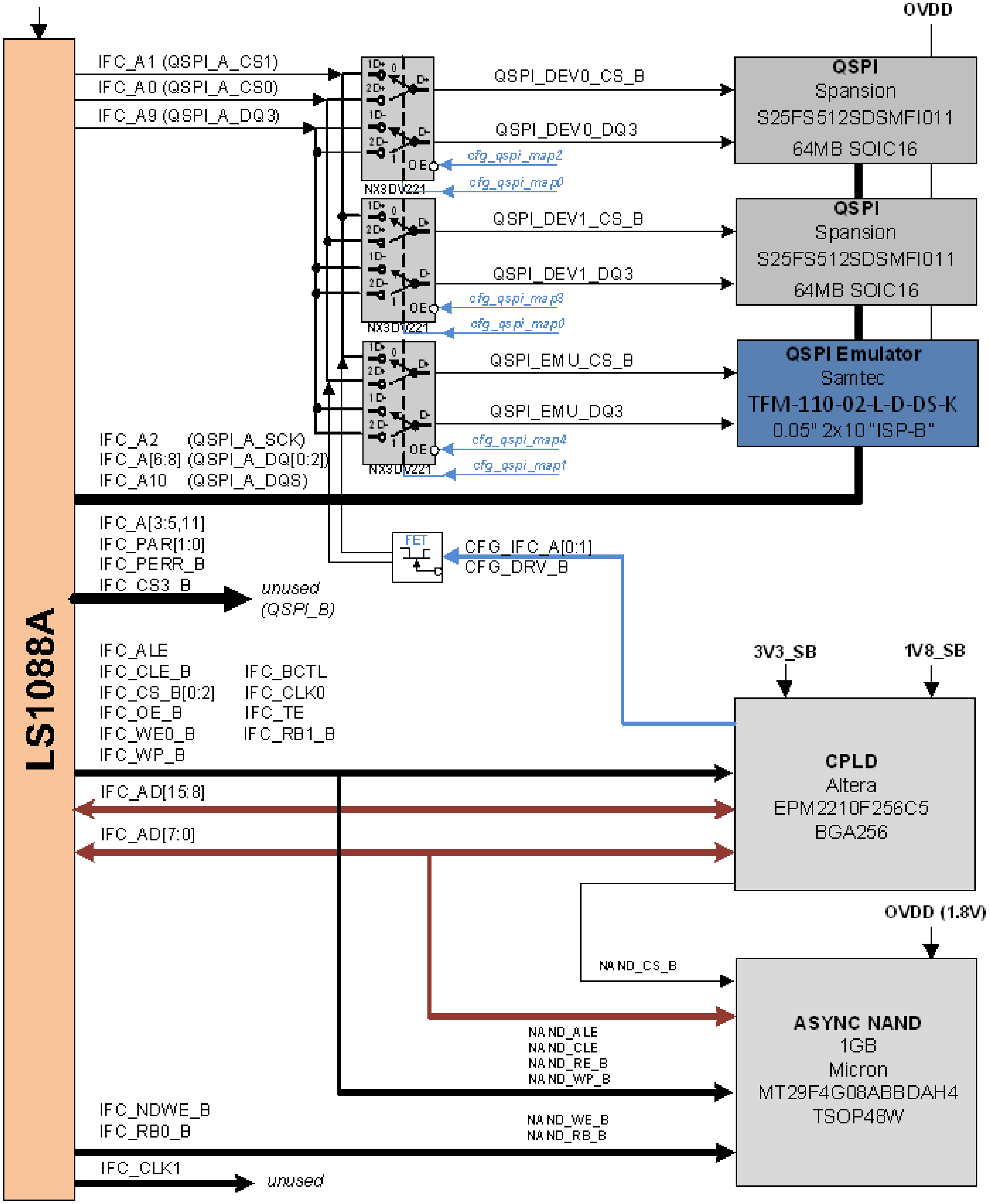

LS1088A
OVDD
IFC_A1 (QSPI_A_CS1)
IFC_A0 (QSPI_A_CS0)
IFC_A9 (QSPI_A_DQ3)
NX3DV221
NX3DV221
NX3DV221
1D+
2D+
1D-
2D-
D+
D-
OE
QSPI_DEV0_CS_B
QSPI_DEV0_DQ3
cfg_qspi_map2
cfg_qspi_map0
QSPI Spansion S25FS512SDSMFI011 64MB SOIC16
QSPI_DEV1_CS_B
QSPI_DEV1_DQ3
cfg_qspi_map3
cfg_qspi_map0
QSPI Spansion S25FS512SDSMFI011 64MB SOIC16
QSPI_EMU_CS_B
QSPI_EMU_DQ3
cfg_qspi_map4
cfg_qspi_map1
QSPI Emulator Samtec TFM-110-02-L-D-DS-K 0.05" 2x10 "ISP-B"
IFC_A2 (QSPI_A_SCK)
IFC_A[6:8] (QSPI_A_DQ[0:2])
IFC_A10 (QSPI_A_DQS)
IFC_A[3:5,11]
IFC_PAR[1:0]
IFC_PERR_B
IFC_CS3_B
unused (QSPI_B)
FET
CFG_IFC_A[0:1]
CFG_DRV_B
3V3_SB
1V8_SB
IFC_ALE
IFC_CLE_B
IFC_CS_B[0:2]
IFC_OE_B
IFC_WE0_B
IFC_WP_B
IFC_BCTL
IFC_CLK0
IFC_TE
IFC_RB1_B
CPLD Altera EPM2210F256C5 BGA256
IFC_AD[15:8]
IFC_AD[7:0]
OVDD (1.8V)
NAND_CS_B
NAND_ALE
NAND_CLE
NAND_RE_B
NAND_WP_B
ASYNC NAND 1GB Micron MT29F4G08ABBDAH4 TSOP48W
IFC_NDWE_B
IFC_RB0_B
NAND_WE_B
NAND_RB_B
IFC_CLK1
unused

Figure 2-10. IFC interface

QSPI devices and the SPI emulator can be reassigned as the boot device; all others are fixed and unchangeable. The table below summarizes the devices and chip-select connections.

Table 2-14. IFC Device Table

Device	Details	Size	Memory Controller	Addressing: SW_QMAP[2:0][1]				
				000	001	010	011	100
QSPI #0	Spansion S25FS512DSBHI210	64MB	QSPI “A”	QSPI_A CS0	QSPI_A CS1	QSPI_A CS1	-	QSPI_A CS0
QSPI #1			QSPI “A”	QSPI_A CS1	QSPI_A CS0	-	QSPI_A CS1	-
EMU	SPI Emulator (optional): PromJet + SPI option[2] DediProg[3]	varies	QSPI “A”	-	-	QSPI_A CS0	QSPI_A CS0	QSPI_A CS1
NAND	Micron MT29F4G08ABBDAH4	2GB	IFC / FCM	IFC_CS0_B				
BCSR	System Controller CPLD	4K	IFC / NOR	IFC_CS2_B				

1. SW_QMAP is used to preset BRDCFG0[7:5], which drives the signals CFG_QSPI_MAP[4:0] so as to implement the above table. The QMAP value used can be changed through the BCSR space. Refer to BRDCFG0 for details.
2. PromJets with low-voltage (1.8V) and SPI support can be adapted to the connector. Freescale does not supply the PromJet nor the custom cable. For details, see www.emutec.com.
3. The EMPro100 with 1.8V firmware and the optional ISP-ADP-intel-B cable. Freescale does not supply the emulator nor the cable. For details, see www.dediprog.com

2.6.1 IFC Architecture Changes

The LS1088ARDB emphasizes support for QSPI as the primary system boot source, instead of parallel NOR. This is a significant change from previous QDS and RDB models, but extra support has been added to maintain standard development features.

As compared to previous platforms, “virtual banking” (where hardware alters the MSB address pins of parallel NOR) is no longer possible. Software will have to carefully manage the placement of various non-bootable code images (FMan, RFS, etc.) using the dual QSPI device, NAND, eMMC or other storage.

The following table summarizes some of these IFC changes.

Table 2-15. IFC QSPI-related changes

Previous IFC Feature	New IFC Feature	Notes
VBANK	QMAP	VBANK (switches and registers) divide a single parallel NOR into 8 different images by changing the upper address lines. This is not possible with serial devices. QMAP allows selecting between 1 of 2 devices.

Table continues on the next page...

Table 2-15. IFC QSPI-related changes (continued)

Previous IFC Feature	New IFC Feature	Notes
		The majority of U-Boot user use only “vbank 0” or “vbank 4” (i.e. only two images), so this is directly compatible.
LBMAP	QMAP	LBMAP (switches and registers) allows remapping NAND, NOR and PromJet (NOR flash emulator) among the IFC chip-selects IFC_CS[0:2].
Set LBMAP to NAND	(default)	NAND is now the only device on IFC_CS0_B of the non-QSPI IFC.
BCSR Access on CS3	BCSR Access on CS2	Historically, BCSRs are on IFC_CS3_B. When QSPI is used, IFC_CS3_B does not exist, so BCSRs were reassigned to IFC_CS2_B.

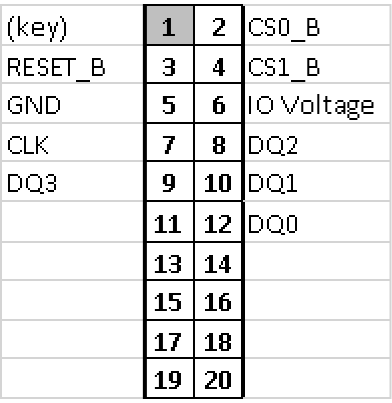
2.6.2 QSPI NOR Flash

The QSPI NOR flash devices are the Spansion S25FS512SDSMFI011 quad-SPI serial flash memories, each 64MB. These flashes are controlled with the dedicated QuadSPI controller, which replaces portions of the IFC interface.

While the LS1088A IFC interface supports two QSPI controllers, each with two chip-selects, only QSPI_A using QSPI_A_CS0 is bootable. The LS1088ARDB includes logic to re-arrange the devices on QSPI_A, so QSPI_B is not normally populated with memory.

2.6.3 QSPI NOR Emulator

The LS1088ARDB supports the use of external QSPI NOR programmers or emulators using a 20-pin 0.05” pitch header, SamTec TFM-110-02-L-D-DS-K or equivalent. The pinout is shown in the figure below.



(key)	1	2	CS0_B
RESET_B	3	4	CS1_B
GND	5	6	IO Voltage
CLK	7	8	DQ2
DQ3	9	10	DQ1
	11	12	DQ0
	13	14	
	15	16	
	17	18	
	19	20	

Figure 2-11. QSPI Emulator Header

This header may be used with the following emulators.

- EmuTec PromJet -- SPI option + custom cable required.
- DediProg EM100P -- ISP-ADP-intel-B cable required. Custom (1.8V) firmware required.

NOTE

The QSPI emulator attaches through a connector and ribbon cable, and so may not be able to run at high speed (100 MHz) as with on-board devices. Software may want to detect emulator boot (via BCSR register BRDCFG0) and limit the speed accordingly.

2.6.4 NAND Flash

The ONFI 2.2-compatible SLC NAND flash memory (Micron MT29F4G08ABBDAH4) is 1 GB in size. The NAND flash is controlled by the LS1088A IFC FCM machine.

As NAND is the only non-QSPI device on the IFC interface, no special connections are required. NAND is always on IFC_CS0_B, and its RB# signal is always on IFC_RB0_B.

Programming details include:

- MSEL = NAND machine
- Speed: 90 ns

Programmed timing values vary depending on the SYSCLK and RCW values chosen.

2.6.5 CPLD/QixMin Register Access

The BCSR registers in the CPLD can be accessed using GPCM mode in the IFC controller; however, because QSPI takes over the fixed address pins IFC_A[11:0], those pins are not available. For LS1088ARDB, setup code must instead set IFC parameters ADM_SHIFT_MODE and ADM_SHIFT tp align the address using the remaining pins. This has the side effect of reducing the address space to only 64K; however this is more than sufficient for BCSR access.

Programming details include:

- MSEL = GPCM
- ADM_SHIFT = 0 (LS1088A) or 24 (LS1043A)
- ADM_SHIFT_MODE = 0
- Speed: 300 ns

2.7 Secure Digital Host Controller (SDHC)

LS1088ARDB supports the SDHC interface by providing a connector for SD cards and a mux to route the SDHC signals (plus some SPI signals) to an on-board eMMC device. This allows evaluation of the features shown in the table below.

Table 2-16. SDHC interface features

Interface	Supports	Features
SD Slot	SD Card 2.0 or 3.0	SD UHS-1 speed modes: - SDR12, - SDR25, - SDR50, - SDR104, - DDR50 1-bit/4-bit SD/SDIO Automatic or manual EVDD control. Bootable SDHC interface.
eMMC Device >= 8GB	MTFC4GACAANA	MMC HS200 DDR Bootable eMMC interface. 8-bit interface.

The following figure shows the SDHC interface (as well as the SPI block, which is partially usable by SDHC).

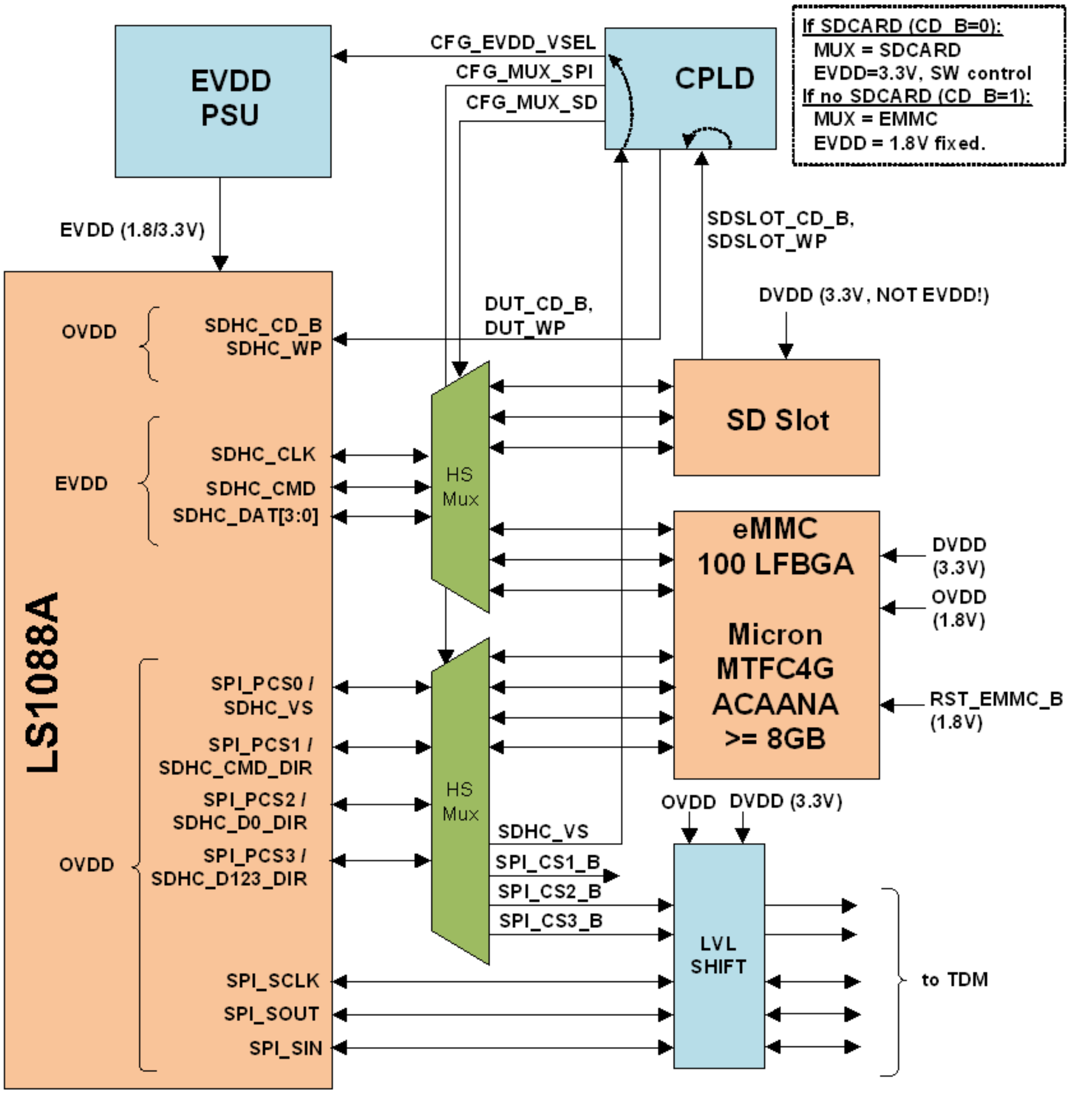

EVDD PSU
CFG_EVDD_VSEL
CFG_MUX_SPI
CFG_MUX_SD
CPLD
If SDCARD (CD_B=0):
MUX = SDCARD
EVDD=3.3V, SW control
If no SDCARD (CD_B=1):
MUX = EMMC
EVDD = 1.8V fixed.
EVDD (1.8/3.3V)
SDSLOT_CD_B,
SDSLOT_WP
DUT_CD_B,
DUT_WP
DVDD (3.3V, NOT EVDD!)
LS1088A
OVDD
SDHC_CD_B
SDHC_WP
EVDD
SDHC_CLK
SDHC_CMD
SDHC_DAT[3:0]
HS Mux
SD Slot
eMMC
100 LFBGA
Micron
MTFC4G
ACAANA
>= 8GB
DVDD (3.3V)
OVDD (1.8V)
RST_EMMC_B (1.8V)
OVDD
SPI_PCS0 / SDHC_VS
SPI_PCS1 / SDHC_CMD_DIR
SPI_PCS2 / SDHC_D0_DIR
SPI_PCS3 / SDHC_D123_DIR
HS Mux
SDHC_VS
SPI_CS1_B
SPI_CS2_B
SPI_CS3_B
OVDD
DVDD (3.3V)
LVL SHIFT
to TDM
SPI_SCLK
SPI_SOUT
SPI_SIN

Figure 2-12. SDHC interfaces

Some special features of the SDHC interface are:

- The mux routing signals to the SDHC slot or the eMMC device occurs automatically based on SDHC card detect (CD_B).
- The CPLD manages EVDD: for eMMC use, OVDD=1.8V and EVDD stays at 1.8V always. For SD card use, EVDD defaults to 3.3V and switches to 1.8V when instructed by the DUT.
- The mux is specifically blocked from connecting the EVDD-powered SDHC signals to the OVDD-powered eMMC device when the rails are different. This is a power-up configuration and cannot be changed on the fly.

- EVDD voltage switching can be managed by the processor with SDHC_VS if the SPI port is disabled. If SPI is needed for TDM, EVDD can be managed by register IO.
- SDHC CD_B and WP signals are managed by the CPLD for cases where eMMC is used, which do not provide those signals.

NOTE

The eMMC devices are 8 bits; when using eMMC, the SPI bus is not available.

2.8 Serial Peripheral Interface (SPI)

The SPI interface is used to communicate with various on-board peripherals or as alternate SDHC functions. No on-board memory is provided for SPI, as the LS1088A does not support booting from non-QSPI devices. The figure below shows the SPI interface (as well as portions of the SDHC block).

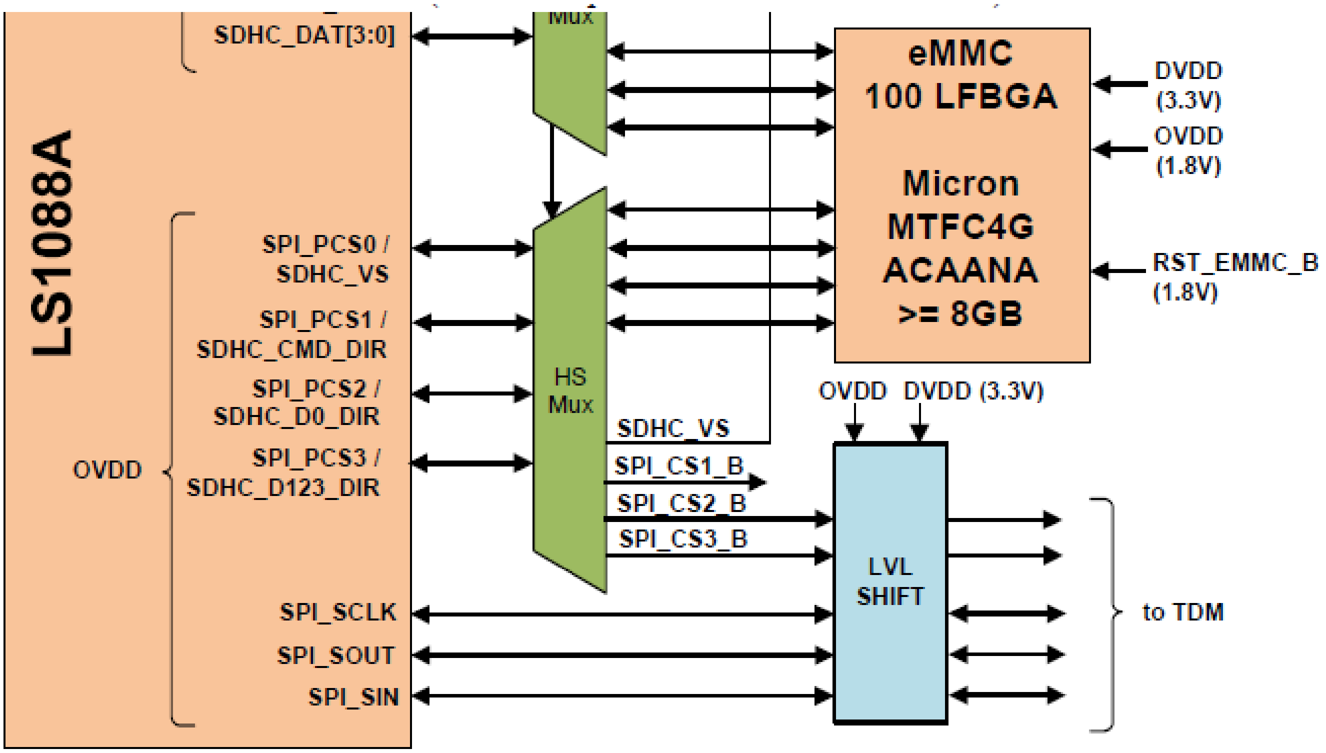

LS1088A
SDHC_DAT[3:0]
Mux
eMMC
100 LFBGA
Micron
MTFC4G
ACAANA
>= 8GB
DVDD
(3.3V)
OVDD
(1.8V)
RST_EMMC_B
(1.8V)
OVDD
SPI_PCS0 /
SDHC_VS
SPI_PCS1 /
SDHC_CMD_DIR
SPI_PCS2 /
SDHC_D0_DIR
SPI_PCS3 /
SDHC_D123_DIR
HS
Mux
SDHC_VS
SPI_CS1_B
SPI_CS2_B
SPI_CS3_B
OVDD
DVDD (3.3V)
LVL
SHIFT
to TDM
SPI_SCLK
SPI_SOUT
SPI_SIN

Figure 2-13. SPI interfaces

The following table describes the SPI functions available.

Table 2-17. SPI connectivity

SPI Signal	Function	Connection	Description
SPI_CS0_B	SDHC_VS	CPLD	Used only for SDHC_VS, SPI_CS0_B is not supported.
SPI_CS1_B	SPI_CS1_B	unused	
SPI_CS2_B	SPI_CS2_B	TDM Riser	E1/T1 framer or SLIC/SLAC Device CS1_B.
SPI_CS3_B	SPI_CS3_B	TDM Riser	E1/T1 framer or SLIC/SLAC Device CS0_B.
SPI_SCLK	SPI_SCLK	TDM Riser	E1/T1 framer or SLIC/SLAC Device on TDM Riser.
SPI_SOUT	SPI_SOUT		
SPI_SIN	SPI_SIN		

Note that RCW programming to enable alternate function “SDHC_VS” for the SDHC block causes all other SPI CS pins to be unusable.

2.9 USB Interfaces

The LS1088ARDB supports two USB 3.0 controllers, with each port connected to a different type of USB connector for maximum flexibility. The table below describes the USB ports.

Table 2-18. USB Ports

USB Port	Connector	Location	Supports
USB1	Type A	Front panel	Host Mode OTG Mode
USB2	micro AB	Front Panel	Host Mode OTG Mode

Each port supports host mode or OTG mode, with a 2-pin jumper. “Host Mode” is the default; remove the jumper to enable OTG mode.

Each port also provides an individually-controllable +5V USB power supply, the NXP NX5P2190, with per-controller enable (USBx_DRVVBUS) and fault monitoring (USBx_PWRFAULT) and up to 1.2A current per port.

The following figure shows the LS1088ARDB USB interface.

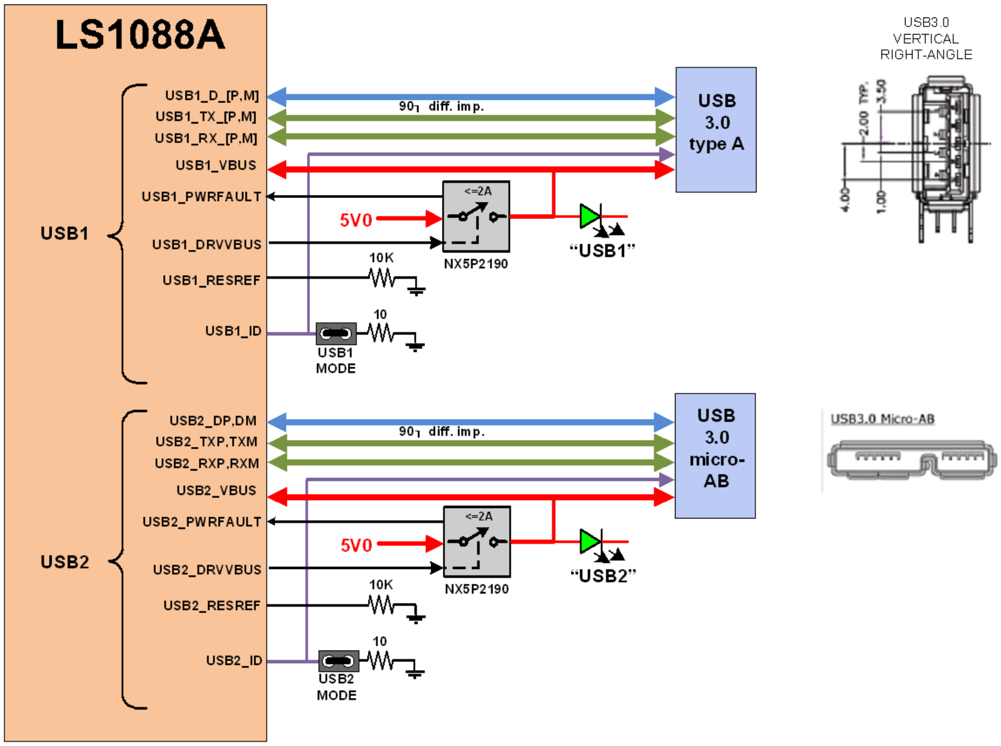

LS1088A
USB1
USB1_D_[P,M]
USB1_TX_[P,M]
USB1_RX_[P,M]
USB1_VBUS
USB1_PWRFAULT
USB1_DRVVBUS
USB1_RESREF
USB1_ID
90Ω diff. imp.
5V0
<=2A
NX5P2190
10K
10
USB1 MODE
"USB1"
USB 3.0 type A
USB3.0 VERTICAL RIGHT-ANGLE
USB2
USB2_DP,DM
USB2_TXP,TXM
USB2_RXP,RXM
USB2_VBUS
USB2_PWRFAULT
USB2_DRVVBUS
USB2_RESREF
USB2_ID
USB2 MODE
"USB2"
USB 3.0 micro-AB
USB3.0 Micro-AB

Figure 2-14. USB architecture

Each USB connector has an LED nearby ("USB1" and "USB2") which are active when USB +5V power is enabled.

2.10 I2C Ports

The LS1088A/LS1043A have four I2C buses. For all platforms, only I2C1 is used for system setup and monitoring; the other ports are used for USB, SDHC or TDM purposes. The following figure shows an overview of the main I2C connections.

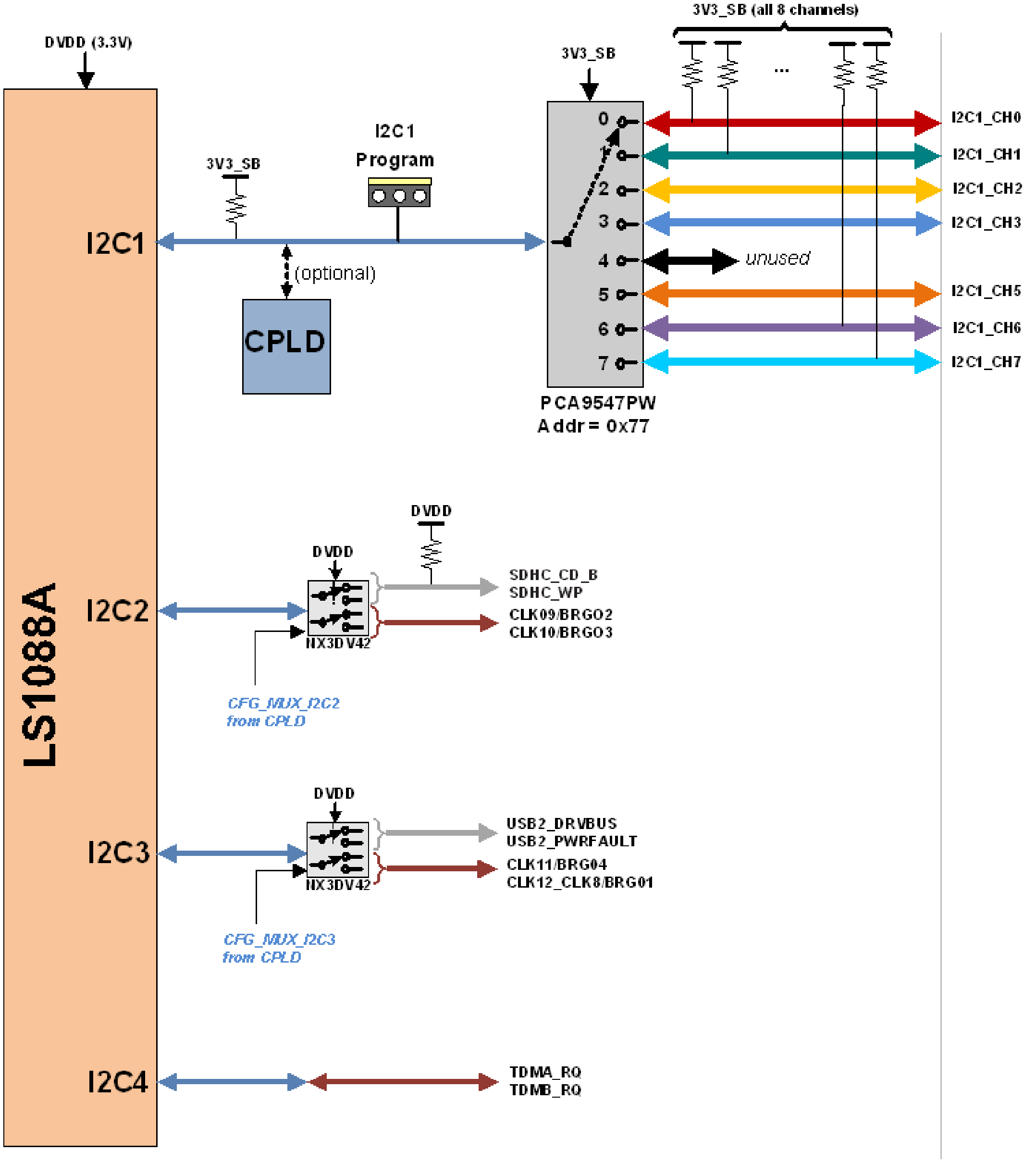

DVDD (3.3V)
LS1088A
I2C1
3V3_SB
I2C1
Program
(optional)
CPLD
3V3_SB
3V3_SB (all 8 channels)
...
0
1
2
3
4
5
6
7
unused
PCA9547PW
Addr= 0x77
I2C1_CH0
I2C1_CH1
I2C1_CH2
I2C1_CH3
I2C1_CH5
I2C1_CH6
I2C1_CH7
I2C2
DVDD
DVDD
NX3DV42
SDHC_CD_B
SDHC_WP
CLK09/BRGO2
CLK10/BRGO3
CFG_MUX_I2C2
from CPLD
I2C3
DVDD
NX3DV42
USB2_DRVBUS
USB2_PWRFAULT
CLK11/BRG04
CLK12_CLK8/BRG01
CFG_MUX_I2C3
from CPLD
I2C4
TDMA_RQ
TDMB_RQ

Figure 2-15. I2C Port Breakout

Note that to effectively manage the large number of I2C devices present, I2C1 is connected to a PCA9547 I2C multiplexer. Software must program this device to access one of the eight sub-channels, which attaches I2C devices categorized by function (clock, SerDes, slots, etc.).

The I2C devices indirectly available on I2C1 are shown in the following figure.

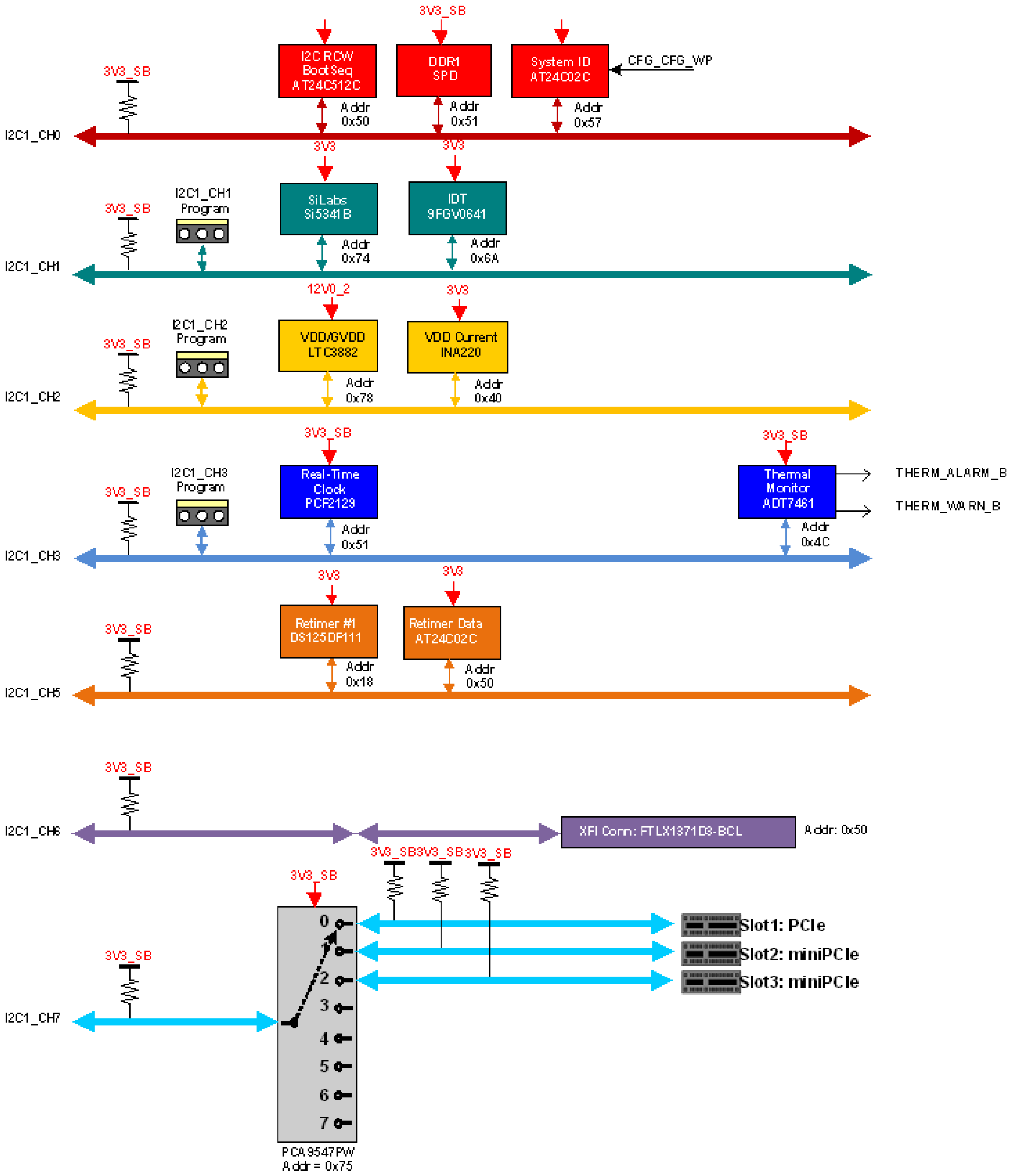

3V3_SB
I2C RCW
BootSeq
AT24C512C
Addr
0x50
DDR1
SPD
Addr
0x51
System ID
AT24C02C
Addr
0x57
CFG_CFG_WP
I2C1_CH0
3V3
3V3
3V3_SB
I2C1_CH1
Program
SiLabs
Si5341B
Addr
0x74
IDT
9FGV0641
Addr
0x6A
I2C1_CH1
12V0_2
3V3
I2C1_CH2
Program
VDD/GVDD
LTC3882
Addr
0x78
VDD Current
INA220
Addr
0x40
I2C1_CH2
3V3_SB
I2C1_CH3
Program
Real-Time
Clock
PCF2129
Addr
0x51
Thermal
Monitor
ADT7461
Addr
0x4C
THERM_ALARM_B
THERM_WARN_B
I2C1_CH3
3V3
3V3
Retimer #1
DS125DF111
Addr
0x18
Retimer Data
AT24C02C
Addr
0x50
I2C1_CH5
I2C1_CH6
XFI Conn: FTLX1371D3-BCL
Addr: 0x50
I2C1_CH7
0
1
2
3
4
5
6
7
PCA9547PW
Addr = 0x75
Slot1: PCIe
Slot2: miniPCIe
Slot3: miniPCIe

Figure 2-16. I2C1 I2C Devices

For I2C[2:4], the pins default to USB and SDHC functions; alternately they can be used as TDM channel signals. No programming is necessary unless TDM is required.

Note that, for the PCA9547, the device is reset when the system is reset. The device defaults to channel 0 by default, insuring transparent access to the DDR SPD EEPROM on reset.

The following table summarizes the available I2C devices.

Table 2-19. I2C1 Bus Device Table

I2C Channel	7b Addr.	Description	Device	Notes
(all)	-	LS1088A	I2C Master	
	0x66	CPLD	I2C Slave	I2C access to CPLD BCSRs (registers).
	0x77	PCA9547	I2C Bus Multiplexer	First-level multiplexer.
CH0	0x50	RCW + PBL	Atmel AT24C512	4KiB EEPROM: Stores RCW and PBLOADER data. Write protectable.
	0x51	SPD EEPROM	SPD: 512B paged EEPROM Thermal: 256B Microchip MCP98242	DIMM SPD and temperature data. SPD contents follow established DDR4 SPD standards. Thermal monitors are usually, but not guaranteed, present.
	0x57	SystemID	Atmel AT24C02	256B EEPROM containing factory-preset MAC addresses, serial number/errata, etc. Write protectable.
CH1	0x6A	SerDes1 Clock SerDes2 Clock	IDT IDT9FGV0641	
	0x74	SYSCLK Clock DDRCLK Clock PHY Clocks	SiliconLabs Si5341B	
CH2	0x40	VDD Volt/Curr Monitor	TI INA220	Reports V+I data for VDD.
	0x5A	VDD/GVDD Power	LinearTech LTC3882	Global address: channel 0
	0x5B			Global address: channel 1
	0x63			General (paged) PMBus port.
CH3	0x4C	Thermal Monitor	OnSemi ADT7461A	Monitors processor thermal diodes.
	0x51	Real-time clock	NXP PCF2129	Time and periodic interrupt.
CH4	open			
CH5	0x18	Retimer #1	TI DS100RT110	Retimer (RX+TX) for SerDes 1 lane “C”
	0x50	Retimer Data	Atmel AT24C02	Retimer initialization data (optional)
CH6	0x50	SFP Cage	FTLX1371D3-BCL	
CH7	0x75	I2C Bus Multiplexer	NXP PCA9547	Second-level multiplexer for PCIe slot access.
CH7+CH0	n/a	PCIe Slot #1	Board-specific device(s).	Address, if any at all, depends upon card.
CH7+CH1	n/a	miniPCIe Slot #2		
CH7+CH2	n/a	miniPCIe Slot #3		
CH7+CH[3:7]	open			

NOTE

“7b” addresses do not include the R/W bit as an address member, though some datasheets might do so. For consistency, all I2C addresses are 7 bits of address only.

2.11 Interrupts

Most LS1088A IRQ pins are reserved for use with the TDM facility. The remaining pins are used to merge various board-related interrupt sources for handling by the processor; or for general GPIO use. The interrupts are connected as shown in the figure below.

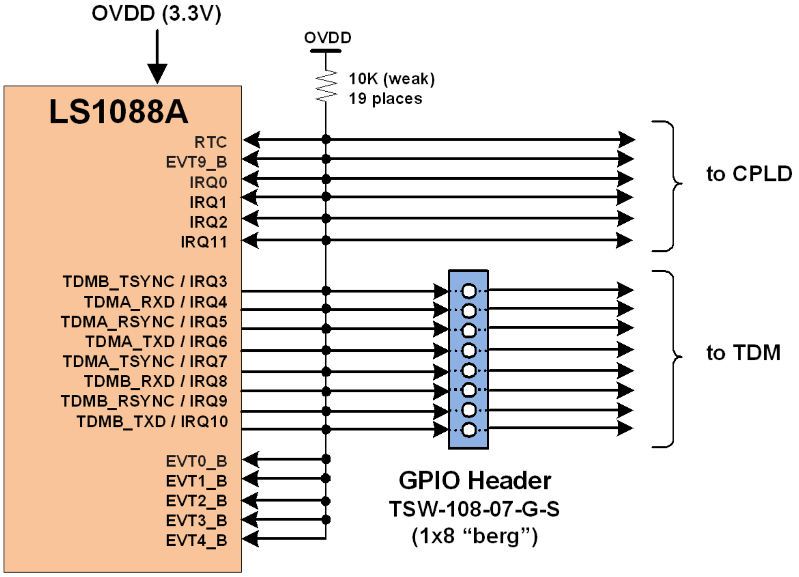

OVDD (3.3V)
OVDD
10K (weak)
19 places
LS1088A
RTC
EVT9_B
IRQ0
IRQ1
IRQ2
IRQ11
TDMB_TSYNC / IRQ3
TDMA_RXD / IRQ4
TDMA_RSYNC / IRQ5
TDMA_TXD / IRQ6
TDMA_TSYNC / IRQ7
TDMB_RXD / IRQ8
TDMB_RSYNC / IRQ9
TDMB_TXD / IRQ10
EVT0_B
EVT1_B
EVT2_B
EVT3_B
EVT4_B
to CPLD
to TDM
GPIO Header
TSW-108-07-G-S
(1x8 "berg")

Figure 2-17. Interrupt Architecture

The table below summarizes the interrupt assignments used.

Table 2-20. Interrupt Assignments

Signal Name	Supported Functions	Description
IRQ0_B	TDM Interrupts	TDMRiser Card Interrupts: IRQ_TDM1_B -- Channel 0 IRQ_TDM2_B -- Channel 1
	RTC Interrupt	Real-Time Clock Interrupt: IRQ_RTC_B -- PCF2129 RTC
IRQ1_B	1G Ethernet Interrupts	QSGMII PHY Interrupts: IRQ_QSPHY1_B -- F104 PHY #1 IRQ_QSPHY2_B -- F104 PHY #2
IRQ2_B	10G Ethernet Interrupt	AQR105 PHY Interrupt: IRQ_AQR105_B -- AQR105 #1
IRQ3_B	unused	IRQ[3:10] used only for TDM purposes
IRQ4_B		
IRQ5_B		

Table continues on the next page...

Table 2-20. Interrupt Assignments (continued)

Signal Name	Supported Functions	Description
IRQ6_B		
IRQ7_B		
IRQ8_B		
IRQ9_B		
IRQ10_B		
IRQ11_B	unused	reserved

2.12 System Controller

The LS1088ARDB system controller (or “CPLD” for short) controls the operation of the system, including the following features:

- AC power supply control
- On-board regulator control and sequencing
- Reset assertion to processor and devices.
- Processor and system configuration
- Interrupt management
- System alert monitoring and status display
- Remapping of system boot devices
- Control and status registers

The following figures show the system controller architectural details.

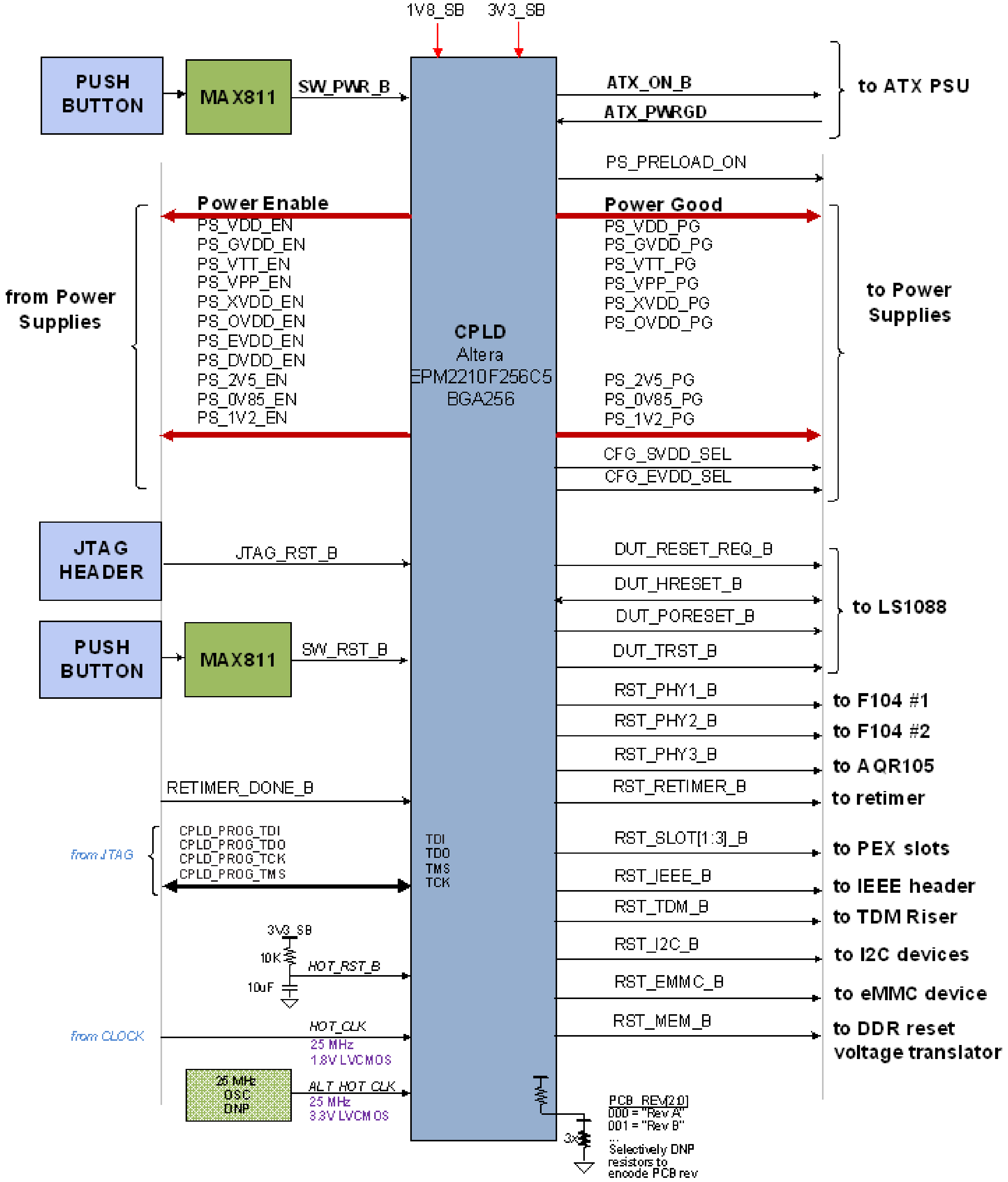

1V8_SB
3V3_SB
PUSH BUTTON
MAX811
SW_PWR_B
ATX_ON_B
ATX_PWRGD
to ATX PSU
PS_PRELOAD_ON
Power Enable
PS_VDD_EN
PS_GVDD_EN
PS_VTT_EN
PS_VPP_EN
PS_XVDD_EN
PS_OVDD_EN
PS_EVDD_EN
PS_DVDD_EN
PS_2V5_EN
PS_0V85_EN
PS_1V2_EN
from Power Supplies
CPLD
Altera
EPM2210F256C5
BGA256
Power Good
PS_VDD_PG
PS_GVDD_PG
PS_VTT_PG
PS_VPP_PG
PS_XVDD_PG
PS_OVDD_PG
PS_2V5_PG
PS_0V85_PG
PS_1V2_PG
CFG_SVDD_SEL
CFG_EVDD_SEL
to Power Supplies
JTAG HEADER
JTAG_RST_B
DUT_RESET_REQ_B
DUT_HRESET_B
DUT_PORESET_B
DUT_TRST_B
to LS1088
PUSH BUTTON
MAX811
SW_RST_B
RST_PHY1_B
to F104 #1
RST_PHY2_B
to F104 #2
RST_PHY3_B
to AQR105
RETIMER_DONE_B
RST_RETIMER_B
to retimer
from JTAG
CPLD_PROG_TDI
CPLD_PROG_TDO
CPLD_PROG_TCK
CPLD_PROG_TMS
TDI
TDO
TMS
TCK
RST_SLOT[1:3]_B
to PEX slots
RST_IEEE_B
to IEEE header
RST_TDM_B
to TDM Riser
3V3_SB
10K
HOT_RST_B
10uF
RST_I2C_B
to I2C devices
RST_EMMC_B
to eMMC device
from CLOCK
HOT_CLK
25 MHz
1.8V LVCMOS
RST_MEM_B
to DDR reset voltage translator
25 MHz
OSC
DNP
ALT_HOT_CLK
25 MHz
3.3V LVCMOS
3x
PCB_REV[2:0]
000 = "Rev A"
001 = "Rev B"
...
Selectively DNP resistors to encode PCB rev

Figure 2-18. System controller architecture

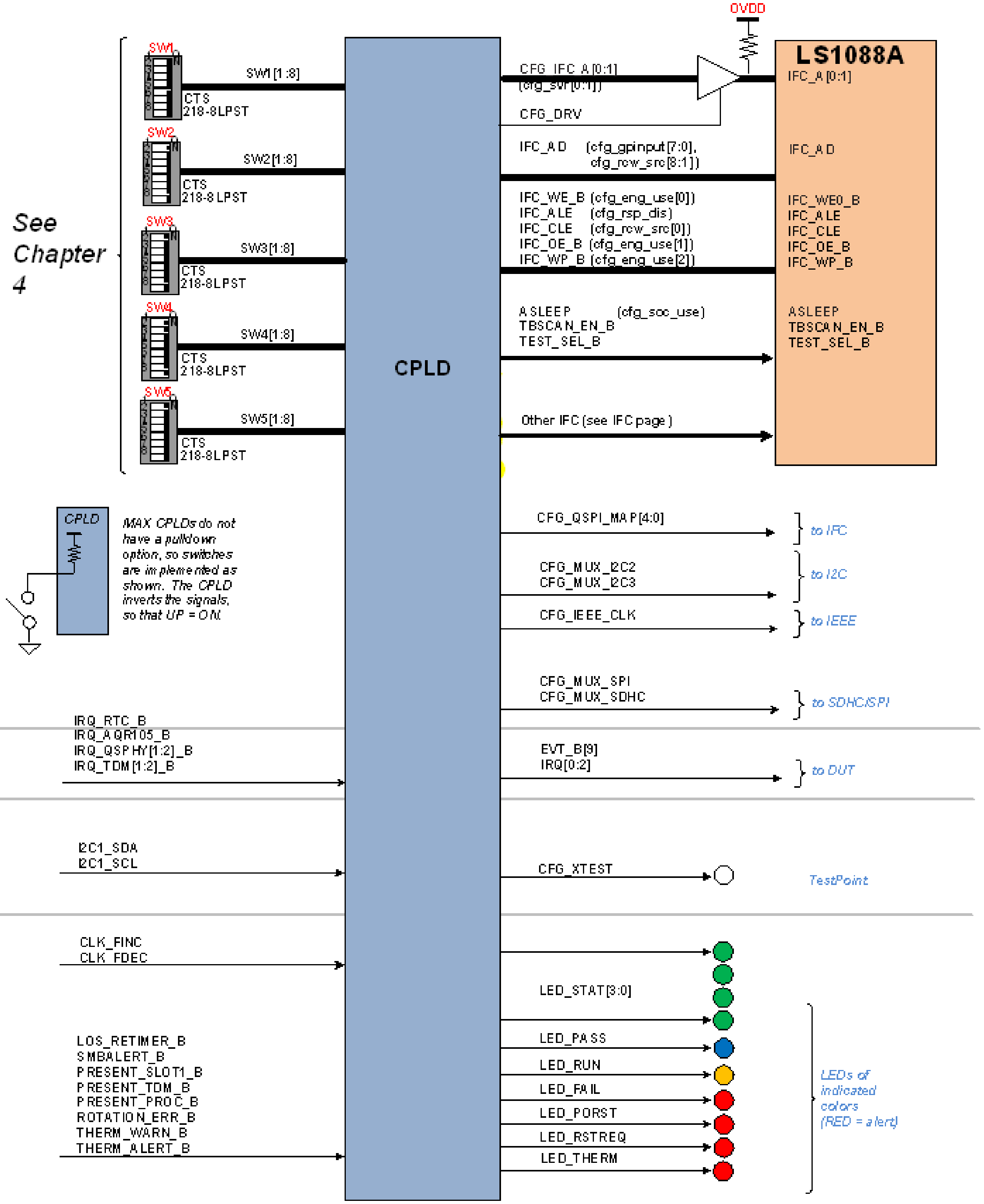

OVDD
LS1088A
SW1
SW1[1:8]
CTS
218-8LPST
SW2
SW2[1:8]
CTS
218-8LPST
SW3
SW3[1:8]
CTS
218-8LPST
SW4
SW4[1:8]
CTS
218-8LPST
SW5
SW5[1:8]
CTS
218-8LPST
See Chapter 4
CPLD
CFG_IFC_A[0:1]
(cfg_svr[0:1])
CFG_DRV
IFC_A[0:1]
IFC_AD (cfg_gpinput[7:0], cfg_rcw_src[8:1])
IFC_AD
IFC_WE_B (cfg_eng_use[0])
IFC_ALE (cfg_rsp_dis)
IFC_CLE (cfg_rcw_src[0])
IFC_OE_B (cfg_eng_use[1])
IFC_WP_B (cfg_eng_use[2])
IFC_WE0_B
IFC_ALE
IFC_CLE
IFC_OE_B
IFC_WP_B
ASLEEP (cfg_soc_use)
TBSCAN_EN_B
TEST_SEL_B
ASLEEP
TBSCAN_EN_B
TEST_SEL_B
Other IFC (see IFC page)
CPLD
MAX CPLDs do not have a pulldown option, so switches are implemented as shown. The CPLD inverts the signals, so that UP = ON.
CFG_QSPI_MAP[4:0]
to IFC
CFG_MUX_I2C2
CFG_MUX_I2C3
to I2C
CFG_IEEE_CLK
to IEEE
CFG_MUX_SPI
CFG_MUX_SDHC
to SDHC/SPI
IRQ_RTC_B
IRQ_AQR105_B
IRQ_QSPHY[1:2]_B
IRQ_TDM[1:2]_B
EVT_B[9]
IRQ[0:2]
to DUT
I2C1_SDA
I2C1_SCL
CFG_XTEST
TestPoint
CLK_FINC
CLK_FDEC
LED_STAT[3:0]
LOS_RETIMER_B
SMBALERT_B
PRESENT_SLOT1_B
PRESENT_TDM_B
PRESENT_PROC_B
ROTATION_ERR_B
THERM_WARN_B
THERM_ALERT_B
LED_PASS
LED_RUN
LED_FAIL
LED_PORST
LED_RSTREQ
LED_THERM
LEDs of indicated colors (RED = alert)

Figure 2-19. System controller architecture (continued)

The system controller is implemented in an Altera CPLD, the EPM2210F256C5 256-ball micro-BGA.

The system controller is powered continuous 3.3V and 1.8V regulators, powered from the ATX PSU +5V standby power. This allows it to control all aspects of board bring-up, including initial power sequencing.

2.12.1 System Configuration

The system controller uses switches to configure the target system into various modes. Switches are sampled and stored in registers. Some registers can be changed from software running on the processor, such as BRDCFG5 which is used to configure the I2C multiplexers among other settings. Other settings, such as those that change HW configurations sampled only at reset, such as the RCW_SRC location, cannot be changed. The following figure shows the configuration hardware arrangement.

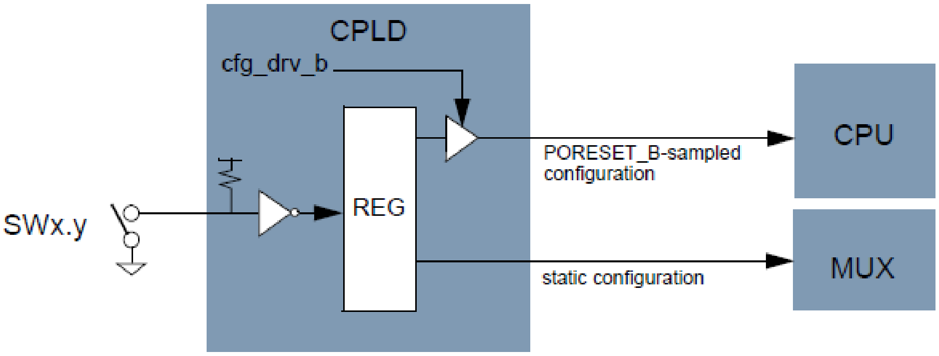


Figure 2-20. Configuration sampling

Note that switches cause a short to ground when closed. To make it easier to set and “read” switches, values are inverted in the CPLD, so that when a switch is “ON”, the value used is “1”.

All switches can be read from software to easily determine the system configuration for reporting purposes (see the CMS chapter of the programming model).

The table below describes the LS1088A reset configuration signals.

Table 2-21. Processor configuration settings

Configuration Signal	LS1088A Pin	Switch	Register	Description
CFG_RCW_SRC[8:1]	IFC_AD[15:8]	SW1[1:8]	DUTCFG0[7:0]	Most-significant 8 bits of RCW location.
CFG_RCW_SRC0	IFC_CLE	SW2[1]	DUTCFG1[0]	Least-significant bit of RCW location.
CFG_RSP_DIS	IFC_ALE	SW5[4]	DUTCFG6[7]	Pause after fetching RCW.
CFG_SVR[0:1]	IFC_A[0:1]	SW3[2:3]	DUTCFG2[2:1]	Silicon variations.
TEST_SEL_B[1]	TEST_SEL_B	SW3[1]	DUTCFG2[0]	Silicon variations.
CFG_ENG_USE0	IFC_WE_0_B	SW5[1:3]	DUTCFG11[7:5]	Optional features.

Table continues on the next page...

Table 2-21. Processor configuration settings (continued)

Configuration Signal	LS1088A Pin	Switch	Register	Description
CFG_ENG_USE1 CFG_ENG_USE2	IFC_OE_B IFC_WP_B			
CFG_SOC_USE	ASLEEP	-	DUTCFG6[0]	Undefined option.
CFG_GPINPUT[1:0]	IFC_AD0	SW5[7:8]	DUTCFG12[1:0]	User defined.
TBSCAN_EN_B	TBSCAN_EN_B	SW4[8]	CTL[7]	Controls whether the JTAG operates in boundary scan or debug mode.

1. TEST_SEL_B is a static signal (constantly driven), unlike most other processor configuration signals.

All other configuration signals are static and unrelated to the processor. The following table summarizes these configuration signals.

Table 2-22. Non-Processor Configuration Settings

Configuration Signal	Switch	Register	Description
CFG_SYSCLK	SW3[6:8]	BRDCFG1[3:0]	Controls SYSCLK speed.
CFG_MUX_I2C2	-	BRDCFG5[7]	Controls routing of I2C2 signals: SDHC or TDM.
CFG_MUX_I2C3	-	BRDCFG5[6]	Controls routing of I2C3 signals: USB2 or TDM.
CFG_MUX_SPI	SW1+SW2[1][1]	BRDCFG5[3]	Controls routing of SPI signals; SPI or eMMC.
CFG_MUX_SDHC		BRDCFG5[2]	Controls routing of SDHC signals: SDHC or eMMC.
CFG_IEEE_CLK	-	BRDCFG5[4]	Controls source of TSEC_GTX_CLK: internal or external.
CFG_REFCLK_SEL	SW3[5]	BRDCFG5[0]	Controls reference source for SerDes2 and attached slots.

1. These switches set the RCW_SRC location as shown in the previous table. If the boot device selected is the eMMC device, the muxes are set to allow this; otherwise, SDHC and SPI are the defaults (which allows SDHC boot).

There are switches not listed above; these switches do not directly control board signals, but instead alter the behavior of the system controller. Refer to the next chapter for complete details.

2.12.2 System Startup

The system controller manages the orderly startup of the system by managing power enables and reset assertion (including device configuration), in the order shown in the table below.

Table 2-23. Startup sequence

Controller	Step	Actions	Description
PWR	1	Wait for power-on event.	Triggered by SW_PWR_B, or by setting SW_AUTO_ON=1.
PWR	2	Enable ATX power supply.	Enable ATX PSU, wait for it to report “power good”. LS1088A PORESET_B is asserted during power-up.
PWR	3	Apply power to group 1.	Enable group 1 power supplies, wait for all members to report “power good” (if supported): DVDD OVDD 0V85 2V1
PWR	4	Apply power to group 2.	Enable group 2 power supplies, wait for all members to report “power good” (if supported). VDD XVDD
PWR	5	Apply power to group 3.	Enable group 3 power supplies, wait for all members to report “power good” (if supported). GVDD VTT VPP
PWR	6	Complete power sequencer; trigger reset sequencer.	Control transfers from PWR to RST handlers. The power sequencer watches for power switch events and will restart at PWR step #1 if any are detected.
RST	1	Assert all resets.	LS1088A PORESET_B is asserted if not already asserted. Device resets are asserted: RST_SLOT[1:3]_B RST_PHY[1:3]_B RST_MEM_B RST_I2C_B RST_RETIMER_B RST_IEEE_B RST_TDM_B The LS1088A asserts ASLEEP and HRESET_B in response. ASLEEP is monitored with a LED, otherwise the signals are ignored.
RST	2	Wait for reset clear.	Wait for reset assertion to be released. The reset sequencer will stall as long as any reset input is asserted: JTAG_HRST_B SW_RST_B
RST	2	Sample switches.	Internal registers are reset to defaults.

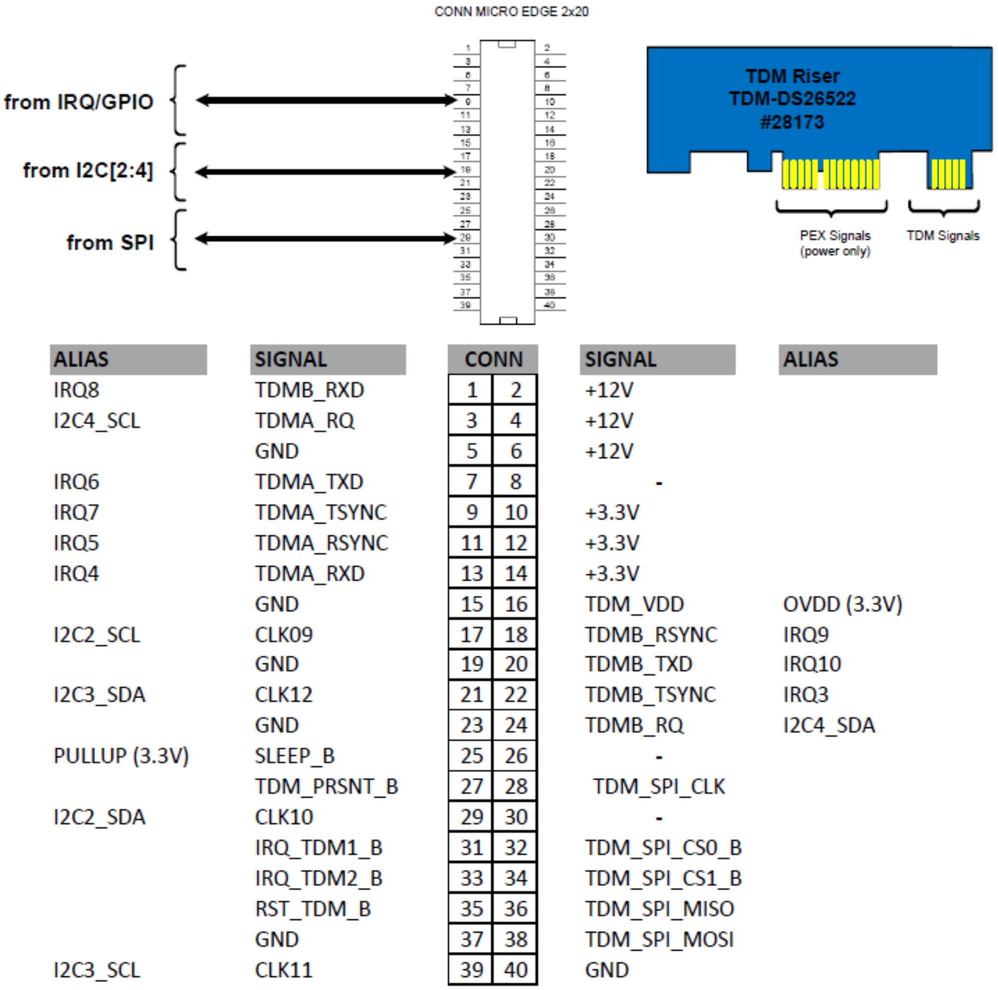
Table continues on the next page...

Table 2-23. Startup sequence (continued)

Controller	Step	Actions	Description
			Registers which default to switch values are set now.
RST	3	Drive configuration values.	Reset-sampled configurations signals are driven: CFG_RCW_SRC[8:0] CFG_RSP_DIS CFG_SVR[0:1] CFG_ENG_USE[0:2] CFG_SOC_USE CFG_GPIN[Static (constant) configuration signals are driven: CFG_QSPI_MAP[4:0] CFG_MUX_I2C[2:4] CFG_MUX_SLOT3 CFG_MUX_SPI CFG_MUX_SDHC CFG_IEEE_CLK CFG_DRV_B is asserted now, to help with the few config signals that cannot be driven by the CPLD.
RST	4	Release resets.	Release all resets shown in step #1. The processor samples reset pins at this time.
RST	5	Tristate reset-sampled pins.	3 SYSCLK periods after step 4: De-assert CFG_DRV_B. Tristate config drive outputs. This insures proper configuration hold time. The CPLD is no longer involved in reset activity.
RST	6	Processor reset.	The LS1088A begins loading RCW data from the configured source. Once RCW load is complete, the LS1088A de-asserts HRESET_B and ASLEEP. If RCW data is correct, the system will start running code. If there is an error, RESET_REQ_B is asserted and the system halts.
RST	7	Reset sequence complete.	The CPLD has finished reset management. The reset sequencer watches for power switch events and will restart at RST step #1 if any are detected.

2.13 TDM Interface

The TDM facilities of the LS1088ARDB are supported through a special card, the “TDM Riser”. This card contains a Maxim DS26522 E1/T1 interface, and is installed in PCIExpress slot #1, which supports the special side-band connector containing TDM signals. The following figure shows the TDM architecture.



ALIAS	SIGNAL	CONN		SIGNAL	ALIAS
IRQ8	TDMB_RXD	1	2	+12V	
I2C4_SCL	TDMA_RQ	3	4	+12V	
	GND	5	6	+12V	
IRQ6	TDMA_TXD	7	8	-	
IRQ7	TDMA_TSYNC	9	10	+3.3V	
IRQ5	TDMA_RSYNC	11	12	+3.3V	
IRQ4	TDMA_RXD	13	14	+3.3V	
	GND	15	16	TDM_VDD	OVDD (3.3V)
I2C2_SCL	CLK09	17	18	TDMB_RSYNC	IRQ9
	GND	19	20	TDMB_TXD	IRQ10
I2C3_SDA	CLK12	21	22	TDMB_TSYNC	IRQ3
	GND	23	24	TDMB_RQ	I2C4_SDA
PULLUP (3.3V)	SLEEP_B	25	26	-	
	TDM_PRSNT_B	27	28	TDM_SPI_CLK	
I2C2_SDA	CLK10	29	30	-	
	IRQ_TDM1_B	31	32	TDM_SPI_CS0_B	
	IRQ_TDM2_B	33	34	TDM_SPI_CS1_B	
	RST_TDM_B	35	36	TDM_SPI_MISO	
	GND	37	38	TDM_SPI_MOSI	
I2C3_SCL	CLK11	39	40	GND	

Figure 2-21. TDM Riser architecture

NOTE

The TDM Riser is not included with the system; to order, use part number “TDM-DS26522”.

To use the TDM function of the LS1088ARDB system, the steps shown in the following table must be followed.

Table 2-24. TDM Riser configuration

Configuration	Location	Description	Side Effects
RCW[IIC2_EXT] = 010	Boot Image RCW Data	Converts I2C2_SCL to CLK09 Converts I2C2_SDA to CLK10	SDHC_CD_B and SDHC_WP are not readable by the SDHC IP. Software can check the signals by reading QixMin register STAT_PRES1.
BRDCFG5[7] = 1	QixMin Registers		
RCW[IIC3_EXT] = 100	Boot Image RCW Data	Converts I2C3_SCL to CLK11 Converts I2C3_SDA to CLK12	USB2 is not usable.
BRDCFG5[6] = 1	QixMin Registers		
RCW[IIC4_EXT] = 010	Boot Image RCW Data	Converts I2C4_SCL to TDMA_RQ Converts I2C4_SDA to TDMB_RQ	
BRDCFG5[3] = 0	QixMin Registers	Connects SPI to TDM Riser	Only needed if booted from eMMC.
RCW[IRQ_EXT] = 001	Boot Image RCW Data	Converts IRQ[3] to TDMB_TSYNC Converts IRQ[4] to TDMA_RXD Converts IRQ[5] to TDMA_RSYNC Converts IRQ[6] to TDMA_TXD Converts IRQ[7] to TDMA_TSYNC Converts IRQ[8] to TDMB_RXD Converts IRQ[9] to TDMB_RSYNC Converts IRQ[10] to TDMB_TXD	None.

NOTE

When the TDM Riser is installed, the PCIExpress functionality for that slot is not available.

2.14 Thermal Management

The LS1088A has a thermal monitoring diode which can be measured by an ADT7461 thermal monitor device. Software can perform direct die temperature readings with an accuracy of ±1 °C. See the I2C section for addressing information.

In addition to monitoring, the ADT7461 can also triggering alarms upon detecting thermal problems. To do this, ADT7461 THERM and ALERT signals are connected to the system controller, as well as to status LEDs. The CPLD uses these signals to power down the system, to protect the LS1088A from over-temperature damage.

No programming is necessary; however, the default thermal limit is 85°C which may be higher than desired. To change the thermal trip point, issue the following I2C writes:

Table 2-25. Thermal Monitor configuration

I2C Write	Description
0x77 0x0B 0x0B	Program PCA9547 to get access to I2C1_CH3 (sub-channel of ADT7461).
0x68 0x19 <TLIMIT>	Program thermal limit of ADT7461 external measurement (the processor). “TLIMIT” can be any user determined value; for example, decimal 50.

NOTE

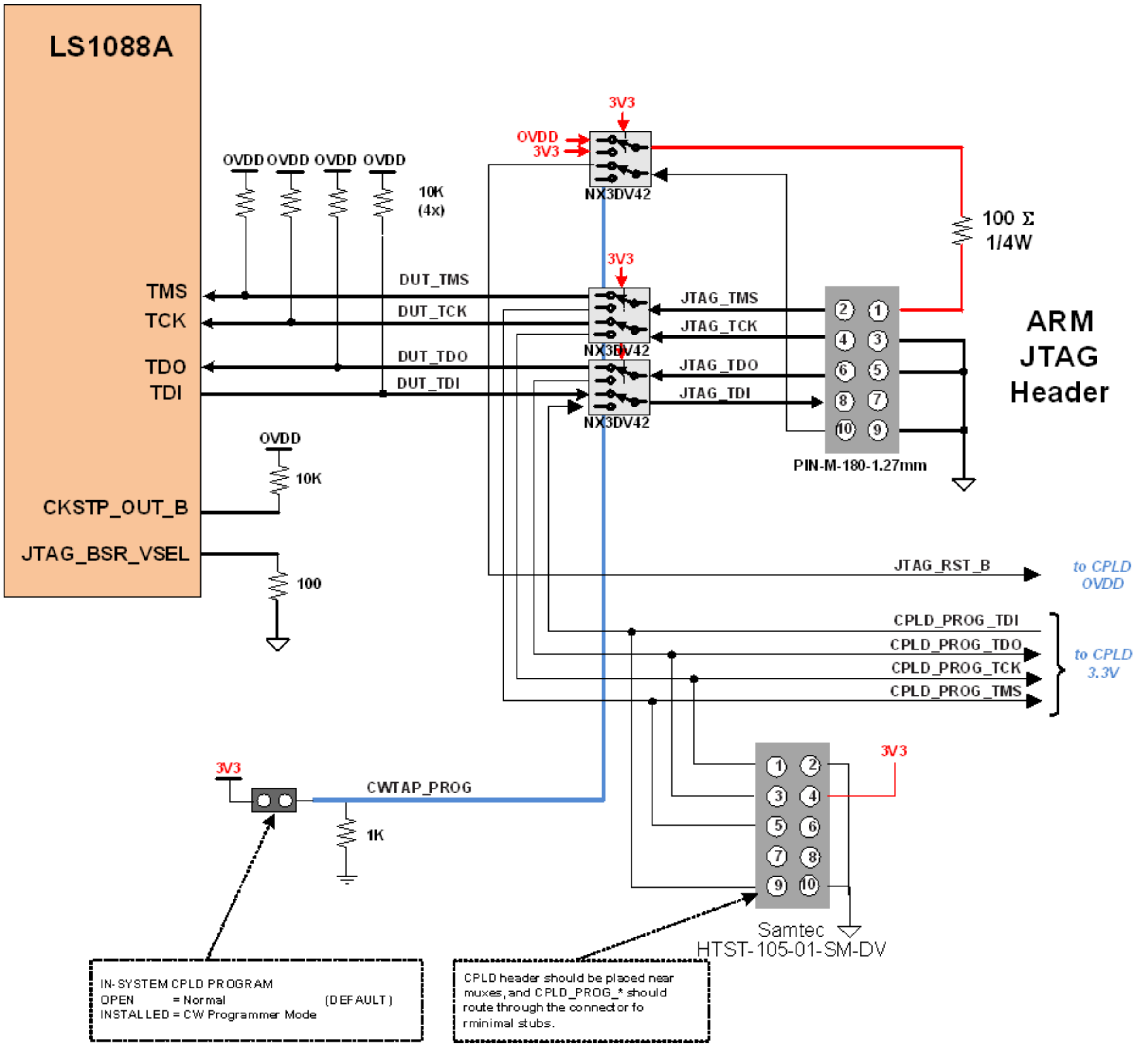
The special mode switch “SW_BYPASS_B” disables thermal monitoring. This is often necessary if operating the board without a processor installed, or when using an interposer, as an open thermal diode connection will measure as 127°C.

2.15 JTAG Port

The JTAG port provides access to the processor using a standard 10-pin ARM debug connector, which allows easy connection of a CodeWarrior TAP (CWTap) module for debugging and download support.

Normally, the JTAG header is just a simple direct connection. For the LS1088ARDB, the JTAG signals are multiplexed and can be optionally routed to the CPLD programming inputs. The CWTap has the ability drive standard CPLD/FPGA programming files over JTAG, so this allows systems to update the CPLD (if necessary) without requiring purchase of a third-party programmer.

The resulting JTAG architecture is shown in the following figure.


LS1088A
TMS
TCK
TDO
TDI
CKSTP_OUT_B
JTAG_BSR_VSEL
OVDD OVDD OVDD OVDD
10K
(4x)
DUT_TMS
DUT_TCK
DUT_TDO
DUT_TDI
OVDD
10K
100
OVDD
3V3
3V3
NX3DV42
3V3
NX3DV42
NX3DV42
JTAG_TMS
JTAG_TCK
JTAG_TDO
JTAG_TDI
100 Σ
1/4W
2 1
4 3
6 5
8 7
10 9
PIN-M-180-1.27mm
ARM
JTAG
Header
JTAG_RST_B
to CPLD
OVDD
CPLD_PROG_TDI
CPLD_PROG_TDO
CPLD_PROG_TCK
CPLD_PROG_TMS
to CPLD
3.3V
3V3
CWTAP_PROG
1K
3V3
1 2
3 4
5 6
7 8
9 10
Samtec
HTST-105-01-SM-DV

IN-SYSTEM CPLD PROGRAM
OPEN = Normal (DEFAULT)
INSTALLED = CW Programmer Mode

CPLD header should be placed near muxes, and CPLD_PROG_* should route through the connector fo rminimal stubs.

Figure 2-22. JTAG connections

Note that the complexity shown above is entirely due to requirements to support in-system programming of the CPLD from a CodeWarrior TAP. A typical customer implementation would eliminate the multiplexer for a very straightforward connection.

2.16 Serial Ports (DUART)

The LS1088A provides two DUART blocks, which supports two full serial ports with hardware flow control, or four serial ports with no flow control. The board has a stacked conventional DB9M connector, so that two serial ports are simultaneously available.

Two transceivers from Linear Technology (LTC2804-1) translate the signals to RS232 levels. The following figure shows the UART connectivity.

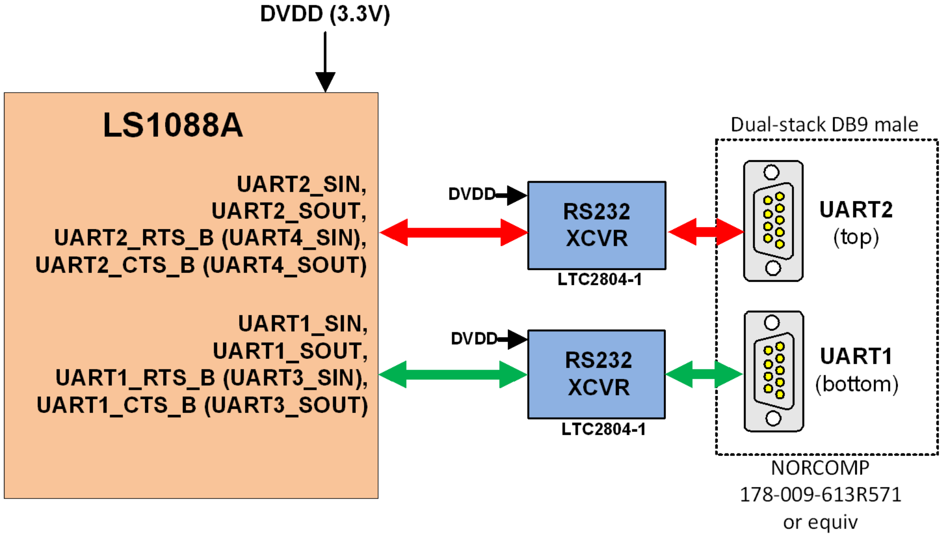

DVDD (3.3V)
LS1088A
UART2_SIN,
UART2_SOUT,
UART2_RTS_B (UART4_SIN),
UART2_CTS_B (UART4_SOUT)
UART1_SIN,
UART1_SOUT,
UART1_RTS_B (UART3_SIN),
UART1_CTS_B (UART3_SOUT)
DVDD
RS232
XCVR
LTC2804-1
DVDD
RS232
XCVR
LTC2804-1
Dual-stack DB9 male
UART2
(top)
UART1
(bottom)
NORCOMP
178-009-613R571
or equiv

Figure 2-23. DUART interfaces

2.16.1 Quad Serial Port Support

The serial ports support converting each 4-wire serial port into two independent 2-wire serial ports (for a total of four). When enabled, the RTS1_B/RTS2_B signals become TXD3/TXD4, while CTS1_B/CTS2_B becomes RXD3/RXD4.

To evaluate UART3 and/or UART4, a custom DB9 interface cable must be created, as shown in the figure below.

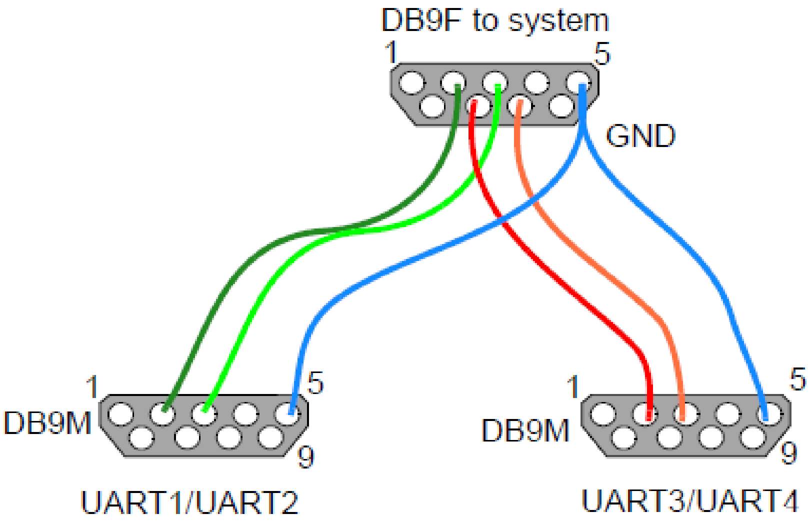

DB9F to system
1
5
GND
1
5
DB9M
9
UART1/UART2
1
5
DB9M
9
UART3/UART4

Figure 2-24. 4-Wire to 2-Wire UART adapter

NOTE

Freescale Semiconductor does not make or supply this cable.

2.17 Ethernet (ETH) Controller Interface

The LS1088ARDB does not support legacy (RGMII) Ethernet controllers, instead opting for much faster QSGMII connectivity available over SerDes interface 1. The pins are not used, as shown in the figure below.

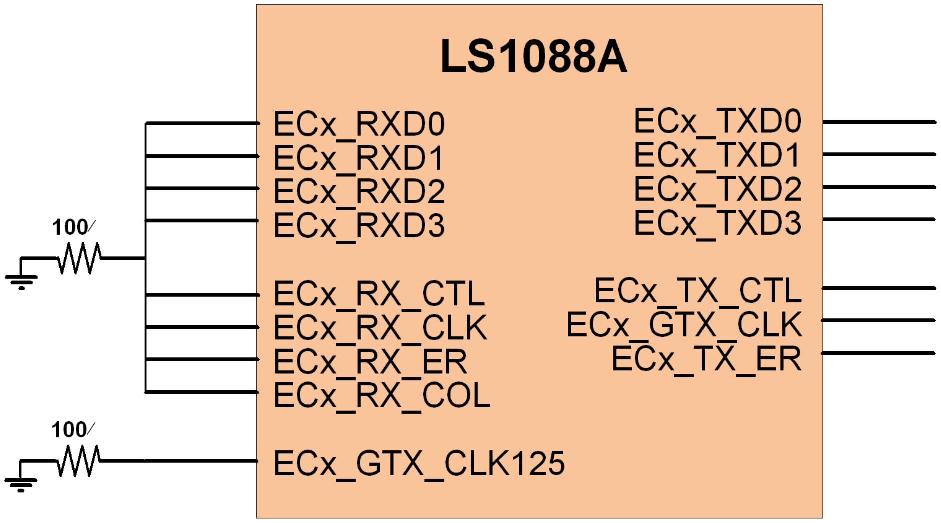

LS1088A
ECx_RXD0
ECx_RXD1
ECx_RXD2
ECx_RXD3
ECx_RX_CTL
ECx_RX_CLK
ECx_RX_ER
ECx_RX_COL
ECx_GTX_CLK125
ECx_TXD0
ECx_TXD1
ECx_TXD2
ECx_TXD3
ECx_TX_CTL
ECx_GTX_CLK
ECx_TX_ER
100⁄
100⁄

Figure 2-25. Unused ETH controllers

2.18 IEEE 1588™ PTP Support

The LS1088ARDB includes support for the IEEE 1588™ Precision Time Protocol (PTP) which works in tandem with the ETH controller to time-stamp the incoming packets. A 12-pin header is provided on the RDB to allow support of 1588 protocol.

The following figure shows the organization of the IEEE 1588 system.

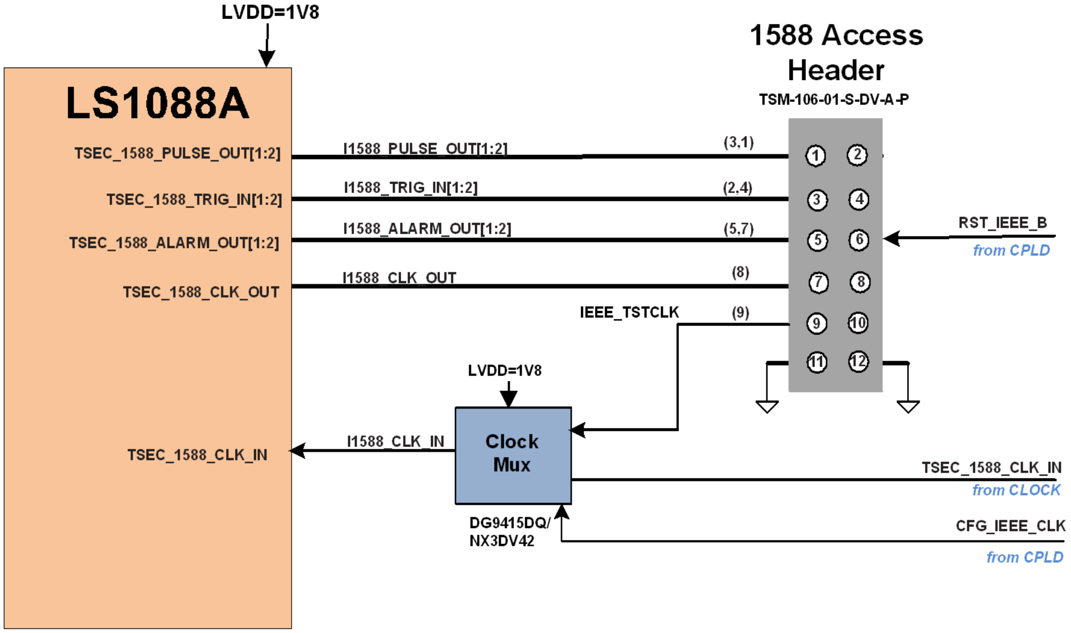

LVDD=1V8
LS1088A
TSEC_1588_PULSE_OUT[1:2]
TSEC_1588_TRIG_IN[1:2]
TSEC_1588_ALARM_OUT[1:2]
TSEC_1588_CLK_OUT
TSEC_1588_CLK_IN
1588 Access Header
TSM-106-01-S-DV-A-P
I1588_PULSE_OUT[1:2]
(3,1)
I1588_TRIG_IN[1:2]
(2,4)
I1588_ALARM_OUT[1:2]
(5,7)
I1588_CLK_OUT
(8)
IEEE_TSTCLK
(9)
① ②
③ ④
⑤ ⑥
⑦ ⑧
⑨ ⑩
⑪ ⑫
RST_IEEE_B
from CPLD
LVDD=1V8
I1588_CLK_IN
Clock Mux
DG9415DQ/
NX3DV42
TSEC_1588_CLK_IN
from CLOCK
CFG_IEEE_CLK
from CPLD

Figure 2-26. IEEE 1588 interface

The IEEE1588 test header provides testing options.

Table 2-26. IEEE 1588 Port

IEEE1588 Feature	Specifics	Description
Clocks	Input clock	ETH reference clock (to processor) is driven from an on-board 125.0 MHz oscillator source. Under software configuration, it may be clocked from the IEEE1588 header instead.
	Output clock	ETH output clock is driven to the IEEE1588 header.
Signals	Other related signals	All remaining IEEE1588 signals are connected to the dedicated header.

2.19 GPIO Access

The LS1088A has no dedicated GPIO pins. Instead, GPIO functions are multiplexed internally onto other pins, which must be disabled before using the GPIO functions. For the LS1088ARDB, GPIO access is provided via IRQ pins IRQ[3:10], but only when those pin are not used for IRQ or TDM purposes. The following figure shows the GPIO access header.

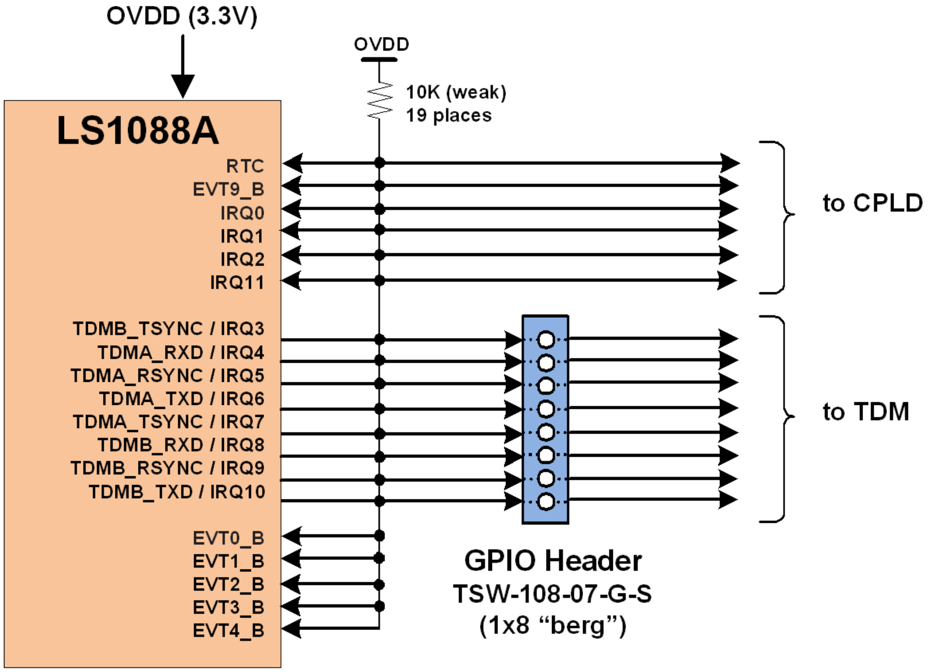

OVDD (3.3V)
LS1088A
RTC
EVT9_B
IRQ0
IRQ1
IRQ2
IRQ11
TDMB_TSYNC / IRQ3
TDMA_RXD / IRQ4
TDMA_RSYNC / IRQ5
TDMA_TXD / IRQ6
TDMA_TSYNC / IRQ7
TDMB_RXD / IRQ8
TDMB_RSYNC / IRQ9
TDMB_TXD / IRQ10
EVT0_B
EVT1_B
EVT2_B
EVT3_B
EVT4_B
OVDD
10K (weak)
19 places
to CPLD
to TDM
GPIO Header
TSW-108-07-G-S
(1x8 “berg”)

Figure 2-27. GPIO interface

By programming the RCW “IRQ_EXT” field properly, GPIO access is an unused IRQ pins can be reassigned to GPIO purposes. These signals flow through a 1x8 “Berg” header, with pinout as shown in the table below.

Table 2-27. GPIO Connector

Header Pin	LS1088A Pin	LS1088A Alternate Function	LS1088A GPIO Function
1	IRQ[3]	TDMB_TSYNC	GPIO_3[27]
2	IRQ[4]	TDMA_RXD	GPIO_3[28]
3	IRQ[5]	TDMA_RSYNC	GPIO_3[29]
4	IRQ[6]	TDMA_TXD	GPIO_4[4]
5	IRQ[7]	TDMA_TSYNC	GPIO_4[5]
6	IRQ[8]	TDMB_RXD	GPIO_4[6]
7	IRQ[9]	TDMB_RSYNC	GPIO_4[7]
8	IRQ[10]	TDMB_TXD	GPIO_4[8]

Note that all IRQ signals have a weak pull-up, so GPIO pins programmed to input mode will default to “1”.

Chapter 3
Programming Model

The Qixis device contains many registers that are accessible over the IFC, JTAG TAP, or I2C external interfaces; or from optional internal devices such a DCM or ARM management processor. This chapter explains each of the registers in the register block.

Table 3-1. Qixis Register Location Map

Base	+0	+1	+2	+3	+4	+5	+6	+7
000	ID	VER	QVER	MODEL	MINOR	CTL	AUX	-
008	-	STATSYS	ALARM	STATPRS1	STATPRS2	-	LED	-
010	RCFG	-	-	-	-	-	-	-
018	-	-	-	-	-	LOSSTAT	-	-
020	-	-	PWREVENT	-	PWRMSTAT	PWRSTAT1	PWRSTAT2	-
028	-	-	-	-	-	-	-	-
030	CLKSPD1	-	-	CLKID	SYSCLKD0	SYSCLKD1	-	-
038	-	-	-	-	-	-	-	-
040	RSTCTL	RSTSTAT	REASON	RSTFRC1	RSTFRC2	RSTFRC3	-	-
048	-	-	-	RSTMASK1	RSTMASK2	RSTMASK3	-	-
050	BRDCFG0	BRDCFG1	BRDCFG2	-	BRDCFG4	BRDCFG5	-	-
058	-	BRDCFG9	-	-	-	-	-	-
060	DUTCFG0	DUTCFG1	DUTCFG2	-	-	-	DUTCFG6	-
068	-	-	-	DUTCFG11	DUTCFG12	-	-	-
070	-	-	-	-	-	-	-	-
078	-	-	-	-	-	-	-	-
080	-	-	-	-	-	-	-	-
088	-	-	-	-	-	-	-	-
090	-	-	-	-	-	-	-	-
098	-	-	-	-	-	-	-	-
0A0	-	-	-	-	-	-	-	-
0A8	-	-	-	-	-	-	-	-
0B0	-	-	-	-	-	-	-	-
0B8	-	-	-	-	-	-	-	-
0C0	-	-	-	-	-	-	-	-

Table continues on the next page...

Table 3-1. Qixis Register Location Map (continued)

Base	+0	+1	+2	+3	+4	+5	+6	+7
0C8	-	-	-	-	-	-	-	-
0D0	-	-	-	-	-	-	-	-
0D8	CMSA	CMSD	-	-	-	-	-	-
0E0	-	-	-	-	-	-	-	-
0E8	-	-	-	-	-	-	-	-
0F0	-	-	-	-	-	-	-	-
0F8	-	-	-	-	-	-	-	-

3.1 Register Conventions

An undefined register address does not have any defined register value. Reads and writes to such addresses should be avoided. If you attempt to read such addresses, undefined data is returned. Undefined register addresses may be defined in the future.

For registers which do not define all bits, reserved bits behave as follows:

- DUTCFG: read as 1; write 1's to unused bits.
- Others: read as 0; write 0's to unused bits.

Future definitions of reserved bits will maintain backward compatibility with the above rules.

3.2 Resets

The reset values for registers are defined as follows:

- NONE - Register cannot be reset. Applies to read-only registers.
- ARST - Auxiliary Reset: registers are reset when the system powers up with standby power, and is never altered by hardware again. Software writes are preserved.
- CRST - Control Reset: registers are not reset except under exceptional situations, such as power cycles or watchdog timeout.
- RRST - Reconfig Reset: configuration registers are reset as with CRST unless a reconfiguration reset has been requested.
- GRST - General Reset: always reset, for any reason.

Generally, a register is wholly affected by only one reset source, however there are exceptions and these are shown with separate reset lines for each reset source.

3.3 Identification Registers

The ID block of registers contain values which identify the board, including major revisions to the board and/or system controller FPGA or CPLD.

3.3.1 ID

The ID register contains a unique classification number. This ID number is used by system software to identify board types. The ID number remains same for all board revisions.

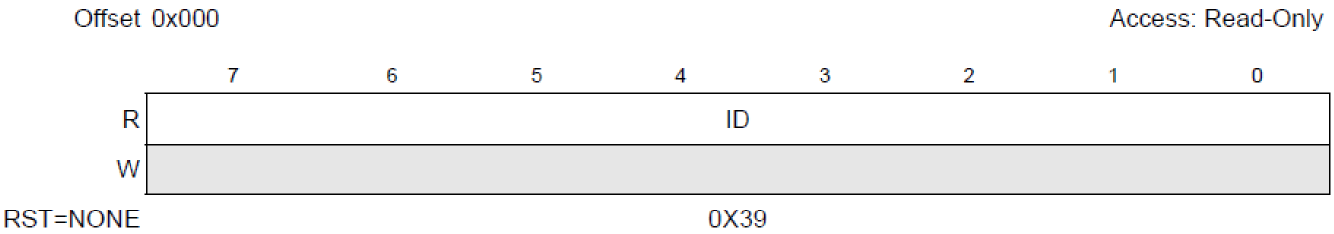


Figure 3-1. ID Register

Table 3-2. ID Register Field Descriptions

Bits	Name	Description
7-0	ID	The board-specific identifier for the system. 0x39= LS1088ARDB

3.3.2 VER

The VER register records version information for the PCB board as well the board architecture. The PCB board version can change without impacting the board architecture version, and vice versa.

Figure 3-2.

Offset 0x001 Access: Read-Only

	7	6	5	4	3	2	1	0
R	ARCH				BRD			
W								
RST=NONE	0001				0001			

Figure 3-2. VER Register

Table 3-3. VER Register Field Descriptions

Bits	Name	Description
7-4	ARCH	Board architecture version: 1= V1 2= V2 (etc.)
3-0	BRD	PCB board version: 1= Rev A (or pre-release) 2= Rev B (etc.)

The ARCH field is used by QIXIS and software to handle architecture changes. The ARCH field allows the use of a common QIXIS image across multiple board revisions, if supported by the device.

The BRD field lets end users determine the version of the board. Software can use this field to print board version identification. For example:

```
printf("Board Version: %c", (get_pixis( VER ) & 0x0F) + 'A' - 1 );
```

3.3.3 QVER

The QVER register contains the major version information of the Qixis system controller FPGA. Minor revision information is contained within the TagROM (see: QTAG).

Offset 0x002 Access: Read-Only

	7	6	5	4	3	2	1	0
R	QVER							
W								
RST=NONE	00000001							

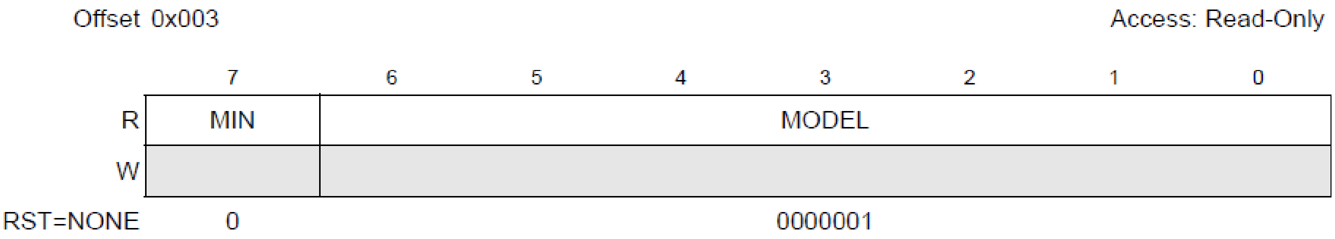
Figure 3-3. QVER Register

Table 3-4. QVER Register Field Descriptions

Bits	Name	Description
7-0	QVER	Qixis version as a decimal value: 1= Version 1 2= Version 2

3.3.4 MODEL

The MODEL register contains information about the software programming model version. The MODEL field is updated if a register or register field is added or updated.



Offset 0x003

Access: Read-Only

	7	6	5	4	3	2	1	0
R	MIN	MODEL						
W								
RST=NONE	0	0000001						

Figure 3-4. MODEL Register

Table 3-5. MODEL Register Field Descriptions

Bits	Name	Description
7	MIN	Programming Model Type: 0= Normal Qixis register set. 1= Minimal Qixis register set (QixMin).
6-0	MODEL	Programming model version: 1= Version 1 2= Version 2

3.3.5 MINOR

The MINOR register contains the minor revision number. Concatenated with the QVER register, it forms the revision information for the QixMin device.

The full revision name is:

```
(qver).(minor)
```

Offset 0x004 Access: Read-Only

	7	6	5	4	3	2	1	0
R	MIN							
W								
RST=NONE	0X01							

Figure 3-5. MINOR Register

Table 3-6. MINOR Register Field Descriptions

Bits	Name	Description
7-0	MIN	The minor revision number, increases on each distribution.

3.4 Control and Status Registers

This block of registers control the operation of Qixis itself (or other operations which do not constitute controlling the board or the DUT, which are managed with BRDCFG/ DUTCFG registers) or monitor the status of various things.

3.4.1 CTL

The CTL register is used to control various aspects of the target system.

Offset 0x005 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	SCANEN	-		XTEST	-		LED	FAIL
RST=CRST	SW_TBSCAN	00		0	00		0	0

Figure 3-6. CTL Register

Table 3-7. CTL Register Field Descriptions

Bits	Name	Description
7	SCANEN	Controls TB_SCAN_EN. X= value to drive.
6-5	-	Reserved.
4	XTEST	This bit directly drives the XTEST signal, typically driving an SMA connector. The function is user-defined.
3-2	-	Reserved.

Table continues on the next page...

Table 3-7. CTL Register Field Descriptions (continued)

Bits	Name	Description
1	LED	Software Diagnostic LED Enable: 0= Diagnostic LEDs operate normally. 1= Software can directly control the M3:M0 monitoring LEDs using the LED register.
0	FAIL	Software Failure Diagnostic LED: 0= FAIL LED is not asserted due to software (it might still be on due to hardware failures). 1= FAIL LED is forced on. Generally, this indicates a software-diagnosed error.

3.4.2 AUX

The AUX register may be used to store system information. The AUX register is initialized to zero when the system is powered-up, and never altered by hardware again.

Offset 0x006 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	AUX							
RST=ARST	00000000							

Figure 3-7. AUX Register

Bits	Name	Description
7-0	AUX	User-defined value.

3.4.3 STAT_SYS

The STAT_SYS register reports general system status.

Offset 0x009 Access: Read-Only

	7	6	5	4	3	2	1	0
R	-			RTIMER	ALTCPU	ALTERED	ASLEEP	-
W								
RST=NONE	000			0	0	0	0	0

Figure 3-8. STAT_SYS Register

Table 3-8. STAT_SYS Register Field Descriptions

Bits	Name	Description
7-5	-	Reserved.
4	RTIMER	Retimer Done Monitor
3	ALTCPU	Alternate CPU Installed: 0= The standard DUT is installed. 1= An alternate, pin-compatible, DUT has been installed.
2	ALTERED	Reconfiguration Active: 0= The system has been configured as normal. 1= The system has been reconfigured by software.
1	ASLEEP	ASLEEP Reporting: 0= At least one core is actively operating. 1= All cores are in sleep mode.
0	-	Reserved.

3.4.4 ALARM

The STAT_ALARM register detects and reports any alarms raised in the QIXIS system.

Write 1 to a STAT_ALARM register bit to prevent Qixis from recognizing that alarm condition. By default, all alarms are handled.

Offset 0x00A

Access: Read-Only

	7	6	5	4	3	2	1	0
R	MON		CTL	VTOFF	ORIENT	VCT	TWARN	TALERT
W								
RST=ARST	00		0	0	0	0	0	0

Figure 3-9. ALARM Register

Table 3-9. ALARM Register Field Descriptions

Bits	Name	Description
7-6	MON	
5	CTL	Software Fault (CTL[FAIL] was set).
4	VTOFF	VCC Power Supply Temp Off Fault 0= The system is powered normally. 1= The system powers off due to over-temperature of the supply monitored by VT (see bit 5).
3	ORIENT	Processor Orientation Fault:

Table continues on the next page...

Table 3-9. ALARM Register Field Descriptions (continued)

Bits	Name	Description
		0= The processor is correctly installed. 1= The processor is installed incorrectly, and the power is turned off forcibly.
2	VCT	VCC/Core Power Supply Temperature Warning: 0= The VCC power supply temperature is within normal limits. 1= The VCC power supply temperature has exceeded warning limits.
1	TWARN	Temperature Fault: 0= The temperature is within normal limits. 1= The temperature has exceeded warning limits. NOTE: This signal is controlled by the ADT7461, and the temperature limits and behavior (latching vs. transient) depend upon software programming.
0	TALERT	Temperature Alert: 0= The temperature is within normal limits. 1= The temperature has exceeded fault limits. NOTE: This signal is controlled by the ADT7461, and the temperature limits and behavior (latching vs. transient) depend upon software programming.

3.4.5 STAT_PRES1

The STAT_PRES1 detects the installation of various devices/cards.

Offset 0x00B

Access: Read-Only

	7	6	5	4	3	2	1	0
R	DUT	-	CPU_ID		TDMR	-	WP	CD
W								
RST=NONE	0	1	11		1	1	1	1

Figure 3-10. STAT_PRES1 Register

Table 3-10. STAT_PRES1 Register Field Descriptions

Bits	Name	Description
7	DUT	Processor Present: 0= A processor is detected (soldered-in or socketed). 1= No device detected.
6	-	Reserved.
5-4	CPU_ID	Processor Installed:

Table continues on the next page...

Table 3-10. STAT_PRES1 Register Field Descriptions (continued)

Bits	Name	Description
		00= An unknown device is installed. 01= An LS1043A is installed. 10= An LS1047A is installed. 11= An LS1088A is installed.
3	TDMR	TDMRiser Card Present: 0= A TDMRiser card is installed in the dedicated slot. 1= No TDMRiser detected.
2	-	Reserved.
1	WP	SD Card write-protect: 0= A write-enabled card is installed in the slot. 1= The card is write-protected, or no card is installed.
0	CD	SD Card Present: 0= A card is detected in the slot. 1= No card detected.

3.4.6 STAT_PRES2

The STAT_PRES2 detects the installation of cards in various PCI Express or SGMII slots.

Offset 0x00C

Access: Read-Only

	7	6	5	4	3	2	1	0
R	-					SLOT3	SLOT2	SLOT1
W								
RST=NONE	11111					1	1	1

Figure 3-11. STAT_PRES2 Register

Table 3-11. STAT_PRES2 Register Field Descriptions

Bits	Name	Description
7-3	-	Reserved.
2	SLOT3	(same as SLOT1)
1	SLOT2	(same as SLOT1)
0	SLOT1	0= a card is installed. 1= no card is installed.

3.4.7 LED

The LED register can be used to directly control the monitoring LEDs (M7-M0) for software debugging and messaging purposes. Direct control of the LEDs is possible only when CTL[LED] is set to 1; otherwise Qixis uses them to display general system activity.

Offset 0x00E Access: Read/Write

	7	6	5	4	3	2	1	0
R W	LED							
RST=GRST	00000000							

Figure 3-12. LED Register

Table 3-12. LED Register Field Descriptions

Bits	Name	Description
7-0	LED	LED Status Control: 0= LED M[bitno] is off. 1= LED M[bitno] is on.

3.5 Reconfiguration Registers

This block of registers controls the operation of the reconfiguration system, which is used to alter the configuration of the board or processor into different voltages, SYSCLK frequencies, boot device selections, or any other configuration controlled by a BRDCFG or DUTCFG register.

It also provides access to the DCM, the Data Collection Manager, which records voltage, current and power for several supplies independent of processor activity.

3.5.1 RCFG

The RCFG_CTL register is used to control the reconfiguration sequencer.

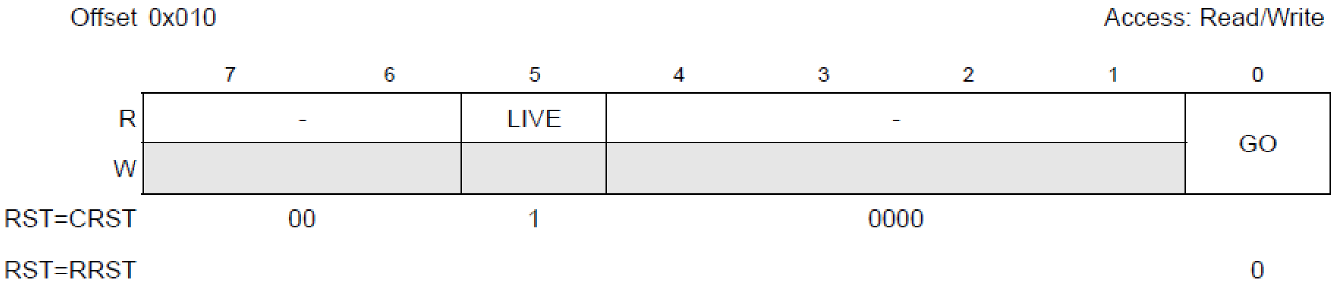

Offset 0x010
Access: Read/Write
7
6
5
4
3
2
1
0
R
-
LIVE
-
GO
W
RST=CRST
00
1
0000
RST=RRST
0

Figure 3-13. RCFG Register

Table 3-13. RCFG Register Field Descriptions

Bits	Name	Description
7-6	-	Reserved.
5	LIVE	Immediate changes for BRDCFG registers: 1= BRDCFG registers outputs occur immediately. For QixMin, LIVE is always 1.
4-1	-	Reserved.
0	GO	Reconfiguration Start: 0= Reconfiguration sequencer is idle. 1= On the 0-to-1 transition, the reconfiguration process begins.

3.5.2 LOS_STAT

The LOS_STAT reports loss of lock for various devices.

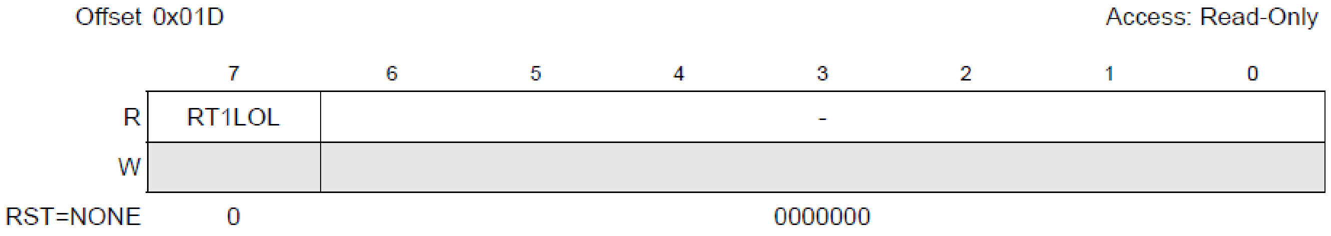

Offset 0x01D
Access: Read-Only
7
6
5
4
3
2
1
0
R
RT1LOL
-
W
RST=NONE
0
0000000

Figure 3-14. LOS_STAT Register

Table 3-14. LOS_STAT Register Field Descriptions

Bits	Name	Description
7	RT1LOL	Retimer #1 (Lane D) Loss: 0= Receive and transmit pathway(s) operating normally 1= Receive or transmit pathway(s) pathway lost sync.
6-0	-	Reserved.

3.6 Power Control/Status Registers

The power registers provide the ability to monitor general power status, as well as individual power status (for those supplies that have reporting capability). Other registers provide limited power control features (most power control is through the PMBus/I2C interface).

3.6.1 PWR_EVENT

The PWR_EVENT records events which cause power changes.

Offset 0x022 Access: Read-Only

	7	6	5	4	3	2	1	0
R	PPEVENT				PEVENT			
W								
RST=NONE	0000				0000			

Figure 3-15. PWR_EVENT Register

Table 3-15. PWR_EVENT Register Field Descriptions

Bits	Name	Description
7-4	PPEVENT	Previous Power Event: This field contains the previous value stored in the PEVENT field.
3-0	PEVENT	Power Event: The field will contain one of the following codes, indicating the event which caused the power change: 0000= None (never powered up). 0001= Forced power-off (fault, temp, etc). 0010= Automatic power-up (SW_AUTO is set). 0011= POWER switch used to power on. 0100= RST_CTL2[PWR] used to power on. 0101= DCM used to power on. 0110= ATX PSU dropped power (external event). 0111= POWER switch used to power off. 1000= RST_CTL2[PWR] used to power off. 1001= DCM used to power off. 1010= Thermal fault forced power off. 1111= Unknown (PSEQ fault).

3.6.2 PWR_MSTAT

The PWR_MSTAT register monitors the overall power status of the board, including that of the ATX (or bench) power supply used to power all other rails.

Offset 0x024 Access: Read-Only

	7	6	5	4	3	2	1	0
R	ATXON	ATXGD	-	FAULT	PWROK	-	SSTATE	
W								
RST=NONE	1	1	0	0	1	0	11	

Figure 3-16. PWR_MSTAT Register

Table 3-16. PWR_MSTAT Register Field Descriptions

Bits	Name	Description
7	ATXON	ATX Power Supply Control Status: 0= Power supply is set to off. 1= Power supply is set to on.
6	ATXGD	ATX Power Supply Status: 0= Power supply is off or not yet stable. 1= Power supply is on and stable.
5	-	Reserved.
4	FAULT	Faulted: 0= Power supply system operating normally. 1= Power supply system was shutdown for some reason. Check the ALARM register for details.
3	PWROK	General Power Status: 0= One or more power supplies are off or not yet stable. 1= All power supplies are on and stable.
2	-	Reserved.
1-0	SSTATE	Reports the current power savings level, for those devices which support it. 11= S3 - completely on Note: If a device does not support hardware (that is, external) power savings modes, S3 is always reported.

3.6.3 PWR_STAT1

The PWR_STATn registers are used to monitor the status of individual power supplies. If a bit is set to '1', the respective power supply is operating correctly.

Note that unassigned bits default to one, allowing power failure detection to be easily performed (if the value is not 0xFF, at least one supply is not operating).

Due to the high variability of the hardware devices used, PWR_STATn register bits are not assigned any universally fixed values. For more details, see the target platform documentation.

Offset 0x025 Access: Read-Only

	7	6	5	4	3	2	1	0
R	-		XVDD	TA_BB	-	V0.85	VPP	VDD
W								
RST=NONE	11		1	1	1	1	1	1

Figure 3-17. PWR_STAT1 Register

Table 3-17. PWR_STAT1 Register Field Descriptions

Bits	Name	Description
7-6	-	Reserved.
5	XVDD	XVDD (SerDes IO Voltage) Monitor.
4	TA_BB	TA_BB Monitor
3	-	Reserved.
2	V0.85	VCC_0.85V Monitor.
1	VPP	DDR4 Interface VPP Monitor
0	VDD	Core Power Monitor

3.6.4 PWR_STAT2

Monitors various power statuses; see PWR_STAT1 for details.

Offset 0x026 Access: Read-Only

	7	6	5	4	3	2	1	0
R	-		VCC1P2	OVDD	-	VCC_2V5	VTT1	GVDD
W								
RST=NONE	11		1	1	1	1	1	1

Figure 3-18. PWR_STAT2 Register

Table 3-18. PWR_STAT2 Register Field Descriptions

Bits	Name	Description
7-6	-	Reserved.
5	VCC1P2	VCC_1.2V Monitor
4	OVDD	OVDD Monitor
3	-	Reserved.
2	VCC_2V5	2V5 Monitor
1	VTT1	DDR termination power #1
0	GVDD	DDR Power.

3.7 Clock Control Registers

The clock control registers control programmable clock synthesizers used to supply clocks to the processor and associated peripherals.

3.7.1 CLK_SPD1

The CLK_SPD1 register is used to report the user-selectable speed settings (typically from switches) for the SYSCLK and DDRCLK clocks.

Values in the CLK_SPD1 register are used by boot software accurately initialize timing-dependent parameters, such as for UART baud rates, I2C clock rates, and DDR memory timing.

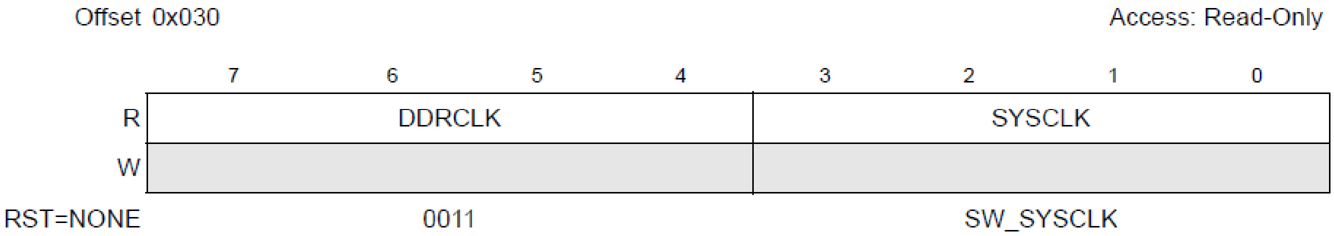


Figure 3-19. CLK_SPD1 Register

Table 3-19. CLK_SPD1 Register Field Descriptions

Bits	Name	Description
7-4	DDRCLK	DDRCLK Rate Selection: 0011= 133.333333 MHz (fixed)
3-0	SYSCLK	SYSCLK Rate Selection: 0000= 66.66 MHz

Table 3-19. CLK_SPD1 Register Field Descriptions

Bits	Name	Description
		0001= 83.33 MHz 0010= 100.00 MHz 0011= 125.00 MHz 0100= 133.33 MHz 0101= 150.00 MHz Other values are Reserved.

3.7.2 CLK_ID

The CLK_ID register is used to identify the arrangement of the clock control registers. Software should check CLK_ID register before attempting to interpret/control the clock control registers.

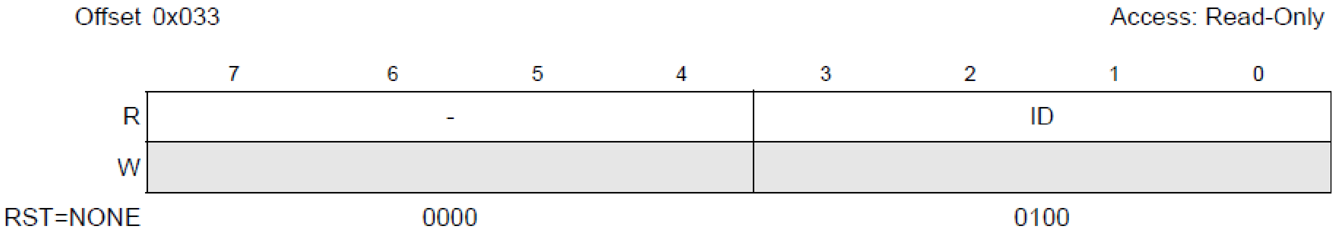


Figure 3-20. CLK_ID Register

Table 3-20. CLK_ID Register Field Descriptions

Bits	Name	Description
7-4	-	Reserved.
3-0	ID	System Clock ID = 0100 (QIXIS-2) CLK0= SYSCLK is provided by an SI5341B synthesizer using CLK_SYSCLKD[0:1]

3.7.3 SYSCLK_D0

Provides the 8 MSBits of the targeted SYSCLK frequency.

Offset 0x034 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	SYS0							
RST=RRST	SW_SYSCLK							

Figure 3-21. SYSCLK_D0 Register

Table 3-21. SYSCLK_D0 Register Field Descriptions

Bits	Name	Description
7-0	SYS0	Sysclk Target Value: On RCFG.GO, SYSCLK will be changed to the value in this register concatenated with SYSCLK_D1[SYS1]. The frequency is a multiple of 0.3333 MHz, so the register is preset with, and programmed to, the value SYSCLK*3. Note: Changes to SYSCLK only take effect on the next restart (via RCFG.GO).

3.7.4 SYSCLK_D1

Provides the 2 LSBits of the targeted SYSCLK frequency.

Offset 0x035 Access: Read/Write

	7	6	5	4	3	2	1	0
R	SYS1		-				FDEC	FINC
W								
RST=RRST	SW_SYSCLK		0000				0	0

Figure 3-22. SYSCLK_D1 Register

Table 3-22. SYSCLK_D1 Register Field Descriptions

Bits	Name	Description
7-6	SYS1	Sysclk Target Value: On RCFG.GO, SYSCLK will be changed to the value in this register prepended with SYSCLK_D0[SYS0]. The frequency is a multiple of 0.3333 MHz, so the register is preset with, and programmed to, the value SYSCLK*3. Note: Changes to SYSCLK only take effect on the next restart (via RCFG.GO).
5-2	-	Reserved.
1	FDEC	Frequency Decrement: Drives the Si5341 FDEC input directly. On the 0-to-1 transition, the Si5341 will decrement SYSCLK by 0.333 MHz.

Table continues on the next page...

Table 3-22. SYSCLK_D1 Register Field Descriptions (continued)

Bits	Name	Description
		Note: This change to SYSCLK is immediate. There is no guarantee the processor PLL will maintain PLL lock if SYSCLK changes too much.
0	FINC	Frequency Increment: Drives the Si5341 FINC input directly. On the 0-to-1 transition, the Si5341 will increment SYSCLK by 0.333 MHz. Note: This change to SYSCLK is immediate. There is no guarantee the processor PLL will maintain PLL lock if SYSCLK changes too much.

3.8 Reset Control Registers

The reset control register group handles reset behavior configuration and general monitoring of resets.

3.8.1 RST_CTL

The RST_CTL register is used configure or trigger reset actions.

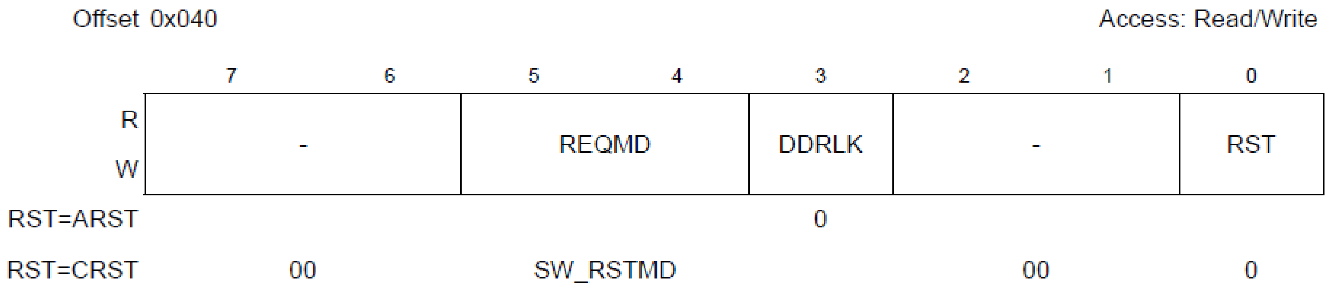


Figure 3-23. RST_CTL Register

Table 3-23. RST_CTL Register Field Descriptions

Bits	Name	Description
7-6	-	Reserved.
5-4	REQMD	00= Disabled - do nothing. 11= Normal - assert PORESET_B to DUT to begin normal reset sequence.
3	DDRLK	DDR Reset Lock: 0= Reset is asserted to the DDR DIMMs/devices normally. 1= Reset will not be asserted to the DDR DIMMs/devices. With proper DDR controller setup and careful software setup DDR contents can survive resets.

Table continues on the next page...

Table 3-23. RST_CTL Register Field Descriptions (continued)

Bits	Name	Description
		This bit is not cleared with a general reset, but is preserved, as long as power is available. It is expected that software that sets this bit is also responsible for clearing it.
2-1	-	Reserved.
0	RST	Reset: 0= Reset sequencer operates normally. 1= Upon transition from 0 to 1, restart the reset sequence.

3.8.2 RST_STAT

The RST_STAT register reports the current status of various reset-related signals.

Offset 0x041

Access: Read-Only

	7	6	5	4	3	2	1	0
R	WAIT	SYSRST	-			HRST	PORST	RREQ
W								
RST=NONE	0	0	000			0	0	0

Figure 3-24. RST_STAT Register

Table 3-24. RST_STAT Register Field Descriptions

Bits	Name	Description
7	WAIT	Reset Waiting: 0= Reset sequencer is operating normally. 1= Reset sequencer is in RMT-WAIT state, waiting for permission to proceed.
6	SYSRST	System Reset: 0= System is operating normally. 1= System is in reset.
5-3	-	Reserved.
2	HRST	HRESET_B status: 0= HRESET_B is not asserted. 1= HRESET_B is asserted.
1	PORST	PORESET_B status: 0= PORESET_B is not asserted. 1= PORESET_B is asserted.
0	RREQ	RESET_REQ_B status:

Table 3-24. RST_STAT Register Field Descriptions

Bits	Name	Description
		0= RESET_REQ_B is not asserted. 1= RESET_REQ_B is asserted.

3.8.3 RST_REASON

The RST_REASON register is used to report the cause of the most-recent reset cycle.

Offset 0x042

Access: Read-Only

	7	6	5	4	3	2	1	0
R	PREV				REASON			
W								
RST=NONE	1111				0000			

Figure 3-25. RST_REASON Register

Table 3-25. RST_REASON Register Field Descriptions

Bits	Name	Description
7-4	PREV	Previous reset reason: See REASON field codes.
3-0	REASON	Reset Reason: 0000= Power-on reset 0001= COP/JTAG HRESET_B was asserted 0010= (reserved) 0011= RST_CTL[RST] was set 0100= Reset switch (chassis or on-board) was pushed. 0101= RCFG_CTL[GO] (that is, reconfiguration reset) was asserted. 0110= RESET_REQ_B assertion (from processor) was asserted. 1111= No event recorded yet.

3.8.4 RST_FORCE1

The RST_FORCEn registers are used to force reset to a particular device, independent of the general reset sequencer. As long as a bit is set to 1, the reset signal to grouped devices will be asserted.

Due to the high variability of hardware devices used, RST_FORCEn registers do not have a universally-defined purpose. Consult the target platform documentation for details; a table of customary assignments is shown below, but keep in mind it is only a reference.

Offset 0x043 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	-		QSPI	I2C	EPHY3	EPHY2	EPHY1	MEM
RST=GRST	00		0	0	0	0	0	0

Figure 3-26. RST_FORCE1 Register

Table 3-26. RST_FORCE1 Register Field Descriptions

Bits	Name	Description
7-6	-	Reserved.
5	QSPI	1= Assert RST_QSPI_B.
4	I2C	1= Assert RST_I2C_B.
3	EPHY3	1= Assert RST_EPHY3_B
2	EPHY2	1= Assert RST_EPHY2_B
1	EPHY1	1= Assert RST_EPHY1_B
0	MEM	Reset all DDR slots. 1= Assert RST_MEM_B (RST_MEM_DRV_B translated to DDR voltage level).

3.8.5 RST_FORCE2

Assert selected reset sources. See RST_FORCE1 for details.

Offset 0x044 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	IEEE	RTIME	CLK	TDM	EMMC	TRST	HRST	PORST
RST=GRST	0	0	0	0	0	0	0	0

Figure 3-27. RST_FORCE2 Register

Table 3-27. RST_FORCE2 Register Field Descriptions

Bits	Name	Description
7	IEEE	1= Assert RST_IEEE_B / RST_1588_B for IEEE-1588 test cards.
6	RTIME	1= Assert RST_RETIMER_B
5	CLK	1= Assert RST_CLK.
4	TDM	1= Assert RST_TDMRISER_B.
3	EMMC	1= Assert RST_EMMC_B.
2	TRST	1= Assert DUT_TRST_B.
1	HRST	1= Assert DUT_HRESET_B. NOTE: This bit only asserts the signal to the DUT; it is not intended to be used as a general system reset.
0	PORST	1= Assert DUT_PORESET_B. NOTE: This bit only asserts the signal to the DUT; it is not intended to be used as a general system reset.

3.8.6 RST_FORCE3

Assert selected reset sources. See RST_FORCE1 for details.

Offset 0x045

Access: Read/Write

	7	6	5	4	3	2	1	0
R W	SLOT1	SLOT2	SLOT3	-				
RST=GRST	0	0	0	00000				

Figure 3-28. RST_FORCE3 Register

Table 3-28. RST_FORCE3 Register Field Descriptions

Bits	Name	Description
7	SLOT1	1= Assert RST_SLOT1_B.
6	SLOT2	1= Assert RST_SLOT2_B.
5	SLOT3	1= Assert RST_SLOT3_B.
4-0	-	Reserved.

3.8.7 RST_MASK1

The RST_MASKn registers are used to block reset to a particular device, independent of the general reset sequencer. As long as a bit is set to 1, the reset signal to that device or devices will be blocked.

RST_MASKn bits have the same bit definition as their counterparts in RST_FORCEn.

Note that RST_MASK bits are cleared on AUX reset, and so are usually only cleared by software. This is very different from the RST_FORCE registers.

Offset 0x04B

Access: Read/Write

	7	6	5	4	3	2	1	0
R W	-		QSPI	I2C	EPHY3	EPHY2	EPHY1	MEM
RST=ARST	00		0	0	0	0	0	0

Figure 3-29. RST_MASK1 Register

Table 3-29. RST_MASK1 Register Field Descriptions

Bits	Name	Description
7-6	-	Reserved.
5	QSPI	1= Mast RST_QSPI_B.
4	I2C	1= Mask RST_I2C_B.
3	EPHY3	1= Mask RST_EPHY3_B
2	EPHY2	1= Mask RST_EPHY3_B
1	EPHY1	1= Mask RST_EPHY1_B
0	MEM	1= Mask RST_MEM_B (DDR slots, etc.)

3.8.8 RST_MASK2

Mask selected reset sources. See RST_FORCE1 for details.

Offset 0x04C

Access: Read/Write

	7	6	5	4	3	2	1	0
R W	IEEE	RTIME	CLK	TDM	EMMC	-	HRST	PORST
RST=ARST	0	0	0	0	0	0	0	0

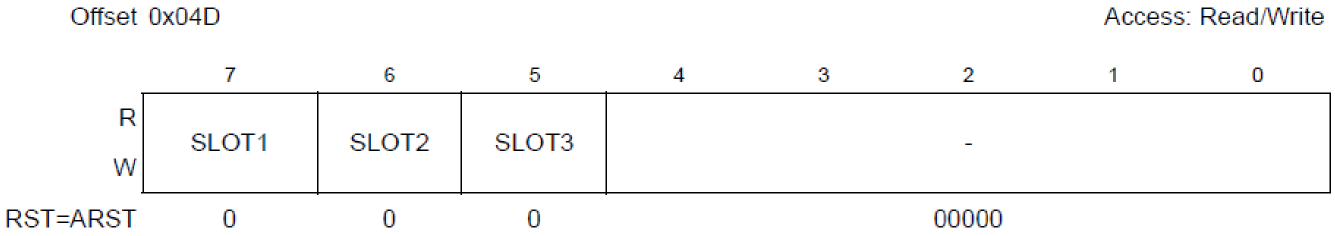
Figure 3-30. RST_MASK2 Register

Table 3-30. RST_MASK2 Register Field Descriptions

Bits	Name	Description
7	IEEE	1= Mask RST_IEEE_B.
6	RTIME	1= Mask RST_RTIMER_B.
5	CLK	1= Mask RST_CLK.
4	TDM	1= Mask RST_TDMRISER_B.
3	EMMC	1= Mask RST_EMMC_B.
2	-	Reserved.
1	HRST	1= Mask DUT_HRESET_B.
0	PORST	1= Mask DUT_PORESET_B.

3.8.9 RST_MASK3

Mask selected reset sources. See RST_FORCE1 for details.



Offset 0x04D

Access: Read/Write

	7	6	5	4	3	2	1	0
R W	SLOT1	SLOT2	SLOT3	-				
RST=ARST	0	0	0	00000				

Figure 3-31. RST_MASK3 Register

Table 3-31. RST_MASK3 Register Field Descriptions

Bits	Name	Description
7	SLOT1	1= Mask RST_SLOT1_B.
6	SLOT2	1= Mask RST_SLOT2_B.
5	SLOT3	1= Mask RST_SLOT3_B.
4-0	-	Reserved.

3.9 Board Configuration Registers

This block of registers control the configuration of the board. BRDCFG registers are always static, driven at all times power is available. There are up to 16 registers providing up to 128 control options; however, not every platform implements all the registers.

3.9.1 BRDCFG0

The BRDCFG0 register is commonly used to select IFC and QSPI boot devices.

Offset 0x050 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	QMAP			-				
RST=RRST	SW_QMAP			00000				

Figure 3-32. BRDCFG0 Register

Table 3-32. BRDCFG0 Register Field Descriptions

Bits	Name	Description
7-5	QMAP	QMAP controls hows QSPI_A chip-selects are connected to various peripherals. QSPI_CSA_0 QSPI_CSA_1 ========== ========== 000= DEV #0 DEV #1 001= DEV #1 DEV #0 010= EMU DEV #0 011= EMU DEV #1 100= DEV #0 EMU
4-0	-	Reserved

3.9.2 BRDCFG1

The BRDCFG1 register shows/controls SYSCLK and DDRCLK speeds.

Offset 0x051 Access: Read-Only

	7	6	5	4	3	2	1	0
R	-		DDRCLK		SYSCLK			
W								
RST=RRST	00		01		0010			

Figure 3-33. BRDCFG1 Register

Table 3-33. BRDCFG1 Register Field Descriptions

Bits	Name	Description
7-6	-	Reserved.
5-4	DDRCLK	DDRCLK Frequency Selection: 10= 100.000000 MHz (fixed)
3-0	SYSCLK	SYSCLK Frequency Selection: 0010= 100.000000 MHz (fixed)

3.9.3 BRDCFG2

The BRDCFG2 register controls SerDes clock speeds for all SerDes blocks.

Offset 0x052

Access: Read-Only

	7	6	5	4	3	2	1	0
R	SD1CK1		SD1CK2		SD2CK1		SD2CK2	
W								
RST=RRST	00		10		SW_SPREAD		SW_SPREAD	

Figure 3-34. BRDCFG2 Register

Table 3-34. BRDCFG2 Register Field Descriptions

Bits	Name	Description
7-6	SD1CK1	SerDes1 Clock #1 Rate: 00= 100.000 MHz
5-4	SD1CK2	SerDes1 Clock #2 Rate: 10= 156.250 MHz (fixed)
3-2	SD2CK1	SerDes2 Clock #1 Rate: 00= 100.000 MHz (fixed, SW_SPREAD=0) 11= 100.000 MHz (spread-spectrum enabled, SW_SPREAD=1)
1-0	SD2CK2	SerDes2 Clock #2 Rate: 00= 100.000 MHz (fixed, SW_SPREAD=0) 11= 100.000 MHz (spread-spectrum enabled, SW_SPREAD=1)

3.9.4 BRDCFG4

BRDCFG4 controls EMI routing as well as other target-dependent resources.

Offset 0x054 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	-			TABBVSEL	SVDDVSEL	PEXSS	-	
RST=RRST	000			1	1	SW_SPREAD_EN	00	

Figure 3-35. BRDCFG4 Register

Table 3-35. BRDCFG4 Register Field Descriptions

Bits	Name	Description
7-5	-	Reserved.
4	TABBVSEL	TA_BB Voltage Selection: 0= 0.9V 1= 1.0V (default) NOTE: If VDD is changed via PMBus, TABBVSEL must be changed as well to track VDD as close as possible. Valid for Rev B boards or later only.
3	SVDDVSEL	SVDD Voltage Selection: 0= 0.9V 1= 1.0V
2	PEXSS	PCI Express Spread-Spectrum Enable: Controls the net labelled CFG_PEXSS or CFG_SPREAD_EN. 0= Disabled. 1= Enabled for SERDES3 and SERDES4.
1-0		Reserved

3.9.5 BRDCFG5

BRDCFG5 controls target-dependent resources.

Offset 0x055 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	I2C2	I2C3	-	IEEECLK	SPISDHC		-	EVDDF
RST=RRST	0	0	0	0	00		0	0

Figure 3-36. BRDCFG5 Register

Table 3-36. BRDCFG5 Register Field Descriptions

Bits	Name	Description
7	I2C2	Controls I2C2 routing: 0= I2C2 connect to CPLD for SDHC_CD_B/SDHC_WP signals. 1= I2C2 connect to TDM Riser for CLK09/CLK10 signals.
6	I2C3	Controls I2C3 routing: 0= I2C3 connect to USB2 for USB2_DRVBUS/USB2_PWRFAULT signals. 1= I2C3 connect to TDM Riser for CLK11/CLK12 signals.
5	-	Reserved.
4	IEEECLK	Controls where the processor receives EC clocks: 0= On-board 125 MHz reference. 1= Via IEEE-1588 header.
3-2	SPISDHC	Controls the SPI and SDHC signal routing: 10= Force SDHC Mode • SPI_CS[0] is routed to CPLD for SDHC_VS use. • SPI_CS[1] is unused. • SPI_CS[2:3] are routed to the TDMRiser slot. 11= Force eMMC Mode • SPI_CS[0:3] are routed to the eMMC card. 0X= Auto Mode • If SDHC_CS_B=0 (SDHC card installed): Use SDHC mode described above. • Else SDHC_CS_B=1 (no SDHC card installed): Use eMMC mode described above.
1	-	Reserved
0	EVDDF	EVDD Force. 0= EVDD operates normally: tracking SD Card vs. eMMC use. 1= EVDD is forced to 1.8V always.

3.9.6 BRDCFG9

BRDCFG9 controls target-dependent resources.

Offset 0x059

Access: Read/Write

	7	6	5	4	3	2	1	0
R W	-			SFP_TX	-			
RST=RRST	000			X	0000			

Figure 3-37. BRDCFG9 Register

Table 3-37. BRDCFG9 Register Field Descriptions

Bits	Name	Description
7-5	-	Reserved.
4	SFP_TX	Enables transmit of an SFP module by controlling the TX_DISABLE pin (net nSFP_TX_EN). 0= SFP transmit enabled. 1= SFP transmit disabled. The default value is based on the SerDes protocol selected.
3-0	-	Reserved

3.10 DUT Configuration Registers

This block of 16 registers control the configuration of the DUT (Device Under Test). DUTCFG registers, unlike BRDCFG registers, are not always static. They are driven low only during the reset configuration sampling interval (PORESET_B assertion), and remain tri-stated thereafter; however, there are occasionally some DUT configuration signals that are static. For example, TEST_SEL/TEST_SEL_B.

3.10.1 DUTCFG0

The DUTCFG0 register is used to control fixed DUT configurations, in particular the RCW location setting (cfg_rcw_src).

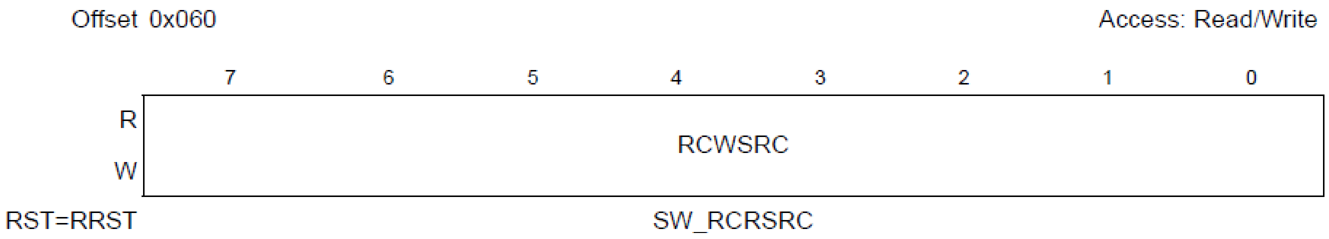


Figure 3-38. DUTCFG0 Register

Table 3-38. DUTCFG0 Register Field Descriptions

Bits	Name	Description
7-0	RCWSRC	RCW Source Location: The 8 most-significant bits of the RCW location configuration (cfg_rcw_src[8:1]).

3.10.2 DUTCFG1

DUTCFG1 manages additional cfg_rcw_src bits and DRAM type (if supported).

Offset 0x061 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	DRAM	-		TE	-			RSRC8
RST=RRST	SW_DRAM	11		1	111			1

Figure 3-39. DUTCFG1 Register

Table 3-39. DUTCFG1 Register Field Descriptions

Bits	Name	Description
7	DRAM	DRAM Type: 0 = DDR4 (LS1043A only). 1 = DDR4 (LS1088A only). NOTE: Only DDR4 is supported, but the configuration value varies depending on the device.
6-5	-	Reserved.
4	TE	IFC Transceiver Enable: Controls cfg_te.
3-1	-	Reserved.
0	RSRC8	RCW Source Location (additional): Controls cfg_rcw_src[0] (the LSB of the 9-bit value).

3.10.3 DUTCFG2

DUTCFG2 manages device selection (SVR) and internal-only device test features.

Offset 0x062 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	-					SVR01		TEST
RST=RRST	11111					SW_SVR		1

Figure 3-40. DUTCFG2 Register

Table 3-40. DUTCFG2 Register Field Descriptions

Bits	Name	Description
7-3	-	Reserved.
2-1	SVR01	Controls cfg_svr[0:1] (note the bit order).
0	TEST	Controls processor pin TESTSEL_B'.' NOTE: Unlike all other DUTCFG bits, this one is static (always driven).

3.10.4 DUTCFG6

The DUTCFG6 register is used to sample device-specific configuration modes.

Offset 0x066 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	RSPDS	-						SOC
RST=RRST	1	111111						1

Figure 3-41. DUTCFG6 Register

Table 3-41. DUTCFG6 Register Field Descriptions

Bits	Name	Description
7	RSPDS	Reset Sequencer Pause Disable: Configures cfg_rsp_dis: 0 : Reset Sequencer Pause 1 : Reset Sequencer Normal
6-1	-	Reserved.
0	SOC	Controls cfg_soc_use: 0 : (system-dependent) 1 : (system-dependent)

3.10.5 DUTCFG11

The DUTCFG11 register is used to control the CFG_ENGUSE[7:0] signals. The function of these bits are defined by Freescale engineers for special use.

Offset 0x06B

Access: Read/Write

	7	6	5	4	3	2	1	0
R W	ENGUSE0	ENGUSE1	ENGUSE2	-				
RST=RRST	SW_ENG0	SW_ENG1	SW_ENG2	11111				

Figure 3-42. DUTCFG11 Register

Table 3-42. DUTCFG11 Register Field Descriptions

Bits	Name	Description
7	ENGUSE0	Differential Clock Mode (cfg_enguse0): 0= Processor uses differential SYSCLK_P/SYSCLK_N input. 1= Processor uses single-ended SYSCLK input.
6	ENGUSE1	Reserved (cfg_enguse1): 1= Default value for unassigned pins.
5	ENGUSE2	Reserved (cfg_enguse2): 1= Default value for unassigned pins.
4-0	-	Reserved.

3.10.6 DUTCFG12

The DUTCFG12 register is used to control the general-purpose GPCFG signals.

These configurations are used exclusively by end customers for their own purposes.

Offset 0x06C

Access: Read/Write

	7	6	5	4	3	2	1	0
R W	GCA							
RST=RRST	11111111							

Figure 3-43. DUTCFG12 Register

Table 3-43. DUTCFG12 Register Field Descriptions

Bits	Name	Description
7-0	GCA	General Purpose Configuration Controls: GCA drives cfg_gpin[7:0]. No hardware definition, software determined meanings.

3.11 Core Management Space Registers

The core management address/data registers allow access to internal Qixis control registers, most of which are undocumented. The primary user-visible purpose of the CMS_A/CMS_D registers is to allow direct access to the DIP switch settings, for board configuration reporting.

3.11.1 CMSA

The CMSA register selects one of the internal core management registers within Qixis for subsequent read- or write-access via the CMSD register.

For RDB systems, only the switch-access registers are defined.

Offset 0x0D8

Access: Read/Write

	7	6	5	4	3	2	1	0
R W	ADDR							
RST=ARST	00000000							

Figure 3-44. CMSA Register

Table 3-44. CMSA Register Field Descriptions

Bits	Name	Description
7-0	ADDR	Select internal CMS register for read/write via CMS_D, one of: 0x00-0x0F : SW# : Number of switches the system has. 0x01-0x0F : SW[1:n] : Image of SW1..SWn Ranges not listed are reserved.

A standard use of the CMSA/CMSD port is to read the state of configuration switches, as follows:

```
Qixis_Set_Reg( CMS_A, 0x00 );
nr = Qixis_Get_Reg( CMS_D );
for (i = 1; i <= nr; i++) {
Qixis_Set_Reg( CMS_A, i );
printf("SW%1d = %02X n", i, Qixis_Get_Reg( CMS_D ));
}
```

3.11.2 CMSD

CMSD contains the value of a CMS register selected by CMSA. See CMSA for details.

Offset 0x0D9 Access: Read/Write

	7	6	5	4	3	2	1	0
R W	DATA							
RST=ARST	00000000							

Figure 3-45. CMSD Register

Table 3-45. CMSD Register Field Descriptions

Bits	Name	Description
7-0	DATA	Read/write internal CMS registers selected with CMS_A.

Appendix A
Revision history

The table below summarizes revisions to this document.

Table A-1. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 0	11/2016		Initial public release

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