



# MC33883

## H-Bridge Gate Driver IC

Rev. 11.0 — 27 April 2020

Data sheet: technical data

## 1 General description

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The 33883 is an H-bridge gate driver (also known as a full-bridge pre-driver) IC with integrated charge pump and independent high and low side gate driver channels. The gate driver channels are independently controlled by four separate input pins, thus allowing the device to be optionally configured as two independent high side gate drivers and two independent low side gate drivers. The low side channels are referenced to ground. The high side channels are floating.

The gate driver outputs can source and sink up to 1.0 A peak current pulses, permitting large gate-charge MOSFETs to be driven and/or high pulse-width modulation (PWM) frequencies to be utilized. A linear regulator is incorporated, providing a 15 V typical gate supply to the low side gate drivers. The 33883 is AEC-Q100 qualified.

This device powered by SMARTMOS technology.

## 2 Features

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- $V_{CC}$  operating voltage range from 5.5 V up to 55 V
- $V_{CC2}$  operating voltage range from 5.5 V up to 28 V
- CMOS / LSTTL compatible I / O
- 1.0 A peak gate driver current
- Built-in high side charge pump
- Under-voltage lockout (UVLO)
- Over-voltage lockout (OVLO)
- Global enable with  $<10 \mu\text{A}$  Sleep mode
- Supports PWM up to 100 kHz
- Qualified in compliance with AEC-Q100



### 3 Simplified application diagram

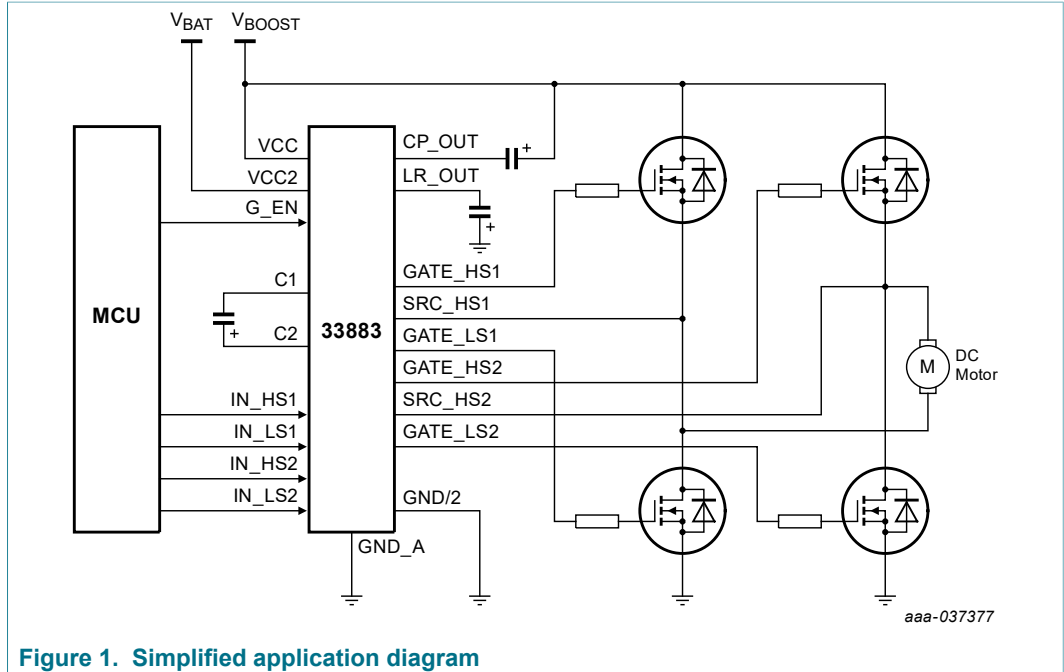


Figure 1. Simplified application diagram

### 4 Applications

- Automotive: 12 V to high-voltage battery packs
- E-bikes, e-scooters
- Energy Storage Systems (ESS)
- Uninterruptible Power Supply (UPS)
- Battery junction box

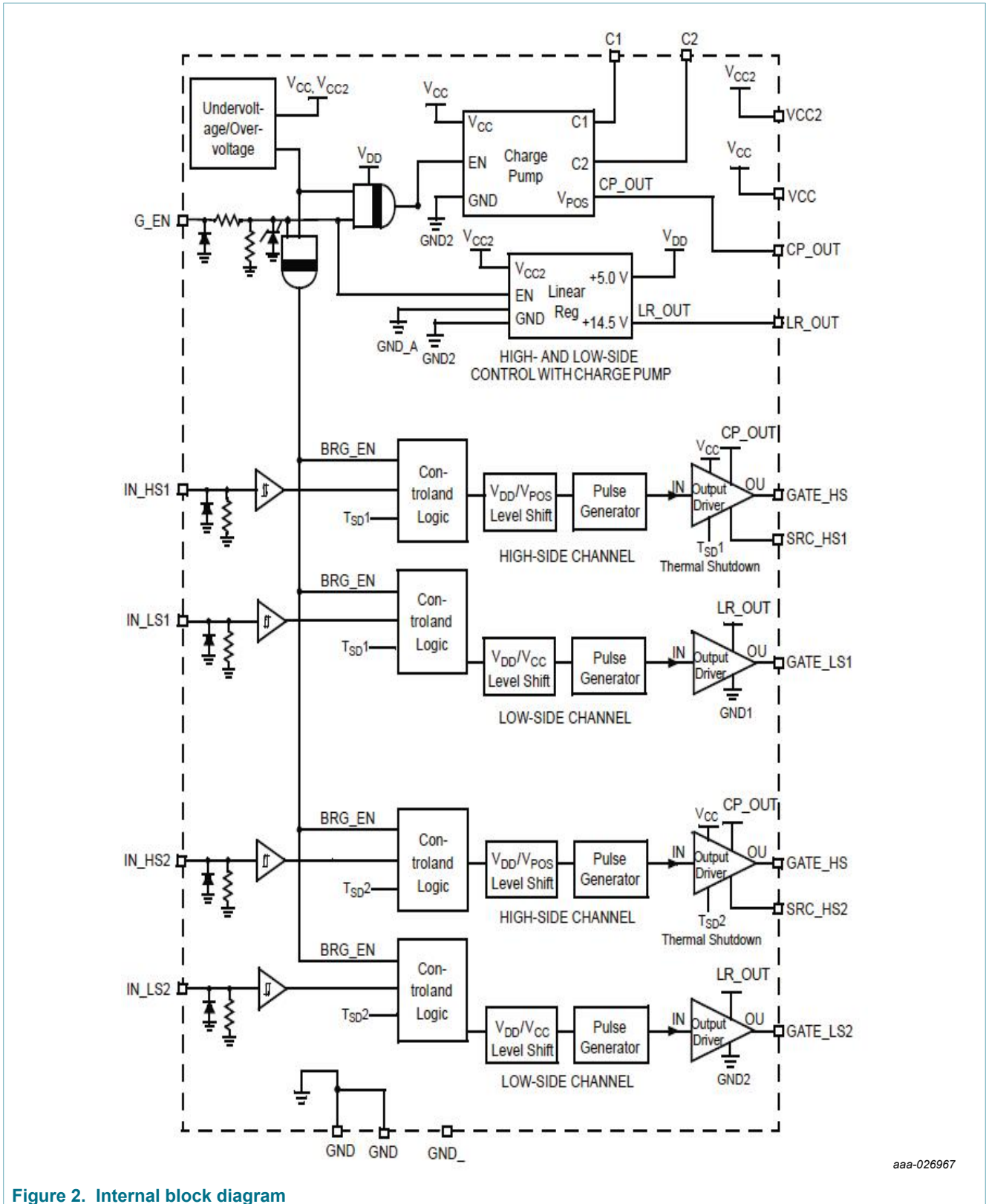
### 5 Ordering information

Table 1. Orderable part variations

Part number <sup>[1]</sup>	VDD	Temperature (T <sub>J</sub> )	Package
MC33883HEG	5.5 to 55 V	-40 °C to 125 °C	20-pin 20 SOICW, 1.27 mm pitch

[1] To order parts in tape and reel, add the R2 suffix to the part number.

6 Internal block diagram



aaa-026967

Figure 2. Internal block diagram

## 7 Pinning information

### 7.1 Pinout diagram

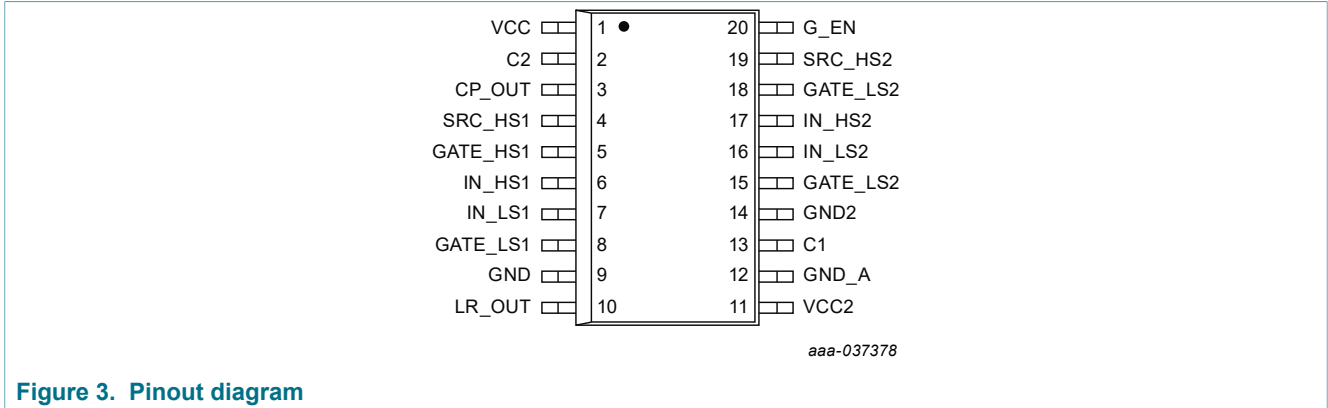


Figure 3. Pinout diagram

### 7.2 Pin definitions

For a detailed description of each pin, see [Section 9 "Functional description"](#).

Table 2. Pin definitions

Pin number	Pin name	Pin function	Definition
1	VCC	Supply Voltage 1	Device power supply 1.
2	C2	Charge Pump Capacitor	External capacitor for internal charge pump.
3	CP_OUT	Charge Pump Out	External reservoir capacitor for internal charge pump.
4	SRC_HS1	Source 1 Output High Side	Source of high-side 1 MOSFET
5	GATE_HS 1	Gate 1 Output High Side	Gate of high-side 1 MOSFET.
6	IN_HS1	Input High Side 1	Logic input control of high-side 1 gate (i.e., IN_HS1 logic HIGH = GATE_HS1 HIGH).
7	IN_LS1	Input Low Side 1	Logic input control of low-side 1 gate (i.e., IN_LS1 logic HIGH = GATE_LS1 HIGH).
8	GATE_LS1	Gate 1 Output Low Side	Gate of low-side 1 MOSFET.
9	GND1	Ground 1	Device ground 1.
10	LR_OUT	Linear Regulator Output	Output of internal linear regulator.
11	VCC2	Supply Voltage 2	Device power supply 2.
12	GND_A	Analog Ground	Device analog ground.
13	C1	Charge Pump Capacitor	External capacitor for internal charge pump.
14	GND2	Ground 2	Device ground 2.
15	GATE_LS2	Gate 2 Output Low Side	Gate of low-side 2 MOSFET.
16	IN_LS2	Input Low Side 2	Logic input control of low-side 2 gate (i.e., IN_LS2 logic HIGH = GATE_LS2 HIGH).
17	IN_HS2	Input High Side 2	Logic input control of high-side 2 gate (i.e., IN_HS2 logic HIGH = GATE_HS2 HIGH).
18	GATE_HS 2	Gate 2 Output High Side	Gate of high-side 2 MOSFET.
19	SRC_HS2	Source 2 Output High Side	Source of high-side 2 MOSFET.

Pin number	Pin name	Pin function	Definition
20	G_EN	Global Enable	Logic input Enable control of device (i.e., G_EN logic HIGH = Full Operation, G_EN logic LOW = Sleep Mode).

## 8 General product characteristics

### 8.1 Maximum ratings

**Table 3. Maximum ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings might cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Supply Voltage 1	$V_{CC}$	-0.3 to 65	V
Supply Voltage 2 (1)	$V_{CC2}$	<sup>[1]</sup> -0.3 to 35	V
Linear Regulator Output Voltage	$V_{LR\_OUT}$	-0.3 to 18	V
High-Side Floating Supply Absolute Voltage	$V_{CP\_OUT}$	-0.3 to 65	V
High-Side Floating Source Voltage	$V_{SRC\_HS}$	-2.0 to 65	V
High-Side Source Current from CP_OUT in Switch ON State	$I_S$	250	mA
High-Side Gate Voltage	$V_{GATE\_HS}$	-0.3 to 65	V
High-Side Gate Source Voltage (2)	$V_{GATE\_HS} - V_{SRC\_HS}$	<sup>[2]</sup> -0.3 to 20	V
High-Side Floating Supply Gate Voltage	$V_{CP\_OUT} - V_{GATE\_HS}$	-0.3 to 65	V
Low-Side Gate Voltage	$V_{GATE\_LS}$	-0.3 to 17	V
Wake-Up Voltage	$V_{G\_EN}$	-0.3 to 35	V
Logic Input Voltage	$V_{IN}$	-0.3 to 10	V
Charge Pump Capacitor Voltage	$V_{C1}$	-0.3 to $V_{LR\_OUT}$	V
Charge Pump Capacitor Voltage	$V_{C2}$	-0.3 to 65	V
ESD Voltage		<sup>[3]</sup>	V
Human Body Model on All Pins (VCC and VCC2 as Two Power Supplies)	$V_{ESD1}$	±1500	
Machine Model	$V_{ESD2}$	±130	

[1]  $V_{CC2}$  can sustain load dump pulse of 40 V, 400 ms, 2.0 Ω.

[2] In case of high current ( $SRC\_HS > 100$  mA) and high voltage (>20 V) between GATE\_HSX and SRC\_HS an external zener of 18 V is needed as shown in Figure 14.

[3] ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP} = 100$  pF,  $R_{ZAP} = 1500$  Ω), ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP} = 200$  pF,  $R_{ZAP} = 0$  Ω).

### 8.2 Static electrical characteristics

**Table 4. Static electrical characteristics**

Characteristics noted under conditions  $V_{CC} = 12$  V,  $V_{CC2} = 12$  V,  $C_{CP} = 33$  nF,  $G\_EN = 4.5$  V unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^\circ\text{C}$  under nominal conditions unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
<b>Operating conditions</b>					
$V_{CC}$	Supply Voltage 1 for Output High-Side Driver and Charge Pump	5.5	—	55	V
$V_{CC2}$	Supply Voltage 2 for Linear Regulation	5.5	—	28	V

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CP_OUT</sub>	High-Side Floating Supply Absolute Voltage	V <sub>CC</sub> + 4	—	V <sub>CC</sub> + 11 but < 65	V
<b>Logic</b>					
V <sub>IH</sub>	Logic 1 Input Voltage (IN_LS and IN_HS)	2.0	—	10	V
V <sub>IL</sub>	Logic 0 Input Voltage (IN_LS and IN_HS)	—	—	0.8	V
I <sub>N+</sub>	Logic 1 Input Current V <sub>IN</sub> = 5.0 V	200	—	1000	μA
V <sub>G_EN</sub>	Wake-Up Input Voltage (G_EN)	4.5	5.0	V <sub>CC2</sub>	V
I <sub>G_EN</sub>	Wake-Up Input Current (G_EN) V <sub>G_EN</sub> = 14 V	—	200	500	μA
I <sub>G_EN2</sub>	Wake-Up Input Current (G_EN) V <sub>G_EN</sub> = 28 V	—	—	1.5	mA
<b>Linear regulator</b>					
V <sub>LR_OUT</sub>	Linear regulator V <sub>LR_OUT</sub> @ V <sub>CC2</sub> from 15 V to 28 V, I <sub>LOAD</sub> from 0 mA to 20 mA V <sub>LR_OUT</sub> @ I <sub>LOAD</sub> = 20 mA V <sub>LR_OUT</sub> @ I <sub>LOAD</sub> = 20 mA, V <sub>CC2</sub> = 5.5 V, V <sub>CC</sub> = 5.5 V	12.5 V <sub>CC2</sub> - 1.5 4.0	— — —	16.5 — —	V
<b>Charge pump</b>					
V <sub>CP_OUT</sub>	Charge Pump Output Voltage, Reference to VCC VCC = 12 V, ILOAD = 0 mA, CCP_OUT = 1.0 μF VCC = 12 V, ILOAD = 7.0 mA, CCP_OUT = 1.0 μF VCC2 = VCC = 5.5 V, ILOAD = 0 mA, CCP_OUT = 1.0 μF VCC2 = VCC = 5.5 V, ILOAD = 7.0 mA, CCP_OUT = 1.0 μF VCC = 55 V, ILOAD = 0 mA, CCP_OUT = 1.0 μF VCC = 55 V, ILOAD = 7.0 mA, CCP_OUT = 1.0 μF	7.5 7.0 2.3 1.8 7.5 7.0	— — — — — —	— — — — — —	V
I <sub>C1</sub>	Peak Current Through Pin C1 Under Rapidly Changing VCC Voltages (see <a href="#">Figure 13</a> )	-2.0	—	2.0	A
V <sub>C1MIN</sub>	Minimum Peak Voltage at Pin C1 Under Rapidly Changing VCC Voltages (see <a href="#">Figure 13</a> )	-1.5	—	—	V
<b>Supply voltage</b>					
I <sub>VCCSLEEP</sub>	Quiescent VCC Supply Current V <sub>G_EN</sub> = 0 V and V <sub>CC</sub> = 55 V V <sub>G_EN</sub> = 0 V and V <sub>CC</sub> = 12 V	— —	— —	10 10	μA
I <sub>VCCOP</sub>	Operating VCC Supply Current <sup>[1]</sup> V <sub>CC</sub> = 55 V and V <sub>CC2</sub> = 28 V V <sub>CC</sub> = 12 V and V <sub>CC2</sub> = 12 V	— —	2.2 0.7	— —	mA
I <sub>VCCLOG</sub>	Additional Operating VCC Supply Current for Each Logic Input Pin Active <sup>[2]</sup> V <sub>CC</sub> = 55 V and V <sub>CC2</sub> = 28 V	—	—	5.0	mA
I <sub>VCC2SLEEP</sub>	Quiescent VCC2 Supply Current V <sub>G_EN</sub> = 0 V and V <sub>CC</sub> = 12 V V <sub>G_EN</sub> = 0 V and V <sub>CC</sub> = 28 V	— —	— —	5.0 5.0	mA
I <sub>VCC2OP</sub>	Operating VCC2 Supply Current <sup>[1]</sup> V <sub>CC</sub> = 55 V and V <sub>CC2</sub> = 28 V V <sub>CC</sub> = 12 V and V <sub>CC2</sub> = 12 V	— —	— —	12 9.0	mA

Symbol	Parameter	Min	Typ	Max	Unit	
$I_{V_{CC2}LOG}$	Additional Operating $V_{CC2}$ Supply Current for Each Logic Input Pin Active $V_{CC} = 55\text{ V}$ and $V_{CC2} = 28\text{ V}$	[2]	—	5.0	mA	
UV	Undervoltage Shutdown VCC	4.0	5.0	5.5	V	
UV2	Undervoltage Shutdown VCC2	[3]	4.0	5.0	5.5	V
OV	Overvoltage Shutdown VCC	57	61	65	V	
OV2	Overvoltage Shutdown VCC2	29.5	31	35	V	
<b>Output</b>						
RDS	Output Sink Resistance (Turned Off) $I_{discharge\ LSS} = 50\text{ mA}$ , $V_{SRC\_HS} = 0\text{ V}$	[3]	—	22	$\Omega$	
RDS	Output Source Resistance (Turned On) $I_{charge\ HSS} = 50\text{ mA}$ , $V_{CP\_OUT} = 20\text{ V}$	[3]	—	22	$\Omega$	
ICHARGE HSS	Charge Current of the External High-Side MOSFET Through GATE_HSn Pin	[4]	—	100	200	mA
VMAX	Maximum Voltage ( $V_{GATE\_HS} - V_{SRC\_HS}$ ) INH = Logic 1, $I_{Smax} = 5.0\text{ mA}$	—	—	18	V	

- [1] Logic input pin inactive (high impedance).
- [2] High-frequency PWM-ing ( $\gg 20\text{ kHz}$ ) of the logic inputs will result in greater power dissipation within the device. Care must be taken to remain within the package power handling rating.
- [3] The device may exhibit predictable behavior between 4.0 V and 5.5 V.
- [4] See [Figure 5](#) for a description of charge current.

### 8.3 Dynamic electrical characteristics

**Table 5. Dynamic electrical characteristics**

Characteristics noted under conditions  $7.0\text{ V} \leq V_{SUP} \leq 18\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ ,  $GND = 0.0\text{ V}$  unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^\circ\text{C}$  under nominal conditions unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	
<b>Timing characteristics</b>						
$t_{PD}$	Propagation Delay High Side and Low Side $C_{LOAD} = 5.0\text{ nF}$ , Between 50% Input to 50% Output (see <a href="#">Figure 4</a> )	[1]	—	200	300	ns
$t_R$	Turn-On Rise Time $C_{LOAD} = 5.0\text{ nF}$ , 10% to 90%, (see <a href="#">Figure 4</a> )	[1] [2]	—	80	180	ns
$t_F$	Turn-Off Fall Time $C_{LOAD} = 5.0\text{ nF}$ , 10% to 90%, (see <a href="#">Figure 4</a> )	[1] [2]	—	80	180	ns

- [1]  $C_{LOAD}$  corresponds to a capacitor between GATE\_HS and SRC\_HS for the high side and between GATE\_LS and ground for low side.
- [2] Rise time is given by time needed to change the gate from 1.0 V to 10 V (vice versa for fall time).

8.4 Timing diagram

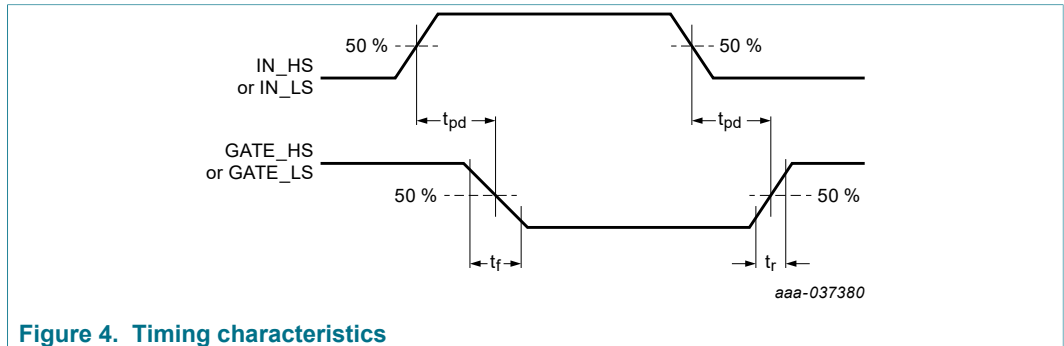


Figure 4. Timing characteristics

9 Functional description

9.1 Introduction

The 33883 is an H-bridge gate driver (or full-bridge pre-driver) with integrated charge pump and independent high- and low-side driver channels. It has the capability to drive large gate-charge MOSFETs and supports high PWM frequency. In sleep mode its supply current is very low.

9.2 Functional pin description

9.2.1 Supply voltage pins (VCC and VCC2)

The VCC and VCC2 pins are the power supply inputs to the device. VCC is used for the output high-side drivers and the charge pump. VCC2 is used for the linear regulation. They can be connected together or independent with different voltage values. The device can operate with VCC up to 55 V and VCC2 up to 28 V.

The VCC and VCC2 pins have undervoltage (UV) and overvoltage (OV) shutdown. If one of the supply voltage drops below the undervoltage threshold or rises above the overvoltage threshold, the gate outputs are switched LOW in order to switch off the external MOSFETs. When the supply returns to a level that is above the UV threshold or below the OV threshold, the device resumes normal operation according to the established condition of the input pins.

9.2.2 Input high-side and low-side pins (IN\_HS1, IN\_HS2, IN\_LS1, IN\_LS2)

The IN\_HS<sub>n</sub> and IN\_LS<sub>n</sub> pins are input control pins used to control the gate outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. IN\_HS<sub>n</sub> and IN\_LS<sub>n</sub> independently control GATE\_HS<sub>n</sub> and GATE\_LS<sub>n</sub>, respectively.

During wake-up, the logic is supplied from the G\_EN pin. There is no internal circuit to prevent the external high-side and low-side MOSFETs from conducting at the same time.

9.2.3 Source output high-side pins (SRC\_HS1 and SRC\_HS2)

The SRC\_HS<sub>n</sub> pins are the sources of the external high-side MOSFETs. The external high-side MOSFETs are controlled using the IN\_HS<sub>n</sub> inputs.



### 9.2.4 Gate high-side and low-side pins (GATE\_HS1, GATE\_HS2, GATE\_LS1, GATE\_LS2)

The GATE\_HS<sub>n</sub> and GATE\_LS<sub>n</sub> pins are the gates of the external high- and low-side MOSFETs. The external high- and low-side MOSFETs are controlled using the IN\_HS<sub>n</sub> and IN\_LS<sub>n</sub> inputs.

### 9.2.5 Global enable (G\_EN)

The G\_EN pin is used to place the device in a sleep mode. When the G\_EN pin voltage is a logic LOW state, the device is in sleep mode. The device is enabled and fully operational when the G\_EN pin voltage is logic HIGH, typically 5.0 V.

### 9.2.6 Charge pump out (CP\_OUT)

The CP\_OUT pin is used to connect an external reservoir capacitor for the charge pump.

### 9.2.7 Charge pump capacitor pins (C1 and C2)

The C1 and C2 pins are used to connect an external capacitor for the charge pump.

### 9.2.8 Linear regulator output (LR\_OUT)

The LR\_OUT pin is the output of the internal regulator. It is used to connect an external capacitor.

### 9.2.9 Ground pins (GND\_A, GND1, GND2)

These pins are the ground pins of the device. They should be connected together with a very low impedance connection.

## 9.3 Functional truth table

Table 6. Functional truth table

Conditions	G_EN	IN_HS <sub>n</sub>	IN_LS <sub>n</sub>	Gate_HS <sub>n</sub>	Gate_LS <sub>n</sub>	Comments
Sleep	0	x	x	0	0	Device is in Sleep mode. The gates are at low state.
Normal	1	1	1	1	1	Normal mode. The gates are controlled independently.
Normal	1	0	0	0	0	Normal mode. The gates are controlled independently.
Undervoltage	1	x	x	0	0	The device is currently in fault mode. The gates are at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overvoltage	1	x	x	0	0	The device is currently in fault mode. The gates are at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overtemperature on High-Side Gate Driver	1	1	x	0	x	The device is currently in fault mode. The high-side gate is at low state. Once the fault is removed, the 33883 recovers its normal mode.
Overtemperature on Low-Side Gate Driver	1	x	1	x	0	The device is currently in fault mode. The low-side gate is at low state. Once the fault is removed, the 33883 recovers its normal mode.

### 9.4 Functional device operation

Driver characteristics

Figure 5 represents the external circuit of the high-side gate driver. In the schematic, HSS represents the switch that is used to charge the external high-side MOSFET through the GATE\_HS pin. LSS represents the switch that is used to discharge the external high-side MOSFET through the GATE\_HS pin. A 180 kΩ internal typical passive discharge resistance and a 18 V typical protection zener are in parallel with LSS. The same schematic can be applied to the external low-side MOSFET driver simply by replacing pin CP\_OUT with pin LR\_OUT, pin GATE\_HS with pin GATE\_LS, and pin SRC\_HS with GND.

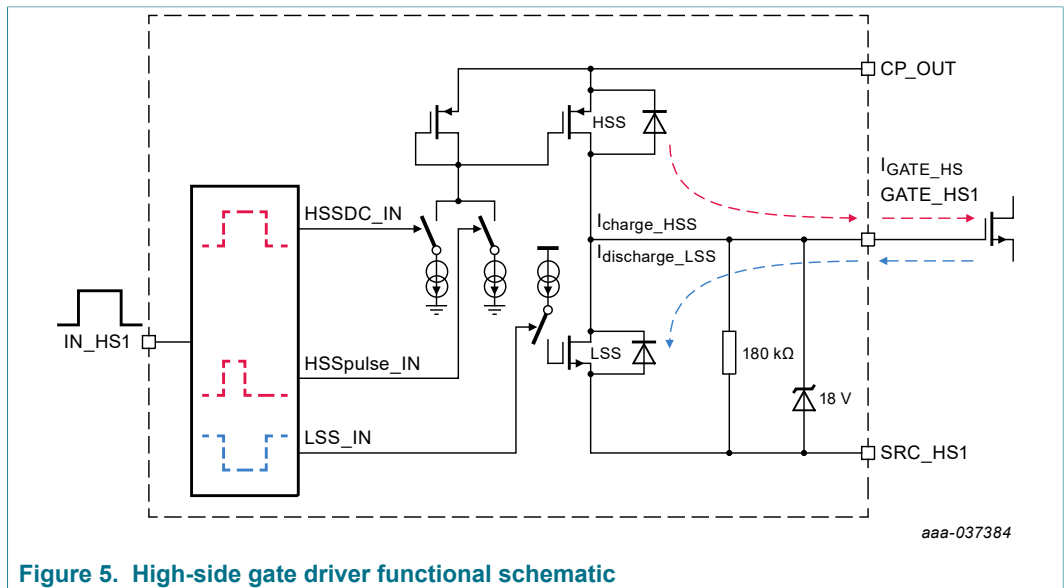
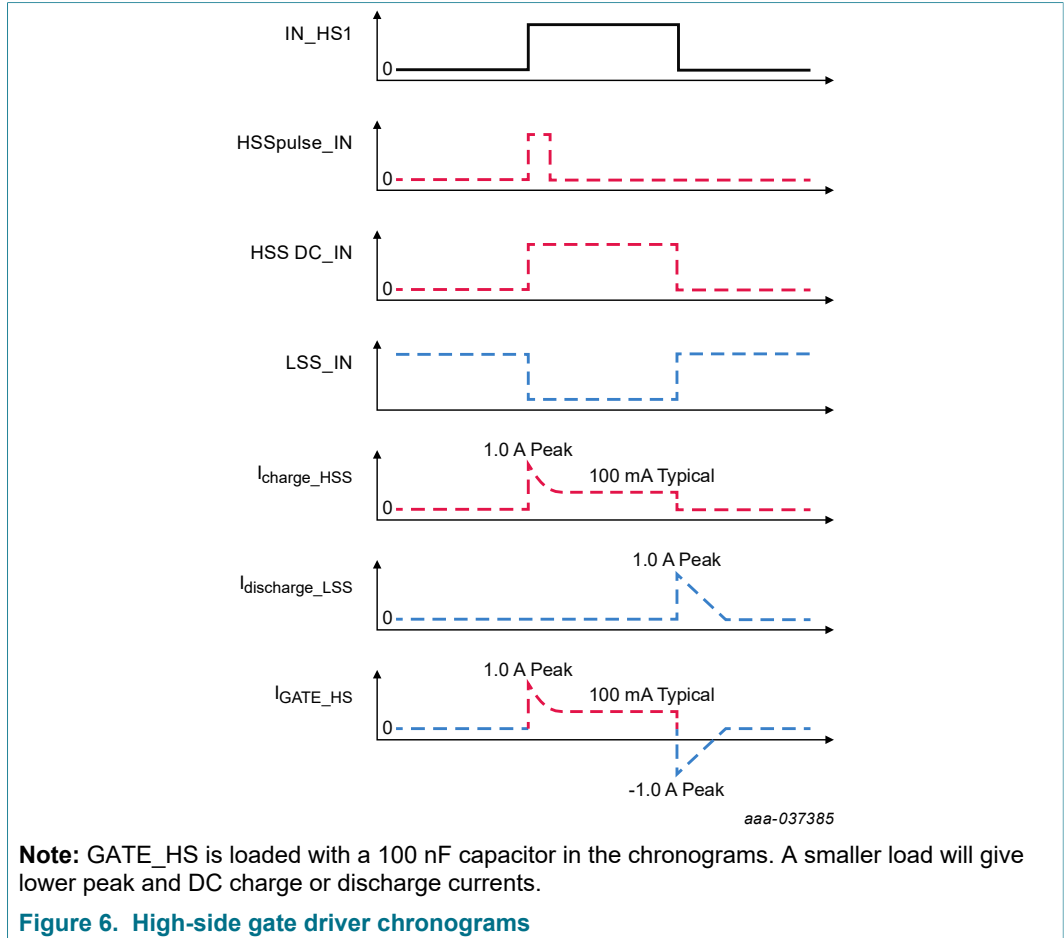


Figure 5. High-side gate driver functional schematic

The different voltages and current of the high-side gate driver are illustrated in Figure 6. The output driver sources a peak current of up to 1.0 A for 200 ns to turn on the gate. After 200 ns, 100 mA is continuously provided to maintain the gate charged. The output driver sinks a high current to turn off the gate. This current can be up to 1.0 A peak for a 100 nF load.



## 9.5 Modes of operation

### 9.5.1 Turn-on

For turn-on, the current required to charge the gate source capacitor  $C_{iss}$  in the specified time can be calculated as follows:

$$I_P = \frac{Q_G}{t_r} = \frac{80 \text{ nC}}{80 \text{ ns}} \approx 1.0 \text{ A}$$

Where  $Q_g$  is power MOSFET gate charge and  $t_r$  is peak current for rise time.

### 9.5.2 Turn-off

The peak current for turn-off can be obtained in the same way as for turn-on, with the exception that peak current for fall time,  $t_f$ , is substituted for  $t_r$ :

$$I_P = \frac{Q_G}{t_f} = \frac{80 \text{ nC}}{80 \text{ ns}} \approx 1.0 \text{ A}$$

In addition to the dynamic current required to turn off or on the MOSFET, various application-related switching scenarios must be considered. These scenarios are presented in Figure 7. In order to withstand high dV/dt spikes, a low resistive path between gate and source is implemented during the OFF-state.

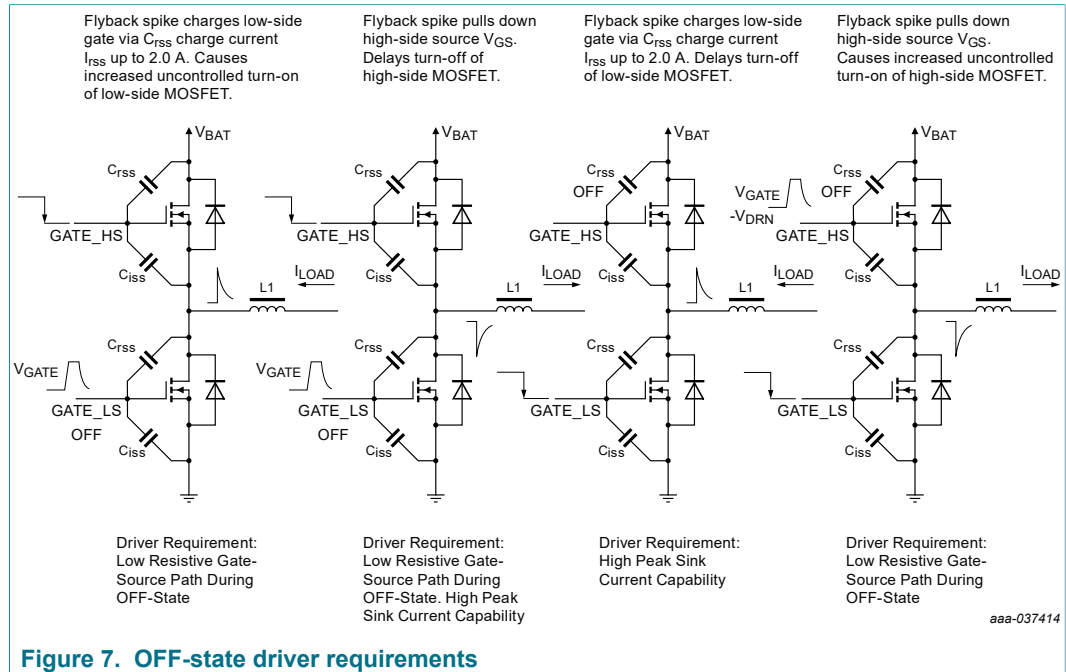


Figure 7. OFF-state driver requirements

### 9.5.3 Low-drop linear regulator

The low-drop linear regulator is supplied by  $V_{CC2}$ . If  $V_{CC2}$  exceeds 15.0 V, the output is limited to 14.5 V (typical).

The low-drop linear regulator provides the 5.0 V for the logic section of the driver, the  $V_{gs\_ls}$  buffered at LR\_OUT, and the +14.5 V for the charge pump, which generates the CP\_OUT. The low-drop linear regulator provides 4.0 mA average current per driver stage.

In case of the full bridge, that means approximately 16 mA — 8.0 mA for the high side and 8.0 mA for the low side.

**Note:** The average current required to switch a gate with a frequency of 100 kHz is:

$$I_{CP} = Q_G * f_{PWM} = 80 \text{ nC} * 100 \text{ kHz} = 8.0 \text{ mA}$$

In a full-bridge application, only one high-side and one low-side switches on or off at the same time.

### 9.5.4 Charge pump

The charge pump generates the high-side driver supply voltage (CP\_OUT), buffered at CCP\_OUT. Figure 8 shows the charge pump basic circuit without load.

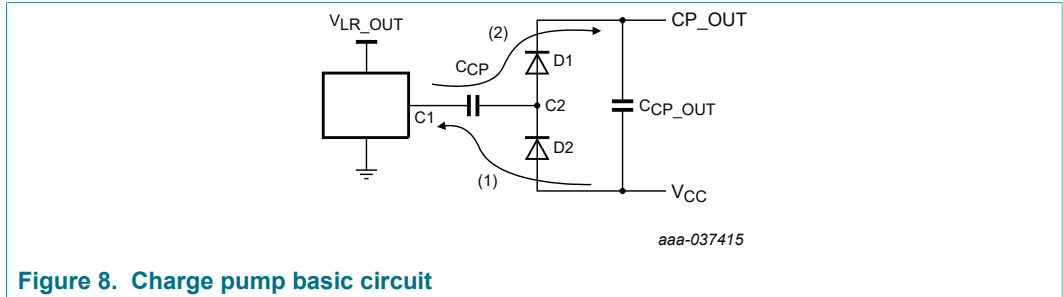


Figure 8. Charge pump basic circuit

When the oscillator is in low state [(1) in Figure 8],  $C_{CP}$  is charged through  $D2$  until its voltage reaches  $V_{CC} - V_{D2}$ . When the oscillator is in high state (2),  $C_{CP}$  is discharged through  $D1$  in  $C_{CP\_OUT}$ , and final voltage of the charge pump,  $V_{CP\_OUT}$ , is  $V_{CC} + V_{LR\_OUT} - 2V_D$ . The frequency of the 33883 oscillator is about 330 kHz.

9.5.5 External capacitors choice

External capacitors on the charge pump and on the linear regulator are necessary to supply high peak current absorbed during switching.

Figure 9 represents a simplified circuitry of the high-side gate driver. Transistors  $Tosc1$  and  $Tosc2$  are the oscillator-switching MOSFETs. When  $Tosc1$  is on, the oscillator is at low level. When  $Tosc2$  is on, the oscillator is at high level. The capacitor  $C_{CP\_OUT}$  provides peak current to the high-side MOSFET through HSS during turn-on (3).

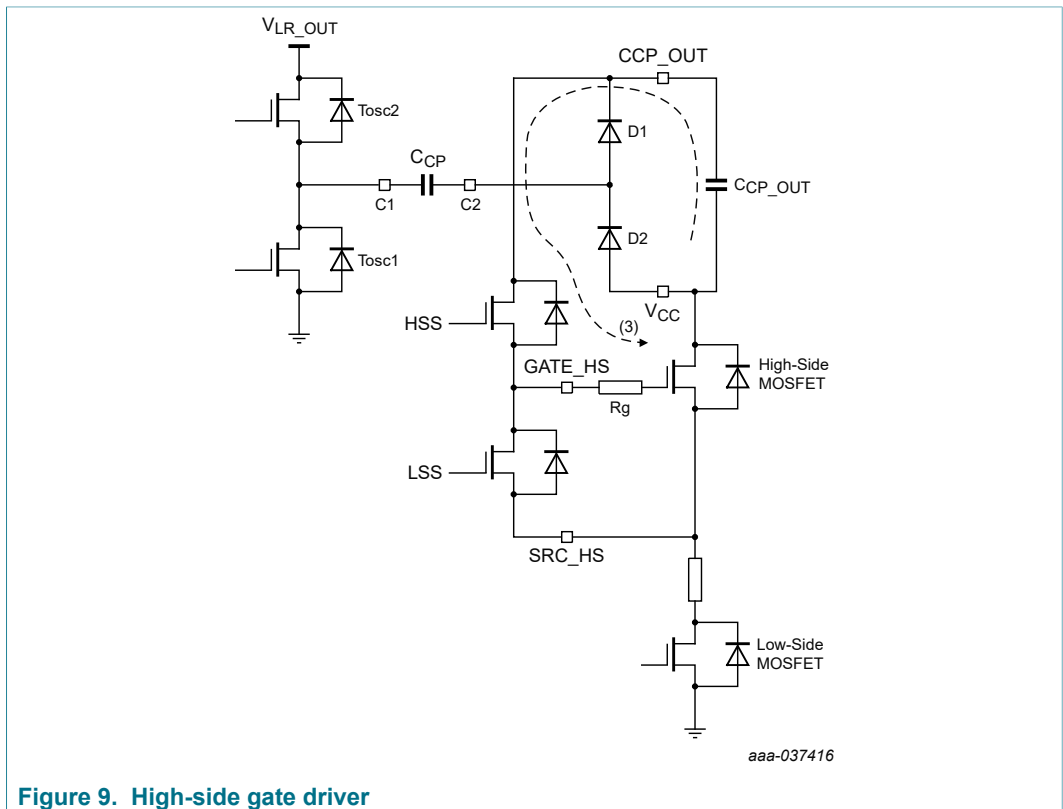


Figure 9. High-side gate driver

9.5.6  $C_{CP}$

$C_{CP}$  choice depends on power MOSFET characteristics and the working switching frequency. Figure 10 contains two diagrams that depict the influence of  $C_{CP}$  value on  $V_{CP\_OUT}$  average voltage level. The diagrams represent two different frequencies for two power MOSFETs, MTP60N06HD and MPT36N06V.

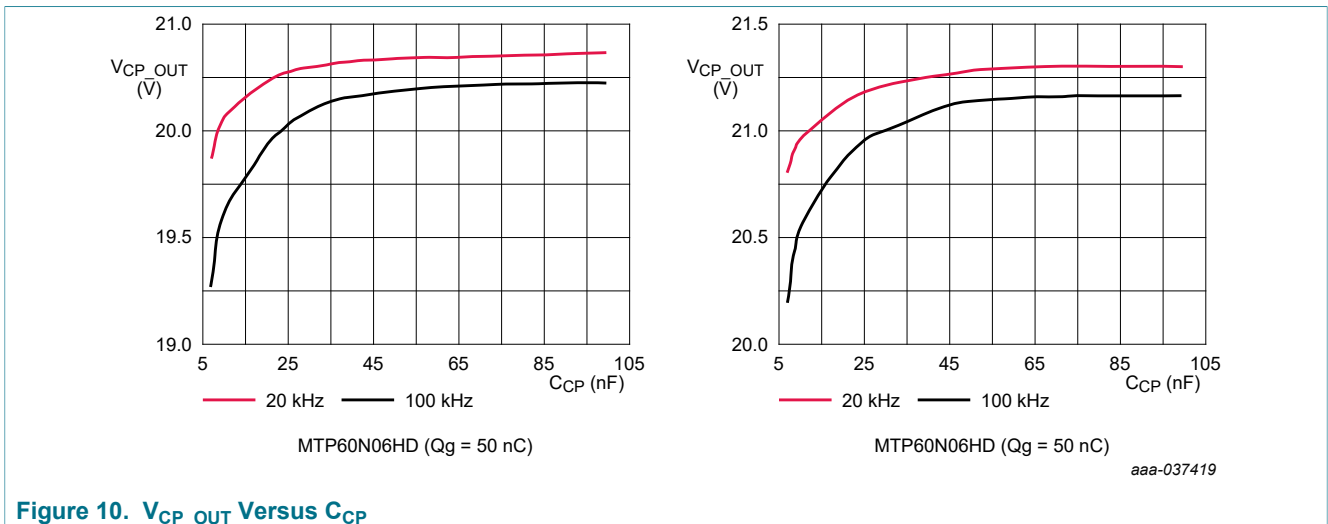


Figure 10.  $V_{CP\_OUT}$  Versus  $C_{CP}$

The smaller the  $C_{CP}$  value is, the smaller the  $V_{CP\_OUT}$  value is. Moreover, for the same  $C_{CP}$  value, when the switching frequency increases, the average  $V_{CP\_OUT}$  level decreases. For most of the applications, a typical value of 33 nF is recommended.

9.5.7  $C_{CP\_OUT}$

Figure 11 depicts the simplified  $C_{CP\_OUT}$  current and voltage waveforms.  $f_{PWM}$  is the working switching frequency.

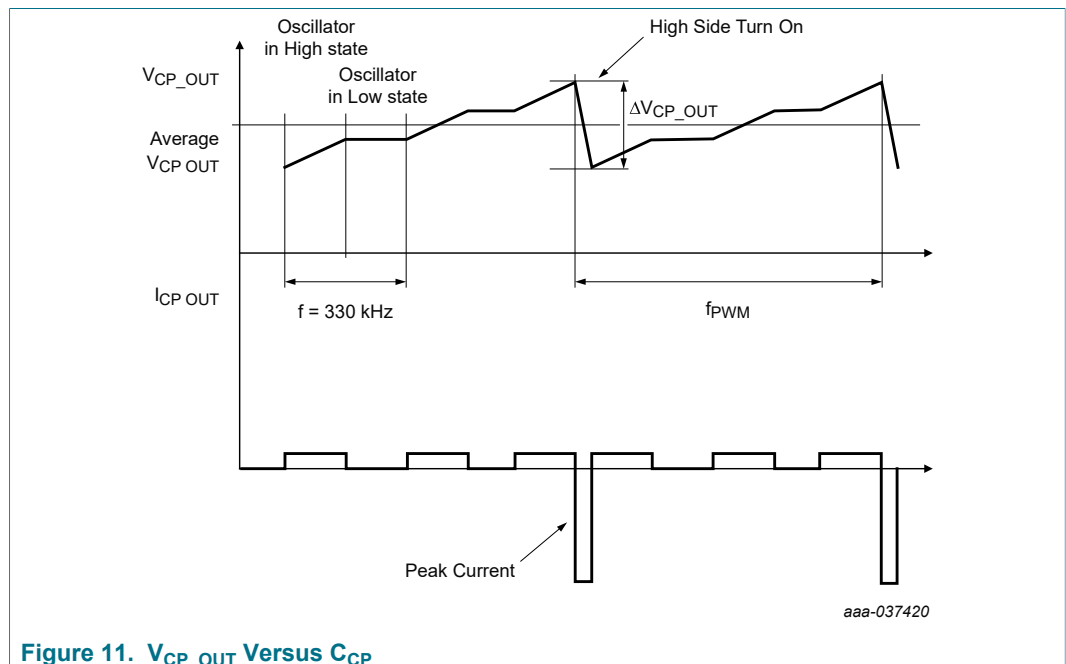


Figure 11.  $V_{CP\_OUT}$  Versus  $C_{CP}$

As shown above, at high-side MOSFET turn-on  $V_{CP\_OUT}$  voltage decreases. This decrease can be calculated according to the  $C_{CP\_OUT}$  value as follows:

$$\Delta V_{CP\_OUT} = \frac{Q_G}{C_{CP\_OUT}}$$

Where  $Q_g$  is power MOSFET gate charge.

### 9.5.8 $C_{LR\_OUT}$

$C_{LR\_OUT}$  provides peak current needed by the low-side MOSFET turn-on.  $V_{LR\_OUT}$  decrease is as follows:

$$\Delta V_{LR\_OUT} = \frac{Q_G}{C_{LR\_OUT}}$$

### 9.5.9 Typical values of capacitors

In most working cases the following typical values are recommended for a well-performing charge pump:

$C_{CP} = 33 \text{ nF}$ ,  $C_{CP\_OUT} = 470 \text{ nF}$ , and  $C_{LR\_OUT} = 470 \text{ nF}$

These values give a typical 100 mV voltage ripple on  $V_{CP\_OUT}$  and  $V_{LR\_OUT}$  with  $Q_g = 50 \text{ nC}$ .

## 9.6 Protection and diagnostic features

### 9.6.1 Gate protection

The low-side driver is supplied from the built-in low-drop regulator. The high-side driver is supplied from the internal charge pump buffered at  $CP\_OUT$ .

The low-side gate is protected by the internal linear regulator, which ensures that  $V_{GATE\_LS}$  does not exceed the maximum  $V_{GS}$ . Especially when working with the charge pump, the voltage at  $CP\_OUT$  can be up to 65 V. The high-side gate is clamped internally in order to avoid a  $V_{GS}$  exceeding 18 V.

Gate protection does not include a fly-back voltage clamp that protects the driver and the external MOSFET from a fly-back voltage that can occur when driving inductive load. This fly-back voltage can reach high negative voltage values and needs to be clamped externally, as shown in [Figure 12](#).

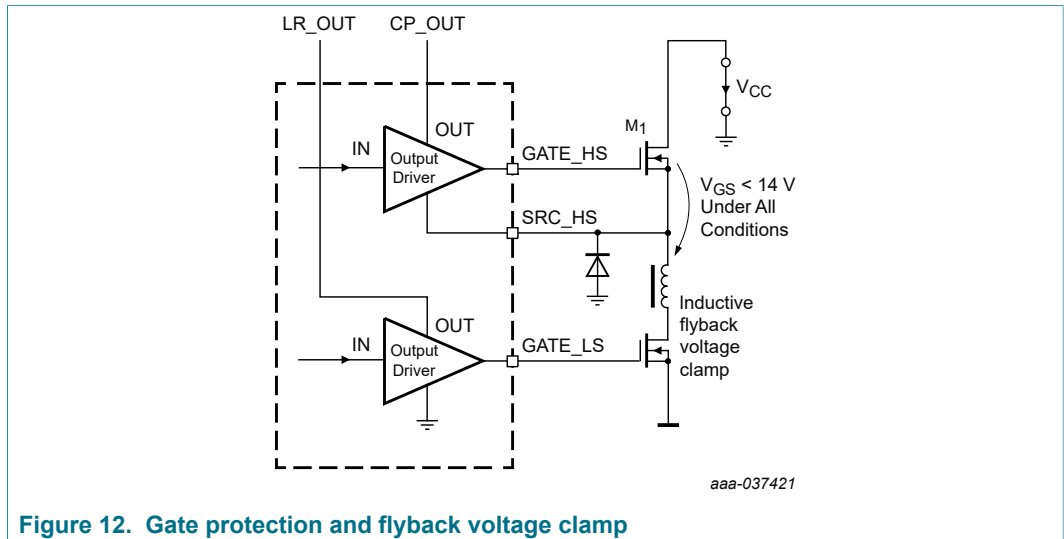


Figure 12. Gate protection and flyback voltage clamp

9.6.2 Load dump and reverse battery

$V_{CC}$  and  $V_{CC2}$  can sustain load a dump pulse of 40 V and double battery of 24 V. Protection against reverse polarity is ensured by the external power MOSFET with the free-wheeling diodes forming a conducting pass from ground to  $V_{CC}$ . Additional protection is not provided within the circuit. To protect the circuit an external diode can be put on the battery line. It is not recommended putting the diode on the ground line.

9.6.3 Temperature protection

There is temperature shutdown protection per each half-bridge. Temperature shutdown protects the circuitry against temperature damage by switching off the output drivers. Its typical value is 175 °C with an hysteresis of 15 °C.

9.6.4 DV/DT at  $V_{CC}$

$V_{CC}$  voltage must be higher than (SRC\_HS voltage minus a diode drop voltage) to avoid perturbation of the high-side driver.

In some applications a large  $dV / dt$  at pin C2 owing to sudden changes at  $V_{CC}$  can cause large peak currents flowing through pin C1, as shown in Figure 13.

For positive transitions at pin C2, the absolute value of the minimum peak current,  $I_{C1min}$ , is specified at 2.0 A for a  $t_{C1min}$  duration of 600 ns.

For negative transitions at pin C2, the maximum peak current,  $I_{C1max}$ , is specified at 2.0 A for a  $t_{C1max}$  duration of 600 ns. Current sourced by pin C1 during a large  $dV / dt$  will result in a negative voltage at pin C1 (Figure 13). The minimum peak voltage  $V_{C1min}$  is specified at -1.5 V for a duration of  $t_{C1max} = 600$  ns. A series resistor with the charge pump capacitor ( $C_{cp}$ ) capacitor can be added in order to limit the surge current.



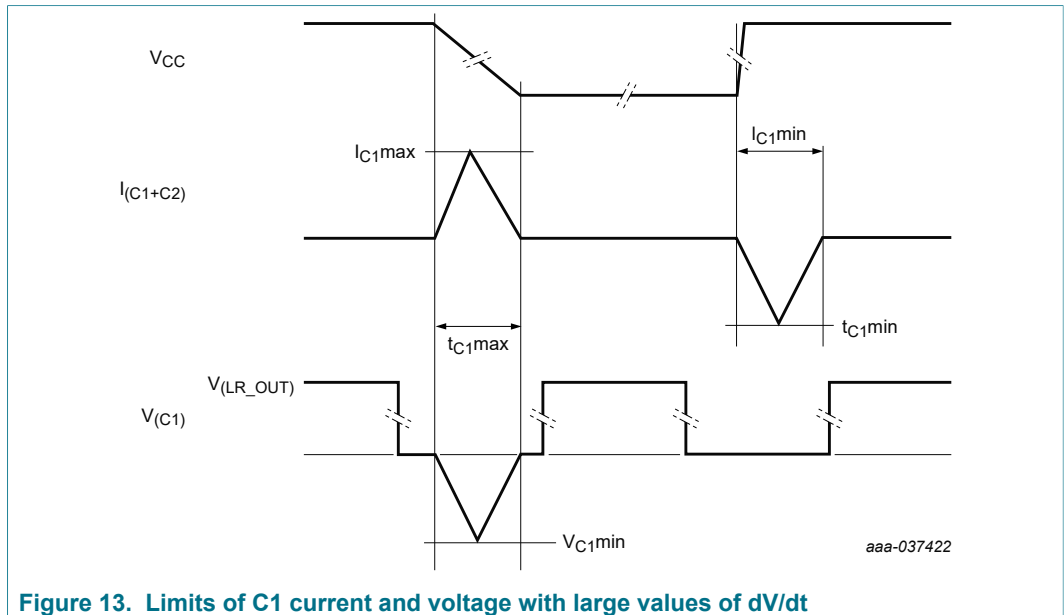


Figure 13. Limits of C1 current and voltage with large values of dV/dt

In the case of rapidly changing  $V_{CC}$  voltages, the large  $dV/dt$  may result in perturbations of the high-side driver, thereby forcing the driver into an OFF state. The addition of capacitors C3 and C4, as shown in Figure 14, reduces the  $dV/dt$  of the source line, consequently reducing driver perturbation. Typical values for R3 / R4 and C3 / C4 are 10  $\Omega$  and 10 nF, respectively.

### 9.6.5 DV/DT at $V_{CC2}$

When the external high-side MOSFET is on, in case of rapid negative change of  $V_{CC2}$  the voltage ( $V_{GATE\_HS} - V_{SRC\_HS}$ ) can be higher than the specified 18 V. In this case a resistance in the SRC line is necessary to limit the current to 5.0 mA max. It will protect the internal zener placed between GATE\_HS and SRC pins.

In case of high current ( $SRC\_HS > 100$  mA) and high voltage ( $> 20$  V) between GATE\_HSX and SRC\_HS an external zener of 18 V is needed as shown in Figure 14.



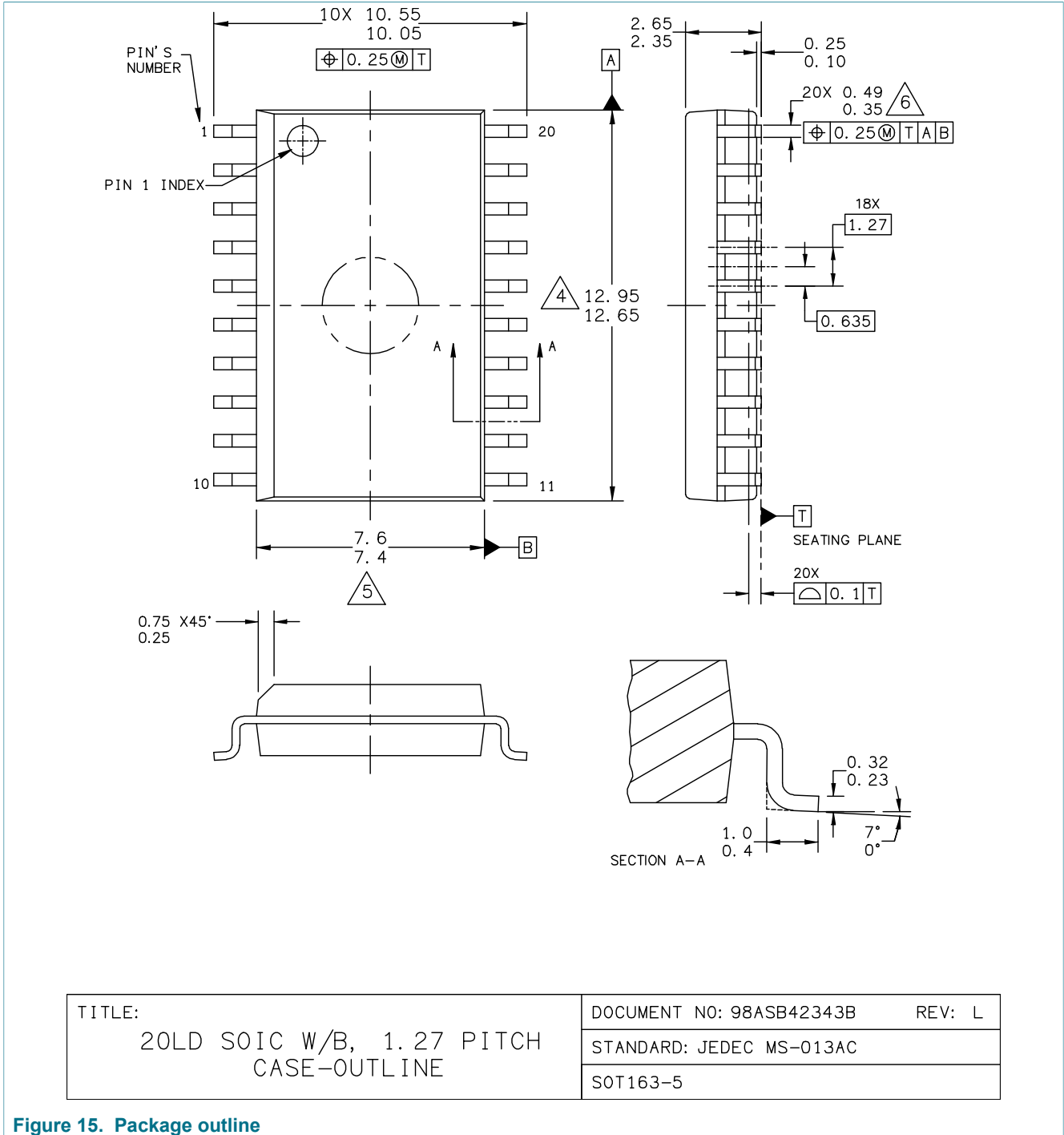


Figure 15. Package outline

## 12 Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33883 v.11.0	20200427	Technical data	2020040161	MC33883 v.10.0
Modifications	<ul style="list-style-type: none"> <li>Changed format to match latest NXP data sheet format</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a>: Added "Qualified in compliance with AEC-Q100"</li> </ul>			
MC33883 v.10.0	10/2012	Technical data	—	MC33883 v.9.0
Modifications	<ul style="list-style-type: none"> <li>Updated orderable part number from MCZ33883EG to MC33883HEG.</li> <li>Updated Freescale form and style</li> <li>Removed MC33883DW from the ordering information</li> <li>Changed from Advance Information to Technical Data</li> </ul>			
MC33883 v.9.0	1/2007	Technical data	—	MC33883 v.8.0
Modifications	<ul style="list-style-type: none"> <li>Implemented Revision History page</li> <li>Updated to the current Freescale format and style</li> <li>Added MCZ33883EG/R2 to the Ordering Information</li> <li>Updated the package drawing to Rev. J</li> <li>Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from <a href="#">Table 3</a>. Added note with instructions from <a href="http://www.freescale.com">www.freescale.com</a>.</li> </ul>			

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## Tables

Tab. 1.	Orderable part variations .....	2	Tab. 5.	Dynamic electrical characteristics .....	7
Tab. 2.	Pin definitions .....	4	Tab. 6.	Functional truth table .....	9
Tab. 3.	Maximum ratings .....	5	Tab. 7.	Package Outline .....	18
Tab. 4.	Static electrical characteristics .....	5	Tab. 8.	Revision history .....	20

## Figures

Fig. 1.	Simplified application diagram .....	2	Fig. 10.	VCP_OUT Versus CCP .....	14
Fig. 2.	Internal block diagram .....	3	Fig. 11.	VCP_OUT Versus CCP .....	14
Fig. 3.	Pinout diagram .....	4	Fig. 12.	Gate protection and flyback voltage clamp .....	16
Fig. 4.	Timing characteristics .....	8	Fig. 13.	Limits of C1 current and voltage with large values of dV/dt .....	17
Fig. 5.	High-side gate driver functional schematic .....	10	Fig. 14.	Application schematic with external protection circuit .....	18
Fig. 6.	High-side gate driver chronograms .....	11	Fig. 15.	Package outline .....	19
Fig. 7.	OFF-state driver requirements .....	12			
Fig. 8.	Charge pump basic circuit .....	13			
Fig. 9.	High-side gate driver .....	13			

## Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>
<b>3</b>	<b>Simplified application diagram</b> .....	<b>2</b>
<b>4</b>	<b>Applications</b> .....	<b>2</b>
<b>5</b>	<b>Ordering information</b> .....	<b>2</b>
<b>6</b>	<b>Internal block diagram</b> .....	<b>3</b>
<b>7</b>	<b>Pinning information</b> .....	<b>4</b>
7.1	Pinout diagram .....	4
7.2	Pin definitions .....	4
<b>8</b>	<b>General product characteristics</b> .....	<b>5</b>
8.1	Maximum ratings .....	5
8.2	Static electrical characteristics .....	5
8.3	Dynamic electrical characteristics .....	7
8.4	Timing diagram .....	8
<b>9</b>	<b>Functional description</b> .....	<b>8</b>
9.1	Introduction .....	8
9.2	Functional pin description .....	8
9.2.1	Supply voltage pins (VCC and VCC2) .....	8
9.2.2	Input high-side and low-side pins (IN_HS1, IN_HS2, IN_LS1, IN_LS2) .....	8
9.2.3	Source output high-side pins (SRC_HS1 and SRC_HS2) .....	8
9.2.4	Gate high-side and low-side pins (GATE_ HS1, GATE_HS2, GATE_LS1, GATE_LS2) .....	9
9.2.5	Global enable (G_EN) .....	9
9.2.6	Charge pump out (CP_OUT) .....	9
9.2.7	Charge pump capacitor pins (C1 and C2) .....	9
9.2.8	Linear regulator output (LR_OUT) .....	9
9.2.9	Ground pins (GND_A, GND1, GND2) .....	9
9.3	Functional truth table .....	9
9.4	Functional device operation .....	10
9.5	Modes of operation .....	11
9.5.1	Turn-on .....	11
9.5.2	Turn-off .....	11
9.5.3	Low-drop linear regulator .....	12
9.5.4	Charge pump .....	12
9.5.5	External capacitors choice .....	13
9.5.6	CCP .....	14
9.5.7	CCP_OUT .....	14
9.5.8	CLR_OUT .....	15
9.5.9	Typical values of capacitors .....	15
9.6	Protection and diagnostic features .....	15
9.6.1	Gate protection .....	15
9.6.2	Load dump and reverse battery .....	16
9.6.3	Temperature protection .....	16
9.6.4	DV/DT at VCC .....	16
9.6.5	DV/DT at VCC2 .....	17
<b>10</b>	<b>Typical applications</b> .....	<b>18</b>
<b>11</b>	<b>Packaging</b> .....	<b>18</b>
11.1	Package mechanical dimensions .....	18
<b>12</b>	<b>Revision history</b> .....	<b>20</b>
<b>13</b>	<b>Legal information</b> .....	<b>21</b>

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