Document Number: MC34SB0800
Rev. 3.0, 8/2016

Fully integrated octal valve controller system on chip

SB0800

INDUSTRIAL CONTROLLER CHIP

AE SUFFIX (PB-FREE)
98ASA10763D
64-PIN LQFP-EP

The SB0800 device is a valves and pump controller system designed for use in harsh industrial environments.

It has eight high-current low-side drivers for use with solenoid valves, and high-side gate drivers for use with controlling two external N-channel MOSFETs, for DC motor and a master relay for solenoid coils. Alongside this, the SB0800 has three analog to digital converters, plus a low-side driver allowing drive resistive charges. The SB0800 boosts an internal charge pump, permitting the high-side drivers to use inexpensive N-channel MOSFETs. The digital I/O pins can be configured for both 5.0 V and 3.3 V levels for easy connection to any microprocessor. The SB0800 uses standard SPI protocol communication.

The SB0800 is a perfect solution for hydraulic and pneumatic applications. This device is powered by SMARTMOS technology.

Features

- Operating voltage 6.0 V to 36 V
- Eight valves control
  - Four current regulated valves up to 2.25 A (5.0 kHz)
  - Four PWMed valves up to 5.0 A (5.0 kHz)
- High-side predriver for valves protection
- Pump motor predriver up to 500 Hz PWM
- 16-bit SPI interface with watchdog
- Three 10-bit ADC channels
- High-side driver for general purpose ($R_{DS(on)}$ 1.0 Ω)
- Low-side driver for resistive charge ($R_{DS(on)}$ 14.0 Ω)
- Die temperature warning
- Supervision

Applications

Industrial Controller

- Spot Welding
- Fluid Coating
- Temperature Control
- Brake Pressure
- Laser Cutting
- Bottle Moulding
- Filling Pressure
- 3D Printer
- Oxygen Concentrator
- Medical test equipment
- Dialysis machines
- Blood pressure
- Soda dispensers
- Heavy equipment and construction machinery
- Fork lifts
- Water control system for irrigation (connected to farm tractor)
- Food control in animal farm

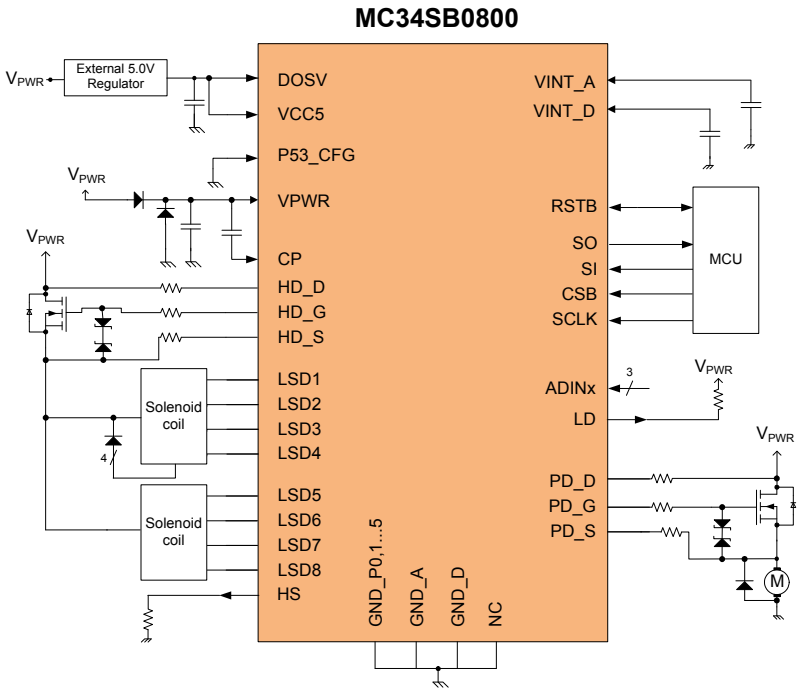

Figure 1. SB0800 simplified 5.0 V application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

1 Orderable parts

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search for the following device numbers.

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package	Description	Notes
34SB0800 octal valves and pump controller system on chip for industrial				
MC34SB0800AE	-40 °C to 125 °C	10 x 10, 64 LQFP-EP	• Four PWMed valve controls and four current regulated valve controls • Safe switch control • Pump motor control up to 500 Hz • High-side driver for general purpose • Low-side FET for resistive loads	(1)

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

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2 Internal block diagram

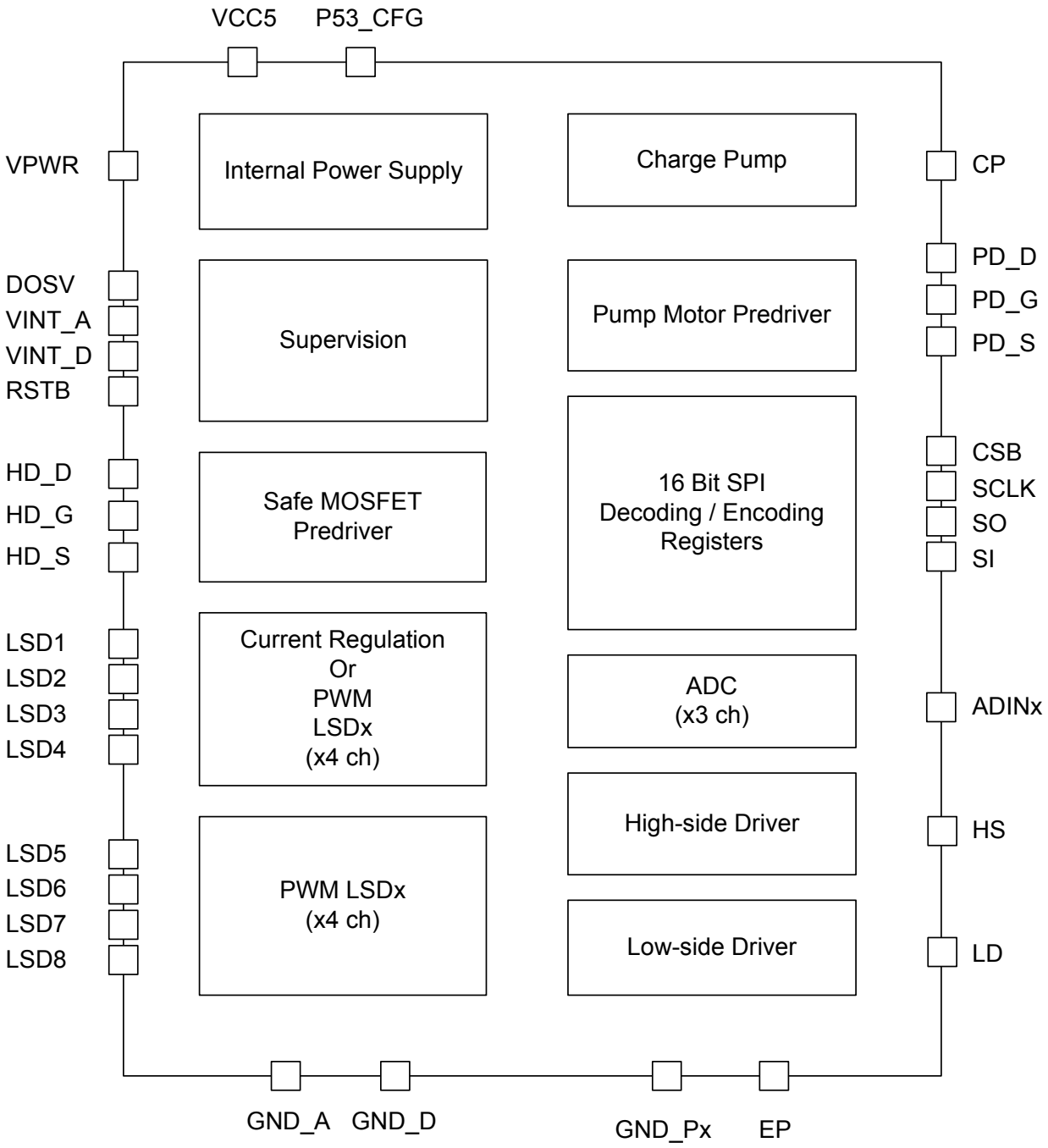


Figure 2. SB0800 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

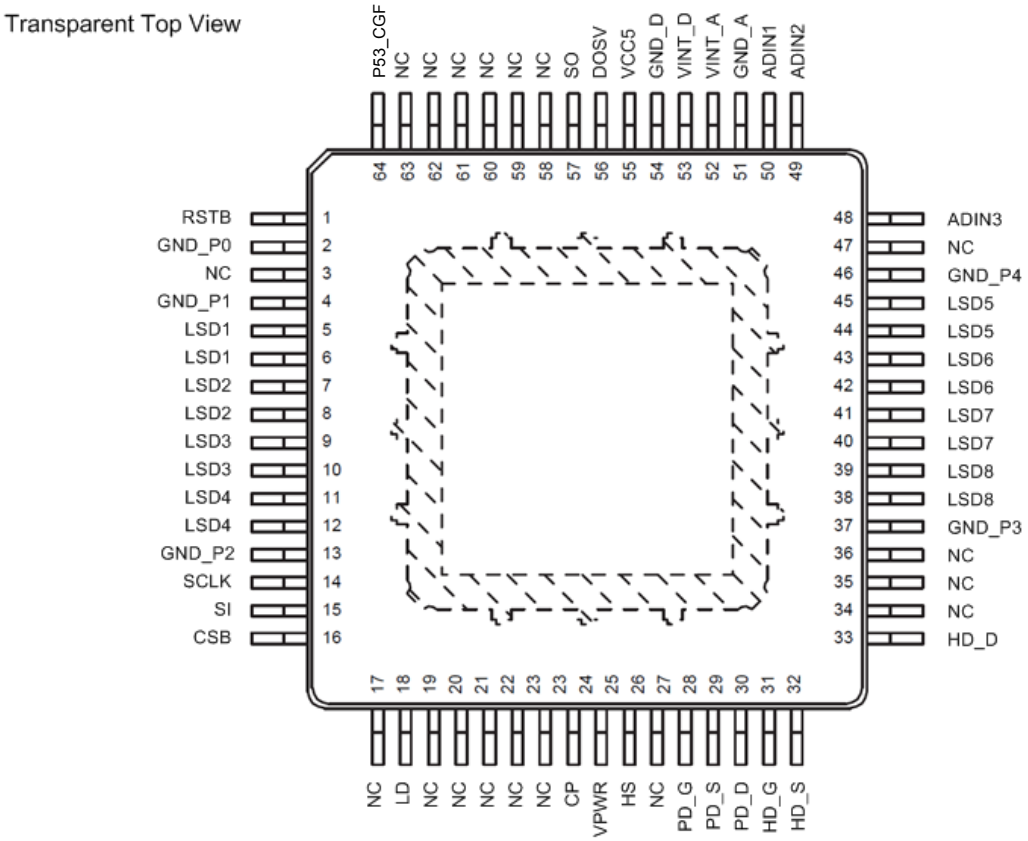


Figure 3. SB0800 64-pin LQFP-EP pinout diagram

3.2 Pin definitions

Table 2. SB0800 pin definitions

Pin number	Pin name	Pin function	Definition	DOSV = 5.0 V	DOSV = 3.3 V	Notes
1	RSTB	Reset	Reset PIN	external pull-up		
2	GND_P0	Supply	Power Ground 0 (4)	no	no	
4	GND_P1	Supply	Power Ground 1	no	no	(4)
5, 6	LSD1	Low-side Driver for Current Regulated & PWMed Valves	Open Drain Output for Low-side Driver 1	no	no	(2)
7, 8	LSD2	Low-side Driver for Current Regulated & PWMed Valves	Open Drain Output for Low-side Driver 2	no	no	(2)
9, 10	LSD3	Low-side Driver for Current Regulated & PWMed Valves	Open Drain Output for Low-side Driver 3	no	no	(2)
11, 12	LSD4	Low-side Driver for Current Regulated & PWMed Valves	Open Drain Output for Low-side Driver 4	no	no	(2)
13	GND_P2	Supply	Power Ground 2	no	no	(4)
14	SCLK	SPI	SPI Interface Clock Input	no	no	
15	SI	SPI	SPI Interface Digital Input	no	no	
16	CSB	SPI	SPI Interface Chip Interface	no	no	
18	LD	Low-side Driver	Open Drain Output for Low-side	no	no	
24	CP	Charge Pump	Charge Pump Output. For internal use, connect a storage capacitor of > 68 nF to VPWR.	no	no	
25	VPWR	Supply	Supply PIN connect to battery through reverse diode	no	no	
26	HS	High-side Driver for General Purpose (optional)	High-side driver for general purpose	no	no	
28	PD_G	Motor Pump Driver	Gate Output to Control Pump Motor FET Connect to gate of external pump motor FET	no	no	
29	PD_S	Motor Pump Driver	Source Feedback Pump Motor FET Connect to source of external pump motor FET	no	no	
30	PD_D	Motor Pump Driver	Drain Feedback Pump Motor FET Connect to drain of external pump motor FET	no	no	
31	HD_G	High-side Driver for Valve's Fail-safe FET	Gate Output to Control High-side FET Connect to gate of external pump motor FET	no	no	
32	HD_S	High-side Driver for Valve's Fail-safe FET	Source Feedback High-side FET Connect to source of external High-side FET	no	no	
33	HD_D	High-side Driver for Valve's Fail-safe FET	Drain Feedback High-side FET Connect to drain of external High-side FET	no	no	
37	GND_P3	Supply	Power Ground 3	no	no	(4)
38, 39 (2)	LSD8	Low-side Driver for PWMed Valves	Open Drain Output for Low-side Driver 8	no	no	
40, 41 (2)	LSD7	Low-side Driver for PWMed Valves	Open Drain Output for Low-side Driver 7	no	no	
42, 43 (2)	LSD6	Low-side Driver for PWMed Valves	Open Drain Output for Low-side Driver 6	no	no	
44, 45 (2)	LSD5	Low-side Driver for PWMed Valves	Open Drain Output for Low-side Driver 5	no	no	
46	GND_P4	Supply	Power Ground 4	no	no	(4)
48	ADIN3	ADC	Analog to Digital Input 3	no	no	

Table 2. SB0800 pin definitions (continued)

Pin number	Pin name	Pin function	Definition	DOSV = 5.0 V	DOSV = 3.3 V	Notes
49	ADIN2	ADC	Analog to Digital Input 2	no	no	
50	ADIN1	ADC	Analog to Digital Input 1	no	no	
51	GND_A	Supply	Analog Ground	no	no	
52	VINT_A	Internal Function	2.5 V internal supply for analog	no	no	(2)
53	VINT_D	Internal Function	2.5 V internal supply for digital	no	no	(2)
54	GND_D	Supply	Digital Ground	no	no	
55	VCC5	Supply	5.0 V Supply PIN	5V	5V	
56	DOSV	Supply	Digital Output Voltage Supply, DOSV under voltage reset	5V	3.3V	
57	SO	SPI	SPI Interface Digital Output	DOSV bias		
64	P53_CFG	Supply	Input to select output voltage at DOSV (5.0 V/ 3.3 V)	no	no	
20, 21, 22, 23, 58, 59, 60, 61, 62	NC	Not connected	Pin used for production tests and must not be grounded	no	no	
3, 17, 19, 27, 34, 35, 36, 47, 63	NC	Not connected	Pin used for production tests and must be grounded	no	no	
Exposed pad	GND_P5	Supply	Power Ground 5	no	no	(4)

Notes

2. Pins must be shorted together
3. 220 nF/10 V capacitor needed
4. All GND_Px pins must be shorted together at the PCB level.

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

Voltage parameters are absolute voltages referenced to GND_A, GND_D and flag (tied together internally). Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Supply					
V_{VPWR}	Analog Power supply voltage	-0.3	40	V	
V_{DOSV}	Digital Output Supply Voltage	-0.3	7.0	V	
V_{P53_CFG}	Selection of 5.0 V or 3.3 V for the digital	-0.3	7.0	V	
V_{VCC5}	Digital power supply voltage	-0.3	7.0	V	
V_{GND_A}	Ground analog	-0.3	0.3	V	
V_{GND_D}	Ground digital	-0.3	0.3	V	
V_{GND_P}	Ground exposed pad	-0.3	0.3	V	
Internal function					
V_{VINT_A}	Internal regulator analog power supply	-0.3	3.0	V	
V_{VINT_D}	Internal regulator digital power supply	-0.3	3.0	V	
Charge pump					
V_{CP}	Internal charge pump	-0.3 or V_{PWR} -0.3	V_{PWR} +15	V	
High-side driver for general purpose					
V_{HS}	High-side driver	-0.3	40 or V_{PWR} +0.3	V	
High-side driver for valve's fail-safe FET					
V_{HD_G}	Gate of the high-side predriver	-20	55	V	
V_{HD_S}	Source of the high-side predriver	-0.3	40	V	
V_{HD_D}	Drain of the high-side predriver	-0.3	40	V	
Motor pump driver					
V_{PD_G}	Gate of the Motor Pump predriver	-0.3	55	V	
V_{PD_S}	Source of the Motor Pump predriver	-0.3	40	V	
V_{PD_D}	Drain of the Motor Pump predriver	-0.3	40	V	
Reset					
V_{RSTB}	Reset pin	-0.3	7.0	V	
A to D converter					
V_{ADINx}	Input analog to digital	-0.3	7.0	V	

Table 3. Maximum ratings (continued)

Voltage parameters are absolute voltages referenced to GND_A, GND_D and flag (tied together internally). Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
SPI					
V_{SO}	Serial peripheral interface slave output	-0.3	DOSV +0.3	V	
V_{SI}	Serial peripheral interface slave input	-0.3	7.0	V	
V_{CSB}	Serial peripheral interface chip select	-0.3	7.0	V	
V_{SCLK}	Serial peripheral interface clock	-0.3	7.0	V	
Low-side driver for valves (LSD1-8)					
V_{LSDx}	Low-side driver for valves	Table	active clamp		
Low-side driver					
V_{LD}	Low-side driver	-100 mA	40	V	
Energy capability					
$E_{LSD1—4}$	Energy capability (EAR) at 125 °C • LSD1—4, with 20 mH load	—	30	mJ	
$E_{LSD5—8}$	Energy capability (EAR) at 125 °C • LSD5—8, with 20 mH load	—	40	mJ	
E_{HS}	Energy capability (EAR) at 125 °C • HS, with 20 mH load	—	13	mJ	
Currents					
$I_{LSDX(POS)}$	Drain continuous current; during on state • LSDx	—	5.0	A	
$I_{LSDX(NEG)}$	Maximum negative current for 5.0 ms without being destroyed • LSDx	-6.0	—	A	
I_{DIG}	Input current • P53_CFG, SI, CSB, SCLK, RSTB	-20	20	mA	

4.2 Operating conditions

This section describes the operating conditions and the current consumptions. Conditions apply to all the following data, unless otherwise noted.

Table 4. Operating conditions

Voltage parameters are absolute voltages referenced to GND. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min.	Typ.	Max.	Unit	Notes
V_{PWR}	Functional operating supply voltage. Device is fully functional. • All features are operating	6.0	—	36	V	
V_{CC5}	Functional operating supply voltage. Device is fully functional. • All features are operating.	4.75	—	5.25	V	
V_{DOSV}	Functional operating supply voltage. Device is fully functional. • All features are operating.	3.13	—	5.25	V	

4.3 Supply currents

This section describes the operating conditions and the current consumptions. Conditions apply to all the following data, unless otherwise noted.

Table 5. Supply currents

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 36 V, 4.75 V ≤ V_{CC5} ≤ 5.25 V, 3.13 V ≤ V_{DOSV} ≤ 5.25 V, -40 °C ≤ T_J ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Description (rating)	Min.	Typ.	Max.	Unit	Notes
VPWR current consumptions						
I_{QVPWR}	Quiescent current of VPWR measured at 36 V, V_{CC5} = 0 V	—	—	30	μA	
I_{VPWR}	Current of VPWR in operating mode, V_{CC5} = 5.0 V	—	20	—	mA	
VCC5 current consumptions						
I_{VCC5}	Current of VCC5 pin in operating mode (SPI frequency at 10 MHz)	—	10	—	mA	
DOSV current consumptions						
I_{DOSV}	Current of DOSV pin in operating mode (SPI frequency at 10 MHz)	—	—	10	mA	

4.4 Thermal ratings

Table 6. Thermal data

Symbol	Description (rating)	Min.	Typ.	Max.	Unit	Notes
T_J	Operational junction Temperature	-40	—	150	°C	
T_{STG}	Storage Temperature	-65	—	150	°C	
$R_{\theta JC}$	RθJC, Thermal Resistance, Junction to Case (Package exposed pad) - Steady state	—	—	2.0	°C/W	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	—	—	Note 7	°C	(5)(6)

Notes

5. Lead soldering temperature limit is for 10 seconds maximum duration. Lead soldering can be done twice. Device must be delivered in dry pack.
6. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

4.5 Logical inputs and outputs

Table 7. Logical inputs/outputs

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Description (rating)	Min.	Max.	Unit	Notes
Logical inputs					
V_{IH_X}	Input High-voltage • P53_CFG, RSTB, SI, CSB, SCLK, ADIN1, ADIN2, ADIN3	—	2.0	V	
V_{IL_X}	Input Low-voltage • P53_CFG, RSTB, SI, CSB, SCLK, ADIN1, ADIN2, ADIN3	0.8	—	V	
Logical outputs					
V_{OH_X}	Input High-voltage, with 1.0 mA • SO	0.8 x DOSV	—	V	
V_{OL_X}	Input Low-voltage, with 1.0 mA • SO	—	0.4	V	
$VOL_{\_RSTB}$	RSTB Low-voltage, with 1.0 mA • RSTB	—	0.4	V	

5 General description

5.1 Block diagram

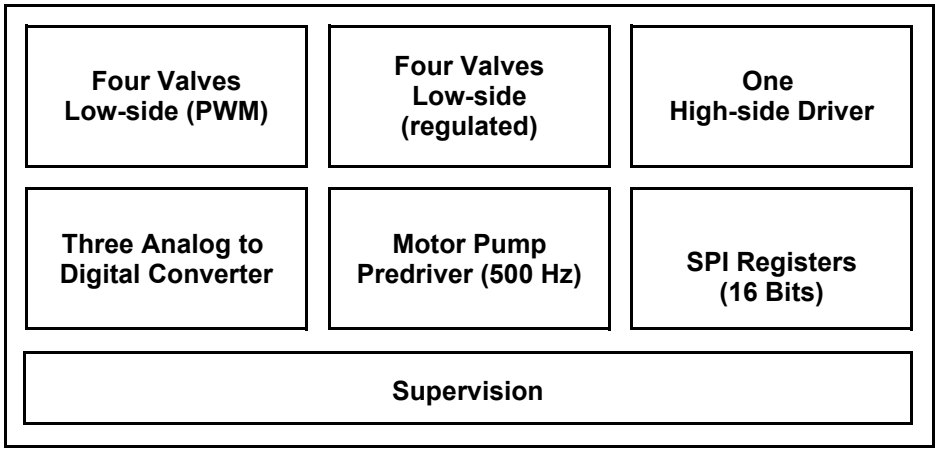


Figure 4. SB0800 functional block diagram

5.2 Functional description

The SB0800 device is a valves and pump controller, designed for use in harsh industrial environments, requiring few external components.

The SB0800 eight high-current low-side drivers for use with solenoid valves, and high-side gate drivers for controlling two external N-channel MOSFETs for use with a pump motor and master relay for a solenoid coil. In conjunction with this primary functionality, the SB0800 has one low-side driver to control a resistive load. The SB0800 boosts an internal charge-pump, allowing the high-side drivers to use inexpensive N-channel MOSFETs. The digital I/O pins can be configured for both 5.0 V and 3.3 V levels for easy connection to any microprocessor. Also, the device integrated three Analog to Digital converters. The SB0800 uses standard SPI protocol for communication.

5.3 Features

This section presents the detailed features of SB0800.

Table 8. Device features set

Function	Description
High-side Driver for Fail-safe FET	• High-side Fail-safe FET driver • Overcurrent shutdown • Load leakage detection
High-side Driver for general purpose	• High-side switch connected to VPWR (1.0 Ω max Rds(on) at 125 °C) • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown
Pump Driver	• Pump motor driver up to 500 Hz PWM frequency controllable through SPI command or a digital signal • Overcurrent shutdown between external FET drain and source

Table 8. Device features set (continued)

Function	Description
Low-side solenoid driver (x4)	• Solenoid driver (300 mΩ max. $R_{DS(on)}$ at 125 °C) works either as current regulator or as PWM • Current regulation deviation: ±2.0% • Configurable PWM frequency from 3.0 kHz to 5.0 kHz • PWM duty cycle 10-bit resolution • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown • Send current regulation error flag (only for current regulation modules)
Low-side solenoid driver (x4)	• Solenoid driver (225 mΩ max $R_{DS(ON)}$ at 125 °C) are PWM low-side driver • Configurable PWM frequency from 3.0 kHz to 5.0 kHz • PWM duty cycle resolution 0.39% • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown • Max switch-off energy 40 mJ
Low-side resistive Driver	• Low-side driver (20 mA max, $R_{DS(on)}$ 8.0 Ω) • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown
Low-side Driver	• Low-side driver (350 mA max, $R_{DS(on)}$ 1.0 Ω) • Open load detection • V_{DS} state monitoring • Overcurrent shutdown • Overtemperature shutdown
Analog to Digital Converter (x3)	• 10-bit ADC • External ADINx pins • Internal voltages and temperature information • Allow to control the pump by a MCU • Allow to control the low-side resistive driver by a MCU
Supervision	• VINT_x undervoltage (internal regulator) • VCC5 & DOSV undervoltage (supply voltage from external) • Watchdog fault • ALU check counter overflow • External reset fault • VPWR undervoltage and overvoltage detections • Mismatch MAIN-AUX OSC CLK • Temperature warning • SPI failure • Charge pump issue • GND supervision

6 Functional block description

6.1 Error handling

Table 9. Error handling

Type of error	Detection condition	Action	Clear SPI flag	Restart condition	Notes
High-side driver					
Overcurrent between external FET Drain and Source	ON	HD_G Off + SPI fault flag (HD_oc)	Write 1 to HD_clr_flt 1	Write 1 to HD_clr_ fit and then turn on by SPI command (hd_ on)	
Load leakage	hd_on rise-edge (SPI bit)	Ignore hd_on rise-edge command + SPI fault flag (HD lkg)	Write 1 to HD_clr_flt	Write 1 to HD_clr_flt and then turn on by SPI command (hd_ on)	
Pump motor PWM driver					
Overcurrent between external FET Drain and Source	ON	PD_G Off+ SPI fault flag (PD_oc)	Write 1 to PD_clr_flt	Write 1 to PD_clr_flt and then turn-on by SPI command (pd on)	
LSDx					
Open Load	OFF	SPI flag only (LSDx_op)	Read diagnosis	No	
V_{DS} state monitoring	ON/OFF	Read V_{DS} state by SPI (vds_LSDx)	update with min filter time (T1) rise and fall edge	No	
Overcurrent	ON	OFF fault FET only + SPI fault flag (LSDx_oc)	Write 1 to LSD_clr_flt	Write 1 to LSD_clr_flt and turn on by SPI command (LSDx duty cycle or current set point)	
Overtemperature	ON	OFF fault FET only + SPI fault flag (LSDx_ot)	Write 1 to LSD_clr_flt	Write 1 to LSD_clr_flt and turn on by SPI command (LSDx duty cycle or current set point)	
Current regulation error (only for LSD1-4)	ON	Read SPI flag only (LSDx_crer)	Read diagnosis	No	
LDx					
Open Load	OFF	SPI flag only (LDx_op)	Read diagnosis	No	
V_{DS} state monitoring	ON/OFF	Send V_{DS} state by SPI (V_{DS_LD})	update with min filter time (T1) rise and fall edge	No	
Overcurrent	ON	OFF fault FET only + SPI fault flag (LD_oc)	Write 1 to LD_clr_flt	Write 1 to LD_clr_flt and turn on by SPI command (LD_on)	
Overtemperature	ON	OFF fault FET only + SPI fault flag (LD_ot)	Write 1 to LD_clr_flt	Write 1 to LD_clr_flt and turn on by SPI command (LD_on)	
HS					
Open Load	OFF	SPI flag only (HS_ op)	Read diagnosis	No	
V_{DS} state monitoring	ON/OFF	Send V_{DS} state by SPI (V_{DS_HS})	update with min filter time	No	
Overcurrent	ON	OFF fault FET only + SPI fault flag (HS_oc)	Write 1 to HS_clr_flt	Write 1 to HS_clr_flt and then turn on by SPI command (HS_ on)	

Table 9. Error handling (continued)

Type of error	Detection condition	Action	Clear SPI flag	Restart condition	Notes
Overtemperature	ON	OFF fault FET only + SPI fault flag (HS_ot)	Write 1 to HS_clr_flt	Write 1 to HS_clr_flt and then turn on by SPI command (HS_on)	
Supervision					
VINT_x Undervoltage	All except Sleep mode	SPI register reset & Vint_uv go to High	Read Vint_uv bit	No	
VCC5 & DOSV Undervoltage	All except Sleep mode	SPI register reset except VCC5_uv go to High	Wait undervoltage reset filter time T1 (see Table 19)	See Table 19,	
External reset fault	No internal RSTB pulldown	SPI registers go to initial state	Read the Message 0 of SPI register (see Table 19)	See Table 19,	
VPWR Undervoltage	RSTB is high state	All LSDx Off (Clear all LSDx duty cycle registers or current set point) + SPI fault flag (V_{PWR_UV})	1. Normal condition 2. Read diagnosis (V_{PWR_UV})	1. Normal condition 2. Turn on by SPI command (LSDx duty cycle or current set point)	
VPWR Overvoltage	RSTB is in high state	All LSDx Off (Clear all LSDx duty cycle registers or current set point) + SPI fault flag (V_{PWR_OV})	1. Normal condition 2. Read diagnosis (V_{PWR_OV})	1. Normal condition 2. Turn on by SPI command (LSDx duty cycle or current set point)	
Mismatch SB0800 MAIN-AUX OSC CLK	RSTB is in high state	SPI registers goes to initial state low except, see Table 27	Read RST_clk bit	No	
Temperature Warning	RSTB is in high state	SPI flag	1. Normal condition 2. Read diagnosis	No	
SPI Failure	RSTB is in high state	SPI flag (Fmsg)	Read diagnosis	No	
V_{PRE} 10 Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	(9)
V_{PRE} 12 Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	(9)
VINT_x Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	(9)
V_{cp_vpwr} Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	
Temperature Monitoring	RSTB is in high state	Send by SPI (ADC)	No	No	(9)
GND_D Supervision	RSTB is in high state	SPI flag only (FGND)	No	No	
GND_A Supervision; indirect detection by VCC5 or DOSV	RSTB is in high state	SPI flag only (VCC5_UV or DOSV_UV)	No	No	

Notes

7. If xxx_clr_flt is written “1” by SPI, all SPI flags are set “0”, so SW engineer has to read the SPI flag first and then write xxx_clr_flt to default value “0”.
8. SW engineering can monitor internal supply voltage in real time with ADC reading, and can use fail-safe function. If these ADC results are not in a certain range, uC can reset the SB0800 (see ADC section).
9. Fail-safe switch off until power is off

6.2 High-side driver

6.2.1 Function description

The high-side driver is intended to control the fail-safe switch for the overall solenoid path, and HD_G is controlled by the SPI command.

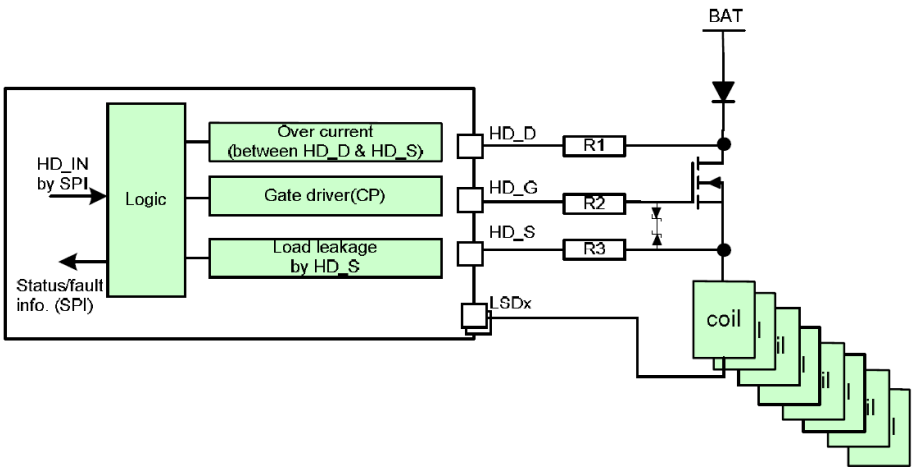


Figure 5. High-side driver

6.2.2 High-side driver and fault protection

6.2.2.1 Overcurrent

High-side driver protects the external n-channel power FET on HD_G in overcurrent conditions. The drain-source voltage of the FET on HD_G is checked if the high-side driver is switched on. If the measured drain-source voltage exceeds the overcurrent voltage threshold, the output of the overcurrent comparator is enabled. If the output of the comparator is active longer than the defined filter time, the output HD_G is switched off. Overcurrent detection logic has a masking time from hd_on turn-on against malfunctions on transient time. After switching off the power FET on HD_G by an overcurrent condition, the power FET can be turned back to a “normal state” by a SPI write 1 to the “HD_clr_flt” register, and then turned on by a SPI command.

6.2.2.2 Load leakage detection

Each time HD_G is turned on, the ILCdet current is sourced out of the HD_S pin for the time t_{HD_LC}, to check the external leakage current on the node in the application. The high-side switch on HD_G is turned on if the measured voltage is over the detection threshold. If this test fails, HD_G does not turn-on and the fault flag is set to high. The power FET can be turned back to a “normal state” only by a SPI write 1 to the “HD_clr_flt” register, and then turned on by a SPI command. When the power FET is switched off, the gate capacitance of the FET is discharged by a constant current, which is controlled fast and slow by a SPI command (HPD_sr).

6.2.2.3 External components of high-side driver

For protection, external resistors R_{HD_D}, R_{HD_G}, and R_{HD_S} are required (for example: R_{HD_D} = 100 Ω, R_{HD_G} = 100 Ω, R_{HD_S} = 100 Ω). The zener clamping is necessary to protect the gate and source. The zener chains are used for avalanche clamping and protection against transients.

Table 10. High-side driver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
HD_G						
V_{HD_ON}	HD_G switch-on voltage - with pd_on: PWMat 500 Hz, 50% duty cycle through the SPI • 5.5 V ≤ V_{PWR} < 6.0 V • 6.0 V ≤ V_{PWR} < 7.0V • 7.0 V ≤ V_{PWR} < 10 V • 10 V ≤ V_{PWR} < 36 V	V_{PWR}+ 4 V_{PWR}+5 V_{PWR}+7 V_{PWR}+10	— — — —	V_{PWR}+ 15 V_{PWR}+15 V_{PWR}+15 V_{PWR}+15	V	
V_{HD_OFF}	HD_G switch-off voltage	—	—	1	V	
t_{HD_ON}	Turn-on time - After t_{HD_LC}	—	—	1.4	ms	
$I_{HD\_OFF\_SLOW}$	Turn-off current slow - V_{HD_G} > 2.0 V. HPD_sr = 0	70	100	200	µA	
$I_{HD\_OFF\_FAST}$	Turn-off current fast - V_{HD_G} > 2.0 V, HPD_sr = 1	1.0	2.0	4.5	mA	
HD_S						
$I_{LEAK\_HD\_SRC}$	Leakage current - 0 ≤ V_{HD_S} ≤ 36 V, 6.0 ≤ VPWR ≤ 36 V	—	—	50	µA	
HD_D						
$L_{LEAK\_HD\_DRN}$	Leakage current - VCC5 = DOSV = 0 V, HD_D = PD_D = V_{PWR} = 36 V	—	—	10	µA	
Overcurrent detection						
V_{HD_OC}	Overcurrent detection threshold - V_{HD_D}-V_{HD_S}, R_{DRN}, R_{SRC} = 100 Ω	-15%	1.0	+15%	V	
Load leakage current detection						
$I_{HD\ LC}$	HD_S source current	—	1.5	—	mA	

6.3 Pump motor pre-driver

6.3.1 Function description

This module is designed for pump motor predrivers, a maximum of 500 Hz PWM is possible. The pump motor pre-driver can be driven by a SPI command (pd_on) or through the ADIN1 pin by selecting Adin1_dis bit at “1”.

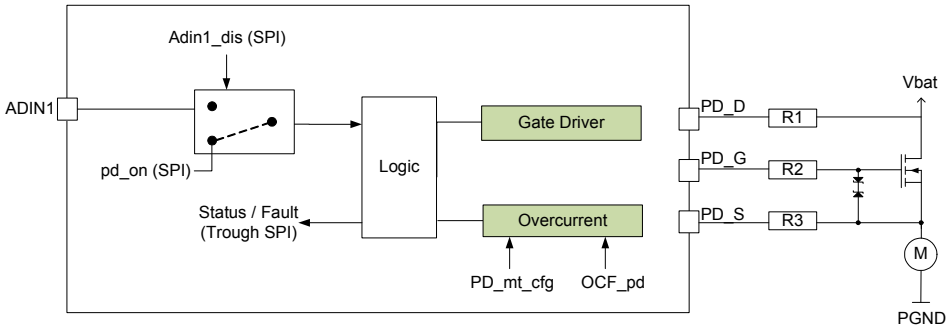


Figure 6. Pump motor predriver

6.3.2 Fault Detection

6.3.2.1 Overcurrent

The pump pre-driver protects the external n-channel power FET on PD_G in overcurrent conditions. The drain-source voltage of the FET on PD_G is checked if the high-side predriver is switched on. If the measured drain-source voltage exceeds the overcurrent voltage threshold, the output of the overcurrent comparator is enabled. If the output of the comparator is active longer than the defined filter time, the output PD_G is switched off. Overcurrent detection logic has a masking time from pd_on turn-on against malfunctions in transient time. The masking time and filter time of the pump predriver is controllable by the SPI bit (See SPI and data register). After switching off the power FET on PD_G by an overcurrent condition, the power FET can be turned back to a “normal state” by a SPI write 1 to the “PD_clr_flt” register, and then turned on by a SPI command.

When the power FET is switched off, the gate capacitance of the FET is discharged by a constant current, which is controlled fast and slow by a SPI command (HPD_sr).

6.3.2.2 External components of pump predriver

Protection of the resistors R_{PD_D}, R_{PD_G}, and R_{PD_S} is required (for example: R_{PD_D} = 2.0 kΩ, R_{PD_G} = 100 Ω, R_{PD_S} = 2.0 kΩ). Zener clamping is necessary to protect the gate and source. The zener chains are used for avalanche clamping and protection against transients.

Table 11. Pump motor predriver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
PD_G						
V_{PD_ON}	PD_G switch-on voltage - with pd_on: PWM at 500 Hz, 50% duty cycle through the SPI, 16 nF between PD_G & GND. pd_on = 1 without PWM • 5.5 V ≤ VPWR < 6.0 V • 6.0 V ≤ VPWR < 7.0V • 7.0 V ≤ VPWR < 10 V • 10 V ≤ VPWR < 36 V	V_{PWR}+ 4 V_{PWR}+5 V_{PWR}+7 V_{PWR}+10	— — — —	V_{PWR}+ 15 V_{PWR}+15 V_{PWR}+15 V_{PWR}+15	V	
V_{PD_OFF}	PD_G switch-off voltage - pull-up current < 20 µA	—	—	1	V	
t_{PD_ON}	Turn-on time	—	0.5	—	ms	
$I_{PD\_OFF\_SLOW}$	Turn-off current slow - PD_G > 2.0 V. HPD_sr = 0	70	100	200	µA	
$I_{PD\_OFF\_FAST}$	Turn-off current fast - PD_G >2.0 V, HPD_sr = 1	1.0	2.0	4.5	nA	
PD_S						
$I_{LEAK\_PD\_SRC}$	Leakage current - 0 ≤ VPD_src ≤ 36 V, 6.0 ≤ VPWR ≤ 36 V	—	—	10	µA	
PD_D						
$I_{LEAK\_PD\_DRN}$	Leakage current - VCC5 = DOSV = 0 V, HD_D = PD_D = VPWR = 36 V	—	—	10	µA	
Overcurrent detection						
V_{PD_OC}	Overcurrent detection threshold - V_{PD_D} - V_{PD_SRC}, R_{DRN}, R_{SRC} = 2.0 kΩ	-15%	1.0	+15%	V	
t_{PD_OC1}	Overcurrent detection filter time - OCF_pd = 0	—	T2	—	µs	
t_{PD_OC2}	Overcurrent detection filter time - OCF_pd = 1	—	4*T1	—	µs	

6.4 Low-side driver

6.4.1 Functional description

The SB0800 is designed to drive inductive loads in low-side configuration. All four channels are monitored by logic and faults are individually reported by the SPI. All external wiring to the loads and supply pins of the device are controlled. The device is self-protected against short-circuit and overtemperature at the outputs.

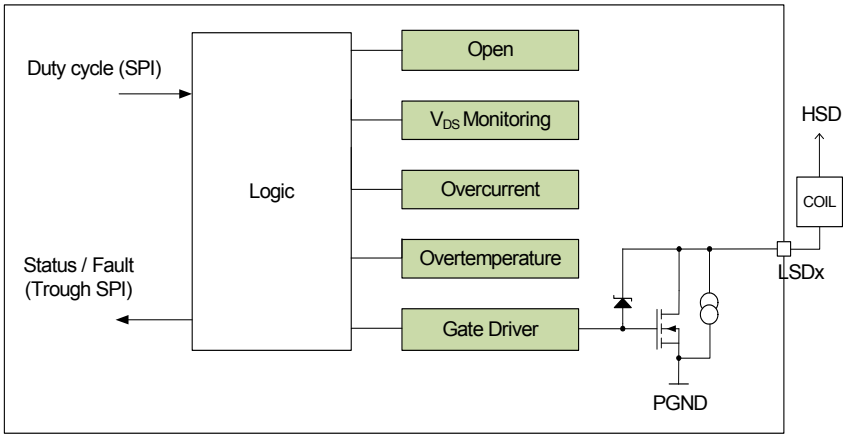


Figure 7. PWM low-side driver

Channel 1 to 4 can work either as current regulator or as PWM. When Channels 1 to 4 work as a current regulator, freewheeling diodes must be connected. Each channel comprises an output transistor, a predriver circuit, a diagnostic circuitry, and a current regulator. The SPI register defines the target output current. The output current is controlled through the output PWM of the power stage. The LSD1-4 current slopes are controlled by a SPI command to reduce switching loss.

The four power outputs consist of DMOS-power transistors with open drain outputs. The output transistor is equipped with an active clamp to limit the voltage at its output during turn-off with inductive loads. When the external fly-back diode is connected, the current re-circulation executes via the diode to the battery. When the diode is not connected, the PWM driver is equivalent to a digital driver. In those conditions, the inductive load forces the output voltage to increase until the voltage at the output is such that the output transistor turns on again. This lasts until the inductor current becomes zero. At that moment, the output transistor turns off. The predriver is in charge of applying the necessary voltage on the output transistor gate to minimize the On-resistance of the output switch.

The duty cycle of PWM low-side drivers is programmed via an 8-bit SPI message. The duty cycle between 0% and 100% can be selected and the LSB of the 8 bits is weighted with an 0.39% duty. Each channel has an 8-bit SPI register of PWM duty cycle.

The PWM low-side driver uses each channel as a digital low-side switch.

PWMx duty cycle = 1111 1111 - Digital low-side switch ON (conducting)

PWMx duty cycle = 0000 0000 - Digital low-side switch OFF

The SB0800 provides interleaved phase shift switching to minimize switching noise of the solenoid coil. Each LSD1 to 4 have this cycle.

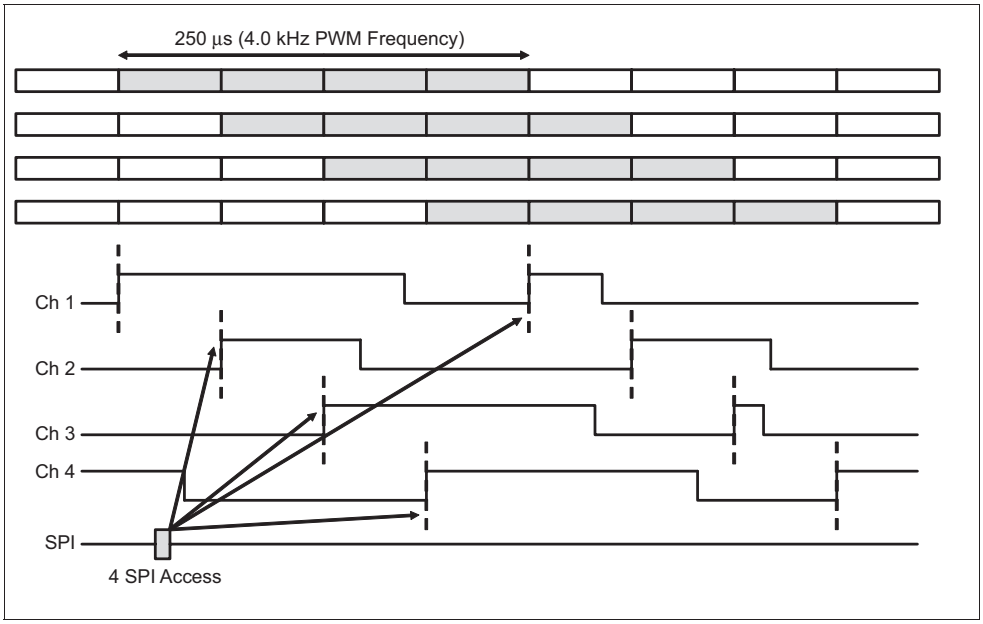


Figure 8. PWM valve control interleave

Table 12. Low-side driver electrical characteristics

V_{PWR} = 6.0 to 36 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output						
R_{ON_LSD14}	On Resistance Channel 1 to 4: CR • T_J = 125 °C; 9.0 V ≤ V_{PWR} ≤ 36 V; I_{LOAD} = 2.0 A	—	—	0.255	Ω	
$R_{ON\_LSD14\_E}$	On Resistance Channel 1 to 4: CR (extended mode) • T_J = 125 °C; 5.5 V ≤ V_{PWR} ≤ 9.0 V; I_{LOAD} = 2.0 A	—	—	0.33	Ω	
I_{LEAK_LSD}	Drain Leakage Current • LSD = 36 V	—	—	10	µA	
V_{CL_LSD}	Active Clamp Voltage	—	38	45	V	
Timings						
t_{R_CR1} t_{F_CR1}	Rise Time/Fall Time • 10% to 90%, I_{LOAD} = 1.0 A, V_{PWR} =24 V; no capacitor didt = 0 (SPI bit)	1.0 0.1	1.7 1.35	3.0 3.0	µs	
t_{R_CR2} t_{F_CR2}	Rise Time/Fall Time • 10% to 90%, I_{LOAD} = 1.0 A, V_{PWR} = 24 V; no capacitor didt = 1 (SPI bit)	0.05 0.1	0.5 1.0	1.0 3.0	µs	
t_D on CR t_D off CR	Turn on/off Delay Time • Digital 1 to 10% or 90%, I_{LOAD} = 1.0 A, V_{PWR} = 24 V, no capacitor	0.0	—	3.0	µs	(10)

Table 12. Low-side driver electrical characteristics (continued)

V_{PWR} = 6.0 to 36 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Timings						
LF_PWM	Output PWM frequency for LSD1-4 • LF_PWM xx = 111 • LF_PWM xx = 110 • LF_PWM xx = 101 • LF_PWM xx = 100 • LF_PWM xx = 000 (default) • LF_PWM xx = 011 • LF_PWM xx = 001 • LF_PWM xx = 010	-20%	 3.0 3.2 3.4 3.6 3.9 4.2 4.5 5.0	20%	kHz	
0000 0000 0000 0001 … 1111 1110 1111 1111	PWM Duty Cycle Programming (8-bits) • Can be used for digital low-side driver	— — — — —	OFF 0.39 — 99.61 ON	— — — — —	%	

Notes

10. Digital: internal digital signal delivered by interleave synchronization block. See Figure 8.

6.4.2 LSD1 to LSD4 current regulation driver

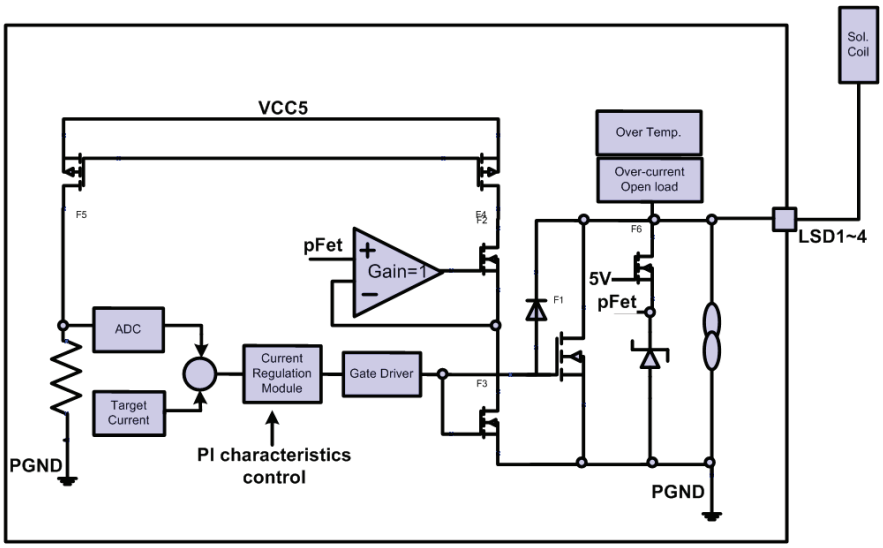


Figure 9. PWM low-side driver (current regulated)

The load current is sensed by an internal low-side sense FET and digitized by an internal A/D converter. The target value of the current is given SPI messages. A digital current regulation circuitry compares the actual load current with the target current value and steers the duty cycle of the low-side power switch. The PI regulator characteristic can be adjusted via the SPI.

6.4.2.1 Target current

Each current regulator channel has its own 10-bit target current register. The LSB of the 10 bits is weighted with 2.2 mA. A zero value disables the power stage of the respective channel. A new target current is instantaneously passed to the settling time, which is the settling of the new current value.

PWMx target current value = 00 0000 0000 → 0 mA

PWMx target current value = 00 0000 0001 → 2.2 mA

...

PWMx target current value = 11 1111 1110 → 2.248 A

PWMx target current value = 11 1111 1111 → 2.250 A

CR_DIS12/34	CR_fb	Mode	LSD1-4 duty cycle (8-bit) or current read (10-bit)
0	0	current regulation	Read current target (to check SPI write)
0	1	current regulation	Read output duty cycle value for gate driver.
1	0	PWM	Read programmed PWM duty cycle (to check SPI write)
1	1	PWM	Read hardware ADC current value

6.4.2.2 Current measurement

The output current is measured during the “ON’ phase of the low-side driver. A fraction of the output current is diverted and (using a “current mirror” circuit) generates across an internal resistance a voltage relative to ground, this being proportional to the output current.

6.4.3 PI characteristics

Digital PI-regulator with the Transfer function is programmed via the SPI register.

Transfer function: $\frac{KI}{z-1} + KP$

The integrator feedback register I charac bits define the regulation behavior of all channels. The default value is 1/8. Both current regulators remain idle until a non-zero value in I charac was programmed. A high proportional feedback value accelerates the regulator feedback and provides a faster settling of the regulated current after disturbances like battery voltage surge.

Table 13. Duty cycle descriptions

The duty cycle of PWM output is clamped minimum by options and maximum 100% (see 6.10, “SPI and data register").

Option	LLC<1>	LLC<0>	Minimum duty cycle
0	0	0	10% • the measurement is done at $t_{ON}/2$ by consequence • the regulation current will be set at $t_{ON}/2$
1	0	1	3.12% • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle

Table 13. Duty cycle descriptions

The duty cycle of PWM output is clamped minimum by options and maximum 100% (see 6.10, “SPI and data register").

Option	LLC<1>	LLC<0>	Minimum duty cycle
2	1	0	3.12% + forced min duty cycle to 1.56% every two cycles • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle • for a duty cycle set at 1.56%, no measurement is done
3	1	1	3.12% + skip min duty cycle every two cycles • for a duty cycle > 10%, the measurement is done at $t_{ON}/2$ by consequence the regulation current will be set at $t_{ON}/2$ • for a duty cycle 3.2% < DC < 10%, the measurement is done at $t_{ON}/2$ for 10% of duty cycle up at t_{ON} for 3.2% of duty cycle • no measurement is done during the skipping mode

If the target current value is not reached within the regulation error delay time of t_{CR_ERR}, the flag of the SPI register “LSDx_crer” is set to high. The current regulation loop is still running and tries to regulate at the target. Because it is not at the target, the duty cycle is either 100%, or minimum duty cycle by option. LSDx_crer error detection has no effect on the driver, only SPI fault reporting. The microcontroller can detect the fault through the SPI (LSDx_crer bit + ADC current reading), and shutdown the driver by sending 0 target current. Set Current – ADC result > “error threshold” during t_{CR_ERR} then LSDx_crer is set to 1.

This flag is latched & can be reset by the SPI read (LSDx_crer). Each of the four current regulation low-side drivers can be used as a PWM low-side switch. CR_disxx flag is enabled HIGH. The 8 MSB bits of the target current message are the PWM duty cycle. The first duty is controlled by the SPI bit FDCL (See SPI and data register).

Table 14. LSD1 to LSD4 current regulation driver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current regulation						
0000 0000 0000 0001 ... 1111 1111	Target current programming (10-bits)	— — — —	OFF 2.2 ... 2.25	— — — —	mA A	
I_{CR_DEV}	Maximum regulation deviation • 0 mA ≤ I_{TARGET} < 50 mA, includes ADC error • 50 mA ≤ I_{TARGET} < 100 mA, includes ADC error • 100 mA ≤ I_{TARGET} < 250 mA, includes ADC error • 250 mA ≤ I_{TARGET} < 400 mA, includes ADC error • 400 mA ≤ I_{TARGET} < 2.25 A, includes ADC error	— — — — —	— — — — —	65 50 25 ±10 ±2.0	mA %	(11)

Notes

11. Maximum regulation deviation performances noted in the table depend on external conditions (V_{PWR}, load (R,L)).

6.5 Low-side driver for resistive load

6.5.1 Power output stages

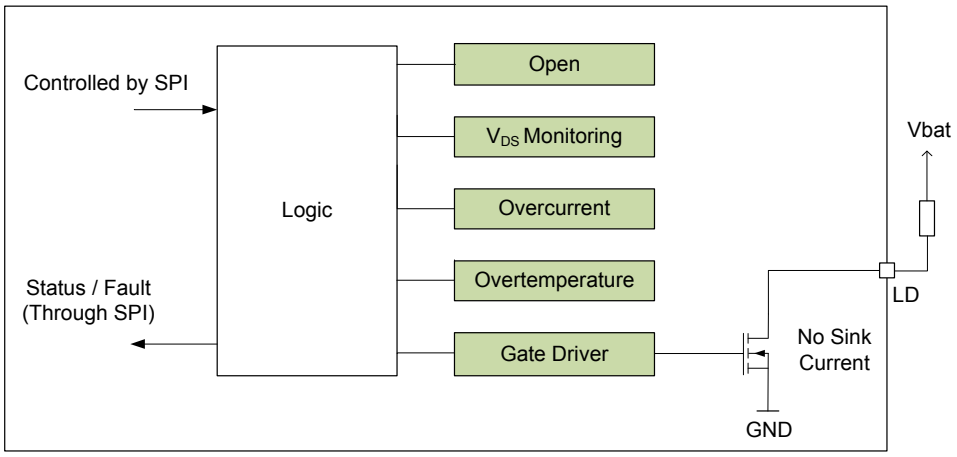


Figure 10. Low-side driver for resistive load diagram block

The low-side driver consists of DMOS-power transistors with open drain output. The low-side driver can be driven by SPI commands or by a MCU through the ADIN2. The low-side driver is composed of an output transistor, a predriver circuit, and diagnostic circuitry. The predriver applies the necessary voltage on the output transistor gate to minimize the On resistance of the output switch. To avoid leakage current path, LD has no sink current.

Table 15. Low-side driver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output LD						
R_{ON_LD}	On Resistance for LD • T_J = 125 °C, 6.0 V ≤ V_{PWR} ≤ 36 V	—	—	14	Ω	
	DC Current Capability	—	—	20	mA	
I_{LEAK_LD}	Drain Leakage Current • V_{PWR} = 0, V_{CC5} = 0, LD = 30 V, no sink current	—	—	5.0	µA	
Timings						
$t_{D\_ON\_LD}$	Turn On Delay Time for LD	—	—	1.0	µs	(12)
$t_{D\_OFF\_LD}$	Turn Off Delay Time for LD	—	—	1.0	µs	(12)

Notes

12. From Digital Signal to 50% (turn ON) or 50% (turn OFF). R_L = 1.0 kΩ, V_{PWR} = 30V, no capacitor

6.5.2 Fault detection

Open load

An open condition is detected when the LD output is below the threshold OP_{LD} for the defined filter time t_{OP_LD}, the fault bit is set ld_OP (SPI error flag only). This function only operates during the off state.

V_{DS} state monitoring

The V_{DS} state monitoring gives real time state of LD drain voltage vs OP_{LD} voltage. This signal is filtered and sent through the SPI vds_ld bit. If the V_{DS} voltage is higher than OP_{LD} with a filter time (T1), vds_ld is set to “1”.

Overcurrent

When the current is above the overcurrent threshold OC_{LD} for the defined filter time t_{OC_LD}, the driver is switched off, a SPI fault bit ld_OC is set, and the turn-on SPI command is cleared. The driver can be returned to the “normal state” by a SPI write “1” to “LD_clr_flt”, then turned on by a SPI command (LD_on).

Overtemperature

When the temperature is above the overtemperature threshold OT_{LD} for the defined filter time t_{OT_LD}, the driver is switched off, a SPI fault bit ld_OT is set, and the turn-on SPI command is cleared. The driver can be returned to the “normal state” when the temperature returns to the normal state, a SPI write “1” to “LD_clr_flt”, then turning on a SPI command (LD_on).

Table 16. Low-side driver electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Overcurrent shutdown						
OC_{LD}	Overcurrent Shutdown Threshold Current for LD	—	100	—	mA	
t_{OC_LD}	Overcurrent Shutdown Filter Time	—	T1	—	µs	
Open load detection						
OP_{LD}	Open Load Detection Threshold (also used for V_{DS} monitoring)	—	2.0	—	V	
t_{OP_LD}	Open Load Detection Filter Time	—	T2	—	µs	
V_{DS} monitoring						
t_{VDS_LD}	V_{DS} State Filter Time (rise & fall edge filter time)	—	T1	—	µs	
Overtemperature shutdown						
OT_{LD}	Overtemperature Detection Threshold	180	195	210	°C	
t_{OT_LD}	Overtemperature Detection Filter Time	—	T1	—	µs	

6.6 Analog to digital converter (x3ch)

ADC is referenced to VCC5 voltage and converts the voltage on 10 bits. It is used to read the following voltages:

- Three analog input pins: ADINx
- Internal voltage supplies (VINT_A, VINT_D, V_{PRE10}, V_{PRE12}, V_{CP_VPWR})
- Average temperature of die, which is used by the temperature warning detection circuit (TEMP). Refer to the SPI Message Structure, Message #9.
- Allows to read the current drain by the LSD1-4 in PWM mode.

Also, it is possible to use ADIN1 and / or ADIN2 to control respectively the motor pump and / or the low-side driver for resistive load directly by the MCU.

Table 17. Direct control of pump and low-side

Adin1_dis	Pump control
0	Pd_on bit (SPI command)
1	By MCU
Adin2_en	**Low-side for resistive load control**
0	By MCU
1	Ld_on (SPI command)

Table 18. ADC electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
ADC						
A_{DC_ERR}	Total Error - 0 < ADINx < VCC5	—	3	—	LSB	(13)
t_{CONV}	Conversion Time	—	6.6	—	µs	
t_{RFT}	Refresh Time - min ADC update time; shorter than 1.0 ms	—	100	—	µs	
ADINx						
I_{ADI_LK}	Input Leakage Current - 0 < ADINx < VCC5	-10.0	—	10.0	µA	
C_{ADI_CAP}	Input Capacitance	–	—	30	pF	
Internal voltage						
$A_{D\_VINT\_A}$	Voltage of internal analog regulator	440	512	590	LSB	
$A_{D\_VINT\_D}$	Voltage of internal digital regulator	440	512	590	LSB	
A_{D_VPRE10}	V_{PRE10} - ADC ratio =V_{PRE10}/3.3, 9.0 < V_{PWR} < 36 V	400	600	800	LSB	
A_{D_VPRE12}	V_{PRE12} - ADC ratio = V_{PRE12}/3.0, 9.0 < V_{PWR} < 36 V	590	790	980	LSB	
A_{D_VCP}	V_{CP}-V_{PRWR} - ADC ratio = V_{CP} - V_{PWR}/4.0, 9.0 < V_{PWR} < 36 V	330	—	810	LSB	
Temperature reading						
A_{D_TEMP25}	Voltage at 25 °C	—	717	—	LSB	
$A_{D\_DEV\_TEMP}$	deviation with 1.0 °C increments	—	-2.0	—	LSB/°C	

Notes

13. If ADINx voltage is between VCC5 to max_rating, the ADC value does not change. Also between VCC5 min and GND, the ADC value does not change.
14. SW engineer can monitor internal supply voltage in real time with ADC, SPI reading, and can use fail-safe function.

6.7 High-side

6.7.1 Function description

The device has one high-side, having an integrated high-side switch, controlled by the SPI command HS_on. It allows connecting and disconnecting loads like voltage dividers from the supply line, to reach low quiescent current of the total ECU or to driver small size relay driver.

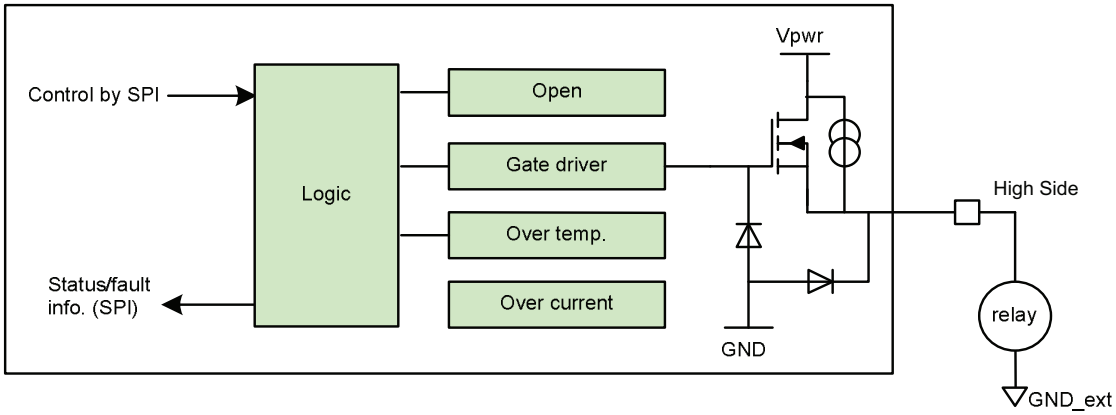


Figure 11. High-side driver

6.7.2 Fault detection

6.7.2.1 Ground shift

With a 2.0 V GND shift on the external relay coil (50 Ω), 30 mA could flow through the high-side output (diode between the SB0800_gnd & the high-side output) without damage to the SB0800 (see Figure 11).

6.7.2.2 Open load

An open condition is detected when the high-side output is higher than the threshold OP_HS for the defined filter time t_{OP_HS}. The fault bit is set HS_op (SPI error flag only). The function only operates during the off state.

6.7.2.3 V_{DS} state monitoring

The V_{DS} state monitoring gives the real time state of HS drain voltage vs. OP_HS voltage. This signal is filtered and sent through the SPI vds_HS bit. If the HS output is lower than OP_hs with a filter time (T1), vds_HS is set to “1”.

6.7.2.4 Overcurrent

When the current is above the overcurrent threshold OC_hs for the defined filter time t_{OC_HS}, the driver is switched off, a SPI fault bit HS_oc is set, and the turn-on SPI command is cleared. The driver can be turned back to a “normal state” by a SPI write “1” to “HS_clr_flt”, then a turn on by the SPI command (HS_on).

6.7.2.5 Overtemperature

When the temperature is above the overtemperature threshold OT_hs for the defined filter time t_{OT_HS}, the driver is switched off, a SPI fault bit HS_ot is set, and the turn-on SPI command is cleared. The driver can be turned back to a “normal state” when the temperature returns to a normal state, a SPI write “1” to “HS_clr_flt”, and then a turn on by the SPI command (HS_on).

Table 19. High-side electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output HS						
R_{ON_HS}	On resistance • T_J = 125 °C, 9.0 V ≤ V_{PWR} ≤ 36 V • T_J = 125 °C, 6.0 V ≤ V_{PWR} ≤ 9.0 V	— —	— —	1.0 1.5	Ω	
	DC current capability	—	270	—	mA	
I_{LEAK_HS}	Drain leakage current - V_{PWR} = 14 V, V_{CC5} = 0	—	—	2.0	µA	
$V_{\_BVDSS\_HS}$	Breakdown Voltage	40	—	—	V	
Timing						
$t_{D\_ON\_HS}$/ $t_{D\_OFF\_HS}$	Turn on/off delay time	—	—	20	µs	(15)
Overcurrent shutdown						
$OC_{\_HS}$	Overcurrent shutdown threshold current	—	650	—	mA	
t_{OC_HS}	Overcurrent shutdown filter time - measured by sense FET	—	T1	—	µs	
Open load detection						
$OP_{\_HS}$	Open load detection threshold - include GND shift = 2.0 V, also used for V_{DS} monitoring	—	4.0	—	V	
V_{DS} monitoring						
t_{VDS_HS}	V_{DS} state filter time	—	T1	—	µs	(16)
Overtemperature shutdown						
$OT_{\_HS}$	Overtemperature detection threshold	180	195	210	°C	
t_{OT_HS}	Overtemperature detection filter time	—	T1	—	µs	

Notes

15. From digital signal to 50% (turn ON) or 50% (turn OFF). R_L=1.0 KΩ, V_{PWR} = 30 V, no capacitor
16. Used open load detection comparator rise & fall edge filter time

6.8 Monitoring module

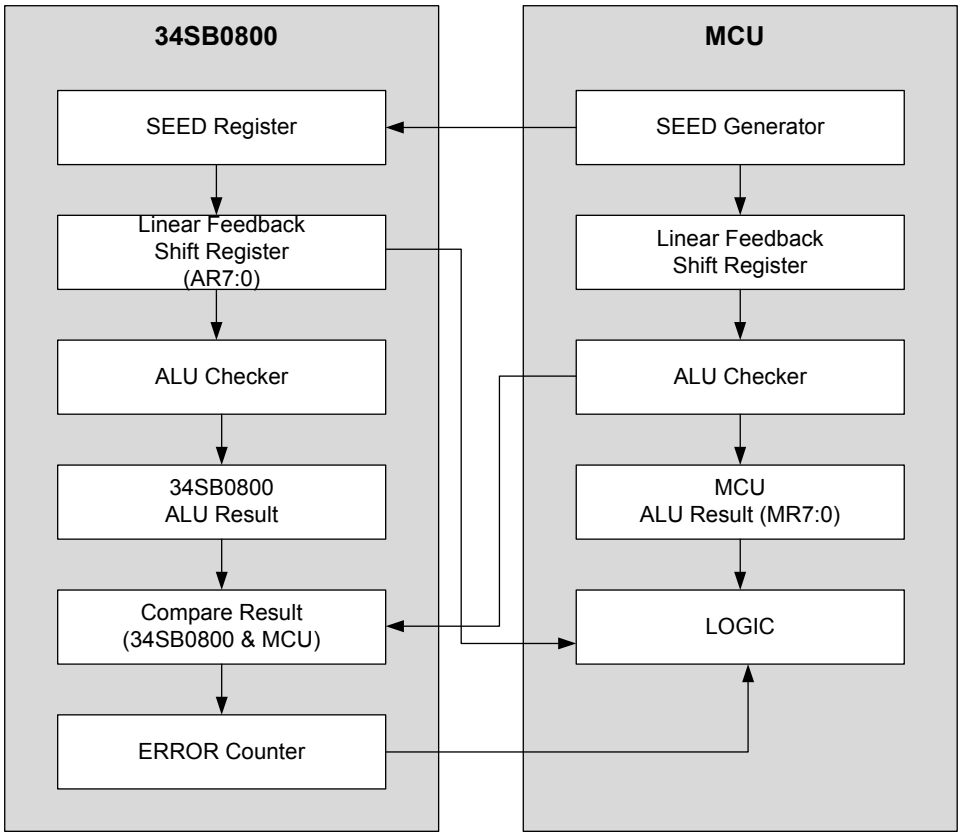


Figure 12. Block diagram of SB0800 monitoring module and MCU

The monitoring module in SB0800 works independently from the MCU functionality. The SEED is an 8-bit word, initializing the monitoring module and transferred by the SPI. The MCU generates the SEED, and must fetch and send correct calculation results (MR7:0) to the SB0800 monitoring module within a defined time window. The SB0800 monitoring module confirms the result is sent and correct in the time window. ALU checker results of SB0800 monitoring module are transferred to the MCU by the SPI. The monitoring module also calculates the expected correct result, which is compared to the actual result from MCU.

The result from MCU is an 8-bit MR. The 8 bits are sent to the monitoring module via the SPI interface. The monitoring cycle time starts by a write of MR, with the next MR written within in a fixed time window. A new cycle time is started automatically by a write of MR.

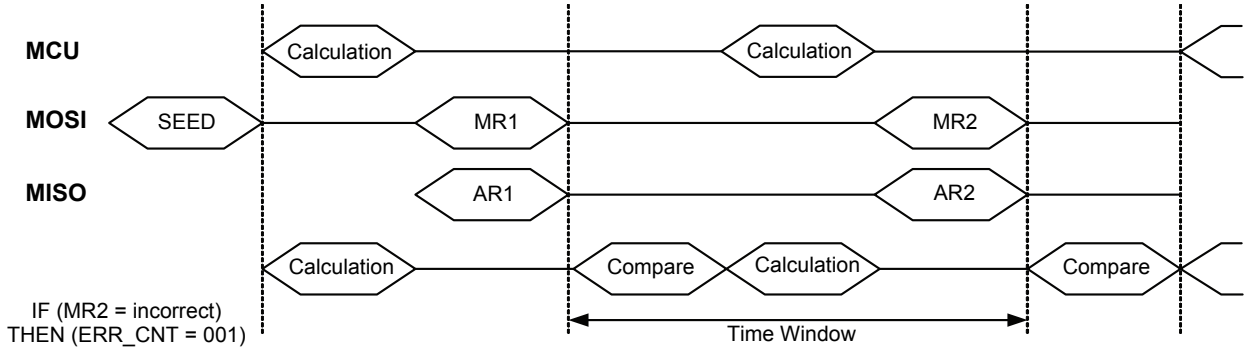


Figure 13. Timing diagram of SB0800 monitoring module and MCU

ERR_CNT is a 3-bit counter. An incorrect result leads to incrementing the ERR_CNT by one, and a correct result leads to decrementing by one. The ERR_CNT 3-bit can be read by the SPI interface.

6.8.1 ERR_CNT behavior

Reset with (RSTB pin = “Low”)

IF (ERR_CNT ≥ 101) THEN (RSTB pin = “Low”) AND (MON_CNT reset)
IF (ERR_CNT ≤ 100) AND (MR = incorrect) THEN (ERR_CNT = ERR_CNT+1)
IF (ERR_CNT = 000) AND (MR = correct) THEN (ERR_CNT = ERR_CNT)
IF (001 ≤ MON_CNT ≤ 100) AND (MR = correct) THEN (ERR_CNT = ERR_CNT - 1)

The SB0800 monitors the time window of the SPI message #18 without writing to the SEED. The time window (t_{WD}) counter starts with the RSTB pin rising edge. The time window (t_{WD}) counter is reset with the SPI message #18 (with valid parity bit) and restart. If the SPI message #18 (with valid parity bit) is not transferred from the MCU before the time window (t_{WD}) end period, the RSTB pin goes to a LOW state for the duration time of t_{RSTB_REC} and the RST_wd flag is set “High”. When RSTB is at a low state (internal, external), the time window (t_{WD}) counter is reset to zero.

6.8.2 Linear feedback shift register (LFSR)

Both the SB0800 monitoring module and the MCU have LFSR for a pseudo-random number generator of ALU checker inputs. LFSR works in parallel with the SB0800 and MCU. LFSR is initialized by the SPI with a SEED 8-bit, then each MR write command generates a new pseudo-random number. The FF hex-value cannot be used for the SEED.

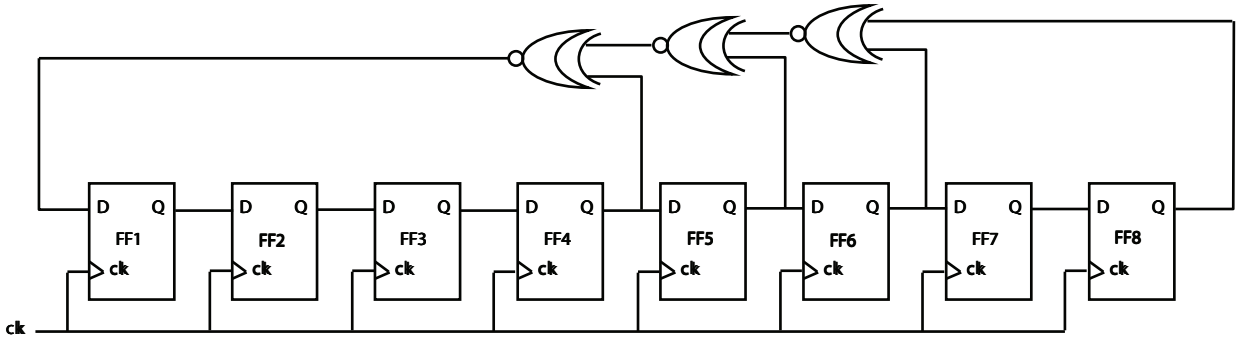


Figure 14. Diagram of linear feedback shift register (LFSR)

6.8.3 ALU checker

Both the SB0800 monitoring module and the MCU have an ALU checker. The ALU checker work in parallel with the SB0800 and MCU. The 8-bit input of the ALU checker is the 8-bit output of LFSR. The ALU checker proceeds on five sequential calculations.

Multiplier pseudo-random value by fix value 4
Adder output multiplier by fix value 6
Subtract previous value with fix value 4
Inverting previous value: bitwise complement
Divider previous value by fix value 4

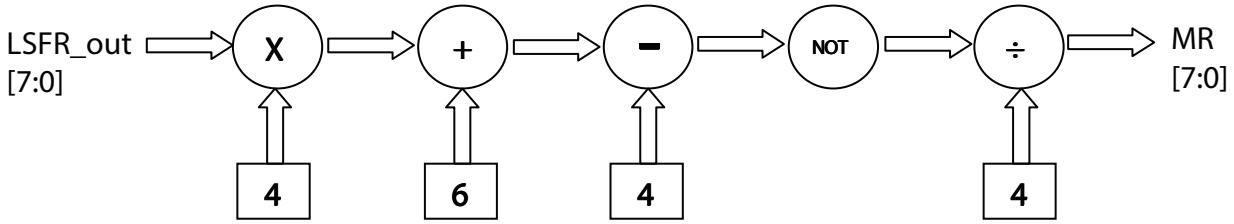


Figure 15. Diagram of ALU checker

Table 20. Monitoring module electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
MCU monitoring module						
t_{WD}	Timing window for Watchdog	10	—	60	ms	
t_{VAM}	Variation of the Watchdog Window Timing	60	75	90	ms	

Notes

17. The maximum setting window for the watchdog can be decreased to a SPI timing access. The range given in Table 33 shows the typical use case.

Sequence examples to run the watchdog:

Check when the pin reset goes high.

1st command: send the message 0: 0x00 to clear flags

2nd command: send the message 0: 0x00 to reinitialize the seed value. Then, no need to send the seed value again

3rd command: message 18: send the corresponding MR value calculated due the the seed value

4th: send the message desired

Note: The message 18 (MR value) should be sent according the the tWD timing

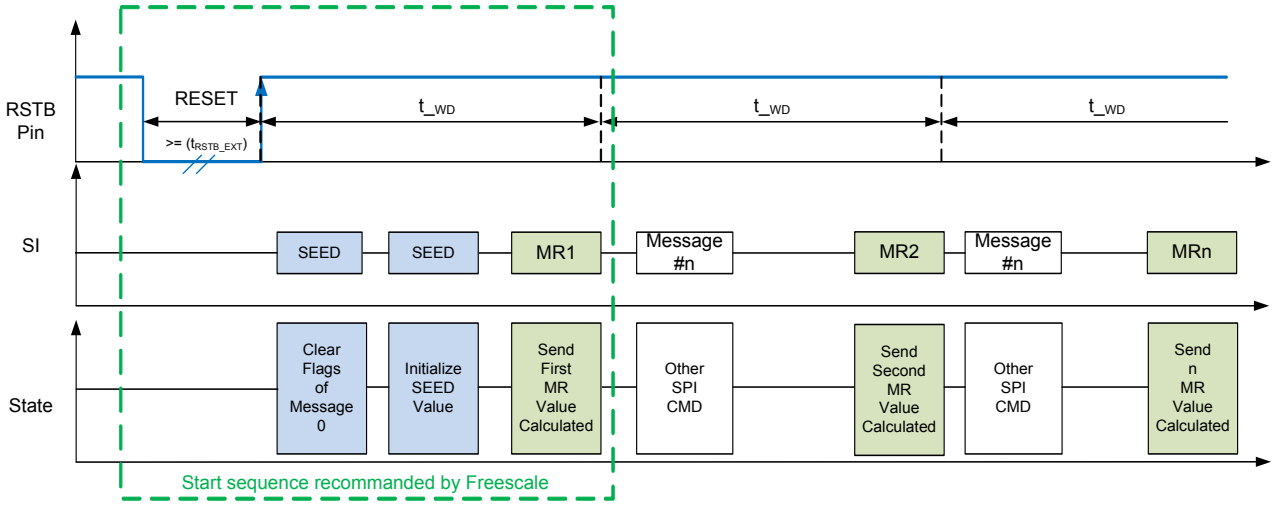


Figure 16. Watchdog sequence example

6.9 Supervision

Table 21. Reaction to supply fault and reset condition

Event	RSTB	LSDx	HD	PD	LD	SPI	Notes
Normal mode: After RSTB rising edge, No fault	High	Normal	Normal	Normal	Normal	Normal	
VINT_x undervoltage	Low (output)	OFF	OFF	OFF	OFF	SPI register go to initial state Low except for Vint_uv which is reset to 1. After first read of Vint_uv, it is set back to 0.	(18)
Clock fail reset	Low (output)	OFF	OFF	OFF	OFF	SPI registers go to initial state Low except for Vint_uv unchanged & RST_clk which is set to 1. After first read of RST_clk, it is set back to 0.	(18)

Table 21. Reaction to supply fault and reset condition (continued)

Event	RSTB	LSDx	HD	PD	LD	SPI	Notes
DOSV undervoltage	Low (output)	OFF	OFF after $t_{LSDx\_HD\_G}$	OFF	OFF	SPI register go to initial state except reset flag (Vint_uv, VCC5_uv, DOSV_uv, RST_wd, RST_alu, RST_ext, RST_CLK) and hd_on (tLSDx_HD_G timing).	(18)
VCC5 undervoltage	Low (output)	OFF	OFF after $t_{LSDx\_HD\_G}$	OFF	OFF	SPI register go to initial state except reset flag (Vint_uv, VCC5_uv, DOSV_uv, RST_wd, RST_alu, RST_ext, RST_CLK) and hd_on (tLSDx_HD_G timing).	(18)
Watchdog fault or ALU fault	Low during t_{RSTB_REC} (output)	OFF	OFF after $t_{LSDx\_HD\_G}$	OFF	OFF	SPI register go to initial state except: - reset flag (Vint_uv, VCC5_uv, DOSV_uv, RST_wd, RST_alu, RST_ext, RST_CLK) - clear flag bits - hd_on (tLSDx_HD_G timing). - MR - Seed Note: P_charac and I_charac bits are reset in case of Watchdog fault or ALU fault, but SPI read returns the direct SPI write content.	(18)
External Reset	Low (input)	OFF	OFF after $t_{LSDx\_HD\_G}$	OFF	OFF	Same SPI behavior as Watchdog fault or ALU fault except seed. SPI register go to initial state except: - reset flag (Vint_uv, VCC5_uv, DOSV_uv, RST_wd, RST_alu, RST_ext, RST_CLK) - clear flag bits - hd_on (tLSDx_HD_G timing). - MR Notes: P_charac and I_charac bits are reset in case of external reset, but SPI read returns the direct SPI write content. Watchdog circuit Seed register (written by SPI write Message #0) is reset by External reset event and impossible to write to unless External reset flag is cleared. In the case of External reset, two identical SPI write Message #0 should be executed to reinitialize Seed register. First SPI Message #0 will clear External reset flag and second SPI Message #0 will finally reinitialize Seed register. In application, writing seed is preferred after checking if RST_ext is 1. (Only External Reset flag is to block writing Seed.)	
VPWR overvoltage	No effect	OFF	OFF after $t_{LSDx\_HD\_G}$	On	No effect	Following SPI registers go to initial state Low: A. LSDx Duty cycle or current set point. B. hd_on	
VPWR undervoltage	No effect	OFF	OFF after $t_{LSDx\_HD\_G}$	OFF	No effect	Following SPI registers go to initial state Low: A. LSDx Duty cycle or current set point. B. hd_on	

Notes

18. State defines for the duration of the fault and the following reset recovery time period.

Restart conditions:
SPI write message #0 has first to be executed to clear any reset or fault flags. Then new SPI command can be sent.

Table 22. Start point of reset recovery time

Fault mode	Start point of t_{RST_REC}
VINT_A or VINT_D_uv or VCC_uv or DOSV_uv	Come back normal voltage of all voltages
Watchdog or ALU fault	Fall edge of RSTB pin

6.9.1 Additional safety functions

6.9.1.1 VINT_A or VINT_D undervoltage supervision

The SB0800 uses an internal supply for analog functions (VINT_A) and digital functions (VINT_D). The supply voltage VINT_A and VINT_D are supervised for undervoltage. When the voltage becomes lower than each threshold VINT_A_uv and VINT_D_uv, the RSTB pin is asserted low after detection filter time (t_{VINT}). This reset state will continue until the voltage at pin VINT raises again. And if VINT becomes higher than each threshold VINT_A_uv and VINT_D_uv for same filter time (t_{VINT}), the RSTB Pin goes high after reset recovery time (t_{RST_REC}) and the related flag of the SPI register is set to high. For stabilization the internal supply VINT_A & VINT_D requires external capacitors. Two band-gaps are included in the SB0800, one is for the voltage reference and the other is for the diagnostic. The VINT_A and VINT_D voltages are sending through the SPI.

6.9.1.2 VCC5 supervision

See Table 21 Reset condition and reaction.

6.9.1.3 DOSV supervision

The supply voltage DOSV is supervised for undervoltage. When the voltage at pin DOSV becomes lower than DOSV_uv, the RST pin is asserted low after detection filter time (t_{VDUV}). This reset state will continue until the voltage at pin DOSV raises again. And if DOSV becomes higher than (DOSV_uv) for same filter time (t_{VDUV}), the RSTB Pin goes high after reset recovery time (t_{RST_REC}) and the related flag of the SPI register is set to high.

The P53_CFG pin decides the DOSV pin undervoltage threshold.

Pin	Condition	Description
P53_CFG	Short to GND	5.0 V DOSV undervoltage threshold
	Short to VCC5	3.3V DOSV undervoltage threshold

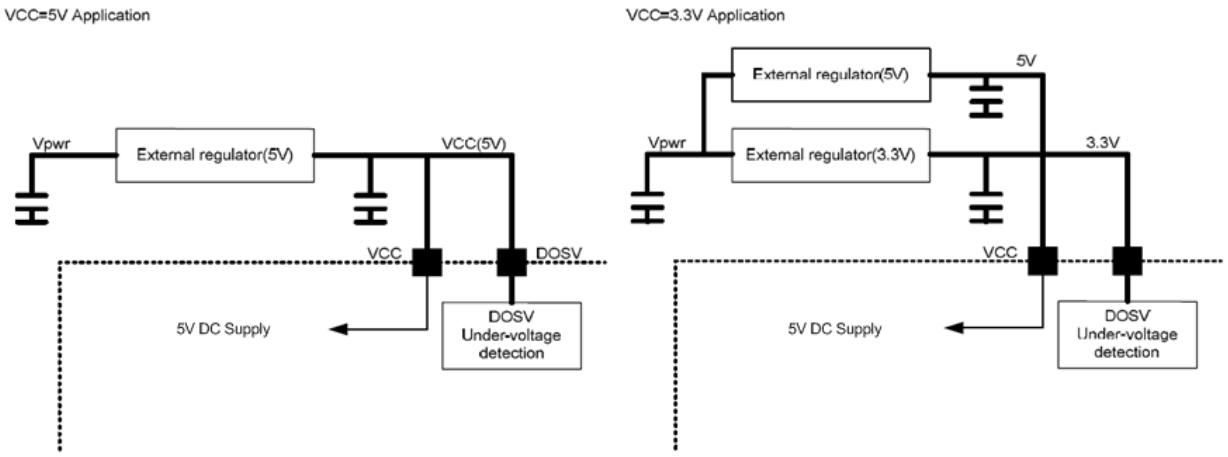


Figure 17. Configuration of VCC5 and DOSV for 5.0 V or 3.3 V application

6.9.1.4 Charge pump

The charge pump generates a voltage of typically 12 V above the supply V_{PWR}. The charge pump voltage is intended for internal use only. No additional load shall be connected to the CP pin. The charge pump requires a capacitor for energy storage and to cover transients. The voltage difference between CP and VPWR can be read by the SPI.

6.9.1.5 Internal clock supervision (mismatch MAIN-AUX CLK)

The SB0800 has two independent clock modules, one is the main supply clock to all SB0800 systems. The other monitors the main clock fault and if a fault is detected, the SB0800 resets with the RST_CLK function (Table 21). This function starts when RSTB is in a high state.

Mutual Supervision of Both Main and Auxiliary Clock:

Clock monitoring continues to perform comparisons between the two clocks sources, CLK1 and CLK2. When everything is working correctly, both clocks are present and both have the same frequency of 14 MHz. If one of the clocks stops or if clocks are misaligned in frequency more than ±25% of 14 MHz (Table 23), an RSTB reset is generated (Table 21) and a SPI flag is reported (RST_CLK). The reset flag RST_CLK (same as other reset flags) is cleared in “clear on read” fashion, or in other words, the flag is cleared by a SPI Read command that reads the flag. In the case of a clock monitoring fault, the clock monitoring process will restart only after the clock monitoring flag (RST_CLK) is cleared on the first SPI message.

If either CLK1or CLK2 disappears indefinitely, the clock monitoring fault will show anywhere from T1 to 2*T2. If clock frequencies are misaligned in more than ±25% of 14 MHz, the clock monitoring fault will show after a time delay of T2, as measured by the reference clock CLK1. The misaligned frequency detection error is measured in time window of T2 and the measurement is based on CLK1 clock as reference, therefore if the CLK1 frequency changes, the time window T2 cannot be guaranteed.

The SB0800 internal clock monitoring function can be disabled by the SPI command (StopCLK2), with no effect of functionality except the clock monitoring function, because CLK1 is activated, but CLK2 is deactivated. Frequency modulation can be controlled by the FM_amp and FM_EM bits (See SPI and data register). The SPI command (FM_EN) enables the frequency modulated oscillator by two deviation frequency to spread the oscillator's energy over a wide frequency band. There are two kinds of deviation frequencies (350 kHz and 700 kHz), which are decided by the SPI command (FM_amp). This spreading decreases the peak electromagnetic radiation level and improves electromagnetic compatibility (EMC) performance.

If preferred, the sequence following by SPI command (StopCLK2), and later on if decided to reactivate the CLK2 (clock monitoring re-activated), a reset clk can be generated due to the fact the clk2 re-start, and can have a settling time > 2*T2, 1.0 ms max. In this case, reset is detected during reset recovery time and the CLK_RST (reading message #0) flag should read in a normal condition.

6.9.1.6 Die temperature warning

The SB0800 has 1 temperature warning sensor in the cool place of the die. The threshold of temperature warning is 20 °C below overtemperature. In case of a temperature warning, outputs are not shutdown and the SPI-Bit shows the actual status at accessing time.

6.9.1.7 Ground supervision

GND-loss monitors the voltage between PGND (global reference GND) and GND_D. In case of a disconnection of GND_D vs. all other grounds (pin 2, 4, 13, 37, 46, 51, and back side ground are soldered to ground), a detection GND_D disconnect as soon as the GND_D is higher than the threshold (V_GL) vs. others grounds, is reported through the flag FGND via the SPI register and set high after a filter time (t_{GL}).

1. Connection degraded (resistive path)
   A. GND_D vs other grounds > V_GL but by having Vint_D –GND_D > min voltage required
   B. SPI communication still possible, and the flag FGND will be at 1
2. Disconnection (open physically) during a sequence (in Normal mode), the logic embedded will be frozen, because the voltage Vint_D –GND_D < min voltage required
   A. No SPI communication is possible
   B. If GND_D is reconnected normally, SPI communication recovers and the flag FGND will be at 1

Table 23. Electrical characteristics

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Reset output SB0800 to MCU						
t_{RSTB_REC}	Reset Recovery Time	-20%	45	20%	ms	
Reset input MCU to SB0800						
t_{RST_MIN}	Minimum External Reset Time (only for application)	—	10	—	µs	
DOSV undervoltage						
$DOSV_{UV\_5V}$ $DOSV_{UV\_3P3}$	Undervoltage Reset Threshold at Shutdown (falling edge of DOSV) • P53_CFG = Low (< 0.8 V) • P53_CFG = High (> 2.0 V)	 — —	 4.5 2.9	 — —	V	
t_{DVUV}	Undervoltage Reset Filter Time	—	T1	—	µs	
VCC5 undervoltage						
$VCC5_{UV}$	Undervoltage Threshold	—	4.5	—	V	
t_{VCUV}	Undervoltage Filter Time	—	T1	—	µs	
VCC5 supply						
I_{VCC5} I_{DOSV}	Consumption Current • VCC5 = 5.0 V; HD,PD = on; RSTB = high • During SPI communication	 — —	 — —	 20 10	mA	

Table 23. Electrical characteristics (continued)

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Internal logic supply						
Vint_A	Internal Analog Voltage - I_{LOAD} = -10 mA	2.30	2.5	2.8	V	
Vint_D	Internal Digital Voltage - I_{LOAD} = -10 mA	2.30	2.5	2.8	V	
C_Vint	Stabilization Capacitor at V_INT - Low-voltage capacitor (<4.0 V)	—	220	—	nF	
Internal logic supply undervoltage						
$Vint\_A_{UV}$ $Vint\_D_{UV}$	Undervoltage Reset threshold	—	2.0	—	V	
t_{VINT}	Undervoltage Reset Filter time	—	1.0	—	µs	
VPWR supply						
$I_{\_VPWR}$	Consumption current - VPWR = 36 V, HD, PD = on, RSTB = high	—	5.0	—	mA	
$I_{\_STBY\_VPWR}$	Consumption current at sleep mode - VCC5 = DOSV = 0 V, HD_D = PD_D = VPWR = 36 V	—	2.0	20	µA	
VPWR overvoltage						
$VPWR_{\_OV}$	VPWR Overvoltage Threshold (rising edge)	—	38	—	V	
$VPWR_{\_OV\_HYS}$	Overvoltage Detection Hysteresis - $VPWR_{\_OV(ON)}$ = $VPWR_{\_OV(SHUTDOWN)}$ -$VPWR_{\_OV\_HYS}$	—	0.6	1.0	V	
t_{VPWR_OV}	Overvoltage Detection Filter Time - Both directions	—	T2	—	µs	
VPWR undervoltage						
$VPWR_{\_UV}$	Undervoltage Shutdown Threshold (falling edge)	—	5.1	—	V	
$VPWR_{\_UV\_HYS}$	Undervoltage Detection Hysteresis - $VPWR_{\_OV(ON)}$ = $VPWR_{\_OV(SHUTDOWN)}$ -$VPWR_{\_OV\_HYS}$	30	100	200	mV	
t_{VPUV}	Undervoltage Detection Filter Time	—	T2	—	µs	
Ground-loss detection						
$V_{\_GL}$	GND_d-loss detection threshold - Reference GND_Px	—	0.5	—	V	
t_{GL}	GND_d-loss detection filter time - Reference GND_Px	—	T2	—	µs	
Oscillator						
$f_{\_OSC}$	Main Oscillator Frequency	-7.0%	14	7.0%	MHz	
e_{CLK}	Mismatch MAIN-AUX OSC CLK - enable V_{INT_X} is normal voltage digital comparison between the two clocks.	—	±25	—	%	
t_{CLK}	Mismatch OSC Filter Time	T1	T2	2*T2	µs	(19)
	Frequency Modulation Band 1 - FM_amp = 0	—	350	—	kHz	
	Frequency Modulation Band 2 - FM_amp = 1	—	700	—	kHz	
	Frequency Modulation Speed	—	110	—	kHz	
Overtemperature/temperature warning						
T_W	Temperature Warning Detection Threshold	150	165	180	°C	
t_{TW}	Temperature Warning Detection Filter Time	—	T2	—	µs	
Charge pump						
$C_{\_CP}$	Charge pump external capacitor - Tolerance < ±20%	—	220	—	nF	
$V_{\_CP}$	Charge pump voltage - hd_on = pd_on = 1, LSD 100% duty cycle.		V_{PWR}+13	—	V	(20)

Table 23. Electrical characteristics (continued)

V_{PWR} = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to +125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Timing						
T1	Logic time base T1	14.4	18.2	22	µs	
T2	Logic time base T2	232	293	360	µs	

Notes

19. The t_{CLK} parameter is decided by a frequency checker and comparing two clocks. If either main clock or AUX clock frequency disappears longer than T1, the SB0800 goes to reset by the clock frequency checker and the CLK_RST flag will be detected. Meanwhile, comparing the main clock and AUX clock is done during T2 and the SB0800 is possible to go to reset every T2. Because measurement and reset activation are asynchronous, t_{CLK} can reach 2*T2 in the worst case by comparing two clocks.
20. For more details, refer to the HD_G & PD_G parameters

Write 1 to any xxx_clr_flt register will create a reset of the fault flag during 1 clock period after the SPI message. xxx_clr_flt automatically goes to “0” after 1 clock from fault flag reset.

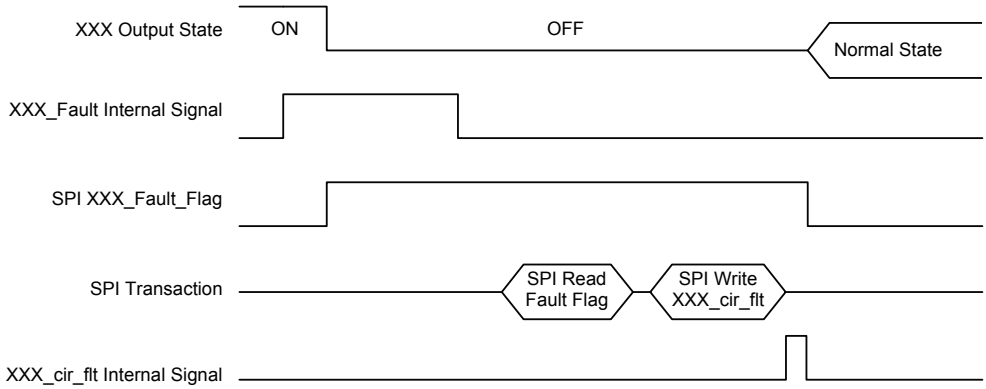


Figure 18. Timing diagram of xxx_clr_flt

6.10 SPI and data register

6.10.1 Function description

The SPI serial interface has the following features:

- Full duplex, four-wire synchronous communication
- Slave mode operation only
- Fixed SCLK polarity and phase requirements
- Fixed 16-bit command word
- SCLK operation up to 10.0 MHz

The Serial Peripheral Interface (SPI) is used to transmit and receive data synchronously with the MCU. Communication occurs over a full-duplex, four-wire SPI bus. The 34SB0800 device operates only as a slave device to the master, and requires four external pins; SI, SO, SCLK, and CSB. All words are 16 bits long and MSB is sent first.

The SPI simultaneously turns on the serial output SO and returns the MISO return bits. When receiving, valid data is latched on the rising edge of each SCLK pulse. The serial output data is available on the rising edge of SCLK, and transitions on the falling edge of SCLK. The number of clock cycles occurring on the pin SCLK while the CSB pin is asserted low must be 16. If the number of clock pulses is not 16 or a parity fault, the SPI MOSI data is ignored. The SB0800 takes even parity. On next data read SO message, “Fmsg” bit sets to 1, and other data bits sets to 0. The parity bit sets to 1. On the first SPI communication after reset, the read SO message sets to 1010101010101010.

The fault registers are double buffered. The first buffer layer latches a fault at the time the fault is detected. This inner layer buffer clears when the fault condition is no longer present and the fault bit communicates to the MCU by a MISO response. The second layer buffer latches the output of the inner layer buffer whenever the CSB pin transitions from low to high. The output of the second layer buffer is transferred to the shift register after the corresponding MOSI command is received from the MCU.

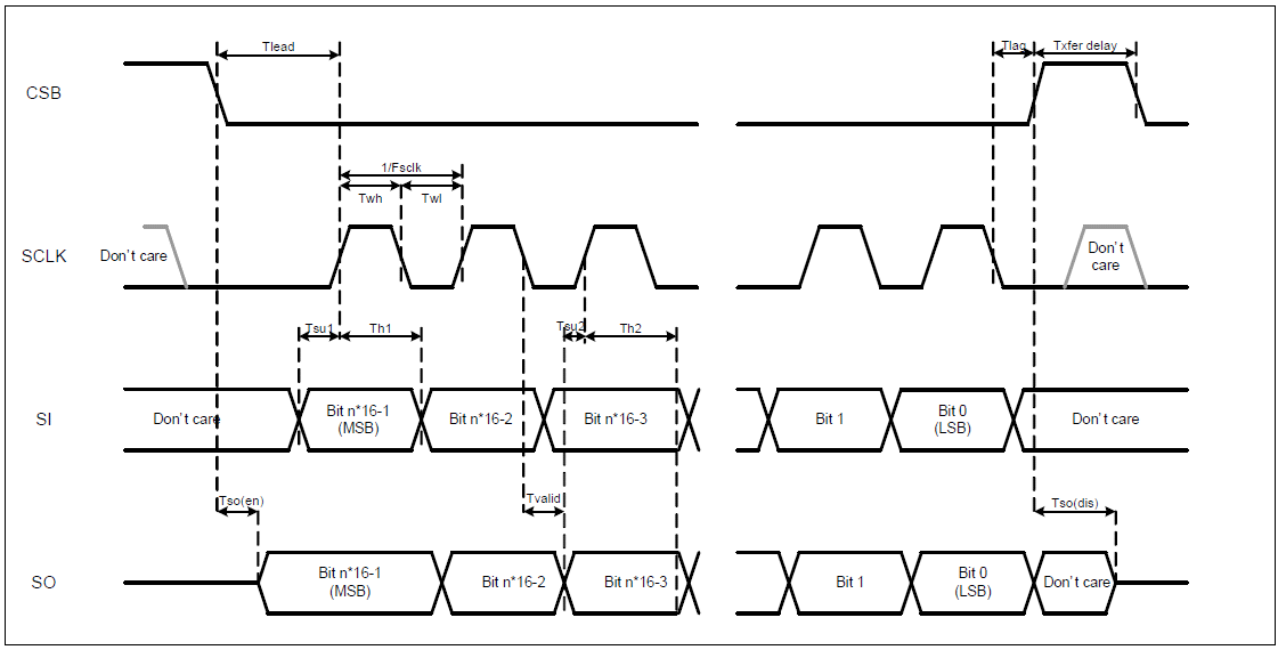


Figure 19. SPI timing diagram

Table 24. SPI timing electrical characteristics

VPWR = 6.0 to 36 V, VCC5 = 4.75 to 5.25 V, DOSV = 3.13 to 5.25 V, T_J = -40 to 125 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface timing [21]						
f_{SPI}	Recommended Frequency of SPI Operation - $t_{SPI} = 1/f_{SPI}$	—	—	10	MHz	
t_{LEAD}	Falling Edge of CSB to the Rising Edge of SCLK (required setup time)	—	$t_{SPI}/2$	50	ns	
t_{LAG}	Falling Edge of SCLK to the Rising Edge of CSB (required setup time)	—	$t_{SPI}/2$	50	ns	
T_{XFER_DELAY}	No Data Time Between SPI Commands	—	—	—	ns	
t_{WH}	High Time of SCLK	—	$t_{SPI}/2$	—	ns	
t_{WL}	Low Time of SCLK	—	$t_{SPI}/2$	—	ns	
t_{SU1}	SI to Rising Edge of SCLK (required setup time)	—	—	—	ns	
$t_{SO(EN)}$	Time from Falling Edge of CSB to SO Low-impedance	—	—	30	ns	
$t_{SO(DIS)}$	Time from Rising Edge of CSB to SO High-impedance	—	—	30	ns	
t_{VALID}	Time from Falling Edge of SCLK to SO Data_valid - 0.2xDOSV ≤ 0.8xDOSV, CL = 50 pF	—	—	30	ns	

Notes

21. The inputs of the SPI module (SCLK, CSB, SI) are driven between 0 V and DOSV voltage.

6.10.2 SPI message structure

addr #		Write										Read													
DEC	BIN	9	8	7	6	5	4	3	2	1	0	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	00000	SED<7:0>								HPD_sr	PD_mt_cfg	Version				dosv_uv	Vcc_uv	Vint_uv	RST_clk	RST_ext	RST_alu	RST_wd	X	HPD_sr	PD_mt_cfg
1	00001	P charac				I charac			lsd_sink_dis	1	0	Manufacturing data				P charac				I charac			lsd_sink_dis	X	X
2	00010	Reserved																							
3	00011	0	0	0	0	FM_amp	FM_EN	StopCL K2	Adin2_en	Adin1_dis	OCF_pd	SB0800_CLK_CNT<7:0>								Vpwr_ov	X	Vpwr_uv	FGND	OTW	X
4	00100	0	0	0	0	0	0	0	0	0	0	0	X	X	X	TEMP<9:0>									
5	00101	0	0	0	0	pd_on	hd_on	0	0	HS_on	LD_on	PD_oc	HD_oc	X	X	VINT_D<9:0>									
6	00110	HS_clr_flt	0	0	0	HD_clr_flt	0	0	LD_clr_flt	PD_clr_flt	LSD_clr_flt	ld_oc	ld_op	ld_ot	vds_ld	vpre10<9:0>									
7	00111	0	0	Iclamp	didt	FDCL	LLC <1>	LLC <0>	CR_fb	CR_dis 12	CR_dis 34	X	CR_fb	CR_dis 12	CR_dis 34	vpre12<9:0>									
8	01000	0	0	0	0	0	0	0	0	0	0	lsd1_cr er	lsd2_cr er	lsd3_cr er	lsd4_cr er	vcp_vpwr<9:0>									
9	01001	0	0	0	0	LF_PWM_14			LF_PWM_58			X	X	X	X	VINT_A<9:0>									
10	01010	LSD1 duty cycle (8-bit) or current set point (10-bit)										lsd1_oc	lsd1_op	lsd1_ot	vds_LSD1	LSD1 duty cycle (8bit) or current read (10 bit)									
11	01011	LSD2 duty cycle (8-bit) or current set point (10-bit)										lsd2_oc	lsd2_op	lsd2_ot	vds_LSD2	LSD2 duty cycle (8bit) or current read (10 bit)									
12	01100	LSD3 duty cycle (8-bit) or current set point (10-bit)										lsd3_oc	lsd3_op	lsd3_ot	vds_LSD3	LSD3 duty cycle (8bit) or current read (10 bit)									
13	01101	LSD4 duty cycle (8-bit) or current set point (10-bit)										lsd4_oc	lsd4_op	lsd4_ot	vds_LSD4	LSD4 duty cycle (8bit) or current read (10 bit)									
14	01110	LSD5 duty cycle								0	0	lsd5_oc	lsd5_op	lsd5_ot	vds_LSD5	LSD5 duty cycle								0	0
15	01111	LSD6 duty cycle								0	0	lsd6_oc	lsd6_op	lsd6_ot	vds_LSD6	LSD6 duty cycle								0	0
16	10000	LSD7 duty cycle								0	0	lsd7_oc	lsd7_op	lsd7_ot	vds_LSD7	LSD7 duty cycle								0	0
17	10001	LSD8 duty cycle								0	0	lsd8_oc	lsd8_op	lsd8_ot	vds_LSD8	LSD8 duty cycle								0	0
18	10010	0	0	MR<7:0>								X	X	HD_lkg	ERR_CNT					AR<7:0>					
24	11000	0	0	0	0	0	0	0	0	0	0	HS_oc	HS_op	HS_ot	vds_HS	ADIN1<9:0>									
25	11001	0	0	0	0	0	0	0	0	0	0	X	X	X	X	ADIN2<9:0>									
26	11010	0	0	0	0	0	0	0	0	0	0	X	X	X	X	ADIN3<9:0>									

Notes

22. MSB(B15) of both write and read messages is parity bit, whereas only B14 of read message is Fmsg, which show previous write message fault.
23. The ‘X’ bit is used for tests manufacturing.

6.10.3 SPI message description

6.10.3.1 Message #0

Table 25. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					SED<7:0>								HPD_sr	PD_mt_cfg

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 00000	
SED<7:0>	09:02	SEED value of linear feedback shift register	
HPD_sr	01	Bit = 0	HSD & PD slew rate selection is slow (default mode)
		Bit = 1	HSD & PD slew rate selection is fast
PD_mt_cfg	00	Bit = 0	Overcurrent masking time is mt_{PD_OC1} (default mode)
		Bit = 1	There is no Overcurrent masking time

Table 26. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	Version #				dosv_uv	Vcc_uv	Vint_uv	RST_clk	RST_ext	RST_alu	RST_wd	X	HPD_sr	PD_mt_cfg

Field	Bits		Description
P	15	Parity bit	
Fmsg	14	Bit = 0	Previous transfer was valid
		Bit = 1	Parity bit is not correct. Error detected during previous transfer
Version #	13: 10	Version number is xxxx pass	
dosv_uv	09	Bit = 0	DOSV continues normal voltage
		Bit = 1	DOSV was less than DOSV undervoltage threshold longer than tDVUV
Vcc5 uv	08	Bit = 0	VCC5 continues normal voltage
		Bit = 1	VCC5 was less than VCC5_uv longer tVCUV
Vint uv	07	Bit = 0	Vint_D and Vint_A continues normal voltage
		Bit = 1	Vint_D or Vint_A voltage was low
RST_clk	06	Bit = 0	SB0800 internal clock is okay
		Bit = 1	SB0800 internal clock fault was detected.
RST_ext	05	Bit = 0	Normal
		Bit = 1	Reset from external (RSTB pin)
RST_alu	04	Bit = 0	Normal
		Bit = 1	Reset from monitoring module (ERR_CNT≥101)
RST_wd	03	Bit = 0	Normal
		Bit = 1	Valid MR wasn’t updated within t_wd

Field	Bits	Description	
HPD_sr	01	Bit = x	Feedback internal HPD_sr register value
PD_mt_cfg	00	Bit = x	Feedback internal PD_mt_cfg register value

6.10.3.2 Message #1

Table 27. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					P charac				I charac			lsd_sink_dis	1	X

Field	Bits		
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 00001	
P charac	09: 06	BIT	P character
		0111	Factor of P-characteristic = 1.2188
		0110	Factor of P-characteristic = 1.1875
		0101	Factor of P-characteristic = 1.1562
		0100	Factor of P-characteristic = 1.125
		0011	Factor of P-characteristic = 1.0938
		0010	Factor of P-characteristic = 1.0625
		0001	Factor of P-characteristic = 1.0312
		0000	Factor of P-characteristic = 1
		1000	Factor of P-characteristic = 1
		1001	Factor of P-characteristic = 0.9688
		1010	Factor of P-characteristic = 0.9375
		1011	Factor of P-characteristic = 0.9062
		1100	Factor of P-characteristic = 0.875
		1101	Factor of P-characteristic = 0.8438
		1110	Factor of P-characteristic = 0.8125
		1111	Factor of P-characteristic = 0.7812
I charac	05: 03	001	Factor of I-characteristic = 0.25
		010	Factor of I-characteristic = 0.1875
		011	Factor of I-characteristic = 0.1562
		100	Factor of I-characteristic = 0.3125 (Imax)
		000	Factor of I-characteristic = 0.125 (default)
		101	Factor of I-characteristic = 0.0938
		110	Factor of I-characteristic = 0.0625
		111	Factor of I-characteristic = 0.0312
lsd_sink_dis	02	Bit = 0	LSD sink current for open detection is enabled (default mode)
		Bit = 1	LSD sink current for open detection is disabled

Table 28. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	Manufacturing data				P charac				I charac			lsd_sink_dis	X	X

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
Manufacturing data	13: 10	Could be used for traceability (same as version #)	
P charac	09: 06	Feedback of P charac	
I charac	05: 03	Feedback of I charac	
lsd_sink_dis	02	Feedback of lsd_sink_dis	

6.10.3.3 Message #2

Reserved

6.10.3.4 Message #3

Table 29. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					X	X	X	X	FM_amp	FM_EN	Stop CLK 2	Adin2_en	Adin1_dis	OCF_pd

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14:10	Message Identifier: 00011	
FM_amp	05	Bit = 0	Frequency modulation band 1
		Bit = 1	Frequency modulation band 2
FM_EN	04	Bit = 0	Frequency of Main/Aux oscillator clocks is fixed
		Bit = 1	Frequency of Main/Aux oscillator clocks is modulated by the frequency defined by FM_amp
StopCLK2	03	Bit = 0	SB0800 internal clock monitoring function is enabled
		Bit = 1	SB0800 internal clock monitoring function is disabled
Adin2_en	02	Bit = 0	Allow to control the pump trough an output of the MCU
		Bit = 1	Allow to control the pump trough SPI command (LD_on bit)
Adin1_dis	01	Bit = 0	Allow to control the low-side for resistive load trough SPI command (Pd_on bit)
		Bit = 1	Allow to control the low-side for resistive load trough an output of the MCU
OCF_pd	00	Overcurrent filter time of pump driver is selectable by OCF_pd	

Table 30. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	SB0800_CLK_CNT<7:0>								Vpwr ov	X	Vpwr uv	FGND	OTW	X

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
SB0800_CLK_CNT<7:0>	13: 06	Monitoring result from SB0800 internal clock(?)	
Vpwr_ov	05	Bit = 0	Normal
		Bit = 1	VPWR overvoltage
Vpwr_uv	03	Bit = 0	Normal
		Bit = 1	VPWR undervoltage
FGND	02	Bit = 0	Normal
		Bit = 1	GND _D loss detection
OTW_ov	01	Bit = 0	Normal
		Bit = 1	Overtemperature warning

6.10.3.5 Message #4

Table 31. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 00111

Table 32. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	0	X	X	X	TEMP<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
TEMP<9:0>	09:00	10-bit ADC of average die temperature	

6.10.3.6 Message #5

Table 33. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	pd_on	hd_on	0	0	HS_on	LD_on

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 00101	
pd_on	05	Bits = 0	Pump motor driver is off
		Bits = 1	Pump motor driver is on
hd_on	04	Bits = 0	High-side driver is off
		Bits = 1	High-side driver is on
LD_on	00	Bits = 0	Low-side is off
		Bits = 1	Low-side turn on

Table 34. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	PD_oc	HD_oc	X	X	VINT_D<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
PD_oc	13	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD1
HD_oc	12	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD2
VINT_D<9:0>	09:00	10-bit ADC internal supply	

6.10.3.7 Message #6

Table 35. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					HS_clr_flt	0	0	0	HD_clr_flt	0	0	LD_clr_flt	PD_clr_flt	LSD_clr_flt

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 00110	
HS_clr_flt	09	Bit = 0	HS_oc and HS_ot are conserved (default mode)
		Bit = 1	Clear HS_oc and HS_ot
HD_clr_flt	05	Bit = 0	HD_oc and HD_lkg are conserved (default mode)
		Bit = 1	Clear HD_oc and HD_lkg
LD_clr_flt	02	Bit = 0	LD_oc and LD_ot are conserved (default mode)
		Bit = 1	Clear LD_oc and LD_ot
PD_clr_flt	01	Bit = 0	PD_oc is conserved (default mode)
		Bit = 1	Clear PD_oc
LSD_clr_flt	00	Bit = 0	All LSDx_oc and LSDx_ot are conserved (default mode)
		Bit = 1	Clear All LSDx_oc and LSDx_ot

Table 36. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	ld_oc	ld_op	ld_ot	vds_ld	vpre10<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
ld_oc	13	Bit = 0	Normal
		Bit = 1	Overcurrent shut down of low-side
ld_op	12	Bit = 0	Normal
		Bit = 1	Open load detection of low-side
ld_ot	11	Bit = 0	Normal
		Bit = 1	Overtemperature shut down of low-side
vds_ld	10	Bit = 0	Normal
		Bit = 1	Vds detection of low-side (information only)
vpre10<9:0>	09:00	10-bit ADC of vpre10	

6.10.3.8 Message #7

Table 37. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	Iclamp	didt	FDCL	LLC <1>	LLC <0>	CR_fb	CR_dis 12	CR_dis 34

Field	Bits	Description		
P	15	Parity bit		
Iclamp	07	Bit = 0 Integrator limit is 0x03FF		
		Bit = 1 Integrator limit is 0x07FF		
didt	06	Bit = 0 Rise / Fall time of LSD is long (tr/tf_CR1)		
		Bit = 1 Rise / Fall time of LSD is short (tr/tf_CR2)		
FDCL	05	Bit = 0 The first duty cycle is controlled by current		
		Bit = 1 First duty cycle from off state to a target value is limited to a fixed duty cycle. (Fixed value is the duty cycle which a target current is transformed in duty cycle, lowest value is 10%)		
LLC	04:03	Bit = 00	Minimum duty cycle (DC) is 10% The measurement is done at Ton/2	
		Bit = 01	Minimum duty cycle (DC) is 3.12% For DC > 10%, the measurement is done at Ton/2. For 3.12% < DC < 10%, the measurement is done at the maximum value between Ton/2 and 3.12%	
		Bit = 10	Bit = 10 Minimum duty cycle (DC) is: 3.12% + 1.56% every two cycles For DC > 10%, the measurement is done at Ton/2. For 3.12% < DC < 10% the regulation current approach up to 3.12% of DC and the measurement is done at the maximum value between Ton/2 and 3.12% For 1.56% < DC < 3.12%, 3.12% of DC and 1.56%. DC are forced every two cycles and no measurement is done during 1.56% of DC.	
		Bit = 11	Minimum duty cycle (DC) is: 3.12% + skipping DC every two cycles For DC > 10%, the measurement is done at Ton/2. For 3.12% < DC < 10% the regulation current approach up to 3.12% of DC and the measurement is done at the maximum value between Ton/2 of DC and 3.12% For DC < 3.12%, the regulation current forces 3.12% and skipping every two cycles and no measurement is done during the skipping mode.	
CR_fb	02	Bit = 0	LSDx Feedback = SPI written value	
		Bit = 1	LSDx Feedback = output	
			CR_fb = 0	CR_fb = 1
CR_dis12	01	CR_dis12 = 0	LSD1,2 Current regulation	LSD1,2 Current regulation
		CR_dis12 = 1	LSD1,2 PWM	LSD1,2 PWM
CR_dis34	00	CR_dis34 = 0	LSD3,4 Current regulation	LSD3,4 Current regulation
		CR_dis34 = 1	LSD3,4 PWM	LSD3,4 PWM

Table 38. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	X	CR_fb	CR_dis 12	CR_dis 34	vpre12<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
CR_fb	12	Feedback of CR_fb	
CR_dis12		Feedback of CR_dis12	
CR_dis34		Feedback of CR_dis34	
vpre12<9:0>	09:00	10-bit ADC of vpre12	

6.10.3.9 Message #8

Table 39. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 01000

Table 40. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd1_cr er	lsd2_cr er	lsd3_cr er	lsd4_cr er	vcp_vpwr<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
lsd1_crer	13	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD1
lsd2_crer	12	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD2
lsd3_crer	11	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD3
lsd4_crer	10	Bit = 0	Normal
		Bit = 1	Current regulation error detection of LSD4
vcp_vpwr<9:0>	09:00	10-bit ADC of vcp_vpwr	

6.10.3.10 Message #9

Table 41. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					X	X	X	X	LF_PWM_14			LF_PWM_58		

Field	Bits	Description	
P	15	Parity bit	
MSG_ID	14: 10	Message Identifier: 01001	
LF_PWM_14	05:03	Bit = 000	Output PWM frequency of LSD(1~4)= 3.9 kHz
		Bit = 001	Output PWM frequency of LSD(1~4)= 4.5 kHz
		Bit = 010	Output PWM frequency of LSD(1~4)= 5.0 kHz
		Bit = 011	Output PWM frequency of LSD(1~4)= 4.2 kHz
		Bit = 100	Output PWM frequency of LSD(1~4)= 3.6 kHz
		Bit = 101	Output PWM frequency of LSD(1~4)= 3.4 kHz
		Bit = 110	Output PWM frequency of LSD(1~4)= 3.2 kHz
		Bit = 111	Output PWM frequency of LSD(1~4)= 3.0 kHz
LF_PWM_58	02:00	Bit = 000	Output PWM frequency of LSD(5~8)= 3.9 kHz
		Bit = 001	Output PWM frequency of LSD(5~8)= 4.5 kHz
		Bit = 010	Output PWM frequency of LSD(5~8)= 5.0 kHz
		Bit = 011	Output PWM frequency of LSD(5~8)= 4.2 kHz
		Bit = 100	Output PWM frequency of LSD(5~8)= 3.6 kHz
		Bit = 101	Output PWM frequency of LSD(5~8)= 3.4 kHz
		Bit = 110	Output PWM frequency of LSD(5~8)= 3.2 kHz
		Bit = 111	Output PWM frequency of LSD(5~8)= 3.0 kHz

Table 42. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg					VINT_A<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
VINT_A<9:0>	09:00	10-bit ADC of internal supply	

6.10.3.11 Message #10

Table 43. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD1 duty cycle (8-bit) or current set point (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
MSG_ID	14: 10	Message Identifier: 01010		
LSD1 duty cycle (8-bit) or current set point(10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis12= 0	LSD1, 2 current regulation Write current target (10 bits, 0 to 2.25 A)	LSD1,2 current regulation Write current target (10 bits, 0 to 2.25 A)
		CR_dis12= 1	LSD1, 2 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD1[1:0]=XX	LSD1,2 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD1[1:0]=XX

Table 44. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd1_ oc	lsd1_op	lsd1_ot	vds_ LSD1	LSD1 duty cycle (8-bit) or current read (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.	
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.	
lsd1_ oc	13	Bit = 0	Normal	
		Bit = 1	Overcurrent shutdown of LSD1	
lsd1_op	12	Bit = 0	Normal	
		Bit = 1	Open Load detection of LSD1	
lsd1_ot	11	Bit = 0	Normal	
		Bit = 1	Overtemperature shutdown of LSD1	
vds_LSD1	10	Bit = 0	Normal	
		Bit = 1	V_{DS} detection of LSD1 (information only)	
LSD1 duty cycle (8-bit) or current read (10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis12= 0	LSD1,2 current regulation Read current target (to check SPI write) (10 bits, 0 to 2.25 A)	LSD1,2 current regulation Output duty cycle value for gate driver (8 bits, for the range to 100%)
		CR_dis12= 1	LSD1,2 PWM Read programmed PWM duty cycle (to check SPI write) (8 bits at 0%, 100% and 10% to 90%) LSD(1~2)[1:0]=00	LSD1,2 PWM Read hardware ADC current value (10 bits for the range to 4.5A)

6.10.3.12 Message #11

Table 45. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD2 duty cycle (8bit) or current set point (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
MSG_ID	14: 10	Message Identifier: 01011		
LSD2 duty cycle (8-bit) or current set point(10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis12= 0	LSD1,2 current regulation Write current target (10 bits, 0 to 2.25 A)	LSD1,2 current regulation Write current target (10 bits, 0 to 2.25 A)
		CR_dis12= 1	LSD1,2 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD2[1:0]=XX	LSD1,2 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD2[1:0]=XX

Table 46. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd2_ oc	lsd2_op	lsd2_ot	vds_LSD2	LSD2 duty cycle (8-bit) or current read (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.	
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.	
lsd2_ oc	13	Bit = 0	Normal	
		Bit = 1	Overcurrent shutdown of LSD2	
lsd2_op	12	Bit = 0	Normal	
		Bit = 1	Open load detection of LSD2	
lsd2_ot	11	Bit = 0	Normal	
		Bit = 1	Overtemperature shutdown of LSD2	
vds_LSD2	10	Bit = 0	Normal	
		Bit = 1	V_{DS} detection of LSD2 (information only)	
LSD2 duty cycle (8-bit) or current read (10-bit)	09:00		CR_fb = 0	CR_fb=1
		CR_dis12= 0	LSD1,2 current regulation Read current target (to check SPI write) (10 bits, 0 to 2.25 A)	LSD1,2 current regulation Output duty cycle value for gate driver (8 bits, for the range to 100%)
		CR_dis12= 1	LSD1,2 PWM Read programmed PWM duty cycle (to check SPI write) (8 bits at 0%, 100% and 10% to 90%) LSD(1~2)[1:0]=00	LSD1,2 PWM Read hardware ADC current value (10 bits for the range to 4.5 A)

6.10.3.13 Message #12

Table 47. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD3 duty cycle (8-bit) or current set point (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
MSG_ID	14: 10	Message Identifier: 01100		
LSD3 duty cycle (8-bit) or current set point(10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis34= 0	LSD3,4 current regulation Write current target (10 bits, 0 to 2.25 A)	LSD3,4 current regulation Write current target (10 bits, 0 to 2.25 A)
		CR_dis34= 1	LSD3,4 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD3[1:0]=XX	LSD3,4 PWM Write programmed duty cycle (8 bits at 0%, 100% and 10% to 90%) LSD3[1:0]=XX

Table 48. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd3_ oc	lsd3_op	lsd3_ot	vds_LSD3	LSD3 duty cycle (8-bit) or current read (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.	
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.	
lsd3_ oc	13	Bit = 0	Normal	
		Bit = 1	Overcurrent shutdown of LSD3	
lsd3_op	12	Bit = 0	Normal	
		Bit = 1	Open load detection of LSD3	
lsd3_ot	11	Bit = 0	Normal	
		Bit = 1	Overtemperature shutdown of LSD3	
vds_LSD3	10	Bit = 0	Normal	
		Bit = 1	V_{DS} detection of LSD3 (information only)	
LSD3 duty cycle (8-bit) or current read (10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis34= 0	LSD3,4 current regulation Read current target (to check SPI write) (10 bits, 0 to 2.25 A)	LSD3,4 current regulation Output duty cycle value for gate driver (8 bits, for the range to 100%)
		CR_dis34= 1	LSD3,4 PWM Read programmed PWM duty cycle (to check SPI write) (8 bits at 0%, 100% and 10% to 90%) LSD(3~4)[1:0]=00	LSD3,4 PWM Read hardware ADC current value (10 bits for the range to 4.5 A)

6.10.3.14 Message #13

Table 49. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD4 duty cycle (8-bit) or current set point (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
MSG_ID	14: 10	Message Identifier: 01101		
LSD4 duty cycle (8-bit) or current set point (10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis34= 0	LSD3, 4 current regulation Write current target (10 bits for the range to 2.25 A)	LSD3, 4 current regulation Write current target (10 bits for the range to 2.25 A)
		CR_dis34= 1	LSD3,4 PWM Write programmed duty cycle (8 bits for the range to 100%) LSD4[1:0]=XX	LSD3, 4 PWM Write programmed duty cycle (8 bits for the range to 100%) LSD4[1:0]=XX

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd4_ oc	lsd4_op	lsd4_ot	vds_LSD4	LSD4 duty cycle (8-bit) or current read (10-bit)									

Field	Bits	Description		
P	15	Parity bit		
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.	
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.	
lsd4_ oc	13	Bit = 0	Normal	
		Bit = 1	Overcurrent shutdown of LSD4	
lsd4_op	12	Bit = 0	Normal	
		Bit = 1	Open load detection of LSD4	
lsd4_ot	11	Bit = 0	Normal	
		Bit = 1	Overtemperature shutdown of LSD4	
vds_LSD4	10	Bit = 0	Normal	
		Bit = 1	V_{DS} detection of LSD4 (information only)	
LSD4 duty cycle (8-bit) or current read (10-bit)	09:00		CR_fb=0	CR_fb=1
		CR_dis34= 0	LSD3,4 current regulation Read current target (to check SPI write) (10 bits, 0 to 2.25 A)	LSD3,4 current regulation Output duty cycle value for gate driver (8 bits, for the range to 100%)
		CR_dis34= 1	LSD3,4 PWM Read programmed PWM duty cycle (to check SPI write) (8 bits at 0%, 100% and 10% to 90%) LSD(3~4)[1:0]=00	LSD3,4 PWM Read hardware ADC current value (10 bits for the range to 4.5 A)

6.10.3.15 Message #14

Table 50. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD5 duty cycle (8bit)								X	X

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 01110
LSD5 duty cycle	09:02	LSD5 PWM duty cycle

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd5_ oc	lsd5_op	lsd5_ot	vds_ LSD5	LSD5 duty cycle (8bit)								X	X

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
lsd5_ oc	13	Bit = 0	Normal
		Bit = 1	Overcurrent shutdown of LSD5
lsd5_op	12	Bit = 0	Normal
		Bit = 1	Open load detection of LSD5
lsd5_ot	11	Bit = 0	Normal
		Bit = 1	Overtemperature shutdown of LSD5
vds_LSD5	10	Bit = 0	Normal
		Bit = 1	V_{DS} detection of LSD5 (information only)
LSD5 duty cycle (8-bit)	09:02	Read Programmed PWM duty cycle (to check SPI write) (8 bits for the range to 100%)	

6.10.3.16 Message #15

Table 51. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD6 duty cycle (8bit)								X	X

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 01111
LSD6 duty cycle	09:02	LSD6 PWM duty cycle

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd6_ oc	lsd6_op	lsd6_ot	vds_ LSD6	LSD6 duty cycle (8bit)								X	X

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
lsd6_ oc	13	Bit = 0	Normal
		Bit = 1	Overcurrent shutdown of LSD6
lsd6_op	12	Bit = 0	Normal
		Bit = 1	Open load detection of LSD6
lsd6_ot	11	Bit = 0	Normal
		Bit = 1	Overtemperature shutdown of LSD6
vds_LSD6	10	Bit = 0	Normal
		Bit = 1	V_{DS} detection of LSD6 (information only)
LSD6 duty cycle (8-bit)	09:02	Read Programmed PWM duty cycle (to check SPI write) (8 bits for the range to 100%)	

6.10.3.17 Message #16

Table 52. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD7 duty cycle (8bit)								X	X

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 10000
LSD7 duty cycle	09:02	LSD7 PWM duty cycle

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd7_ oc	lsd7_op	lsd7_ot	vds_ LSD7	LSD7 duty cycle (8bit)								X	X

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
lsd7_ oc	13	Bit = 0	Normal
		Bit = 1	Overcurrent shutdown of LSD7
lsd7_op	12	Bit = 0	Normal
		Bit = 1	Open load detection of LSD7
lsd7_ot	11	Bit = 0	Normal
		Bit = 1	Overtemperature shutdown of LSD7
vds_LSD7	10	Bit = 0	Normal
		Bit = 1	V_{DS} detection of LSD7 (information only)
LSD7 duty cycle (8-bit)	09:02	Read Programmed PWM duty cycle (to check SPI write) (8 bits for the range to 100%)	

6.10.3.18 Message #17

Table 53. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					LSD8 duty cycle (8bit)								X	X

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 10001
LSD8 duty cycle	09:02	LSD8 PWM duty cycle

Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	lsd8_ oc	lsd8_op	lsd8_ot	vds_ LSD8	LSD7 duty cycle (8bit)								X	X

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
lsd8_ oc	13	Bit = 0	Normal
		Bit = 1	Overcurrent shutdown of LSD8
lsd8_op	12	Bit = 0	Normal
		Bit = 1	Open load detection of LSD8
lsd8_ot	11	Bit = 0	Normal
		Bit = 1	Overtemperature shutdown of LSD7
vds_LSD8	10	Bit = 0	Normal
		Bit = 1	V_{DS} detection of LSD8 (information only)
LSD8 duty cycle (8-bit)	09:02	Read Programmed PWM duty cycle (to check SPI write) (8 bits for the range to 100%)	

6.10.3.19 Message #18

Table 54. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					X	X	MR<7:0>							

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 10010
MR<7:0>	07:00	Monitoring result of MCU

Table 55. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	X	X	X	HD_lkg	ERR_CNT			AR<7:0>						

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
HD_lkg	11	Bit = 0	Normal
		Bit = 1	High-side driver leakage detected
ERR_CNT	10:08	3 bit error counter value of monitoring logic	
AR<7:0>	07:00	Monitoring result of SB0800	

6.10.3.20 Message #19 to 23

Reserved

6.10.3.21 Message #24

Table 56. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 11000

Table 57. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg	HS_oc	HS_op	HS_ot	vds_HS	AD_RST1<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
HS_oc	13	Bit = 0	Normal
		Bit = 1	Overcurrent shut down of high-side
HS_op	12	Bit = 0	Normal
		Bit = 1	Open load detection of high-side
HS_ot	11	Bit = 0	Normal
		Bit = 1	Overtemperature shut down of high-side
vds_HS	10	Bit = 0	Normal
		Bit = 1	Vds detection of high-side (information only)
AD_RST1<9:0>	09:00	10-bit ADC of ADIN1	

6.10.3.22 Message #25

Table 58. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					0	0	0	0	0	0	0	0	0	0

Field	Bits	Description

P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 11001

Table 59. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg					AD_RST2<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
AD_RST2<9:0>	09:00	10-bit ADC of ADIN2	

6.10.3.23 Message #26

Table 60. Write message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	MSG_ID					X	X	X	X	X	X	X	X	X	X

Field	Bits	Description
P	15	Parity bit
MSG_ID	14: 10	Message Identifier: 11010

Table 61. Read message

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
P	Fmsg					AD_RST3<9:0>									

Field	Bits	Description	
P	15	Parity bit	
Fmsg	14	Bit = 0	Parity bit is correct. Previous transfer was valid.
		Bit = 1	Parity bit is not correct. Error detected during previous transfer.
AD_RST3<9:0>	09:00	10-bit ADC of ADIN3	

7 Typical applications

7.1 Application diagrams

This section presents a typical Industrial applications schematic using SB0800, as shown in Figure 20.

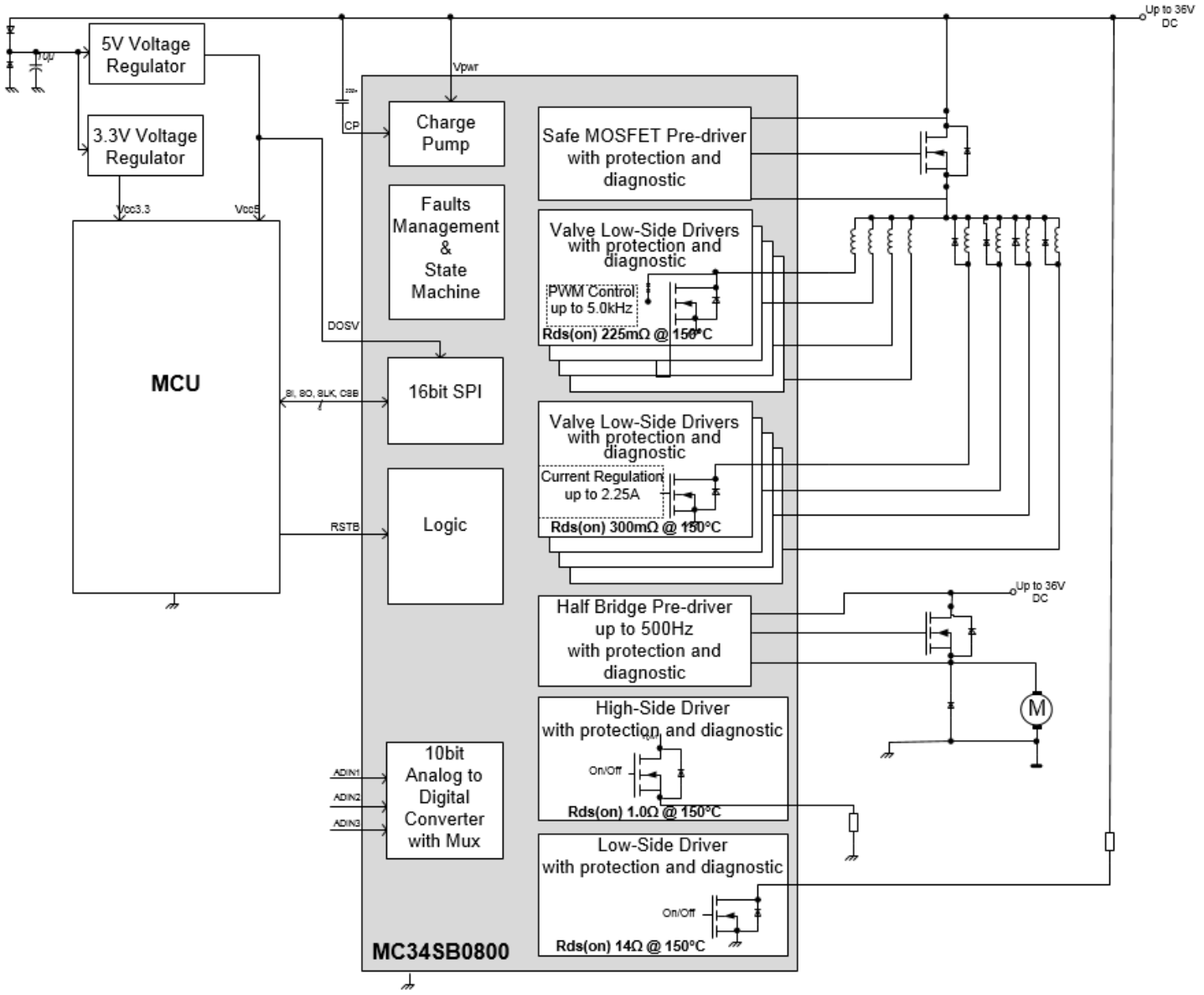


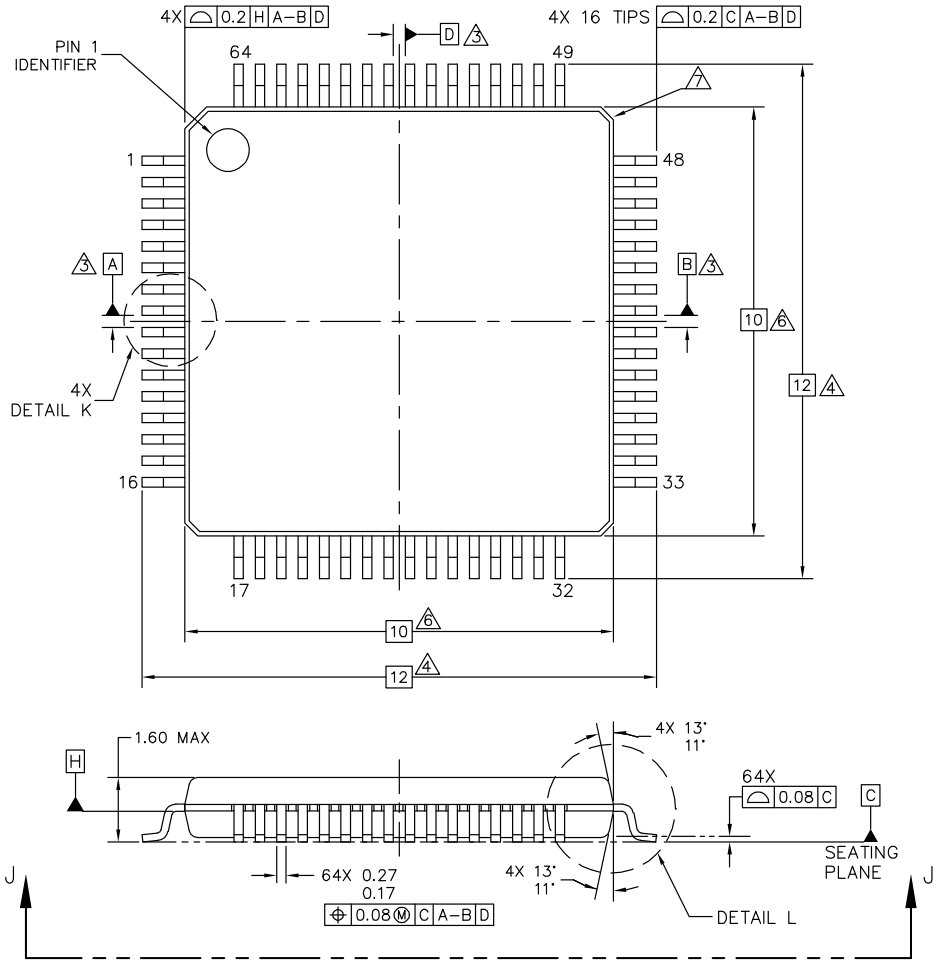
Figure 20. Industrial valves and pump control unit simplified diagram

8 Packaging

8.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Package	Suffix	Package outline drawing number
10 x 10, 64-Pin LQFP Exposed Pad, with 0.5 mm pitch, and a 6.1 x 6.1 exposed pad	AE	98ASA10763D



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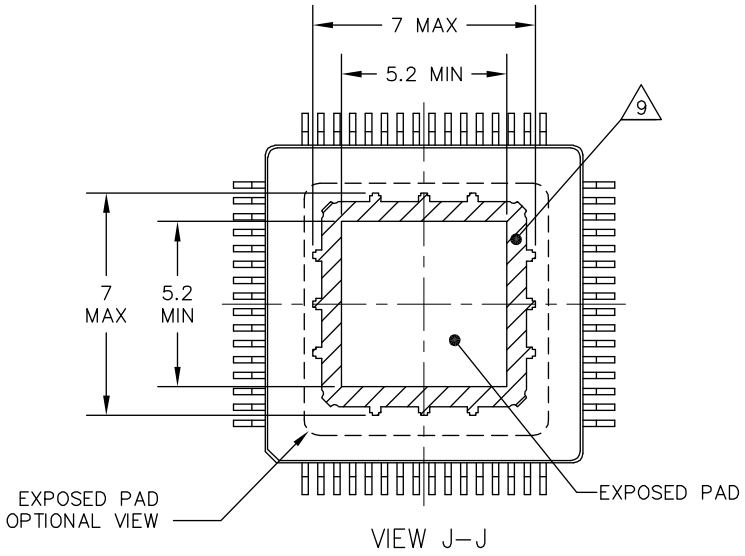
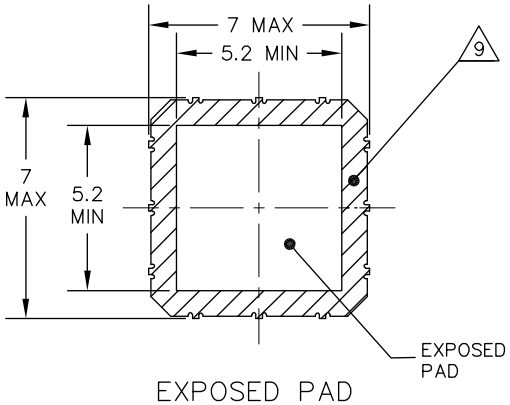
TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: B
	CASE NUMBER: 1899–03	20 SEP 2012
	STANDARD: JEDEC MS–026 BCD	

SB0800



VIEW J–J



EXPOSED PAD
OPTIONAL VIEW

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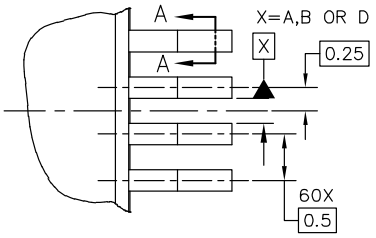
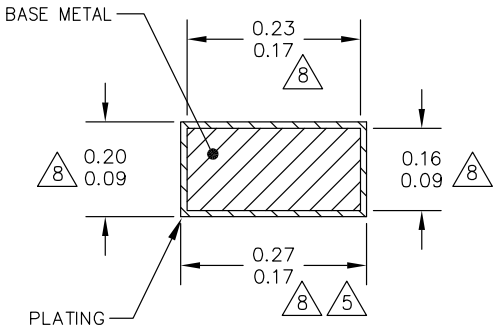
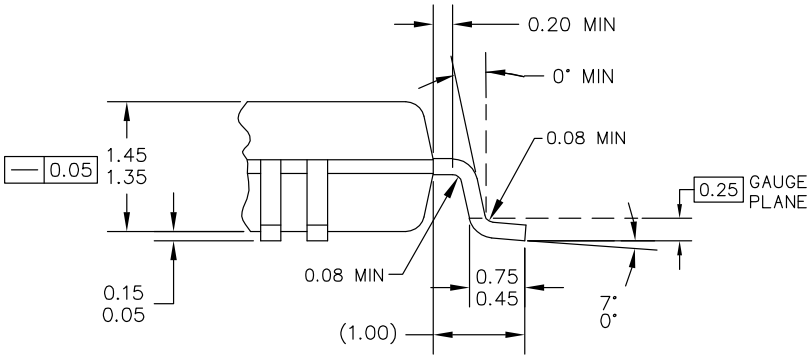
	CASE NUMBER: 1899-03	20 SEP 2012	
	STANDARD: JEDEC MS-026 BCD		



DETAIL K



SECTION A–A
64 PLACES
ROTATED 90° CLOCKWISE



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	CASE NUMBER: 1899-03	20 SEP 2012
	STANDARD: JEDEC MS-026 BCD	

SB0800

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10763D	REV: B
LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	CASE NUMBER: 1899-03	20 SEP 2012
	STANDARD: JEDEC MS-026 BCD	

9 Revision history

Revision	Date	Description of changes
1.0	5/2014	• Initial release
2.0	11/2014	• Increased the operating voltage of the device to 36 V • Updated the parameters with new operating value
	4/2015	• Changed doc classification from Product Preview to Advance Information • Corrected form and style
	5/2015	• Updated document title
3.0	5/2015	• Added t_{VAM} to Table 20 • Added Figure 16
	8/2016	• Updated document to NXP form and style

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