NXP Semiconductors
Data Sheet: Technical Data

Document Number MC9S08PL60
Rev. 4, 06/2020

MC9S08PL60

MC9S08PL60 Series Data Sheet

Supports: MC9S08PL60 and MC9S08PL32

Key features

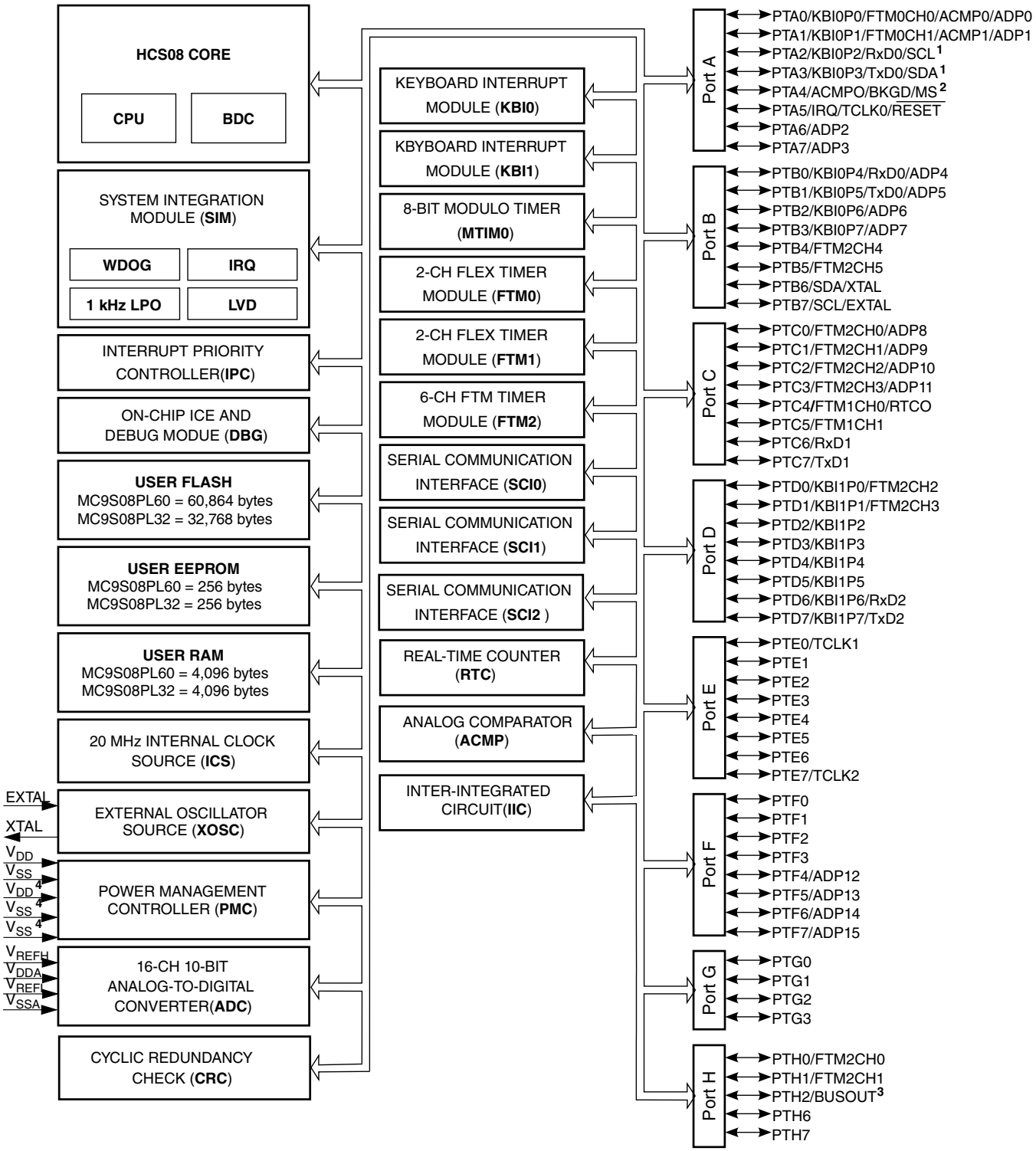
- 8-Bit S08 central processor unit (CPU)
  - Up to 20 MHz bus at 2.7 V to 5.5 V across temperature range of -40 °C to 85 °C
  - Supporting up to 40 interrupt/reset sources
  - Supporting up to four-level nested interrupt
  - On-chip memory
  - Up to 60 KB flash read/program/erase over full operating voltage and temperature
  - Up to 256 byte EEPROM; 2-byte erase sector; program and erase while executing flash
  - Up to 4096 byte random-access memory (RAM)
  - Flash and RAM access protection
- Power-saving modes
  - One low-power stop mode; reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- Clocks
  - Oscillator (XOSC) - loop-controlled Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 4 MHz to 20 MHz
  - Internal clock source (ICS) - containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allowing 1% deviation across temperature range of 0 °C to 70 °C and 2% deviation across temperature range of -40 °C to 85 °C; up to 20 MHz
- System protection
  - Watchdog with independent clock source
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Peripherals
  - ACMP - one analog comparator with both positive and negative inputs; separately selectable interrupt on rising and falling comparator output; filtering
  - ADC - 16-channel, 10-bit resolution; 2.5 µs conversion time; data buffers with optional watermark; automatic compare function; internal bandgap reference channel; operation in stop mode; optional hardware trigger
  - CRC - programmable cyclic redundancy check module
  - FTM - three flex timer modulators modules including one 6-channel and two 2-channel ones; 16-bit counter; each channel can be configured for input capture, output compare, edge- or center-aligned PWM mode
  - IIC - One inter-integrated circuit module; up to 400 kbps; multi-master operation; programmable slave address; supporting broadcast mode and 10-bit addressing; supporting SMBUS and PMBUS
  - MTIM - one modulo timers with 8-bit prescaler and overflow interrupt
  - RTC - 16-bit real timer counter (RTC)
  - SCI - three serial communication interface (SCI/UART) modules optional 13-bit break; full duplex non-return to zero (NRZ); LIN extension support
- Input/Output
  - Up to 57 GPIOs including one output-only pin
  - Two 8-bit keyboard interrupt modules (KBI)
  - Two true open-drain output pins
- Development support
  - Single-wire background debug interface
  - Breakpoint capability to allow three breakpoints setting during in-circuit debugging
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes

- Package options
  - 64-pin QFP
  - 44-pin LQFP
  - 32-pin LQFP

Table of Contents

1 MCU block diagram

The block diagram below shows the structure of the MCUs.



1. PTA2 and PTA3 operate as true open drain when working as output.
2. PTA4/ACMPO/BKGD/MS is an output-only pin when used as port pin.
3. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
4. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 1. MCU block diagram

2 Orderable part numbers

The following table summarizes the part numbers of the devices covered by this document.

Table 1. Ordering information

Part Number	MC9S08PL60			MC9S08PL32		
	CQH	CLD	CLC	CQH	CLD	CLC
Max. frequency (MHz)	20	20	20	20	20	20
Flash memory (KB)	60	60	60	32	32	32
RAM (KB)	4	4	4	4	4	4
EEPROM (B)	256	256	256	256	256	256
10-bit ADC	16ch	12ch	12ch	16ch	12ch	12ch
ACMP	1	1	1	1	1	1
16-bit FlexTimer	6ch+2ch+2ch	6ch+2ch+2ch	6ch+2ch+2ch	6ch+2ch+2ch	6ch+2ch+2ch	6ch+2ch+2ch
8-bit Modulo timer	1	1	1	1	1	1
RTC	Yes	Yes	Yes	Yes	Yes	Yes
IIC	Yes	Yes	Yes	Yes	Yes	Yes
SCI (LIN Capable)	3	3	3	3	3	3
Watchdog	Yes	Yes	Yes	Yes	Yes	Yes
CRC	Yes	Yes	Yes	Yes	Yes	Yes
KBI pins	16	16	13	16	16	13
GPIO	57	42	30	57	42	30
Package	64-QFP	44-LQFP	32-LQFP	64-QFP	44-LQFP	32-LQFP

3 Part identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format:

MC 9 S08 PL AA B CC

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	• MC = fully qualified, general market flow
9	Memory	• 9 = flash based
S08	Core	• S08 = 8-bit CPU
PL	Device family	• PL
AA	Approximate flash size in KB	• 60 = 60 KB • 32 = 32 KB
B	Operating temperature range (°C)	• C = –40 to 85
CC	Package designator	• QH = 64-pin QFP • LD = 44-pin LQFP • LC = 32-pin LQFP

3.4 Example

This is an example part number:

MC9S08PL60CQH

4 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.

Table continues on the next page...

Table 2. Parameter Classifications (continued)

C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

5 Ratings

5.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 85	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

5.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	–0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, XTAL, or true open drain pin)	–0.3	V_{DD} + 0.3	V
	Digital input voltage (true open drain pin)	-0.3	6	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. All digital I/O pins, except open-drain pin , are internally clamped to V_{SS} and V_{DD}. is only clamped to V_{SS}.

6 General

6.1 Nonswitching electrical specifications

6.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 3. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	C	Output high voltage	All I/O pins, standard-drive strength	5 V, I_{load} = -5 mA	V_{DD} - 0.8	—	—	V
	C			3 V, I_{load} = -2.5 mA	V_{DD} - 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V_{OL}	C	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
	C			3 V, I_{load} = 2.5 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	V_{DD}>4.5V	0.70 × V_{DD}	—	—	V
	C			V_{DD}>2.7V	0.75 × V_{DD}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	V_{DD}>4.5V	—	—	0.30 × V_{DD}	V
	C			V_{DD}>2.7V	—	—	0.35 × V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\lvert I_{In}\rvert$	P	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZ}\rvert$	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZTOT}\rvert$	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V_{IN} = V_{DD} or V_{SS}	—	—	2	µA

Table continues on the next page...

Table 3. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R_{PU}[2]	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	kΩ
I_{IC}	D	DC injection current[3, 4, 5]	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
3. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}.
4. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
5. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 4. LVD and POR Specification

Symbol	C	Description		Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1, 2]		1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1)[3]		4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V

Table continues on the next page...

Table 4. LVD and POR Specification (continued)

Symbol	C	Description		Min	Typ	Max	Unit
V_{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVDW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVDW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVDW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [4]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

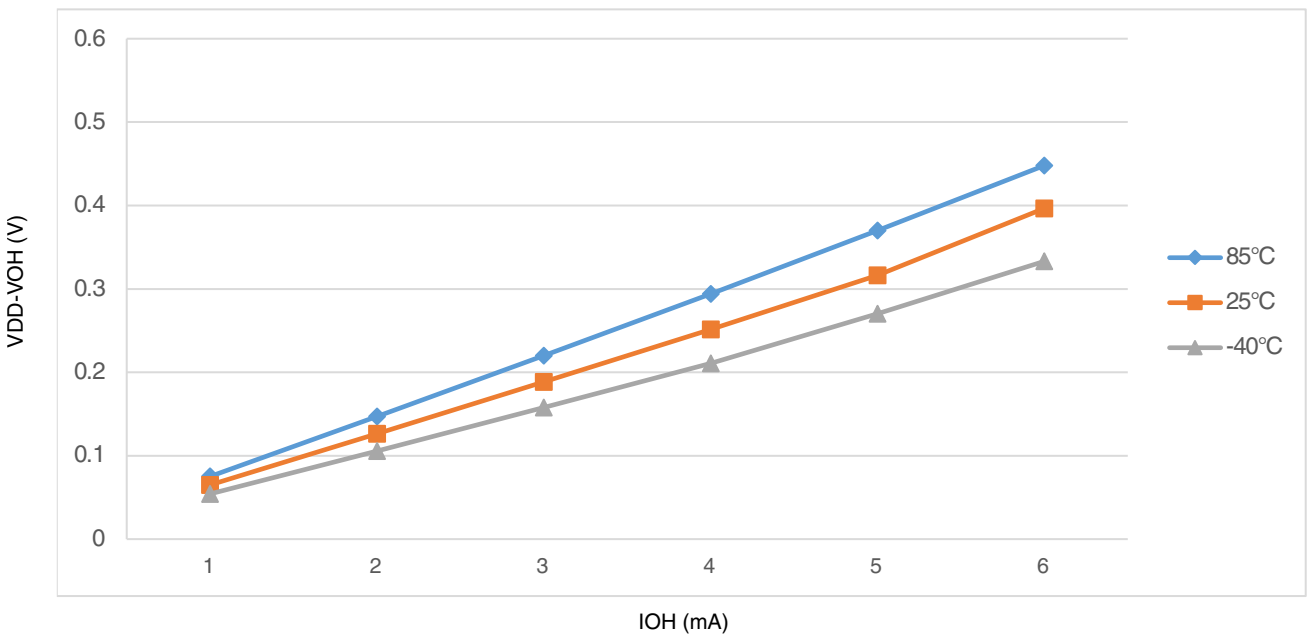


Figure 2. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 5 V)

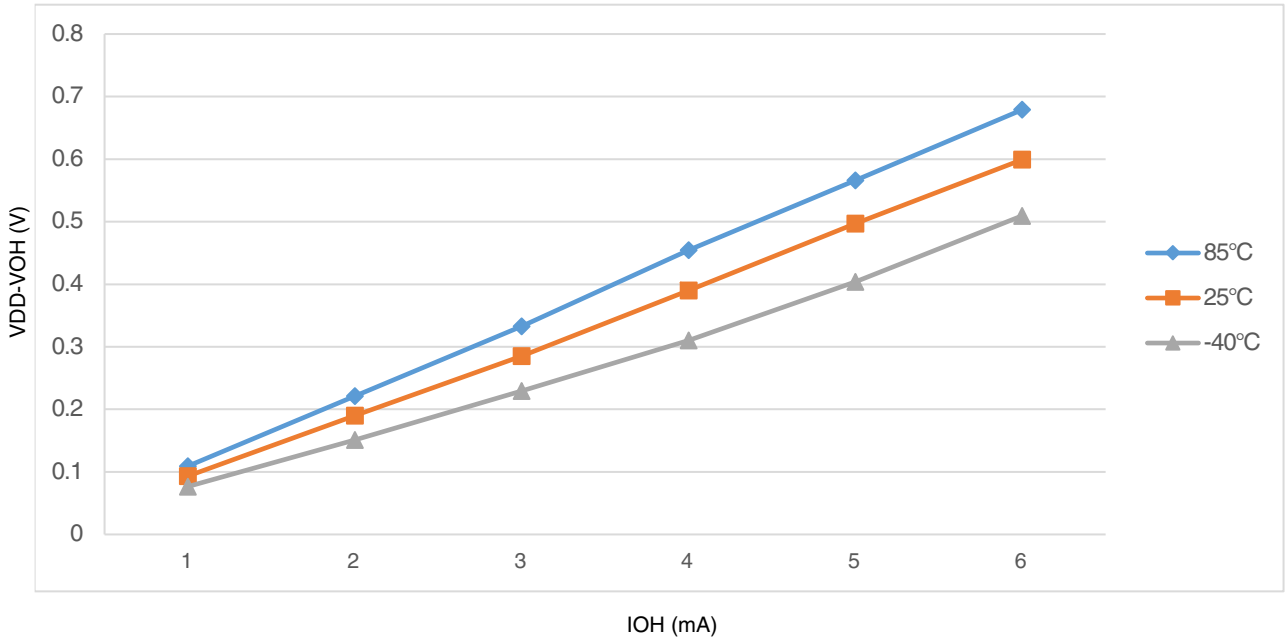


Figure 3. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 3 V)

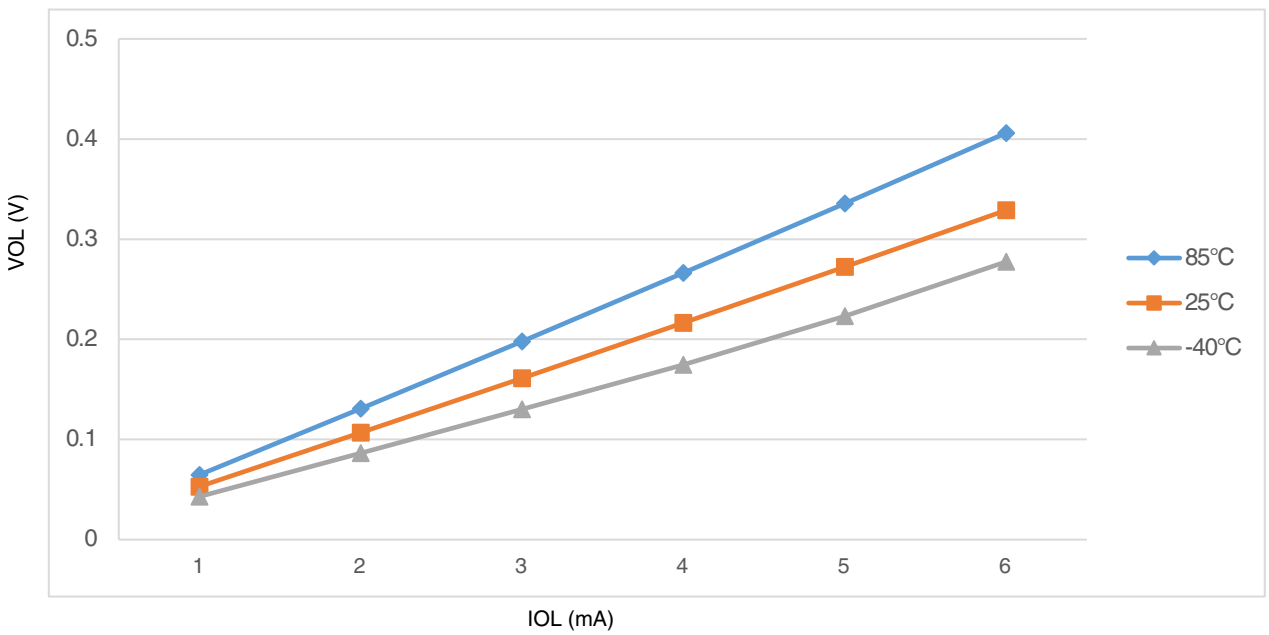


Figure 4. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 5 V)

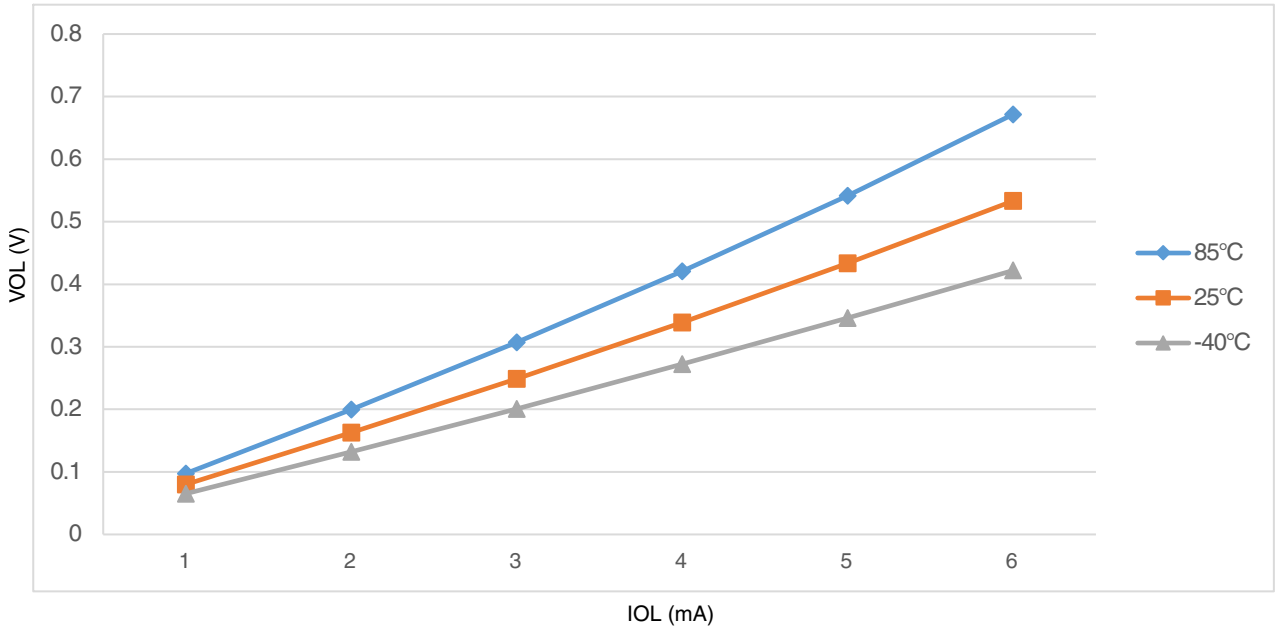


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 3 V)

6.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 5. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI_{DD}	20 MHz	5	12.6	—	mA	-40 to 85 °C
	C			10 MHz		7.2	—		
				1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
				1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI_{DD}	20 MHz	5	10.5	—	mA	-40 to 85 °C
	C			10 MHz		6.2	—		
				1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
				1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI_{DD}	20 MHz	5	12.1	14.8	mA	-40 to 85 °C
	C			10 MHz		6.5	—		
				1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		

Table continues on the next page...

Table 5. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
				1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI_{DD}	20 MHz	5	9.8	12.3	mA	-40 to 85 °C
	C			10 MHz		5.4	—		
				1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
				1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI_{DD}	20 MHz	5	7.8	—	mA	-40 to 85 °C
	C			10 MHz		4.5	—		
				1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
				10 MHz		3.5	—		
				1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock)[2, 3]	$S3I_{DD}$	—	5	1.45	—	µA	-40 to 85 °C
	C			—	3	1.4	—		-40 to 85 °C
7	C	ADC adder to stop3	—	—	5	44	—	µA	-40 to 85 °C
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	40	—		
8	C	LVD adder to stop3[4]	—	—	5	130	—	µA	-40 to 85 °C
	C				3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 µA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
3. ACMP adder cause <10 µA I_{DD} increase typically.
4. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

6.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult NXP applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

6.2 Switching specifications

6.2.1 Control timing

Table 6. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
3	D	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
4	D	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes		t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[3]		t_{MSH}	100	—	—	ns
7	D	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path[4]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
8	D	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
9	C	Port rise and fall time - standard drive strength (load = 50 pF)[5]	—	t_{Rise}	—	10.2	—	ns
	C			t_{Fall}	—	9.5	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels in operating temperature range.

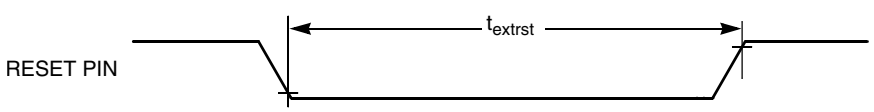


Figure 6. Reset timing

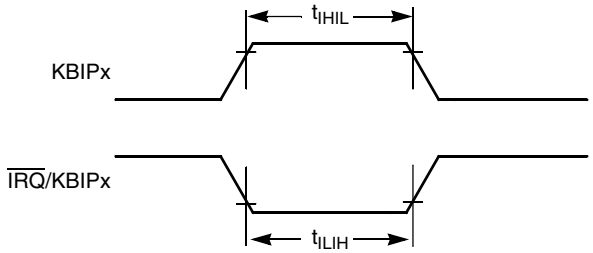


Figure 7. IRQ/KBIPx timing

6.2.2 Debug trace timing specifications

Table 7. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t_{cyc}	Clock period	Frequency dependent		MHz
t_{wl}	Low pulse width	2	—	ns
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns

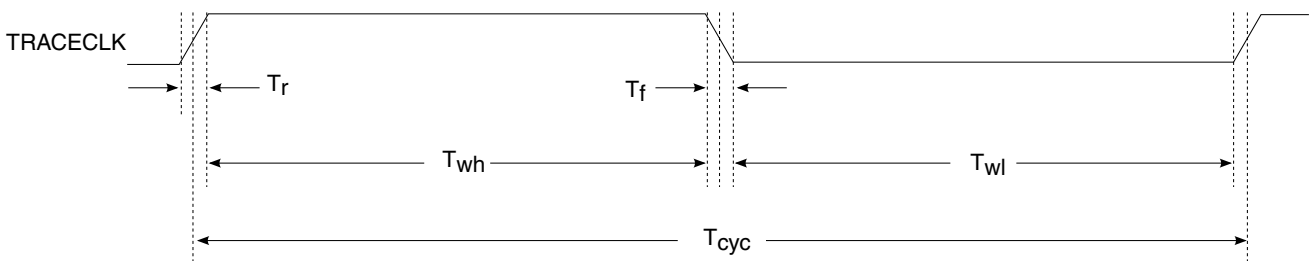


Figure 8. TRACE_CLKOUT specifications

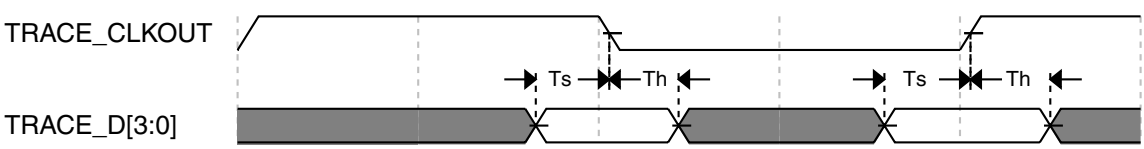


Figure 9. Trace data specifications

6.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

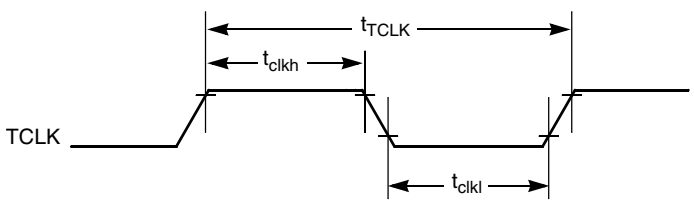


Figure 10. Timer external clock

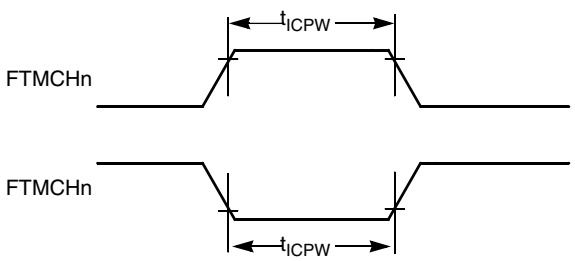


Figure 11. Timer input capture pulse

6.3 Thermal specifications

6.3.1 Thermal operating requirements

Table 9. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	105	°C
T_A	Ambient temperature	–40	85	°C

NOTE

Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

6.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 10. Thermal attributes

Board type	Symbol	Description	64 QFP	44 LQFP	32 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	61	75	86	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	47	53	57	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	50	62	72	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	41	47	51	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	32	34	33	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	23	20	24	°C/W	5

Table continues on the next page...

Table 10. Thermal attributes (continued)

Board type	Symbol	Description	64 QFP	44 LQFP	32 LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	8	5	6	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

7 Peripheral operating requirements and behaviors

7.1 External oscillator (XOSC) and ICS characteristics

Table 11. XOSC and ICS specifications (temperature range = -40 to 85 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1) FEE or FBE mode[2]	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note[3]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[4]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [4]	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ

Table continues on the next page...

Table 11. XOSC and ICS specifications (temperature range = -40 to 85 °C ambient) (continued)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
5	D	Series resistor - High Frequency	Low-Power Mode[4]	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 32.768 kHz crystal; High range = 20 MHz crystal[5, 6]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	D	Square wave input clock frequency	FEE or FBE mode[2]	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—		—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency[5]	Over full voltage and temperature range	Δf_{dco_t}	—	—	±2.0	$\%f_{dco}$
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time[5, 7]		$t_{Acquire}$	—	—	2	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[8]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

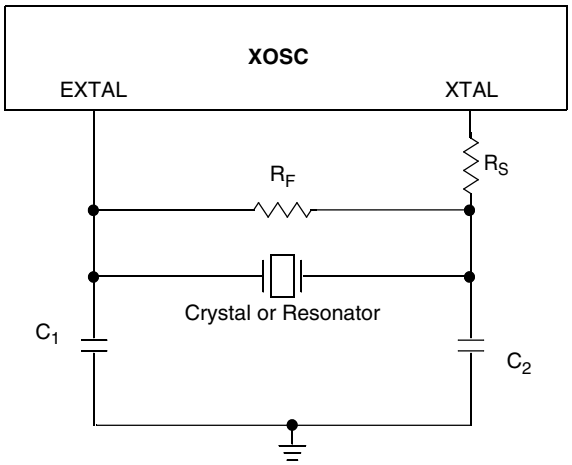


Figure 12. Typical crystal or resonator circuit

7.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 12. Flash clock characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase across the operating temperature range	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f_{NVMBUS}	1	—	20	MHz
D	NVM operating frequency	f_{NVMOP}	0.8	1.0	1.05	MHz
C	FLASH Program/erase endurance T_L to T_H in the operating temperature range	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance T_L to T_H in the operating temperature range	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

All timing parameters are a function of the bus clock frequency, F_{NVMBUS}. All program and erase times are also a function of the NVM operating frequency, f_{NVMOP}.

Each command timing is given by:

$t_{command}=f_{NVMOP}$ cycle × $1/f_{NVMOP}$ + f_{NVMBUS} cycle × $1/f_{NVMBUS}$

Table 13. Flash timing characteristics

C	Characteristic	Symbol	f_{NVMOP} cycle	f_{NVMBUS} cycle
D	Erase Verify All Blocks	t_{VFYALL}	—	17338
D	Erase Verify Flash Block	t_{RD1BLK}	—	16913
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	810
D	Erase Verify Flash Section	t_{RD1SEC}	—	484
D	Erase Verify EEPROM Section	$t_{DRD1SEC}$	—	555
D	Read Once	t_{RDONCE}	—	450
D	Program Flash (2 word)	t_{PGM2}	68	1397
D	Program Flash (4 word)	t_{PGM4}	122	2128
D	Program Once	$t_{PGMONCE}$	122	2090
D	Program EEPROM (1 Byte)	t_{DPGM1}	47	1371
D	Program EEPROM (2 Byte)	t_{DPGM2}	94	2120
D	Program EEPROM (3 Byte)	t_{DPGM3}	141	2869
D	Program EEPROM (4 Byte)	t_{DPGM4}	188	3618
D	Erase All Blocks	t_{ERSALL}	100066	17743
D	Erase Flash Block	t_{ERSBLK}	100060	17236
D	Erase Flash Sector	t_{ERSPG}	20015	868
D	Erase EEPROM Sector	t_{DERSPG}	5015	756
D	Unsecure Flash	t_{UNSECU}	100066	17730
D	Verify Backdoor Access Key	t_{VFYKEY}	—	464
D	Set User Margin Level	t_{MLOADU}	—	407

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

7.3 Analog

7.3.1 ADC characteristics

Table 14. 5 V 10-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDAD})	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	-100	0	+100	mV	

Table continues on the next page...

Table 14. 5 V 10-bit ADC operating conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

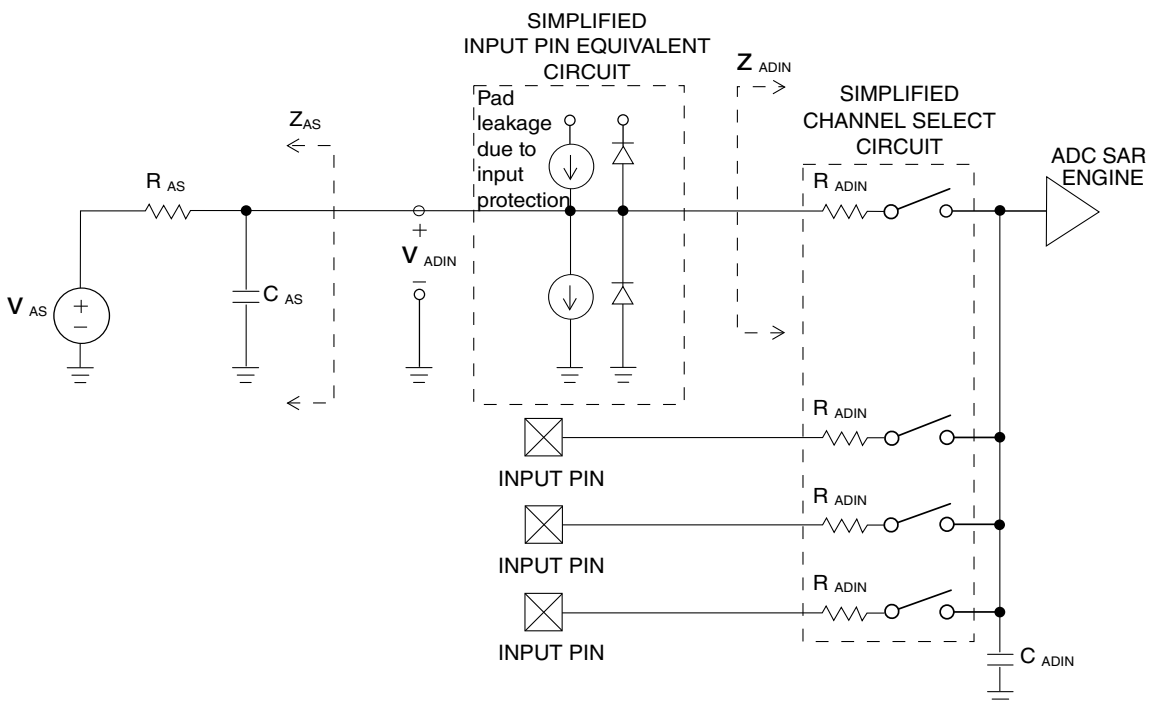


Figure 13. ADC input impedance equivalency diagram

Table 15. 10-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current		T	I_{DDA}	—	133	—	μA

Table continues on the next page...

Table 15. 10-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
ADLPC = 1 ADLSMP = 1 ADCO = 1							
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2]	10-bit mode	P	E_{TUE}	—	±1.5	±2.0	LSB[3]
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	10-bit mode[4]	P	DNL	—	±0.25	±0.5	LSB[3]
	8-bit mode[4]	P		—	±0.15	±0.25	
Integral Non-Linearity	10-bit mode	T	INL	—	±0.3	±0.5	LSB[3]
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error[5]	10-bit mode	P	E_{ZS}	—	±0.25	±1.0	LSB[3]
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error[6]	10-bit mode	T	E_{FS}	—	±0.5	±1.0	LSB[3]
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤10 bit modes	D	E_Q	—	—	±0.5	LSB[3]
Input leakage error[7]	all modes	D	E_{IL}	$I_{In} * R_{AS}$			mV

Table continues on the next page...

Table 15. 10-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 85°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. 1 LSB = (V_{REFH} - V_{REFL})/2^N
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. V_{ADIN} = V_{SSA}
6. V_{ADIN} = V_{DDA}
7. I_{In} = leakage current (refer to DC characteristics)

7.3.2 Analog comparator (ACMP) electricals

Table 16. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	µA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	µs

7.4 Communication interfaces

7.4.1 Inter-Integrated Circuit Interface (I2C) timing

Table 17. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs

Table continues on the next page...

Table 17. I2C timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I²C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

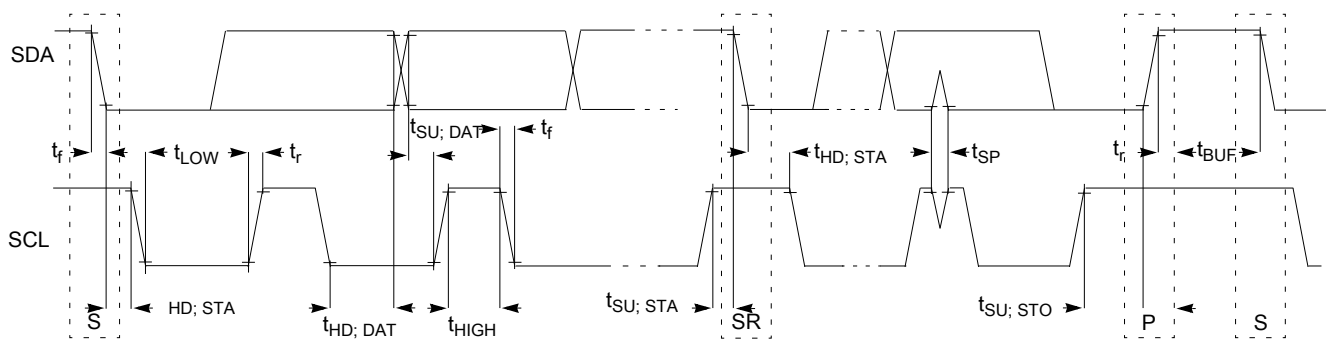


Figure 14. Timing definition for fast and standard mode devices on the I²C bus

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
44-pin LQFP	98ASS23225W
64-pin QFP	98ASB42844B

9 Pinout

9.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 18. Pin availability by package pin-count

Pin Number			Lowest Priority <-- --> Highest				
64-QFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTD1	KBI1P1	FTM2CH3	—	—
2	2	2	PTD0	KBI1P0	FTM2CH2	—	—
3	—	—	PTH7	—	—	—	—
4	3	—	PTH6	—	—	—	—
5	4	3	PTE7	—	TCLK2	—	—
6	5	—	PTH2	—	BUSOUT	—	—
7	6	4	—	—	—	—	V_{DD}
8	—	—	—	—	—	V_{DDA}	V_{REFH}
9	—	—	—	—	—	V_{SSA}	V_{REFL}
10	7	5	—	—	—	—	V_{SS}
11	8	6	PTB7	—	SCL	—	EXTAL
12	9	7	PTB6	—	SDA	—	XTAL
13	—	—	—	—	—	—	V_{SS}
14	10	—	PTH1	—	FTM2CH1	—	—
15	11	—	PTH0	—	FTM2CH0	—	—
16	—	—	PTE6	—	—	—	—
17	—	—	PTE5	—	—	—	—
18	12	8	PTB5	FTM2CH5	—	—	—
19	13	9	PTB4	FTM2CH4	—	—	—

Table continues on the next page...

Table 18. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-QFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
20	14	10	PTC3	FTM2CH3	—	ADP11	—
21	15	11	PTC2	FTM2CH2	—	ADP10	—
22	16	12	PTD7	KBI1P7	TXD2	—	—
23	17	13	PTD6	KBI1P6	RXD2	—	—
24	18	—	PTD5	KBI1P5	—	—	—
25	19	14	PTC1	—	FTM2CH1	ADP9	—
26	20	15	PTC0	—	FTM2CH0	ADP8	—
27	—	—	PTF7	—	—	ADP15	—
28	—	—	PTF6	—	—	ADP14	—
29	—	—	PTF5	—	—	ADP13	—
30	—	—	PTF4	—	—	ADP12	—
31	21	16	PTB3	KBI0P7	—	ADP7	—
32	22	17	PTB2	KBI0P6	—	ADP6	—
33	23	18	PTB1	KBI0P5	TXD0	ADP5	—
34	24	19	PTB0	KBI0P4	RXD0	ADP4	—
35	—	—	PTF3	—	—	—	—
36	—	—	PTF2	—	—	—	—
37	25	20	PTA7	—	—	ADP3	—
38	26	21	PTA6	—	—	ADP2	—
39	27	—	PTE4	—	—	—	—
40	—	—	—	—	—	—	V_{SS}
41	—	—	—	—	—	—	V_{DD}
42	—	—	PTF1	—	—	—	—
43	28	—	PTF0	—	—	—	—
44	29	—	PTD4	KBI1P4	—	—	—
45	30	—	PTD3	KBI1P3	—	—	—
46	31	22	PTD2	KBI1P2	—	—	—
47	32	23	PTA3[1]	KBI0P3	TXD0	SCL	—
48	33	24	PTA2[1]	KBI0P2	RXD0	SDA	—
49	34	25	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
50	35	26	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
51	36	27	PTC7	—	TxD1	—	—
52	37	28	PTC6	—	RxD1	—	—
53	—	—	PTE3	—	—	—	—
54	38	—	PTE2	—	—	—	—
55	—	—	PTG3	—	—	—	—
56	—	—	PTG2	—	—	—	—
57	—	—	PTG1	—	—	—	—

Table continues on the next page...

Table 18. Pin availability by package pin-count (continued)

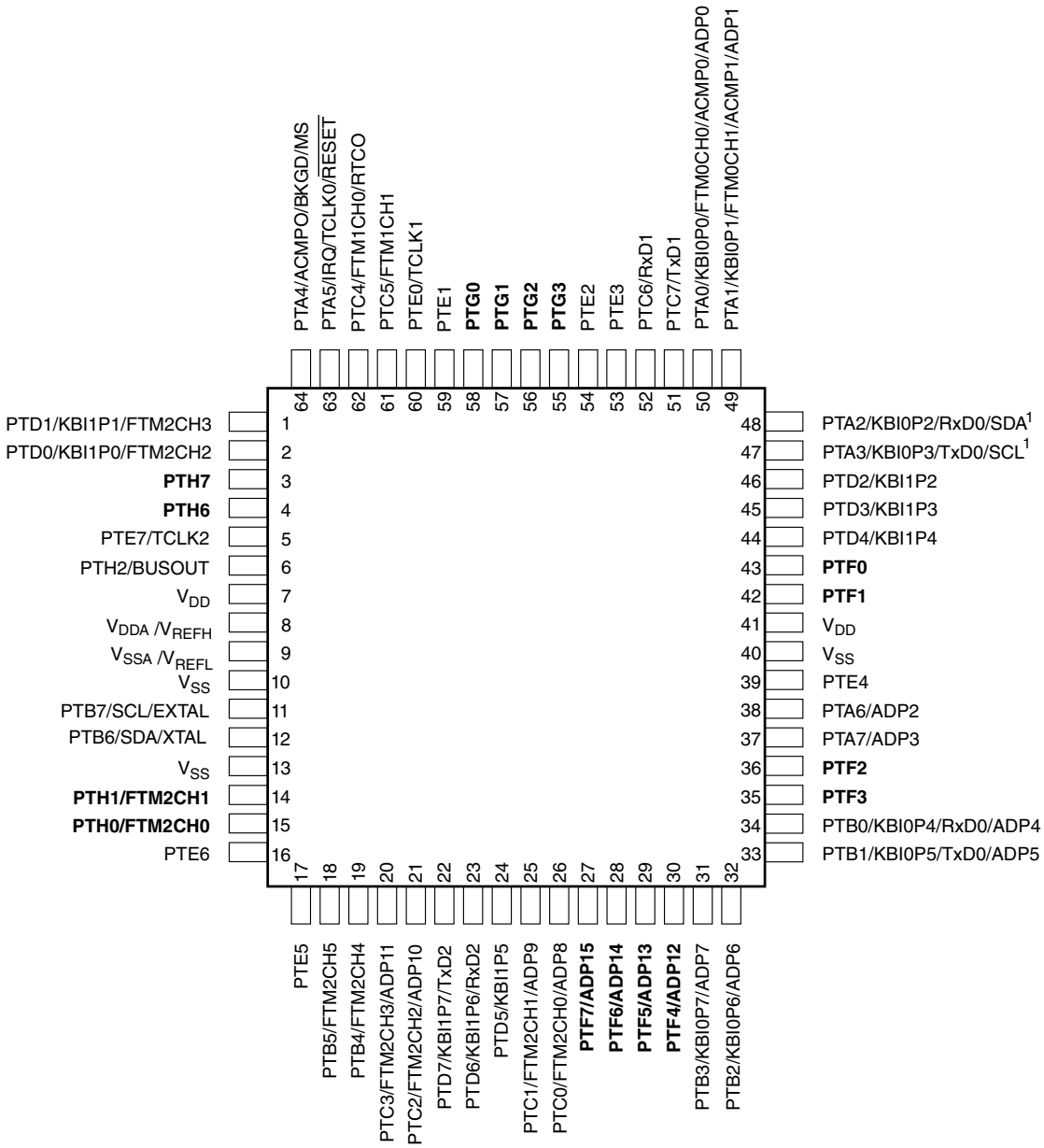
Pin Number			Lowest Priority <-- --> Highest				
64-QFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
58	—	—	PTG0	—	—	—	—
59	39	—	PTE1	—	—	—	—
60	40	—	PTE0	—	—	TCLK1	—
61	41	29	PTC5	—	FTM1CH1	—	—
62	42	30	PTC4	—	FTM1CH0	RTCO	—
63	43	31	PTA5	IRQ	TCLK0	—	$\overline{\text{RESET}}$
64	44	32	PTA4	—	ACMPO	BKGD	MS

1. This is a true open-drain pin when operated as output.

Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

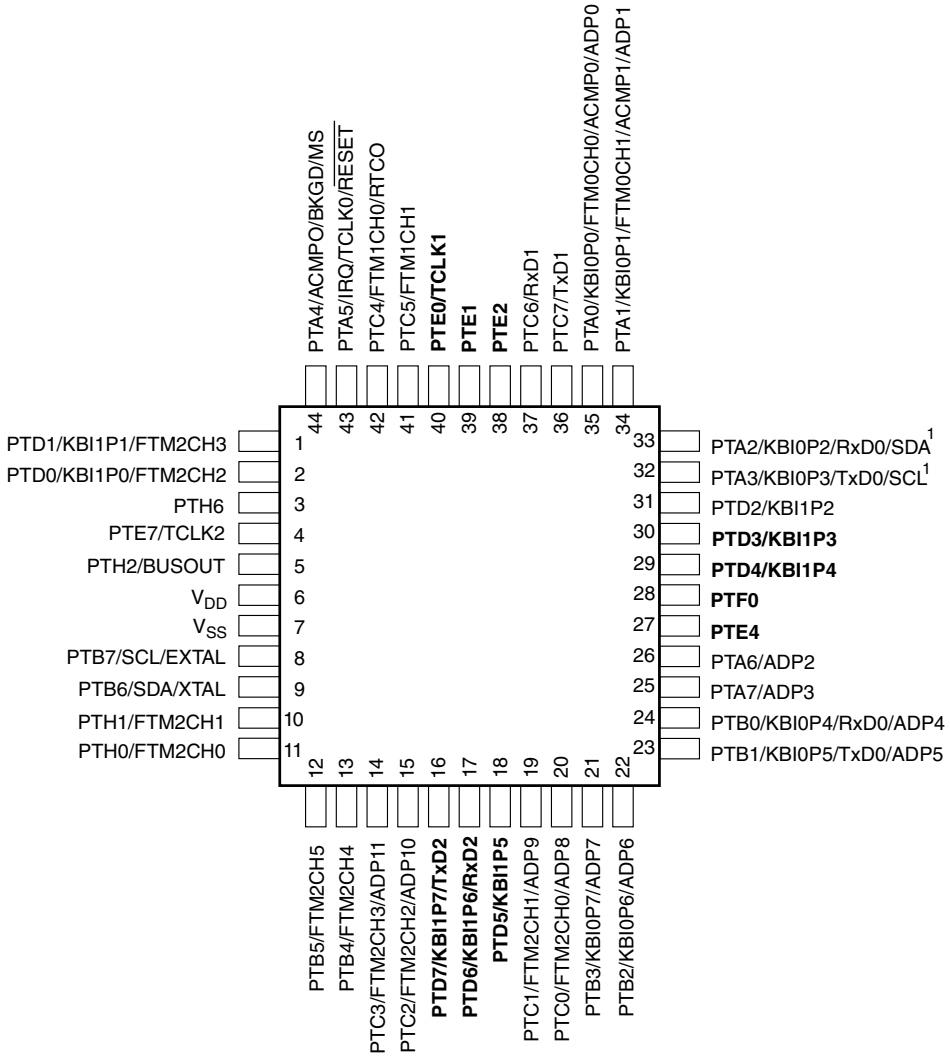
9.2 Device pin assignment



Pins in **bold** are not available on less pin-count packages.

1 True open drain pins

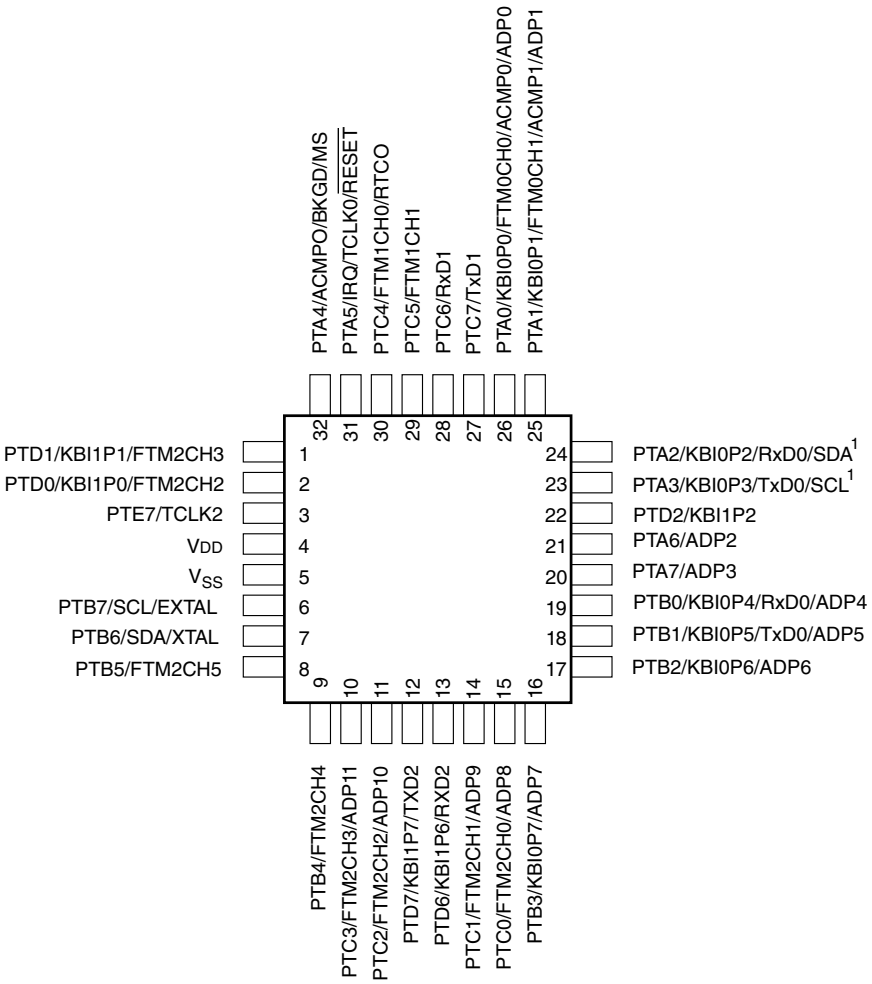
Figure 15. MC9S08PL60 64-pin QFP package



Pins in **bold** are not available on less pin-count packages.

1. True open drain pins

Figure 16. MC9S08PL60 44-pin LQFP package



1.True open drain pins

Figure 17. MC9S08PL60 32-pin LQFP package

10 Revision history

The following table provides a revision history for this document.

Table 19. Revision history

Rev. No.	Date	Substantial Changes
0	03/2018	• Initial Created
1	04/2018	Completed all the TBDs and added 20-pin TSSOP and 16-pin TSSOP packages.
2	01/2019	• Added ACMP module and related information across the whole book. • Added Thermal operating requirements.
3	08/2019	• Added MCU block diagram. • Updated flash characteristics in the NVM specifications. • Updated the S3I$_{DD}$ values in the Supply current characteristics

Table continues on the next page...

Table 19. Revision history (continued)

Rev. No.	Date	Substantial Changes
4	06/2020	• Added IIC module and related information. • Updated PTA0 and PTA1 pinout signalling in 44-pin LQFP package in the Device pin assignment.

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Document Number MC9S08PL60
Revision 4, 06/2020

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for 8-bit Microcontrollers - MCU ***category:***

Click to view products by NXP ***manufacturer:***

Other Similar products are found below :

CY8C20524-12PVXIT MB95F012KPFT-G-SNE2 MB95F013KPMC-G-SNE2 MB95F263KPF-G-SNE2 MB95F264KPFT-G-SNE2 MB95F398KPMC-G-SNE2 MB95F478KPMC2-G-SNE2 MB95F564KPF-G-SNE2 MB95F636KWQN-G-SNE1 MB95F696KPMC-G-SNE2 MB95F698KPMC2-G-SNE2 MB95F698KPMC-G-SNE2 MB95F818KPMC1-G-SNE2 901015X CY8C3MFIDOCK-125 403708R MB95F354EPF-G-SNE2 MB95F564KWQN-G-SNE1 MB95F636KP-G-SH-SNE2 MB95F694KPMC-G-SNE2 MB95F778JPMC1-G-SNE2 MB95F818KPMC-G-SNE2 LC87F0G08AUJA-AH CP8361BT CG8421AF MB95F202KPF-G-SNE2 DF36014FPV 5962-8768407MUA MB95F318EPMC-G-SNE2 MB94F601APMC1-GSE1 MB95F656EPF-G-SNE2 LC78615E-01US-H LC87F5WC8AVU-QIP-H MB95F108AJSPMC-G-JNE1 73S1210F-68M/F/PJ MB89F538-101PMC-GE1 LC87F7DC8AVU-QIP-H MB95F876KPMC-G-SNE2 MB88386PMC-GS-BNDE1 LC87FBK08AU-SSOP-H LC87F2C64AU-QFP-H MB95F636KNWQN-G-118-SNE1 MB95F136NBSTPFV-GS-N2E1 LC87F5NC8AVU-QIP-E CY8C20324-12LQXIT LC87F76C8AU-TQFP-E CG8581AA LC87F2G08AU-SSOP-E CP8085AT MB95F564KPF-G-UNE2