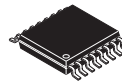




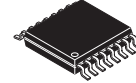
## MC9S08QL8

### MC9S08QL8 Series

#### Covers: MC9S08QL8 and MC9S08QL4



20-Pin TSSOP  
Case 948E



16-Pin TSSOP  
Case 948F

#### Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 3.6 V to 1.8 V across temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Up to 8 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 512 bytes random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two very low power stop modes
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Low power run
  - Low power wait
  - 6  $\mu\text{s}$  typical wakeup time from stop3 mode
  - Typical stop current of 250 nA at 3 V,  $25^{\circ}\text{C}$
- Clock Source Options
  - Oscillator (XOSC) — Very low-power, loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- Peripherals
  - ADC — 8-channel, 12-bit resolution; 2.5  $\mu\text{s}$  conversion time; automatic compare function; 1.7 mV/ $^{\circ}\text{C}$  temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V.
  - ACMP — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be tied internally to TPM input capture; operation in stop3
  - TPM — One 1-channel timer/pulse-width modulator (TPM) module; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; ACMP output can be tied internally to input capture
  - MTIM — 8-bit modulo timer module with optional prescaler
  - RTC — (Real-time counter) 8-bit modulo counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wakeup without external components; runs in all MCU modes
  - SCI — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wakeup on active edge
  - KBI — 8-pin keyboard interrupt with selectable edge and level detection modes
- Input/Output
  - 18 GPIOs include one input-only and one output-only pin.
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins except PTA5.
- Package Options
  - 20-pin TSSOP, 16-pin TSSOP

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.



# Table of Contents

1. Ordering Information	3	4.10.2.TPM Module Timing	20
2. MCU Block Diagram	4	4.11. Analog Comparator (ACMP) Electricals	21
3. Pin Assignments	5	4.12. ADC Characteristics	21
4. Electrical Characteristics	7	4.13. Flash Specifications	25
4.1. Introduction	7	4.14. EMC Performance	26
4.2. Parameter Classification	7	5. Part Identification	27
4.3. Absolute Maximum Ratings	7	6. Package Information	28
4.4. Thermal Characteristics	8	6.1. Mechanical Drawings	28
4.5. ESD Protection and Latch-Up Immunity	9		
4.6. DC Characteristics	10		
4.7. Supply Current Characteristics	14		
4.8. External Oscillator (XOSC) Characteristics	15		
4.9. Internal Clock Source (ICS) Characteristics	17		
4.10. AC Characteristics	19		
4.10.1. Control Timing	19		

## Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://nxp.com/>

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
0	06/12/2018	Initial creation.
1	07/16/2018	Added TSSOP 20 package mechanical drawing.

## Related Documentation

Find the most current versions of all documents at: <http://www.nxp.com>

### Reference Manual (MC9S08QL8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

# 1 Ordering Information

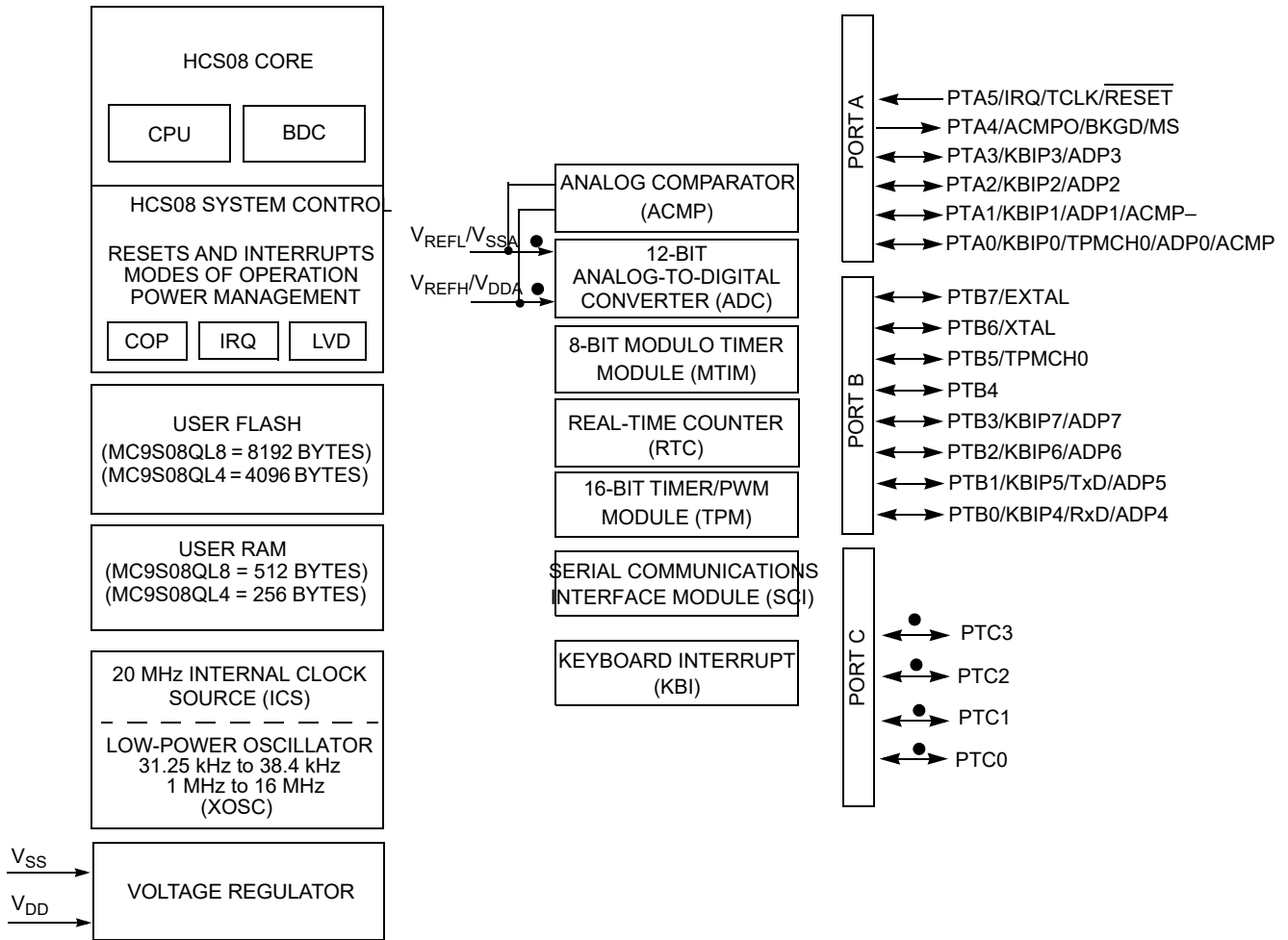
Table 1. Ordering Information

Part Number	MC9S08QL8		MC9S08QL4	
	CTJ	CTG	CTJ	CTG
Max. frequency (MHz)	20	20	20	20
Flash memory (KB)	8	8	4	4
RAM (B)	512	512	256	256
12-bit ADC	8 ch	8 ch	8 ch	8 ch
ACMP	1	1	1	1
16-bit TPM	1 ch	1 ch	1 ch	1 ch
8-bit Modulo timer	1	1	1	1
RTC	Yes	Yes	Yes	Yes
SCI (LIN Capable)	1	1	1	1
KBI pins	8	8	8	8
GPIO <sup>1</sup>	18	14	18	14
Package	20-TSSOP	16-TSSOP	20-TSSOP	16-TSSOP

<sup>1</sup> Port I/O count includes the output-only PTA4 and the input-only PTA5 pins.

## 2 MCU Block Diagram

The block diagram shows the structure of the MC9S08QL8 MCU.



● pins not available on 16-pin package

<sup>1</sup>  $V_{DDA}/V_{REFH}$  and  $V_{SSA}/V_{REFL}$  are double bonded to  $V_{DD}$  and  $V_{SS}$

Figure 1. MC9S08QL8 Series Block Diagram

### 3 Pin Assignments

This chapter shows the pin assignments for the MC9S08QL8 series devices.

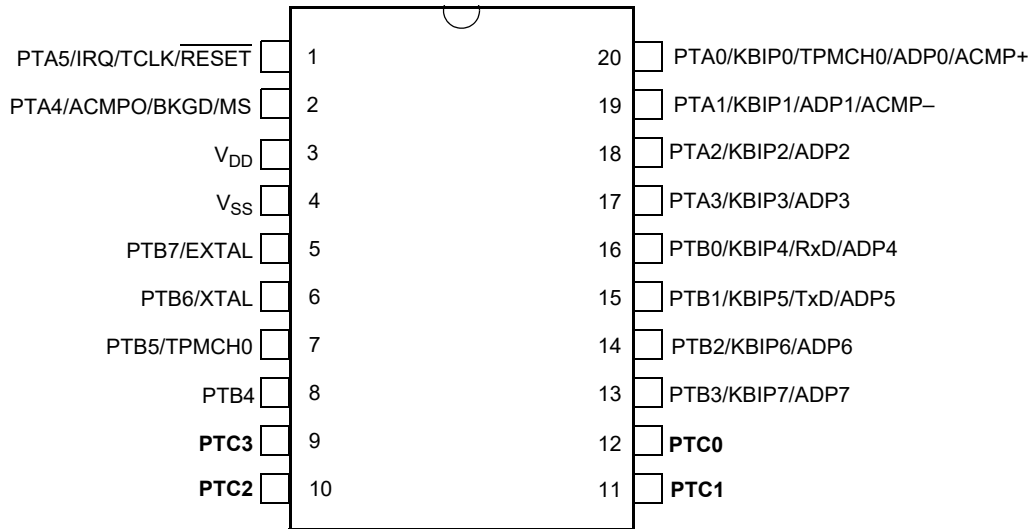
**Table 2. Pin Availability by Package Pin-Count**

Pin Number		<-- Lowest Priority --> Highest				
20	16	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	PTA5	IRQ	TCLK	RESET	
2	2	PTA4	ACMPO	BKGD	MS	
3	3					V <sub>DD</sub>
4	4					V <sub>SS</sub>
5	5	PTB7				EXTAL
6	6	PTB6				XTAL
7	7	PTB5	TPMCH0 <sup>1</sup>			
8	8	PTB4				
9	—	PTC3				
10	—	PTC2				
11	—	PTC1				
12	—	PTC0				
13	9	PTB3	KBIP7		ADP7	
14	10	PTB2	KBIP6		ADP6	
15	11	PTB1	KBIP5	TxD	ADP5	
16	12	PTB0	KBIP4	RxD	ADP4	
17	13	PTA3	KBIP3		ADP3	
18	14	PTA2	KBIP2		ADP2	
19	15	PTA1	KBIP1		ADP1 <sup>2</sup>	ACMP <sup>-2</sup>
20	16	PTA0	KBIP0	TPMCH0	ADP0 <sup>2</sup>	ACMP <sup>+2</sup>

<sup>1</sup> TPMCH0 pin can be repositioned using at PTB5 TPMCH0PS in SOPT2, default reset location is PTA0.

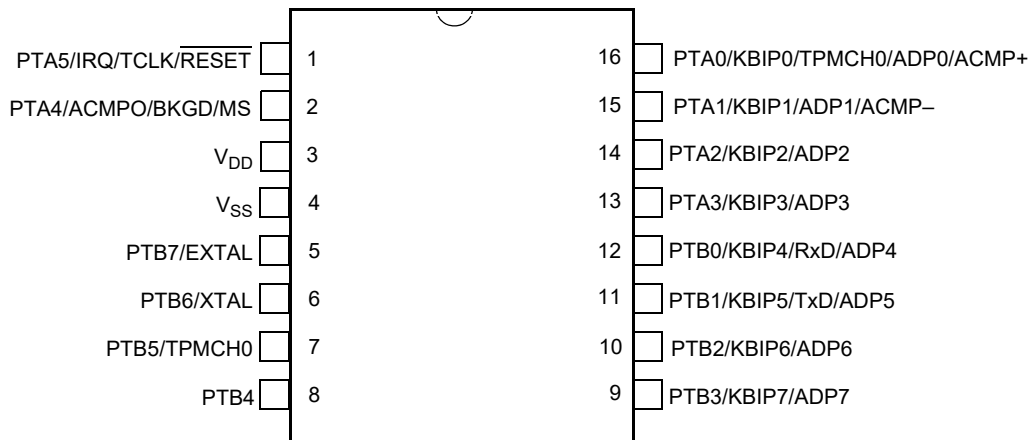
<sup>2</sup> If ADC and ACMP are enabled, both modules will have access to the pin.

## Pin Assignments



Pins shown in bold type are lost in the next lower pin count package.

**Figure 2. MC9S08QL8 Series in 20-Pin TSSOP Package**



**Figure 3. MC9S08QL8 Series in 16-Pin TSSOP Package**

## 4 Electrical Characteristics

### 4.1 Introduction

This chapter contains electrical and timing specifications for the MC9S08QL8 series of microcontrollers available at the time of publication.

### 4.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 3. Parameter Classifications**

<b>P</b>	Those parameters are guaranteed during production testing on each individual device.
<b>C</b>	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
<b>T</b>	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
<b>D</b>	Those parameters are derived mainly from simulations.

#### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

### 4.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 4](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to 3.8	V
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Digital input voltage	$V_{In}$	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	±25	mA
Storage temperature range	$T_{stg}$	-55 to 150	°C

- <sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.
- <sup>2</sup> All functional non-supply pins, except for PTA5 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .
- <sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

## 4.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	$T_A$	$T_L$ to $T_H$ -40 to 85	°C
Maximum junction temperature	$T_{JM}$	95	°C
Thermal resistance 16-pin TSSOP	$\theta_{JA}$	129	°C/W

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

$T_A$  = Ambient temperature, °C

$\theta_{JA}$  = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$



$P_{\text{int}} = I_{\text{DD}} \times V_{\text{DD}}$ , Watts — chip internal power

$P_{\text{I/O}}$  = Power dissipation on input and output pins — user determined

For most applications,  $P_{\text{I/O}} \ll P_{\text{int}}$  and can be neglected. An approximate relationship between  $P_{\text{D}}$  and  $T_{\text{J}}$  (if  $P_{\text{I/O}}$  is neglected) is:

$$P_{\text{D}} = K \div (T_{\text{J}} + 273^{\circ}\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_{\text{D}} \times (T_{\text{A}} + 273^{\circ}\text{C}) + \theta_{\text{JA}} \times (P_{\text{D}})^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring  $P_{\text{D}}$  (at equilibrium) for a known  $T_{\text{A}}$ . Using this value of K, the values of  $P_{\text{D}}$  and  $T_{\text{J}}$  can be obtained by solving Equation 1 and Equation 2 iteratively for any value of  $T_{\text{A}}$ .

## 4.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

**Table 6. ESD and Latch-up Test Conditions**

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	$\Omega$
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	$\Omega$
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{\text{HBM}}$	$\pm 2000$	—	V
2	Charge device model (CDM)	$V_{\text{CDM}}$	$\pm 500$	—	V
3	Latch-up current at $T_A = 85^\circ\text{C}$	$I_{\text{LAT}}$	$\pm 100$	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## 4.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typical <sup>1</sup>	Max	Unit
1	P	Operating Voltage	$V_{\text{DD}}$	—	1.8	—	3.6	V
2	C	Output high voltage	$V_{\text{OH}}$	All I/O pins, low-drive strength $V_{\text{DD}} > 1.8\text{ V}$ , $I_{\text{Load}} = -2\text{ mA}$	$V_{\text{DD}} - 0.5$	—	—	V
	P			All I/O pins, high-drive strength $V_{\text{DD}} > 2.7\text{ V}$ , $I_{\text{Load}} = -10\text{ mA}$	$V_{\text{DD}} - 0.5$	—	—	
	C			$V_{\text{DD}} > 1.8\text{ V}$ , $I_{\text{Load}} = -2\text{ mA}$	$V_{\text{DD}} - 0.5$	—	—	
3	D	Output high current Max total $I_{\text{OH}}$ for all ports	$I_{\text{OHT}}$	$V_{\text{OUT}} < V_{\text{DD}}$	0	—	-80	mA
4	C	Output low voltage	$V_{\text{OL}}$	All I/O pins, low-drive strength $V_{\text{DD}} > 1.8\text{ V}$ , $I_{\text{Load}} = 0.6\text{ mA}$	—	—	0.5	V
	P			All I/O pins, high-drive strength $V_{\text{DD}} > 2.7\text{ V}$ , $I_{\text{Load}} = 10\text{ mA}$	—	—	0.5	
	C			$V_{\text{DD}} > 1.8\text{ V}$ , $I_{\text{Load}} = 3\text{ mA}$	—	—	0.5	
5	D	Output low current Max total $I_{\text{OL}}$ for all ports	$I_{\text{OLT}}$	$V_{\text{OUT}} > V_{\text{SS}}$	0	—	80	mA
6	P	Input high voltage all digital inputs	$V_{\text{IH}}$	$V_{\text{DD}} > 2.7\text{ V}$	$0.70 \times V_{\text{DD}}$	—	—	V
	C			$V_{\text{DD}} > 1.8\text{ V}$	$0.85 \times V_{\text{DD}}$	—	—	
7	P	Input low voltage all digital inputs	$V_{\text{IL}}$	$V_{\text{DD}} > 2.7\text{ V}$	—	—	$0.35 \times V_{\text{DD}}$	
	C			$V_{\text{DD}} > 1.8\text{ V}$	—	—	$0.30 \times V_{\text{DD}}$	
8	C	Input hysteresis all digital inputs	$V_{\text{hys}}$	—	$0.06 \times V_{\text{DD}}$	—	—	mV
9	P	Input leakage current all input only pins (Per pin)	$I_{\text{In}}$	$V_{\text{In}} = V_{\text{DD}}$ or $V_{\text{SS}}$	—	—	200	nA
10	P	Hi-Z (off-state) leakage current all input/output (per pin)	$ I_{\text{OZ}} $	$V_{\text{In}} = V_{\text{DD}}$ or $V_{\text{SS}}$	—	—	200	nA

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typical <sup>1</sup>	Max	Unit
10	C	Total leakage combined for all inputs and Hi-Z pins All input only and I/O	$ I_{OZTOT} $	$V_{IN} = V_{DD}$ or $V_{SS}$	—	—	2	$\mu A$
11	P	Pullup, Pulldown resistors all digital inputs except PTA5/IRQ/TCLK/RESET, when enabled	$R_{PU}$ , $R_{PD}$	—	17.5	—	52.5	$k\Omega$
12	C	Pullup, Pulldown resistors PTA5/IRQ/TCLK/RESET, when enabled <sup>2</sup>	$R_{PU}$ , $R_{PD}$	—	17.5	—	52.5	$k\Omega$
13	D	DC injection current <sup>3, 4, 5</sup> Single pin limit Total MCU limit, includes sum of all stressed pins	$I_{IC}$	$V_{IN} < V_{SS}$ , $V_{IN} > V_{DD}$	-0.2	—	0.2	$mA$
					-5	—	5	$mA$
14	C	Input Capacitance, all pins	$C_{In}$	—	—	—	8	$pF$
15	C	RAM retention voltage	$V_{RAM}$	—	—	0.6	1.0	V
16	C	POR re-arm voltage <sup>6</sup>	$V_{POR}$	—	0.9	1.4	2.0	V
17	D	POR re-arm time	$t_{POR}$	—	10	—	—	$\mu s$
18	P	Low-voltage detection threshold	$V_{LVD}$	$V_{DD}$ falling	1.80	1.84	1.88	V
				$V_{DD}$ rising	1.88	1.92	1.96	
19	P	Low-voltage warning threshold	$V_{LW}$	$V_{DD}$ falling	2.08	2.14	2.26	V
				$V_{DD}$ rising	2.08	2.14	2.26	
20	C	Low-voltage inhibit reset/recover hysteresis	$V_{hys}$	—	—	80	—	$mV$
21	P	Bandgap Voltage Reference <sup>7</sup>	$V_{BG}$	—	1.15	1.17	1.18	V

<sup>1</sup> Typical values are measured at 25 °C. Characterized, not tested

<sup>2</sup> The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear lower when measured externally on the pin.

<sup>3</sup> All functional non-supply pins, except for PTA5 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

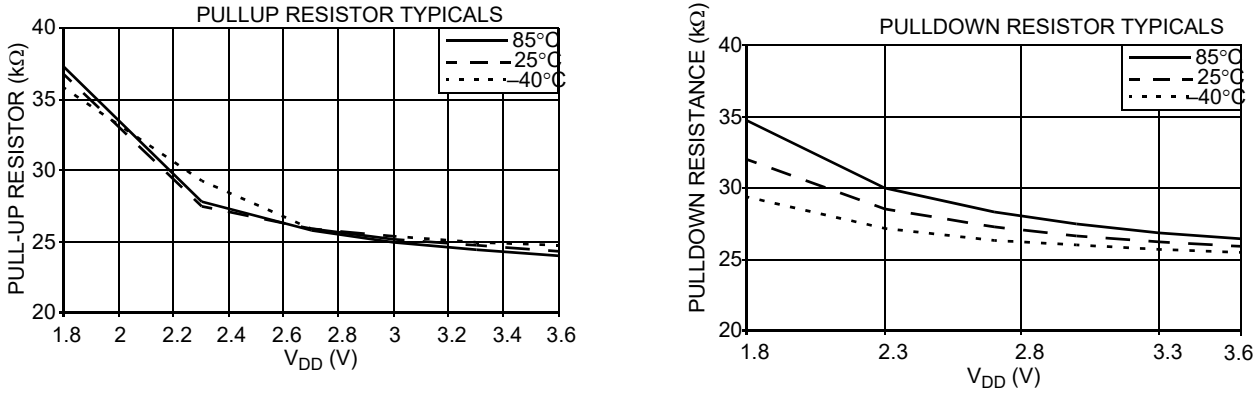
<sup>4</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>5</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If the positive injection current ( $V_{IN} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure that external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

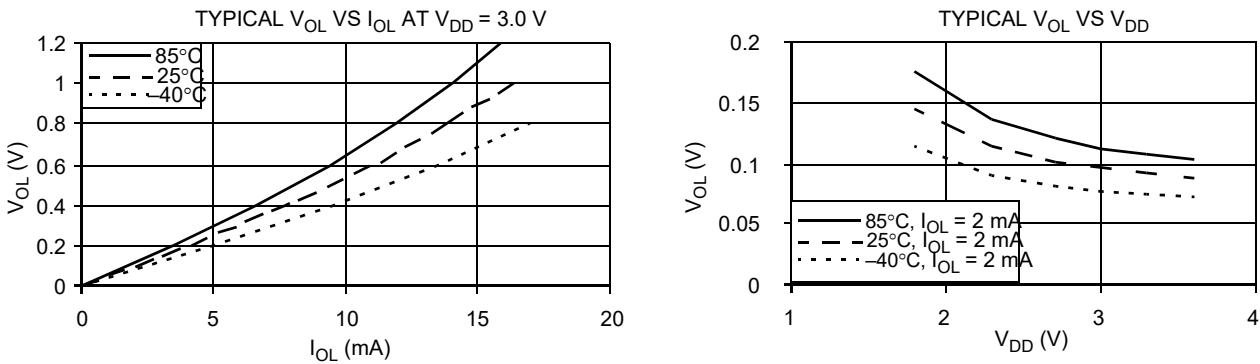
<sup>6</sup> Maximum is highest voltage that POR is guaranteed.

<sup>7</sup> Factory trimmed at  $V_{DD} = 3.0$  V, Temp = 25 °C

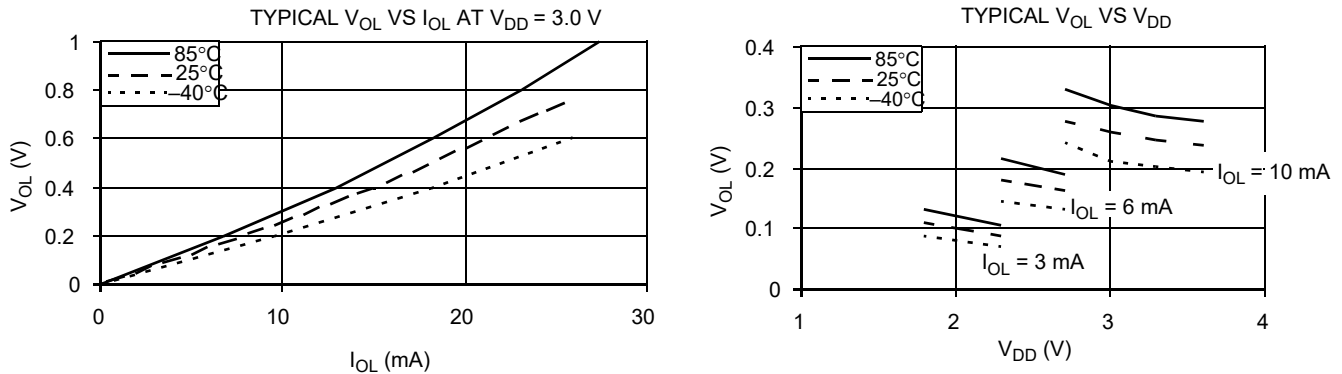
**Electrical Characteristics**



**Figure 4. Pullup and Pulldown Typical Resistor Values (V<sub>DD</sub> = 3.0 V)**



**Figure 5. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)**



**Figure 6. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)**

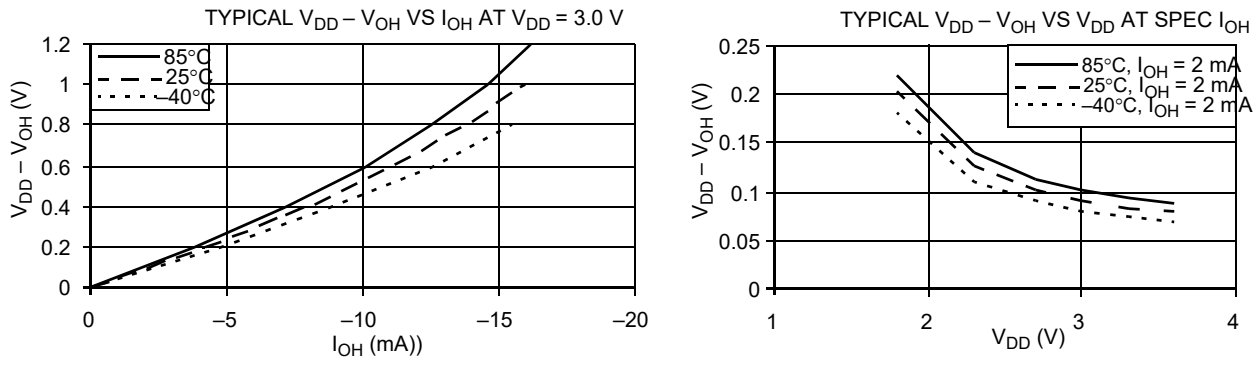


Figure 7. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

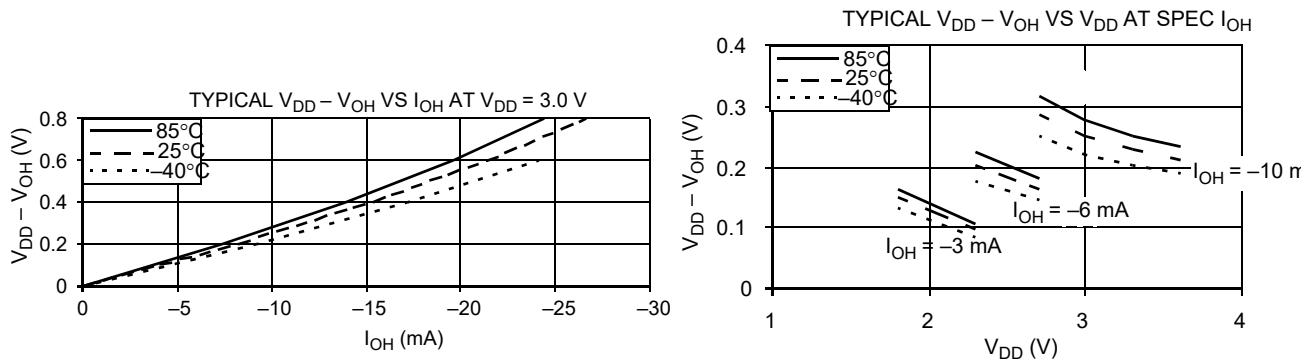


Figure 8. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

## 4.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

**Table 9. Supply Current Characteristics**

Num	C	Parameter	Symbol	Bus Freq	V <sub>DD</sub> (V)	Typical <sup>1</sup>	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	R <sub>I</sub> DD	10 MHz	3	5.60	6	mA	-40 to 85°C
	T			1 MHz		0.80	—		
2	T	Run supply current FEI mode, all modules off	R <sub>I</sub> DD	10 MHz	3	3.60	—	mA	-40 to 85°C
	T			1 MHz		0.75	—		
3	T	Run supply current LPRS=0, all modules off	R <sub>I</sub> DD	16 kHz FBILP	3	165	—	μA	-40 to 85°C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS=1, all modules off	R <sub>I</sub> DD	16 kHz FBELP	3	7.3	—	μA	-40 to 85°C
5	T	Wait mode supply current FEI mode, all modules off	W <sub>I</sub> DD	10 MHz	3	570	—	μA	-40 to 85°C
	T			1 MHz		290	—		
6	T	Wait mode supply current LPRS = 1, all mods off	W <sub>I</sub> DD	16 kHz FBELP	3	1	—	μA	-40 to 85°C
7	P	Stop2 mode supply current	S2 <sub>I</sub> DD	—	3	0.25	0.65	μA	-40 to 25°C
	C			—		0.5	0.8		70°C
	P			—		1	2		85°C
	C			—	2	0.2	0.5		-40 to 25°C
	C			—		0.3	0.6		70°C
	C			—		0.7	1.6		85°C
8	P	Stop3 mode supply current no clocks active	S3 <sub>I</sub> DD	—	3	0.45	0.80	μA	-40 to 25°C
	C			—		1	1.8		70°C
	P			—		3	5.8		85°C
	C			—	2	0.3	0.6		-40 to 25°C
	C			—		0.8	1.5		70°C
	C			—		2.5	5.0		85°C

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				-40°C	25°C	70°C	85°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN <sup>1</sup>	—	63	70	77	81	μA
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD <sup>1</sup>	LVDSE = 1	90	100	110	115	μA
6	T	ACMP <sup>1</sup>	Not using the bandgap (BGBE = 0)	18	20	22	23	μA
7	T	ADC <sup>1</sup>	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	μA

<sup>1</sup> Not available in stop2 mode.

## 4.8 External Oscillator (XOSC) Characteristics

Reference [Figure 9](#) and [Figure 10](#) for crystal or resonator circuits.

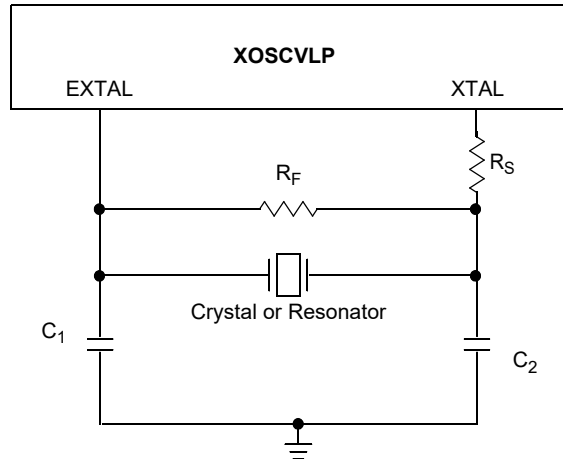
Table 11. XOSCVLP and ICS Specifications (Temperature Range = -40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	$f_{lo}$ $f_{hi}$ $f_{hi}$	32 1 1	— — —	38.4 16 8	kHz MHz MHz
		Low range (RANGE = 0)					
		High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)					
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	$C_1, C_2$	See Note <sup>2</sup> See Note <sup>3</sup>			
3	D	Feedback resistor Low range, low power (RANGE = 0, HGO = 0) <sup>2</sup> Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)	$R_F$	— — —	— 10 1	— — —	MΩ
4	D	Series resistor —	$R_S$	— — — —	— 100 0 0	— — — 0	kΩ
		Low range, low power (RANGE = 0, HGO = 0) <sup>2</sup>					
		Low range, high gain (RANGE = 0, HGO = 1)					
		High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz					
5	C	Crystal start-up time <sup>4</sup>	$t_{CSTL}$ $t_{CSTH}$	— — — —	600 400 5 15	— — — —	ms
		Low range, low power					
		Low range, high gain					
		High range, low power High range, high gain					

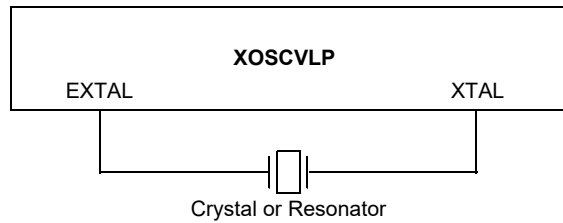
**Table 11. XOSCVLP and ICS Specifications (Temperature Range = -40 to 85°C Ambient)**

Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	$f_{\text{extal}}$	0.03125 0	— —	20 20	MHz

- <sup>1</sup> Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.
- <sup>2</sup> Load capacitors ( $C_1, C_2$ ), feedback resistor ( $R_F$ ) and series resistor ( $R_S$ ) are incorporated internally when RANGE = HGO = 0.
- <sup>3</sup> See crystal or resonator manufacturer's recommendation.
- <sup>4</sup> Proper PC board layout procedures must be followed to achieve specifications.



**Figure 9. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain**



**Figure 10. Typical Crystal or Resonator Circuit: Low Range/Low Power**



## 4.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical <sup>1</sup>	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at $V_{DD} = 3.6$ V and temperature = 25 °C	$f_{int\_t}$	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed	$f_{int\_ut}$	31.25	—	39.06	kHz
3	T	Internal reference start-up time	$t_{IRST}$	—	60	100	μs
4	P	DCO output frequency range — trimmed <sup>2</sup>   Low range (DRS = 00)	$f_{dco\_t}$	16	—	20	MHz
5	P	DCO output frequency <sup>2</sup> Reference = 32768 Hz and DMX32 = 1	$f_{dco\_DMX32}$	—	19.92	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	% $f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	% $f_{dco}$
8	C	Total deviation of DCO output from trimmed frequency <sup>3</sup> Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	$\Delta f_{dco\_t}$	—	–1.0 to 0.5 ±0.5	± 2 ± 1	% $f_{dco}$
10	C	FLL acquisition time <sup>4</sup>	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) <sup>5</sup>	$C_{Jitter}$	—	0.02	0.2	% $f_{dco}$

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

<sup>2</sup> The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

<sup>3</sup> This parameter is characterized and not tested on each device.

<sup>4</sup> This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

<sup>5</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{BUS}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via  $V_{DD}$  and  $V_{SS}$  and variation in crystal oscillator frequency increase the  $C_{Jitter}$  percentage for a given interval.

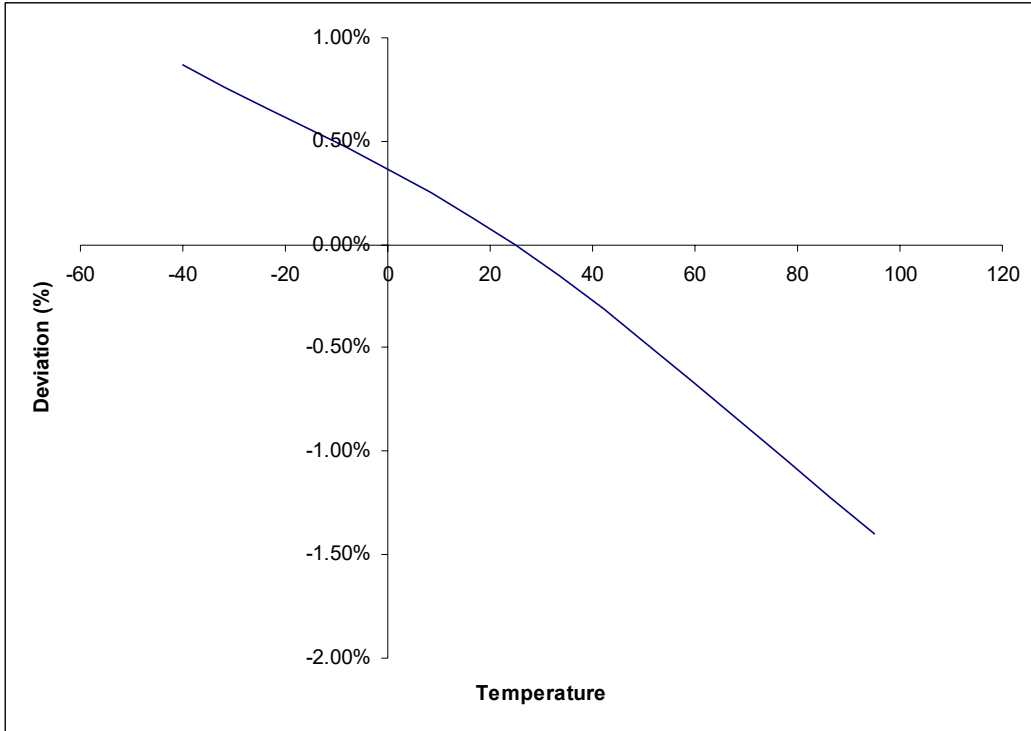


Figure 11. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

## 4.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

### 4.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	D	Bus frequency ( $t_{cyc} = 1/f_{Bus}$ )	$f_{Bus}$	DC	—	10	MHz
2	D	Internal low power oscillator period	$t_{LPO}$	700	—	1300	$\mu s$
3	D	External reset pulse width <sup>2</sup>	$t_{extrst}$	100	—	—	ns
4	D	Reset low drive	$t_{rstdrv}$	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	$t_{MSSU}$	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes <sup>3</sup>	$t_{MSH}$	100	—	—	$\mu s$
7	D	IRQ pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>4</sup>	$t_{LIH}, t_{HIL}$	100 $1.5 \times t_{cyc}$	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>4</sup>	$t_{LIH}, t_{HIL}$	100 $1.5 \times t_{cyc}$	— —	— —	ns
9	D	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) <sup>5</sup> Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{Rise},$ $t_{Fall}$	— —	16 23	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) <sup>5</sup> Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	$t_{Rise},$ $t_{Fall}$	— —	5 9	— —	ns
10	D	Voltage regulator recovery time	$t_{VRR}$	—	4	—	$\mu s$

<sup>1</sup> Typical values are based on characterization data at  $V_{DD} = 3.0 V$ , 25 °C unless otherwise stated.

<sup>2</sup> This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

<sup>3</sup> To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of  $t_{MSH}$  after  $V_{DD}$  rises above  $V_{LVD}$ .

<sup>4</sup> This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

<sup>5</sup> Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range –40°C to 85°C.

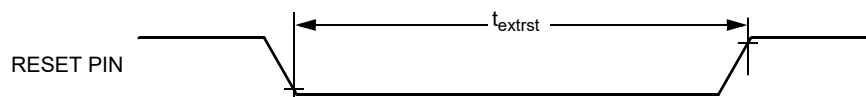


Figure 12. Reset Timing

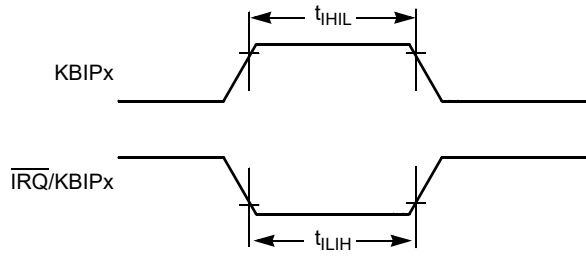


Figure 13.  $\overline{\text{IRQ}}/\text{KBIPx}$  Timing

### 4.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	$f_{\text{TEXT}}$	DC	$1/4 f_{\text{op}}$	MHz
2	D	External clock period	$t_{\text{TEXT}}$	4	—	$t_{\text{CYC}}$
3	D	External clock high time	$t_{\text{TCLKH}}$	1.5	—	$t_{\text{CYC}}$
4	D	External clock low time	$t_{\text{TCLKL}}$	1.5	—	$t_{\text{CYC}}$
5	D	Input capture pulse width	$f_{\text{CPW}}$	1.5	—	$t_{\text{CYC}}$

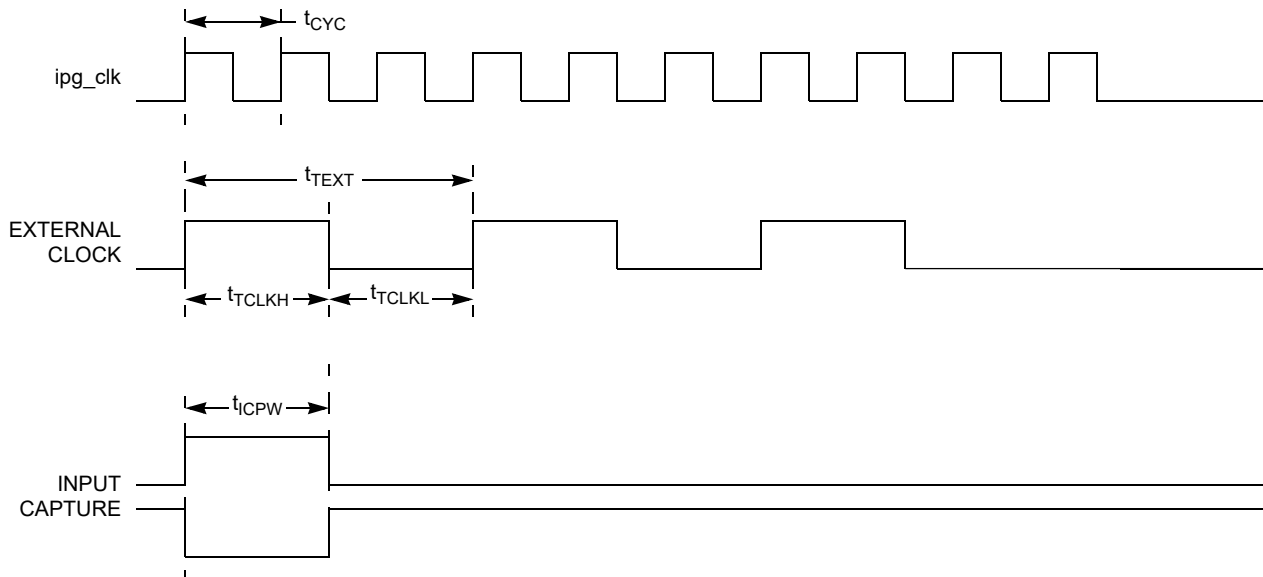


Figure 14. Timer Input Capture Pulse

## 4.11 Analog Comparator (ACMP) Electricals

Table 15. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	$V_{PWR}$	1.8	—	3.6	V
D	Supply current (active)	$I_{DDAC}$	—	20	35	$\mu\text{A}$
D	Analog input voltage	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DD}$	V
P	Analog input offset voltage	$V_{AIO}$	—	20	40	mV
C	Analog comparator hysteresis	$V_H$	3.0	9.0	15.0	mV
P	Analog input leakage current	$I_{ALKG}$	—	—	1.0	$\mu\text{A}$
C	Analog comparator initialization delay	$t_{AINIT}$	—	—	1.0	$\mu\text{s}$

## 4.12 ADC Characteristics

Table 16. 12-Bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDA}$	1.8	—	3.6	V	
	Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ ) <sup>2</sup>	$\Delta V_{DDA}$	-100	0	100	mV	
Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSA}$ ) <sup>2</sup>	$\Delta V_{SSA}$	-100	0	100	mV	
Supply Current	Stop, Reset, Module Off	$I_{DDAD}$	—	0.007	0.8	$\mu\text{A}$	
Input Voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	
Input Capacitance		$C_{ADIN}$	—	4.5	5.5	pF	
Input Resistance		$R_{ADIN}$	—	5	7	k $\Omega$	
Analog Source Resistance	12 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	$R_{AS}$	—	—	2	k $\Omega$	External to MCU
	10 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		—	—	5		
	8 bit mode (all valid $f_{ADCK}$ )		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	$f_{ADCK}$	0.4	—	8.0	MHz	
	Low Power (ADLPC = 1)		0.4	—	4.0		

<sup>1</sup> Typical values assume  $V_{DDA} = 3.0\text{ V}$ ,  $\text{Temp} = 25\text{ }^\circ\text{C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> DC potential difference.

**NOTE**

$V_{DDA}/V_{SSA}$  pins do not exist in package. The signals are derived internally by double bonding to  $V_{DD}/V_{SS}$  pair of pins.

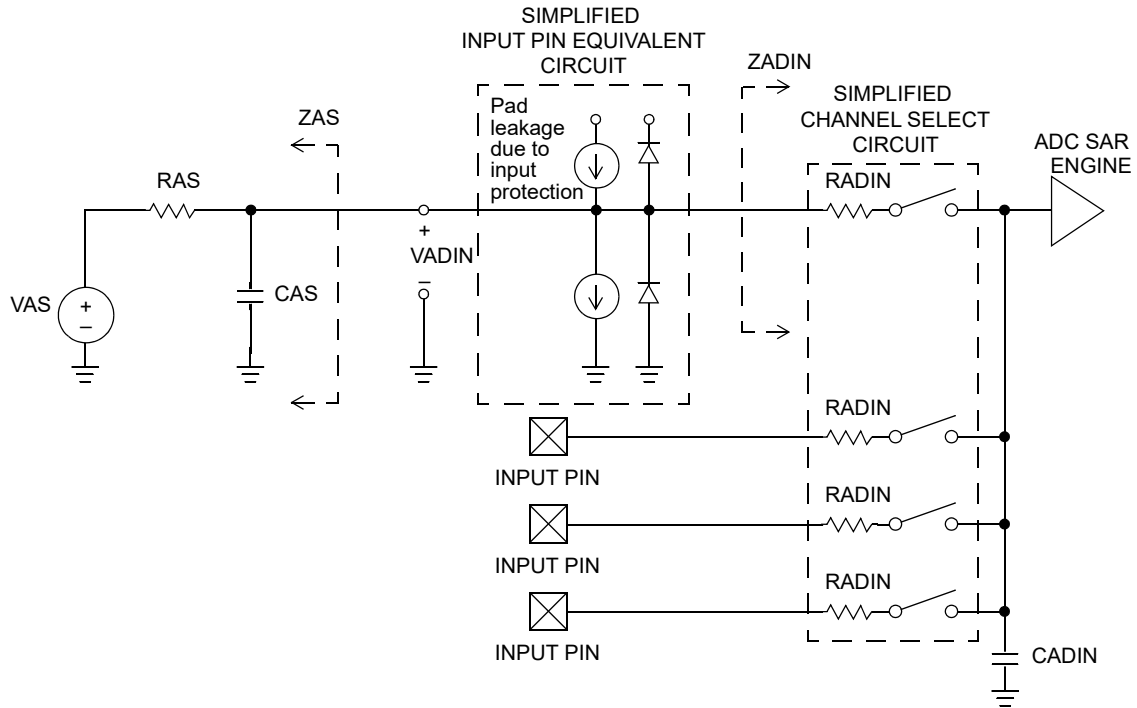


Figure 15. ADC Input Impedance Equivalency Diagram

Table 17. 12-Bit ADC Characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Characteristic	Conditions	C	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	$I_{DDAD}$	—	120	—	$\mu\text{A}$	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	$I_{DDAD}$	—	202	—	$\mu\text{A}$	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	$I_{DDAD}$	—	288	—	$\mu\text{A}$	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		T	$I_{DDAD}$	—	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	T	$I_{DDAD}$	—	0.007	0.8	$\mu\text{A}$	
ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	P	$f_{ADACK}$	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC = 1)			1.25	2	3.3		
Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	T	$t_{ADC}$	—	20	—	ADCK cycles	See reference manual for conversion time variances
	Long Sample (ADLSMP = 1)			—	40	—		
Sample Time	Short Sample (ADLSMP = 0)	T	$t_{ADS}$	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP = 1)			—	23.5	—		
Total Unadjusted Error	12-bit mode	T	$E_{TUE}$	—	—	—	LSB <sup>2</sup>	Includes quantization
	10-bit mode	P		—	$\pm 1.5$	—		
	8-bit mode	T		—	$\pm 0.7$	—		
Differential Non-Linearity	12-bit mode	T	DNL	—	—	—	LSB <sup>2</sup>	
	10-bit mode	P		—	$\pm 0.5$	—		
	8-bit mode	T		—	$\pm 0.3$	—		
Monotonicity and No-Missing-Codes guaranteed								
Integral Non-Linearity	12-bit mode	T	INL	—	—	—	LSB <sup>2</sup>	
	10-bit mode	C		—	$\pm 0.5$	—		
	8-bit mode			—	$\pm 0.3$	—		

## Electrical Characteristics

**Table 17. 12-Bit ADC Characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Characteristic	Conditions	C	Symbol	Min	Typical <sup>1</sup>	Max	Unit	Comment
Zero-Scale Error	12-bit mode	C	$E_{ZS}$	—	—	—	LSB <sup>2</sup>	$V_{ADIN} = V_{SSA}$
	10-bit mode	P		—	±1.5	±2.1		
	8-bit mode	T		—	±0.5	±0.7		
Full-Scale Error	12-bit mode	T	$E_{FS}$	—	—	—	LSB <sup>2</sup>	$V_{ADIN} = V_{DDA}$
	10-bit mode	T		—	±1	±1.5		
	8-bit mode	T		—	±0.5	±0.5		
Quantization Error	12-bit mode	D	$E_Q$	—	—	—	LSB <sup>2</sup>	
	10-bit mode			—	—	±0.5		
	8-bit mode			—	—	±0.5		
Input Leakage Error	12-bit mode	D	$E_{IL}$	—	—	—	LSB <sup>2</sup>	Pad leakage <sup>3*</sup> $R_{AS}$
	10-bit mode			0	±0.2	±4		
	8-bit mode			0	±0.1	±1.2		
Temp Sensor Slope	−40°C– 25°C	D	m	—	1.646	—	mV/°C	
	25°C– 85°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	$V_{TEMP25}$	—	701.2	—	mV	

<sup>1</sup> Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$

<sup>3</sup> Based on input pad leakage current. Refer to pad electricals.



## 4.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply. For more detailed information about program/erase operations, see the memory section.

**Table 18. Flash Characteristics**

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{\text{prog/erase}}$	1.8		3.6	V
D	Supply voltage for read operation	$V_{\text{Read}}$	1.8		3.6	V
D	Internal FCLK frequency <sup>1</sup>	$f_{\text{FCLK}}$	150		200	kHz
D	Internal FCLK period (1/FCLK)	$t_{\text{FcyC}}$	5		6.67	μs
D	Byte program time (random location) <sup>(2)</sup>	$t_{\text{prog}}$		9		$t_{\text{FcyC}}$
D	Byte program time (burst mode) <sup>(2)</sup>	$t_{\text{Burst}}$		4		$t_{\text{FcyC}}$
D	Page erase time <sup>2</sup>	$t_{\text{Page}}$		4000		$t_{\text{FcyC}}$
D	Mass erase time <sup>(2)</sup>	$t_{\text{Mass}}$		20,000		$t_{\text{FcyC}}$
D	Byte program current <sup>3</sup>	$RI_{\text{DDBP}}$	—	4	—	mA
D	Page erase current <sup>3</sup>	$RI_{\text{DDPE}}$	—	6	—	mA
C	Program/erase endurance <sup>4</sup> $T_L$ to $T_H = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $T = 25^\circ\text{C}$	—	10,000	— 100,000	—	cycles
C	Data retention <sup>5</sup>	$t_{\text{D\_ret}}$	15	100	—	years

<sup>1</sup> The frequency of this clock is controlled by a software setting.

<sup>2</sup> These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

<sup>3</sup> The program and erase currents are additional to the standard run  $I_{DD}$ . These values are measured at room temperatures with  $V_{DD} = 3.0$  V, bus frequency = 4.0 MHz.

<sup>4</sup> **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how NXP defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

<sup>5</sup> **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how NXP defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

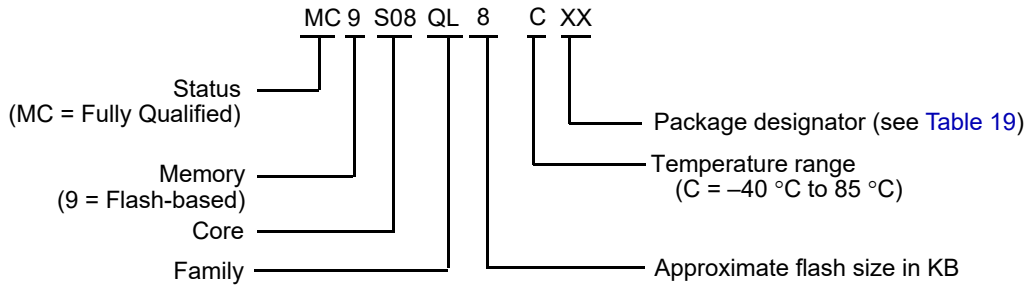
## **4.14 EMC Performance**

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult NXP applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

# 5 Part Identification

This section contains ordering information for the device numbering system.

Example of the device numbering system:



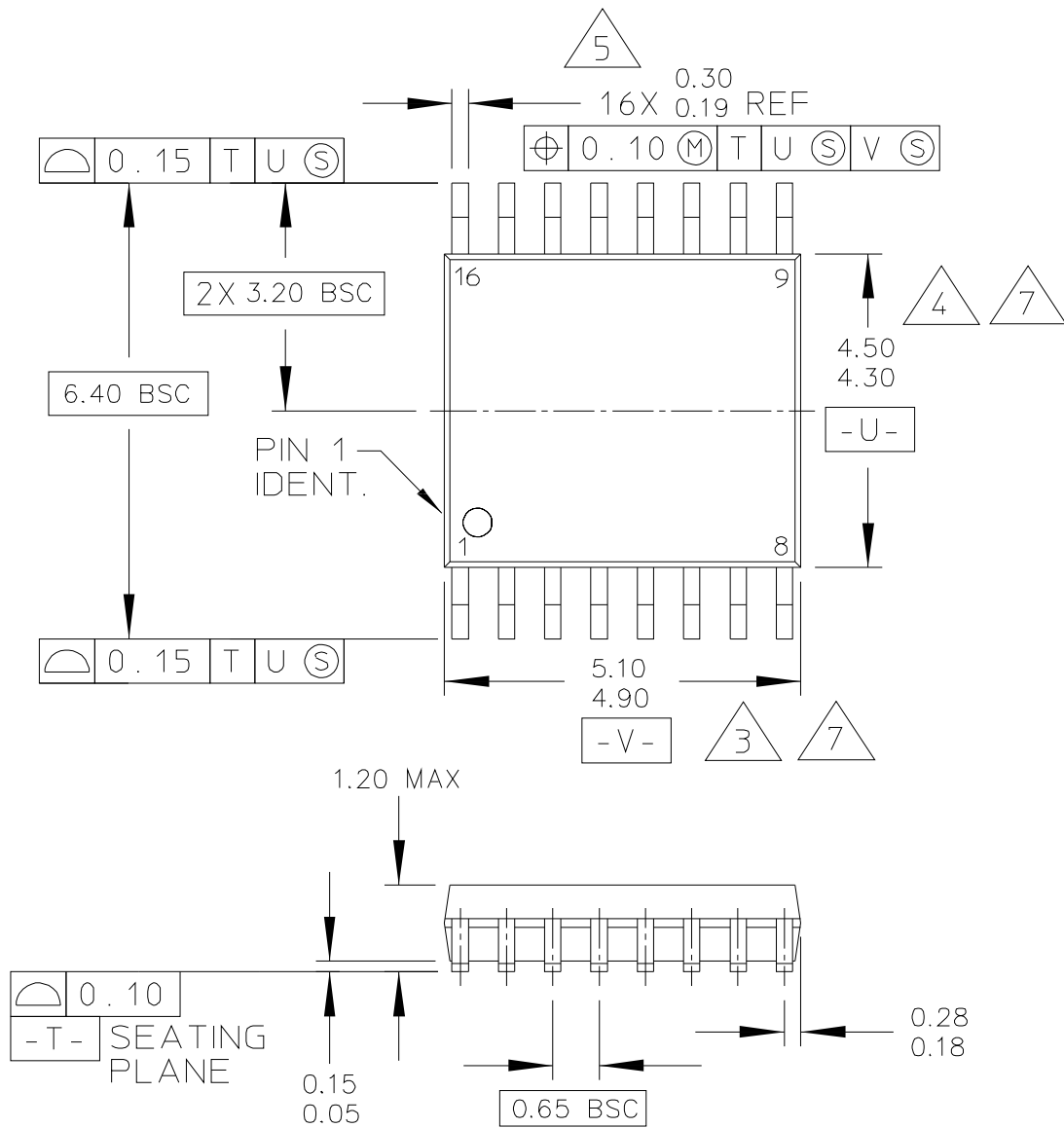
## 6 Package Information

**Table 19. Package Descriptions**

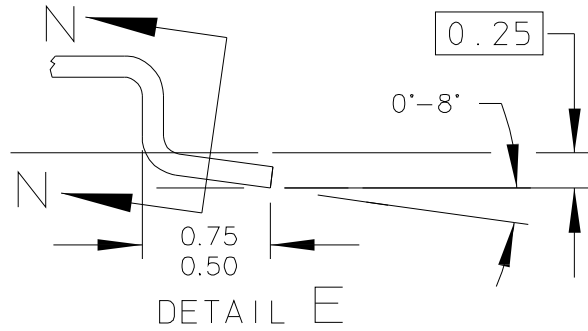
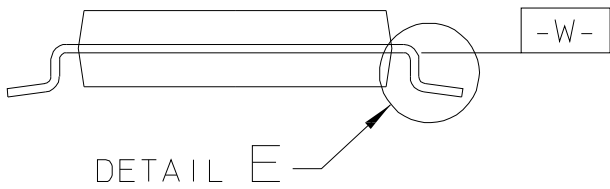
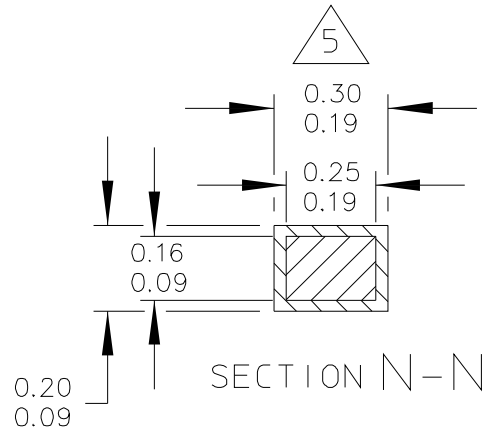
Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
20	Thin Shrink Small Outline Package	TSSOP	TJ	948E	98ASH70169A
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

### 6.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in [Table 19](#).



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TITLE:  16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A		REV: C
	STANDARD: JEDEC		
	SOT403-3	02 MAR 2016	



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TITLE:  16 LD TSSOP, PITCH 0.65MM		DOCUMENT NO: 98ASH70247A	REV: C
		STANDARD: JEDEC	
		SOT403-3	02 MAR 2016



NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

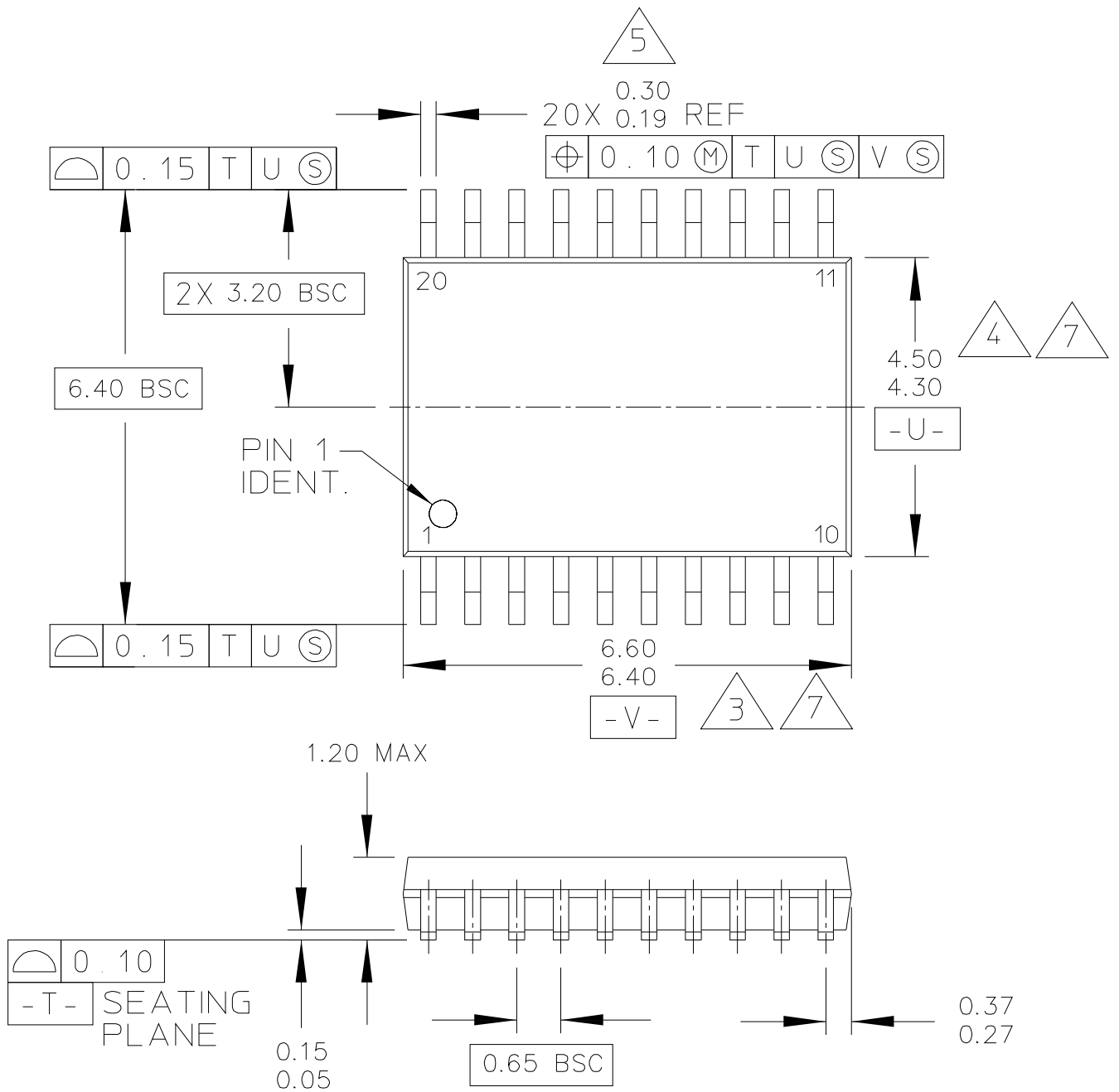
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

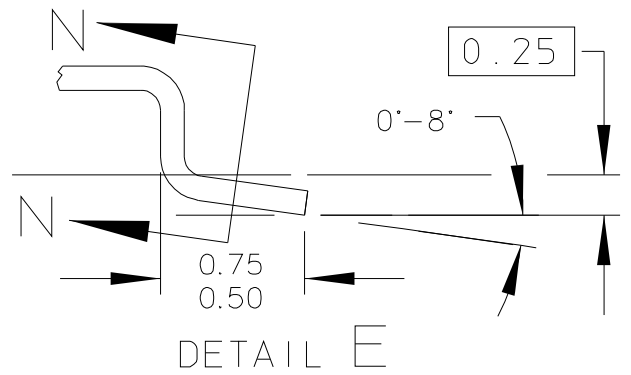
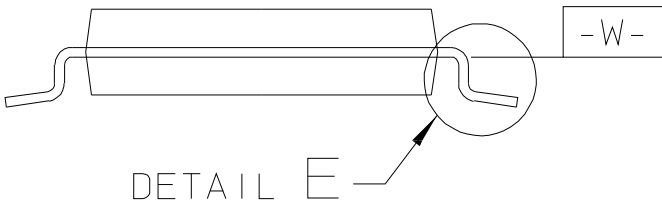
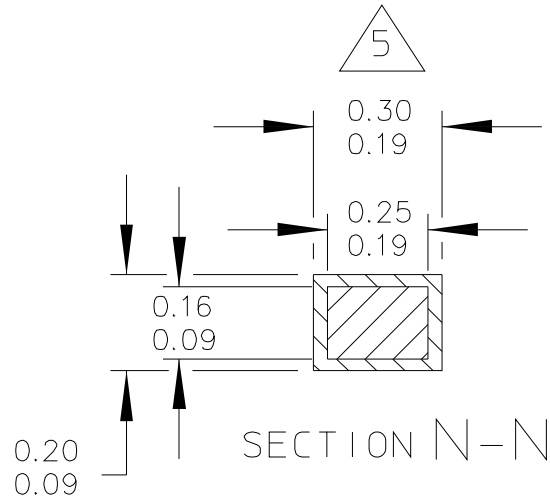
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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		STANDARD: JEDEC	
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NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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