

MCF5208 ColdFire® Microprocessor Data Sheet

Supports MCF5207 & MCF5208

by: Microcontroller Solutions Group

The MCF5207 and MCF5208 devices are highly-integrated, 32-bit microprocessors based on the version 2 ColdFire microarchitecture. Both devices contain a 16-Kbyte internal SRAM, an 8-Kbyte configurable cache, a 2-bank SDR/DDR SDRAM controller, a 16-channel DMA controller, up to three UARTs, a queued SPI, a low-power management mode module, and other peripherals that enable the MCF5207 and MCF5208 for use in industrial control and connectivity applications. The MCF5208 device also features a 10/100 Mbps fast ethernet controller.

This document provides detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of the MCF5207 and MCF5208 microprocessors. It was written from the perspective of the MCF5208 device. See the following section for a summary of differences between the two devices.

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1 MCF5207/8 Device Configurations

The following table compares the two devices described in this document:

Table 1. MCF5207 & MCF5208 Configurations

| Module | MCF5207 | MCF5208 |
|---|------------------------|-----------------------|
| Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit) | • | • |
| Core (System) Clock | up to 166.67 MHz | |
| Peripheral and External Bus Clock (Core clock ÷ 2) | up to 83.33 MHz | |
| Performance (Dhrystone/2.1 MIPS) | up to 159 | |
| Instruction/Data Cache | 8 Kbytes | |
| Static RAM (SRAM) | 16 Kbytes | |
| SDR/DDR SDRAM Controller | • | • |
| Fast Ethernet Controller (FEC) | — | • |
| Low-Power Management Module | • | • |
| UARTs | 3 | 3 |
| I ² C | • | • |
| QSPI | • | • |
| 32-bit DMA Timers | 4 | 4 |
| Watchdog Timer (WDT) | • | • |
| Periodic Interrupt Timers (PIT) | 4 | 4 |
| Edge Port Module (EPORT) | • | • |
| Interrupt Controllers (INTC) | 1 | 1 |
| 16-channel Direct Memory Access (DMA) | • | • |
| FlexBus External Interface | • | • |
| General Purpose I/O Module (GPIO) | • | • |
| JTAG - IEEE [®] 1149.1 Test Access Port | • | • |
| Package | 144 LQFP 144 MAPBGA | 160 QFP 196 MAPBGA |

2 Ordering Information

Table 2. Orderable Part Numbers

| Freescale Part Number | Description | Speed | Temperature |
|-----------------------|---|------------|----------------|
| MCF5207CAG166 | MCF5207 RISC Microprocessor, 144 LQFP | 166.67 MHz | -40° to +85° C |
| MCF5207CVM166 | MCF5207 RISC Microprocessor, 144 MAPBGA | 166.67 MHz | -40° to +85° C |
| MCF5208CAB166 | MCF5208 RISC Microprocessor, 160 QFP | 166.67 MHz | -40° to +85° C |
| MCF5208CVM166 | MCF5208 RISC Microprocessor, 196 MAPBGA | 166.67 MHz | -40° to +85° C |

3 Signal Descriptions

The following table lists all the MCF5208 pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to [Section 4, “Mechanicals and Pinouts”](#) for package diagrams. For a more detailed discussion of the MCF5208 signals, consult the *MCF5208 Reference Manual* (MCF5208RM).

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

Table 3. MCF5207/8 Signal Information and Muxing

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir. ¹ | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|-----------------------------|------|---------------------------------|-------------|-------------------|----------------|------------------------------|-----------------------------------|------------------------------------|------------------------------------|
| Reset | | | | | | | | | |
| $\overline{\text{RESET}}^2$ | — | — | — | I | EVDD | 82 | J10 | 90 | J14 |
| $\overline{\text{RSTOUT}}$ | — | — | — | O | EVDD | 74 | M12 | 82 | N14 |
| Clock | | | | | | | | | |
| EXTAL | — | — | — | I | EVDD | 78 | K12 | 86 | L14 |
| XTAL | — | — | — | O | EVDD | 80 | J12 | 88 | K14 |
| FB_CLK | — | — | — | O | SDVDD | 34 | L1 | 40 | N1 |
| Mode Selection | | | | | | | | | |
| $\overline{\text{RCON}}^2$ | — | — | — | I | EVDD | 144 | C4 | 160 | C3 |
| DRAMSEL | — | — | — | I | EVDD | 79 | H10 | 87 | K11 |
| FlexBus | | | | | | | | | |
| A[23:22] | — | $\overline{\text{FB_CS}}[5:4]$ | — | O | SDVDD | 118, 117 | B9, A10 | 126, 125 | B11, A11 |
| A[21:16] | — | — | — | O | SDVDD | 116–114, 112, 108, 107 | C9, A11, B10, A12, C11, B11 | 124, 123, 122, 120, 116, 115 | B12, A12, A13, B13, B14, C13 |
| A[15:14] | — | SD_BA[1:0] ³ | — | O | SDVDD | 106, 105 | B12, C12 | 114, 113 | C14, D12 |
| A[13:11] | — | SD_A[13:11] ³ | — | O | SDVDD | 104–102 | D11, E10, D12 | 112, 111, 110 | D13, D14, E11 |
| A10 | — | — | — | O | SDVDD | 101 | C10 | 109 | E12 |

Table 3. MCF5207/8 Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir. ¹ | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|--------------------------------------|----------|---|-------------|-------------------|----------------|------------------------|---|-----------------------|--|
| A[9:0] | — | SD_A[9:0] ³ | — | O | SDVDD | 100–91 | E11, D9, E12, F10, F11, E9, F12, G10, G12, F9 | 108–99 | E13, E14, F11–F14, G11–G14 |
| D[31:16] | — | SD_D[31:16] ⁴ | — | I/O | SDVDD | 21–28, 40–47 | F1, F2, G1, G2, G4, G3, H1, H2, K3, L2, L3, K2, M3, J4, M4, K4 | 27–34, 46–53 | J4–J1, K4–K1, M3, N3, M4, N4, P4, L5, M5, N5 |
| D[15:0] | — | FB_D[31:16] ⁴ | — | I/O | SDVDD | 8–15, 51–58 | B2, B1, C2, C1, D2, D1, E2, E1, L5, K5, L6, J6, M6, J7, L7, K7 | 16–23, 57–64 | F3–F1, G4–G1, H1, N6, P6, L7, M7, N7, P7, N8, P8 |
| $\overline{BE}/\overline{BWE}$ [3:0] | PBE[3:0] | $\overline{SD_DQM}$ [3:0] ³ | — | O | SDVDD | 20, 48, 18, 50 | F4, L4, E3, J5 | 26, 54, 24, 56 | H2, P5, H4, M6 |
| \overline{OE} | PBUSCTL3 | — | — | O | SDVDD | 60 | J8 | 66 | M8 |
| \overline{TA}^2 | PBUSCTL2 | — | — | I | SDVDD | 90 | G11 | 98 | H14 |
| $\overline{R/W}$ | PBUSCTL1 | — | — | O | SDVDD | 59 | K6 | 65 | L8 |
| \overline{TS} | PBUSCTL0 | $\overline{DACK0}$ | — | O | SDVDD | 4 | B3 | 12 | E3 |
| Chip Selects | | | | | | | | | |
| $\overline{FB_CS}$ [3:2] | PCS[3:2] | — | — | O | SDVDD | 119, 120 | D7, A9 | — | C11, A10 |
| $\overline{FB_CS1}$ | PCS1 | $\overline{SD_CS1}$ | — | O | SDVDD | 121 | C8 | 127 | B10 |
| $\overline{FB_CS0}$ | — | — | — | O | SDVDD | 122 | B8 | 128 | C10 |
| SDRAM Controller | | | | | | | | | |
| SD_A10 | — | — | — | O | SDVDD | 37 | M1 | 43 | N2 |
| SD_CKE | — | — | — | O | SDVDD | 6 | C3 | 14 | E1 |
| SD_CLK | — | — | — | O | SDVDD | 31 | J1 | 37 | L1 |
| $\overline{SD_CLK}$ | — | — | — | O | SDVDD | 32 | K1 | 38 | M1 |
| $\overline{SD_CS0}$ | — | — | — | O | SDVDD | 7 | A1 | 15 | F4 |
| SD_DQS[3:2] | — | — | — | O | SDVDD | 19, 49 | F3, M5 | 25, 55 | H3, L6 |
| $\overline{SD_SCAS}$ | — | — | — | O | SDVDD | 38 | M2 | 44 | P2 |
| $\overline{SD_SRAS}$ | — | — | — | O | SDVDD | 39 | J2 | 45 | P3 |
| SD_SDR_DQS | — | — | — | O | SDVDD | 29 | H3 | 35 | L3 |
| $\overline{SD_WE}$ | — | — | — | O | SDVDD | 5 | D3 | 13 | E2 |

Table 3. MCF5207/8 Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir. ¹ | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|--|-----------------------|-----------------------------|---------------------------|-------------------|----------------|------------------------|--------------------------|-----------------------|--------------------------|
| External Interrupts Port⁵ | | | | | | | | | |
| $\overline{\text{IRQ7}}^2$ | PIRQ7 ² | — | — | I | EVDD | 134 | A5 | 142 | C7 |
| $\overline{\text{IRQ4}}^2$ | PIRQ4 ² | $\overline{\text{DREQ0}}^2$ | — | I | EVDD | 133 | C6 | 141 | D7 |
| $\overline{\text{IRQ1}}^2$ | PIRQ1 ² | — | — | I | EVDD | 132 | B6 | 140 | D8 |
| FEC | | | | | | | | | |
| FEC_MDC | PFECI2C3 | I2C_SCL ² | U2TXD | O | EVDD | — | — | 148 | D6 |
| FEC_MDIO | PFECI2C2 | I2C_SDA ² | U2RXD | I/O | EVDD | — | — | 147 | C6 |
| FEC_TXCLK | PFECH7 | — | — | I | EVDD | — | — | 157 | B3 |
| — | PFECH6 | — | $\overline{\text{U1RTS}}$ | O | EVDD | 142 | A2 | — | — |
| FEC_TXEN | PFECH6 | — | $\overline{\text{U1RTS}}$ | O | EVDD | — | — | 158 | A2 |
| FEC_TXD0 | PFECH5 | — | — | O | EVDD | — | — | 3 | B1 |
| FEC_COL | PFECH4 | — | — | I | EVDD | — | — | 7 | D3 |
| FEC_RXCLK | PFECH3 | — | — | I | EVDD | — | — | 154 | B4 |
| FEC_RXDV | PFECH2 | — | — | I | EVDD | — | — | 153 | A4 |
| FEC_RXD0 | PFECH1 | — | — | I | EVDD | — | — | 152 | D5 |
| FEC_CRS | PFECH0 | — | — | I | EVDD | — | — | 8 | D2 |
| FEC_TXD[3:1] | PFECL[7:5] | — | — | O | EVDD | — | — | 6–4 | C1, C2, B2 |
| — | PFECL4 | — | $\overline{\text{U0RTS}}$ | O | EVDD | 141 | D5 | — | — |
| FEC_TXER | PFECL4 | — | $\overline{\text{U0RTS}}$ | O | EVDD | — | — | 156 | A3 |
| FEC_RXD[3:2] | PFECL[3:2] | — | — | I | EVDD | — | — | 149–150 | A5, B5 |
| — | PFECL1 | — | $\overline{\text{U1CTS}}$ | I | EVDD | 139 | B4 | — | — |
| FEC_RXD1 | PFECL1 | — | $\overline{\text{U1CTS}}$ | I | EVDD | — | — | 151 | C5 |
| — | PFECL0 | — | $\overline{\text{U0CTS}}$ | I | EVDD | 140 | E4 | — | — |
| FEC_RXER | PFECL0 | — | $\overline{\text{U0CTS}}$ | I | EVDD | — | — | 155 | C4 |
| Note: The MCF5207 does not contain an FEC module. However, the UART0 and UART1 control signals (as well as their GPIO signals) are available by setting the appropriate FEC GPIO port registers. | | | | | | | | | |
| I²C | | | | | | | | | |
| I2C_SDA ² | PFECI2C0 ² | U2RXD ² | — | I/O | EVDD | — | — | — | D1 |
| I2C_SCL ² | PFECI2C1 ² | U2TXD ² | — | I/O | EVDD | — | — | — | E4 |
| DMA | | | | | | | | | |
| $\overline{\text{DACK0}}$ and $\overline{\text{DREQ0}}$ do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and QSPI_CS2 for $\overline{\text{DACK0}}$, $\overline{\text{IRQ4}}$ and QSPI_DIN for $\overline{\text{DREQ0}}$. | | | | | | | | | |

Table 3. MCF5207/8 Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir. ¹ | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|--|---------|-----------------------------|---------------------------|-------------------|----------------|------------------------|--------------------------|-----------------------|--------------------------|
| QSPI | | | | | | | | | |
| QSPI_CS2 | PQSPI3 | $\overline{\text{DACK0}}$ | $\overline{\text{U2RTS}}$ | O | EVDD | 126 | A8 | 132 | D10 |
| QSPI_CLK | PQSPI0 | I2C_SCL ² | — | O | EVDD | 127 | C7 | 133 | A9 |
| QSPI_DOUT | PQSPI1 | I2C_SDA ² | — | O | EVDD | 128 | A7 | 134 | B9 |
| QSPI_DIN | PQSPI2 | $\overline{\text{DREQ0}}^2$ | $\overline{\text{U2CTS}}$ | I | EVDD | 129 | B7 | 135 | C9 |
| Note: The QSPI_CS1 and QSPI_CS0 signals are available on the U1CTS, U1RTS, U0CTS, or U0RTS pins for the 196 and 160-pin packages. | | | | | | | | | |
| UARTs | | | | | | | | | |
| $\overline{\text{U1CTS}}$ | PUARTL7 | DT1IN | QSPI_CS1 | I | EVDD | — | — | 136 | D9 |
| $\overline{\text{U1RTS}}$ | PUARTL6 | DT1OUT | QSPI_CS1 | O | EVDD | — | — | 137 | C8 |
| U1TXD | PUARTL5 | — | — | O | EVDD | 131 | A6 | 139 | A8 |
| U1RXD | PUARTL4 | — | — | I | EVDD | 130 | D6 | 138 | B8 |
| $\overline{\text{U0CTS}}$ | PUARTL3 | DT0IN | QSPI_CS0 | I | EVDD | — | — | 76 | N12 |
| $\overline{\text{U0RTS}}$ | PUARTL2 | DT0OUT | QSPI_CS0 | O | EVDD | — | — | 77 | P12 |
| U0TXD | PUARTL1 | — | — | O | EVDD | 71 | L10 | 79 | P13 |
| U0RXD | PUARTL0 | — | — | I | EVDD | 70 | M10 | 78 | N13 |
| Note: The UART2 signals are multiplexed on the DMA Timers, QSPI, FEC, and I2C pins. For the MCF5207 devices, the UART0 and UART1 control signals are multiplexed internally on the FEC signals. | | | | | | | | | |
| DMA Timers | | | | | | | | | |
| DT3IN | PTIMER3 | DT3OUT | $\overline{\text{U2CTS}}$ | I | EVDD | 135 | B5 | 143 | B7 |
| DT2IN | PTIMER2 | DT2OUT | $\overline{\text{U2RTS}}$ | I | EVDD | 136 | C5 | 144 | A7 |
| DT1IN | PTIMER1 | DT1OUT | U2RXD | I | EVDD | 137 | A4 | 145 | A6 |
| DT0IN | PTIMER0 | DT0OUT | U2TXD | I | EVDD | 138 | A3 | 146 | B6 |
| BDM/JTAG⁶ | | | | | | | | | |
| JTAG_EN ⁷ | — | — | — | I | EVDD | 83 | J11 | 91 | J13 |
| DSCLK | — | $\overline{\text{TRST}}^2$ | — | I | EVDD | 76 | K11 | 84 | L12 |
| PSTCLK | — | TCLK ² | — | O | EVDD | 64 | M7 | 70 | P9 |
| $\overline{\text{BKPT}}$ | — | TMS ² | — | I | EVDD | 75 | L12 | 83 | M14 |
| DSI | — | TDI ² | — | I | EVDD | 77 | H9 | 85 | K12 |
| DSO | — | TDO | — | O | EVDD | 69 | M9 | 75 | M12 |
| DDATA[3:0] | — | — | — | O | EVDD | — | K9, L9, M11, M8 | — | P11, N11, M11, P10 |
| PST[3:0] | — | — | — | O | EVDD | — | L11, L8, K10, K8 | — | N10, M10, L10, L9 |

Table 3. MCF5207/8 Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir. ¹ | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|-----------------------|------|-------------|-------------|-------------------|----------------|---|--------------------------------|---|---|
| ALLPST | — | — | — | O | EVDD | 67 | — | 73 | — |
| Test | | | | | | | | | |
| TEST ⁷ | — | — | — | I | EVDD | 109 | — | — | C12 |
| PLL_TEST | — | — | — | I | EVDD | — | — | — | M13 |
| Power Supplies | | | | | | | | | |
| EVDD | — | — | — | — | — | 1, 33, 63, 66, 72, 81, 87, 125 | E5–E6, F5, G8–G9, H7–H8 | 2, 9, 69, 72, 80, 89, 95, 131 | E5–E7, F5, F6, G5, H10, J9, J10, K8–K10, K13, M9 |
| IVDD | — | — | — | — | — | 30, 68, 84, 113, 143 | D4, D8, H4, H11, J9 | 36, 74, 92, 121, 159 | J12, D4, D11, H11, L4, L11, |
| PLL_VDD | — | — | — | — | — | 86 | H12 | 94 | H13 |
| SD_VDD | — | — | — | — | — | 3, 17, 35, 61, 89, 110, 123 | E7–E8, F8, G5, H5–H6, J3 | 11, 39, 41, 67, 97, 118, 129 | E8–E10, F9, F10, G10, H5, J5, J6, K5–K7, L2 |
| VSS | — | — | — | — | — | 2, 16, 36, 62, 65, 73, 88, 111, 124 | D10, F6–F7, G6–G7 | 1, 10, 42, 68, 71, 81, 96, 117, 119, 130 | A1, A14, F7–F8, G6–G9, H6–H9, J7–J8, L13, M2, N9, P1, P14 |
| PLL_VSS | — | — | — | — | — | 85 | — | 93 | H12 |

NOTES:

- ¹ Refers to pin's primary function.
- ² Pull-up enabled internally on this signal for this mode.
- ³ The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.
- ⁴ Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.
- ⁵ GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.
- ⁶ If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.
- ⁷ Pull-down enabled internally on this signal for this mode.

4 Mechanicals and Pinouts

Drawings in this section show the pinout and the packaging and mechanical characteristics of the MCF5207 and MCF5208 devices.

NOTE

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at <http://www.freescale.com/coldfire>.

4.1 Pinout—144 LQFP

Figure 1 shows a pinout of the MCF5207CAG166 device.

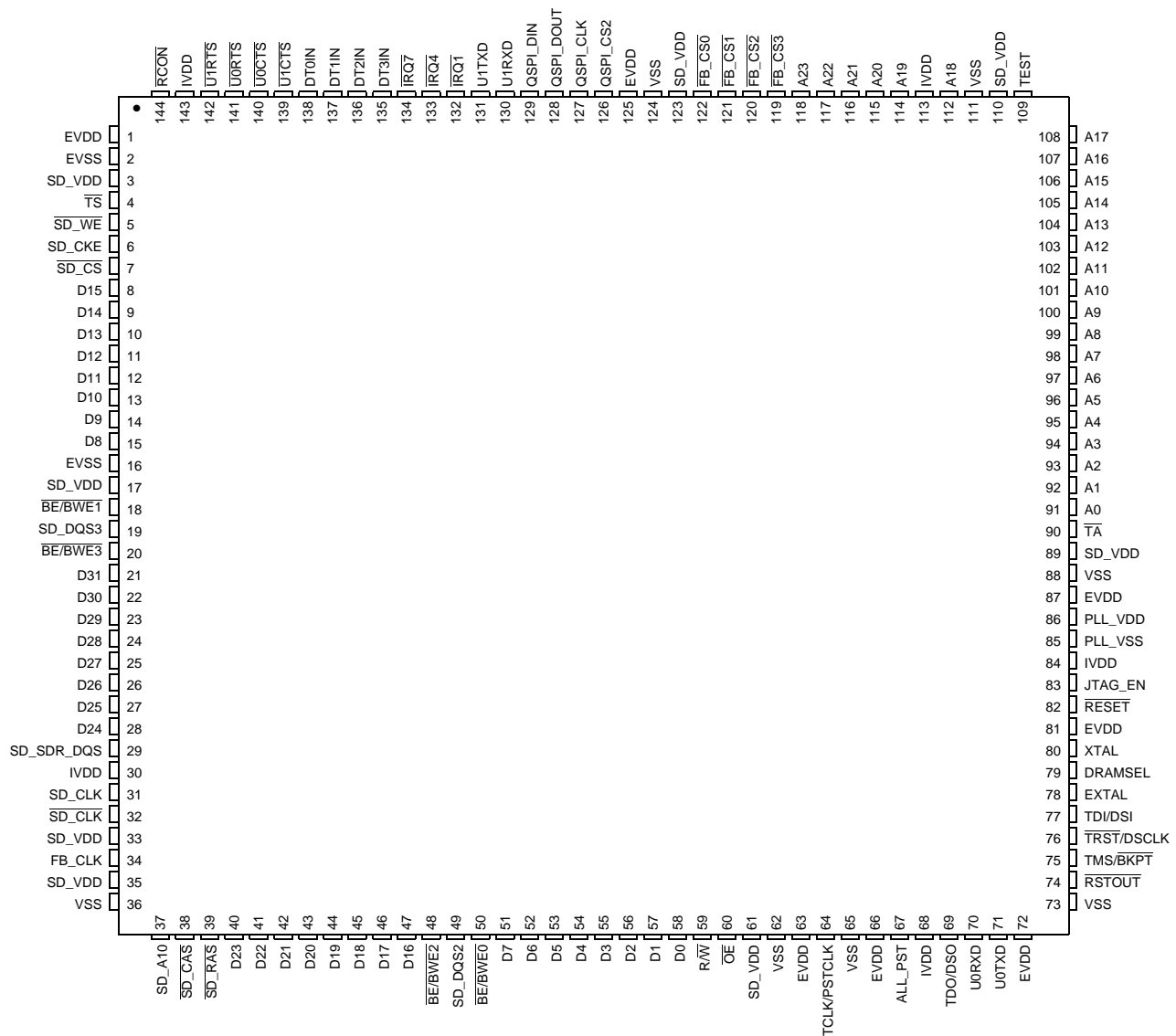


Figure 1. MCF5207CAG166 Pinout Top View (144 LQFP)

4.2 Package Dimensions—144 LQFP

Figure 2 and Figure 3 show MCF5207CAB166 package dimensions.

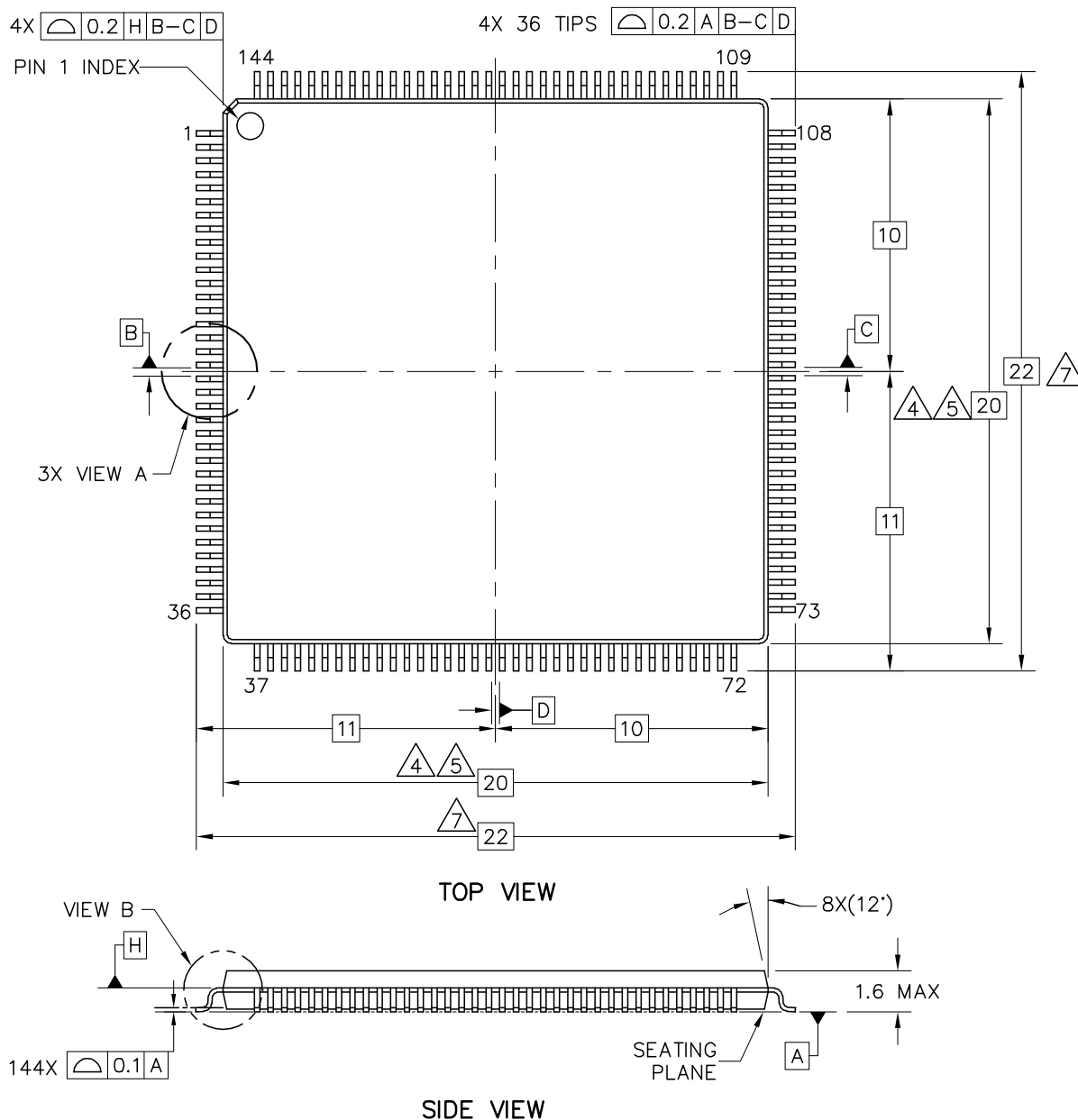
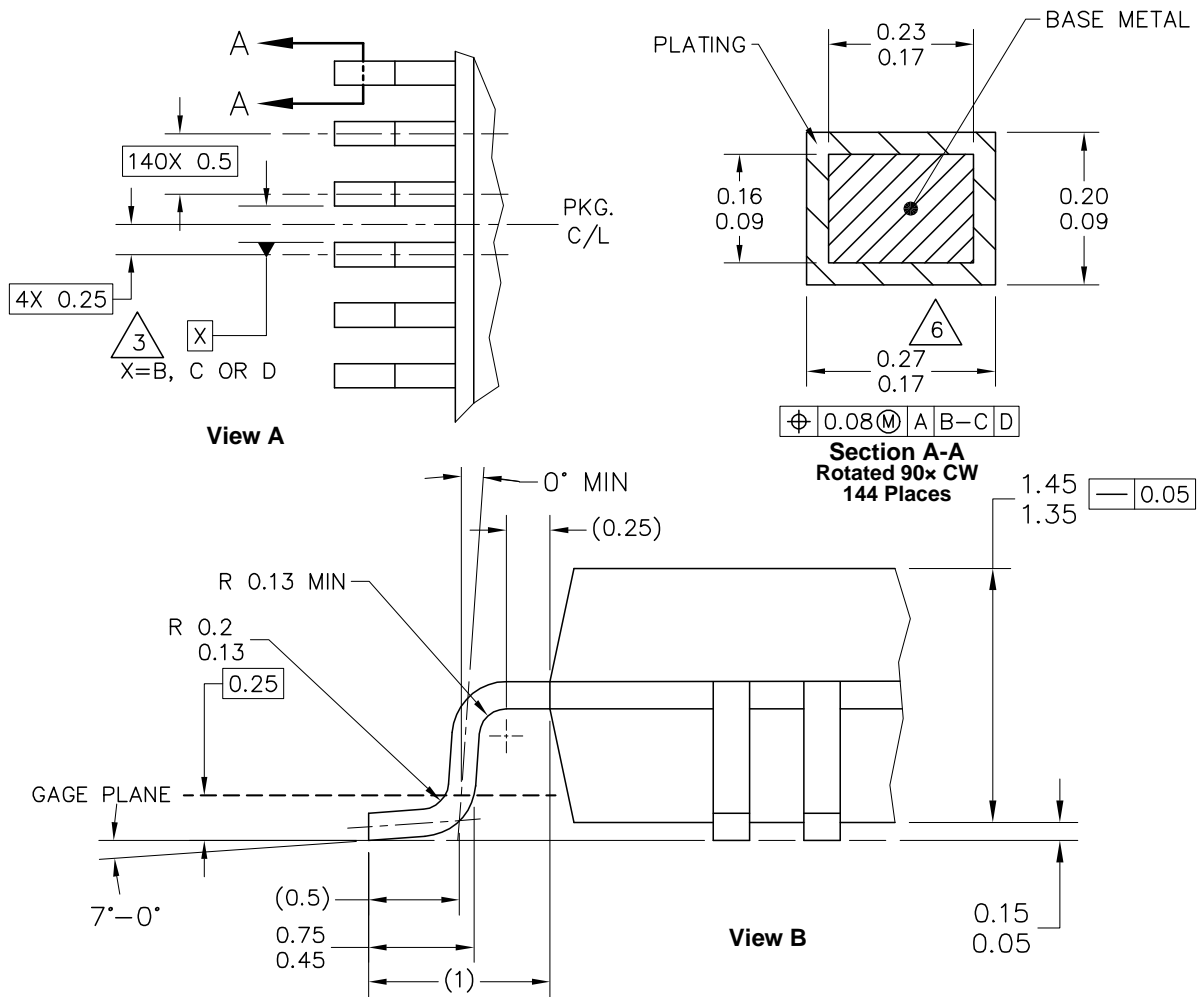


Figure 2. MCF5207CAB166 Package Dimensions (Sheet 1 of 2)



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 mm.
7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 3. MCF5207CAB166 Package Dimensions (Sheet 2 of 2)

4.3 Pinout—144 MAPBGA

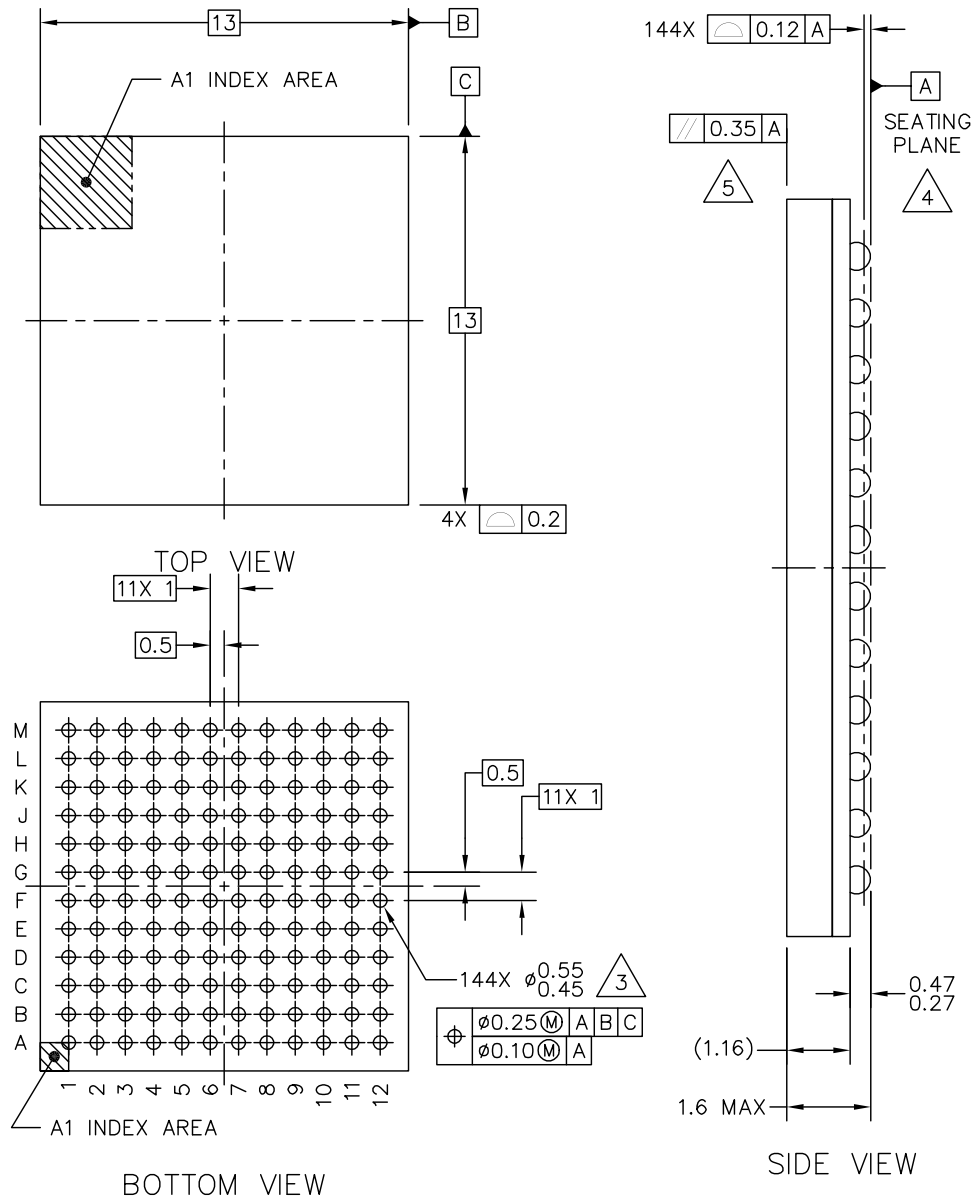
The pinout of the MCF5207CVM166 device is shown below.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|--------------------------|-----------------------------|-----------------------------|-----------------------------|---------------------------|--------------------------------|----------------------------|---|
| A | $\overline{\text{SD_CS}}$ | $\overline{\text{U1RTS}}$ | DT0IN | DT1IN | $\overline{\text{IRQ7}}$ | U1TXD | QSPI_DOUT | QSPI_CS2 | $\overline{\text{FB_CS2}}$ | A22 | A20 | A18 | A |
| B | D14 | D15 | $\overline{\text{TS}}$ | $\overline{\text{U1CTS}}$ | DT3IN | $\overline{\text{IRQ1}}$ | QSPI_DIN | $\overline{\text{FB_CS0}}$ | A23 | A19 | A16 | A15 | B |
| C | D12 | D13 | SD_CKE | $\overline{\text{RCON}}$ | DT2IN | $\overline{\text{IRQ4}}$ | QSPI_CLK | $\overline{\text{FB_CS1}}$ | A21 | A10 | A17 | A14 | C |
| D | D10 | D11 | $\overline{\text{SD_WE}}$ | IVDD | $\overline{\text{U0RTS}}$ | U1RXD | $\overline{\text{FB_CS3}}$ | IVDD | A8 | VSS | A13 | A11 | D |
| E | D8 | D9 | $\overline{\text{BE/BWE1}}$ | $\overline{\text{U0CTS}}$ | EVDD | EVDD | SD_VDD | SD_VDD | A4 | A12 | A9 | A7 | E |
| F | D31 | D30 | SD_DQS3 | $\overline{\text{BE/BWE3}}$ | EVDD | VSS | VSS | SD_VDD | A0 | A6 | A5 | A3 | F |
| G | D29 | D28 | D26 | D27 | SD_VDD | VSS | VSS | EVDD | EVDD | A2 | $\overline{\text{TA}}$ | A1 | G |
| H | D25 | D24 | SD_SDR_DQS | IVDD | SD_VDD | SD_VDD | EVDD | EVDD | TDI/DSI | DRAM SEL | IVDD | PLL_VDD | H |
| J | SD_CLK | $\overline{\text{SD_RAS}}$ | SD_VDD | D18 | $\overline{\text{BE/BWE0}}$ | D4 | D2 | $\overline{\text{OE}}$ | IVDD | $\overline{\text{RESET}}$ | JTAG_EN | XTAL | J |
| K | $\overline{\text{SD_CLK}}$ | D20 | D23 | D16 | D6 | $\overline{\text{R/W}}$ | D0 | PST0 | DDATA3 | PST1 | $\overline{\text{TRST/DSCLK}}$ | EXTAL | K |
| L | FB_CLK | D22 | D21 | $\overline{\text{BE/BWE2}}$ | D7 | D5 | D1 | PST2 | DDATA2 | U0TXD | PST3 | TMS/BKPT | L |
| M | SD_A10 | $\overline{\text{SD_CAS}}$ | D19 | D17 | SD_DQS2 | D3 | TCLK/PSTCLK | DDATA0 | TDO/DSO | U0RXD | DDATA1 | $\overline{\text{RSTOUT}}$ | M |

Figure 4. MCF5207CVM166 Pinout Top View (144 MAPBGA)

4.4 Package Dimensions—144 MAPBGA

Figure 5 shows the MCF5207CAB166 package dimensions.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 5. MCF5207CAB166 Package Dimensions (144 MAPBGA)

4.5 Pinout—160 QFP

Figure 6 shows a pinout of the MCF5208CAB166 device.

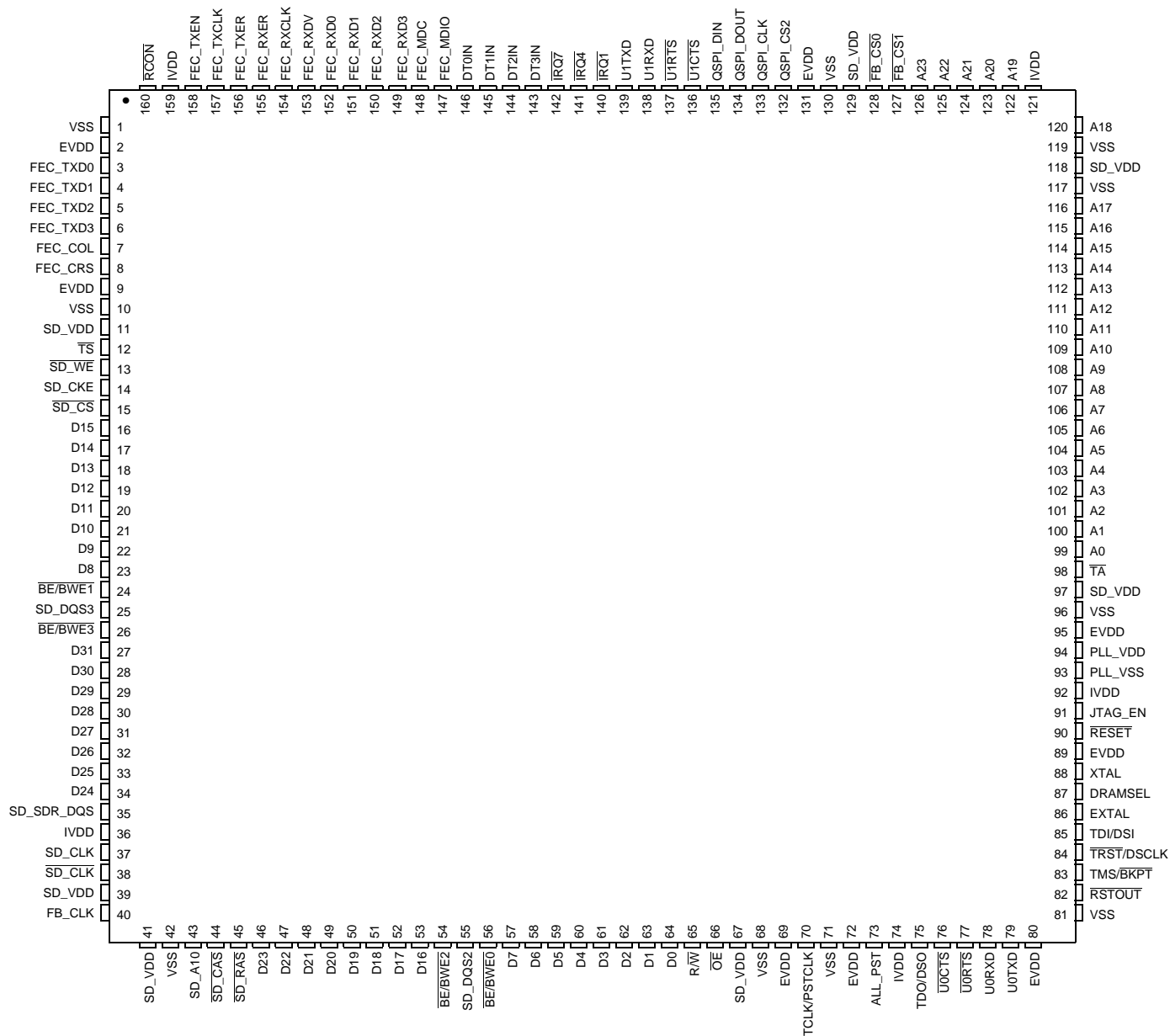


Figure 6. MCF5208CAB166 Pinout Top View (160 QFP)

4.6 Package Dimensions—160 QFP

The package dimensions of the MCF5208CAB166 device are shown in the figures below.

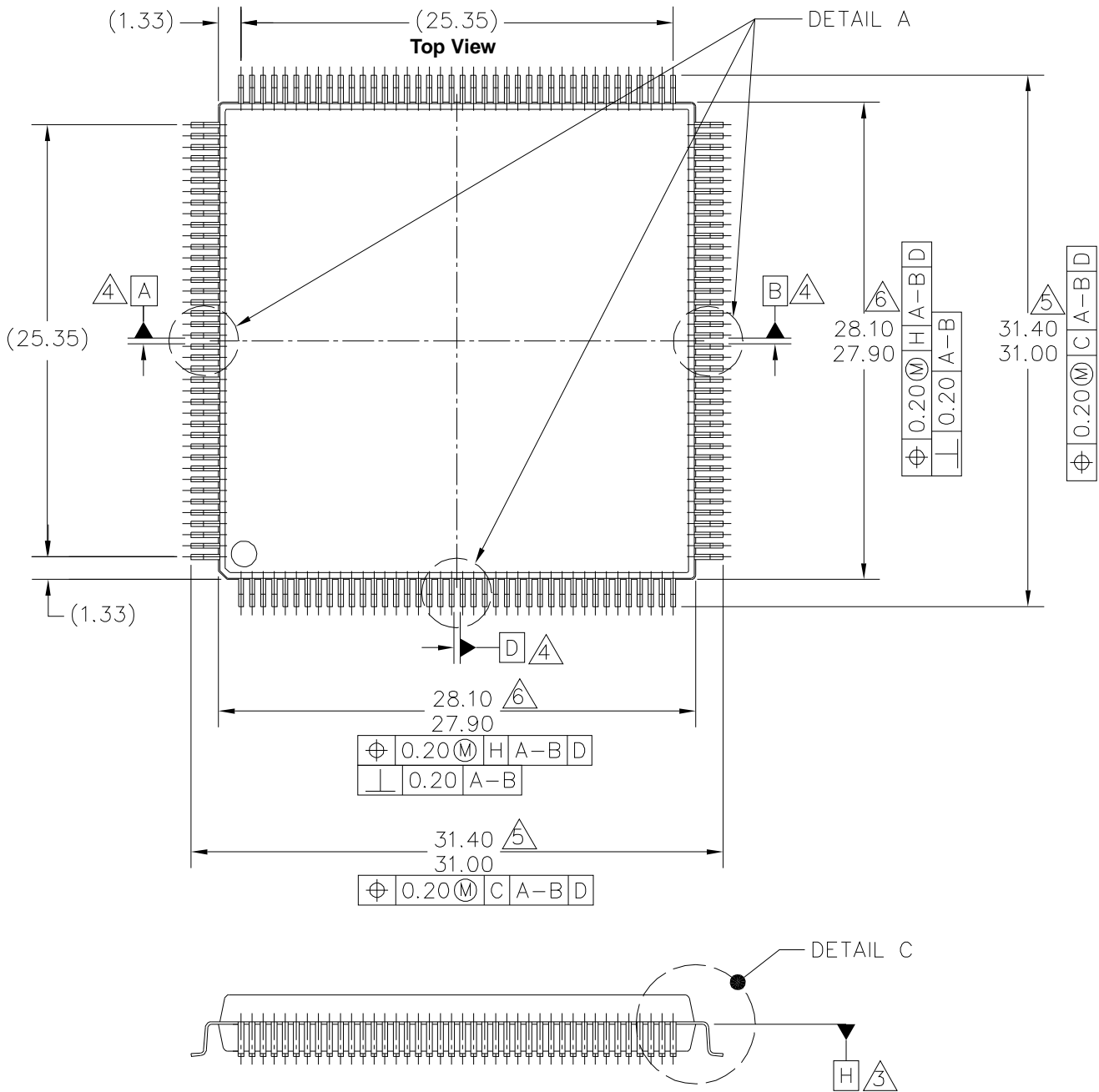
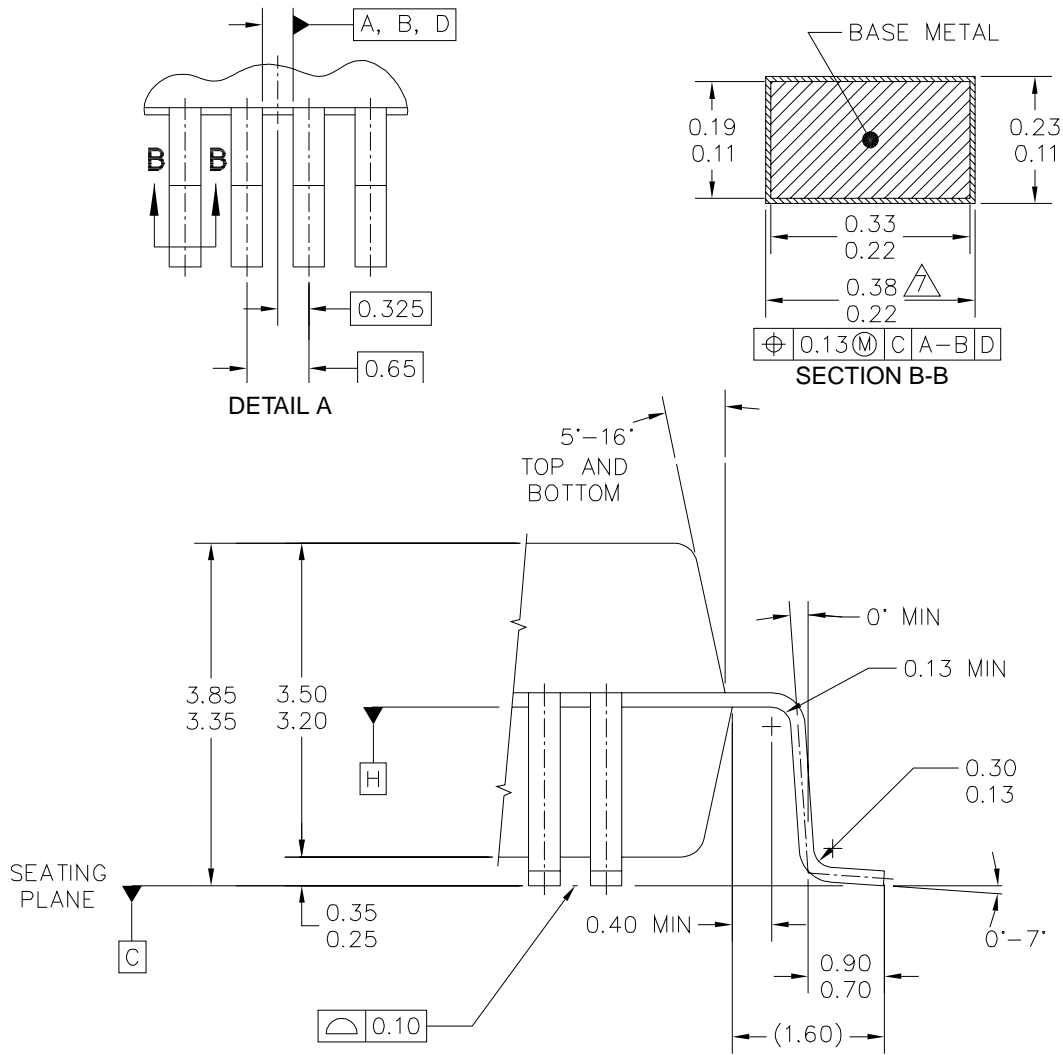


Figure 7. MCF5208CAB166 Package Dimensions (Sheet 1 of 2)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Figure 8. MCF5208CAB166 Package Dimensions (Sheet 2 of 2)

4.7 Pinout—196 MAPBGA

Figure 9 shows a pinout of the MCF5208CVM166 device.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |
|---|----------|----------|------------|-----------|----------|----------|--------|--------|-------------|----------|----------|------------|----------|----------|---|
| A | VSS | FEC_TXEN | FEC_TXER | FEC_RXDV | FEC_RXD3 | DT1IN | DT2IN | U1TXD | QSPL_CLK | FB_CS2 | A22 | A20 | A19 | VSS | A |
| B | FEC_TXD0 | FEC_TXD1 | FEC_TXCLK | FEC_RXCLK | FEC_RXD2 | DT0IN | DT3IN | U1RXD | QSPL_DOUT | FB_CS1 | A23 | A21 | A18 | A17 | B |
| C | FEC_TXD3 | FEC_TXD2 | RCON | FEC_RXER | FEC_RXD1 | FEC_MDIO | IRQ7 | U1RTS | QSPL_DIN | FB_CS0 | FB_CS3 | TEST | A16 | A15 | C |
| D | I2C_SDA | FEC_CRS | FEC_COL | IVDD | FEC_RXD0 | FEC_MDC | IRQ4 | IRQ1 | U1CTS | QSPL_CS2 | IVDD | A14 | A13 | A12 | D |
| E | SD_CKE | SD_WE | TS | I2C_SCL | EVDD | EVDD | EVDD | SD_VDD | SD_VDD | SD_VDD | A11 | A10 | A9 | A8 | E |
| F | D13 | D14 | D15 | SD_CS | EVDD | EVDD | VSS | VSS | SD_VDD | SD_VDD | A7 | A6 | A5 | A4 | F |
| G | D9 | D10 | D11 | D12 | EVDD | VSS | VSS | VSS | VSS | SD_VDD | A3 | A2 | A1 | A0 | G |
| H | D8 | BE/BWE3 | SD_DQS3 | BE/BWE1 | SD_VDD | VSS | VSS | VSS | VSS | EVDD | IVDD | PLL_VSS | PLL_VDD | TA | H |
| J | D28 | D29 | D30 | D31 | SD_VDD | SD_VDD | VSS | VSS | EVDD | EVDD | NC | IVDD | JTAG_EN | RESET | J |
| K | D24 | D25 | D26 | D27 | SD_VDD | SD_VDD | SD_VDD | EVDD | EVDD | EVDD | DRAM_SEL | TDI/DSI | EVDD | XTAL | K |
| L | SD_CLK | SD_VDD | SD_SDR_DQS | IVDD | D18 | SD_DQS2 | D5 | R/W | PST0 | PST1 | IVDD | TRST/DSCLK | VSS | EXTAL | L |
| M | SD_CLK | VSS | D23 | D21 | D17 | BE/BWE0 | D4 | OE | EVDD | PST2 | DDATA1 | TDO/DSO | PLL_TEST | TMS/BKPT | M |
| N | FB_CLK | SD_A10 | D22 | D20 | D16 | D7 | D3 | D1 | VSS | PST3 | DDATA2 | U0CTS | U0RXD | RSTOUT | N |
| P | VSS | SD_CAS | SD_RAS | D19 | BE/BWE2 | D6 | D2 | D0 | TCLK/PSTCLK | DDATA0 | DDATA3 | U0RTS | U0TXD | VSS | P |

Figure 9. MCF5208CVM166 Pinout Top View (196 MAPBGA)

4.8 Package Dimensions—196 MAPBGA

The package dimensions for the MCF5208CVM166 device is shown below.

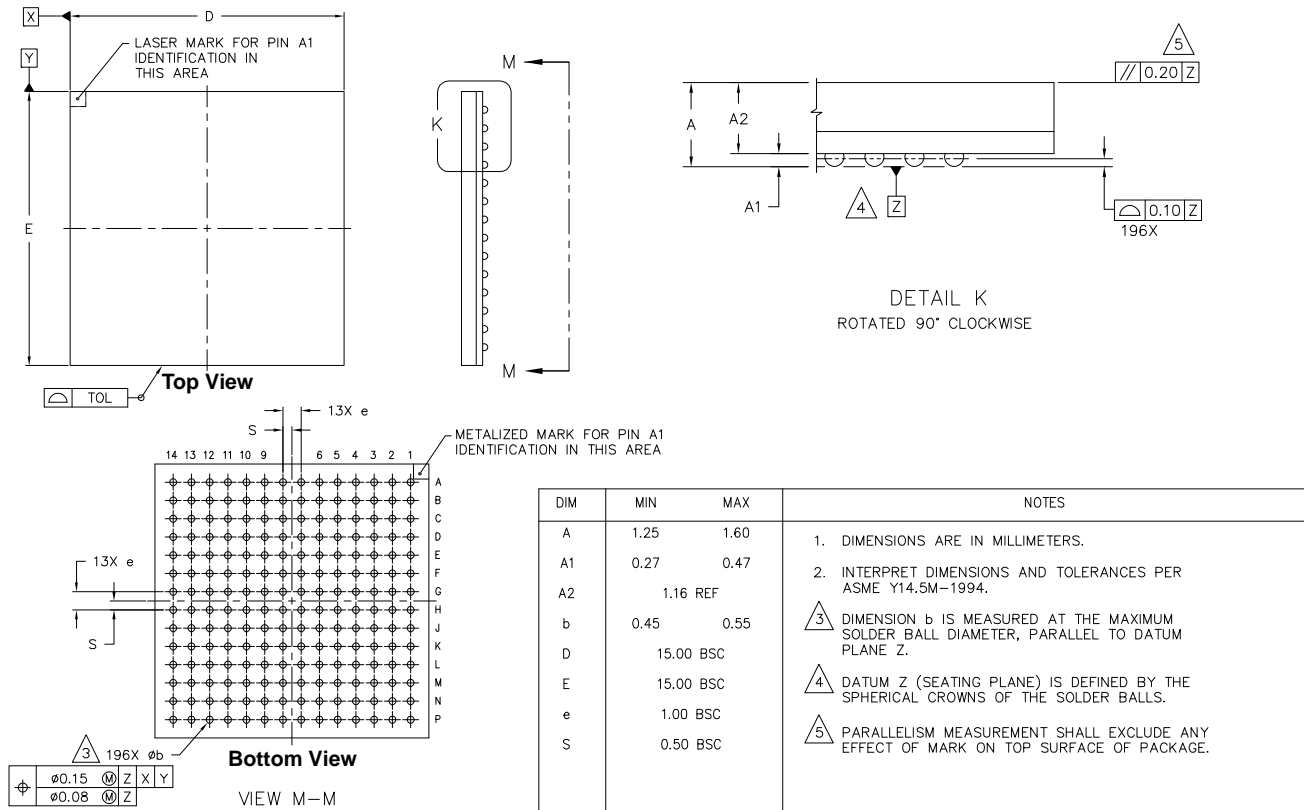


Figure 10. MCF5208CVM166 Package Dimensions (196 MAPBGA)

5 Electrical Characteristics

5.1 Maximum Ratings

Table 4. Absolute Maximum Ratings^{1, 2}

| Rating | Symbol | Value | Unit |
|--|--------------|--------------|------|
| Core Supply Voltage | V_{DD} | -0.5 to +2.0 | V |
| CMOS Pad Supply Voltage | $E_{V_{DD}}$ | -0.3 to +4.0 | V |
| DDR/Memory Pad Supply Voltage | SDV_{DD} | -0.3 to +4.0 | V |
| PLL Supply Voltage | $PLLV_{DD}$ | -0.3 to +2.0 | V |
| Digital Input Voltage ³ | V_{IN} | -0.3 to +3.6 | V |
| Instantaneous Maximum Current Single pin limit (applies to all pins) ^{3, 4, 5} | I_D | 25 | mA |

Table 4. Absolute Maximum Ratings^{1, 2} (continued)

| | | | |
|--|--------------------------|-------------|----|
| Operating Temperature Range (Packaged) | T_A ($T_L - T_H$) | - 40 to 85 | °C |
| Storage Temperature Range | T_{stg} | - 55 to 150 | °C |

NOTES:

- ¹ Functional operating conditions are given in [Section 5.4, “DC Electrical Specifications”](#). Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.
- ² This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).
- ³ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
- ⁴ All functional non-supply pins are internally clamped to V_{SS} and EV_{DD} .
- ⁵ Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD} , the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 5 lists thermal resistance values

Table 5. Thermal Characteristics

| Characteristic | | Symbol | 196MBGA | 144MBGA | 160QFP | 144LQFP | Unit |
|---|-------------------------|----------------|-------------------|-------------------|-------------------|-------------------|------|
| Junction to ambient, natural convection | Four layer board (2s2p) | θ_{JMA} | 47 ^{1,2} | 47 ^{1,2} | 49 ^{1,2} | 65 ^{1,2} | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | θ_{JMA} | 43 ^{1,2} | 43 ^{1,2} | 44 ^{1,2} | 58 ^{1,2} | °C/W |
| Junction to board | | θ_{JB} | 36 ³ | 36 ³ | 40 ³ | 50 ³ | °C/W |
| Junction to case | | θ_{JC} | 22 ⁴ | 22 ⁴ | 39 ⁴ | 19 ⁴ | °C/W |
| Junction to top of package | | Ψ_{jt} | 6 ^{1,5} | 6 ^{1,5} | 12 ^{1,6} | 5 ^{1,7} | °C/W |
| Maximum operating junction temperature | | T_j | 105 | 105 | 105 | 105 | °C |

NOTES:

- ¹ θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer’s system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
- ² Per JEDEC JESD51-6 with the board horizontal.

- ³ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- ⁴ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- ⁵ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.
- ⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.
- ⁷ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \text{Eqn. 1}$$

Where:

- T_A = Ambient Temperature, °C
- Θ_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
- P_D = $P_{INT} + P_{I/O}$
- P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
- $P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273^\circ C)} \quad \text{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273^\circ C) + \Theta_{JMA} \times P_D^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from [Equation 3](#) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving [Equation 1](#) and [Equation 2](#) iteratively for any value of T_A .

5.3 ESD Protection

Table 6. ESD Protection Characteristics^{1, 2}

| Characteristics | Symbol | Value | Unit |
|---------------------------------|--------|-------|------|
| ESD Target for Human Body Model | HBM | 2000 | V |

NOTES:

- ¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

Electrical Characteristics

- ² A device is defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 7. DC Electrical Specifications

| Characteristic | Symbol | Min | Max | Unit |
|---|----------------|--|--|---------|
| Core Supply Voltage | IV_{DD} | 1.4 | 1.6 | V |
| PLL Supply Voltage | $PLL_{V_{DD}}$ | 1.4 | 1.6 | V |
| CMOS Pad Supply Voltage | EV_{DD} | 3.0 | 3.6 | V |
| SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) | SDV_{DD} | 1.70 2.25 3.0 | 1.95 2.75 3.6 | V |
| CMOS Input High Voltage | EV_{IH} | 2 | $EV_{DD} + 0.3$ | V |
| CMOS Input Low Voltage | EV_{IL} | $V_{SS} - 0.3$ | 0.8 | V |
| CMOS Output High Voltage $I_{OH} = -5.0$ mA | EV_{OH} | $EV_{DD} - 0.4$ | — | V |
| CMOS Output Low Voltage $I_{OL} = 5.0$ mA | EV_{OL} | — | 0.4 | V |
| SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) | SDV_{IH} | 1.35 1.7 2 | $SDV_{DD} + 0.3$ $SDV_{DD} + 0.3$ $SDV_{DD} + 0.3$ | V |
| SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) | SDV_{IL} | $V_{SS} - 0.3$ $V_{SS} - 0.3$ $V_{SS} - 0.3$ | 0.45 0.8 0.8 | V |
| SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) $I_{OH} = -5.0$ mA for all modes | SDV_{OH} | $SDV_{DD} - 0.35$ 2.1 2.4 | — — — | V |
| SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) $I_{OL} = 5.0$ mA for all modes | SDV_{OL} | — — — | 0.3 0.3 0.5 | V |
| Input Leakage Current $V_{in} = IV_{DD}$ or V_{SS} , Input-only pins | I_{in} | -1.0 | 1.0 | μ A |

Table 7. DC Electrical Specifications (continued)

| Characteristic | Symbol | Min | Max | Unit |
|--|-----------|-----|-------|---------|
| Weak Internal Pull Up Device Current, tested at V_{IL} Max. ¹ | I_{APU} | -10 | - 130 | μA |
| Input Capacitance ² | C_{in} | — | 7 | pF |
| All input-only pins | | — | 7 | |
| All input/output (three-state) pins | | — | 7 | |

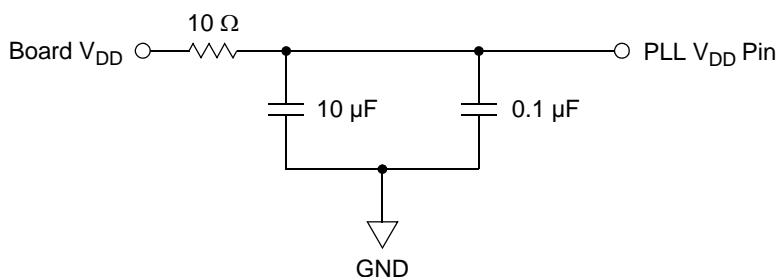
NOTES:

¹ Refer to the signals section for pins having weak internal pull-up devices.

² This parameter is characterized before qualification rather than 100% tested.

5.4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 11 should be connected between the board V_{DD} and the $PLL V_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLL V_{DD}$ pin as possible.


 Figure 11. System PLL V_{DD} Power Filter

5.4.2 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD} .

5.4.2.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD} , SDV_{DD} , or $PLL V_{DD}$ by more than 0.4 V during power ramp-up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 μs to avoid turning on the internal ESD protection clamp diodes.

5.4.2.2 Power Down Sequence

If $IV_{DD}/PLL V_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLL V_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD} , SDV_{DD} , or $PLL V_{DD}$ going low by more than

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0.4 V during power down or there is an undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is:

1. Drop $IV_{DD}/PLL V_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

5.5 Current Consumption

All of the below current consumption data is lab data measured on a single device using an evaluation board. [Table 8](#) shows the typical current consumption in low-power modes at various $f_{sys/2}$ frequencies. Current measurements are taken after executing a STOP instruction.

Table 8. Current Consumption in Low-Power Mode^{1,2}

| Mode | Voltage (V) | Typical ³ (mA) | | | | | Peak ⁴ (mA) |
|------------------------------------|-------------|---------------------------|--------|--------|--------|-----------|------------------------|
| | | 44 MHz | 56 MHz | 64 MHz | 72 MHz | 83.33 MHz | 83.33 MHz |
| Stop Mode 3 (Stop 11) ⁵ | 3.3 | 1.33 | | | | | |
| | 2.5 | 15.19 | | | | | |
| | 1.5 | 0.519 | | | | | |
| Stop Mode 2 (Stop 10) ⁵ | 3.3 | 1.93 | | | | | |
| | 2.5 | 15.19 | | | | | |
| | 1.5 | 1.25 | | | | | |
| Stop Mode 1 (Stop 01) ⁵ | 3.3 | 1.83 | | | | | |
| | 2.5 | 15.23 | | | | | |
| | 1.5 | 8.24 | 10.22 | 9.55 | 10.61 | 12.1 | 12.1 |
| Stop Mode 0 (Stop 00) ⁵ | 3.3 | 2.23 | 2.33 | 2.41 | 2.5 | 2.61 | 2.61 |
| | 2.5 | 16.2 | 16.47 | 16.62 | 16.91 | 17.24 | 17.24 |
| | 1.5 | 8.32 | 10.32 | 9.66 | 10.73 | 12.25 | 12.25 |
| Wait/Doze | 3.3 | 2.23 | 2.33 | 2.41 | 2.5 | 2.6 | 4.07 |
| | 2.5 | 16.2 | 16.48 | 16.62 | 16.91 | 17.24 | 18.77 |
| | 1.5 | 11.53 | 14.36 | 14.29 | 15.92 | 18.21 | 35.45 |
| Run | 3.3 | 6.79 | 9.02 | 14.56 | 19.54 | 29.12 | 30.43 |
| | 2.5 | 16.17 | 16.48 | 16.64 | 16.89 | 17.23 | 18.76 |
| | 1.5 | 16.29 | 20.36 | 21.13 | 23.57 | 27.0 | 44.1 |

NOTES:

- ¹ All values are measured with a 3.30V EV_{DD} , 2.50V SDV_{DD} , and 1.5V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.
- ² Refer to the Power Management chapter in the *MCF5208 Reference Manual* for more information on low-power modes.
- ³ All peripheral clocks except UART0, FlexBus, INTC, reset controller, PLL, and Edge Port off before entering low-power mode. All code executed from flash.
- ⁴ Peak current measured while running a while(1) loop with all modules active.

⁵ See the description of the low-power control register (LCPR) in the *MCF5208 Reference Manual* for more information on stop modes 0–3.

The figure below illustrates the power consumption in a graphical format.

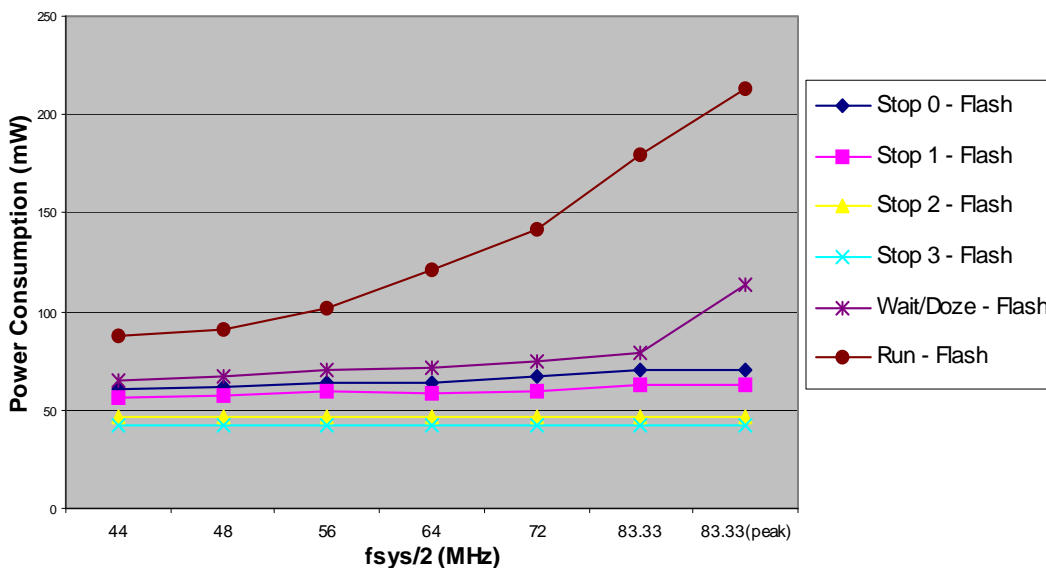


Figure 12. Current Consumption in Low-Power Modes

Table 9. Typical Active Current Consumption Specifications¹

| f _{sys/2} Frequency | Voltage (V) | Typical ² Active (mA) | | Peak ³ Active (mA) |
|------------------------------|-------------|----------------------------------|-------|-------------------------------|
| | | SRAM | Flash | |
| 1 MHz | 3.3 | 2.04 | 2.12 | 2.28 |
| | 2.5 | 15.24 | 15.32 | 15.24 |
| | 1.5 | 1.30 | 1.41 | 1.49 |
| 2 MHz | 3.3 | 2.23 | 2.40 | 3.57 |
| | 2.5 | 15.26 | 15.42 | 15.26 |
| | 1.5 | 1.71 | 1.92 | 2.09 |
| 4 MHz | 3.3 | 2.60 | 2.95 | 3.58 |
| | 2.5 | 15.30 | 15.61 | 15.30 |
| | 1.5 | 2.49 | 2.95 | 3.29 |
| 44 MHz | 3.3 | 7.61 | 17.67 | 25.34 |
| | 2.5 | 16.13 | 19.49 | 16.95 |
| | 1.5 | 24.04 | 28.72 | 39.02 |
| 48 MHz | 3.3 | 8.16 | 26.21 | 34.45 |
| | 2.5 | 16.28 | 20.06 | 17.17 |
| | 1.5 | 26.05 | 31.13 | 42.30 |

Table 9. Typical Active Current Consumption Specifications¹ (continued)

| f _{sys/2} Frequency | Voltage (V) | Typical ² Active (mA) | | Peak ³ Active (mA) |
|------------------------------|-------------|----------------------------------|-------|-------------------------------|
| | | SRAM | Flash | |
| 56 MHz | 3.3 | 10.09 | 30.71 | 38.97 |
| | 2.5 | 16.43 | 20.71 | 17.65 |
| | 1.5 | 30.07 | 35.90 | 47.90 |
| 64 MHz | 3.3 | 15.72 | 31.37 | 42.10 |
| | 2.5 | 16.56 | 21.08 | 17.95 |
| | 1.5 | 32.19 | 38.72 | 53.50 |
| 72 MHz | 3.3 | 20.97 | 31.40 | 48.80 |
| | 2.5 | 16.87 | 21.70 | 18.20 |
| | 1.5 | 35.90 | 43.20 | 59.50 |
| 83.33 MHz | 3.3 | 31.37 | 25.83 | 48.60 |
| | 2.5 | 17.21 | 22.80 | 18.83 |
| | 1.5 | 41.10 | 49.40 | 67.50 |

NOTES:

- ¹ All values are measured with a 3.30V EV_{DD}, 2.50V SDV_{DD}, and 1.5V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.
- ² CPU polling a status register. All peripheral clocks except UART0, FlexBus, INTC, reset controller, PLL, and edge port disabled.
- ³ Peak current measured while running a while(1) loop with all modules active.

5.6 Oscillator and PLL Electrical Characteristics

Table 10. PLL Electrical Characteristics

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|-----|---|--------------------------|---------------------------|---------------------------|-------|
| 1 | PLL Reference Frequency Range Crystal reference External reference | f _{ref_crystal} | 12 | 25 ¹ | MHz |
| | | f _{ref_ext} | 12 | 40 ¹ | MHz |
| 2 | Core frequency CLKOUT Frequency ² | f _{sys} | 488 x 10 ⁻⁶ | 166.66 | MHz |
| | | f _{sys/2} | 244 x 10 ⁻⁶ | 83.33 | MHz |
| 3 | Crystal Start-up Time ^{3, 4} | t _{cst} | — | 10 | ms |
| 4 | EXTAL Input High Voltage Crystal Mode ⁵ All other modes (External, Limp) | V _{IHEXT} | V _{XTAL} + 0.4 | — | V |
| | | V _{IHEXT} | E _{VDD} /2 + 0.4 | — | V |
| 5 | EXTAL Input Low Voltage Crystal Mode ⁵ All other modes (External, Limp) | V _{ILEXT} | — | V _{XTAL} - 0.4 | V |
| | | V _{ILEXT} | — | E _{VDD} /2 - 0.4 | V |
| 7 | PLL Lock Time ^{3, 6} | t _{pll} | — | 50000 | CLKIN |
| 8 | Duty Cycle of reference ³ | t _{dc} | 40 | 60 | % |

Table 10. PLL Electrical Characteristics (continued)

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|-----|--|----------------|------------|--|--------------------------------|
| 9 | XTAL Current | I_{XTAL} | 1 | 3 | mA |
| 10 | Total on-chip stray capacitance on XTAL | C_{S_XTAL} | | 1.5 | pF |
| 11 | Total on-chip stray capacitance on EXTAL | C_{S_EXTAL} | | 1.5 | pF |
| 12 | Crystal capacitive load | C_L | | See crystal spec | |
| 13 | Discrete load capacitance for XTAL | C_{L_XTAL} | | $2 \cdot C_L - C_{S_XTAL} - C_{PCB_XTAL}$ ⁷ | pF |
| 14 | Discrete load capacitance for EXTAL | C_{L_EXTAL} | | $2 \cdot C_L - C_{S_EXTAL} - C_{PCB_EXTAL}$ ⁷ | pF |
| 17 | CLKOUT Period Jitter, ^{3, 4, 7, 8, 9} Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter | C_{jitter} | — — | 10 TBD | % $f_{sys/2}$ % $f_{sys/2}$ |
| 18 | Frequency Modulation Range Limit ^{3, 10, 11} (f_{sys} Max must not be exceeded) | C_{mod} | 0.8 | 2.2 | % $f_{sys/2}$ |
| 19 | VCO Frequency. $f_{VCO} = (f_{ref} \cdot PFD)/4$ | f_{VCO} | 350 | 540 | MHz |

NOTES:

- ¹ The maximum allowable input clock frequency when booting with the PLL enabled is 24 MHz. For higher input clock frequencies, the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.
- ² All internal registers retain data at 0 Hz.
- ³ This parameter is guaranteed by characterization before qualification rather than 100% tested.
- ⁴ Proper PC board layout procedures must be followed to achieve specifications.
- ⁵ This parameter is guaranteed by design rather than 100% tested.
- ⁶ This specification is the PLL lock time only and does not include oscillator start-up time.
- ⁷ C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.
- ⁸ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD} , EV_{DD} , and V_{SS} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.
- ⁹ Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of $C_{jitter} + C_{mod}$.
- ¹⁰ Modulation percentage applies over an interval of 10 μ s, or equivalently the modulation rate is 100KHz.
- ¹¹ Modulation range determined by hardware design.

5.7 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 11 are shown in Figure 14 and Figure 15.

* The timings are also valid for inputs sampled on the negative clock edge.

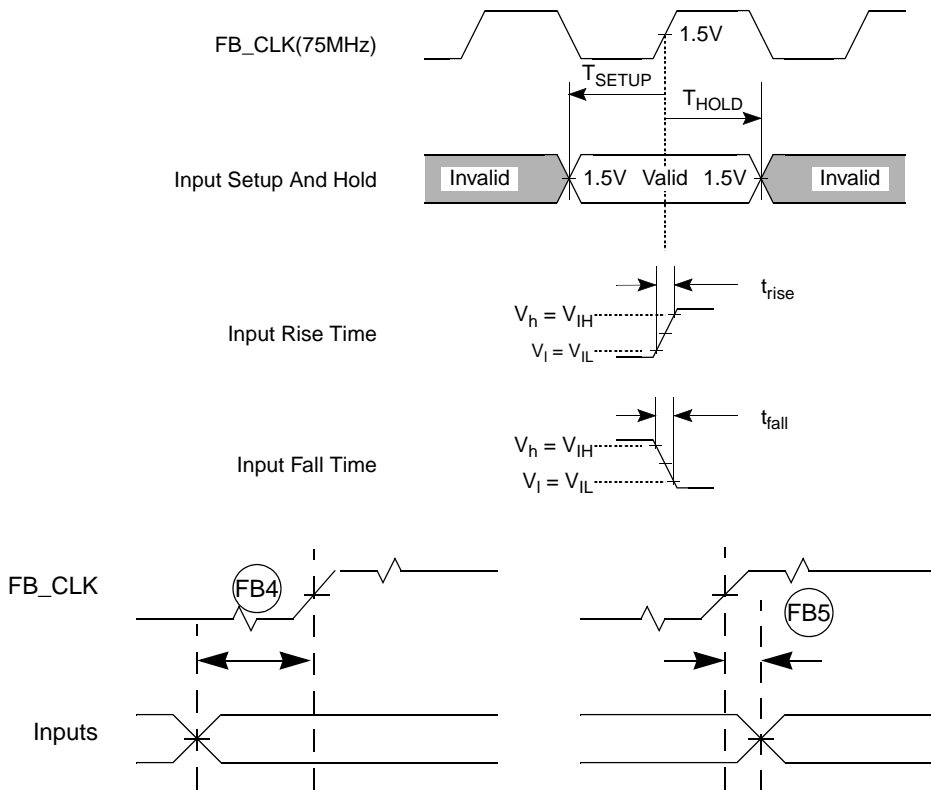


Figure 13. General Input Timing Requirements

5.7.1 FlexBus

FlexBus is a multi-function external bus interface provided to interface to slave-only devices up to a maximum bus frequency of 83.33 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB_CS}}[5:0]$) that can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select $\overline{\text{FB_CS}}[0]$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

5.7.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the system clock.

Table 11. FlexBus AC Timing Specifications

| Num | Characteristic | Symbol | Min | Max | Unit | Notes |
|-----|---|---------------|-----|-------|------|-----------------|
| | Frequency of Operation | | | 83.33 | Mhz | $f_{sys/2}$ |
| FB1 | Clock Period (FB_CLK) | t_{FBCK} | 12 | | ns | t_{cyc} |
| FB2 | Data, and Control Output Valid (A[23:0], D[31:0], FB_CS[5:0], R/W, TS, BE/BWE[3:0] and OE) | $t_{FBCHDCV}$ | — | 7.0 | ns | ¹ |
| FB3 | Data, and Control Output Hold ((A[23:0], D[31:0], FB_CS[5:0], R/W, TS, BE/BWE[3:0], and OE) | $t_{FBCHDCI}$ | 1 | — | ns | ^{1, 2} |
| FB4 | Data Input Setup | t_{DVFBCH} | 3.5 | — | ns | |
| FB5 | Data Input Hold | t_{DIFBCH} | 0 | — | ns | |
| FB6 | Transfer Acknowledge (\overline{TA}) Input Setup | t_{CVFBCH} | 4 | — | ns | |
| FB7 | Transfer Acknowledge (\overline{TA}) Input Hold | t_{CIFBCH} | 0 | — | ns | |

NOTES:

- ¹ Timing for chip selects only applies to the $\overline{FB_CS}[5:0]$ signals. Please see [Section 5.8, "SDRAM Bus"](#) for $\overline{SD_CS}[1:0]$ timing.
- ² The FlexBus supports programming an extension of the address hold. Please consult the device reference manual for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

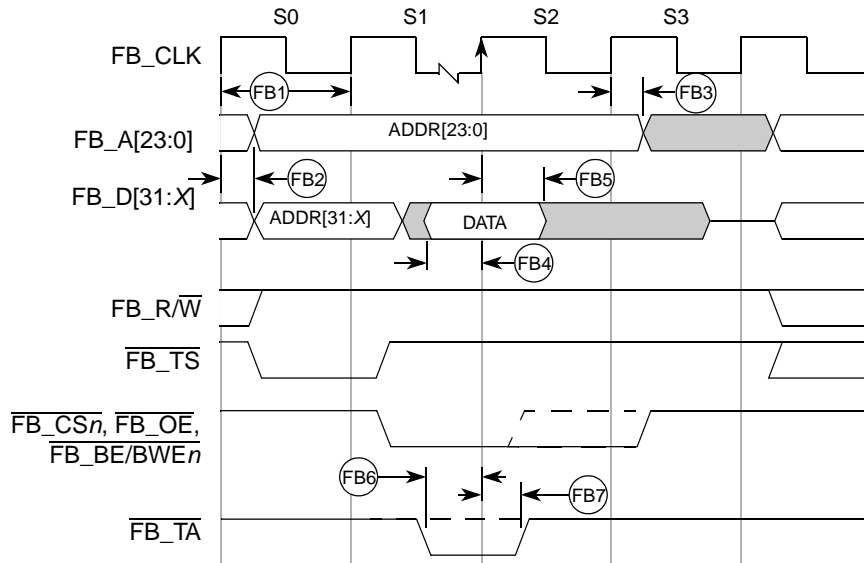


Figure 14. FlexBus Read Timing

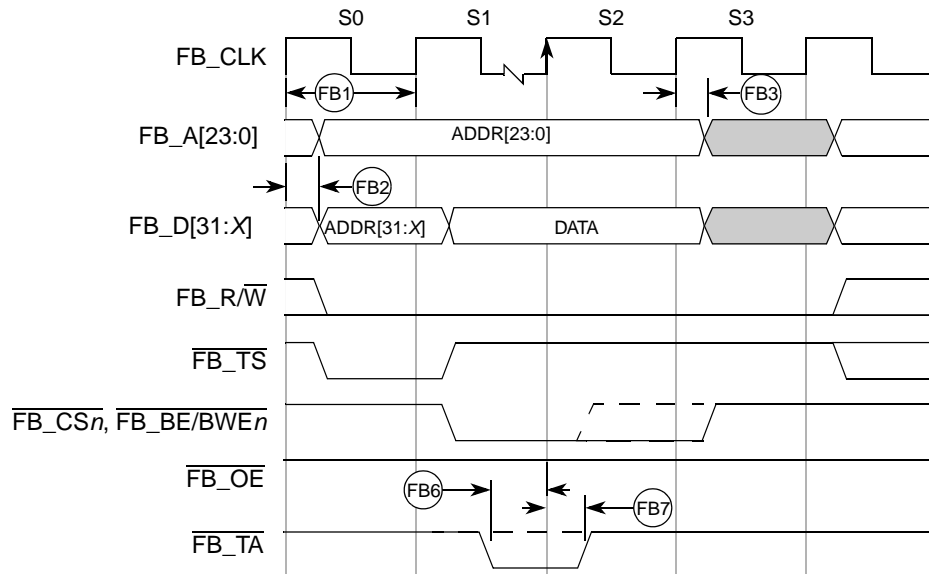


Figure 15. Flexbus Write Timing

5.8 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time. The SDRAM controller uses SSTL2 and SSTL3 I/O drivers. Both SSTL drive modes are programmable for Class I or Class II drive strength.

5.8.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The SDRAM controller is a DDR controller with an SDR mode. Because it is designed to support DDR, a DQS pulse must remain supplied to the device for each data beat of an SDR read. The ColdFire processor accomplishes this by asserting a signal called SD_SDR_DQS during read cycles. Take care during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 12. SDR Timing Specifications

| Symbol | Characteristic | Symbol | Min | Max | Unit | Notes |
|--------|---|---------------|---|-----------------------------|--------|-------|
| | Frequency of Operation | | 60 | 83.33 | MHz | 1 |
| SD1 | Clock Period (t_{CK}) | t_{SDCK} | 12 | 16.67 | ns | 2 |
| SD3 | Pulse Width High (t_{CKH}) | t_{SDCKH} | 0.45 | 0.55 | SD_CLK | 3 |
| SD4 | Pulse Width Low (t_{CKL}) | t_{SDCKL} | 0.45 | 0.55 | SD_CLK | 3 |
| SD5 | Address, $\overline{SD_CKE}$, $\overline{SD_CAS}$, $\overline{SD_RAS}$, $\overline{SD_WE}$, $\overline{SD_BA}$, $\overline{SD_CS}[1:0]$ - Output Valid (t_{CMV}) | $t_{SDCHACV}$ | — | $0.5 \times SD_CLK + 1.0$ | ns | |
| SD6 | Address, $\overline{SD_CKE}$, $\overline{SD_CAS}$, $\overline{SD_RAS}$, $\overline{SD_WE}$, $\overline{SD_BA}$, $\overline{SD_CS}[1:0]$ - Output Hold (t_{CMH}) | $t_{SDCHACI}$ | 2.0 | — | ns | |
| SD7 | SD_SDR_DQS Output Valid (t_{DQSOV}) | t_{DQSOV} | — | Self timed | ns | 4 |
| SD8 | SD_DQS[3:2] input setup relative to SD_CLK ($t_{DQSI S}$) | $t_{DQVSDCH}$ | $0.25 \times SD_CLK$ | $0.40 \times SD_CLK$ | ns | 5 |
| SD9 | SD_DQS[3:2] input hold relative to SD_CLK (t_{DQSIH}) | $t_{DQISDCH}$ | Does not apply. 0.5 SD_CLK fixed width. | | | 6 |
| SD10 | Data (D[31:0]) Input Setup relative to SD_CLK (reference only) (t_{DIS}) | t_{DVSDCH} | $0.25 \times SD_CLK$ | — | ns | 7 |
| SD11 | Data Input Hold relative to SD_CLK (reference only) (t_{DIH}) | t_{DISDCH} | 1.0 | — | ns | |
| SD12 | Data (D[31:0]) and Data Mask (SD_DQM[3:0]) Output Valid (t_{DV}) | $t_{SDCHDMV}$ | — | $0.75 \times SD_CLK + 0.5$ | ns | |
| SD13 | Data (D[31:0]) and Data Mask (SD_DQM[3:0]) Output Hold (t_{DH}) | $t_{SDCHDMI}$ | 1.5 | — | ns | |

NOTES:

- 1 The device supports the same frequency of operation for FlexBus and SDRAM as that of the internal bus clock. Please see the PLL chapter of the *MCF5208 Reference Manual* for more information on setting the SDRAM clock rate.
- 2 SD_CLK is one SDRAM clock in (ns).
- 3 Pulse width high plus pulse width low cannot exceed min and max clock period.
- 4 SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_DQS only pulses during a read cycle and one pulse occurs for each data beat.
- 5 SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS only pulses during a read cycle and one pulse occurs for each data beat.
- 6 The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.
- 7 Because a read cycle in SDR mode continues using the DQS circuit within the device, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens results in successful SDR reads. The input setup spec is provided as guidance.

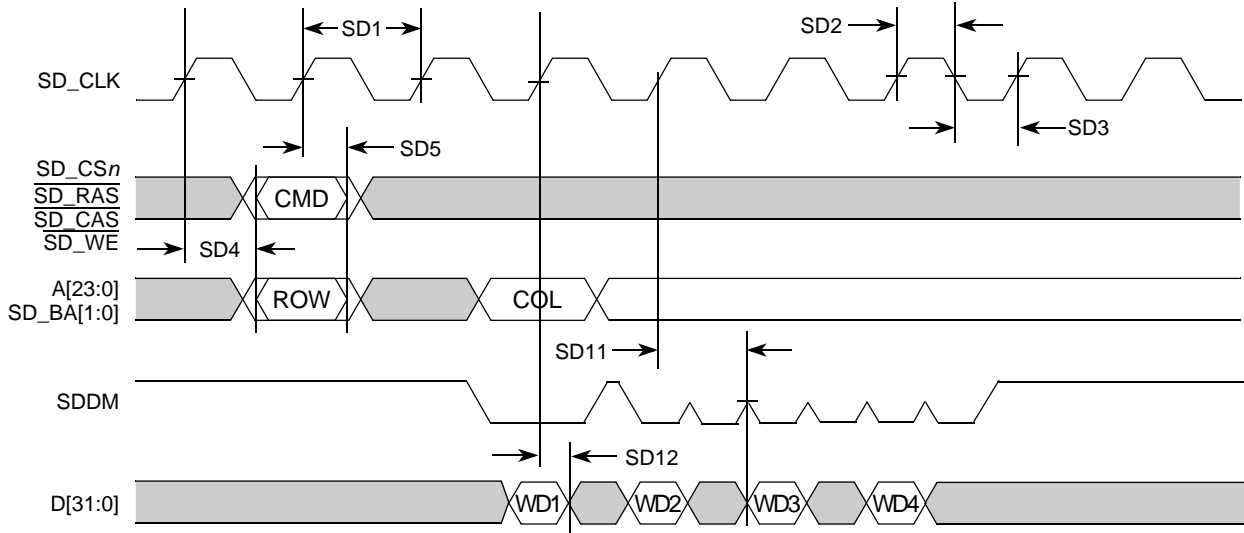
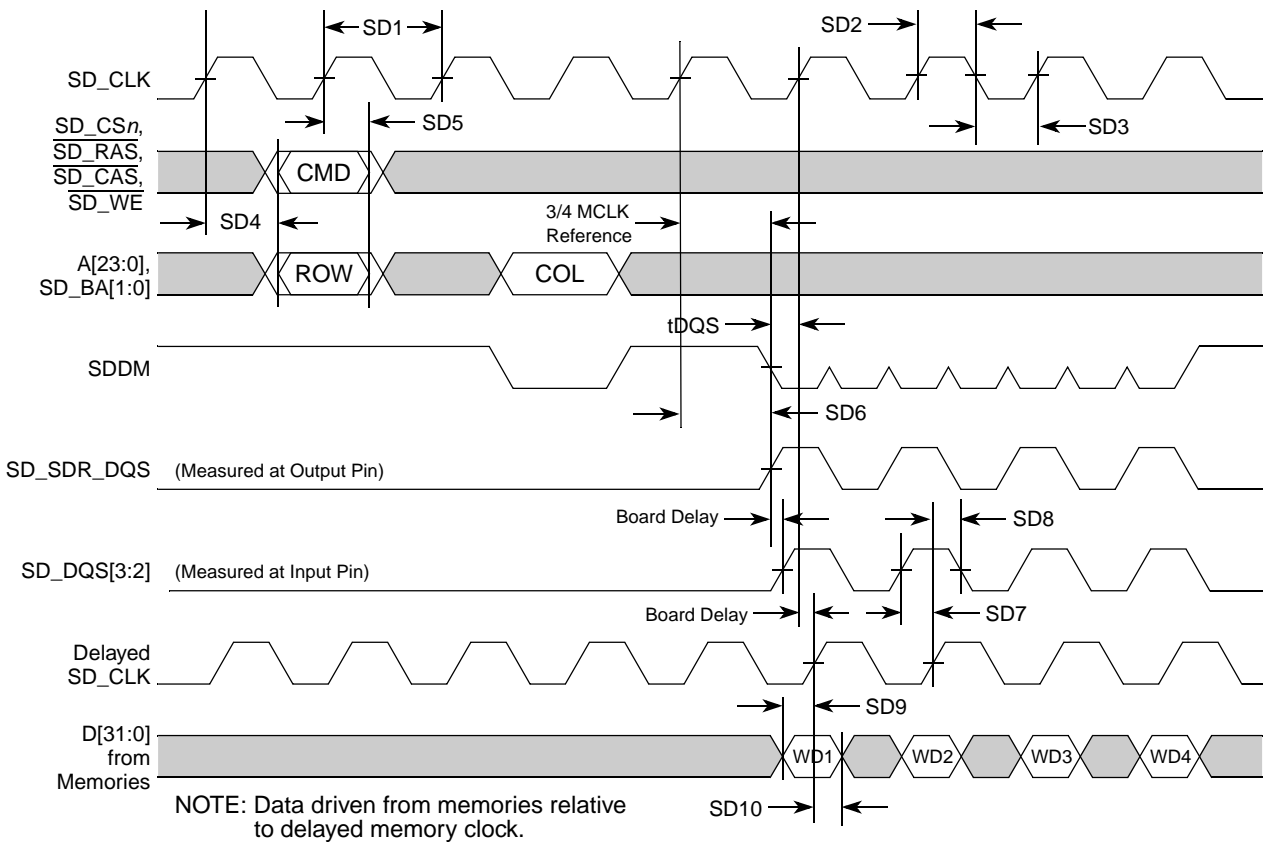


Figure 16. SDR Write Timing



NOTE: Data driven from memories relative to delayed memory clock.

Figure 17. SDR Read Timing

5.8.2 DDR SDRAM AC Timing Characteristics

When using the SDRAM controller in DDR mode, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes. The following timing numbers are subject to change at anytime, and are only provided to aid in early board design. Please contact your local Freescale representative if questions develop.

Table 13. DDR Timing Specifications

| Num | Characteristic | Symbol | Min | Max | Unit | Notes |
|------|---|---------------|-------------------------------|----------------------------|--------|--------|
| — | Frequency of Operation | — | 60 | 83.33 | Mhz | 1 |
| DD1 | Clock Period (SD_CLK) | t_{DDCK} | 12 | 16.67 | ns | 2 |
| DD2 | Pulse Width High | t_{DDCKH} | 0.45 | 0.55 | SD_CLK | 3 |
| DD3 | Pulse Width Low | t_{DDCKL} | 0.45 | 0.55 | SD_CLK | 3 |
| DD4 | Address, SD_CKE, SD_CAS, SD_RAS, SD_WE, SD_CS[1:0] - Output Valid | $t_{SDCHACV}$ | — | $0.5 \times SD_CLK + 1.0$ | ns | 4 |
| DD5 | Address, SD_CKE, SD_CAS, SD_RAS, SD_WE, SD_CS[1:0] - Output Hold | $t_{SDCHACI}$ | 2.0 | — | ns | — |
| DD6 | Write Command to first DQS Latching Transition | t_{CMDVDQ} | — | 1.25 | SD_CLK | — |
| DD7 | Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode) | t_{DQDMV} | 1.5 | — | ns | 5 6 |
| DD8 | Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode) | t_{DQDMI} | 1.0 | — | ns | 7 |
| DD9 | Input Data Skew Relative to DQS (Input Setup) | t_{DQDQ} | — | 1 | ns | 8 |
| DD10 | Input Data Hold Relative to DQS. | t_{DIDQ} | $0.25 \times SD_CLK + 0.5ns$ | — | ns | 9 |
| DD11 | DQS falling edge from SDCLK rising (output hold time) | $t_{DQLSDCH}$ | 0.5 | — | ns | — |
| DD12 | DQS input read preamble width (t_{RPRE}) | t_{DQRPRE} | 0.9 | 1.1 | SD_CLK | — |
| DD13 | DQS input read postamble width (t_{RPST}) | t_{DQRPST} | 0.4 | 0.6 | SD_CLK | — |
| DD14 | DQS output write preamble width (t_{WPRE}) | t_{DQWPRE} | 0.25 | — | SD_CLK | — |
| DD15 | DQS output write postamble width (t_{WPST}) | t_{DQWPST} | 0.4 | 0.6 | SD_CLK | — |

NOTES:

- ¹ The frequency of operation is 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.
- ² SD_CLK is one SDRAM clock in (ns).
- ³ Pulse width high plus pulse width low cannot exceed min and max clock period.
- ⁴ Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.
- ⁵ This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, the input setup on the memory is in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].
- ⁶ The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

Electrical Characteristics

- 7 This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative to MEM_DQS[0].
- 8 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).
- 9 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

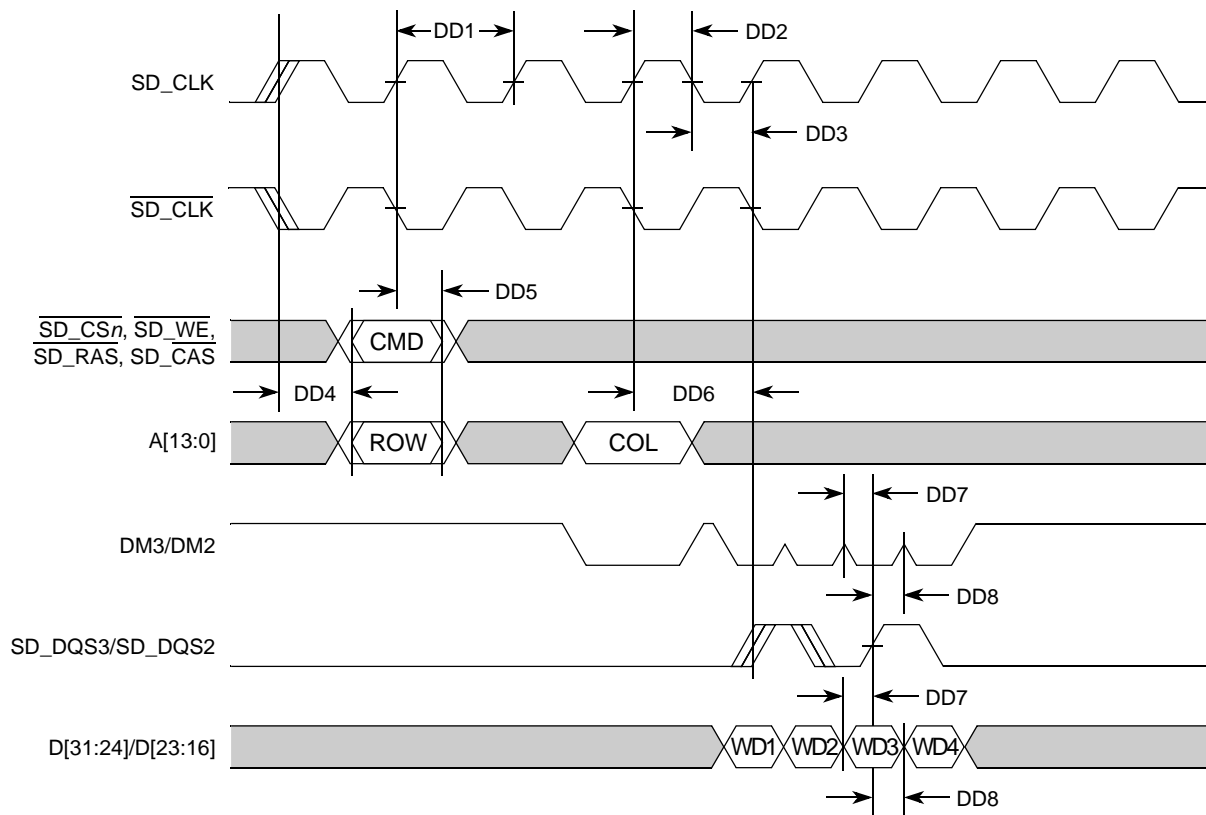


Figure 18. DDR Write Timing

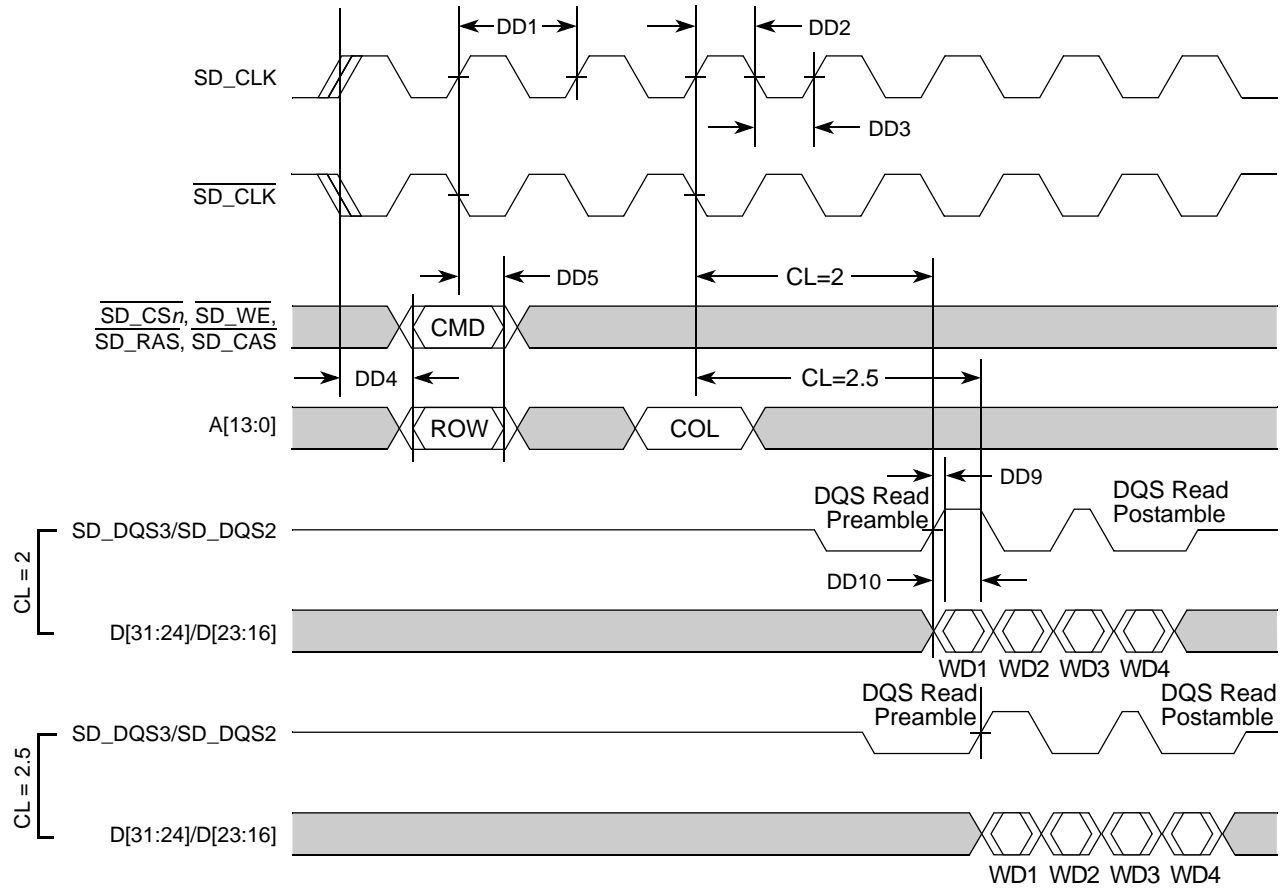


Figure 19. DDR Read Timing

5.9 General Purpose I/O Timing

 Table 14. GPIO Timing¹

| Num | Characteristic | Symbol | Min | Max | Unit |
|-----|------------------------------------|-------------|-----|-----|------|
| G1 | FB_CLK High to GPIO Output Valid | t_{CHPOV} | — | 8 | ns |
| G2 | FB_CLK High to GPIO Output Invalid | t_{CHPOI} | 1.5 | — | ns |
| G3 | GPIO Input Valid to FB_CLK High | t_{PVCH} | 8 | — | ns |
| G4 | FB_CLK High to GPIO Input Invalid | t_{CHPI} | 1.5 | — | ns |

NOTES:

¹ GPIO spec cover: \overline{IRQn} , UART and Timer pins.

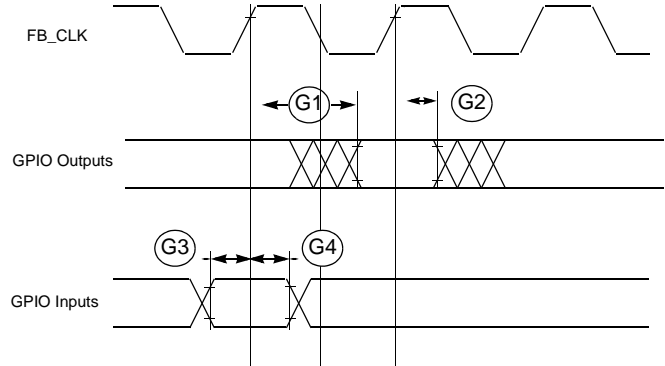


Figure 20. GPIO Timing

5.10 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing

| Num | Characteristic | Symbol | Min | Max | Unit |
|-----|---|--------------------|-----|-----|------------------|
| R1 | $\overline{\text{RESET}}$ Input valid to FB_CLK High | t_{RVCH} | 9 | — | ns |
| R2 | FB_CLK High to $\overline{\text{RESET}}$ Input invalid | t_{CHRI} | 1.5 | — | ns |
| R3 | $\overline{\text{RESET}}$ Input valid Time ¹ | t_{RIVT} | 5 | — | t_{CYC} |
| R4 | FB_CLK High to $\overline{\text{RSTOUT}}$ Valid | t_{CHROV} | — | 10 | ns |
| R5 | $\overline{\text{RSTOUT}}$ valid to Config. Overrides valid | t_{ROVCV} | 0 | — | ns |
| R6 | Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid | t_{COS} | 20 | — | t_{CYC} |
| R7 | Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid | t_{COH} | 0 | — | ns |
| R8 | $\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance | t_{ROICZ} | — | 1 | t_{CYC} |

NOTES:

¹ During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

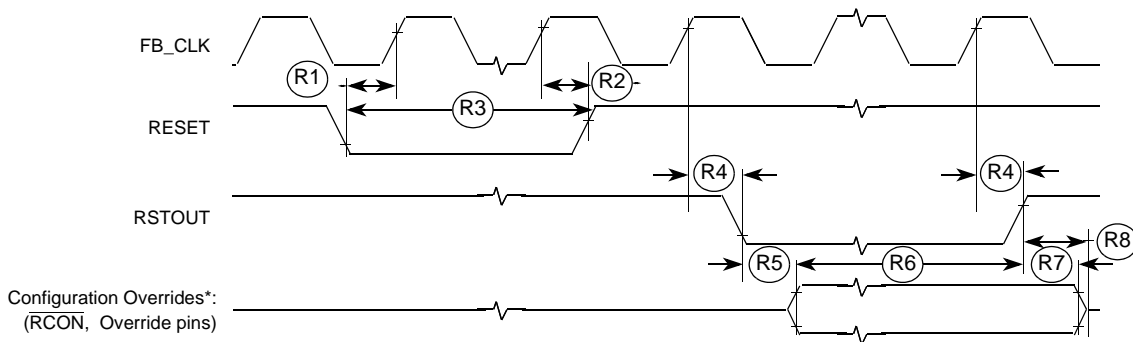


Figure 21. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the *MCF5208 Reference Manual* for more information.

5.11 I²C Input/Output Timing Specifications

Table 16 and Table 17 list specifications for the I²C input and output timing parameters.

Table 16. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

| Num | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|------------------|
| I1 | Start condition hold time | 2 | — | t _{cyc} |
| I2 | Clock low period | 8 | — | t _{cyc} |
| I3 | I2C_SCL/I2C_SDA rise time (V _{IL} = 0.5 V to V _{IH} = 2.4 V) | — | 1 | ms |
| I4 | Data hold time | 0 | — | ns |
| I5 | I2C_SCL/I2C_SDA fall time (V _{IH} = 2.4 V to V _{IL} = 0.5 V) | — | 1 | ms |
| I6 | Clock high time | 4 | — | t _{cyc} |
| I7 | Data setup time | 0 | — | ns |
| I8 | Start condition setup time (for repeated start condition only) | 2 | — | t _{cyc} |
| I9 | Stop condition setup time | 2 | — | t _{cyc} |

Table 17. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

| Num | Characteristic | Min | Max | Unit |
|------------------|--|-----|-----|------------------|
| I1 ¹ | Start condition hold time | 6 | — | t _{cyc} |
| I2 ^{1.} | Clock low period | 10 | — | t _{cyc} |
| I3 ² | I2C_SCL/I2C_SDA rise time (V _{IL} = 0.5 V to V _{IH} = 2.4 V) | — | — | μs |
| I4 ^{1.} | Data hold time | 7 | — | t _{cyc} |
| I5 ³ | I2C_SCL/I2C_SDA fall time (V _{IH} = 2.4 V to V _{IL} = 0.5 V) | — | 3 | ns |
| I6 ^{1.} | Clock high time | 10 | — | t _{cyc} |
| I7 ^{1.} | Data setup time | 2 | — | t _{cyc} |
| I8 ^{1.} | Start condition setup time (for repeated start condition only) | 20 | — | t _{cyc} |
| I9 ^{1.} | Stop condition setup time | 10 | — | t _{cyc} |

NOTES:

- ¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table A-16. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table A-16 are minimum values.
- ² Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
- ³ Specified at a nominal 50-pF load.

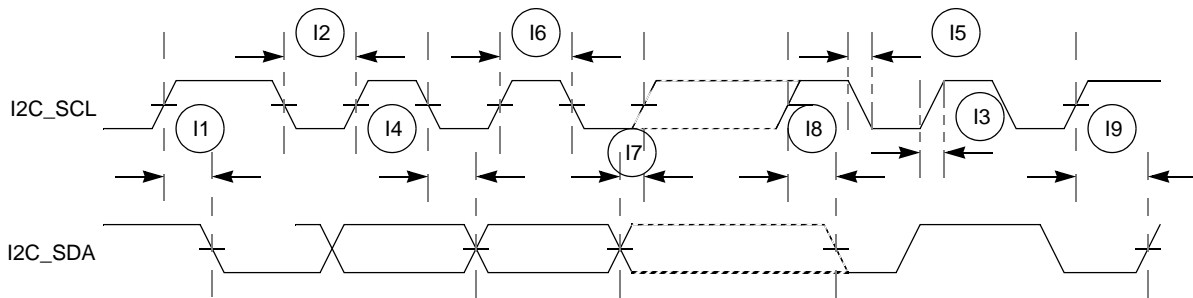


Figure 22. I²C Input/Output Timings

5.12 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

5.12.1 MII Receive Signal Timing (FEC_RXD[3:0], FEC_RXDV, FEC_RXER, and FEC_RXCLK)

The receiver functions correctly up to a FEC_RXCLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_RXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|---|-----|-----|------------------|
| M1 | FEC_RXD[3:0], FEC_RXDV, FEC_RXER to FEC_RXCLK setup | 5 | — | ns |
| M2 | FEC_RXCLK to FEC_RXD[3:0], FEC_RXDV, FEC_RXER hold | 5 | — | ns |
| M3 | FEC_RXCLK pulse width high | 35% | 65% | FEC_RXCLK period |
| M4 | FEC_RXCLK pulse width low | 35% | 65% | FEC_RXCLK period |

Figure 23 shows MII receive signal timings listed in Table 18.

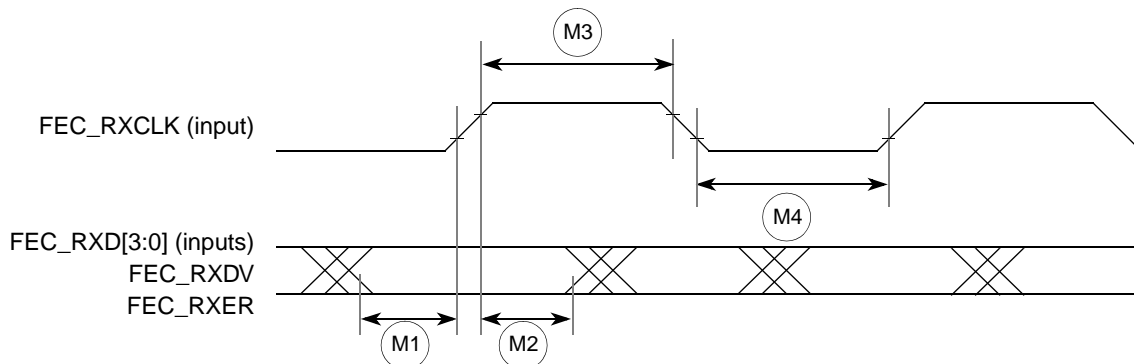


Figure 23. MII Receive Signal Timing Diagram

5.12.2 MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC_TXCLK maximum frequency of 25 MHz +1%. In addition, the processor clock frequency must exceed twice the FEC_TXCLK frequency.

Table 19. MII Transmit Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|---|-----|-----|------------------|
| M5 | FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER invalid | 5 | — | ns |
| M6 | FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER valid | — | 25 | ns |
| M7 | FEC_TXCLK pulse width high | 35% | 65% | FEC_TXCLK period |
| M8 | FEC_TXCLK pulse width low | 35% | 65% | FEC_TXCLK period |

Figure 24 shows MII transmit signal timings listed in Table 19.

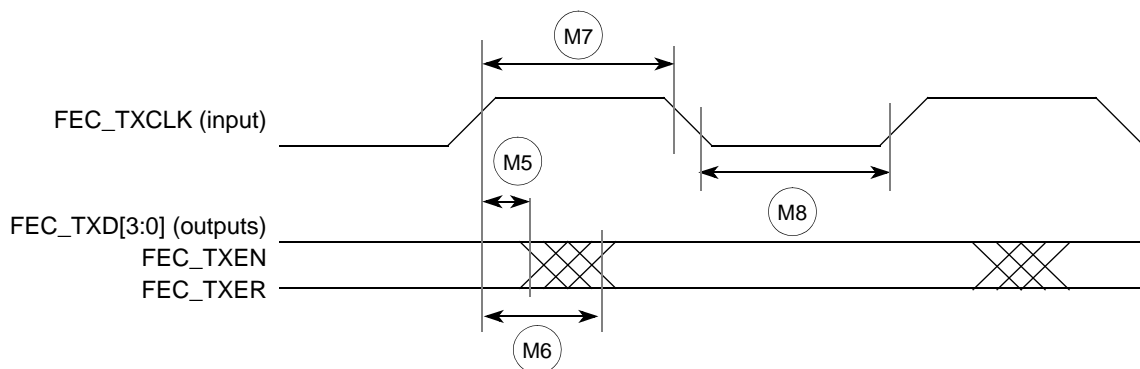


Figure 24. MII Transmit Signal Timing Diagram

5.12.3 MII Async Inputs Signal Timing (FEC_CRIS and FEC_COL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|---------------------------------------|-----|-----|------------------|
| M9 | FEC_CRIS, FEC_COL minimum pulse width | 1.5 | — | FEC_TXCLK period |

Figure 25 shows MII asynchronous input timings listed in Table 20.

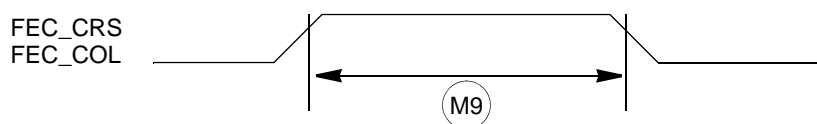


Figure 25. MII Async Inputs Timing Diagram

5.12.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

| Num | Characteristic | Min | Max | Unit |
|-----|---|-----|-----|----------------|
| M10 | FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | FEC_MDC falling edge to FEC_MDIO output valid (max prop delay) | — | 25 | ns |
| M12 | FEC_MDIO (input) to FEC_MDC rising edge setup | 10 | — | ns |
| M13 | FEC_MDIO (input) to FEC_MDC rising edge hold | 0 | — | ns |
| M14 | FEC_MDC pulse width high | 40% | 60% | FEC_MDC period |
| M15 | FEC_MDC pulse width low | 40% | 60% | FEC_MDC period |

Figure 26 shows MII serial management channel timings listed in Table 21.

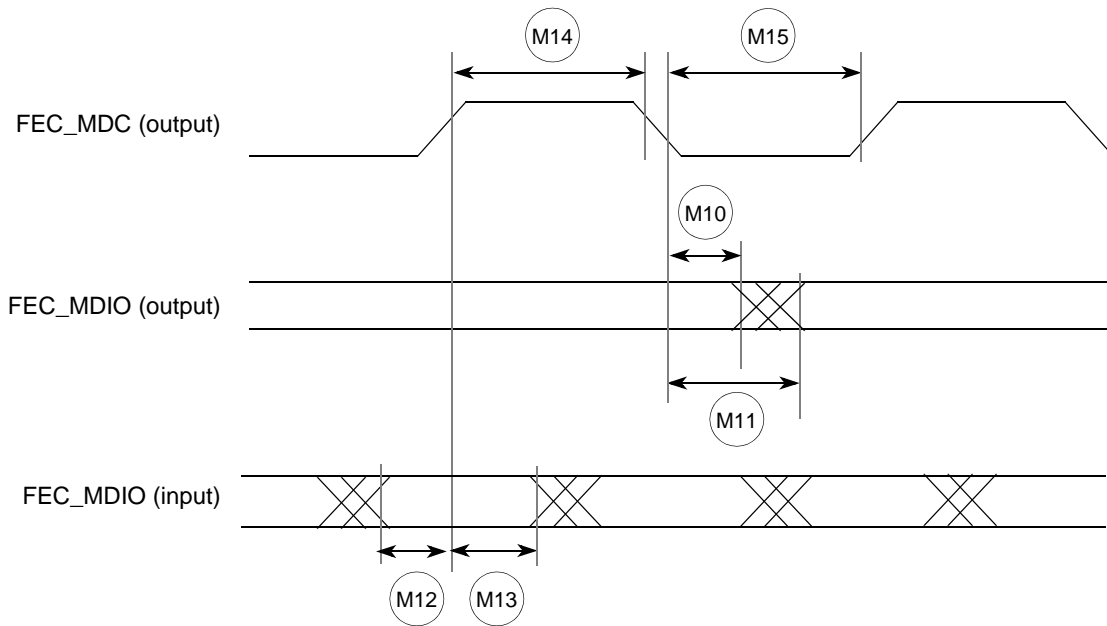


Figure 26. MII Serial Management Channel Timing Diagram

5.13 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

| Name | Characteristic | | | Unit |
|------|---|-----|-----|-----------|
| | | Min | Max | |
| T1 | DT0IN / DT1IN / DT2IN / DT3IN cycle time | 3 | — | t_{CYC} |
| T2 | DT0IN / DT1IN / DT2IN / DT3IN pulse width | 1 | — | t_{CYC} |

5.14 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

| Name | Characteristic | Min | Max | Unit |
|------|---|-----|-----|------|
| QS1 | QSPI_CS[3:0] to QSPI_CLK | 1 | 510 | tcyc |
| QS2 | QSPI_CLK high to QSPI_DOUT valid. | — | 10 | ns |
| QS3 | QSPI_CLK high to QSPI_DOUT invalid. (Output hold) | 1.5 | — | ns |
| QS4 | QSPI_DIN to QSPI_CLK (Input setup) | 9 | — | ns |
| QS5 | QSPI_DIN to QSPI_CLK (Input hold) | 9 | — | ns |

The values in Table 23 correspond to Figure 27.

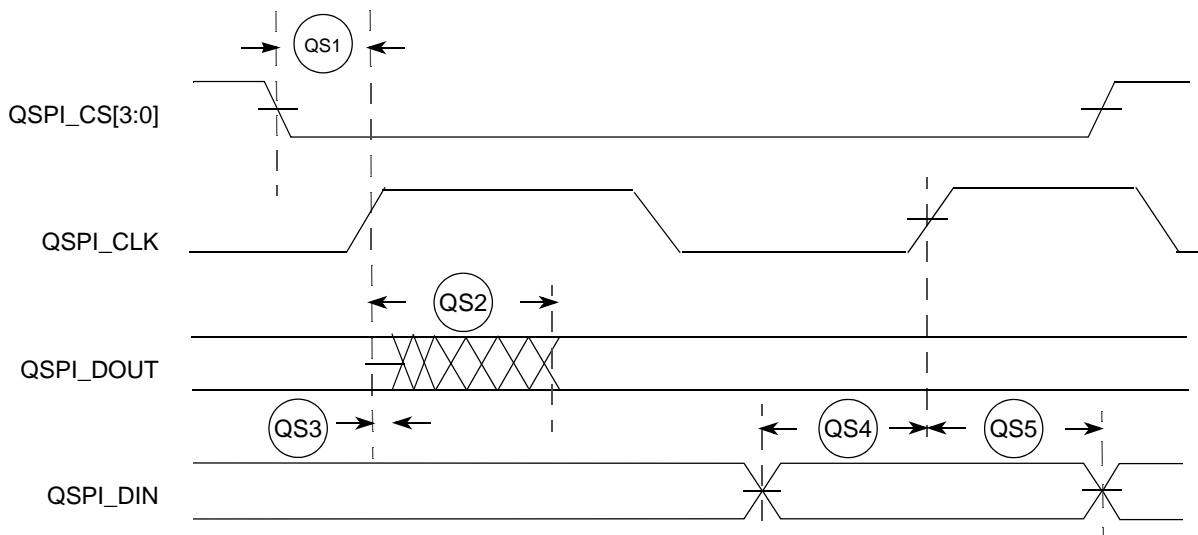


Figure 27. QSPI Timing

5.15 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

| Num | Characteristics ¹ | Symbol | Min | Max | Unit |
|-----|--|--------------|-----|-----|-------------|
| J1 | TCLK Frequency of Operation | f_{JCYC} | DC | 1/4 | $f_{sys/2}$ |
| J2 | TCLK Cycle Period | t_{JCYC} | 4 | — | t_{CYC} |
| J3 | TCLK Clock Pulse Width | t_{JCW} | 26 | — | ns |
| J4 | TCLK Rise and Fall Times | t_{JCRF} | 0 | 3 | ns |
| J5 | Boundary Scan Input Data Setup Time to TCLK Rise | t_{BSDST} | 4 | — | ns |
| J6 | Boundary Scan Input Data Hold Time after TCLK Rise | t_{BSDHT} | 26 | — | ns |
| J7 | TCLK Low to Boundary Scan Output Data Valid | t_{BSDV} | 0 | 33 | ns |
| J8 | TCLK Low to Boundary Scan Output High Z | t_{BSDZ} | 0 | 33 | ns |
| J9 | TMS, TDI Input Data Setup Time to TCLK Rise | t_{TAPBST} | 4 | — | ns |
| J10 | TMS, TDI Input Data Hold Time after TCLK Rise | t_{TAPBHT} | 10 | — | ns |
| J11 | TCLK Low to TDO Data Valid | t_{TDODV} | 0 | 26 | ns |
| J12 | TCLK Low to TDO High Z | t_{TDODZ} | 0 | 8 | ns |
| J13 | \overline{TRST} Assert Time | t_{TRSTAT} | 100 | — | ns |
| J14 | \overline{TRST} Setup Time (Negation) to TCLK High | t_{TRSTST} | 10 | — | ns |

NOTES:

¹ JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

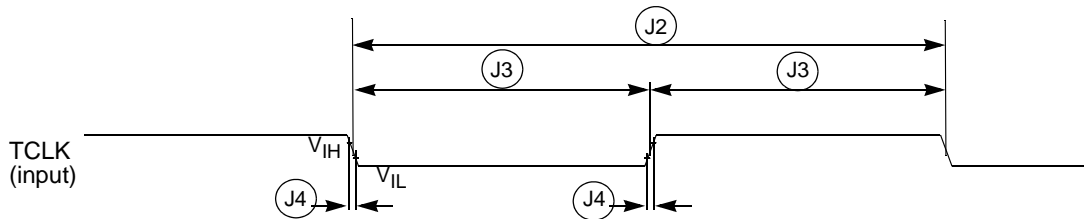


Figure 28. Test Clock Input Timing

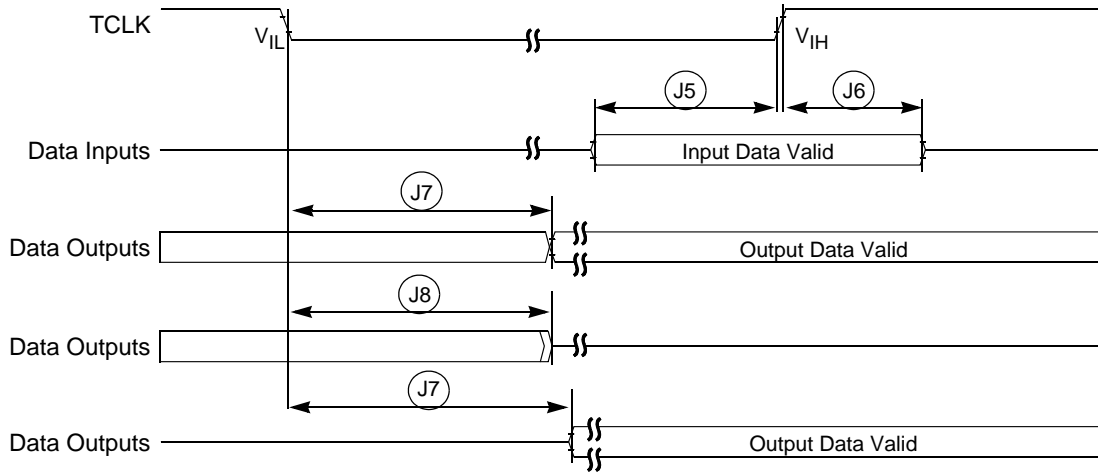


Figure 29. Boundary Scan (JTAG) Timing

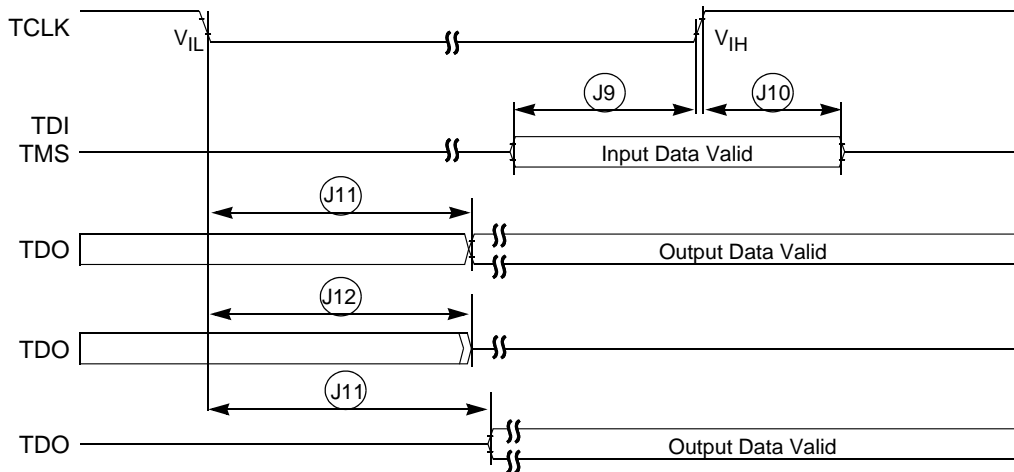


Figure 30. Test Access Port Timing

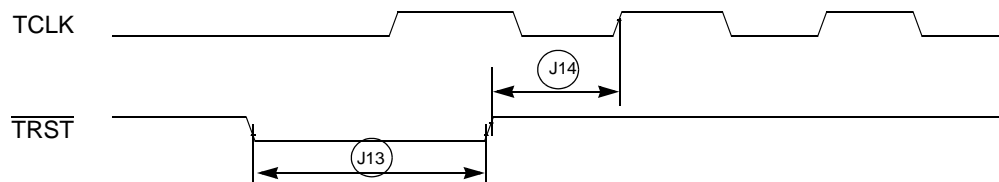


Figure 31. $\overline{\text{TRST}}$ Timing

5.16 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 32.

Table 25. Debug AC Timing Specification

| Num | Characteristic | Min | Max | Unit |
|-----------------|-----------------------------------|-----|-----|-----------|
| D0 | PSTCLK cycle time | 1 | 1 | t_{sys} |
| D1 | PSTCLK rising to PSTDDATA valid | — | 3.0 | ns |
| D2 | PSTCLK rising to PSTDDATA invalid | 1.5 | — | ns |
| D3 | DSI-to-DSCLK setup | 1 | — | PSTCLK |
| D4 ¹ | DSCLK-to-DSO hold | 4 | — | PSTCLK |
| D5 | DSCLK cycle time | 5 | — | PSTCLK |
| D6 | BKPT assertion time | 1 | — | PSTCLK |

NOTES:

¹ DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

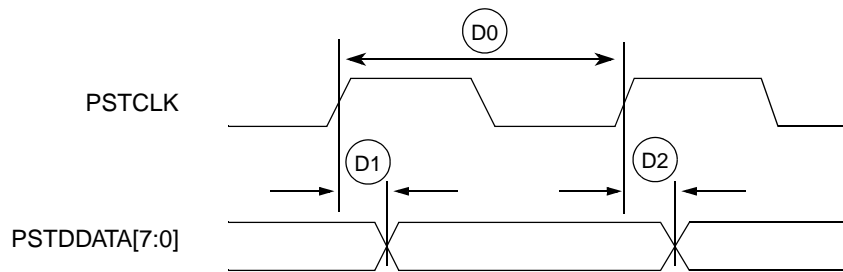


Figure 32. Real-Time Trace AC Timing

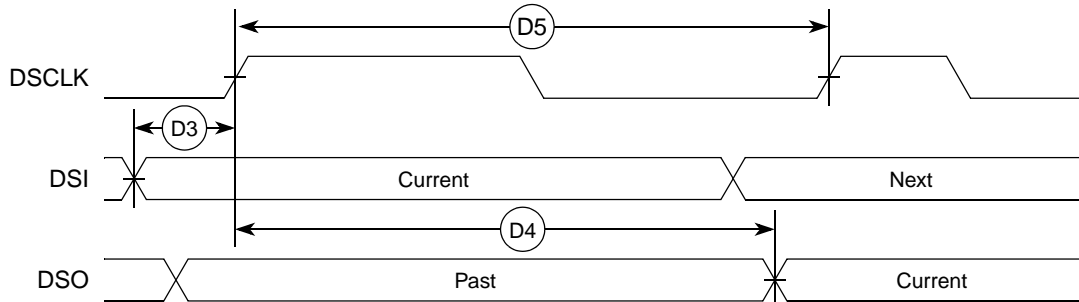


Figure 33. BDM Serial Port AC Timing

6 Revision History

Table 26. Revision History

| Revision Number | Date | Substantive Changes |
|-----------------|-----------|---|
| 0 | 5/23/2005 | <ul style="list-style-type: none"> Initial Release |
| 0.1 | 6/16/2005 | <ul style="list-style-type: none"> Corrected 144QFP pinout in Figure 1. Pins 139-142 incorrectly showed FEC functionality, which are actually UART 0/1 clear-to-send and request-to-send signals. Changed maximum core frequency in Table 10, spec #2, from 240MHz to 166.67MHz. Also, changed symbols in table: $f_{core} \rightarrow f_{sys}$ and $f_{sys} \rightarrow f_{sys/2}$ for consistency throughout document and reference manual. |
| 0.2 | 8/26/2005 | <ul style="list-style-type: none"> Changed ball M9 from SD_VDD to EVDD in Figure 9. Table 3: Pin 33 for 144 LQFP package should be EVDD instead of SD_VDD. $\overline{BE}/\overline{BWE}[3:0]$ for 144 LQFP should be "20, 48, 18, 50" instead of "18, 20, 48, 50" <p>Cleaned up various electrical specifications:</p> <ul style="list-style-type: none"> Table 4: Added DDR/Memory pad supply voltage spec, changed "clock synthesizer supply voltage" to "PLL supply voltage", changed min $PLL_{V_{DD}}$ from -0.5 to -0.3, changed max V_{IN} from 4.0 to 3.6, changed minimum T_{stg} from -65 to -55, Table 5: Changed TBD values in T_j entry to 105°C. Table 7: Changed minimum core supply voltage from 1.35 to 1.4 and maximum from 1.65 to 1.6, added PLL supply voltage entry, added pad supply entries for mobile-DDR, DDR, and SDR, changed minimum input high voltage from $0.7 \times EV_{DD}$ to 2 and maximum from 3.65 to $EV_{DD} + 0.05$, changed minimum input low voltage from $VSS - 0.3$ to -0.05 and maximum from $0.35 \times EV_{DD}$ to 0.8, added input high/low voltage entries for DDR and mobile-DDR, removed high impedance leakage current entry, changed minimum output high voltage from $EV_{DD} - 0.5$ to $EV_{DD} - 0.4$, added DDR/bus output high/low voltage entries, removed load capacitance and DC injection current entries. Added filtering circuits and voltage sequencing sections: Section 5.4.1, "PLL Power Filtering," and Section 5.4.2, "Supply Voltage Sequencing and Separation Cautions." Removed "Operating Conditions" table from Section 5.6, "Oscillator and PLL Electrical Characteristics," because it is redundant with Table 7. Table 11: Changed minimum core frequency to TBD, removed external reference and on-chip PLL frequency specs to have only a CLKOUT frequency spec of TBD to 83.33MHz, removed loss of reference frequency and self-clocked mode frequency entries, in EXTAL input high/low voltage entries changed "All other modes (Dual controller (1:1), Bypass, External)" to "All other modes (External, Limp)", removed XTAL output high/low voltage entries, removed power-up to lock time entry, removed last 5 entries (frequency un-lock range, frequency lock range, CLKOUT period jitter, frequency modulation range limit, and ICO frequency) |
| 0.3 | 9/07/2005 | <ul style="list-style-type: none"> Corrected DRAMSEL footnote #3 in Table 3. Updated Table 3 with 144MAPBGA pin locations. Added 144MAPBGA ballmap to Section 4.3, "Pinout—144 MAPBGA." Changed J12 from PLL_VDD to IVDD in Figure 9. |

Table 26. Revision History (continued)

| Revision Number | Date | Substantive Changes |
|-----------------|------------|---|
| 0.4 | 10/10/2005 | <ul style="list-style-type: none"> • Figure 1 and Table 3: Changed pin 33 from EVDD to SD_VDD • Figure 4 and Table 3: Changed ball D10 from TEST to VSS • Figure 6 and Table 3: Changed pin 39 from EVDD to SD_VDD and pin 117 from TEST to VSS |
| 0.5 | 3/29/2006 | <ul style="list-style-type: none"> • Added “top view” and “bottom view” labels where appropriate to mechanical drawings and pinouts. • Updated mechanical drawings to latest available, and added note to Section 4, “Mechanicals and Pinouts.” |
| 0.6 | 7/21/2006 | <ul style="list-style-type: none"> • Corrected cross-reference to Figure 9 in Section 4.7, “Pinout—196 MAPBGA.” • Corrected L3 label in Figure 9 from SD_DR_DQS to SD_SDR_DQS. • Corrected L6 label in Figure 9 from SD_DQS0 to SD_DQS2 and H3 from SD_DQS1 to SD_DQS3. • Removed second sentence from Section 5.12.2, “MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK),” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.12.2, “MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK),” as this feature is not supported on this device. |
| 1 | 3/28/2007 | <ul style="list-style-type: none"> • Removed preliminary designation from Section 5, “Electrical Characteristics.” • Updated Section 5.2, “Thermal Characteristics.” • Updated Section 5.4, “DC Electrical Specifications.” • Added Section 5.5, “Current Consumption.” • Updated Section 5.6, “Oscillator and PLL Electrical Characteristics.” • Made some corrections to the drawings in Section 5.8, “SDRAM Bus.” • Edited for grammar, punctuation, spelling, style, and format. - JD |
| 2 | 12/4/2008 | <ul style="list-style-type: none"> • Updated FlexBus read and write timing diagrams in Figure 14 and Figure 15. <p>Changed the following specs in Table 12 and Table 13:</p> <ul style="list-style-type: none"> • Minimum frequency of operation from TBD to 60MHz • Maximum clock period from TBD to 16.67 ns |
| 3 | 9/1/2009 | <ul style="list-style-type: none"> • Changed doc type from Advance Information to Technical Data |

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