NXP Semiconductors
Data Sheet: Technical Data

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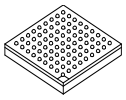
MCIMX6G1AVM05AA
MCIMX6G1AVM07AA
MCIMX6G2AVM05AA
MCIMX6G2AVM07AA

MCIMX6G1AVM05AB
MCIMX6G1AVM07AB
MCIMX6G2AVM05AB
MCIMX6G2AVM07AB

i.MX 6UltraLite Automotive Applications Processors



Package Information
Plastic Package
BGA 14 x 14 mm, 0.8 mm pitch

Ordering Information
See Table 1 on page 3

1 i.MX 6UltraLite introduction

The i.MX 6UltraLite is a high performance, ultra efficient processor family featuring NXP's advanced implementation of the single ARM Cortex®-A7 core, which operates at speeds up to 696 MHz. The i.MX 6UltraLite includes an integrated power management module that reduces the complexity of the external power supply and simplifies the power sequencing. Each processor in this family provides various memory interfaces, including LPDDR2, DDR3, DDR3L, Raw and Managed NAND flash, NOR flash, eMMC, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.

The i.MX 6UltraLite is specifically useful for automotive applications such as:

- Telematics
- Human Machine Interfaces (HMI)

The features of the i.MX 6UltraLite processor include[1]:

- Single-core ARM Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of each device is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The device supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—Multimedia performance is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- Ethernet interfaces—10/100 Mbps Ethernet controllers.
- Human-machine interface—Support digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: High-speed USB on-the-go with PHY, multiple expansion card port (high-speed MMC/SDIO host and other), 12-bit ADC module, CAN port, smart card interface compatible with EMV Standard v4.3, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Automotive environment support—Each processor includes interfaces, such as CAN, three SAI audio interfaces, and an asynchronous sample rate converter for multichannel/multisource audio.
- Advanced security—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the *i.MX 6UltraLite Security Reference Manual* (IMX6ULSRM).
- Integrated power management—The processor integrates linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6UltraLite features, see Section 1.2, “Features"”.

1. The actual feature set depends on the part numbers as described in the Table 1 and Table 2.

1.1 Ordering information

Table 1 provides examples of orderable part numbers covered by this data sheet. The automotive parts in this subset of the i.MX 6UltraLite derivatives are single core devices offered in a 14x14 mm, 0.8 pitch BGA whose temperature range is -40 ^{o} C to 125 ^{o} C. Each of these devices have differences in characteristics or features according to the Table 2.

Table 1. Ordering Information

Part Number	Core Frequency	eFuse Bits	Ethernet Ports (10/100M)	CAN	ADC	CSI	LCD IF
MCIMX6G1AVM05AA	528 MHz	1024	1	1	1	No	No
MCIMX6G1AVM05AB	528 MHz	1024	1	1	1	No	No
MCIMX6G1AVM07AA	696 MHz	1024	1	1	1	No	No
MCIMX6G1AVM07AB	696 MHz	1024	1	1	1	No	No
MCIMX6G2AVM05AA	528 MHz	1536	2	2	2	Yes	Yes
MCIMX6G2AVM05AB	528 MHz	1536	2	2	2	Yes	Yes
MCIMX6G2AVM07AA	696 MHz	1536	2	2	2	Yes	Yes
MCIMX6G2AVM07AB	696 MHz	1536	2	2	2	Yes	Yes

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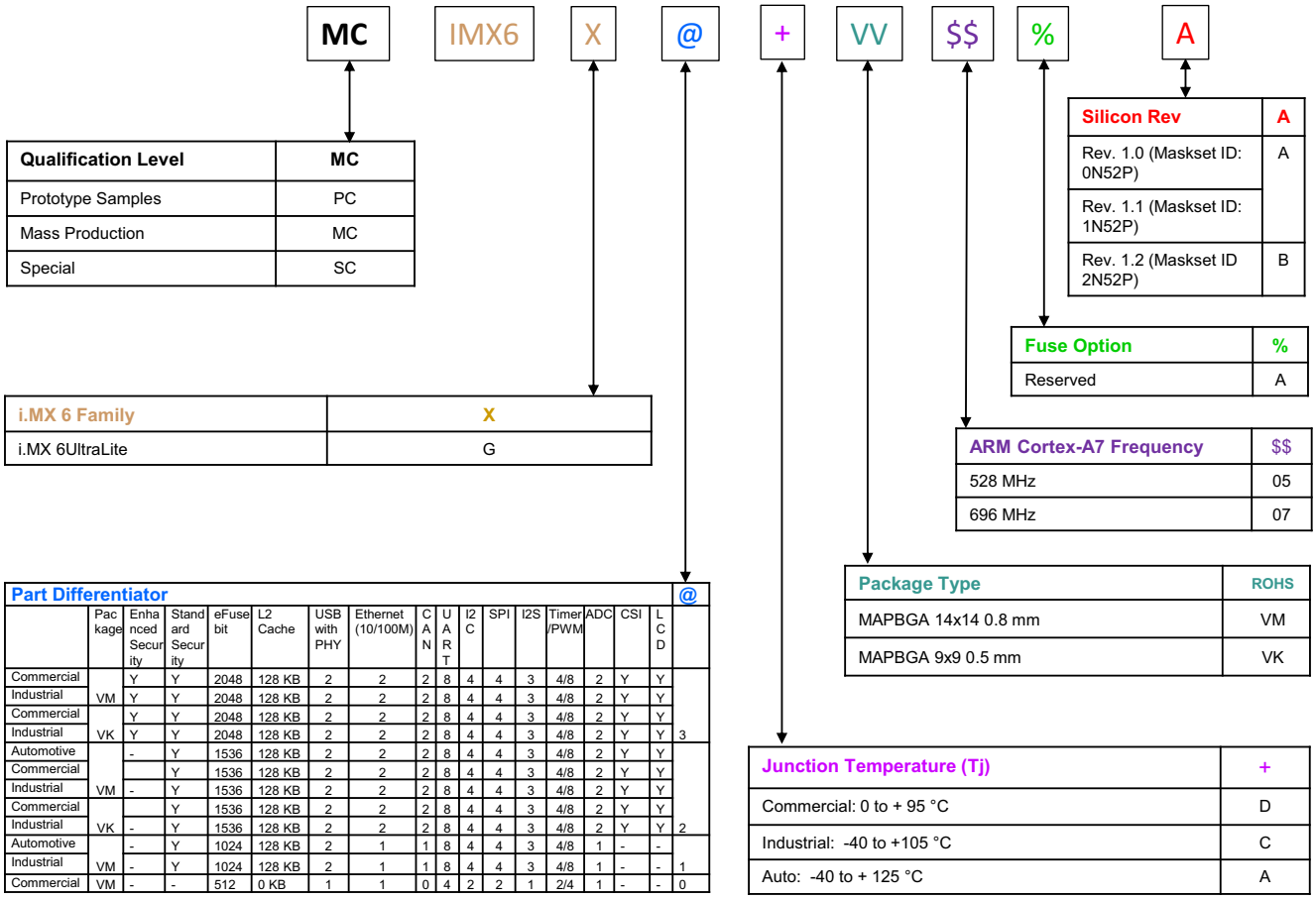
Figure 1 describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX 6UltraLite Automotive Applications Processors Data Sheet (IMX6ULAEC) covers parts listed with an “A (Automotive temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page nxp.com/imx6series or contact an NXP representative for details.



	Package	Enhanced Security	Standard Security	eFuse bit	L2 Cache	USB with PHY	Ethernet (10/100M)	CAN	UART	I2C	SPI	I2S	Timer/PWM	ADC	CSI	LCD	@
Commercial		Y	Y	2048	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	
Industrial	VM	Y	Y	2048	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	
Commercial		Y	Y	2048	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	
Industrial	VK	Y	Y	2048	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	3
Automotive		-	Y	1536	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	
Commercial			Y	1536	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	
Industrial	VM	-	Y	1536	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	
Commercial			Y	1536	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	
Industrial	VK	-	Y	1536	128 KB	2	2	2	8	4	4	3	4/8	2	Y	Y	2
Automotive		-	Y	1024	128 KB	2	1	1	8	4	4	3	4/8	1	-	-	
Industrial	VM	-	Y	1024	128 KB	2	1	1	8	4	4	3	4/8	1	-	-	1
Commercial	VM	-	-	512	0 KB	1	1	0	4	2	2	1	2/4	1	-	-	0

Figure 1. Part Number Nomenclature—i.MX 6UltraLite

Table 2 shows the detailed information about peripherals.

Table 2. Detailed Peripherals Information [1,2,3]

Peripheral Name	Instance	G0	G1	G2	G3
Ethernet	ENET1	Y	Y	Y	Y
	ENET2	NA	NA	Y	Y
USB with PHY	OTG1	Y	Y	Y	Y
	OTG2	NA	Y	Y	Y
CAN	FLEXCAN1	NA	Y	Y	Y
	FLEXCAN2	NA	NA	Y	Y
CSI	CSI	NA	NA	Y	Y
LCD	LCDIF	NA	NA	Y	Y
QSPI	QSPI	Y	Y	Y	Y

Table 2. Detailed Peripherals Information (continued)[1,2,3]

Peripheral Name	Instance	G0	G1	G2	G3
SDIO	uSDHC1	Y	Y	Y	Y
	uSDHC2	Y	Y	Y	Y
UART	UART1	Y	Y	Y	Y
	UART2	Y	Y	Y	Y
	UART3	Y	Y	Y	Y
	UART4	Y	Y	Y	Y
	UART5	NA	Y	Y	Y
	UART6	NA	Y	Y	Y
	UART7	NA	Y	Y	Y
	UART8	NA	Y	Y	Y
ISO7816-3	SIM1	NA	Y	Y	Y
	SIM2	NA	Y	Y	Y
I2C	I2C1	Y	Y	Y	Y
	I2C2	Y	Y	Y	Y
	I2C3	NA	Y	Y	Y
	I2C4	NA	Y	Y	Y
SPI	ECSPI1	Y	Y	Y	Y
	ECSPI2	Y	Y	Y	Y
	ECSPI3	NA	Y	Y	Y
	ECSPI4	NA	Y	Y	Y
I2S/SAI	SAI1	Y	Y	Y	Y
	SAI2	NA	Y	Y	Y
	SAI3	NA	Y	Y	Y

Table 2. Detailed Peripherals Information (continued)[1,2,3]

Peripheral Name	Instance	G0	G1	G2	G3
Timer/PWM	EPIT1	Y	Y	Y	Y
	EPIT2	NA	Y	Y	Y
	GPT1	Y	Y	Y	Y
	GPT2	NA	Y	Y	Y
	PWM1	Y	Y	Y	Y
	PWM2	Y	Y	Y	Y
	PWM3	Y	Y	Y	Y
	PWM4	Y	Y	Y	Y
	PWM5	NA	Y	Y	Y
	PWM6	NA	Y	Y	Y
	PWM7	NA	Y	Y	Y
	PWM8	NA	Y	Y	Y
ADC	ADC1	Y	Y	Y	Y
	ADC2	NA	NA	Y	Y

[1] For detailed pin mux information, please refer to “Chapter 4 External Signals and Pin Multiplexing” of *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

[2] Y stands for yes, NA stands for not available.

[3] G0 and G3 are offered in automotive grade.

1.2 Features

The i.MX 6UltraLite processors are based on ARM Cortex-A7 MPCore™ Platform, which has the following features:

- Supports single ARM Cortex-A7 MPCore (with TrustZone) with:
  - 32 KBytes L1 Instruction Cache
  - 32 KBytes L1 Data Cache
  - Private Timer
  - Cortex-A7 NEON Media Processing Engine (MPE) Co-processor
- General Interrupt Controller (GIC) with 128 interrupts support
- Global Timer
- Snoop Control Unit (SCU)
- 128 KB unified I/D L2 cache
- Single Master AXI bus interface output of L2 cache
- Frequency of the core (including Neon and L1 cache), as per Table 10, "Operating Ranges," on page 23.

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia/shared, fast access RAM (OCRAM, 128 KB)
- Secure/non-secure RAM (32 KB)

- External memory interfaces: The i.MX 6UltraLite processors support handheld DRAM, NOR, and NAND Flash memory standards.
  - 16-bit LP-DDR2-800, 16-bit DDR3-800 and LV-DDR3-800
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bits.
  - 16/8-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.

Each i.MX 6UltraLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays:
  - One parallel display port supports max 85 MHz display clock and up to WXGA (1366 x 768) at 60 Hz
  - Support 24-bit, 18-bit, 16-bit, and 8-bit parallel display
- Camera sensors[1]:
  - One parallel camera port, up to 24 bit and 148.5 MHz pixel clock
  - Support 24-bit, 16-bit, 10-bit, and 8-bit input
  - Support BT.656 interface
- Expansion cards:
  - Two MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
    - 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
- USB:
  - Two high speed (HS) USB 2.0 OTG (Up to 480 Mbps) with integrated HS USB Phy
- Miscellaneous IPs and interfaces:
  - Three SAI supporting up to three I2S
  - Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
  - Eight UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - Support RTS/CTS for hardware flow control
  - Four enhanced CSPI (eCSPI)

1. G2 and G3 only

- Four I^2C
- Two 10/100M Ethernet Controller (IEEE1588 compliant)
- Eight Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- One Quad SPI
- Two Flexible Controller Area Network (FlexCAN)
- Three Watchdog timers (WDOG)
- Two 12-bit Analog to Digital Converters (ADC) with up to 10 input channels in total
- Touch Screen Controller (TSC)

The i.MX 6UltraLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Use Voltage Sensor for monitoring the die voltage
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and NEON
- Support various levels of system power modes
- Use flexible clock gating control scheme
- Two smart card interfaces compatible with EVM Standard 4.3

The i.MX 6UltraLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption, while having the CPU core relatively free for performing other tasks.

The i.MX 6UltraLite processors incorporate the following hardware accelerators:

- PXP—Pixel Processing Pipeline for imagine resize, rotation, overlay and CSC[1]. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 32 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock.
- CSU—Central Security Unit. CSU is configured during boot and by eFUSEs and determine the security level operation mode as well as the TZ policy.

1. G2 and G3 only

- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1 and Table 2. Functions such as display and camera interfaces, connectivity interfaces, and security features are not offered on all derivatives.

2 Architectural overview

The following subsections provide an architectural overview of the i.MX 6UltraLite processor system.

2.1 Block diagram

Figure 2 shows the functional modules in the i.MX 6UltraLite processor system.

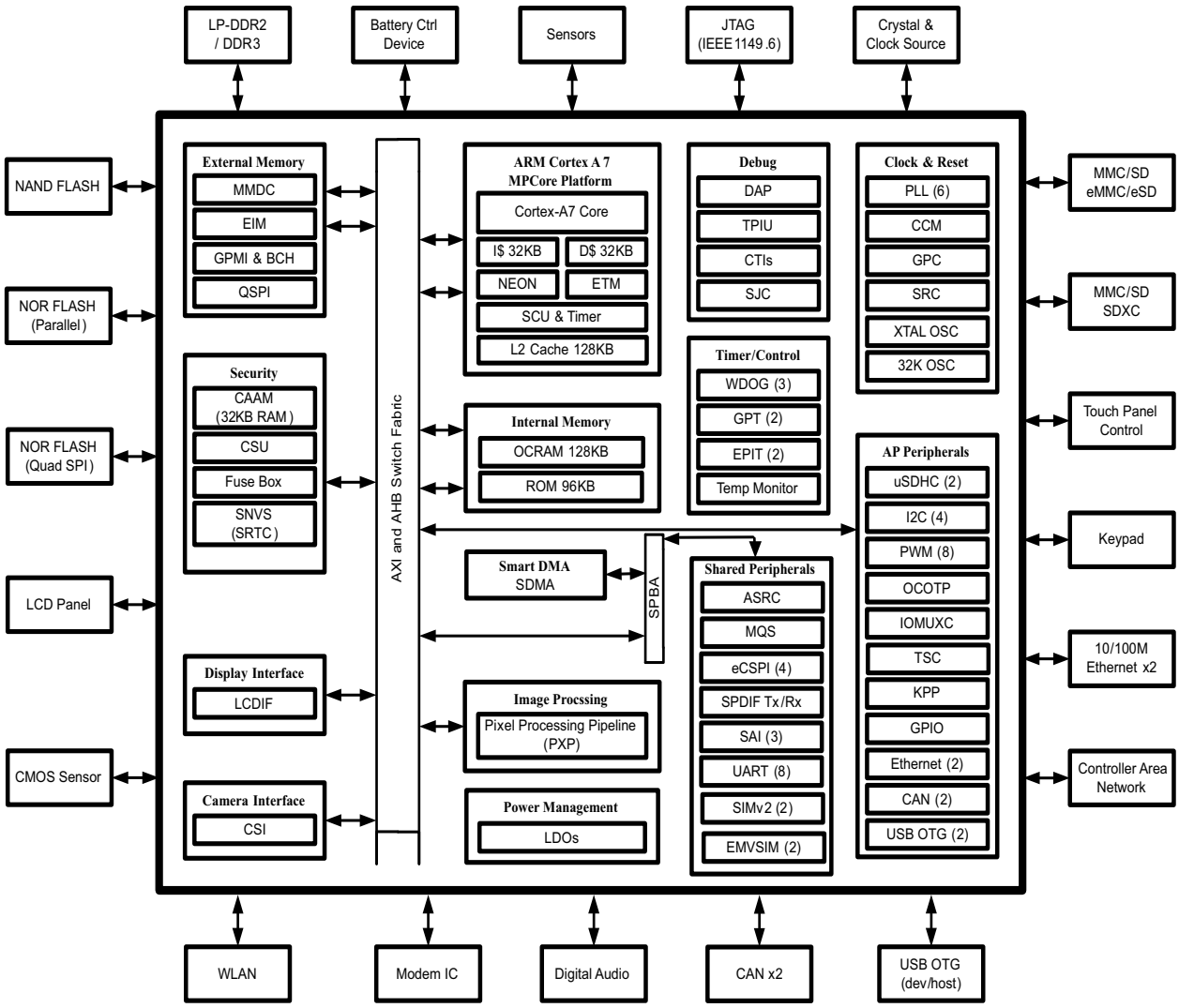


Figure 2. i.MX 6UltraLite System Block Diagram[1]

1. Some modules shown in this block diagram are not offered on all derivatives. See Table 2 for exceptions.

3 Modules list

The i.MX 6UltraLite processors contain a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.[1]

Table 3. i.MX 6UltraLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
ADC1 ADC2	Analog to Digital Converter	—	The ADC is a 12-bit general purpose analog to digital converter.
ARM	ARM Platform	ARM	The ARM Core Platform includes 1x Cortex-A7 core. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
BCH	Binary-BCH ECC Processor	System Control Peripherals	The BCH module provides up to 40-bit ECC for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its deterministic random bit generator (DRBG) validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6UltraLite processors, the security memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.

1. Note that some modules listed in this table are not offered on all derivatives. See Table 2 for exceptions.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6UltraLite platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A7 Core Platform.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit NOR-Flash memories, at slow frequency • Multiple chip selects
EMV SIM1 EMV SIM2	Europay, Master and Visa Subscriber Identification Module	Connectivity peripherals	EMV SIM is designed to facilitate communication to Smart Cards compatible to the EMV version 4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 standard.
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPMI	General Purpose Memory Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices and 40-bit ECC for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2	General Purpose Timer	Timer peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module act as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Support of byte-swapping • Library of Scripts and API is available
2x SIMv2	Smart Card	Connectivity peripherals	Smart card interface compliant with ISO7816.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6UltraLite processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6UltraLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
System Counter	—	—	The system counter module is a programmable system counter which provides a shared time base to the Cortex A series cores as part of ARM's generic timer architecture. It is intended for use in application where the counter is always powered on and supports multiple, unrelated clocks.
TSC	Touch Screen	Touch Controller	With touch controller to support 4-wire and 5-wire resistive touch panel.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4 UART5 UART6 UART7 UART8	UART Interface	Connectivity Peripherals	Each of the UART modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6UltraLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
USB	Universal Serial Bus 2.0	Connectivity Peripherals	USBO2 (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
WDOG1 WDOG3	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.

3.1 Special signal considerations

Table 4 lists special signal considerations for the i.MX 6UltraLite processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments"." Signal descriptions are provided in the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

Table 4. Special Signal Considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused either or both of the CLK1_N/P pairs may remain unconnected.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI is mounted with 18 pF capacitor. Please refer to the EVK board reference design for details. The logic level of this forcing clock cannot exceed NVCC_PLL level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.

Table 4. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user can tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when two DDR3 ICs plus the i.MX 6UltraLite are drawing current on the resistor divider.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
GPANAIO	This signal is reserved for NXP manufacturing use only. This output must remain unconnected.
JTAG_*nnnn*	The JTAG interface is summarized in Table 5. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6UltraLite reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.
TEST_MODE	TEST_MODE is for NXP factory use. The user must tie this pin directly to GND.

Table 5. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up

Table 5. JTAG Controller Interface Summary (continued)

JTAG	I/O Type	On-chip Termination
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended connections for unused analog interfaces

Table 6 shows the recommended connections for unused analog interfaces.

Table 6. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused
CCM	CCM_CLK1_N, CCM_CLK1_P	Float
USB	USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_CHD_B, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS	Float
ADC	ADC_VREFH	Tie to VDDA_ADC_3P3
	VDDA_ADC_3P3	VDDA_ADC_3P3 must be powered even if the ADC is not used.

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6UltraLite processors.

4.1 Chip-Level conditions

This section provides the device-level electrical characteristics for the IC. See Table 7 for a quick reference to the individual tables and sections.

Table 7. i.MX 6UltraLite Chip-Level Conditions

For these characteristics	Topic appears
Absolute maximum ratings	on page 20
Thermal resistance	on page 21
Operating ranges	on page 22
External clock sources	on page 24
Maximum supply currents	on page 25
Low power mode supply currents	on page 27
USB PHY current consumption	on page 28

4.1.1 Absolute maximum ratings

CAUTION

Stress beyond those listed under Table 8 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 8 shows the absolute maximum operating ratings.

Table 8. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core Supplies Input Voltage (LDO Enabled)	VDD_SOC_IN	-0.3	1.6	V
Core Supplies Input Voltage (LDO Bypass)	VDD_SOC_IN	-0.3	1.4	V
VDD_HIGH_IN Supply voltage	VDD_HIGH_IN	-0.3	3.6	V
Core Supplies Output Voltage (LDO Enabled)	VDD_ARM_CAP VDD_SOC_CAP	-0.3	1.4	V
VDD_HIGH_CAP LDO Output Supply Voltage	VDD_HIGH_CAP	-0.3	2.6	V

Table 8. Absolute Maximum Ratings (continued)

Supply Input Voltage to Secure Non-Volatile Storage and Real Time Clock	VDD_SNVS_IN	-0.3	3.6	
USB VBUS Supply	USB_OTG_VBUS	—	5.5	V
IO Supply for DDR Interface	NVCC_DRAM	-0.4	1.975 (See note 1)	V
Supply for DDR pre-drivers	NVCC_DRAM_2P5	-0.3	2.85	V
IO Supply for GPIO Type Pins	NVCC_CSI NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NAND NVCC_SD1	-0.5	3.7	V
Supply for ADC 3P3V	VDDA_ADC_3P3	—	3.7	V
MLB I/O Supply Voltage	Supplies denoted as I/O Supply	-0.3	2.8	V
Input/Output Voltage range (Non-DDR pins)	V_{in}/V_{out}	-0.5	OVDD + 0.3 (See note 2)	V
Input/Output Voltage range (DDR Pins)	V_{in}/V_{out}	-0.5	OVDD + 0.4 (See note 1, 2)	V
ESD damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	 V
Storage Temperature range	$T_{STORAGE}$	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575 V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal resistance

4.1.2.1 14x14 MM (VM) package thermal resistance

Table 9 displays the 14x14 MM (VM) package thermal resistance data.

Table 9. 14x14 MM (VM) Thermal Resistance Data[1]

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural convection	Single-layer board (1s)	$R_{\theta JA}$	58.4	°C/W	2,3
Junction to Ambient Natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	37.6	°C/W	3,3,4
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	48.6	°C/W	2,4
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	32.9	°C/W	2,4

Table 9. 14x14 MM (VM) Thermal Resistance Data[1]

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Board	—	$R_{\theta JB}$	21.8	°C/W	5
Junction to Case	—	$R_{\theta JC}$	19.3	°C/W	6
Junction to Package Top	Natural Convection	Ψ_{JT}	2.3	°C/W	7
Junction to Package Bottom	Natural Convection	Ψ_{JB}	12.0	°C/W	8

1 As per JEDEC JESD51-2 the intent of (thermal resistance) measurement is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

8 Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB

4.1.3 Operating ranges

Table 10 provides the operating ranges of the i.MX 6UltraLite processors. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

Table 10. Operating Ranges

Parameter Description	Symbol	Operating Conditions	Min	Typ	Max[1]	Unit	Comment
Run Mode: LDO Enabled	VDD_SOC_IN	—	1.375	—	1.5	V	VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point (VDD_ARM_CAP and VDD_SOC_CAP) for correct supply voltage regulation.
	VDD_ARM_CAP	A7 core at 696 MHz	1.25	—	1.3	V	Output voltage must be set to the following rules: • VDD_ARM_CAP <= VDD_SOC_CAP • VDD_SOC_CAP - VDD_ARM_CAP < 330 mV
		A7 core at 528 MHz	1.15	—	1.3		
		A7 core at 396 MHz	1.00	—	1.3		
		A7 core at 198 MHz	0.925	—	1.3		
	VDD_SOC_CAP	—	1.15	—	1.3	V	—
Run Mode: LDO Bypassed	VDD_SOC_IN	A7 core operation at 528 MHz or below	1.15	—	1.3	V	A7 core operation above 528 MHz is not supported when LDO is bypassed.
SUSPEND (DSM) Mode	VDD_SOC_IN	—	0.90	—	1.3	V	Refer to Table 14 Low Power Mode Current and Power Consumption on page 14
VDD_HIGH internal Regulator	VDD_HIGH_IN[2]	—	2.80	—	3.6	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[3]	—	2.40	—	3.6	V	Can be combined with VDDHIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS	—	4.40	—	5.5	V	—
	USB_OTG2_VBUS	—	4.40	—	5.5	V	—
DDR I/O supply	NVCC_DRAM	LPDDR2	1.14	1.2	1.3	V	—
		DDR3L	1.28	1.35	1.45	V	—
		DDR3	1.43	1.5	1.575	V	—
	NVCC_DRAM2P5	—	2.25	2.5	2.75	V	—

Table 10. Operating Ranges (continued)

GPIO supplies	NVCC_CSI NVCC_ENET NVCC_GPIO NVCC_UART NVCC_LCD NVCC_NAND NVCC_SD1	—	1.65	1.8, 2.8, 3.3	3.6	V	All digital I/O supplies (NVCC_xxxx) must be powered (unless otherwise specified in this data sheet) under normal conditions whether the associated I/O pins are in use or not.
A/D converter	VDDA_ADC_3P3	—	3.0	3.15	3.6	V	VDDA_ADC_3P3 must be powered when chip is in RUN mode, IDLE mode, or SUSPEND mode. VDDA_ADC_3P3 should not be powered when chip is in SNVS mode.
Temperature Operating Ranges							
Junction temperature	TJ	Automotive	-40		125	°C	See the application note, i.MX 6UltraLite Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This result in an optimized power/speed ratio.

2 In setting VDD_HIGH_IN voltage, refer to the Errata ERR010690 (SNVS_LP Registers Reset Issue).

3 In setting VDD_SNVS_IN voltage with regards to Charging Currents and RTC, refer to the *i.MX 6UltraLite Hardware Development Guide* (IMX6ULHDG).

Table 11 shows on-chip LDO regulators that can supply on-chip loads.

Table 11. On-Chip LDOs[1] and their On-Chip Loads

Voltage Source	Load	Comment
VDD_HIGH_CAP	NVCC_DRAM_2P5	Board-level connection to VDD_HIGH_CAP

1 On-chip LDOs are designed to supply i.MX6UltraLite loads and must not be used to supply external loads.

4.1.4 External clock sources

Each i.MX 6UltraLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 12 shows the interface frequency requirements.

Table 12. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 12 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum supply currents

The data shown in Table 13 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

See the i.MX 6UltraLite Power Consumption Measurement Application Note (AN5170) for more details on typical power consumption under various use case definitions.

Table 13. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_SOC_IN	696 MHz ARM clock based on Dhrystone test	600	mA
VDD_SOC_IN	528 MHz ARM clock based on Dhrystone test	500	mA
VDD_HIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	500[2]	μA
USB_OTG1_VBUS USB_OTG2_VBUS	—	50[3]	mA
VDDA_ADC_3P3	100 Ohm maximum loading for touch panel	35	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	(See[4])	—
NVCC_DRAM_2P5	—	50	mA
NVCC_GPIO	N=16	Use maximum IO Equation[5]	—
NVCC_UART	N=16	Use maximum IO equation[5]	—
NVCC_ENET	N=16	Use maximum IO equation[5]	—
NVCC_LCD	N=29	Use maximum IO equation[5]	—
NVCC_NAND	N=17	Use maximum IO equation[5]	—
NVCC_SD1	N=6	Use maximum IO equation[5]	—
NVCC_CSI	N=12	Use maximum IO equation[5]	—
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the *i.MX 6UltraLite Power Consumption Measurement Application Note* (AN5170) or examples of DRAM power consumption during specific use case scenarios.

[5] General equation for estimated, maximum power consumption of an IO power supply:
Imax = N x C x V x (0.5 x F)
Where:
N—Number of IO pins supplied by the power line
C—Equivalent external capacitive load
V—IO voltage
(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)
In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low power mode supply currents

Table 14 shows the current core consumption (not including I/O) of i.MX 6UltraLite processors in selected low power modes.

Table 14. Low Power Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Units
SYSTEM IDLE: LDO Enabled	• LDO_ARM and LDO_SOC are set to 1.15 V • LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • DDR is in self refresh • 24 MHz XTAL is ON • 528 PLL is active, other PLLS are power down • High-speed peripheral clock gated, but remain powered	VDD_SOC_IN (1.275 V)	7.7	mA
		VDD_HIGH_IN (3.0 V)	10.5	
		VDD_SNVS_IN (3.0 V)	0.06	
		Total	41.5	mW
SYSTEM IDLE: LDO Bypassed	• LDO_ARM and LDO_SOC are set to bypass mode • LDO_2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • CPU in WFI, CPU clock gated • DDR is in self refresh • 24 MHz XTAL is ON • 528 PLL is active, other PLLs are power down • High-speed peripheral clock gated, but remain powered	VDD_SOC_IN (1.15 V)	7.5	mA
		VDD_HIGH_IN (3.0 V)	9.5	
		VDD_SNVS_IN (3.0 V)	0.06	
		Total	37.3	mW
LOW POWER IDLE: LDO Enabled	• LDO_SOC is set to 1.15 V, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are set to weak mode • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • High-speed peripheral are powered off	VDD_SOC_IN (1.275 V)	3.2	mA
		VDD_HIGH_IN (3.0 V)	1.5	
		VDD_SNVS_IN (3.0 V)	0.05	
		Total	8.7	mW
LOW POWER IDLE: LDO Bypassed	• LDO_SOC is in bypass mode, LDO_ARM is in PG mode • LDO-2P5 and LDO_1P1 are set to weak mode • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC used as clock source • High-speed peripheral are powered off	VDD_SOC_IN (1.15 V)	2.8	mA
		VDD_HIGH_IN (3.0 V)	0.4	
		VDD_SNVS_IN (3.0 V)	0.05	
		Total	4.57	mW

Table 14. Low Power Mode Current and Power Consumption (continued)

SUSPEND (DSM)	• LDO_SOC is in bypass mode, LDO_ARM is in PG mode • LDO_2P5 and LDO_1P1 are shut off • CPU in power gate mode • DDR is in self refresh • All PLLs are power down • 24 MHz XTAL is off, 24 MHz RCOSC is off • All clocks are shut off, except 32 kHz RTC • High-speed peripheral are powered off	VDD_SOC_IN (0.9 V)	0.44	mA
		VDD_HIGH_IN (3.0 V)	0.03	
		VDD_SNVS_IN (3.0 V)	0.03	
		Total	0.58	mW
SNVS (RTC)	• All SOC digital logic, analog module are shut off • 32 kHz RTC is alive • Tamper detection circuit remains active	VDD_SOC_IN (0 V)	0	mA
		VDD_HIGH_IN (0 V)	0	
		VDD_SNVS_IN (3.0 V)	0.02	
		Total	0.06	mW

[1] Typical process material in fab

4.1.7 USB PHY current consumption

4.1.7.1 Power down mode

In power down mode, everything is powered down, including the USB VBUS valid detectors in typical condition. Table 15 shows the USB interface current consumption in power down mode.

Table 15. USB PHY Current Consumption in Power Down Mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL (1.1 V)
Current	5.1 μA	1.7 μA	< 0.5 μA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- VDD_HIGH_IN should be turned on before VDD_SOC_IN.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS and USB_OTG2_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

CAUTION

For power sequence control on VDD_HIGH_IN and VDD_SOC_IN, refer to the ERR010690 (SNVS_LP Registers Reset Issue).

4.2.3 Power supplies usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package information and contact assignments".”

4.3 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO operation only.

4.3.1 Digital regulators (LDO_ARM, LDO_SOC)

There are two digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on-die trimming. This translates into more stable voltage for the on-chip logics.

These regulators have two basic modes:

- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2 Regulators for analog modules

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 10 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the USB Phy, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 10 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the DDR IOs, USB Phy, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB VUSB voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB VBUS supply, when both are present. If only one of the USB VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.4 PLL’s electrical characteristics

4.4.1 Audio/Video PLL’s electrical parameters

Table 16. Audio/Video PLL’s Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 17. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 18. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 19. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 ARM PLL

Table 20. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	648 MHz ~ 1296 MHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement an oscillator. The oscillator is powered from NVCC_PLL.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implement a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the backup battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from the VDD_HIGH_IN/VDD_SNVS_IN. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k.

Table 21. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Fosc	—	32.768 KHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 μA	—	The 4 μA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 μA when ring oscillator is inactive, 20 μA when the ring oscillator is running. Another 1.5 μA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 μA on vdd_rtc when the ring oscillator is not running.
Bias resistor	—	14 MΩ	—	This integrated bias resistor sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.

Table 21. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- XTALI and RTC_XTALI (Clock Inputs) DC Parameters
- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O DC Parameters

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

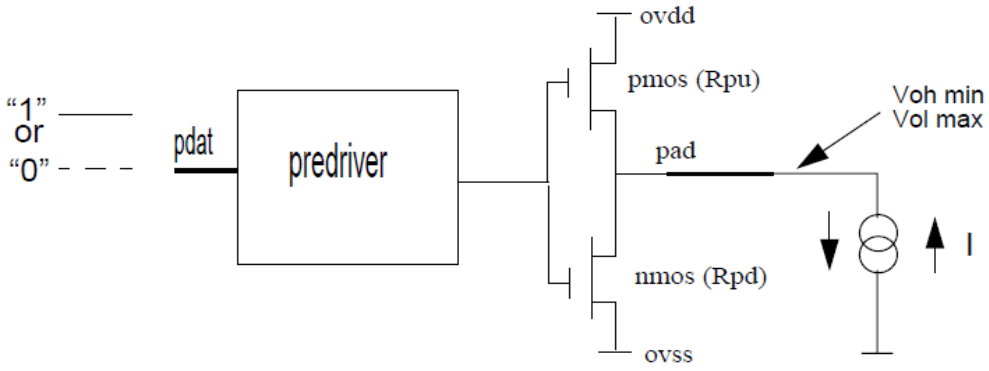


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC parameters

Table 22 shows the DC parameters for the clock inputs.

Table 22. XTALI and RTC_XTALI DC Parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL	NVCC_PLL	V
XTALI low-level DC input voltage	Vil	—	0	0.2	V

Table 22. XTALI and RTC_XTALI DC Parameters[1] (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
RTC_XTALI high-level DC input voltage	Vih	—	0.8	1.1	V
RTC_XTALI low-level DC input voltage	Vil	—	0	0.2	V

1 The DC parameters are for external clock input only.

4.6.2 Single voltage General Purpose I/O (GPIO) DC parameters

Table 23 shows DC parameters for GPIO pads. The parameters in Table 23 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 23. Single Voltage GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Ioh= -0.1mA (ipp_dse=001,010) Ioh= -1mA (ipp_dse=011,100,101,110,111)	OVDD-0.15	–	V
Low-level output voltage[1]	VOL	Iol= 0.1mA (ipp_dse=001,010) Iol= 1mA (ipp_dse=011,100,101,110,111)	–	0.15	V
High-Level input voltage[1,2]	VIH	—	0.7*OVDD	OVDD	V
Low-Level input voltage[1,2]	VIL	—	0	0.3*OVDD	V
Input Hysteresis (OVDD= 1.8V)	VHYS_LowVDD	OVDD=1.8V	250	—	mV
Input Hysteresis (OVDD=3.3V)	VHYS_HighVDD	OVDD=3.3V	250	—	mV
Schmitt trigger VT+[2,3]	VTH+	—	0.5*OVDD	—	mV
Schmitt trigger VT-[2,3]	VTH-	—	—	0.5*OVDD	mV
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=0V	—	212	μA
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=OVDD	—	1	μA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=0V	—	100	μA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=OVDD	—	1	μA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=0V	—	48	μA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=OVDD	—	1	μA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=OVDD	—	48	μA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=0V	—	1	μA
Input current (no PU/PD)	IIN	VI = 0, VI = OVDD	-1	1	μA
Keeper Circuit Resistance	R_Keeper	VI =0.3*OVDD, VI = 0.7* OVDD	105	175	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes. For details on supported DDR memory configurations, see Section 4.10, "Multi-Mode DDR Controller (MMDC)".

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6UltraLite Applications Processor* (IMX6ULHDG).

4.6.3.1 LPDDR2 mode I/O DC parameters

Table 24. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA	0.9*OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1mA	—	0.1*OVDD	V
Input Reference Voltage	Vref	—	0.49*OVDD	0.51*OVDD	V
DC High-Level input voltage	Vih_DC	—	Vref+0.13	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.13	V
Differential Input Logic High	Vih_diff	—	0.26	Note[2]	—
Differential Input Logic Low	Vil_diff	—	Note[2]	-0.26	—
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-15	15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	110	175	kΩ
Input current (no pull-up/down)	Iin	VI = 0, VI = OVDD	-2.5	2.5	μA

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3.2 DDR3/DDR3L mode I/O DC parameters

The parameters in Table 26 are guaranteed per the operating ranges in Table 10, unless otherwise noted.

Table 26. DDR3/DDR3L I/O DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA Voh (for ipp_dse=001)	0.8*OVDD[1]	—	V
Low-level output voltage	VOL	Iol= 0.1mA Vol (for ipp_dse=001)	0.2*OVDD	—	V

Table 26. DDR3/DDR3L I/O DC Electrical Characteristics (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -1mA Voh (for all except ipp_dse=001)	0.8*OVDD	—	V
Low-level output voltage	VOL	Iol= 1mA Vol (for all except ipp_dse=001)	0.2*OVDD	—	V
Input Reference Voltage	Vref	—	0.49*ovdd	0.51*ovdd	V
DC High-Level input voltage	Vih_DC	—	Vref[2]+0.1	OVDD	V
DC Low-Level input voltage	Vil_DC	—	OVSS	Vref-0.1	V
Differential Input Logic High	Vih_diff	—	0.2	—	V
Differential Input Logic Low	Vil_diff	—	—	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper Circuit Resistance	Rkeep	—	105	165	kΩ
Input current (no pull-up/down)	Iin	VI = 0,VI = OVDD	-2.9	2.9	μA

1 OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

2 Vref – DDR3/DDR3L external reference voltage

4.6.4 LVDS I/O DC parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 27 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 27. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.7 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

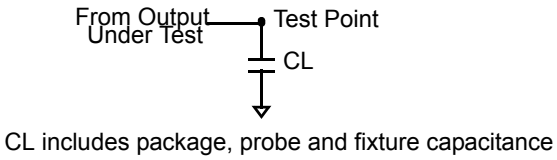


Figure 4. Load Circuit for Output

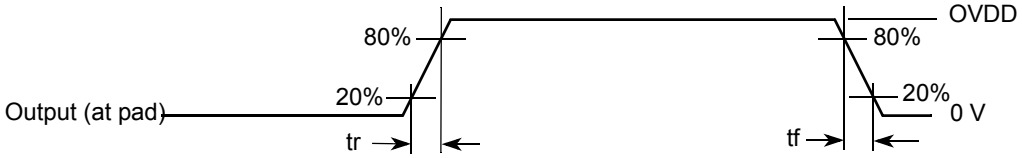


Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 28 and Table 29, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 28. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 29. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC parameters

The Multi-mode DDR Controller (MMDC) is compatible with JEDEC-compliant SDRAMs. For details on supported DDR memory configurations, see Section 4.10, “Multi-Mode DDR Controller (MMDC)".

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6UltraLite Applications Processor* (IMX6ULHDG).

Table 30 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 30. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	V
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	0.3	V-ns

Table 30. DDR I/O LPDDR2 Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω ± 30%	1.5	3.5	V/ns
		50 Ω to Vref. 5pF load.Drive impedance = 60 Ω ± 30%	1	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr - Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 31 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 31. DDR I/O DDR3/DDR3L Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref - 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref - 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3D specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) - Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 x OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.8 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 6UltraLite processors for the following I/O types:

- Single Voltage General Purpose I/O (GPIO)

- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).

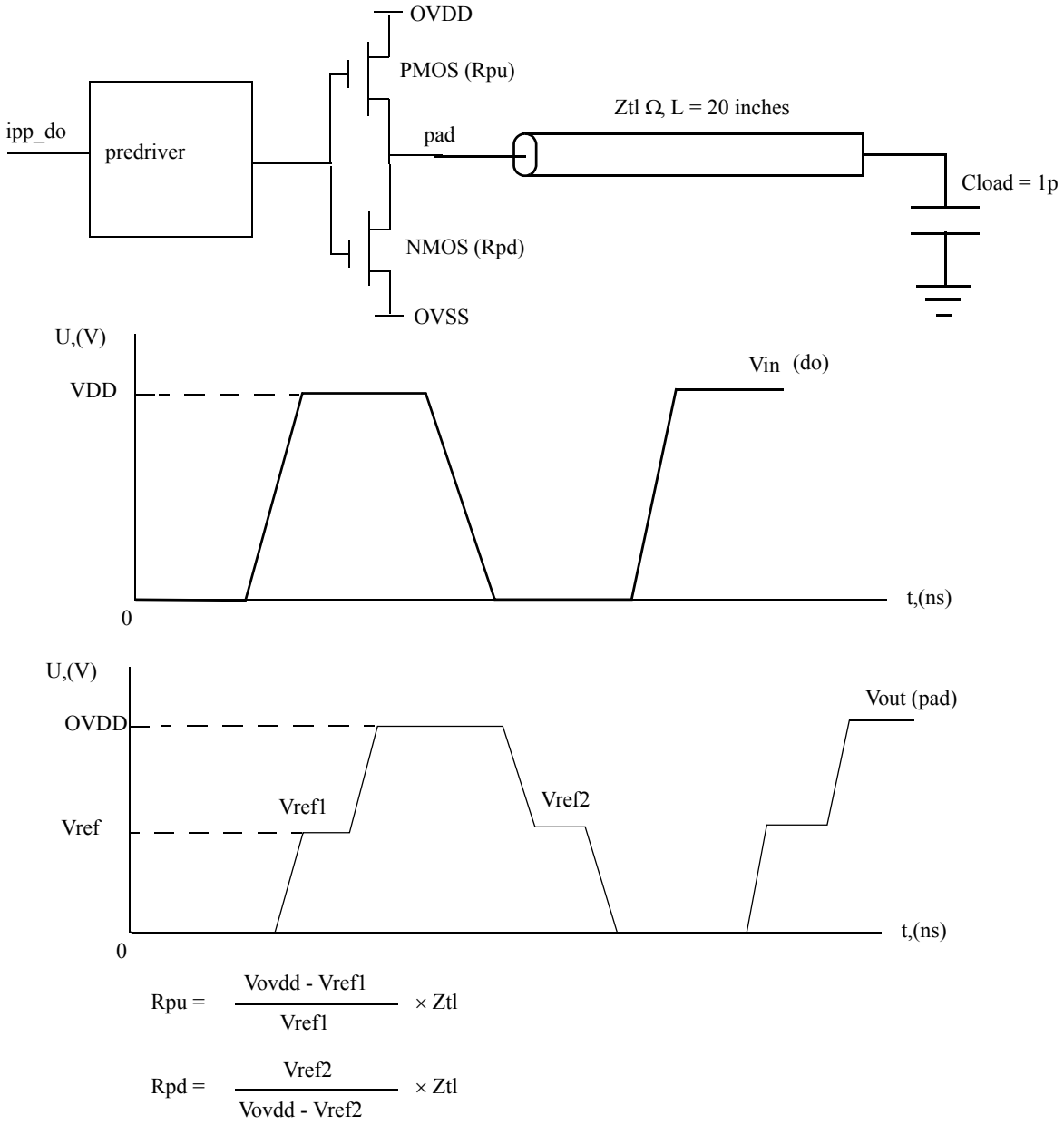


Figure 6. Impedance Matching Load for Measurement

4.8.1 Single voltage GPIO output buffer impedance

Table 32 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 32. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 88 65 52 43 37	Ω

Table 33 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 33. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	157 78 53 39 32 26 23	Ω

4.8.2 DDR I/O output buffer impedance

Table 34 shows DDR I/O output buffer impedance of i.MX 6UltraLite processors.

Table 34. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.
4. It is recommended to use a strong driver strength (<= 48 Ω) for all DDR pads and all DDR type (DDR3/DDR3L/LPDDR2).

4.9 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 6UltraLite processor.

4.9.1 Reset timings parameters

Figure 7 shows the reset timing and Table 35 lists the timing parameters.

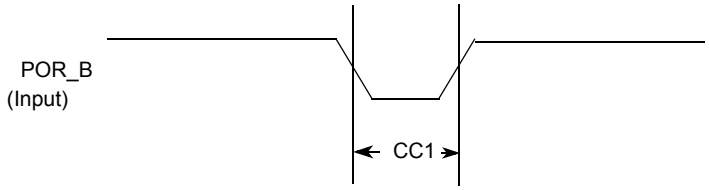


Figure 7. Reset Timing Diagram

Table 35. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

4.9.2 WDOG reset timing parameters

Figure 8 shows the WDOG reset timing and Table 36 lists the timing parameters.

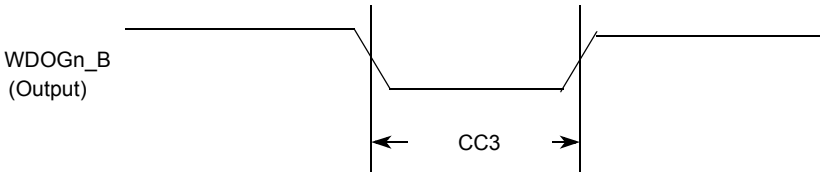


Figure 8. WDOGn_B Timing Diagram

Table 36. WDOGn_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOGn_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Timing parameters in this section that are given as a function of register settings or clock periods are valid for the entire range of allowed frequencies (0–104 MHz).

4.9.3.1 EIM interface pads allocation

EIM supports 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 37 provides EIM interface pads allocation in different modes.

Table 37. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode						Multiplexed Address/Data mode
	8 Bit				16 Bit		16 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 1, DSZ = 001
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]	EIM_ADDR [26:16]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	Reserved	Reserved	EIM_DATA [07:00]	Reserved	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	Reserved	Reserved	EIM_DATA [15:08]	Reserved	EIM_AD [15:08]

[1] For more information on configuration ports mentioned in this table, see the *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

General EIM Timing-Synchronous Mode

Figure 9, Figure 10, and Table 38 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

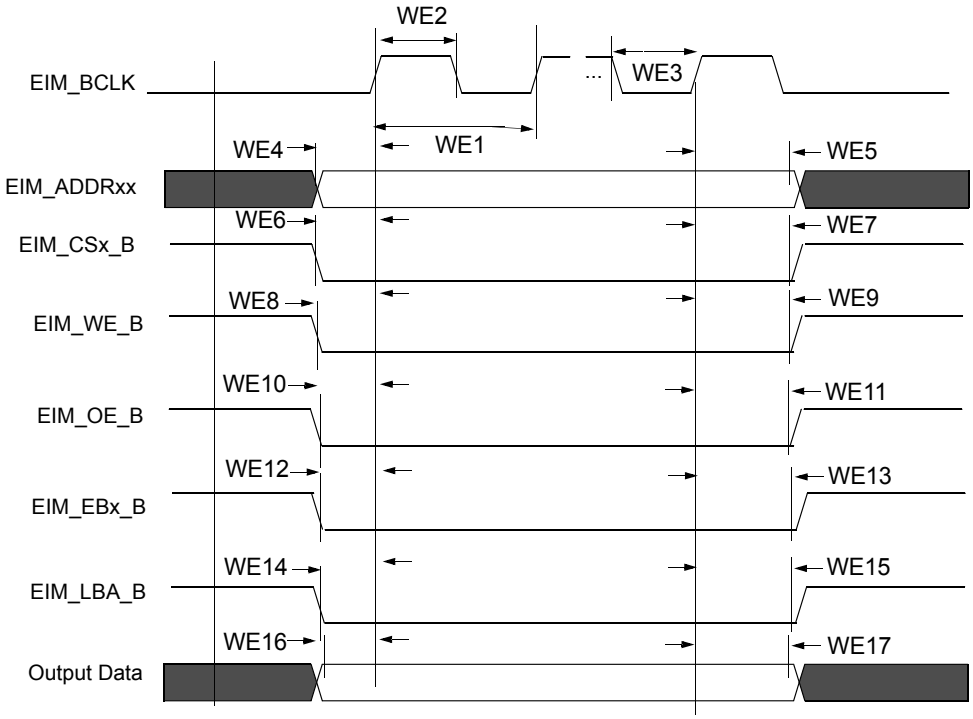


Figure 9. EIM Outputs Timing Diagram

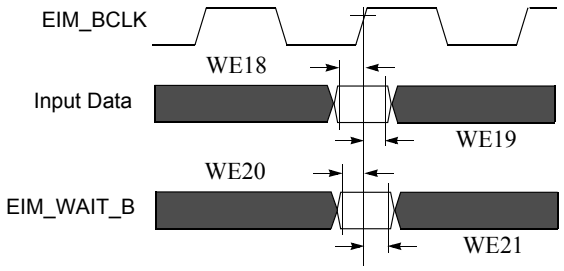


Figure 10. EIM Inputs Timing Diagram

4.9.3.2 Examples of EIM synchronous accesses

Table 38. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK Cycle time[2]	t x (k + 1)	—	ns
WE2	EIM_BCLK Low Level Width	0.4 x t x (k + 1)	—	ns
WE3	EIM_BCLK High Level Width	0.4 x t x (k + 1)	—	ns
WE4	Clock rise to address valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns

Table 38. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE5	Clock rise to address invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE9	Clock rise to EIM_WE_B Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE11	Clock rise to EIM_OE_B Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE13	Clock rise to EIM_EBx_B Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE15	Clock rise to EIM_LBA_B Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE16	Clock rise to Output Data Valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE17	Clock rise to Output Data Invalid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns
WE18	Input Data setup time to Clock rise	2.3	—	ns
WE19	Input Data hold time from Clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to Clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from Clock rise	2	—	ns

1 k represents register setting BCD value.

2 t is clock period (1/Freq.) For 104 MHz, t = 9.165 ns.

Figure 11 to Figure 14 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

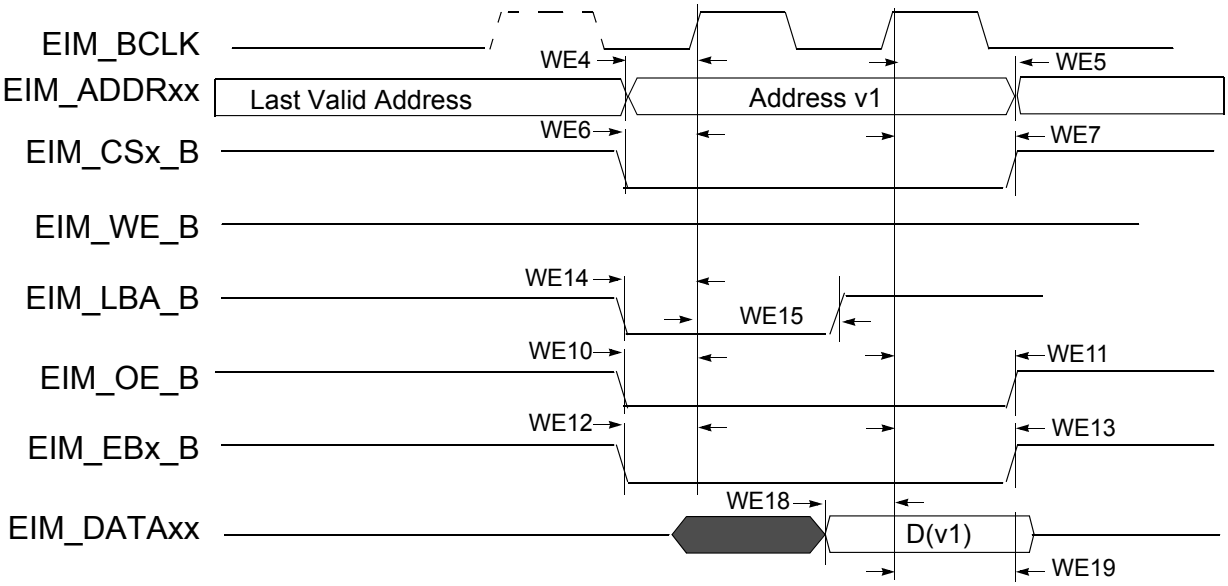


Figure 11. Synchronous Memory Read Access, WSC=1

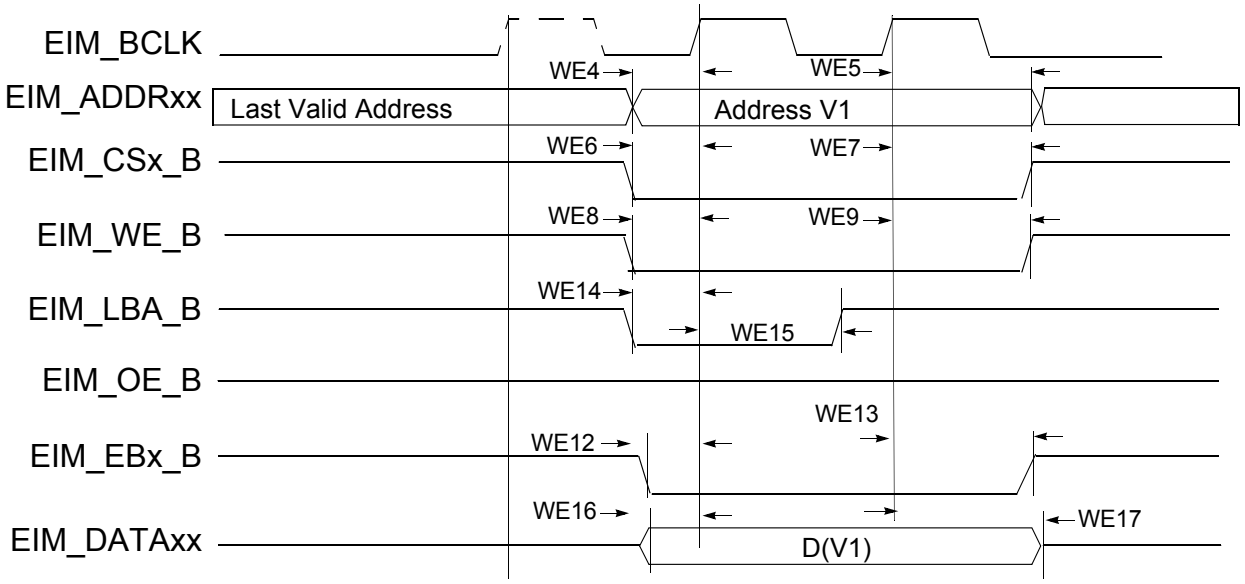


Figure 12. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

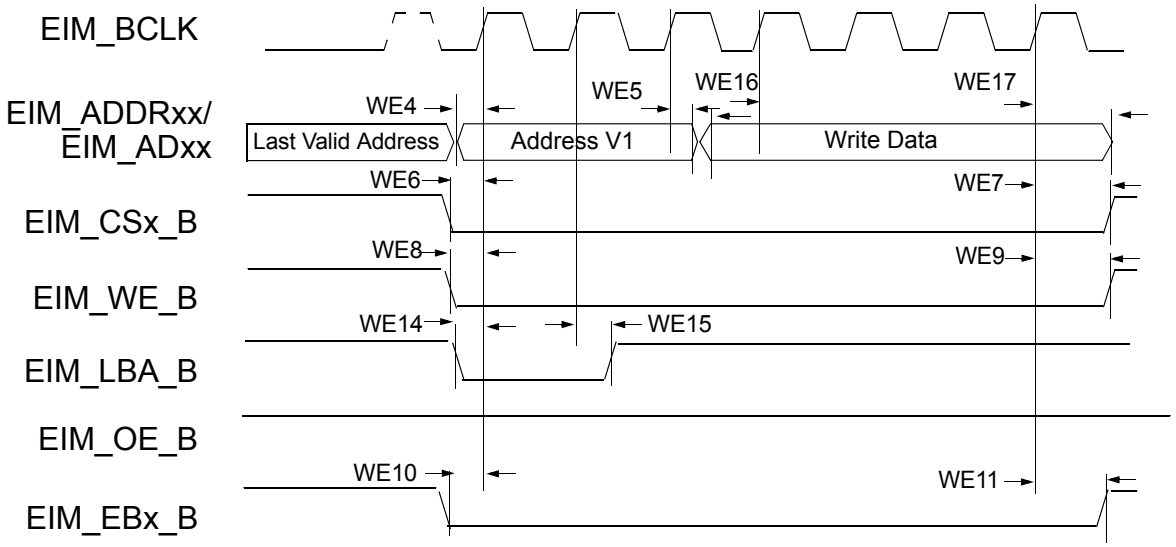


Figure 13. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

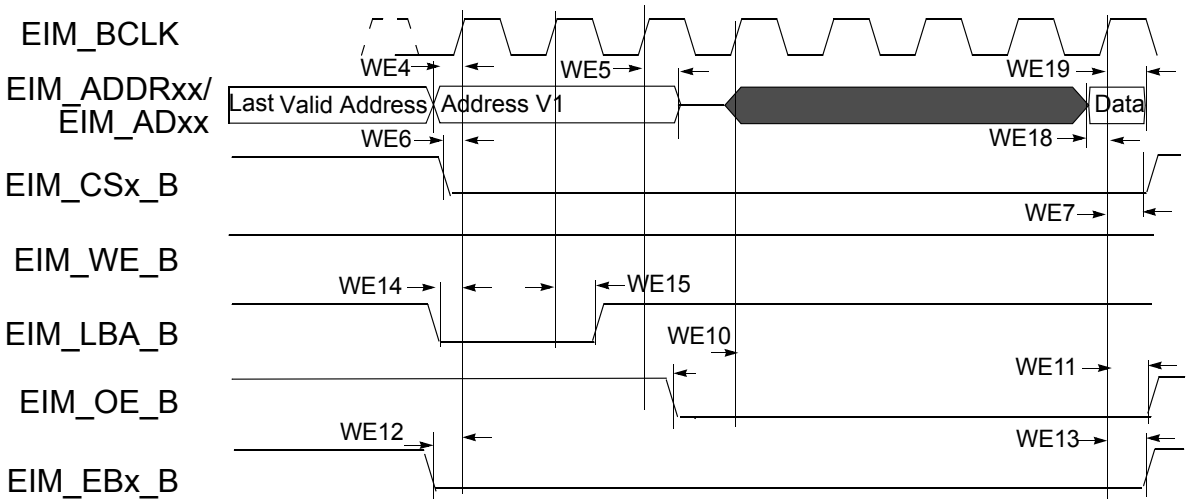


Figure 14. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.3 General EIM timing-asynchronous mode

Figure 15 through Figure 19, and Table 39 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 15 through Figure 18 as RWSC, OEN and CSN is configured differently. See the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for the EIM programming model.

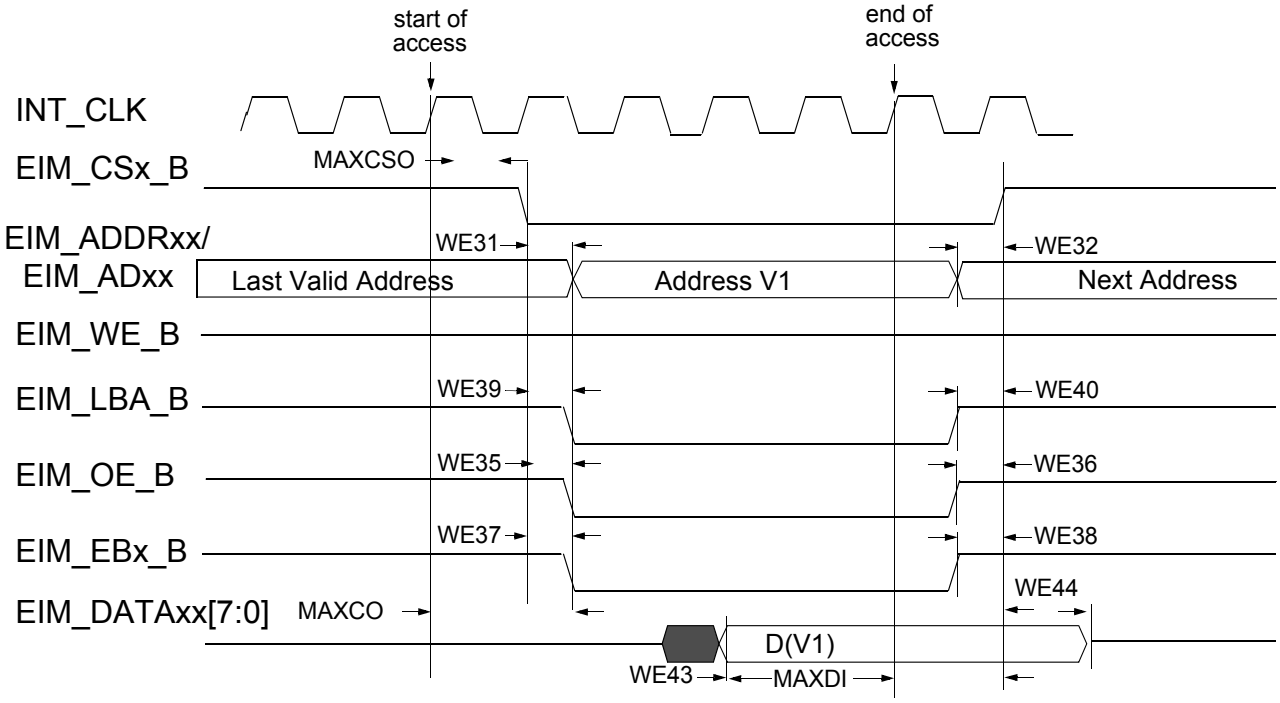


Figure 15. Asynchronous Memory Read Access (RWSC = 5)

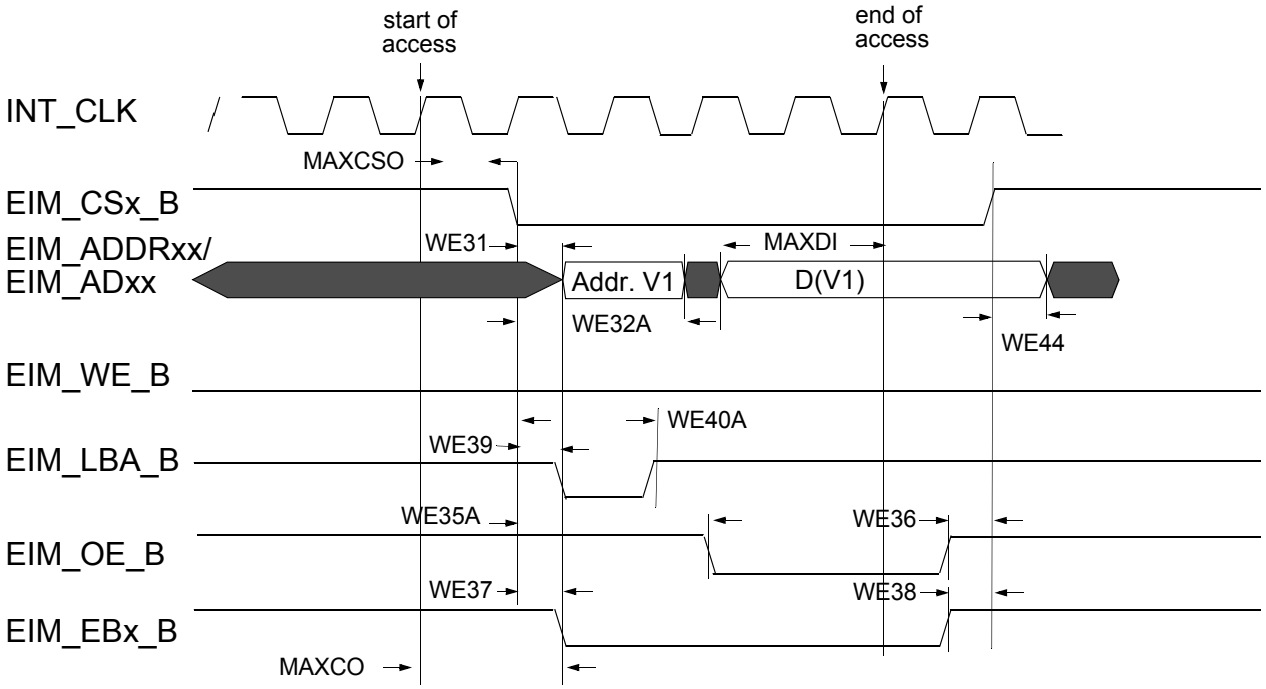


Figure 16. Asynchronous A/D Muxed Read Access (RWSC = 5)

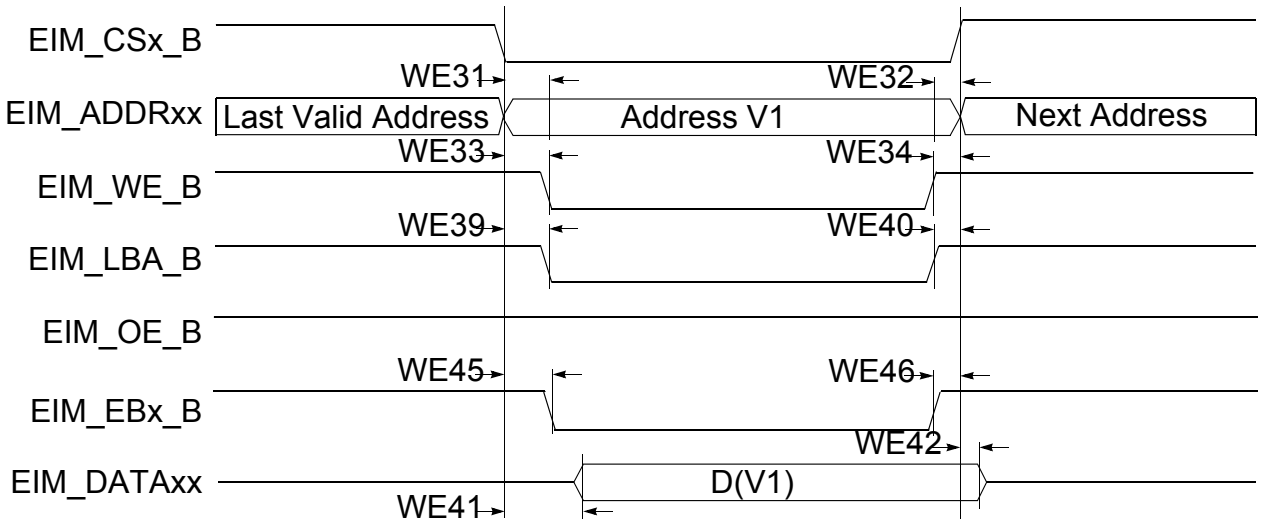


Figure 17. Asynchronous Memory Write Access

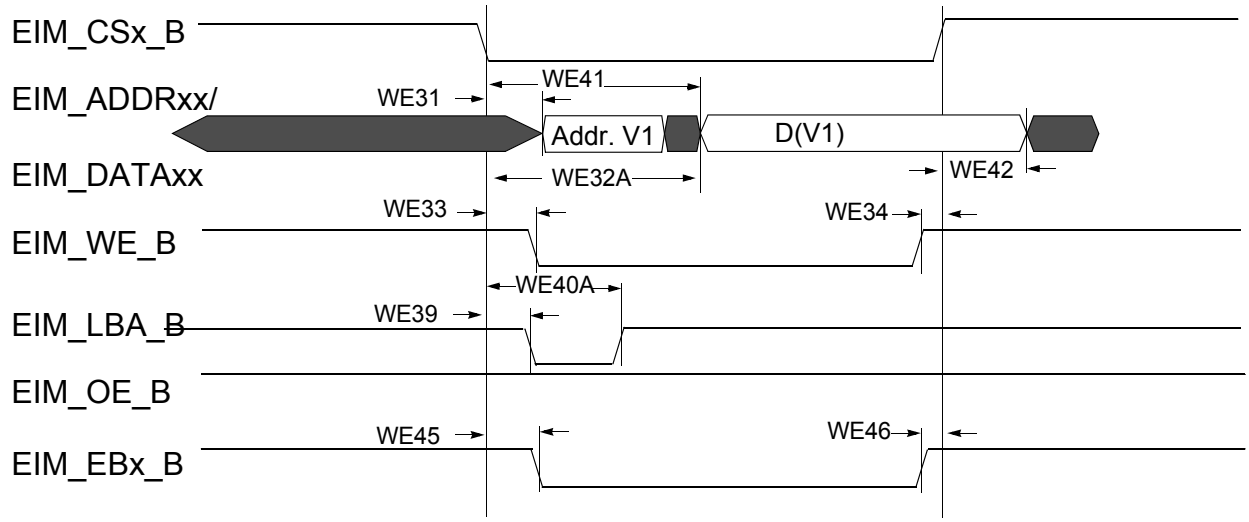


Figure 18. Asynchronous A/D Muxed Write Access

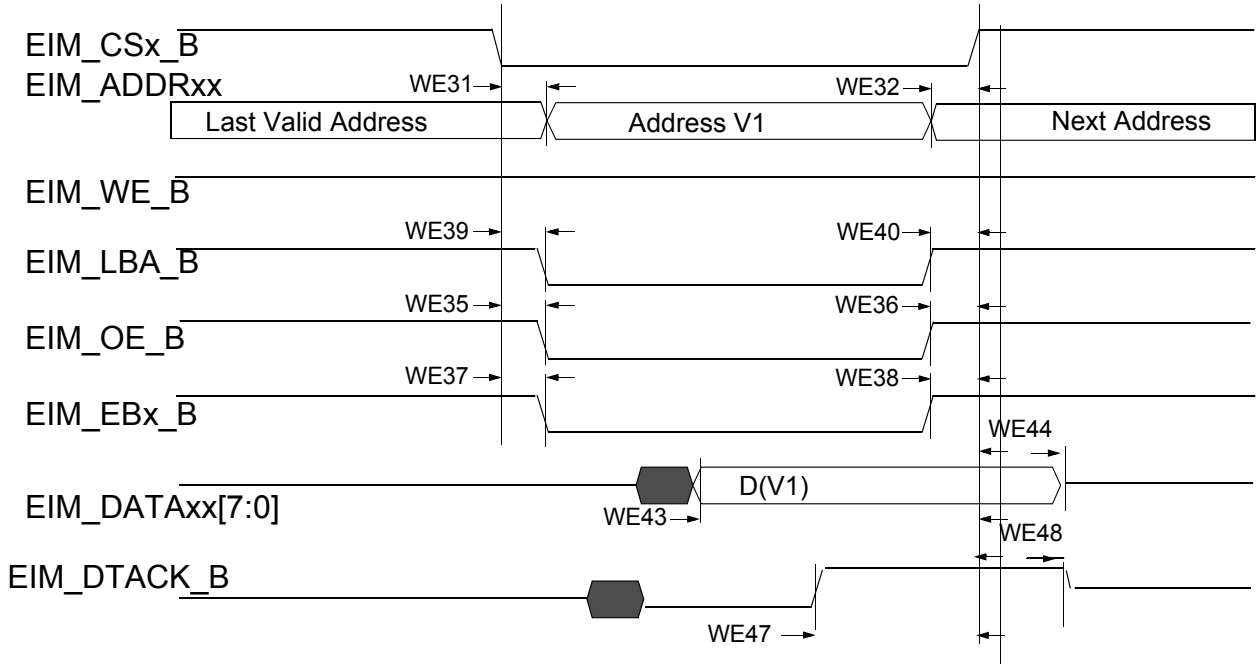


Figure 19. DTACK Mode Read Access (DAP=0)

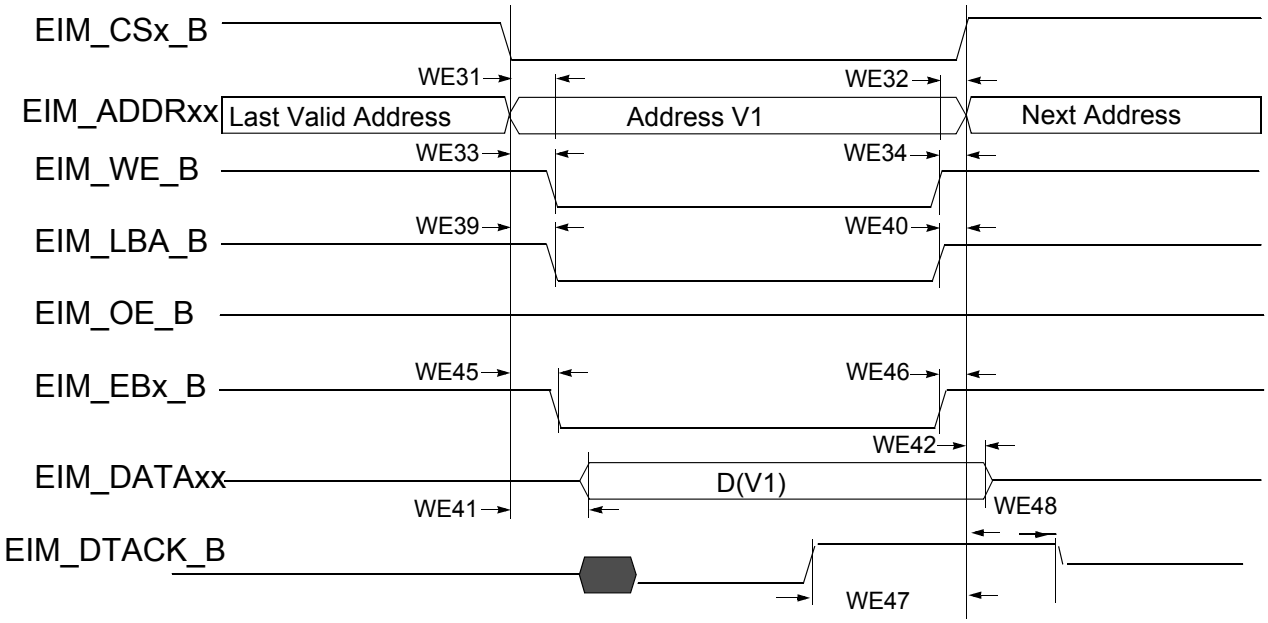


Figure 20. DTACK Mode Write Access (DAP=0)

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4 - WE6 - CSA x t	-3.5 - CSA x t	3.5 - CSA x t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7 - WE5 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
WE32A(muxed A/D	EIM_CSx_B valid to Address Invalid	t + WE4 - WE7 + (ADVN + ADVA + 1 - CSA) x t	t - 3.5 + (ADVN + ADVA + 1 - CSA) x t	t + 3.5 + (ADVN + ADVA + 1 - CSA) x t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8 - WE6 + (WEA - WCSA) x t	-3.5 + (WEA - WCSA) x t	3.5 + (WEA - WCSA) x t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7 - WE9 + (WEN - WCSN) x t	-3.5 + (WEN - WCSN) x t	3.5 + (WEN - WCSN) x t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA - RCSA) x t	-3.5 + (OEA - RCSA) x t	3.5 + (OEA - RCSA) x t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	-3.5 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	3.5 + (OEA + RADVN + RADVA + ADH + 1 - RCSA) x t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7 - WE11 + (OEN - RCSN) x t	-3.5 + (OEN - RCSN) x t	3.5 + (OEN - RCSN) x t	ns

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA) x t	-3.5 + (RBEA - RCSA) x t	3.5 + (RBEA - RCSA) x t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN) x t	-3.5 + (RBEN - RCSN) x t	3.5 + (RBEN- RCSN) x t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14 - WE6 + (ADVA - CSA) x t	-3.5 + (ADVA - CSA) x t	3.5 + (ADVA - CSA) x t	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA) x t	-3.5 + (ADVN + ADVA + 1 - CSA) x t	3.5 + (ADVN + ADVA + 1 - CSA) x t	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA x t	-3.5 - WCSA x t	3.5 - WCSA x t	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA) x t	-3.5 + (WADVN + WADVA + ADH + 1 - WCSA) x t	3.5 + (WADVN + WADVA + ADH + 1 - WCSA) x t	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17 - WE7 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out	10	—	10	ns
MAXDI	EIM_DATAxx maximum delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA) x t	-3.5 + (WBEA - WCSA) x t	3.5 + (WBEA - WCSA) x t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN) x t	-3.5 + (WBEN - WCSN) x t	3.5 + (WBEN - WCSN) x t	ns
MAXDTI	MAXIMUM delay from EIM_DTACK_B to its internal flip-flop + 2 cycles for synchronization	10	—	10	—
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B Invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

2 In this table, CSA means WCSA when write operation or RCSA when read operation

— t means clock period from axi_clk frequency.

—CSA means register setting for WCSA when in write operations or RCSA when in read operations.

—CSN means register setting for WCSN when in write operations or RCSN when in read operations.

—ADVN means register setting for WADVN when in write operations or RADVN when in read operations.

—ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.10 Multi-Mode DDR Controller (MMDC)

The Multi-Mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.10.1 MMDC compatibility with JEDEC-compliant SDRAMs

The i.MX 6UltraLite MMDC supports the following memory types:

- LPDDR2 SDRAM compliant with JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant with JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6UltraLite Applications Processor (IMX6ULHDG)*.

4.10.2 MMDC supported DDR3/DDR3L/LPDDR2 configurations

Table 40 shows the MMDC supported DDR3/DDR3L/LPDDR2 configurations.

Table 40. i.MX 6UltraLite Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	DDR3	DDR3L	LDDDR2
Clock frequency	400 MHz	400 MHz	400 MHz
Bus width	16-bit	16-bit	16-bit
Channel	Single	Single	Single
Chip selects	2	2	2

4.11 General-Purpose Media Interface (GPMI) timing

The i.MX 6UltraLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.11.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 21 through Figure 24 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 41 describes the timing parameters (NF1–NF17) that are shown in the figures.

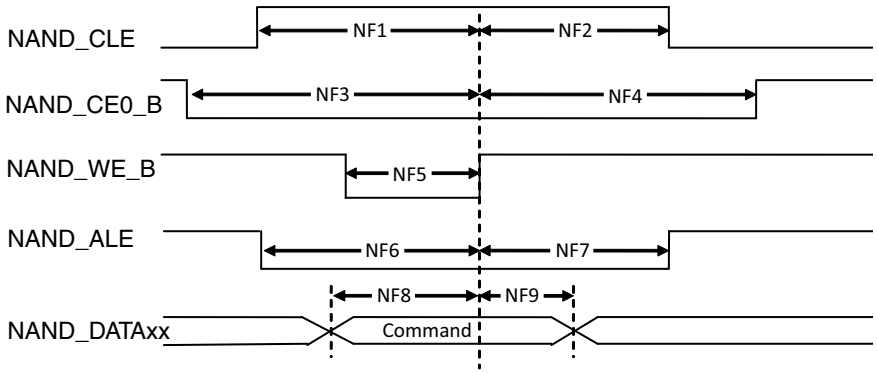


Figure 21. Command Latch Cycle Timing Diagram

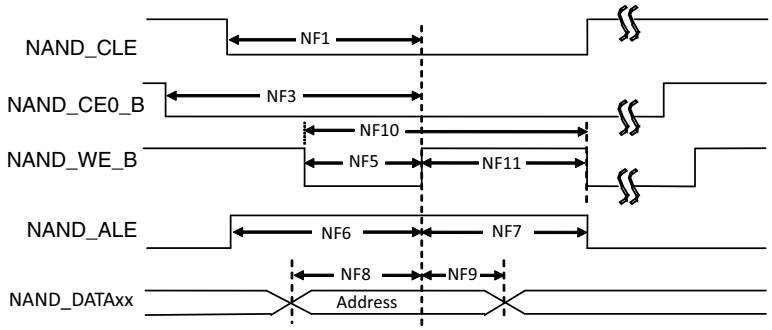


Figure 22. Address Latch Cycle Timing Diagram

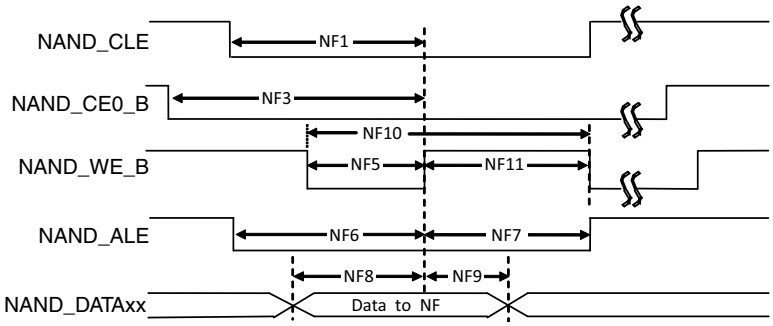


Figure 23. Write Data Latch Cycle Timing Diagram

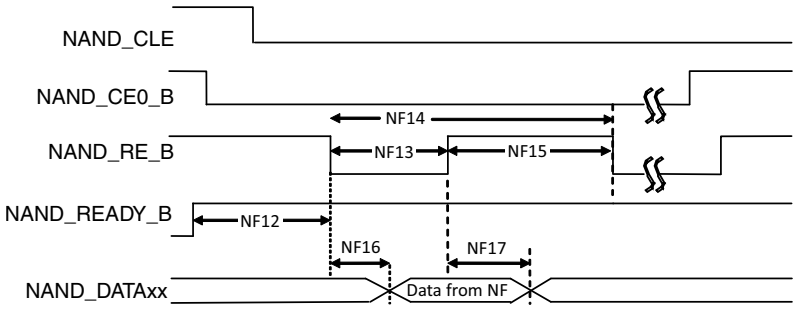


Figure 24. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

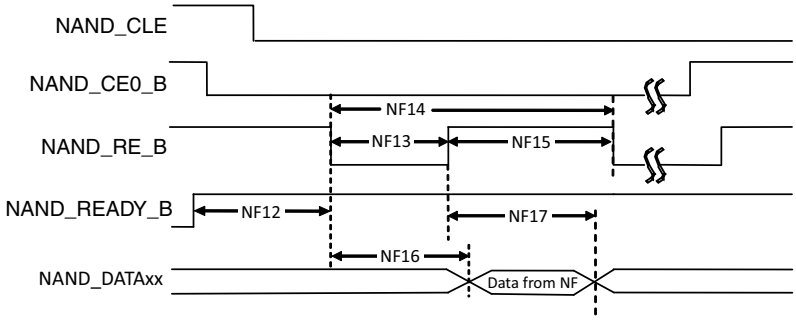


Figure 25. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 41. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		ns
NF3	NAND_CE0_B setup time	tCS	(AS + DS + 1) × T [see 3,2]		ns
NF4	NAND_CE0_B hold time	tCH	(DH+1) × T - 1 [see 2]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see 2]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see 2]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see 2]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see 2]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see 2]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see 3,2]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see 2]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see 2]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see 2]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see 5,6]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see 5,6]	—	ns

1 GPMI's Async Mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is guaranteed by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 24), NF16/NF17 is different from the definition in non-EDO mode (Figure 23). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 6UltraLite Reference Manual*). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.2 Source synchronous mode AC timing (ONFI 2.x compatible)

Figure 26 to Figure 28 show the write and read timing of Source Synchronous Mode.

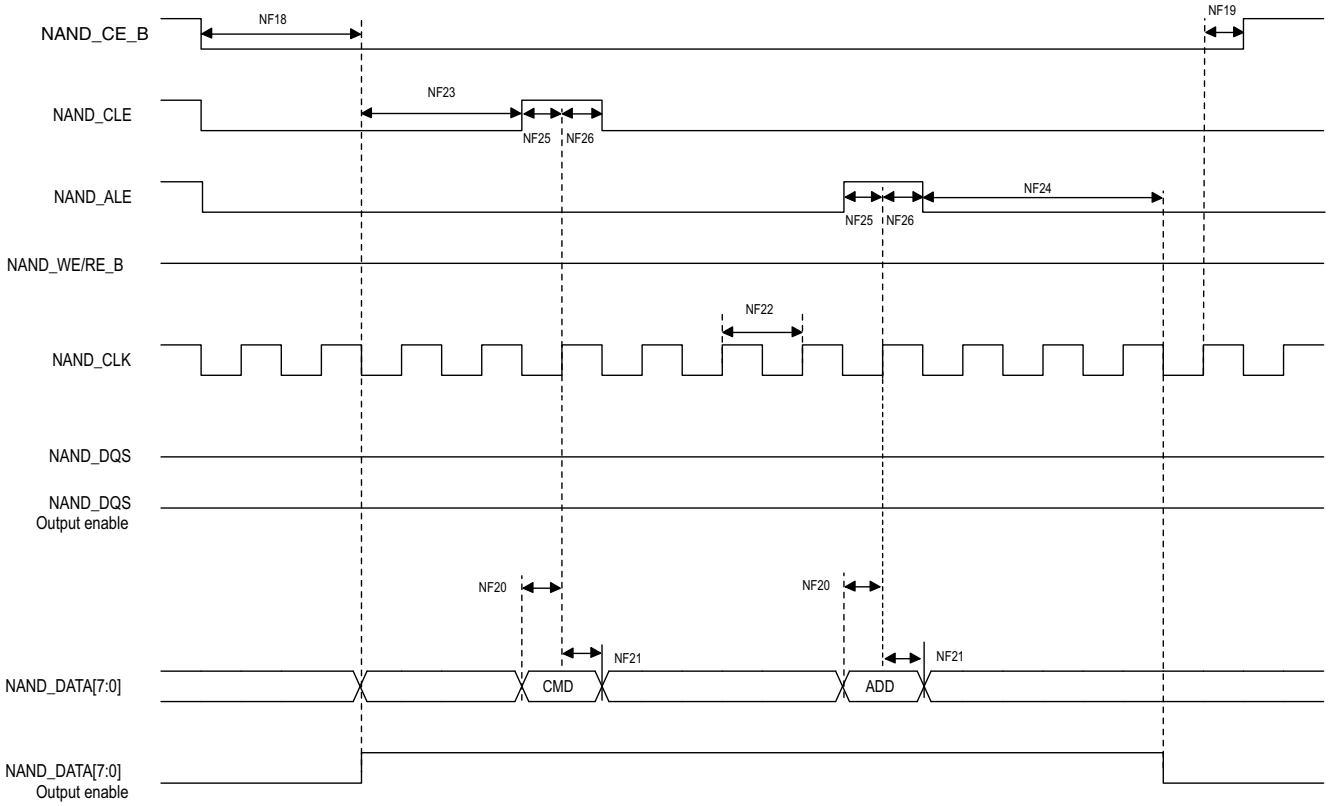


Figure 26. Source Synchronous Mode Command and Address Timing Diagram

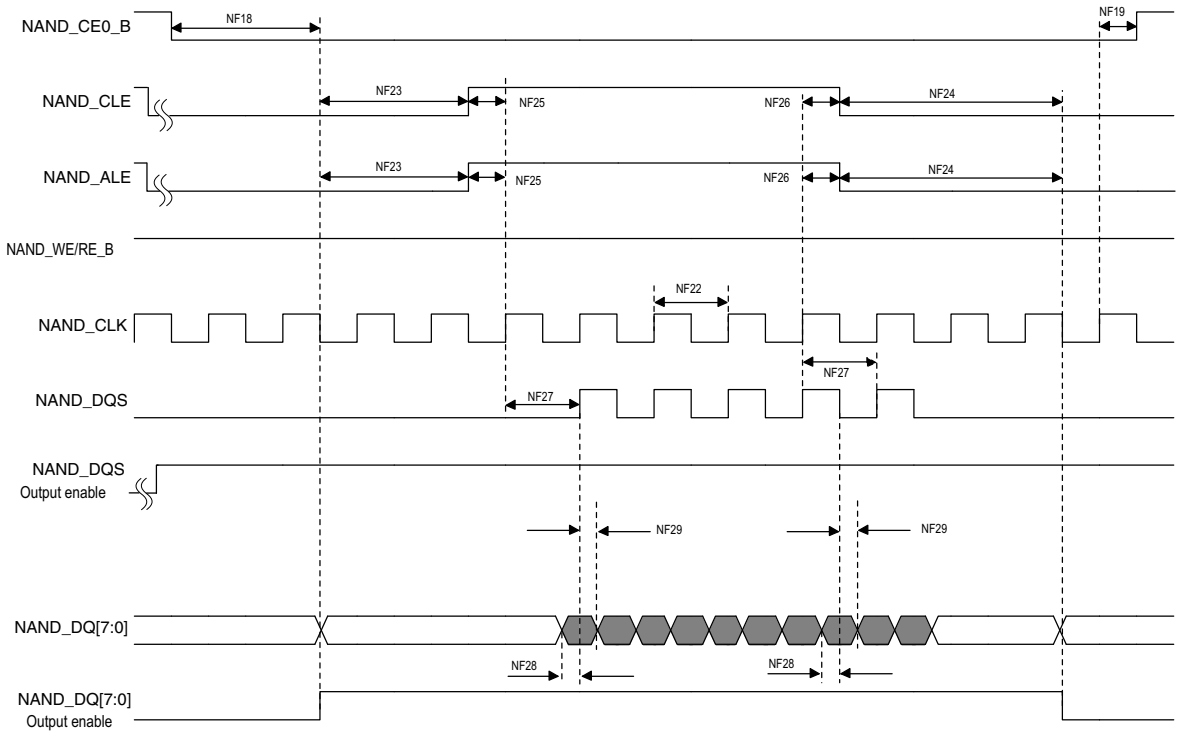


Figure 27. Source Synchronous Mode Data Write Timing Diagram

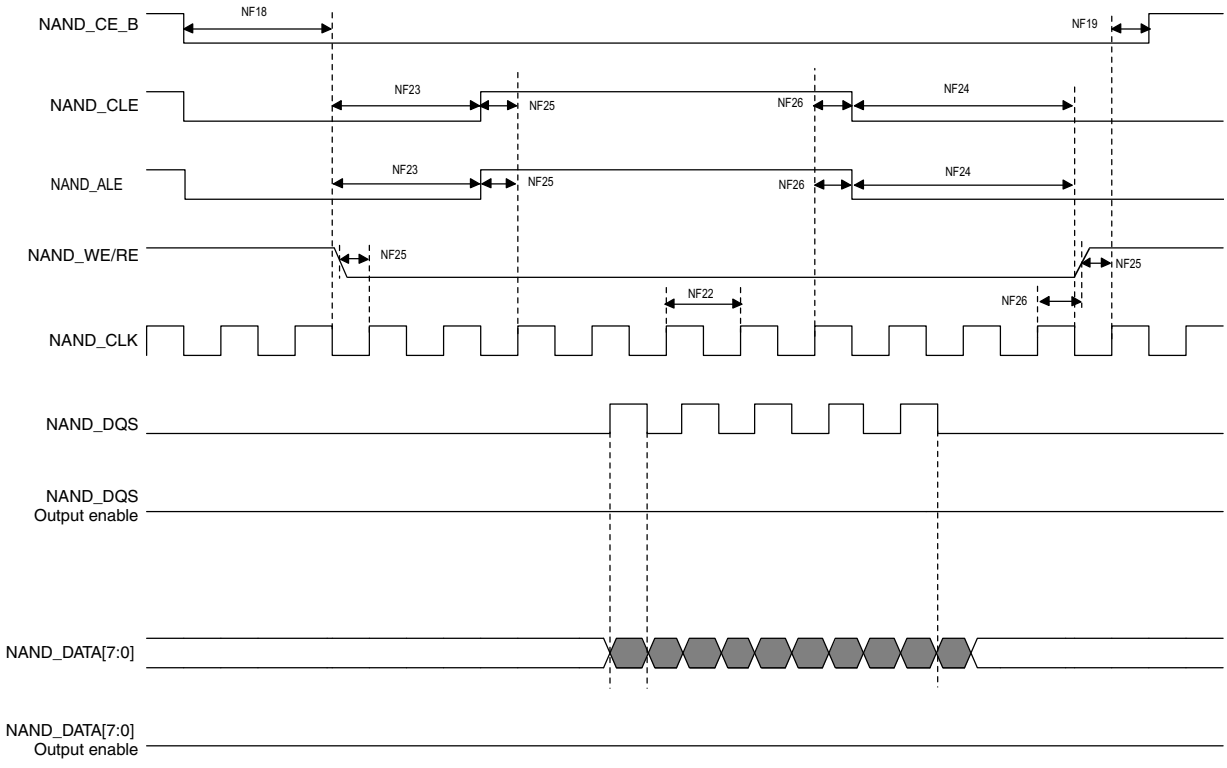


Figure 28. Source Synchronous Mode Data Read Timing Diagram

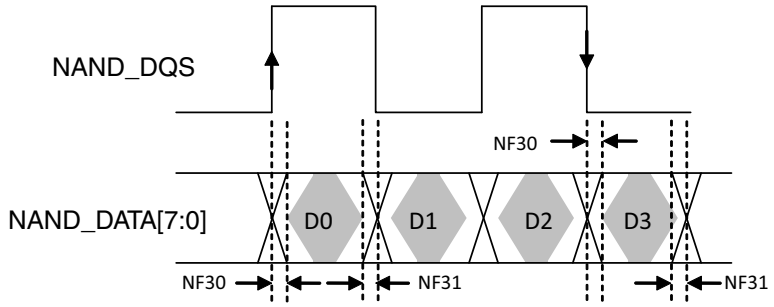


Figure 29. NAND_DQS/NAND_DQ Read Valid Window

Table 42. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	Clock period	tCK	—		ns
NF23	Preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	Postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		—
NF29	Data write hold	—	0.25 × tCK - 0.85		—
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	—

1 GPMI's source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK(GPMI clock period) -0.075ns (half of maximum p-p jitter).

For DDR Source sync mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6UltraLite Reference Manual*). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.3 Samsung toggle mode AC timing

4.11.3.1 Command and address timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.11.1, “Asynchronous mode AC timing (ONFI 1.0 compatible)",” for details.

4.11.3.2 Read and write timing

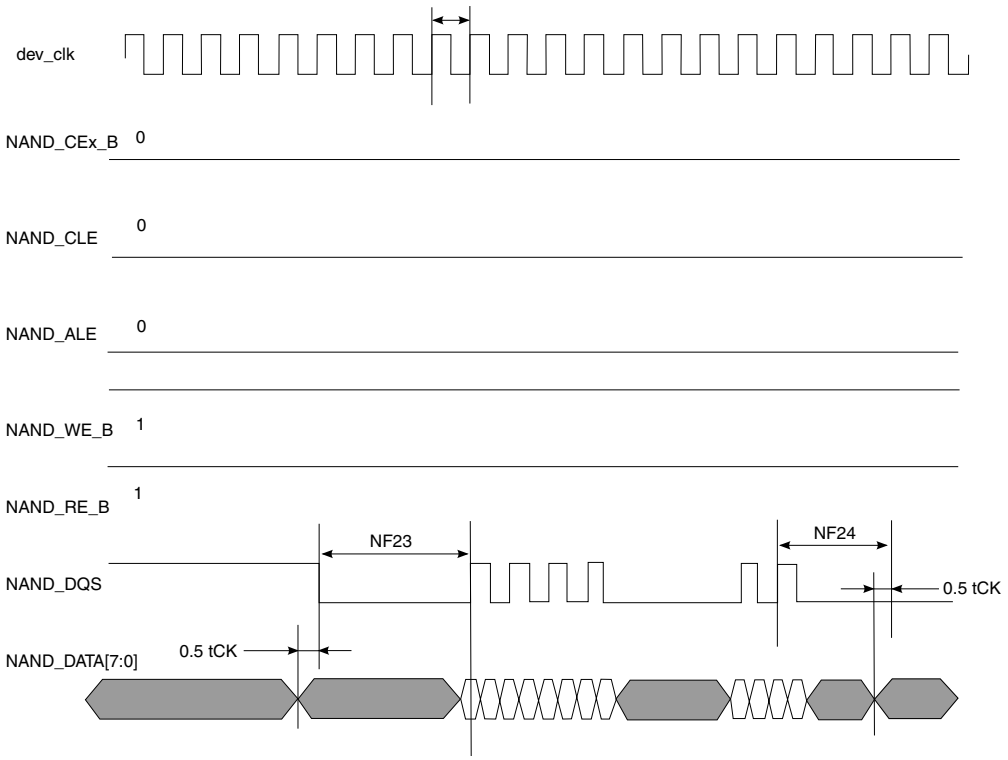


Figure 30. Samsung Toggle Mode Data Write Timing

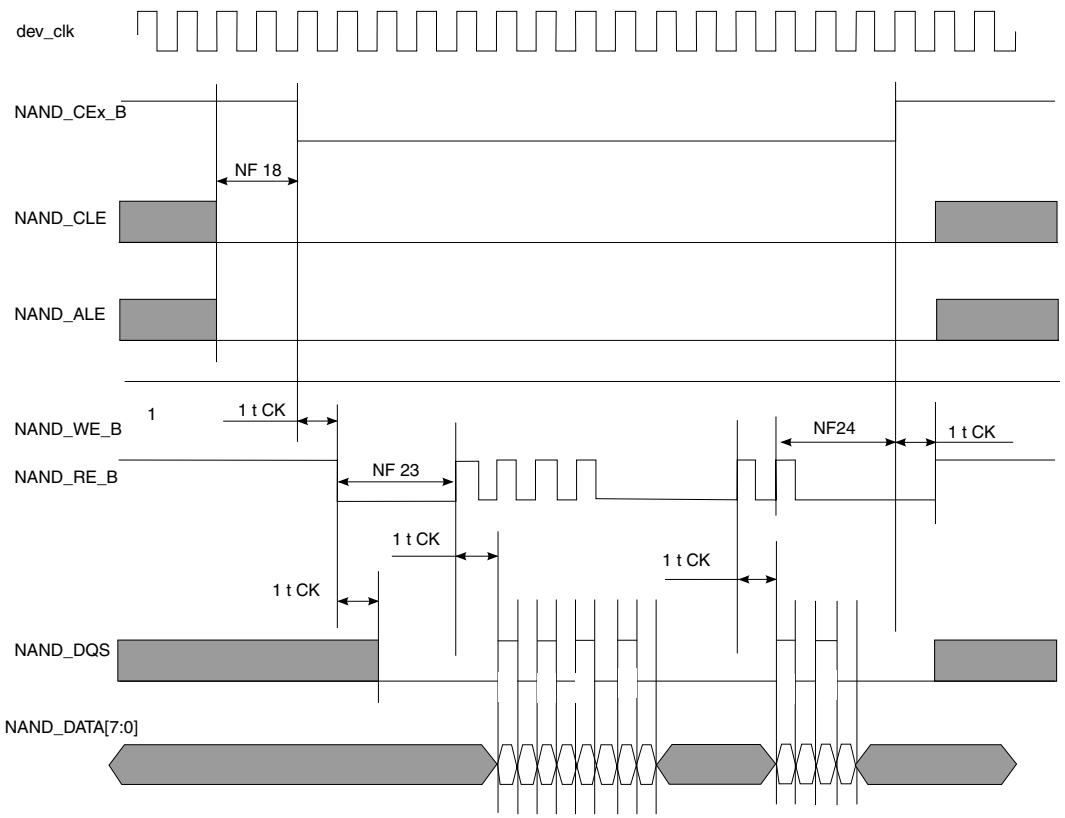


Figure 31. Samsung Toggle Mode Data Read Timing

Table 43. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		—
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see 3,2]		—
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see 2]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see 2]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see 2]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see 2]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see 4,2]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see 5,2]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see 2]	—	ns

Table 43. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	—

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS)

6 Shown in Figure 30.

7 Shown in Figure 31.

For DDR Toggle mode, Figure 29 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 6UltraLite Reference Manual*). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.12 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

4.12.1 CMOS Sensor Interface (CSI) timing parameters

4.12.1.0.1 Gated clock mode timing

Figure 32 and Figure 33 shows the gated clock mode timings for CSI, and Table 44 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

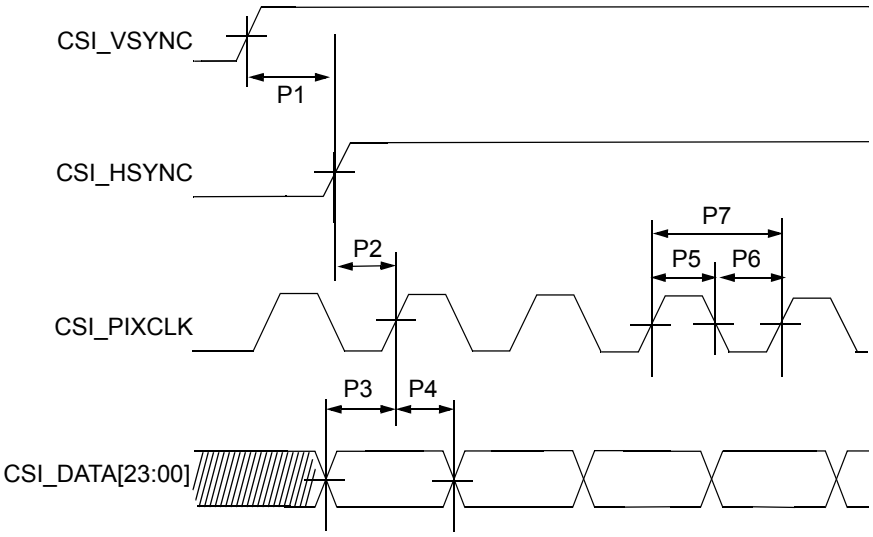


Figure 32. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

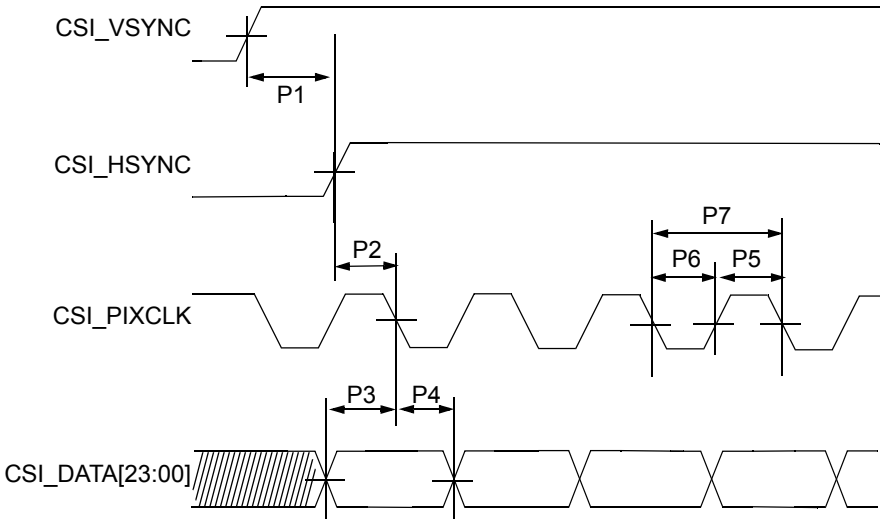


Figure 33. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 44. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns

Table 44. CSI Gated Clock Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Units
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns
P6	CSI pixel clock low time	tCLKl	3.75	—	ns
P7	CSI pixel clock frequency	fCLK	—	133	MHz

4.12.1.0.2 Ungated clock mode timing

Figure 34 shows the ungated clock mode timings of CSI, and Table 45 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

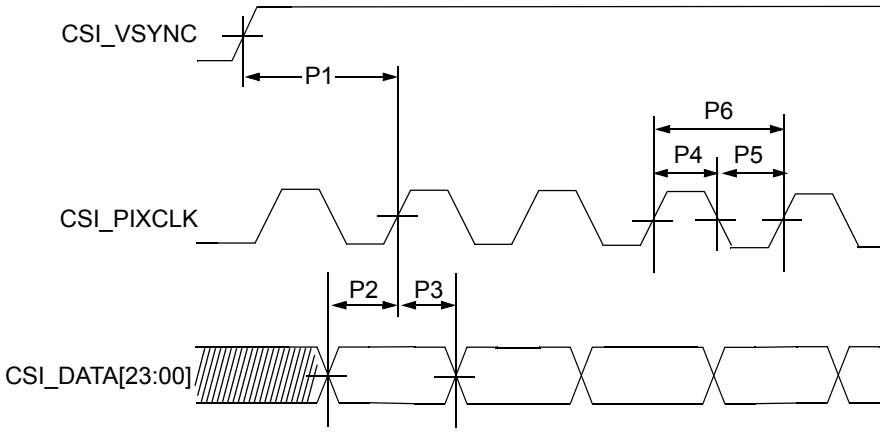


Figure 34. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 45. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	33.5	—	ns
P2	CSI DATA setup time	tDsu	1	—	ns
P3	CSI DATA hold time	tDh	1	—	ns
P4	CSI pixel clock high time	tCLKh	3.75	—	ns
P5	CSI pixel clock low time	tCLKl	3.75	—	ns
P6	CSI pixel clock frequency	fCLK	—	133	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.12.2 ECSPI timing parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.12.2.1 ECSPI master mode timing

Figure 35 depicts the timing of ECSPI in master mode. Table 46 lists the ECSPI master mode timing characteristics.

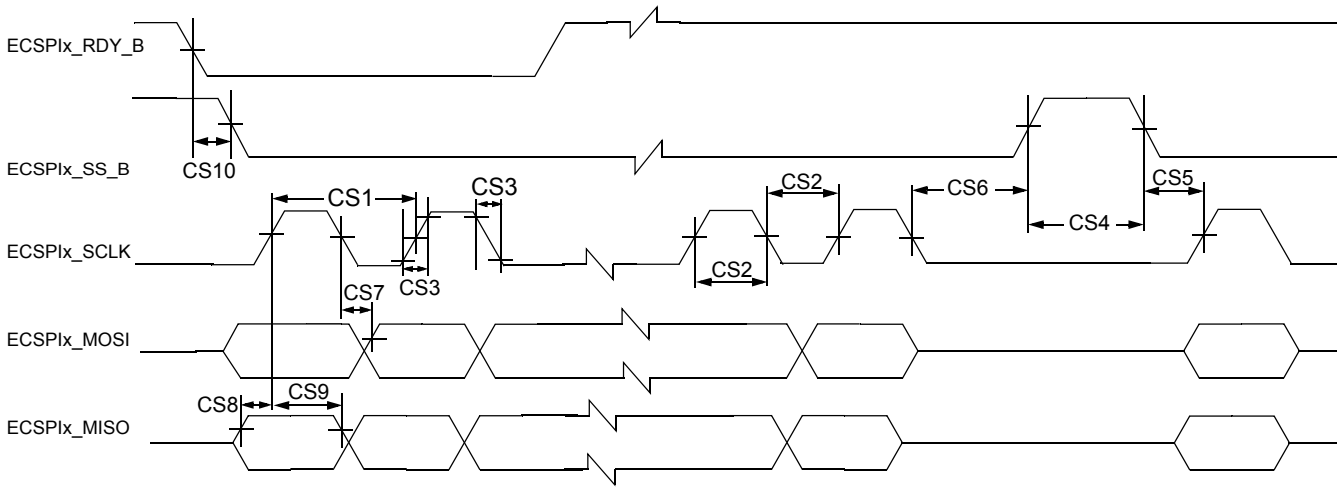


Figure 35. ECSPI Master Mode Timing Diagram

Table 46. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	14	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

[1] See specific I/O AC parameters Section 4.7, “I/O AC parameters”.”

[2] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.2.2 ECSPI slave mode timing

Figure 36 depicts the timing of ECSPI in slave mode. Table 47 lists the ECSPI slave mode timing characteristics.

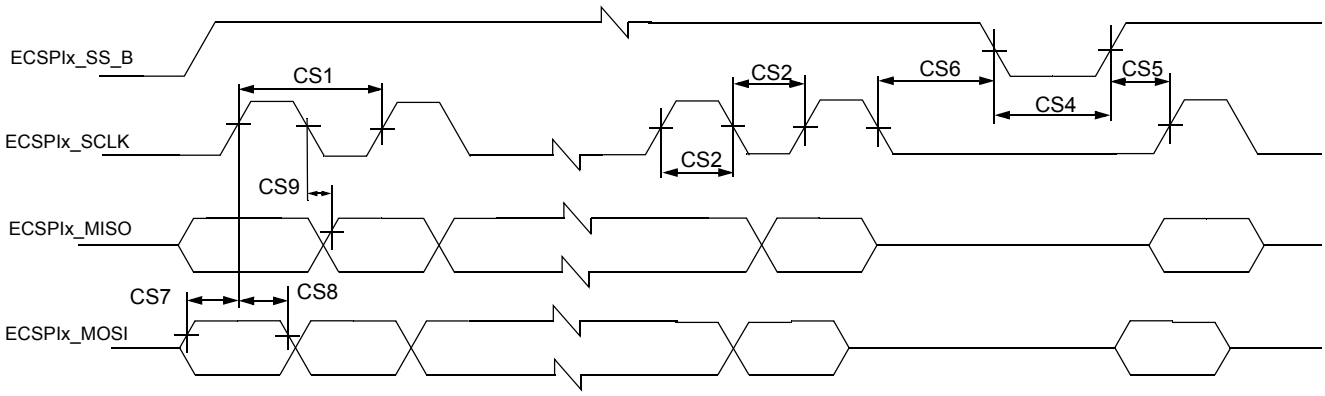


Figure 36. ECSPI Slave Mode Timing Diagram

Table 47. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

4.12.3 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41/4.5 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.12.3.1 SD/eMMC4.3 (single data rate) AC timing

Figure 37 depicts the timing of SD/eMMC4.3, and Table 48 lists the SD/eMMC4.3 timing characteristics.

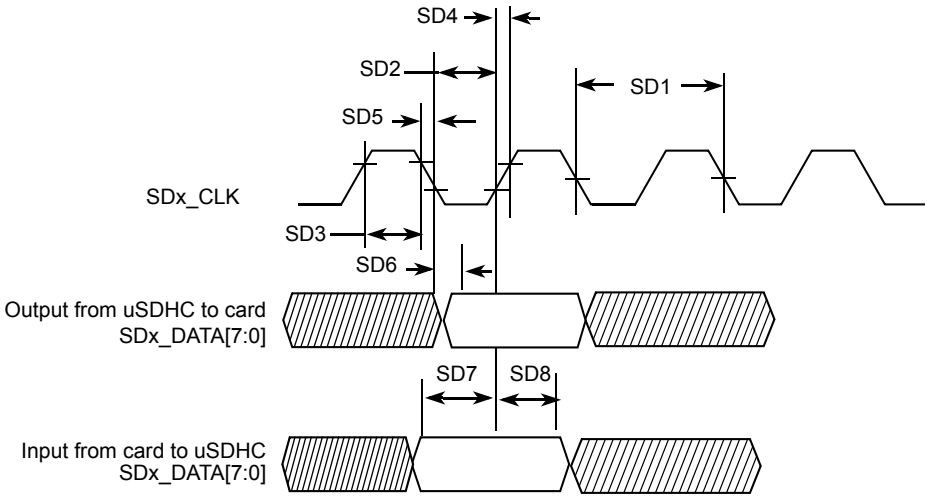


Figure 37. SD/eMMC4.3 Timing

Table 48. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Table 48. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.3.2 eMMC4.4/4.41 (dual data rate) AC timing

Figure 38 depicts the timing of eMMC4.4/4.41. Table 49 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

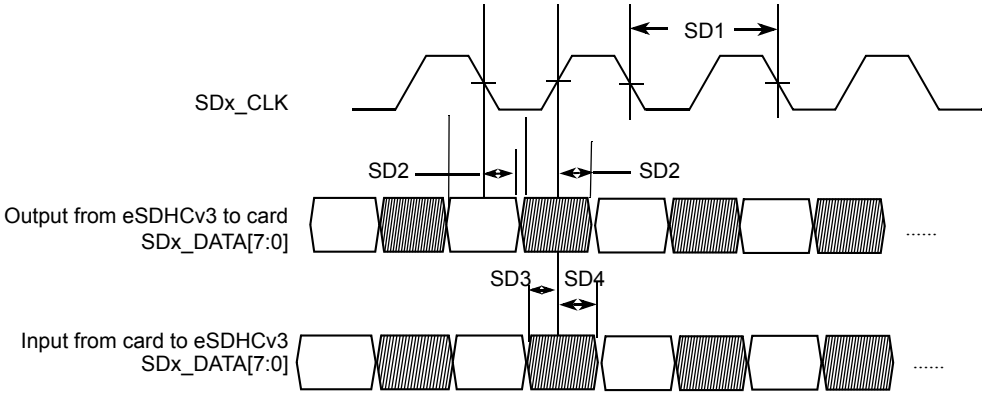


Figure 38. eMMC4.4/4.41 Timing

Table 49. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.12.3.3 SDR50/SDR104 AC timing

Figure 39 depicts the timing of SDR50/SDR104, and Table 50 lists the SDR50/SDR104 timing characteristics.

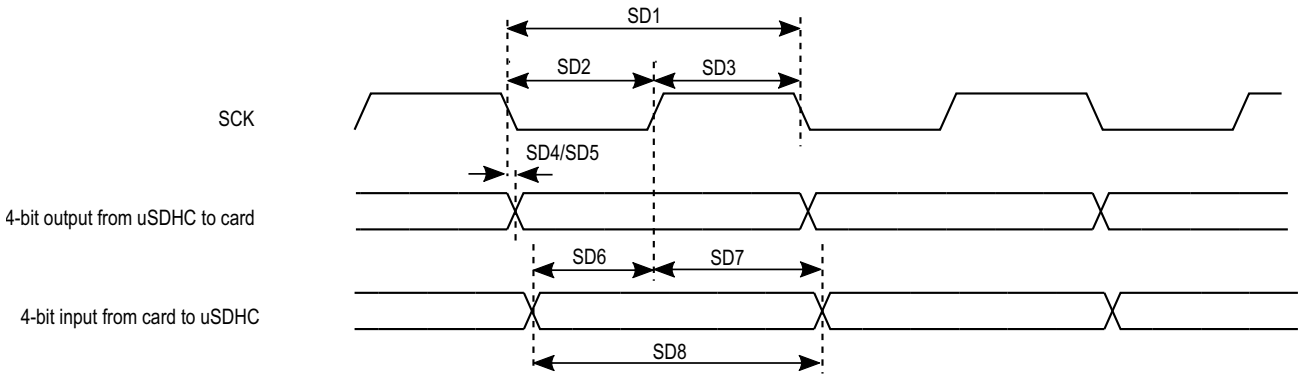


Figure 39. SDR50/SDR104 Timing

Table 50. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]Data window in SDR104 mode is variable.

4.12.3.4 HS200 mode timing

Figure 40 depicts the timing of HS200 mode, and Table 51 lists the HS200 timing characteristics.

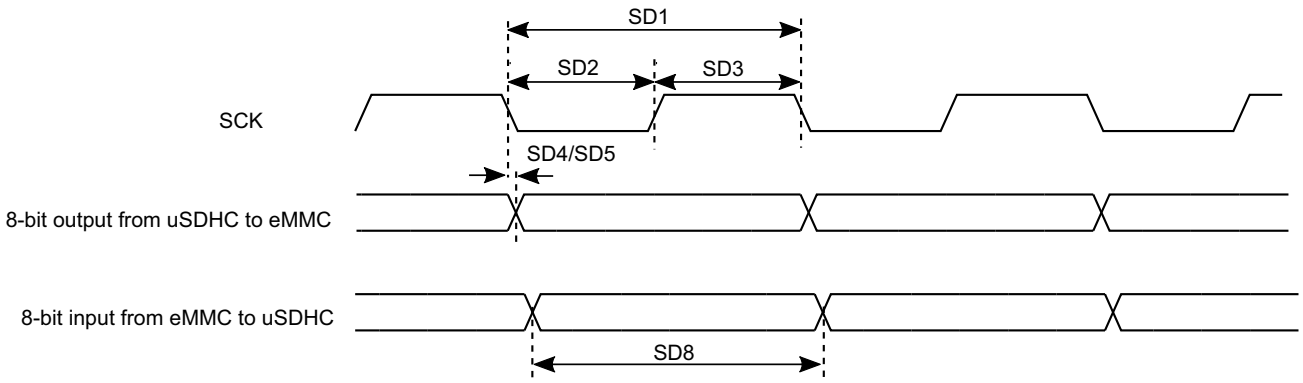


Figure 40. HS200 Mode Timing

Table 51. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.12.3.5 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1 supply are identical to those shown in Table 23, "Single Voltage GPIO DC Parameters," on page 35.

4.12.4 Ethernet Controller (ENET) AC electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.12.4.1 ENET MII mode timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.12.4.1.1 MII receive signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 41 shows MII receive signal timings. Table 52 describes the timing parameters (M1–M4) shown in the figure.

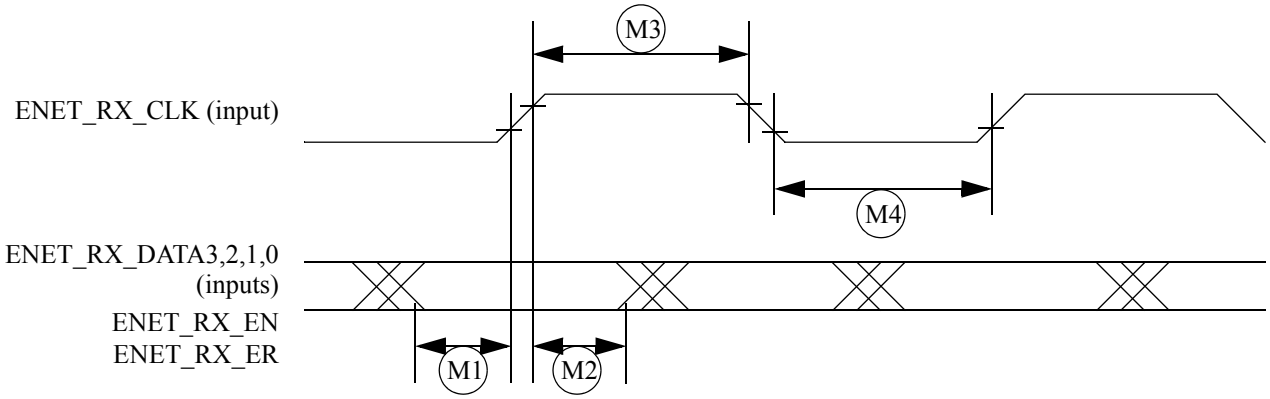


Figure 41. MII Receive Signal Timing Diagram

Table 52. MII Receive Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.12.4.1.2 MII transmit signal timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 42 shows MII transmit signal timings. Table 53 describes the timing parameters (M5–M8) shown in the figure.

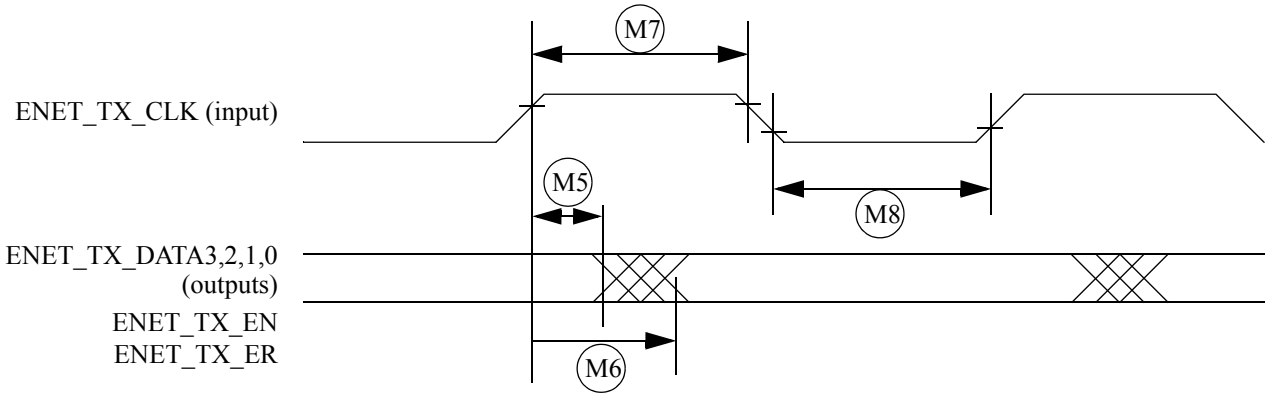


Figure 42. MII Transmit Signal Timing Diagram

Table 53. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.12.4.1.3 MII asynchronous inputs signal timing (ENET_CRS and ENET_COL)

Figure 43 shows MII asynchronous input timings. Table 54 describes the timing parameter (M9) shown in the figure.

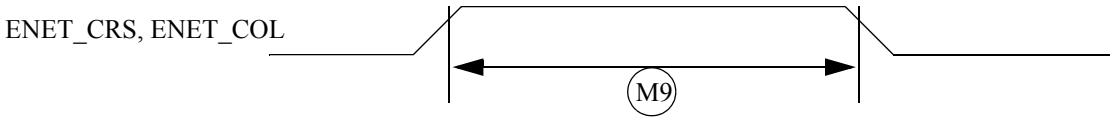


Figure 43. MII Async Inputs Timing Diagram

Table 54. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.12.4.1.4 MII serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 44 shows MII asynchronous input timings. Table 55 describes the timing parameters (M10–M15) shown in the figure.

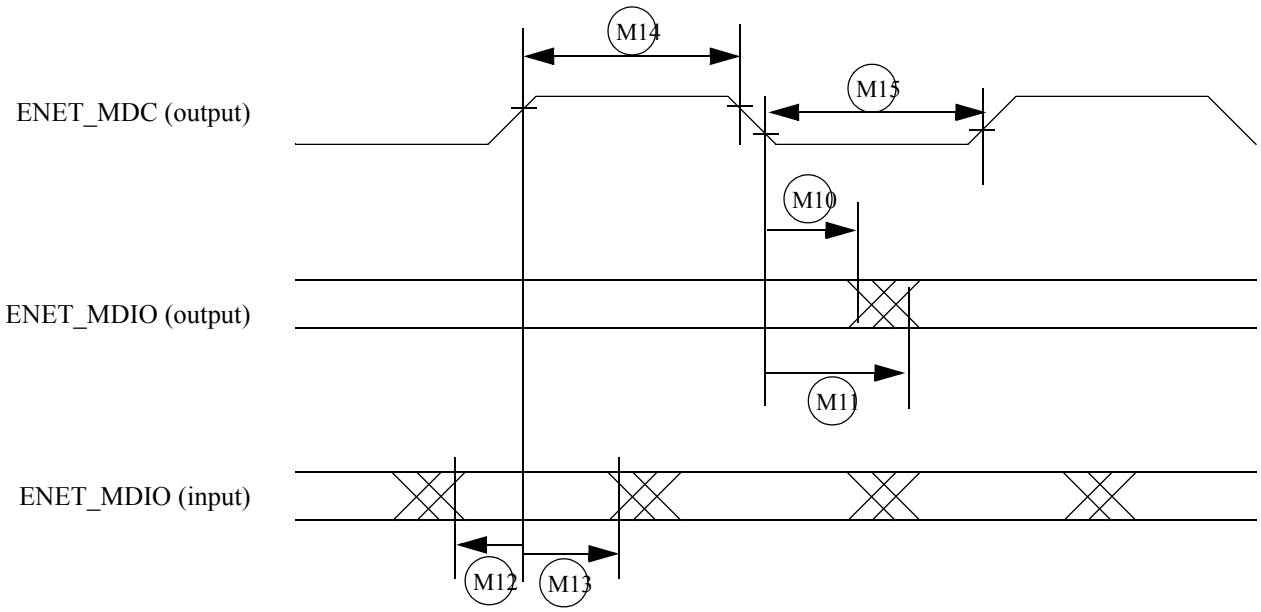


Figure 44. MII Serial Management Channel Timing Diagram

Table 55. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.12.4.2 RMII mode timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

Figure 45 shows RMII mode timings. Table 56 describes the timing parameters (M16–M21) shown in the figure.

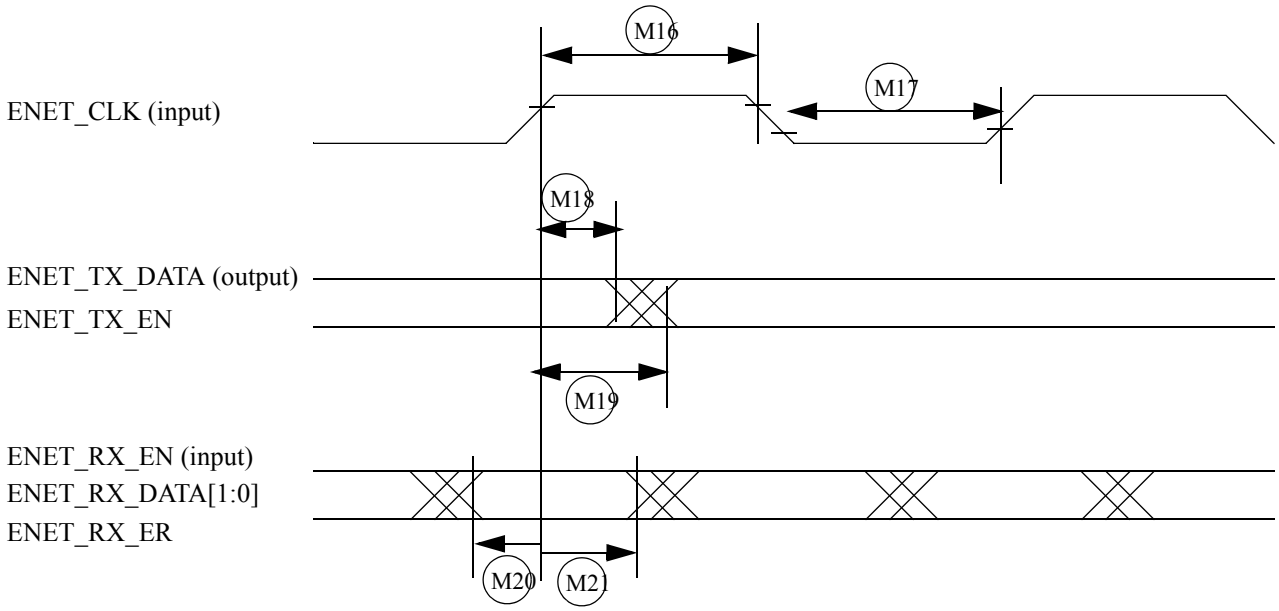


Figure 45. RMII Mode Signal Timing Diagram

Table 56. RMII Signal Timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	13	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	2	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.12.5 Flexible Controller Area Network (FLEXCAN) AC electrical specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6UltraLite Reference Manual* (IMX6ULRM) to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.12.6 I²C module timing parameters

This section describes the timing parameters of the I²C module. Figure 46 depicts the timing of I²C module, and Table 57 lists the I²C module timing characteristics.

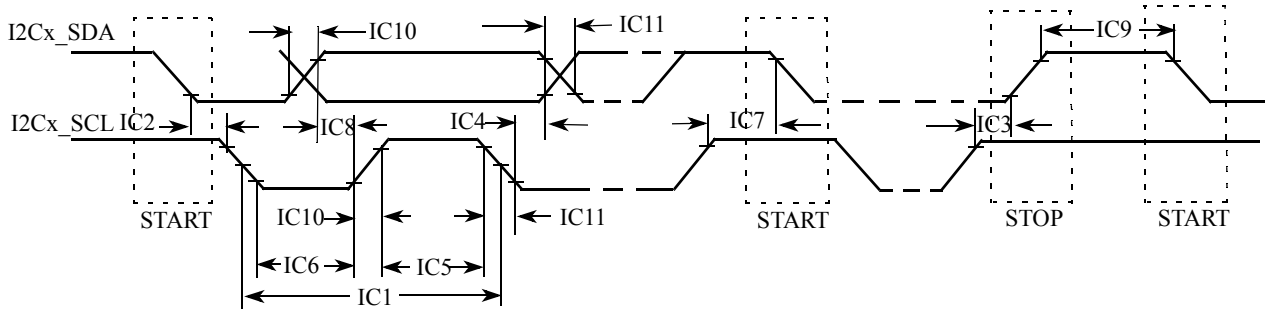


Figure 46. I²C Bus Timing

Table 57. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.12.7 Pulse Width Modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 47 depicts the timing of the PWM, and Table 58 lists the PWM timing parameters.

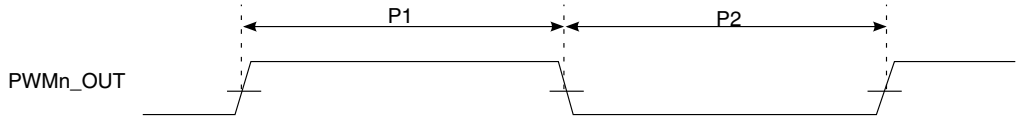


Figure 47. PWM Timing

Table 58. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.12.8 LCD Controller (LCDIF) parameters

Figure 48 shows the LCDIF timing and Table 59 lists the timing parameters.

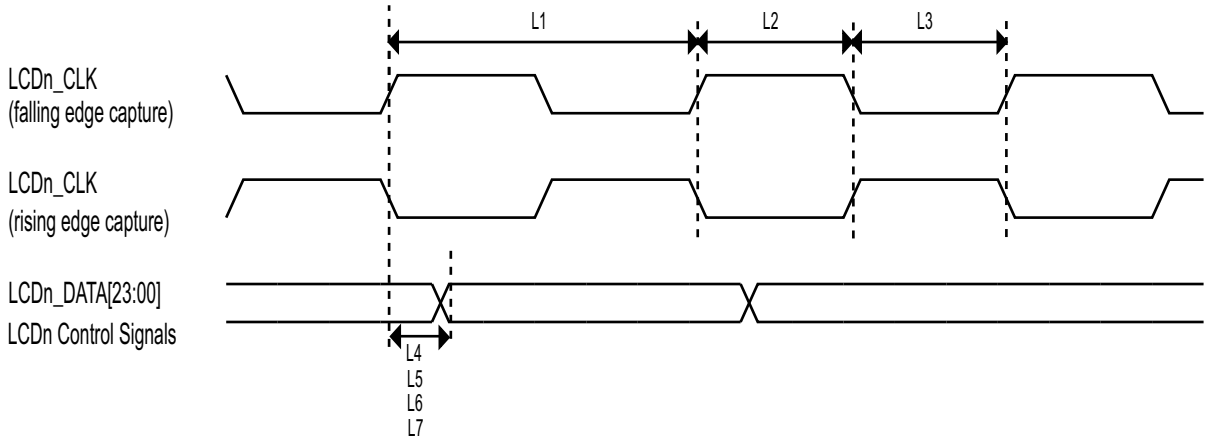


Figure 48. LCD Timing

Table 59. LCD Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	150	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.12.8.1 LCDIF signal mapping

Table 60 lists the details about the mapping signals.

Table 60. LCD Signal Parameters

Pin name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	24-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_RS	—	—	—	—	CCIR_CLK
LCD_VSYNC* (Two options)	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	—
LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	—
LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	—
LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	—
LCD_D23	—	—	—	R[7]	—
LCD_D22	—	—	—	R[6]	—
LCD_D21	—	—	—	R[5]	—
LCD_D20	—	—	—	R[4]	—
LCD_D19	—	—	—	R[3]	—
LCD_D18	—	—	—	R[2]	—
LCD_D17	—	—	R[5]	R[1]	—
LCD_D16	—	—	R[4]	R[0]	—
LCD_D15 / VSYNC*	—	R[4]	R[3]	G[7]	—
LCD_D14 / HSYNC**	—	R[3]	R[2]	G[6]	—
LCD_D13 / LCD_DOTCLK **	—	R21]	R[1]	G[5]	—

Table 60. LCD Signal Parameters (continued)

LCD_D12 / ENABLE**	—	R[1]	R[0]	G[4]	—
LCD_D11	—	R[0]	G[5]	G[3]	—
LCD_D10	—	G[5]	G[4]	G[2]	—
LCD_D9	—	G[4]	G[3]	G[1]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D7	R[2]	G[2]	G[1]	B[7]	Y/C[7]
LCD_D6	R[1]	G[1]	G[0]	B[6]	Y/C[6]
LCD_D5	R[0]	G[0]	B[5]	B[5]	Y/C[5]
LCD_D4	G[2]	B[4]	B[4]	B[4]	Y/C[4]
LCD_D3	G[1]	B[3]	B[3]	B[3]	Y/C[3]
LCD_D2	G[0]	B[2]	B[2]	B[2]	Y/C[2]
LCD_D1	B[1]	B[1]	B[1]	B[1]	Y/C[1]
LCD_D0	B[0]	B[0]	B[0]	B[0]	Y/C[0]
LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	—
LCD_BUSY / LCD_VSYNC	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	—

4.12.9 QUAD SPI (QSPI) timing parameters

Measurement conditions are with 35 pF load on SCK and SIO pins and input slew rate of 1 V/ns.

4.12.9.1 SDR mode

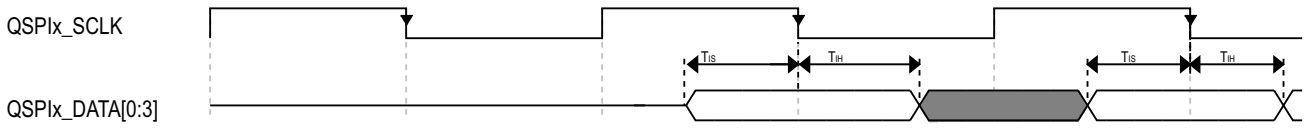


Figure 49. QuadSPI Input/Read Timing (SDR mode with internal sampling)

Table 61. QuadSPI Input Timing (SDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

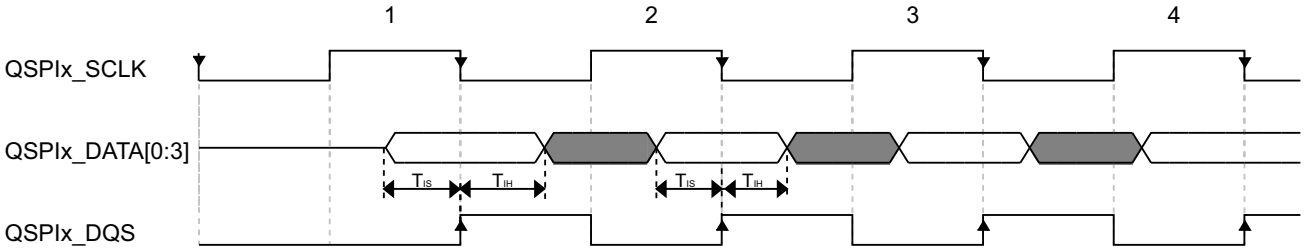


Figure 50. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Table 62. QuadSPI Input/Read Timing (SDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.
- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

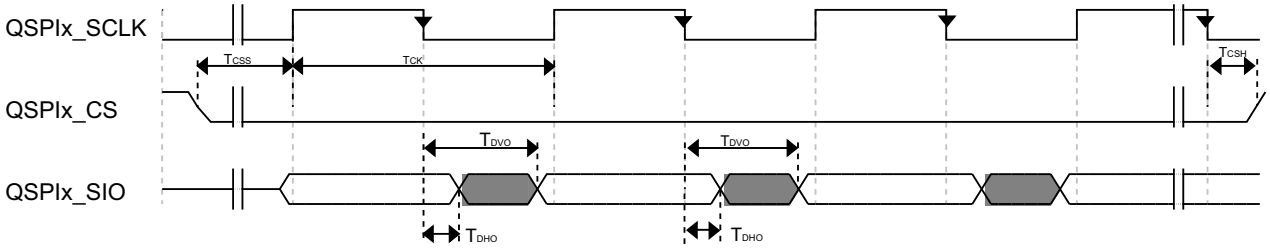


Figure 51. QuadSPI Output/Write Timing (SDR mode)

Table 63. QuadSPI Output/Write Timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	2	ns
T_{DHO}	Output data hold time	0	—	ns
T_{CK}	SCK clock period	10	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for more details.

4.12.9.2 DDR mode

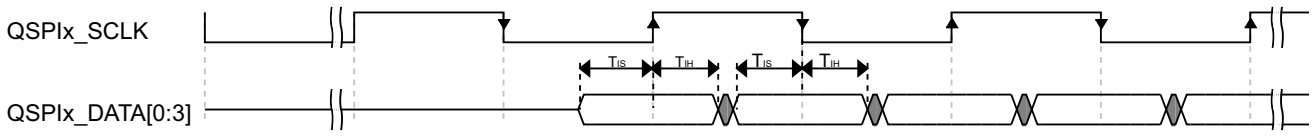


Figure 52. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 64. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

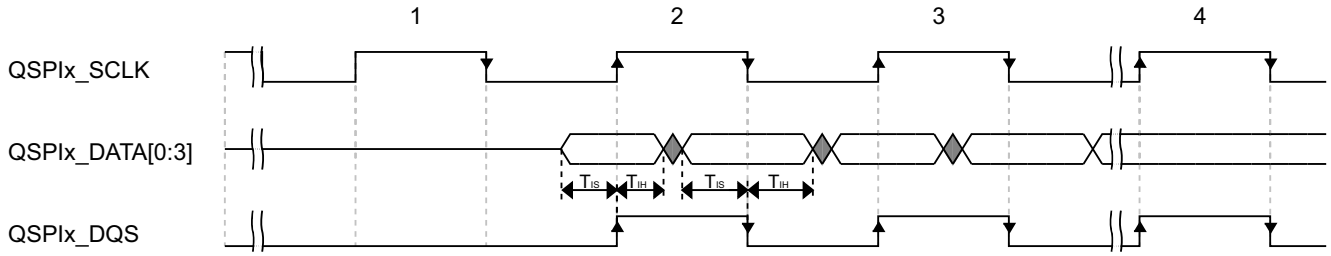


Figure 53. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Table 65. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.
- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.

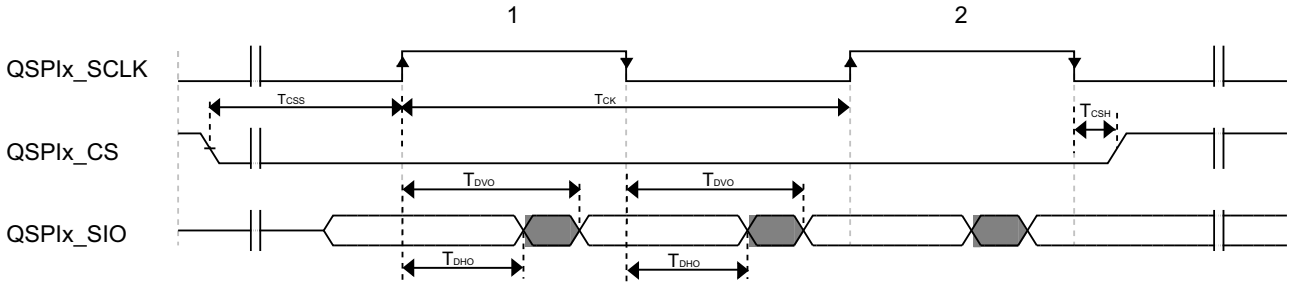


Figure 54. QuadSPI Output/Write Timing (DDR mode)

Table 66. QuadSPI Output/Write Timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	0.25 x T_{SCLK} + 2 ns	ns
T_{DHO}	Output data hold time	0.25 x T_{SCLK}	—	ns
T_{CK}	SCK clock period	20	—	ns

Table 66. QuadSPI Output/Write Timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for more details.

4.12.10 SAI/I2S switching specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 67. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	2 x t_{sys}	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	4 x t_{sys}	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

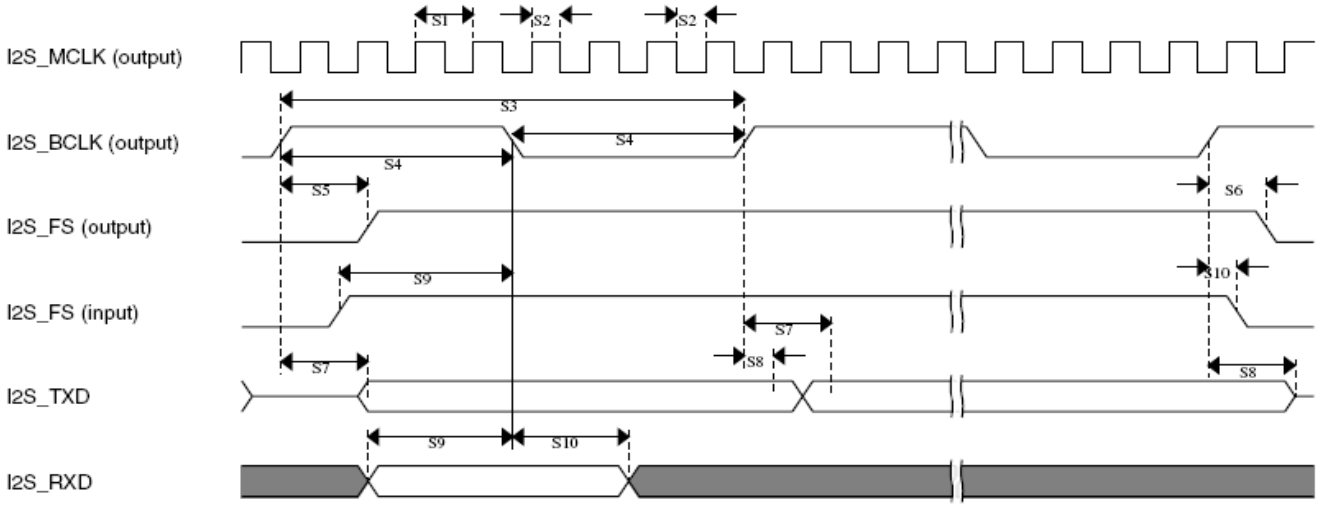


Figure 55. SAI Timing — Master Modes

Table 68. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{sys}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

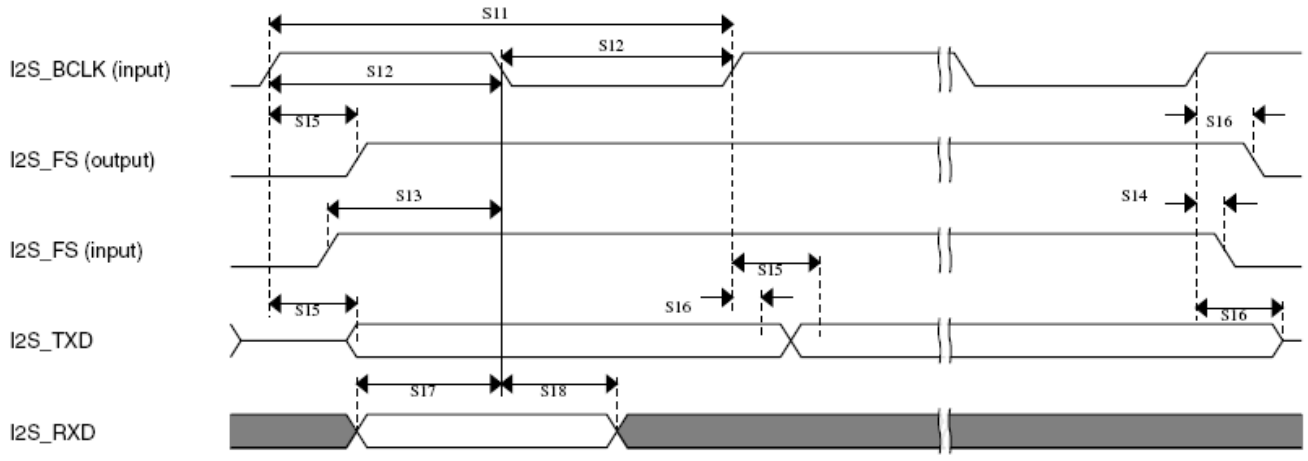


Figure 56. SAI Timing — Slave Modes

4.12.11 SCAN JTAG Controller (SJC) timing parameters

Figure 57 depicts the SJC test clock input timing. Figure 58 depicts the SJC boundary scan timing. Figure 59 depicts the SJC test access port. Signal parameters are listed in Table 69.

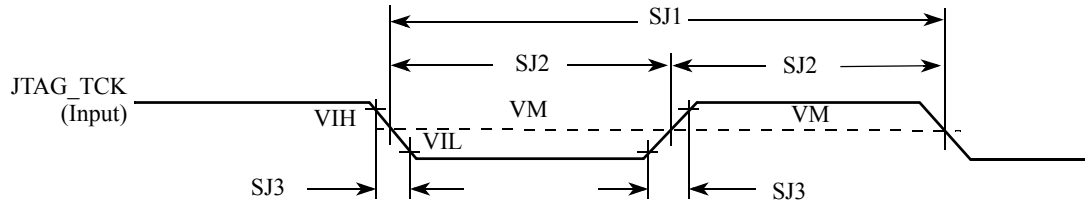


Figure 57. Test Clock Input Timing Diagram

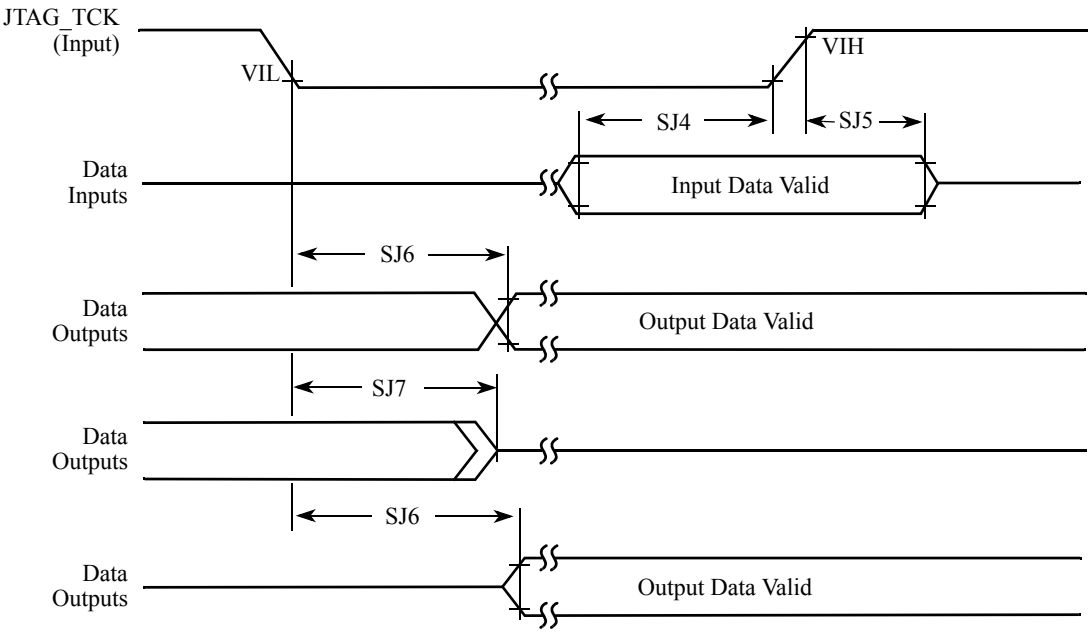


Figure 58. Boundary Scan (JTAG) Timing Diagram

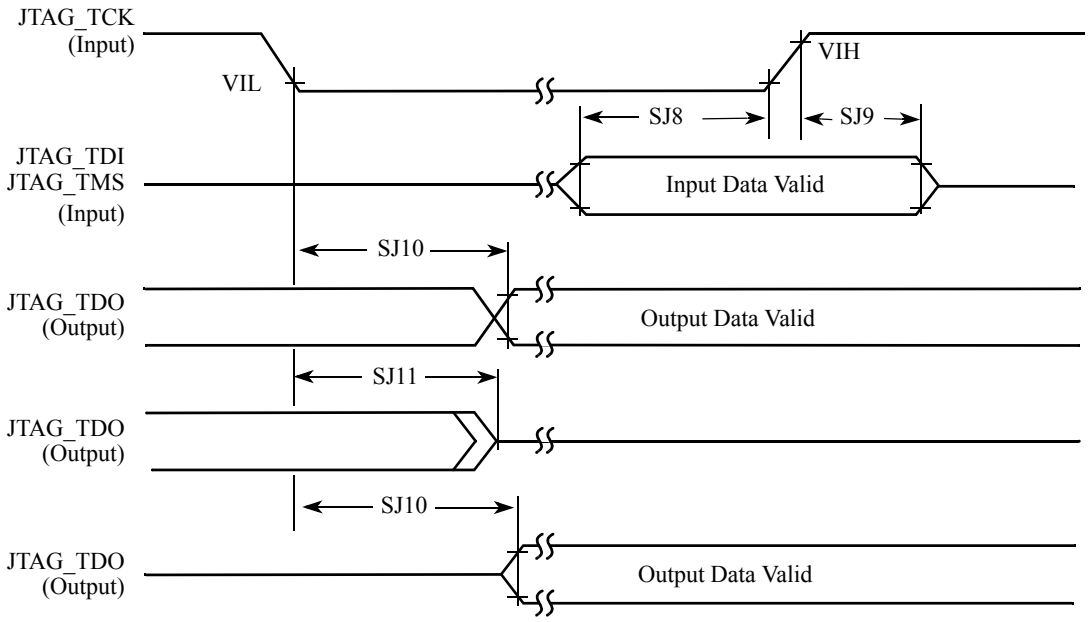


Figure 59. Test Access Port Timing Diagram

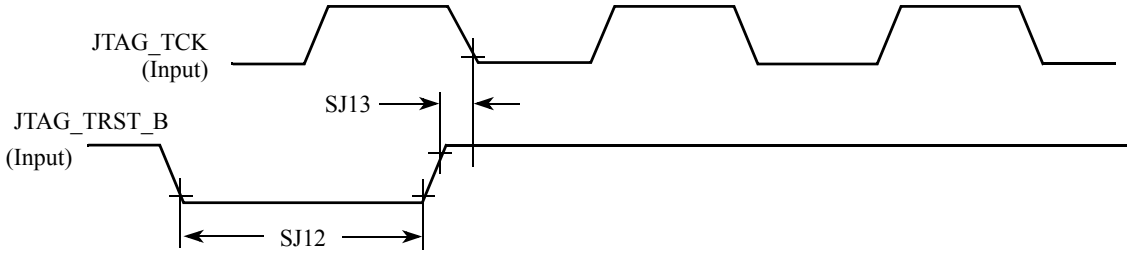


Figure 60. JTAG_TRST_B Timing Diagram

Table 69. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns

Table 69. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.12.12 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 70 and Figure 61 and Figure 62 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 70. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

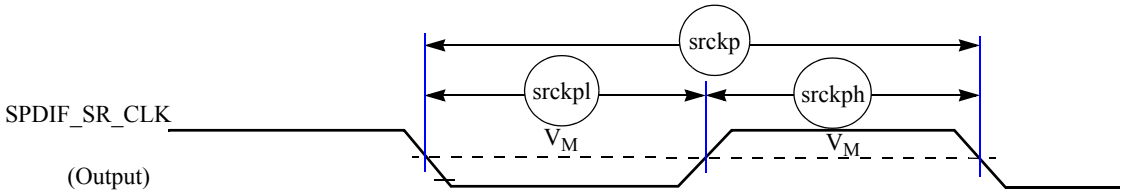


Figure 61. SPDIF_SR_CLK Timing Diagram

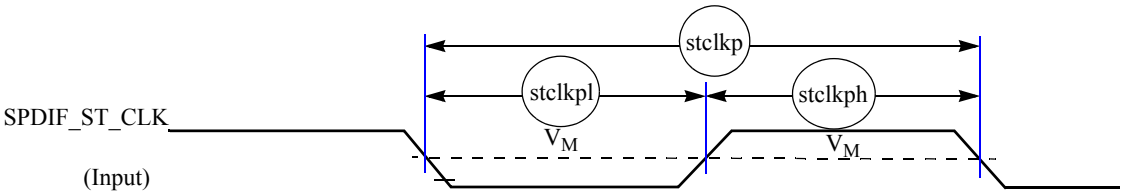


Figure 62. SPDIF_ST_CLK Timing Diagram

4.12.13 UART I/O configuration and timing parameters

4.12.13.1 UART RS-232 serial mode timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.13.1.1 UART transmitter

Figure 63 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 71 lists the UART RS-232 serial mode transmits timing characteristics.

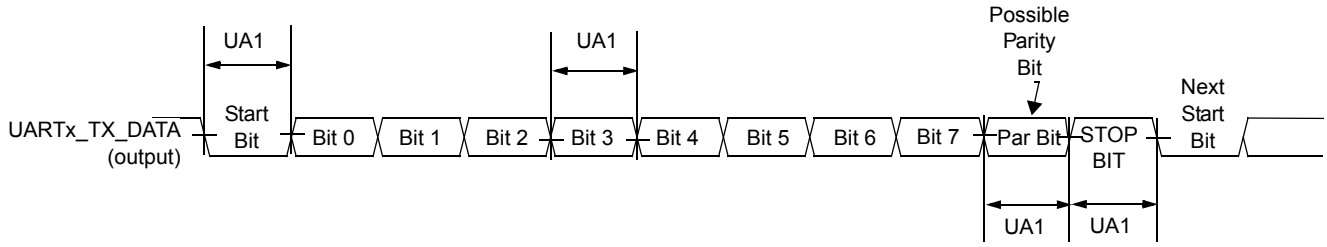


Figure 63. UART RS-232 Serial Mode Transmit Timing Diagram

Table 71. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.12.13.1.2 UART receiver

Figure 64 depicts the RS-232 serial mode receives timing with 8 data bit/1 stop bit format. Table 72 lists serial mode receive timing characteristics.

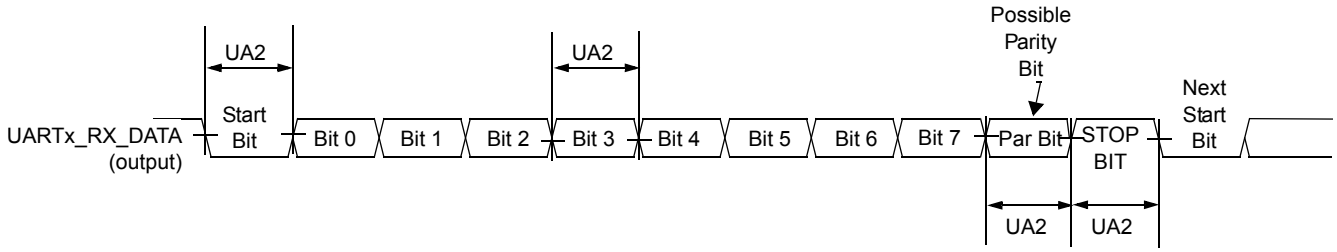


Figure 64. UART RS-232 Serial Mode Receive Timing Diagram

Table 72. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.13.1.3 UART IrDA mode timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA mode transmitter

Figure 65 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 73 lists the transmit timing characteristics.

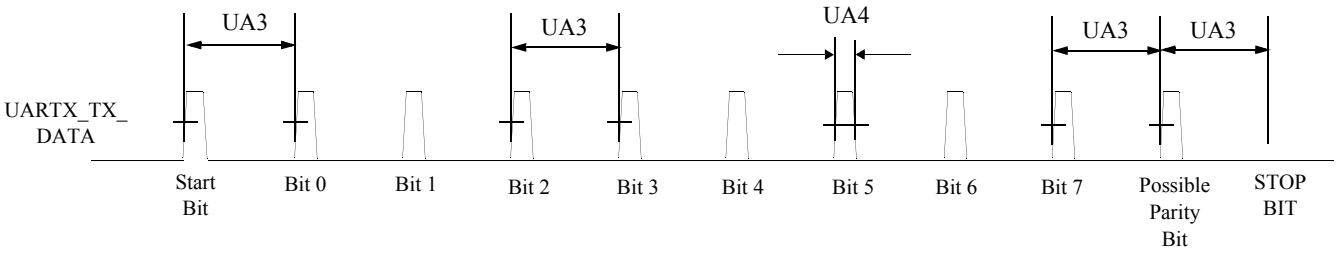


Figure 65. UART IrDA Mode Transmit Timing Diagram

Table 73. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA mode receiver

Figure 66 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 74 lists the receive timing characteristics.

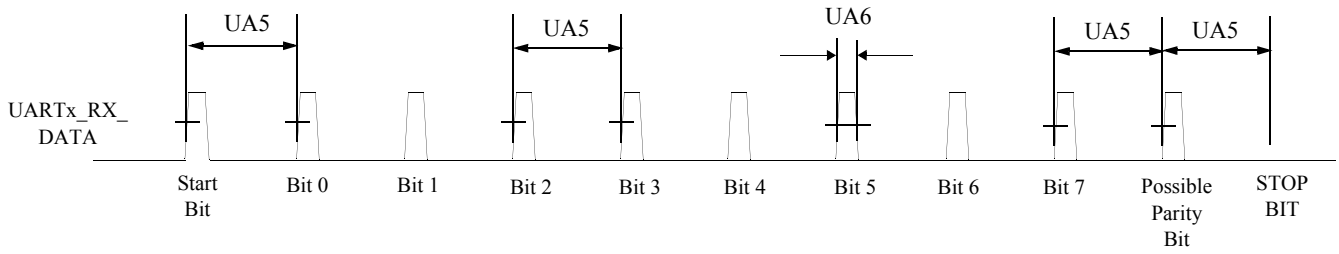


Figure 66. UART IrDA Mode Receive Timing Diagram

Table 74. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.14 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs

— Applies to: Universal Serial Bus Specification, Revision 2.0

- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  — Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  — Revision 1.2, December 7, 2010
  — Portable device only

4.13 A/D converter

4.13.1 12-bit ADC electrical characteristics

4.13.1.1 12-bit ADC operating conditions

Table 75. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	3.0	-	3.6	V	—
	Delta to VDD (VDD-VDDAD)[2]	ΔVDDAD	-100	0	100	mV	—
Ground voltage	Delta to VSS (VSS-VSSAD)	ΔVSSAD	-100	0	100	mV	—
Ref Voltage High	—	V_{REFH}	1.13	V_{DDAD}	V_{DDAD}	V	—
Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	—
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	8/10/12 bit modes	C_{ADIN}	—	1.5	2	pF	—
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	—	5	7	kohms	—
	ADLPC=0, ADHSC=0		—	12.5	15	kohms	—
	ADLPC=1, ADHSC=0		—	25	30	kohms	—
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	—	—	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	—	40	MHz	—
	ADLPC=0, ADHSC=0 12 bit mode		4	—	30	MHz	—
	ADLPC=1, ADHSC=0 12 bit mode		4	—	20	MHz	—

[1] Typical values assume VDDAD = 3.0 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential differences

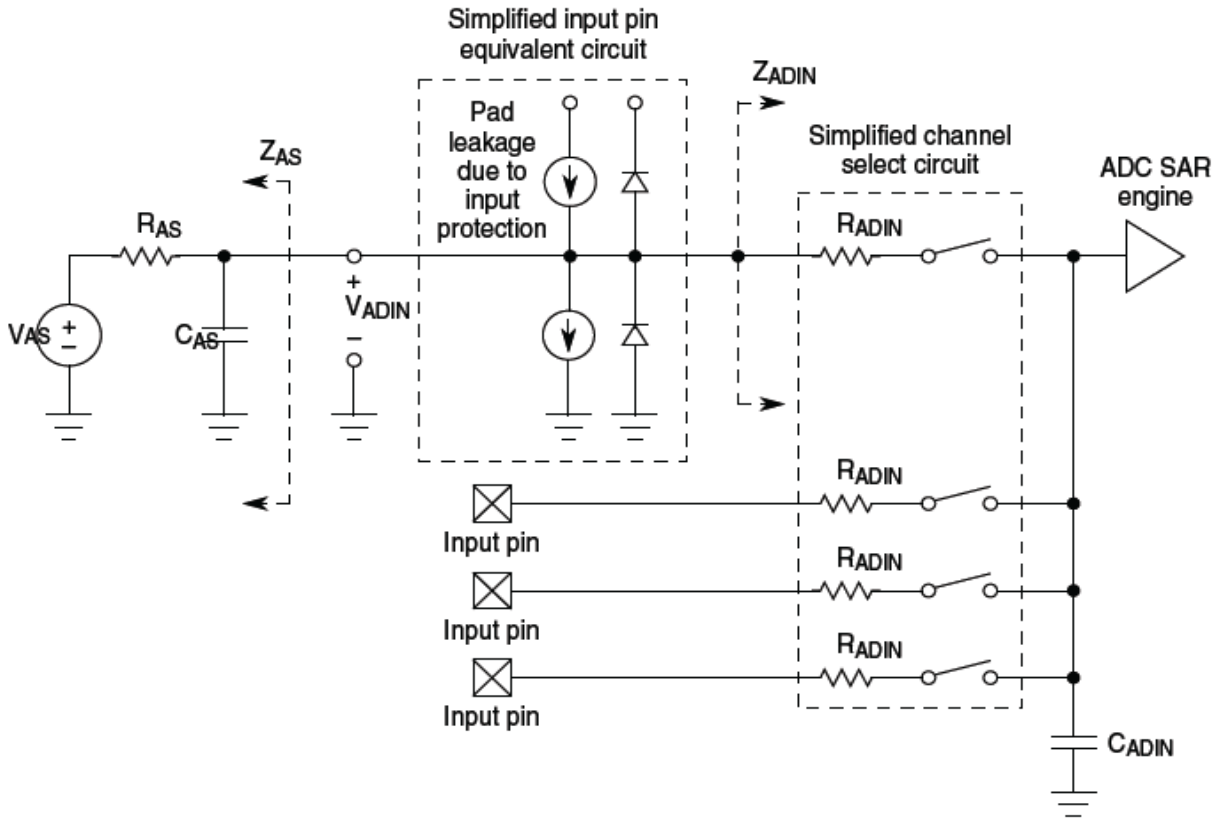


Figure 67. 12-bit ADC Input Impedance Equivalency Diagram

4.13.1.1.1 12-bit ADC characteristics

Table 76. 12-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
[L:] Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	250	—	µA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
[L:] Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	0.8	µA	—
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}	—	10	—	MHz	$t_{ADACK} = 1/f_{ADACK}$
	ADHSC=1		—	20	—		

Table 76. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp	—	2	—	cycles	—
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv	—	28	—	cycles	—
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			

Table 76. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	Comment
Conversion Time	ADLSMP=0 ADSTS=00	Tconv	—	0.7	—	µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
[P:][C:] Total Unadjusted Error	12 bit mode	TUE	—	4.5	—	LSB 1 LSB = $(V_{REFH} - V_{REFL})/2^N$	—
	10 bit mode		—	2	—		
	8 bit mode		—	1.5	—		
[P:][C:] Differential Non-Linearity	12 bit mode	DNL	—	1	—	LSB	—
	10bit mode		—	0.5	—		
	8 bit mode		—	0.2	—		
[P:][C:] Integral Non-Linearity	12 bit mode	INL	—	2.6	—	LSB	—
	10bit mode		—	0.8	—		
	8 bit mode		—	0.3	—		
Zero-Scale Error	12 bit mode	E_{ZS}	—	-0.3	—	LSB	—
	10bit mode		—	-0.15	—		
	8 bit mode		—	-0.15	—		
Full-Scale Error	12 bit mode	E_{FS}	—	-2.5	—	LSB	—
	10bit mode		—	-0.6	—		
	8 bit mode		—	-0.3	—		
[L:] Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	—	Bits	—
[L:] Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	—

[1] All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

[2] Typical values assume V_{DDAD} = 3.0 V, Temp = 25°C, F_{adck}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot mode configuration pins

Table 77 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6UltraLite Fuse Map document and the System Boot chapter in *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

Table 77. Fuses and Associated Pins Used for Boot

Pin	Direction at reset	eFuse name	Details
BOOT_MODE0	Input with 100 K pull-down	N/A	Boot mode selection
BOOT_MODE1	Input with 100 K pull-down	N/A	Boot mode selection

Table 77. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at reset	eFuse name	Details
LCD_DATA00	Input with 100 K pull-down	BT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
LCD_DATA01	Input with 100 K pull-down	BT_CFG1[1]	
LCD_DATA02	Input with 100 K pull-down	BT_CFG1[2]	
LCD_DATA03	Input with 100 K pull-down	BT_CFG1[3]	
LCD_DATA04	Input with 100 K pull-down	BT_CFG1[4]	
LCD_DATA05	Input with 100 K pull-down	BT_CFG1[5]	
LCD_DATA06	Input with 100 K pull-down	BT_CFG1[6]	
LCD_DATA07	Input with 100 K pull-down	BT_CFG1[7]	
LCD_DATA08	Input with 100 K pull-down	BT_CFG2[0]	
LCD_DATA09	Input with 100 K pull-down	BT_CFG2[1]	
LCD_DATA10	Input with 100 K pull-down	BT_CFG2[2]	
LCD_DATA11	Input with 100 K pull-down	BT_CFG2[3]	
LCD_DATA12	Input with 100 K pull-down	BT_CFG2[4]	
LCD_DATA13	Input with 100 K pull-down	BT_CFG2[5]	
LCD_DATA14	Input with 100 K pull-down	BT_CFG2[6]	
LCD_DATA15	Input with 100 K pull-down	BT_CFG2[7]	
LCD_DATA16	Input with 100 K pull-down	BT_CFG4[0]	
LCD_DATA17	Input with 100 K pull-down	BT_CFG4[1]	
LCD_DATA18	Input with 100 K pull-down	BT_CFG4[2]	
LCD_DATA19	Input with 100 K pull-down	BT_CFG4[3]	
LCD_DATA20	Input with 100 K pull-down	BT_CFG4[4]	
LCD_DATA21	Input with 100 K pull-down	BT_CFG4[5]	
LCD_DATA22	Input with 100 K pull-down	BT_CFG4[6]	
LCD_DATA23	Input with 100 K pull-down	BT_CFG4[7]	

5.2 Boot device interface allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 78. QSPI Boot trough QSPI

Ball Name	Signal Name	Mux Mode	Common	Quad Mode	+ Port A DQS	+ Port A CS1	+ Port B	+ Port B DQS	+ Port B CS1
NAND_WP_B	qspi.A_SCLK	Alt2	Yes	Yes					
NAND_DQS	qspi.A_SS0_B	Alt2	Yes	Yes					

Table 78. QSPI Boot trough QSPI (continued)

NAND_READY_B	qspi.A_DATA[0]	Alt2	Yes	Yes					
NAND_CE0_B	qspi.A_DATA[1]	Alt2	Yes	Yes					
NAND_CE1_B	qspi.A_DATA[2]	Alt2	Yes	Yes					
NAND_CLE	qspi.A_DATA[3]	Alt2	Yes	Yes					
NAND_DATA05	qspi.B_DATA[3]	Alt2					Yes		
NAND_DATA04	qspi.B_DATA[2]	Alt2					Yes		
NAND_DATA03	qspi.B_DATA[1]	Alt2					Yes		
NAND_DATA02	qspi.B_DATA[0]	Alt2					Yes		
NAND_WE_B	qspi.B_SS0_B	Alt2					Yes		
NAND_RE_B	qspi.B_SCLK	Alt2					Yes		
NAND_DATA07	qspi.A_SS1_B	Alt2				Yes			
NAND_ALE	qspi.A_DQS	Alt2			Yes				
NAND_DATA00	qspi.B_SS1_B	Alt2							Yes
NAND_DATA01	qspi.B_DQS	Alt2						Yes	

Table 79. SPI Boot through ECSPI1

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4 [5:4]=01b	BOOT_CFG4 [5:4]=10b	BOOT_CFG4 [5:4]=11b
CSI_DATA07	ecspi1.MISO	Alt 3	Yes				
CSI_DATA06	ecspi1.MOSI	Alt 3	Yes				
CSI_DATA04	ecspi1.SCLK	Alt 3	Yes				
CSI_DATA05	ecspi1.SS0	Alt 3		Yes			
LCD_DATA05	ecspi1.SS1	Alt 8			Yes		
LCD_DATA06	ecspi1.SS2	Alt 8				Yes	
LCD_DATA07	ecspi1.SS3	Alt 8					Yes

Table 80. SPI Boot through ECSPI2

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG 4[5:4]=00b	BOOT_CFG4 [5:4]=01b	BOOT_CFG4 [5:4]=10b	BOOT_CFG4 [5:4]=11b
CSI_DATA03	ecspi2.MISO	Alt 3	Yes				
CSI_DATA02	ecspi2.MOSI	Alt 3	Yes				
CSI_DATA00	ecspi2.SCLK	Alt 3	Yes				
CSI_DATA01	ecspi2.SS0	Alt 3		Yes			
LCD_HSYNC	ecspi2.SS1	Alt 8			Yes		

Table 80. SPI Boot through ECSPI2 (continued)

LCD_VSYNC	ecspi2.SS2	Alt 8				Yes	
LCD_RESET	ecspi2.SS3	Alt 8					Yes

Table 81. SPI Boot through ECSPI3

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4[5:4]=01b	BOOT_CFG4[5:4]=10b	BOOT_CFG4 [5:4]=11b
UART2_RTS_B	ecspi3.MISO	Alt 8	Yes				
UART2_CTS_B	ecspi3.MOSI	Alt 8	Yes				
UART2_RX_DATA	ecspi3.SCLK	Alt 8	Yes				
UART2_TX_DATA	ecspi3.SS0	Alt 8		Yes			
NAND_ALE	ecspi3.SS1	Alt 8			Yes		
NAND_RE_B	ecspi3.SS2	Alt 8				Yes	
NAND_WE_B	ecspi3.SS3	Alt 8					Yes

Table 82. SPI Boot through ECSPI4

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4 [5:4]=01b	BOOT_CFG4[5:4]=10b	BOOT_CFG 4[5:4]=11b
ENET2_TX_CLK	ecspi4.MISO	Alt 3	Yes				
ENET2_TX_EN	ecspi4.MOSI	Alt 3	Yes				
ENET2_TX_DATA1	ecspi4.SCLK	Alt 3	Yes				
ENET2_RX_ER	ecspi4.SS0	Alt 3		Yes			
NAND_DATA01	ecspi4.SS1	Alt 8			Yes		
NAND_DATA02	ecspi4.SS2	Alt 8				Yes	
NAND_DATA03	ecspi4.SS3	Alt 8					Yes

Table 83. NAND Boot through GPMI

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_CLE	rawnand.CLE	Alt 0	Yes		
NAND_ALE	rawnand.ALE	Alt 0	Yes		
NAND_WP_B	rawnand.WP_B	Alt 0	Yes		
NAND_READY_B	rawnand.READY_B	Alt 0	Yes		
NAND_CE0_B	rawnand.CE0_B	Alt 0	Yes		
NAND_CE1_B	rawnand.CE1_B	Alt 0		Yes	Yes
NAND_RE_B	rawnand.RE_B	Alt 0	Yes		
NAND_WE_B	rawnand.WE_B	Alt 0	Yes		

Table 83. NAND Boot through GPMI (continued)

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG1[3:2]= 01b	BOOT_CFG1[3:2]= 10b
NAND_DATA00	rawnand.DATA00	Alt 0	Yes		
NAND_DATA01	rawnand.DATA01	Alt 0	Yes		
NAND_DATA02	rawnand.DATA02	Alt 0	Yes		
NAND_DATA03	rawnand.DATA03	Alt 0	Yes		
NAND_DATA04	rawnand.DATA04	Alt 0	Yes		
NAND_DATA05	rawnand.DATA05	Alt 0	Yes		
NAND_DATA06	rawnand.DATA06	Alt 0	Yes		
NAND_DATA07	rawnand.DATA07	Alt 0	Yes		
NAND_DQS	rawnand.DQS	Alt 0	Yes		
CSI_MCLK	rawnand.CE2_B	Alt 2			Yes
CSI_PIXCLK	rawnand.CE3_B	Alt 2			Yes

Table 84. SD/MMC Boot through USDHC1

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)	SDMMC MFG mode
UART1_RTS_B	usdhc1.CD_B	Alt 2					Yes
SD1_CLK	usdhc1.CLK	Alt 0	Yes				
SD1_CMD	usdhc1.CMD	Alt 0	Yes				
SD1_DATA0	usdhc1.DATA0	Alt 0	Yes				
SD1_DATA1	usdhc1.DATA1	Alt 0		Yes	Yes		
SD1_DATA2	usdhc1.DATA2	Alt 0		Yes	Yes		
SD1_DATA3	usdhc1.DATA3	Alt 0	Yes				
NAND_READY_B	usdhc1.DATA4	Alt 1			Yes		
NAND_CE0_B	usdhc1.DATA5	Alt 1			Yes		
NAND_CE1_B	usdhc1.DATA6	Alt 1			Yes		
NAND_CLE	usdhc1.DATA7	Alt 1			Yes		
GPIO1_IO09	usdhc1.RESET_B	Alt 5				Yes	
GPIO1_IO05	usdhc1.VSELECT	Alt 4				Yes	

Table 85. SD/MMC Boot through USDHC2

Ball Name	Signal Name	Mux Mode	Common	4-bit	8-bit	BOOT_CFG1[1]=1 (SD Power Cycle)
NAND_RE_B	usdhc2.CLK	Alt 1	Yes			
NAND_WE_B	usdhc2.CMD	Alt 1	Yes			
NAND_DATA00	usdhc2.DATA0	Alt 1	Yes			
NAND_DATA01	usdhc2.DATA1	Alt 1		Yes	Yes	
NAND_DATA02	usdhc2.DATA2	Alt 1		Yes	Yes	
NAND_DATA03	usdhc2.DATA3	Alt 1	Yes			
NAND_DATA04	usdhc2.DATA4	Alt 1			Yes	
NAND_DATA05	usdhc2.DATA5	Alt 1			Yes	
NAND_DATA06	usdhc2.DATA6	Alt 1			Yes	
NAND_DATA07	usdhc2.DATA7	Alt 1			Yes	
NAND_ALE	usdhc2.RESET_B	Alt 5				Yes
GPIO1_IO08	usdhc2.VSELECT	Alt 4				Yes

Table 86. NOR/OneNAND Boot through EIM

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
CSI_DATA00	weim.AD[0]	Alt 4	Yes		
CSI_DATA01	weim.AD[1]	Alt 4	Yes		
CSI_DATA02	weim.AD[2]	Alt 4	Yes		
CSI_DATA03	weim.AD[3]	Alt 4	Yes		
CSI_DATA04	weim.AD[4]	Alt 4	Yes		
CSI_DATA05	weim.AD[5]	Alt 4	Yes		
CSI_DATA06	weim.AD[6]	Alt 4	Yes		
CSI_DATA07	weim.AD[7]	Alt 4	Yes		
NAND_DATA00	weim.AD[8]	Alt 4	Yes		
NAND_DATA01	weim.AD[9]	Alt 4	Yes		
NAND_DATA02	weim.AD[10]	Alt 4	Yes		
NAND_DATA03	weim.AD[11]	Alt 4	Yes		
NAND_DATA04	weim.AD[12]	Alt 4	Yes		
NAND_DATA05	weim.AD[13]	Alt 4	Yes		
NAND_DATA06	weim.AD[14]	Alt 4	Yes		
NAND_DATA07	weim.AD[15]	Alt 4	Yes		
NAND_CLE	weim.ADDR[16]	Alt 4		Yes	Yes

Table 86. NOR/OneNAND Boot through EIM (continued)

Ball Name	Signal Name	Mux Mode	Common	ADL16 Non-Mux	AD16 Mux
NAND_ALE	weim.ADDR[17]	Alt 4		Yes	Yes
NAND_CE1_B	weim.ADDR[18]	Alt 4		Yes	Yes
SD1_CMD	weim.ADDR[19]	Alt 4		Yes	Yes
SD1_CLK	weim.ADDR[20]	Alt 4		Yes	Yes
SD1_DATA0	weim.ADDR[21]	Alt 4		Yes	Yes
SD1_DATA1	weim.ADDR[22]	Alt 4		Yes	Yes
SD1_DATA2	weim.ADDR[23]	Alt 4		Yes	Yes
SD1_DATA3	weim.ADDR[24]	Alt 4		Yes	Yes
ENET2_RXER	weim.ADDR[25]	Alt 4		Yes	Yes
ENET2_CRS_DV	weim.ADDR[26]	Alt 4		Yes	Yes
CSI_MCLK	weim.CS0_B	Alt 4	Yes		
LCD_DATA08	weim.DATA[0]	Alt 4		Yes	
LCD_DATA09	weim.DATA[1]	Alt 4		Yes	
LCD_DATA10	weim.DATA[2]	Alt 4		Yes	
LCD_DATA11	weim.DATA[3]	Alt 4		Yes	
LCD_DATA12	weim.DATA[4]	Alt 4		Yes	
LCD_DATA13	weim.DATA[5]	Alt 4		Yes	
LCD_DATA14	weim.DATA[6]	Alt 4		Yes	
LCD_DATA15	weim.DATA[7]	Alt 4		Yes	
LCD_DATA16	weim.DATA[8]	Alt 4		Yes	
LCD_DATA17	weim.DATA[9]	Alt 4		Yes	
LCD_DATA18	weim.DATA[10]	Alt 4		Yes	
LCD_DATA19	weim.DATA[11]	Alt 4		Yes	
LCD_DATA20	weim.DATA[12]	Alt 4		Yes	
LCD_DATA21	weim.DATA[13]	Alt 4		Yes	
LCD_DATA22	weim.DATA[14]	Alt 4		Yes	
LCD_DATA23	weim.DATA[15]	Alt 4		Yes	
NAND_RE_B	weim.EB_B[0]	Alt 4		Yes	Yes
NAND_WE_B	weim.EB_B[1]	Alt 4		Yes	Yes
CSI_HSYNC	weim.LBA_B	Alt 4	Yes		
CSI_PIXCLK	weim.OE	Alt 4	Yes		
CSI_VSYNC	weim.RW	Alt 4	Yes		

Table 87. Serial Download through UART1

Ball Name	Signal Name	Mux Mode	Common
UART1_TX_DATA	uart1.TX_DATA	Alt 0	Yes
UART1_RX_DATA	uart1.RX_DATA	Alt 0	Yes

Table 88. Serial Download through UART2

Ball Name	Signal Name	Mux Mode	Common
UART2_TX_DATA	uart2.TX_DATA	Alt 0	Yes
UART2_RX_DATA	uart2.RX_DATA	Alt 0	Yes

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14x14 mm package information

6.1.1 14x14 mm, 0.8 mm pitch, ball matrix

Figure 68 shows the top, bottom, and side views of the 14x14 mm BGA package.

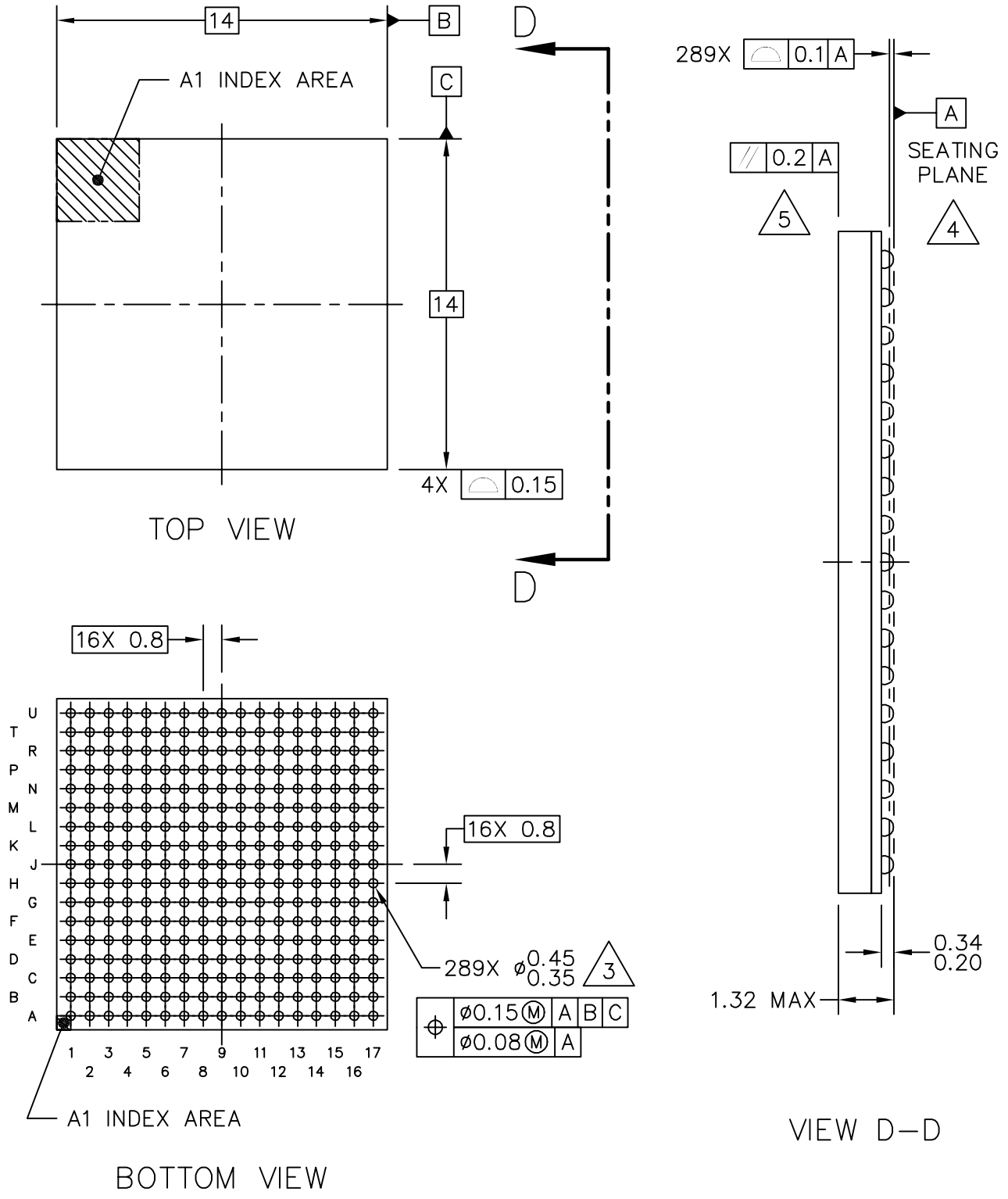


Figure 68. 14x14 mm BGA, Case x Package Top, Bottom, and Side Views

6.1.2 14x14 mm supplies contact assignments and functional contact assignments

Table 89 shows the device connection list for ground, sense, and reference contact signals.

Table 89. 14x14 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	M13	—
DRAM_VREF	p4	—
GPANAIO	R13	—
NGND_KEL0	M12	—
NVCC_CSI	F4	—
NVCC_DRAM	G6, H6, J6, K6, L6, M6	—
NVCC_DRAM_2P5	N6	—
NVCC_ENET	F13	—
NVCC_GPIO	J13	—
NVCC_LCD	E13	—
NVCC_NAND	E7	—
NVCC_PLL	P13	—
NVCC_SD1	C4	—
NVCC_UART	H13	—
VDD_ARM_CAP	G9, G10, G11, H11	—
VDD_HIGH_CAP	R14, R15	—
VDD_HIGH_IN	N13	—
VDD_SNVS_CAP	N12	—
VDD_SNVS_IN	P12	—
VDD_SOC_CAP	G8, H8, J8, J11, K8, K11, L8, L9, L10, L11	—
VDD_SOC_IN	H9, H10, J9, J10, K9, K10	—
VDD_USB_CAP	R12	—
VDDA_ADC_3P3	L13	—
VSS	A1, A17, C3, C7, C11, C15, E8, E11, F6, F7, F8, F9, F10,F11, F12, G3, G5, G7, G12, G15, H7, H12, J5, J7, J12, K7, K12, L3, L7, L12, M7, M8, M9, M10, M11, N3, N5, R3, R5, R7, R11, R16, R17, T14, U1, U14, U17	—

Table 90 shows an alpha-sorted list of functional contact assignments for the 14x14 mm package.

Table 90. 14x14 mm Functional Contact Assignments

Ball Name	14x14 Ball	Power Group	Ball Type	Out of Reset Condition			
				Default Mode	Default Function	Input/ Output	Value
BOOT_MODE0	T10	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	U10	VDD_SNVS_IN	GPIO	ALT5	BOOT_MODE1	Input	100 kΩ pull-down
CCM_CLK1_N	P16	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_N	—	—
CCM_CLK1_P	P17	VDD_HIGH_CAP	LVDS	—	CCM_CLK1_P	—	—
CCM_PMIC_STBY_REQ	U9	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	—
CSI_DATA00	E4	NVCC_CSI	GPIO	ALT5	CSI_DATA00	Input	Keeper
CSI_DATA01	E3	NVCC_CSI	GPIO	ALT5	CSI_DATA01	Input	Keeper
CSI_DATA02	E2	NVCC_CSI	GPIO	ALT5	CSI_DATA02	Input	Keeper
CSI_DATA03	E1	NVCC_CSI	GPIO	ALT5	CSI_DATA03	Input	Keeper
CSI_DATA04	D4	NVCC_CSI	GPIO	ALT5	CSI_DATA04	Input	Keeper
CSI_DATA05	D3	NVCC_CSI	GPIO	ALT0	CSI_DATA05	Input	Keeper
CSI_DATA06	D2	NVCC_CSI	GPIO	ALT5	CSI_DATA06	Input	Keeper
CSI_DATA07	D1	NVCC_CSI	GPIO	ALT5	CSI_DATA07	Input	Keeper
CSI_HSYNC	F3	NVCC_CSI	GPIO	ALT5	CSI_HSYNC	Input	Keeper
CSI_MCLK	F5	NVCC_CSI	GPIO	ALT5	CSI_MCLK	Input	Keeper
CSI_PIXCLK	E5	NVCC_CSI	GPIO	ALT5	CSI_PIXCLK	Input	Keeper
CSI_VSYNC	F2	NVCC_CSI	GPIO	ALT5	CSI_VSYNC	Input	Keeper
DRAM_ADDR00	L5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	100 kΩ pull-up
DRAM_ADDR01	H2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	100 kΩ pull-up
DRAM_ADDR02	K1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	100 kΩ pull-up
DRAM_ADDR03	M2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	100 kΩ pull-up
DRAM_ADDR04	K4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	100 kΩ pull-up
DRAM_ADDR05	L1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	100 kΩ pull-up
DRAM_ADDR06	G2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	100 kΩ pull-up

Table 90. 14x14 mm Functional Contact Assignments (continued)

DRAM_ADDR07	H4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	100 kΩ pull-up
DRAM_ADDR08	J4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	100 kΩ pull-up
DRAM_ADDR09	L2	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	100 kΩ pull-up
DRAM_ADDR10	M4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	100 kΩ pull-up
DRAM_ADDR11	K3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	100 kΩ pull-up
DRAM_ADDR12	L4	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	100 kΩ pull-up
DRAM_ADDR13	H3	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	100 kΩ pull-up
DRAM_ADDR14	G1	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	100 kΩ pull-up
DRAM_ADDR15	K5	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	100 kΩ pull-up
DRAM_CAS_B	J2	NVCC_DRAM	DDR	ALT0	DRAM_CAS_B	Output	100 kΩ pull-up
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	DRAM_CS0_B	Output	100 kΩ pull-up
DRAM_CS1_B	H5	NVCC_DRAM	DDR	ALT0	DRAM_CS1_B	Output	100 kΩ pull-up
DRAM_DATA00	T4	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_DATA01	U6	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_DATA02	T6	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_DATA03	U7	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_DATA04	U8	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_DATA05	T8	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_DATA06	T5	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_DATA07	U4	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_DATA08	U2	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up

Table 90. 14x14 mm Functional Contact Assignments (continued)

DRAM_DATA09	U3	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DATA10	U5	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_DATA11	R4	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_DATA12	P5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_DATA13	P3	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_DATA14	R2	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_DATA15	R1	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_DQM0	T7	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	100 kΩ pull-up
DRAM_DQM1	T3	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	100 kΩ pull-up
DRAM_ODT0	N1	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	100 kΩ pull-down
DRAM_ODT1	F1	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	100 kΩ pull-down
DRAM_RAS_B	M5	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	100 kΩ pull-up
DRAM_RESET	G4	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	100 kΩ pull-down
DRAM_SDBA0	M1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	100 kΩ pull-up
DRAM_SDBA1	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	100 kΩ pull-up
DRAM_SDBA2	K2	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	100 kΩ pull-up
DRAM_SDCKE0	M3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	100 kΩ pull-down
DRAM_SDCKE1	J3	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	100 kΩ pull-down
DRAM_SDCLK0_N	P2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_N	Input	100 kΩ pull-up
DRAM_SDCLK0_P	P1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Input	100 kΩ pull-up
DRAM_SDQS0_N	P7	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_N	Input	100 kΩ pull-down

Table 90. 14x14 mm Functional Contact Assignments (continued)

DRAM_SDQS0_P	P6	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	100 kΩ pull-down
DRAM_SDQS1_N	T2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_N	Input	100 kΩ pull-down
DRAM_SDQS1_P	T1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS1_P	Input	100 kΩ pull-down
DRAM_SDWE_B	J1	NVCC_DRAM	DDR	ALT0	DRAM_SDWE_B	Output	100 kΩ pull-up
DRAM_ZQPAD	N4	NVCC_DRAM	GPIO	—	DRAM_ZQPAD	Input	Keeper
ENET1_RX_DATA0	F16	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA0	Input	Keeper
ENET1_RX_DATA1	E17	NVCC_ENET	GPIO	ALT5	ENET1_RX_DATA1	Input	Keeper
ENET1_RX_EN	E16	NVCC_ENET	GPIO	ALT5	ENET1_RX_EN	Input	Keeper
ENET1_RX_ER	D15	NVCC_ENET	GPIO	ALT5	ENET1_RX_ER	Input	Keeper
ENET1_TX_CLK	F14	NVCC_ENET	GPIO	ALT5	ENET1_TX_CLK	Input	Keeper
ENET1_TX_DATA0	E15	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA0	Input	Keeper
ENET1_TX_DATA1	E14	NVCC_ENET	GPIO	ALT5	ENET1_TX_DATA1	Input	Keeper
ENET1_TX_EN	F15	NVCC_ENET	GPIO	ALT5	ENET1_TX_EN	Input	Keeper
ENET2_RX_DATA0	C17	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA0	Input	Keeper
ENET2_RX_DATA1	C16	NVCC_ENET	GPIO	ALT5	ENET2_RX_DATA1	Input	Keeper
ENET2_RX_EN	B17	NVCC_ENET	GPIO	ALT5	ENET2_RX_EN	Input	Keeper
ENET2_RX_ER	D16	NVCC_ENET	GPIO	ALT5	ENET2_RX_ER	Input	Keeper
ENET2_TX_CLK	D17	NVCC_ENET	GPIO	ALT5	ENET2_TX_CLK	Input	Keeper
ENET2_TX_DATA0	A15	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA0	Input	Keeper
ENET2_TX_DATA1	A16	NVCC_ENET	GPIO	ALT5	ENET2_TX_DATA1	Input	Keeper
ENET2_TX_EN	B15	NVCC_ENET	GPIO	ALT5	ENET2_TX_EN	Input	Keeper
GPIO1_IO00	K13	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	Keeper
GPIO1_IO01	L15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	Keeper
GPIO1_IO02	L14	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	Keeper
GPIO1_IO03	L17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	Keeper
GPIO1_IO04	M16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	Keeper
GPIO1_IO05	M17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	Keeper
GPIO1_IO06	K17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	Keeper
GPIO1_IO07	L16	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	Keeper
GPIO1_IO08	N17	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	Keeper
GPIO1_IO09	M15	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	Keeper

Table 90. 14x14 mm Functional Contact Assignments (continued)

JTAG_MOD	P15	NVCC_GPIO	GPIO	ALT5	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	M14	NVCC_GPIO	GPIO	ALT5	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	N16	NVCC_GPIO	GPIO	ALT5	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	N15	NVCC_GPIO	GPIO	ALT5	JTAG_TDO	Output	Keeper
JTAG_TMS	P14	NVCC_GPIO	GPIO	ALT5	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	N14	NVCC_GPIO	GPIO	ALT5	JTAG_TRST_B	Input	47 kΩ pull-up
LCD_CLK	A8	NVCC_LCD	GPIO	ALT5	LCD_CLK	Input	Keeper
LCD_DATA00	B9	NVCC_LCD	GPIO	ALT5	LCD_DATA00	Input	Keeper
LCD_DATA01	A9	NVCC_LCD	GPIO	ALT5	LCD_DATA01	Input	Keeper
LCD_DATA02	E10	NVCC_LCD	GPIO	ALT5	LCD_DATA02	Input	Keeper
LCD_DATA03	D10	NVCC_LCD	GPIO	ALT5	LCD_DATA03	Input	Keeper
LCD_DATA04	C10	NVCC_LCD	GPIO	ALT5	LCD_DATA04	Input	Keeper
LCD_DATA05	B10	NVCC_LCD	GPIO	ALT5	LCD_DATA05	Input	Keeper
LCD_DATA06	A10	NVCC_LCD	GPIO	ALT5	LCD_DATA06	Input	Keeper
LCD_DATA07	D11	NVCC_LCD	GPIO	ALT5	LCD_DATA07	Input	Keeper
LCD_DATA08	B11	NVCC_LCD	GPIO	ALT5	LCD_DATA08	Input	Keeper
LCD_DATA09	A11	NVCC_LCD	GPIO	ALT5	LCD_DATA09	Input	Keeper
LCD_DATA10	E12	NVCC_LCD	GPIO	ALT5	LCD_DATA10	Input	Keeper
LCD_DATA11	D12	NVCC_LCD	GPIO	ALT5	LCD_DATA11	Input	Keeper
LCD_DATA12	C12	NVCC_LCD	GPIO	ALT5	LCD_DATA12	Input	Keeper
LCD_DATA13	B12	NVCC_LCD	GPIO	ALT5	LCD_DATA13	Input	Keeper
LCD_DATA14	A12	NVCC_LCD	GPIO	ALT5	LCD_DATA14	Input	Keeper
LCD_DATA15	D13	NVCC_LCD	GPIO	ALT5	LCD_DATA15	Input	Keeper
LCD_DATA16	C13	NVCC_LCD	GPIO	ALT5	LCD_DATA16	Input	Keeper
LCD_DATA17	B13	NVCC_LCD	GPIO	ALT5	LCD_DATA17	Input	Keeper
LCD_DATA18	A13	NVCC_LCD	GPIO	ALT5	LCD_DATA18	Input	Keeper
LCD_DATA19	D14	NVCC_LCD	GPIO	ALT5	LCD_DATA19	Input	Keeper
LCD_DATA20	C14	NVCC_LCD	GPIO	ALT5	LCD_DATA20	Input	Keeper
LCD_DATA21	B14	NVCC_LCD	GPIO	ALT5	LCD_DATA21	Input	Keeper
LCD_DATA22	A14	NVCC_LCD	GPIO	ALT5	LCD_DATA22	Input	Keeper
LCD_DATA23	B16	NVCC_LCD	GPIO	ALT5	LCD_DATA23	Input	Keeper

Table 90. 14x14 mm Functional Contact Assignments (continued)

LCD_ENABLE	B8	NVCC_LCD	GPIO	ALT5	LCD_ENABLE	Input	Keeper
LCD_HSYNC	D9	NVCC_LCD	GPIO	ALT5	LCD_HSYNC	Input	Keeper
LCD_RESET	E9	NVCC_LCD	GPIO	ALT5	LCD_RESET	Input	Keeper
LCD_VSYNC	C9	NVCC_LCD	GPIO	ALT5	LCD_VSYNC	Input	Keeper
NAND_ALE	B4	NVCC_NAND	GPIO	ALT5	VDDSOC	Input	Keeper
NAND_CE0_B	C5	NVCC_NAND	GPIO	ALT5	NAND_CE0_B	Input	Keeper
NAND_CE1_B	B5	NVCC_NAND	GPIO	ALT5	NAND_CE1_B	Input	Keeper
NAND_CLE	A4	NVCC_NAND	GPIO	ALT5	NAND_CLE	Input	Keeper
NAND_DATA00	D7	NVCC_NAND	GPIO	ALT5	NAND_DATA00	Input	Keeper
NAND_DATA01	B7	NVCC_NAND	GPIO	ALT5	NAND_DATA01	Input	Keeper
NAND_DATA02	A7	NVCC_NAND	GPIO	ALT5	NAND_DATA02	Input	Keeper
NAND_DATA03	D6	NVCC_NAND	GPIO	ALT5	NAND_DATA03	Input	Keeper
NAND_DATA04	C6	NVCC_NAND	GPIO	ALT5	NAND_DATA04	Input	Keeper
NAND_DATA05	B6	NVCC_NAND	GPIO	ALT5	NAND_DATA05	Input	Keeper
NAND_DATA06	A6	NVCC_NAND	GPIO	ALT5	NAND_DATA06	Input	Keeper
NAND_DATA07	A5	NVCC_NAND	GPIO	ALT5	NAND_DATA07	Input	Keeper
NAND_DQS	E6	NVCC_NAND	GPIO	ALT5	NAND_DQS	Input	Keeper
NAND_RE_B	D8	NVCC_NAND	GPIO	ALT5	NAND_RE_B	Input	Keeper
NAND_READY_B	A3	NVCC_NAND	GPIO	ALT5	NAND_READY_B	Input	Keeper
NAND_WE_B	C8	NVCC_NAND	GPIO	ALT5	NAND_WE_B	Input	Keeper
NAND_WP_B	D5	NVCC_NAND	GPIO	ALT5	NAND_WP_B	Input	Keeper
ONOFF	R8	VDD_SNVS_IN	GPIO	ALT0	ONOFF	Input	100 kΩ pull-up
POR_B	P8	VDD_SNVS_IN	GPIO	ALT0	POR_B	Input	100 kΩ pull-up
RTC_XTALI	T11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALI	—	—
RTC_XTALO	U11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALO	—	—
SD1_CLK	C1	NVCC_SD1	GPIO	ALT5	SD1_CLK	Input	Keeper
SD1_CMD	C2	NVCC_SD1	GPIO	ALT5	SD1_CMD	Input	Keeper
SD1_DATA0	B3	NVCC_SD1	GPIO	ALT5	SD1_DATA0	Input	Keeper
SD1_DATA1	B2	NVCC_SD1	GPIO	ALT5	SD1_DATA1	Input	Keeper
SD1_DATA2	B1	NVCC_SD1	GPIO	ALT5	SD1_DATA2	Input	Keeper
SD1_DATA3	A2	NVCC_SD1	GPIO	ALT5	SD1_DATA3	Input	Keeper
SNVS_PMIC_ON_REQ	T9	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	100 kΩ pull-up

Table 90. 14x14 mm Functional Contact Assignments (continued)

SNVS_TAMPER0	R10	VDD_SNVS_IN	GPIO	—	GPIO5_IO00/SNVS_TAMPER0	Input	Keeper[1]
SNVS_TAMPER1	R9	VDD_SNVS_IN	GPIO	—	GPIO5_IO01/SNVS_TAMPER1	Input	Keeper[1]
SNVS_TAMPER2	P11	VDD_SNVS_IN	GPIO	—	GPIO5_IO02/SNVS_TAMPER2	Input	Keeper[1]
SNVS_TAMPER3	P10	VDD_SNVS_IN	GPIO	—	GPIO5_IO03/SNVS_TAMPER3	Input	Keeper[1]
SNVS_TAMPER4	P9	VDD_SNVS_IN	GPIO	—	GPIO5_IO04/SNVS_TAMPER4	Input	Keeper[1]
SNVS_TAMPER5	N8	VDD_SNVS_IN	GPIO	—	GPIO5_IO05/SNVS_TAMPER5	Input	Keeper[1]
SNVS_TAMPER6	N11	VDD_SNVS_IN	GPIO	—	GPIO5_IO06/SNVS_TAMPER6	Input	Keeper[1]
SNVS_TAMPER7	N10	VDD_SNVS_IN	GPIO	—	GPIO5_IO07/SNVS_TAMPER7	Input	Keeper[1]
SNVS_TAMPER8	N9	VDD_SNVS_IN	GPIO	—	GPIO5_IO08/SNVS_TAMPER8	Input	Keeper[1]
SNVS_TAMPER9	R6	VDD_SNVS_IN	GPIO	—	GPIO5_IO09/SNVS_TAMPER9	Input	Keeper[1]
TEST_MODE	N7	VDD_SNVS_IN	GPIO	ALT0	TEST_MODE	Input	Keeper
UART1_CTS_B	K15	NVCC_UART	GPIO	ALT5	UART1_CTS_B	Input	Keeper
UART1_RTS_B	J14	NVCC_UART	GPIO	ALT5	UART1_RTS_B	Input	Keeper
UART1_RX_DATA	K16	NVCC_UART	GPIO	ALT5	UART1_RX_DATA	Input	Keeper
UART1_TX_DATA	K14	NVCC_UART	GPIO	ALT5	UART1_TX_DATA	Input	Keeper
UART2_CTS_B	J15	NVCC_UART	GPIO	ALT5	UART2_CTS_B	Input	Keeper
UART2_RTS_B	H14	NVCC_UART	GPIO	ALT5	UART2_RTS_B	Input	Keeper
UART2_RX_DATA	J16	NVCC_UART	GPIO	ALT5	UART2_RX_DATA	Input	Keeper
UART2_TX_DATA	J17	NVCC_UART	GPIO	ALT5	UART2_TX_DATA	Input	Keeper
UART3_CTS_B	H15	NVCC_UART	GPIO	ALT5	UART3_CTS_B	Input	Keeper
UART3_RTS_B	G14	NVCC_UART	GPIO	ALT5	UART3_RTS_B	Input	Keeper
UART3_RX_DATA	H16	NVCC_UART	GPIO	ALT5	UART3_RX_DATA	Input	Keeper
UART3_TX_DATA	H17	NVCC_UART	GPIO	ALT5	UART3_TX_DATA	Input	Keeper
UART4_RX_DATA	G16	NVCC_UART	GPIO	ALT5	UART4_RX_DATA	Input	Keeper
UART4_TX_DATA	G17	NVCC_UART	GPIO	ALT5	UART4_TX_DATA	Input	Keeper
UART5_RX_DATA	G13	NVCC_UART	GPIO	ALT5	UART5_RX_DATA	Input	Keeper
UART5_TX_DATA	F17	NVCC_UART	GPIO	ALT5	UART5_TX_DATA	Input	Keeper
USB_OTG1_CHD_B	U16	OPEN DRAIN	GPIO	—	USB_OTG1_CHD_B	—	—

Table 90. 14x14 mm Functional Contact Assignments (continued)

USB_OTG1_DN	T15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DN	—	—
USB_OTG1_DP	U15	VDD_USB_CAP	ANALOG	—	USB_OTG1_DP	—	—
USB_OTG1_VBUS	T12	USB_VBUS	VBUS POWER	—	USB_OTG1_VBUS	—	—
USB_OTG2_DN	T13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DN	—	—
USB_OTG2_DP	U13	VDD_USB_CAP	ANALOG	—	USB_OTG2_DP	—	—
USB_OTG2_VBUS	U12	USB_VBUS	VBUS POWER	—	USB_OTG2_VBUS	—	—
XTALI	T16	NVCC_PLL	ANALOG	—	XTALI	—	—
XTALO	T17	NVCC_PLL	ANALOG	—	XTALO	—	—

[1] SNVS_TAMPER0 to SNVS_TAMPER9 can be configured as GPIO or tamper detection pin, it is depending on the fuse setting TAMPER_PIN_DISABLE[1:0].

6.1.3 14x14 mm, 0.8 mm pitch, ball map

Table 91 shows the 14x14 mm, 0.8 mm pitch ball map for the i.MX 6UltraLite.

Table 91. 14x14 mm, 0.8 mm Pitch, Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS	SD1_DATA3	NAND_READY_B	NAND_CLE	NAND_DATA07	NAND_DATA06	NAND_DATA02	LCD_CLK	LCD_DATA01	LCD_DATA06	LCD_DATA09	LCD_DATA14	LCD_DATA18	LCD_DATA22	ENET2_TX_DATA0	ENET2_TX_DATA1	VSS	A
B	SD1_DATA2	SD1_DATA1	SD1_DATA0	NAND_ALE	NAND_CE1_B	NAND_DATA05	NAND_DATA01	LCD_ENABLE	LCD_DATA00	LCD_DATA05	LCD_DATA08	LCD_DATA13	LCD_DATA17	LCD_DATA21	ENET2_TX_EN	LCD_DATA23	ENET2_RX_EN	B
C	SD1_CLK	SD1_CMD	VSS	NVCC_SD1	NAND_CE0_B	NAND_DATA04	VSS	NAND_WE_B	LCD_VSYNC	LCD_DATA04	VSS	LCD_DATA12	LCD_DATA16	LCD_DATA20	VSS	ENET2_RX_DATA1	ENET2_RX_DATA0	C
D	CSI_DATA07	CSI_DATA06	CSI_DATA05	CSI_DATA04	NAND_WP_B	NAND_DATA03	NAND_DATA00	NAND_RE_B	LCD_HSYNC	LCD_DATA03	LCD_DATA07	LCD_DATA11	LCD_DATA15	LCD_DATA19	ENET1_RX_ER	ENET2_RX_ER	ENET2_TX_CLK	D
E	CSI_DATA03	CSI_DATA02	CSI_DATA01	CSI_DATA00	CSI_PIXCLK	NAND_DQS	NVCC_NAND	VSS	LCD_RESET	LCD_DATA02	VSS	LCD_DATA10	NVCC_LCD	ENET1_TX_DATA1	ENET1_TX_DATA0	ENET1_RX_EN	ENET1_RX_DATA1	E
F	DRAM_ODT1	CSI_VSYNC	CSI_HSYNC	NVCC_CSI	CSI_MCLK	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NVCC_ENET	ENET1_TX_CLK	ENET1_TX_EN	ENET1_RX_DATA0	UART5_TX_DATA	F

Table 91. 14x14 mm, 0.8 mm Pitch, Ball Map (continued)

N	M	L	K	J	H	G
DRAM_ODT0	DRAM_SDBA0	DRAM_ADDR05	DRAM_ADDR02	DRAM_SDWE_B	DRAM_SDBA1	DRAM_ADDR14
DRAM_CS0_B	DRAM_ADDR03	DRAM_ADDR09	DRAM_SDBA2	DRAM_CAS_B	DRAM_ADDR01	DRAM_ADDR06
VSS	DRAM_SDCKE0	VSS	DRAM_ADDR11	DRAM_SDCKE1	DRAM_ADDR13	VSS
DRAM_ZQPAD	DRAM_ADDR10	DRAM_ADDR12	DRAM_ADDR04	DRAM_ADDR08	DRAM_ADDR07	DRAM_RESET
VSS	DRAM_RAS_B	DRAM_ADDR00	DRAM_ADDR15	VSS	DRAM_CS1_B	VSS
NVCC_DRAM_2P5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
TEST_MODE	VSS	VSS	VSS	VSS	VSS	VSS
SNVS_TAMPER5	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER7	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER6	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP	VDD_ARM_CAP
VDD_SNVS_CAP	NGND_KEL0	VSS	VSS	VSS	VSS	VSS
VDD_HIGH_IN	ADC_VREFH	VDDA_ADC_3P3	GPIO1_IO00	NVCC_GPIO	NVCC_UART	UART5_RX_DATA
JTAG_TRST_B	JTAG_TCK	GPIO1_IO02	UART1_TX_DATA	UART1_RTS_B	UART2_RTS_B	UART3_RTS_B
JTAG_TDO	GPIO1_IO09	GPIO1_IO01	UART1_CTS_B	UART2_CTS_B	UART3_CTS_B	VSS
JTAG_TDI	GPIO1_IO04	GPIO1_IO07	UART1_RX_DATA	UART2_RX_DATA	UART3_RX_DATA	UART4_RX_DATA
GPIO1_IO08	GPIO1_IO05	GPIO1_IO03	GPIO1_IO06	UART2_TX_DATA	UART3_TX_DATA	UART4_TX_DATA
N	M	L	K	J	H	G

Table 91. 14x14 mm, 0.8 mm Pitch, Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
U	VSS	DRAM_DATA08	DRAM_DATA09	DRAM_DATA07	DRAM_DATA10	DRAM_DATA01	DRAM_DATA03	DRAM_DATA04	CCM_PMIC_STBY_REQ	BOOT_MODE1	RTC_XTALO	USB_OTG2_VBUS	USB_OTG2_DP	VSS	USB_OTG1_DP	USB_OTG1_CHD_B	VSS	**U**
T	DRAM_SDQS1_P	DRAM_SDQS1_N	DRAM_DQM1	DRAM_DATA00	DRAM_DATA06	DRAM_DATA02	DRAM_DQM0	DRAM_DATA05	SNVS_PMIC_ON_REQ	BOOT_MODE0	RTC_XTALI	USB_OTG1_VBUS	USB_OTG2_DN	VSS	USB_OTG1_DN	XTALI	XTALO	**T**
R	DRAM_DATA15	DRAM_DATA14	VSS	DRAM_DATA11	VSS	SNVS_TAMPER9	VSS	ONOFF	SNVS_TAMPER1	SNVS_TAMPER0	VSS	VDD_USB_CAP	GPANAIO	VDD_HIGH_CAP	VDD_HIGH_CAP	VSS	VSS	**R**
P	DRAM_SDCLK0_P	DRAM_SDCLK0_N	DRAM_DATA13	DRAM_VREF	DRAM_DATA12	DRAM_SDQS0_P	DRAM_SDQS0_N	POR_B	SNVS_TAMPER4	SNVS_TAMPER3	SNVS_TAMPER2	VDD_SNVS_IN	NVCC_PLL	JTAG_TMS	JTAG_MOD	CCM_CLK1_N	CCM_CLK1_P	**P**

6.2 GPIO reset behaviors during reset

Table 92 shows the GPIO behaviors during reset.

Table 92. GPIO Behaviors during Reset [1]

Ball Name	Mux Mode	Function	Input/Output	Value
GPIO01_IO03	ALT7	Reserved	Input	100 kΩ pull-down
UART3_TX_DATA	ALT7	SJC_JTAG_ACT	Output	0
LCD_DATA00	ALT6	SRC_BT_CFG[0]	Input	100 kΩ pull-down
LCD_DATA01	ALT6	SRC_BT_CFG[1]	Input	100 kΩ pull-down
LCD_DATA02	ALT6	SRC_BT_CFG[2]	Input	100 kΩ pull-down
LCD_DATA03	ALT6	SRC_BT_CFG[3]	Input	100 kΩ pull-down
LCD_DATA04	ALT6	SRC_BT_CFG[4]	Input	100 kΩ pull-down

Table 92. GPIO Behaviors during Reset (continued)[1]

Ball Name	Mux Mode	Function	Input/Output	Value
LCD_DATA05	ALT6	SRC_BT_CFG[5]	Input	100 kΩ pull-down
LCD_DATA06	ALT6	SRC_BT_CFG[6]	Input	100 kΩ pull-down
LCD_DATA07	ALT6	SRC_BT_CFG[7]	Input	100 kΩ pull-down
LCD_DATA08	ALT6	SRC_BT_CFG[8]	Input	100 kΩ pull-down
LCD_DATA09	ALT6	SRC_BT_CFG[9]	Input	100 kΩ pull-down
LCD_DATA10	ALT6	SRC_BT_CFG[10]	Input	100 kΩ pull-down
LCD_DATA11	ALT6	SRC_BT_CFG[11]	Input	100 kΩ pull-down
LCD_DATA12	ALT6	SRC_BT_CFG[12]	Input	100 kΩ pull-down
LCD_DATA13	ALT6	SRC_BT_CFG[13]	Input	100 kΩ pull-down
LCD_DATA14	ALT6	SRC_BT_CFG[14]	Input	100 kΩ pull-down
LCD_DATA15	ALT6	SRC_BT_CFG[15]	Input	100 kΩ pull-down
LCD_DATA16	ALT6	SRC_BT_CFG[16]	Input	100 kΩ pull-down
LCD_DATA17	ALT6	SRC_BT_CFG[17]	Input	100 kΩ pull-down
LCD_DATA18	ALT6	SRC_BT_CFG[18]	Input	100 kΩ pull-down
LCD_DATA19	ALT6	SRC_BT_CFG[19]	Input	100 kΩ pull-down
LCD_DATA20	ALT6	SRC_BT_CFG[20]	Input	100 kΩ pull-down
LCD_DATA21	ALT6	SRC_BT_CFG[21]	Input	100 kΩ pull-down
LCD_DATA22	ALT6	SRC_BT_CFG[22]	Input	100 kΩ pull-down
LCD_DATA23	ALT6	SRC_BT_CFG[23]	Input	100 kΩ pull-down

[1] Others are same as value in the column “Out of Reset Condition” of Table 90.

7 Revision history

Table 93 provides a revision history for this data sheet.

Table 93. i.MX 6UltraLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
0	01/2016	• Initial release
0.1	02/2016	• Updated Figure 1 Part Number Nomenclature—i.MX 6UltraLite • Updated Table 1 Ordering Information • Updated Table 3 i.MX 6UltraLite Modules List
1	04/2016	• Updated Table 3 i.MX 6UltraLite Module list for BCH descriptions • Updated Table 4 Special Signal Considerations • Added a note for Table 9 14x14 MM Package Thermal Resistance • Updated Table 14 Low Power Mode Current and Power Consumption • Added a note for Table 22 XTALI and RTC_XTALI DC Parameters • Updated Table 37 EIM Internal Module Multiplexing • Updated Table 50 SDR50/SDR104 Interface Timing Specification • Updated Table 90 14x14 mm Functional Contact Assignments and footnote • Updated Section 4.1.1, “Absolute maximum ratings" • Updated Section 4.6.3, “DDR I/O DC parameters" • Added Section 4.12.8, “LCD Controller (LCDIF) parameters" • Updated Section 4.12.9, “QUAD SPI (QSPI) timing parameters"
2	02/2017	• Updated Table 8, "Absolute Maximum Ratings" • Updated and added a footnote Table 10, "Operating Ranges" • Updated Section 4.2.1, “Power-Up sequence" and Section 4.2.2, “Power-Down sequence" • Removed Section 4.9.4 DDR SDRAM Specific Parameters (DDR3 and LPDDR2) • Updated Figure 18, "Asynchronous A/D Muxed Write Access" • Added a new Section 4.10, “Multi-Mode DDR Controller (MMDC)" • Added a new Section 4.12.8.1, “LCDIF signal mapping" • Updated Table 50, "SDR50/SDR104 Interface Timing Specification" • Updated Figure 40, "HS200 Mode Timing" • Updated Table 51, "HS200 Interface Timing Specification"
2.1	03/2017	• Updated the silicon revision definition in the Figure 1, "Part Number Nomenclature—i.MX 6UltraLite" • Added Rev.1.2 part numbers in the Table 1, "Ordering Information"
2.2	05/2017	• Changed terminology from “floating” to “not connected” • Added a footnote regarding maximum voltage allowance in the Table 8, "Absolute Maximum Ratings" • Replaced the MMDC compatible information with a cross reference in the Section 4.6.3, “DDR I/O DC parameters" and Section 4.7.2, “DDR I/O AC parameters" • Changed SD3 min to 1.7 ns in the Table 50, "SDR50/SDR104 Interface Timing Specification"

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