FS2400_SDS

Fail-safe system basis chip with SMPS and LDO, CAN FD transceiver Rev. 1 — 30 January 2024 Product short of

Product short data sheet



Document information

Information	Content
Keywords	Fail-safe system basis chip, SMPS, LDO, CAN FD transceiver, ultra-wide band (UWB), Near Field Communication (NFC), Bluetooth Low Energy (BLE) devices, small applications, low power
Abstract	The FS2400 is a family of automotive safety system basis chip devices with multiple power supplies designed to support secure car-access applications while maintaining flexibility to fit other small applications requiring low power and CAN FD communication.



1 General description

FS2400 is a family of automotive safety system basis chip (SBC) devices with multiple power supplies designed to support secure car access application using ultra-wide band (UWB), near-field communication (NFC), and Bluetooth Low Energy (BLE) devices. The FS2400 can also fit other small applications requiring low power and CAN FD communication.

This family of devices supports a wide range of applications, offering a choice of output voltage settings, physical interface, integrated system-level features to address low-power and noise-sensitive applications with automotive safety integrity levels (ASIL) up to ASIL B.

The FS2400 integrates a battery-connected switched-mode regulator (V1) and a battery-connected linear regulator (V3) to supply microcontroller, communication devices, and others. V1 offers a high-performance switching regulator capable of operating in Pulse Frequency Modulation (PFM) mode and Force Pulse Width Modulation (FPWM) mode. The mode of operation can be changed using wake pins to optimize noise management.

The FS2400 is developed in compliance with the ISO 26262:2018 standard. It includes enhanced safety features, with fail-safe output, becoming part of a full safety-oriented system, covering ASIL B safety integrity level.

The FS2400 is offered in a 5 mm x 5 mm, 32-Ld HVQFN package with wettable flanks.

2 Features and benefits

Operating range

- 40 V DC maximum input voltage
- Low-power off mode with low sleep current and multiple wake-up sources
- Low-power on mode with HVBUCK (V1) active, HVLDO (V3) selectable by OTP and multiple wake-up sources

Power supplies

- V1: High-voltage synchronous buck converter with integrated FETs. Configurable output voltage (1.9 V to 5 V) and switching frequency, output DC current capability up to 400 mA and PFM mode for Low-power on mode operation
- V3: High-voltage LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V or 5 V and up to 150 mA current capability

System support

- One CAN FD supporting up to 5 Mbps communication following ISO 11898-2:2016 and SAE J2284 standards
- Four wake-up inputs (40 V capable): WAKEx pins, HVIO1 pin, CAN FD or SPI command
- · Hardware ID detection capability
- One high-voltage I/O with wake-up capability (40 V capable): HVIO1
- · Device control via 32 bits SPI interface, with CRC
- Integrated long duration timer (LDT) for system shutdown and wake-up control, programmable up to 194 days
- 12-channel analog multiplexer (AMUX) for system monitoring (temperature, battery voltage, internal voltages)

Functional safety

- Developed following ISO 26262:2018 standard to fit for ASIL B applications
- · Internal monitoring circuitry with its own reference
- · Additional input for external voltage monitoring
- · Window or timeout watchdog function to monitor the MCU software failure
- · Analog built-in self-test (ABIST) on demand
- Safety outputs (RSTB, LIMP0)
- Safety input to monitor external IC state (ERRMON)

Configuration and enablement

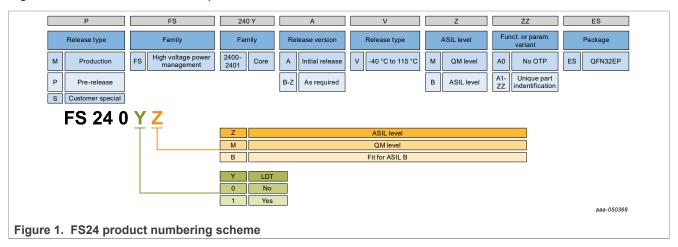
- HVQFN32EP: QFN, 32 pins with exposed pad for optimized thermal management, wettable flanks, 5 mm x 5 mm x 0.85 mm, 0.5 mm pitch
- Permanent device customization via one time programmable (OTP) fuse memory
- OTP emulation mode for system development and evaluation

3 Ordering information

This section describes the part numbers available to be purchased along with their main differences. It also describes how the part number reference is built.

3.1 Part numbers definition

Figure 1 describes how the FS24 part numbers are built.



3.2 Part numbers list

Table 1. Device segmentation

Generic part number	Description	Fit for ASIL	LDT	RSTB	LIMP0	VMON (1, 3)	VMON_EXT (VMON0)	Watchdog	Cyclic INIT CRC check	RSTB 8 sec timer	ABIST	Package
FS2400M ^[1]	QM without LDT	QM	No	Yes	Option	Yes	No	Option	No	No	No	HVQFN32
FS2401M ^[1]	QM with LDT	QM	Yes	Yes	Option	Yes	No	Option	No	No	No	HVQFN32
FS2400B ^[1]	ASIL B without LDT	В	No	Yes	Option	Yes	Option	Yes	Yes	Yes	Yes	HVQFN32
FS2401B ^[1]	ASIL B with LDT	В	Yes	Yes	Option	Yes	Option	Yes	Yes	Yes	Yes	HVQFN32

^[1] Exact orderable part numbers are defined in Table 2.

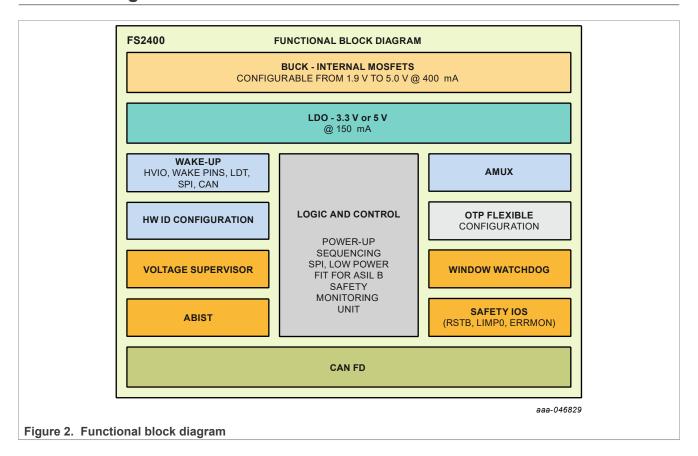
Table 2. Orderable part numbers

Part number ^[1]	Description	Package
MFS2400AVMA0ES ^[2]	Superset covering FS2400M devices.	
MFS2401AVMA0ES ^[2]	Superset covering FS24001M devices.	
MFS2400AVBA0ES ^[2]	Superset covering FS2400B devices.	
MFS2401AVBA0ES ^[2]	Superset covering FS2401B devices.	HVQFN32EP
MFS2400AVMA1ES	Configuration given as an example for Ranger 5 attach, V1 at 3.3 V and V3 at 5 V. QM, LDT disabled.	
MFS2401AVBA1ES	Configuration given as an example for Ranger 5 attach, V1 at 3.3 V and V3 at 5 V. ASIL B, LDT enabled.	
MFS2401AVMAFES	Configuration given as an example for S32K1xx + NCF3321 attach, V1 at 5 V and V3 at 3.3 V. QM, LDT enabled.	

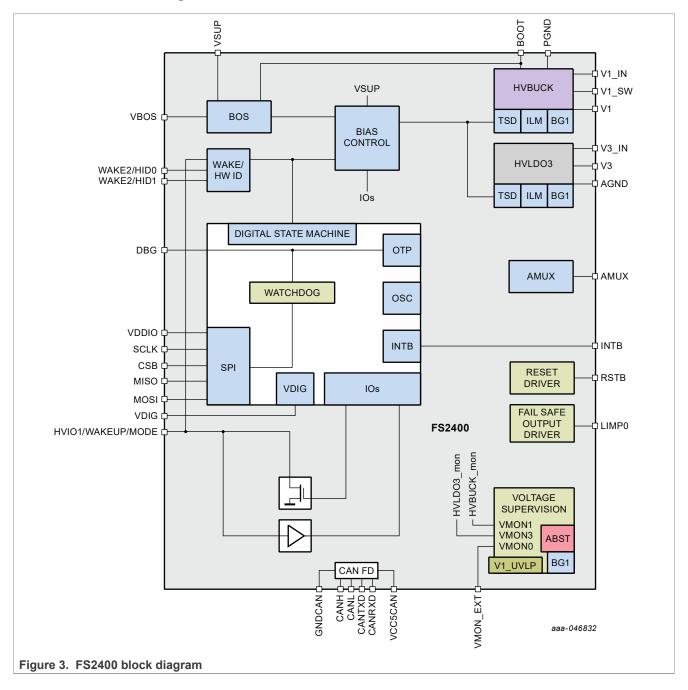
To order parts in tape and reel, add the R2 suffix to the full part number reference.

A0 parts are non-programmed OTP configurations. Preprogrammed OTP configurations are managed through part number extension. For a custom OTP configuration, contact a local NXP sales representative.

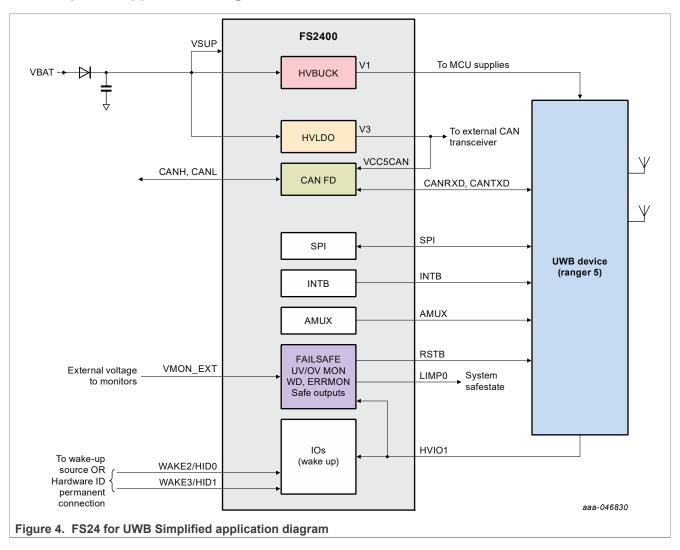
4 Block diagram

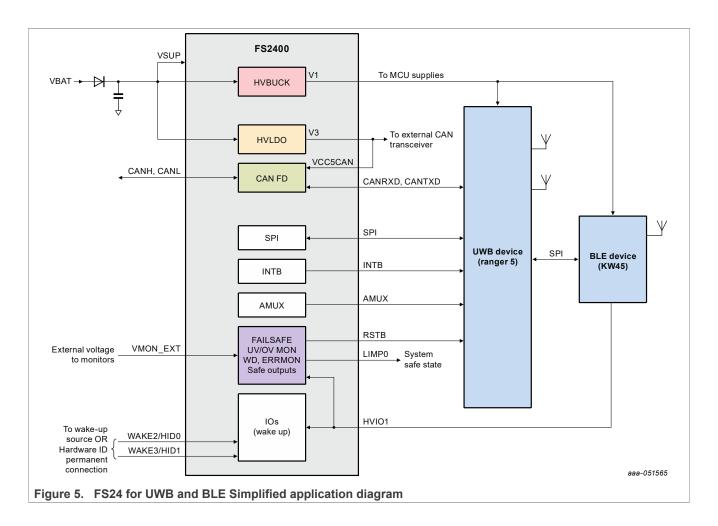


4.1 Internal block diagram



4.2 Simplified application diagram





5 Limiting values

Minimum and maximum ratings

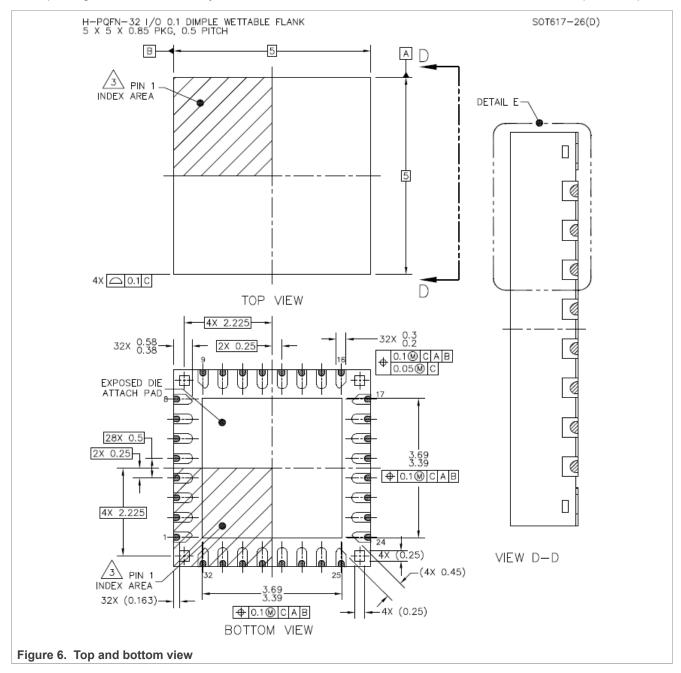
Table 3. Limiting values

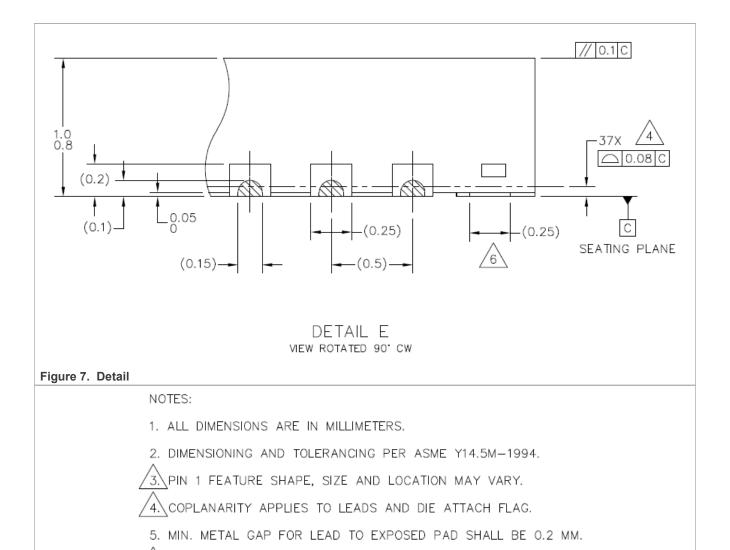
 T_A = -40 °C to 115 °C, unless otherwise specified. VSUP = 5.5 V to 40 V, unless otherwise specified. VDDIO = 1.8 V to 5 V, unless otherwise specified. All voltages referenced to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings		1		
WAKE2/HID0, WAKE3/HID1, LIMP0, HVIO1	Global pins	-0.3	40	V
V1_IN, VSUP, V3_IN	Global supply input pins	-1	40	V
CANH, CANL	Global communication pins	-33	40	V
воот	High-voltage pin/local pin	-0.3	45	V
V1_SW, VMON_EXT	High-voltage pins/local pins	-0.3	40	V
DEBUG	Debug pin to enter in Debug mode; should be grounded in the application	-0.3	10	V
V1,V3, VCC5CAN	Local pins	-0.3	5.6	V
VDDIO, VBOS, AMUX	Local pins	-0.3	5.5	V
CANRXD, CANTXD, MISO, MOSI, SCK, CSB, RSTB, INTB	Local pins	-0.3	VDDIO + 0.3	V
VDIG	Local pin	-0.3	2	V
GND_IO, PGND, GNDCAN	Ground pins	-0.3	0.3	V

6 Package outline

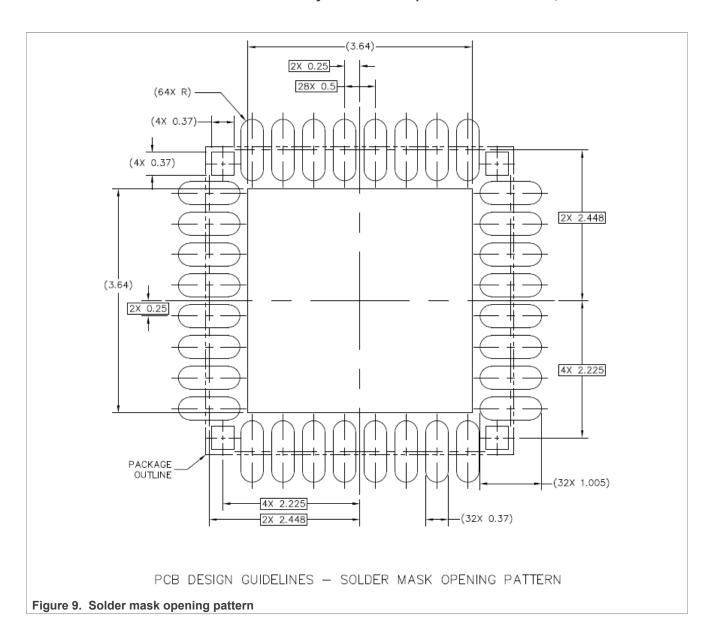
FS24 package is a QFN, thermally enhanced, wettable flanks, 5 mm x 5 mm x 0.85 mm, 0.5 mm pitch, 32 pins.

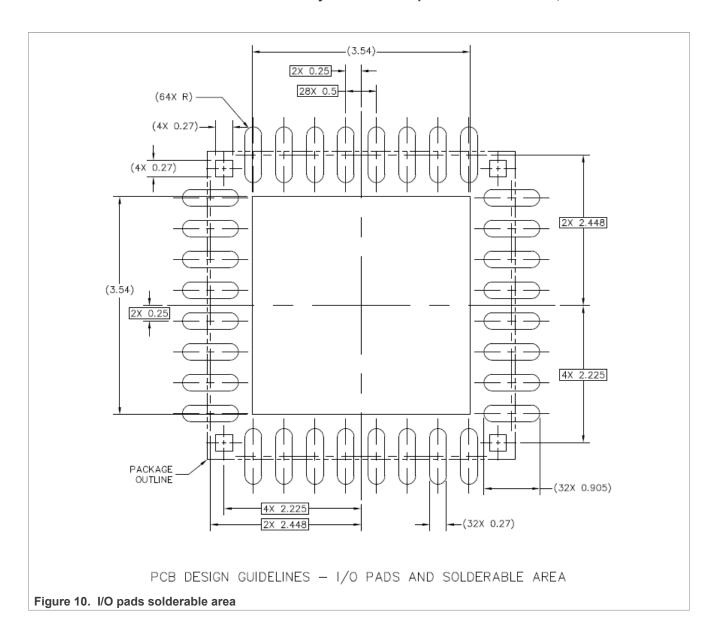


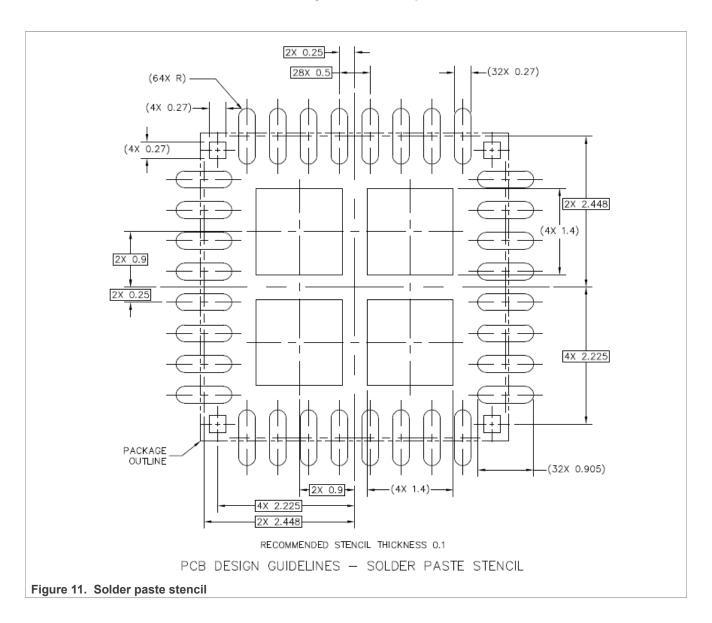


ANCHORING PADS.

Figure 8. Notes







FS2400_SDS

Fail-safe system basis chip with SMPS and LDO, CAN FD transceiver

7 Revision history

Table 4. Revision history

Document ID	Release date	Description
FS2400_SDS v.1.0	30 January 2024	Initial version

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Fail-safe system basis chip with SMPS and LDO, CAN FD transceiver

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