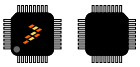
# Kinetis KE1xZ with up to 64 KB Flash

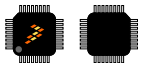
**Up to 48 MHz Arm® Cortex®-M0+ Based Microcontroller**

Providing up to 64 KB flash, up to 8 KB RAM, and a complete set of analog/digital features, KE1xZ64 offers a robust Touch Sense Interface (TSI) and CAN bus for industrial networking, which provides high-level stability and accuracy in customer's home appliance touch UI and industrial control systems.

**MKE1xZ64VLF4**
**MKE1xZ64VLD4**
**MKE1xZ64VFP4**
**MKE1xZ32VLF4**
**MKE1xZ32VLD4**
**MKE1xZ32VFP4**



48 LQFP (LF)
7x7x1.4 mm P 0.5



44 LQFP (LD)
10x10x1.4 mm P 0.8

40 QFN (FP)
5x5x0.85 mm P 0.4

**Core Processor and System**

- Arm® Cortex®-M0+ core, supports up to 48 MHz frequency
- Arm Core based on the ARMv6 Architecture and Thumb®-2 ISA
- Configurable Nested Vectored Interrupt Controller (NVIC)
- Memory-Mapped Divide and Square Root module (MMDVSQ)

**Reliability, safety and security**

- Cyclic Redundancy Check (CRC) generator module
- 128-bit unique identification (ID) number
- Internal watchdog (WDOG) with independent clock source
- External watchdog monitor (EWM) module
- ADC self calibration feature
- On-chip clock loss monitoring

**Power management**

- Low-power Arm Cortex-M0+ core with excellent energy efficiency
- Power management controller (PMC) with multiple power modes: Run, Wait, Stop, VLPR, VLPW and VLPS

**Memory and memory interfaces**

- Up to 64 KB program flash
- Up to 8 KB SRAM
- 64 Bytes flash cache

**Mixed-signal analog**

- 1× 12-bit analog-to-digital converter (ADC) with up to 16 channel analog inputs per module, up to 1 Msps
- 1× high-speed analog comparators (CMP) with internal 8-bit digital to analog converter (DAC)

**Timing and control**

- 2× Flex Timers (FTM) for PWM generation, offering 6ch+2ch
- 1× 16-bit Low-Power Timer (LPTMR) with flexible wake up control
- 1× Programmable Delay Block (PDB) with flexible trigger system
- 1× 32-bit Low-power Periodic Interrupt Timer (LPIT) with 2 independent channels
- Real timer clock (RTC)

**Debug functionality**

- Serial Wire Debug (SWD) debug interface
- Debug Watchpoint and Trace (DWT)
- Micro Trace Buffer (MTB)

- Supports clock gating for unused modules, and specific peripherals remain working in low power modes
- POR, LVD/LVR

**Clock interfaces**

- OSC: high range 4 - 40 MHz (with low power or high-gain mode) and low range 32 - 40 kHz (with high-gain mode only)
- 48 MHz high-accuracy (up to ±1%) fast internal reference clock (FIRC) for normal Run
- 8 MHz / 2 MHz high-accuracy (up to ±3%) slow internal reference clock (SIRC) for low-speed Run
- 128 kHz low power oscillator (LPO)
- Low-power FLL (LPFLL)
- Up to 50 MHz DC external square wave input clock
- System clock generator (SCG)
- Real time counter (RTC)

**Human-machine interface (HMI)**

- Supports up to 32 interrupt request (IRQ) sources
- Up to 42 GPIO pins with interrupt functionality
- Touch sensing input (TSI) module

**Connectivity and communications interfaces**

- 3× low-power universal asynchronous receiver/transmitter (LPUART) modules with FIFO support and low power availability
- 1× low-power serial peripheral interface (LPSPI) modules with FIFO support and low power availability
- 1× low-power inter-integrated circuit (LPI2C) modules with FIFO support and low power availability
- 1× CAN module (MSCAN), with 5 Rx buffers and 3 Tx buffers

**Operating Characteristics**

- Voltage range: 2.7 to 5.5 V
- Ambient temperature range: –40 to 105 °C

## Related Resources

| Type | Description | Resource |
|---|---|---|
| Fact Sheet | The Fact Sheet gives overview of the product key features and its uses. | KE1xZ Family Fact Sheet |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. | KE1xZ64PB[1] |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KE1xZP48M48SF0RM [1] |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | This document:<br>KE1xZP48M48SF0 |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | Kinetis_E_0N16X [1] |
| Package drawing | Package dimensions are provided in package drawings. | 48-LQFP: 98ASH00962A<br>44-LQFP: 98ASS23225W<br>40-QFN: 98ASA01371D |

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

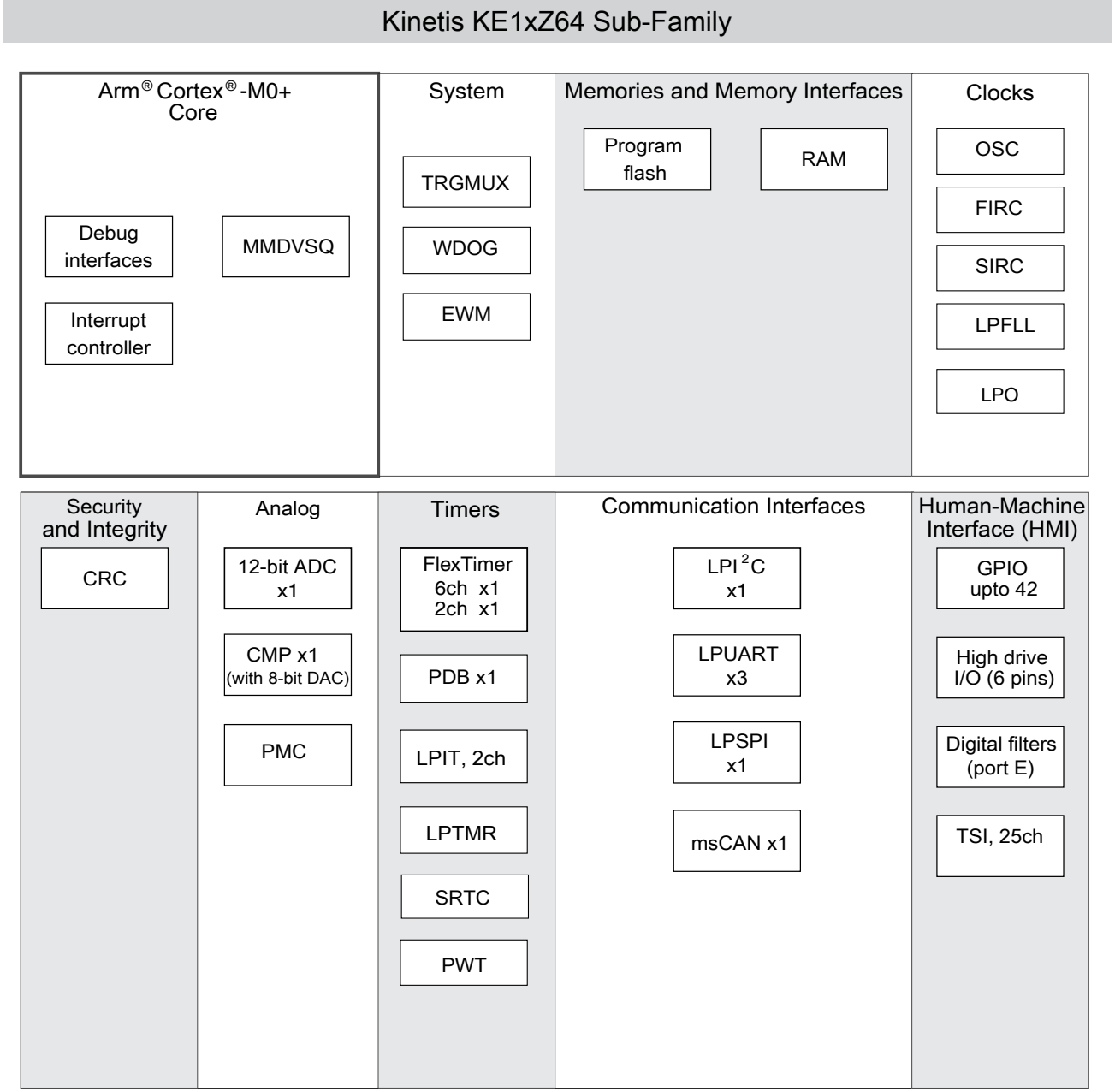



**Figure 1. Functional block diagram**

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# 1 Ordering information

The following chips are available for ordering.

**Table 1. Ordering information**

| Product | Memory | | Package | | IO and ADC channel | | | HMI | Communication |
|---|---|---|---|---|---|---|---|---|---|
| Part number | Flash (KB) | SRAM (KB) | Pin count | Package | GPIOs | GPIOs (INT/HD)[1] | ADC channels | TSI | CAN |
| MKE16Z64VLF4 | 64 | 8 | 48 | LQFP | 42 | 42/6 | 12 | Yes | Yes |
| MKE16Z64VLD4 | 64 | 8 | 44 | LQFP | 38 | 38/6 | 12 | Yes | Yes |
| MKE15Z64VLF4 | 64 | 8 | 48 | LQFP | 42 | 42/6 | 12 | Yes | No |
| MKE15Z64VLD4 | 64 | 8 | 44 | LQFP | 38 | 38/6 | 12 | Yes | No |
| MKE14Z64VLF4 | 64 | 8 | 48 | LQFP | 42 | 42/6 | 12 | No | No |
| MKE14Z64VLD4 | 64 | 8 | 44 | LQFP | 38 | 38/6 | 12 | No | No |
| MKE16Z32VLF4 | 32 | 4 | 48 | LQFP | 42 | 42/6 | 12 | Yes | Yes |
| MKE16Z32VLD4 | 32 | 4 | 44 | LQFP | 38 | 38/6 | 12 | Yes | Yes |
| MKE15Z32VLF4 | 32 | 4 | 48 | LQFP | 42 | 42/6 | 12 | Yes | No |
| MKE15Z32VLD4 | 32 | 4 | 44 | LQFP | 38 | 38/6 | 12 | Yes | No |
| MKE14Z32VLF4 | 32 | 4 | 48 | LQFP | 42 | 42/6 | 12 | No | No |
| MKE14Z32VLD4 | 32 | 4 | 44 | LQFP | 38 | 38/6 | 12 | No | No |
| MKE15Z64VFP4 | 64 | 8 | 40 | QFN | 36 | 36/4 | 11 | Yes | No |
| MKE14Z64VFP4 | 64 | 8 | 40 | QFN | 36 | 36/4 | 11 | No | No |
| MKE15Z32VFP4 | 32 | 4 | 40 | QFN | 36 | 36/4 | 11 | Yes | No |
| MKE14Z32VFP4 | 32 | 4 | 40 | QFN | 36 | 36/4 | 11 | No | No |

1. INT: interrupt pin numbers; HD: high drive pin numbers

# 2 Overview

The following figure shows the system diagram of this device.

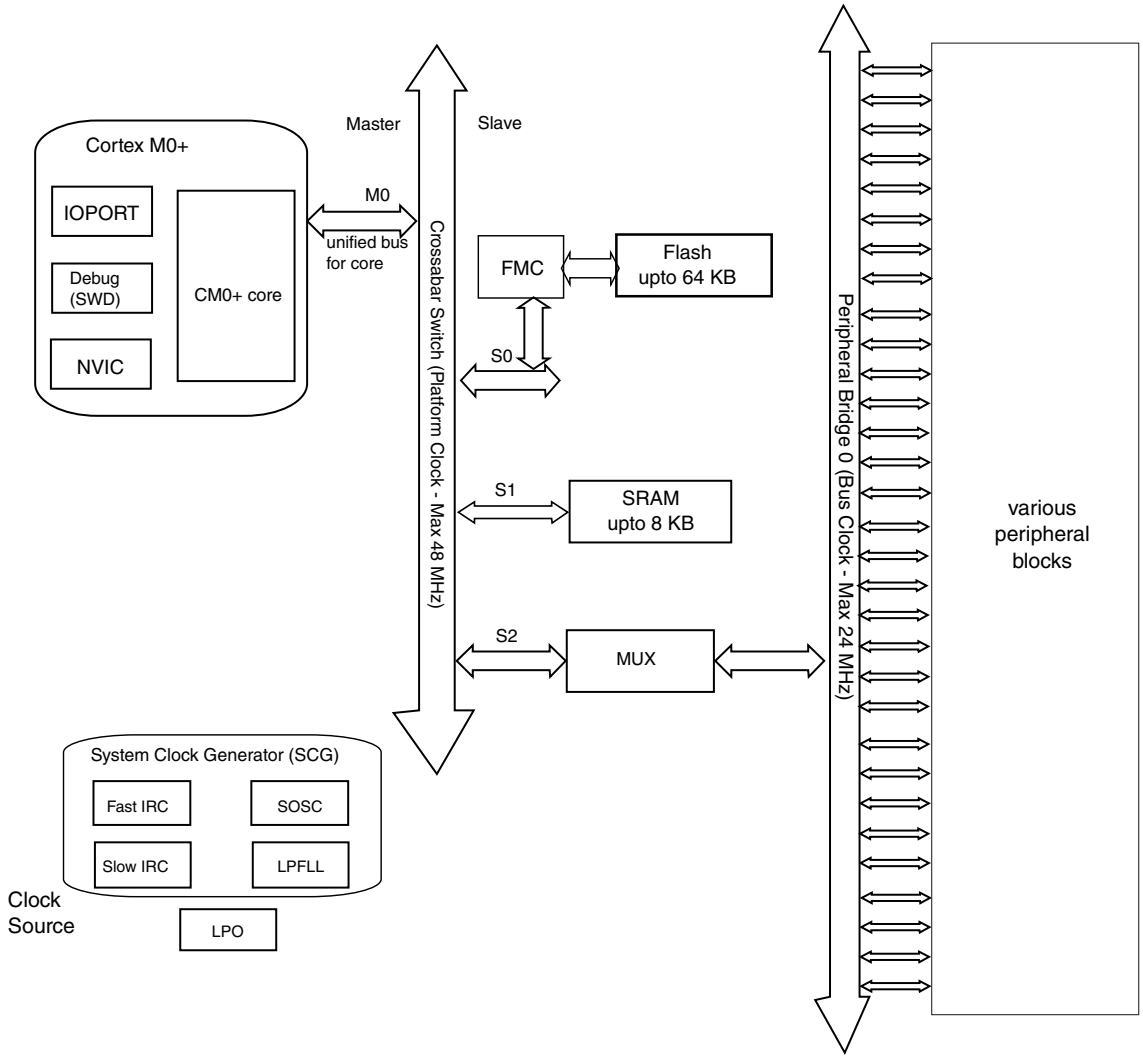



**Figure 2. System diagram**

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

## 2.1 System features

The following sections describe the high-level system features.

### 2.1.1 ARM Cortex-M0+ core

The enhanced ARM Cortex M0+ is the member of the Cortex-M Series of processors targeting microcontroller cores focused on very cost sensitive, low power applications. It has a single 32-bit AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality including support for simple program trace capability. The processor supports the ARMv6-M instruction set (Thumb) architecture including all but three 16-bit Thumb opcodes (52 total) plus seven 32-bit instructions. It is upward compatible with other Cortex-M profile processors.

### 2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 4 priority levels for interrupts. In the NVIC, each source in the IPR registers contains 2 bits. It also differs in number of interrupt sources and supports 32 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency to up to 15 clock cycles for Cortex-M0+. It also can be used to wake the MCU core from Wait and VLPW modes.

### 2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Partial Stop, Stop and VLPS modes.

Wake-up sources for this SoC are listed as below:

**Table 2. AWIC Stop and VLPS Wake-up Sources**

| Wake-up source | Description |
|---|---|
| Available system resets | RESET pin, WDOG , loss of clock(LOC) reset and loss of lock (LOL) reset |
| Pin interrupts | Port Control Module - Any enabled pin interrupt is capable of waking the system |
| ADCx | ADCx is optional functional with clock source from SIRC or OSC |
| CMPx | Functional in Stop/VLPS modes with clock source from SIRC or OSC |
| LPI2C | Functional in Stop/VLPS modes with clock source from SIRC or OSC |
| LPUART | Functional in Stop/VLPS modes with clock source from SIRC or OSC |

*Table continues on the next page...*

**Table 2. AWIC Stop and VLPS Wake-up Sources (continued)**

| Wake-up source | Description |
|---|---|
| LPSPI | Functional in Stop/VLPS modes with clock source from SIRC or OSC |
| LPIT | Functional in Stop/VLPS modes with clock source from SIRC or OSC |
| LPTMR | Functional in Stop/VLPS modes |
| RTC | Functional in Stop/VLPS modes |
| SCG | Functional in Stop mode (Only SIRC) |
| CAN | CAN stop wakeup |
| TSI | Touch sense wakeup |
| NMI | Non-maskable interrupt |

### 2.1.4 Memory

This device has the following features:

- Upto 64 KB of embedded program flash memory.
- Upto 8 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 1 KB.

  The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

  The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

### 2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

**NOTE**

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

**Table 3. Reset source**

| Reset sources | Descriptions | Modules | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | PMC | SIM | SMC | RCM | Reset pin is negated | WDOG | SCG | RTC | LPTMR | Others |
| POR reset | Power-on reset (POR) | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| System resets | Low-voltage detect (LVD) | Y[1] | Y | Y | Y | Y | Y | Y | N | Y | Y |
| | External pin reset ($\overline{\text{RESET}}$) | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |
| | Watchdog (WDOG) reset | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |
| | Multipurpose clock generator loss of clock (LOC) reset | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |
| | Multipurpose clock generator loss of lock (LOL) reset | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |
| | Stop mode acknowledge error (SACKERR) | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |
| | Software reset (SW) | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |
| | Lockup reset (LOCKUP) | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |
| | MDM DAP system reset | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |
| Debug reset | Debug reset | Y[1] | Y[2] | Y[3] | Y[4] | Y | Y[5] | Y[6] | N | N | Y |

1. Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
2. Except SIM_SOPT1
3. Except SMC_PMPROT, SMC_PMCTRL_RUM, SMC_PMCTRL_STOPM, SMC_STOPCTRL, SMC_PMSTAT
4. Except RCM_RPC, RCM_MR, RCM_FM, RCM_SRIE, RCM_SRS, RCM_SSRS
5. Except WDOG_CS[TST]
6. Except SCG_CSR and SCG_FIRCSTAT

This device supports booting from:

- internal flash

## 2.1.6 Clock options

The SCG module controls which clock source is used to derive the system clocks. The clock generation logic divides the selected clock source into a variety of clock domains, including the clocks for the system bus masters, system bus slaves, and flash memory . The clock generation logic also implements module-specific clock gating to allow granular shutoff of modules.

The following figure is a high level block diagram of the clock generation. For more details on the clock operation and configuration, see the Clocking chapter in the Reference Manual.

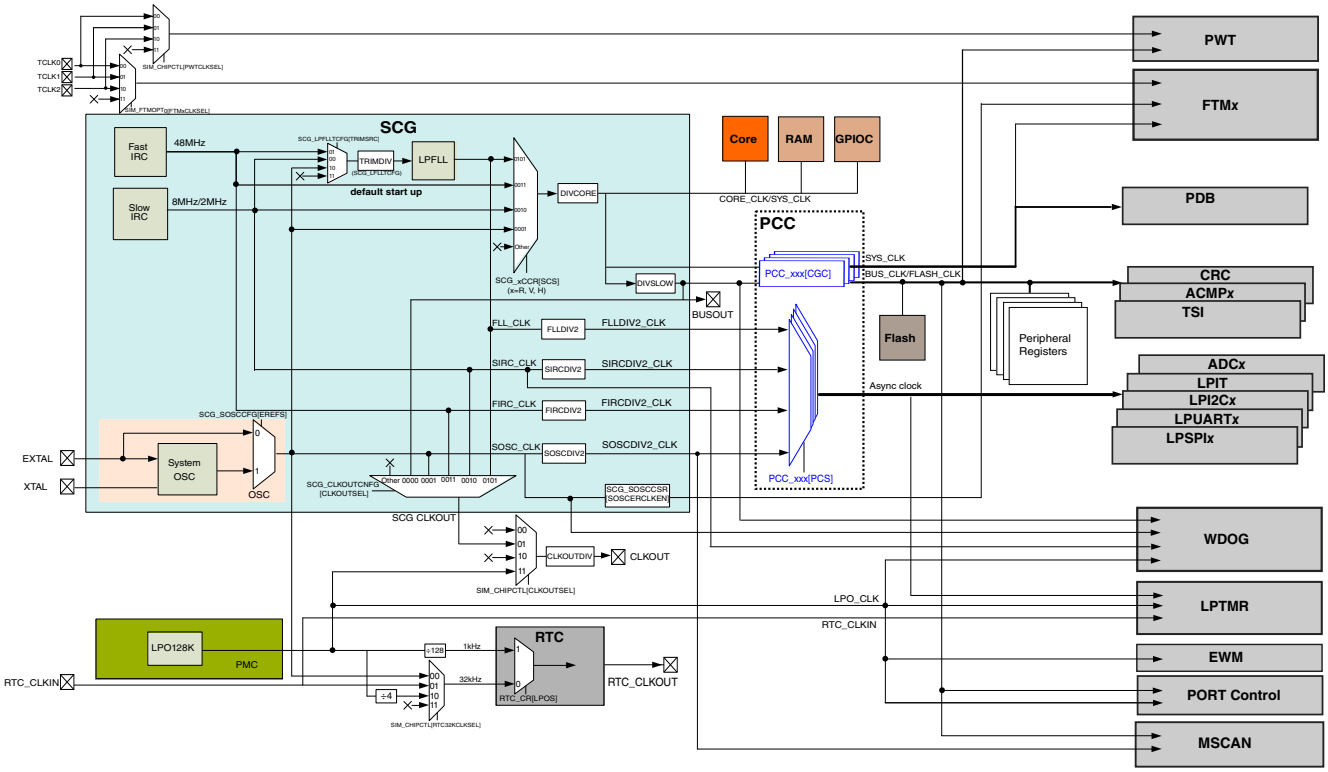



**Figure 3. Clocking block diagram**

## 2.1.7 Security

Security state can be enabled via programming flash configure field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU.

| External interface | Security | Unsecure |
|---|---|---|
| SWD port | Can't access memory source by SWD interface | the debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command |

### 2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex® User Guide.

The PMC provides Normal Run (RUN), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

**Table 5. Peripherals states in different operational modes**

| Core mode | Device mode | Descriptions |
|---|---|---|
| Run mode | | |

*Table continues on the next page...*

**Table 5. Peripherals states in different operational modes (continued)**

| Core mode | Device mode | Descriptions |
|---|---|---|
| | Run | In Run mode, all device modules are operational. |
| | Very Low Power Run | In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. |
| Sleep mode | Wait | In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode. |
| | Very Low Power Wait | In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode. |
| Deep sleep | Stop | In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, CMP, LPTMR, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt. |
| | Very Low Power Stop | In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, LPIT, FlexIO, LPUART, LPI2C,LPSPI, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt. |

**NOTE**

When the MCU is in HSRUN or VLP mode, user cannot write FlexRAM (EEPROM), and cannot launch an FTFE command including flash programming/erasing.

### 2.1.9 Debug controller

This device has extensive debug capabilities including run control and tracing capabilities. The standard ARM debug port supports SWD interface.

## 2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

### 2.2.1 FTM

This device contains two FlexTimer modules.

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

Several key enhancements of this module are made:
- Signed up counter
- Deadtime insertion hardware
- Fault control inputs
- Enhanced triggering functionality
- Initialization and polarity control

### 2.2.2 ADC

This device contains one 12-bit SAR ADC modules. The ADC module supports hardware triggers from FTM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:
- Linear successive approximation algorithm with up to 12-bit resolution
- Up to 12 single-ended external analog inputs
- Support 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable Voltage reference: from external or alternate
- Self-Calibration mode

#### 2.2.2.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see ADC electrical characteristics for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

### 2.2.3 CMP

There are one analog comparators on this device.

- Each CMP has its own independent 8-bit DAC.
- Each CMP supports up to 6 analog inputs from external pins.
- Each CMP is able to convert an internal reference from the bandgap.
- Each CMP supports the round-robin sampling scheme. In summary, this allow the CMP to operate independently in VLPS and Stop modes, whilst being triggered periodically to sample up to 8 inputs. Only if an input changes state is a full wakeup generated.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising and falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, windowed, or digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: Shorter propagation delay at the expense of higher power, and Low power with longer propagation delay
- Functional in all power modes available on this MCU
- The window and filter functions are not available in STOP mode
- Integrated 8-bit DAC with selectable supply reference source and can be power down to conserve power

### 2.2.4 RTC

The RTC is an always powered-on block that remains active in all low power modes.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm

- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt

### 2.2.5 LPIT

The Low Power Periodic Interrupt Timer (LPIT) is a multi-channel timer module generating independent pre-trigger and trigger outputs. These timer channels can operate individually or can be chained together. The LPIT can operate in low power modes if configured to do so. The pre-trigger and trigger outputs can be used to trigger other modules on the device.

### 2.2.6 PDB

The Programmable Delay Block (PDB) provides controllable delays from either an internal or an external trigger, or a programmable interval tick, to the hardware trigger inputs of ADCs and/or generates the interval triggers to DACs, so that the precise timing between ADC conversions and/or DAC updates can be achieved. The PDB can optionally provide pulse outputs (Pulse-Out's) that are used as the sample window in the CMP block.

The PDB module has the following capabilities:

- trigger input sources and one software trigger source
- 1 DAC refresh trigger output, for this device
- configurable PDB channels for ADC hardware trigger
- 1 pulse output, for this device

### 2.2.7 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare

    - Optional interrupt can generate asynchronous wakeup from any low-power mode
    - Hardware trigger output
    - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

### 2.2.8 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

### 2.2.9 LPUART

This product contains three Low-Power UART modules, and can work in Stop and VLPS modes. The module also supports 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×
- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods

    - Idle line wakeup
    - Address mark wakeup
    - Receive data match
- Automatic address matching to reduce ISR overhead:
    - Address mark matching
    - Idle line address matching
    - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

### 2.2.10 LPSPI

This device contains one LPSPI modules. The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave. The LPSPI can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses.

The LPSPI modules have the following features:

- Command/transmit FIFO of 4 words
- Receive FIFO of 4 words
- Host request input can be used to control the start time of an SPI bus transfer

### 2.2.11 LPI2C

This device contains one LPI2C modules. The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master and/or a slave. The LPI2C can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses. The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation. The LPI2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

The LPI2C modules have the following features:

- Standard, Fast, Fast+ and Ultra Fast modes are supported
- HS-mode supported in slave mode

- Multi-master support including synchronization and arbitration
- Clock stretching
- General call, 7-bit and 10-bit addressing
- Software reset, START byte and Device ID require software support
- For master mode:
  - command/transmit FIFO of 4 words
  - receive FIFO of 4 words
- For slave mode:
  - separate I2C slave registers to minimize software overhead due to master/slave switching
  - support for 7-bit or 10-bit addressing, address range, SMBus alert and general call address
  - transmit/receive data register supporting interrupt requests

### 2.2.12 Modular/Scalable Controller Area Network (MSCAN)

This device contains one CAN module. It uses the MSCAN mudule which is a communication controller implementing the CAN 2.0A/B protocol as defined in the Bosch specification dated September 1991.

Its 5 Rx buffers and 3 Tx buffers are adaptable to target CAN applications.

The MSCAN module has the following features :

- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbit/s
- Support for remote frames
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Low power modes, with programmable wakeup on bus activity

### 2.2.13 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.

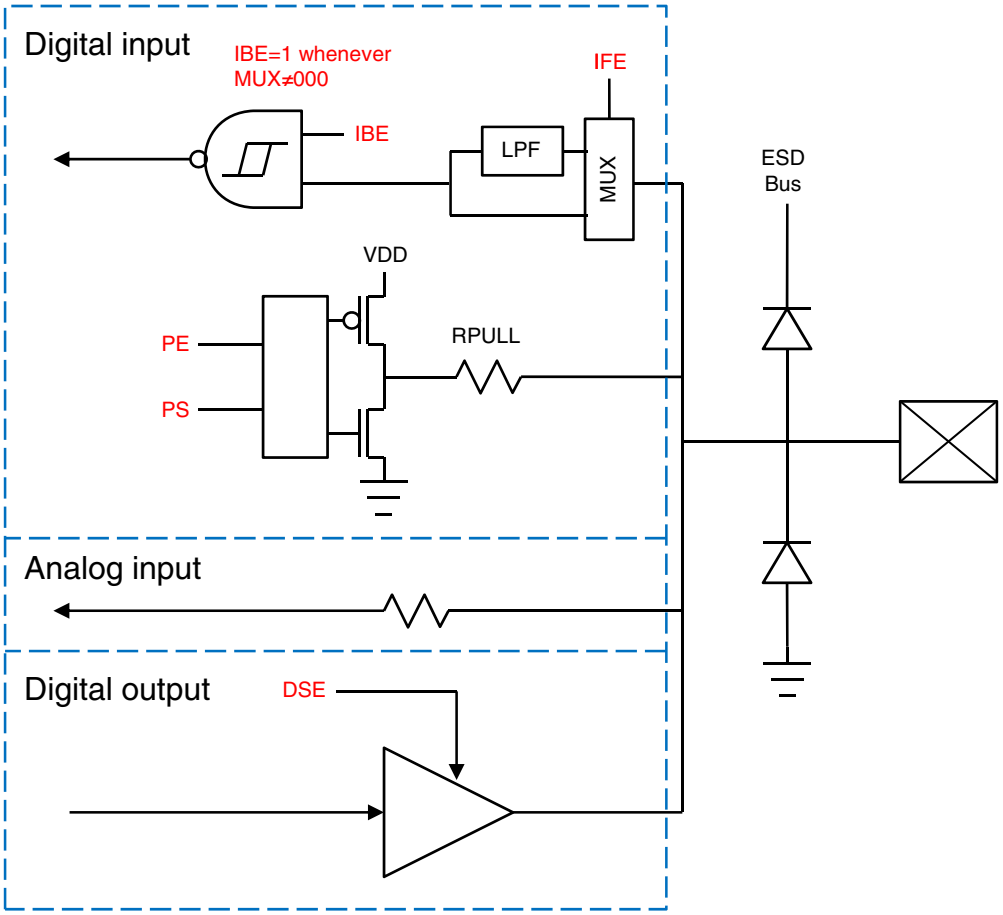



**Figure 4. I/O simplified block diagram**

The PORT module has the following features:

- all PIN support interrupt enable
- Configurable edge (rising, falling, or both) or level sensitive interrupt type
- Support DMA request

- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- GPIO support single-cycle access via fast GPIO.

# 3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. For more details of the system memory and peripheral locations, see the Memory Map chapter in the Reference Manual.

# 4 Pinouts

## 4.1 KE1xZ64 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 48 LQFP | 44 LQFP | 40 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | — | 5 | PTE5 | TSI0_CH0 | TSI0_CH0 | PTE5 | TCLK2 | | | | | EWM_IN |
| — | — | 6 | PTE4 | TSI0_CH1 | TSI0_CH1 | PTE4 | BUSOUT | | | | | EWM_OUT_b |
| — | — | 32 | PTC7 | TSI0_CH16 | TSI0_CH16 | PTC7 | LPUART1_TX | | | | | |
| — | — | 33 | PTC6 | TSI0_CH15 | TSI0_CH15 | PTC6 | LPUART1_RX | | | | | |
| 1 | 1 | 1 | PTD1 | TSI0_CH5 | TSI0_CH5 | PTD1 | FTM0_CH3 | | | | | TRGMUX_OUT2 |
| 2 | 2 | 2 | PTD0 | TSI0_CH4 | TSI0_CH4 | PTD0 | FTM0_CH2 | | | | | TRGMUX_OUT1 |

| 48 LQFP | 44 LQFP | 40 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | — | 3 | PTE11 | TSI0_CH3 | TSI0_CH3 | PTE11 | PWT_IN1 | LPTMR0_ ALT1 | | | | |
| 4 | — | 4 | PTE10 | TSI0_CH2 | TSI0_CH2 | PTE10 | CLKOUT | | | | | |
| 5 | 3 | — | PTE5 | TSI0_CH0 | TSI0_CH0 | PTE5 | TCLK2 | | | CAN0_TX | | EWM_IN |
| 6 | 4 | — | PTE4 | TSI0_CH1 | TSI0_CH1 | PTE4 | BUSOUT | | | CAN0_RX | | EWM_OUT_b |
| 7 | 5 | 7 | VDD | VDD | VDD | | | | | | | |
| 8 | 6 | 7 | VDDA | VDDA | VDDA | | | | | | | |
| 9 | 7 | 7 | VREFH | VREFH | VREFH | | | | | | | |
| 10 | 8 | — | VSS/ VREFL | VSS/ VREFL | VSS/ VREFL | | | | | | | |
| 11 | 9 | 8 | PTB7 | EXTAL | EXTAL | PTB7 | LPI2C0_SCL | | | | | |
| 12 | 10 | 9 | PTB6 | XTAL | XTAL | PTB6 | LPI2C0_SDA | | | | | |
| 13 | 11 | — | PTE3 | TSI0_CH24 | TSI0_CH24 | PTE3 | FTM0_FLT0 | LPUART2_ RTS | | | | |
| 14 | — | 10 | PTE8 | ACMP0_IN3/ TSI0_CH11 | ACMP0_IN3/ TSI0_CH11 | PTE8 | | | | | | |
| 15 | 12 | 11 | PTB5 | TSI0_CH9 | TSI0_CH9 | PTB5 | FTM0_CH5 | LPSPI0_ PCS1 | | | TRGMUX_IN0 | |
| 16 | 13 | 12 | PTB4 | TSI0_CH8 | TSI0_CH8 | PTB4 | FTM0_CH4 | LPSPI0_ SOUT | | | TRGMUX_IN1 | |
| 17 | 14 | 13 | PTC3 | ADC0_SE11/ ACMP0_IN4 | ADC0_SE11/ ACMP0_IN4 | PTC3 | FTM0_CH3 | | | | | |
| 18 | 15 | 14 | PTC2 | ADC0_SE10/ ACMP0_IN5 | ADC0_SE10/ ACMP0_IN5 | PTC2 | FTM0_CH2 | | | | | |
| 19 | 16 | 15 | PTD7 | TSI0_CH10 | TSI0_CH10 | PTD7 | LPUART2_TX | | | | | |
| 20 | 17 | 16 | PTD6 | TSI0_CH7 | TSI0_CH7 | PTD6 | LPUART2_RX | | | | | |
| 21 | 18 | 17 | PTD5 | TSI0_CH6 | TSI0_CH6 | PTD5 | | LPTMR0_ ALT2 | | PWT_IN2 | | LPUART2_ CTS |
| 22 | 19 | 18 | PTC1 | ADC0_SE9/ TSI0_CH23 | ADC0_SE9/ TSI0_CH23 | PTC1 | FTM0_CH1 | | | | | |
| 23 | 20 | 19 | PTC0 | ADC0_SE8/ TSI0_CH22 | ADC0_SE8/ TSI0_CH22 | PTC0 | FTM0_CH0 | | | | | |
| 24 | 21 | 20 | PTB3 | ADC0_SE7/ TSI0_CH21 | ADC0_SE7/ TSI0_CH21 | PTB3 | FTM1_CH1 | LPSPI0_SIN | FTM1_QD_ PHA | | TRGMUX_IN2 | |
| 25 | 22 | 22 | PTB2 | ADC0_SE6/ TSI0_CH20 | ADC0_SE6/ TSI0_CH20 | PTB2 | FTM1_CH0 | LPSPI0_SCK | FTM1_QD_ PHB | | TRGMUX_IN3 | |
| 26 | 23 | 23 | PTB1 | ADC0_SE5 | ADC0_SE5 | PTB1 | LPUART0_TX | LPSPI0_ SOUT | TCLK0 | | | |
| 27 | 24 | 24 | PTB0 | ADC0_SE4 | ADC0_SE4 | PTB0 | LPUART0_RX | LPSPI0_ PCS0 | LPTMR0_ ALT3 | PWT_IN3 | | |
| 28 | 25 | 25 | PTA7 | ADC0_SE3 | ADC0_SE3 | PTA7 | FTM0_FLT2 | LPSPI0_ PCS3 | RTC_CLKIN | | LPUART1_ RTS | |
| 29 | 26 | — | PTA6 | ADC0_SE2 | ADC0_SE2 | PTA6 | FTM0_FLT1 | | | | LPUART1_ CTS | |

| 48 LQFP | 44 LQFP | 40 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 30 | 27 | 21, 40 and EP | VSS | VSS | VSS | | | | | | | |
| 31 | 28 | 26 | VDD | VDD | VDD | | | | | | | |
| 32 | 29 | — | PTD4 | DISABLED | | PTD4 | FTM0_FLT3 | | | | | |
| 33 | 30 | 27 | PTD3 | NMI_b | | PTD3 | | | | | | NMI_b |
| 34 | 31 | — | PTD2 | DISABLED | | PTD2 | | | | | | |
| 35 | 32 | 28 | PTA3 | DISABLED | | PTA3 | | LPI2C0_SCL | EWM_IN | | LPUART0_TX | |
| 36 | 33 | 29 | PTA2 | DISABLED | | PTA2 | | LPI2C0_SDA | EWM_OUT_b | | LPUART0_RX | |
| 37 | 34 | 30 | PTA1 | ADC0_SE1/ ACMP0_IN1/ TSI0_CH18 | ADC0_SE1/ ACMP0_IN1/ TSI0_CH18 | PTA1 | FTM1_CH1 | LPI2C0_ SDAS | | FTM1_QD_ PHA | LPUART0_ RTS | TRGMUX_ OUT0 |
| 38 | 35 | 31 | PTA0 | ADC0_SE0/ ACMP0_IN0/ TSI0_CH17 | ADC0_SE0/ ACMP0_IN0/ TSI0_CH17 | PTA0 | | LPI2C0_ SCLS | | | LPUART0_ CTS | TRGMUX_ OUT3 |
| 39 | 36 | — | PTC7 | TSI0_CH16 | TSI0_CH16 | PTC7 | LPUART1_TX | | | CAN0_TX | | |
| 40 | 37 | — | PTC6 | TSI0_CH15 | TSI0_CH15 | PTC6 | LPUART1_RX | | | CAN0_RX | | |
| 41 | — | — | PTE6 | DISABLED | | PTE6 | LPSPI0_ PCS2 | | | | LPUART1_ RTS | |
| 42 | 38 | — | PTE2 | TSI0_CH19 | TSI0_CH19 | PTE2 | LPSPI0_ SOUT | LPTMR0_ ALT3 | | PWT_IN3 | LPUART1_ CTS | |
| 43 | 39 | 34 | PTE1 | TSI0_CH14 | TSI0_CH14 | PTE1 | LPSPI0_SIN | LPI2C0_ HREQ | | | | |
| 44 | 40 | 35 | PTE0 | TSI0_CH13 | TSI0_CH13 | PTE0 | LPSPI0_SCK | TCLK1 | | | | |
| 45 | 41 | 36 | PTC5 | TSI0_CH12 | TSI0_CH12 | PTC5 | | RTC_ CLKOUT | | | | |
| 46 | 42 | 37 | PTC4 | SWD_CLK | ACMP0_IN2 | PTC4 | FTM1_CH0 | RTC_ CLKOUT | | EWM_IN | FTM1_QD_ PHB | SWD_CLK |
| 47 | 43 | 38 | PTA5 | RESET_b | | PTA5 | | TCLK1 | | | | RESET_b |
| 48 | 44 | 39 | PTA4 | SWD_DIO | | PTA4 | | | ACMP0_OUT | EWM_OUT_b | | SWD_DIO |

## 4.2 Port control and interrupt summary

The following table provides more information regarding the Port Control and Interrupt configurations.

**Table 6. Ports summary**

| Feature | Port A | Port B | Port C | Port D | Port E |
|---|---|---|---|---|---|
| Pull select control | Yes | Yes | Yes | Yes | Yes |
| Pull select at reset | PTA4/PTA5=Pull up, Others=No | No | PTC4=Pull down, Others=No | PTD3=Pull up, Others=No | No |

*Table continues on the next page...*

**Table 6. Ports summary (continued)**

| Feature | Port A | Port B | Port C | Port D | Port E |
|---|---|---|---|---|---|
| Pull enable control | Yes | Yes | Yes | Yes | Yes |
| Pull enable at reset | PTA4/ PTA5=Enabled; Others=Disabled | Disabled | PTC4=Enabled; Others=Disabled | PTD3=Enabled; Others=Disabled | Disabled |
| Passive filter enable control | PTA5=Yes; Others=No | No | No | PTD3=Yes; Others=No | No |
| Passive filter enable at reset | PTA5=Enabled; Others=Disabled | Disabled | Disabled | Disabled | Disabled |
| Open drain enable control | I2C and UART Tx=Enabled; Others=Disabled | I2C and UART Tx=Enabled; Others=Disabled | I2C and UART Tx=Enabled; Others=Disabled | I2C and UART Tx=Enabled; Others=Disabled | I2C and UART Tx=Enabled; Others=Disabled |
| Open drain enable at reset | Disabled | Disabled | Disabled | Disabled | Disabled |
| Drive strength enable control | No | PTB4/PTB5 only | No | PTD0/PTD1 only | PTE0/PTE1 only |
| Drive strength enable at reset | Disabled | Disabled | Disabled | Disabled | Disabled |
| Pin mux control | Yes | Yes | Yes | Yes | Yes |
| Pin mux at reset | PTA4/PTA5=ALT7; Others=ALT0 | ALT0 | PTC4=ALT7; Others=ALT0 | PTD3=ALT7; Others=ALT0 | ALT0 |
| Lock bit | Yes | Yes | Yes | Yes | Yes |
| Interrupt and DMA request | Yes | Yes | Yes | Yes | Yes |
| Digital glitch filter | No | No | No | No | Yes |

## 4.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

### 4.3.1 Core Modules

**Table 7. SWD Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| SWD_CLK | SWD_CLK | Serial Wire Clock | I |
| SWD_DIO | SWD_DIO | Serial Wire Data | I/O |

### 4.3.2 System Modules

**Table 8. System Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| NMI_b | — | Non-maskable interrupt NOTE: Driving the NMI signal low forces a non-maskable interrupt, if the NMI function is selected on the corresponding pin. | I |
| RESET_b | — | Reset bidirectional signal | I/O |
| VDD | — | MCU power | I |
| VSS | — | MCU ground | I |

**Table 9. EWM Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| EWM_IN | EWM_in | EWM input for safety status of external safety circuits. The polarity of EWM_IN is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low. | I |
| EWM_OUT_b | $\overline{\text{EWM\_out}}$ | EWM reset out signal | O |

### 4.3.3 Clock Modules

**Table 10. OSC (in SCG) Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| EXTAL | EXTAL | External clock/Oscillator input | I |
| XTAL | XTAL | Oscillator output | O |

### 4.3.4 Analog

**Table 11. ADC*0* Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| ADC*0*_SE[11:0] | AD[11:0] | Single-Ended Analog Channel Inputs | I |
| VREFH | $V_{REFSH}$ | Voltage Reference Select High | I |

*Table continues on the next page...*

**Table 11. ADC*0* Signal Descriptions (continued)**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| VREFL | $V_{REFSL}$ | Voltage Reference Select Low | I |
| VDDA | $V_{DDA}$ | Analog Power Supply | I |

**Table 12. ACMP*0* Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| ACMP*0*_IN[5:0] | IN[5:0] | Analog voltage inputs | I |
| ACMP*0*_OUT | CMPO | Comparator output | O |

## 4.3.5 Timer Modules

**Table 13. LPTMR0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPTMR0_ALT[3:1] | LPTMR_ALT*n* | Pulse Counter Input pin | I |

**Table 14. RTC Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| RTC_CLKOUT | RTC_CLKOUT | 1 Hz square-wave output or 32 kHz clock | O |

**Table 15. FTM*0* Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| FTM*0*_CH[5:0] | CHn | FTM channel (n), where n can be 5-0 | I/O |
| FTM*0*_FLT[3:0] | FAULTj | Fault input (j), where j can be 3-0 | I |
| TCLK[2:0] | EXTCLK | External clock. FTM external clock can be selected to drive the FTM counter. | I |

**Table 16. FTM*1* Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| FTM*1*_CH[1:0] | CHn | FTM channel (n), where n can be 1-0 | I/O |
| FTM*1*_QD_PHA | PHA | Quadrature decoder phase A input. Input pin associated with quadrature decoder phase A. | I |

*Table continues on the next page...*

**Table 16. FTM*1* Signal Descriptions (continued)**

| | | | |
|---|---|---|---|
| FTM*1*_QD_PHB | PHB | Quadrature decoder phase B input. Input pin associated with quadrature decoder phase B. | I |

## 4.3.6 Communication Interfaces

**Table 17. CAN*n* Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| CAN*n*_RX | CAN Rx | CAN Receive Pin | I |
| CAN*n*_TX | CAN Tx | CAN Transmit Pin | O |

**Table 18. LPSPI*n* Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPSPI*n*_SOUT | SOUT | Serial Data Out | O |
| LPSPI*n*_SIN | SIN | Serial Data In | I |
| LPSPI*n*_SCK | SCK | Serial Clock | I/O |
| LPSPI*n*_PCS[3:0] | PCS[3:0] | Peripheral Chip Select 0-3 | I/O |

**Table 19. LPI2C*n* Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPI2C*n*_SCL | SCL | Bidirectional serial clock line of the I2C system. | I/O |
| LPI2C*n*_SDA | SDA | Bidirectional serial data line of the I2C system. | I/O |
| LPI2C*n*_HREQ | HREQ | Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle. | I |
| LPI2C*n*_SCLS | SCLS | Secondary I2C clock line. | I/O |
| LPI2C*n*_SDAS | SDAS | Secondary I2C data line. | I/O |

**Table 20. LPUART*n* Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPUART*n*_TX | LPUART_TXD | Transmit data | I/O |
| LPUART*n*_RX | LPUART_RXD | Receive data | I |
| LPUART*n*_CTS | LPUART_CTS | Clear to send | I |
| LPUART*n*_RTS | LPUART_RTS | Request to send | O |

### 4.3.7 Human-Machine Interfaces (HMI)

**Table 21. GPIO Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| PTA[7:0] | PORTA7–PORTA0 | General-purpose input/output | I/O |
| PTB[7:0] | PORTB7–PORTB0 | General-purpose input/output | I/O |
| PTC[7:0] | PORTC7–PORTC0 | General-purpose input/output | I/O |
| PTD[7:0] | PORTD7–PORTD0 | General-purpose input/output | I/O |
| PTE[11:10],<br>PTE[8],<br>PTE[6:0] | PORTE11–PORTE10<br>PORTE8<br>PORTE6–PORTE0 | General-purpose input/output | I/O |

**Table 22. TSI0 Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| TSI0_CH[24:0] | TSI[24:0] | TSI sensing pins or GPIO pins | I/O |

## 4.4 Pinout diagram

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous table of Pin Assignments.

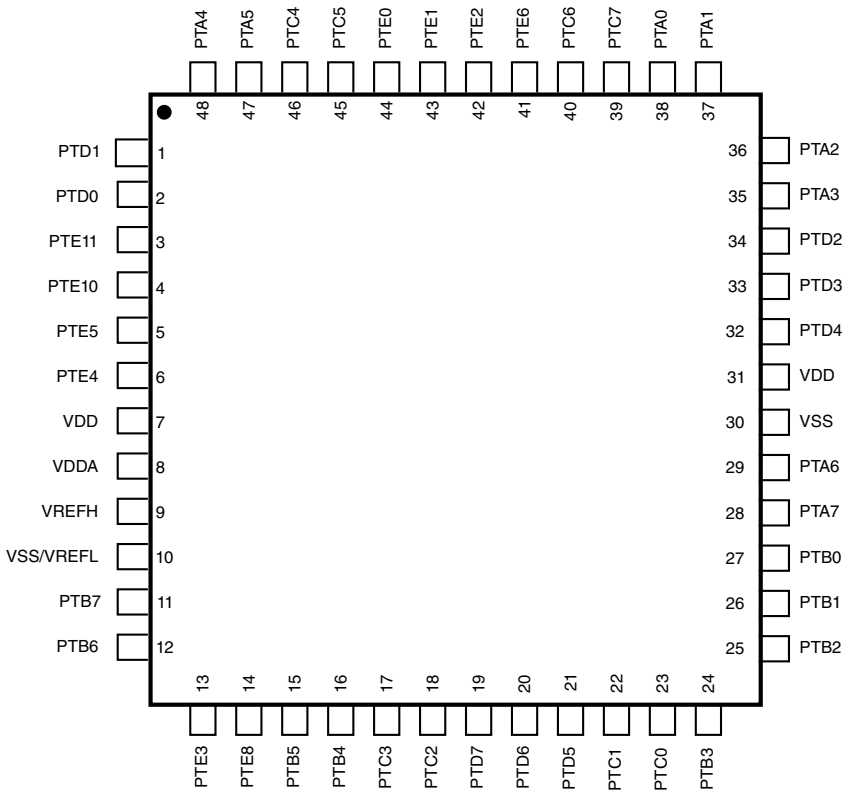



**Figure 5. 48 LQFP Pinout Diagram**

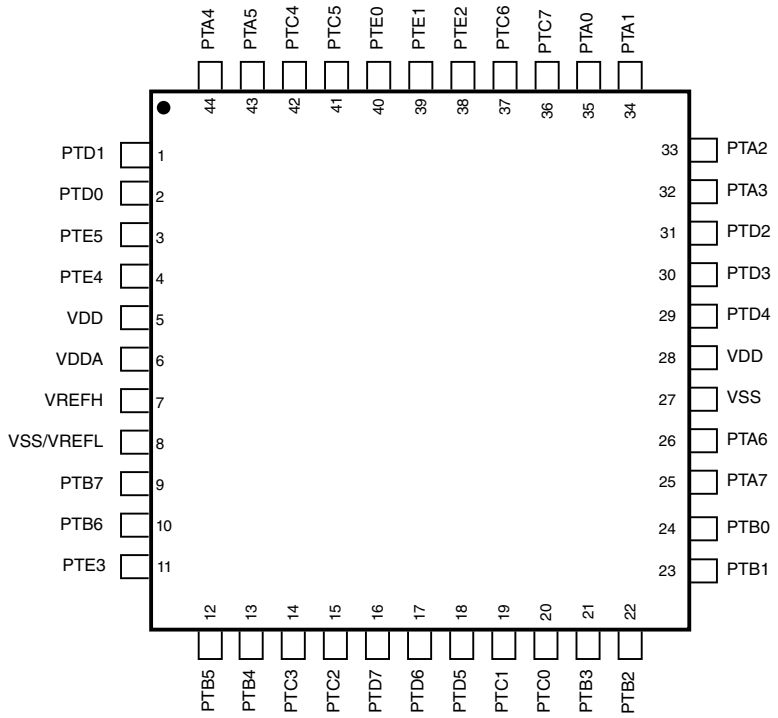



**Figure 6. 44 LQFP Pinout Diagram**

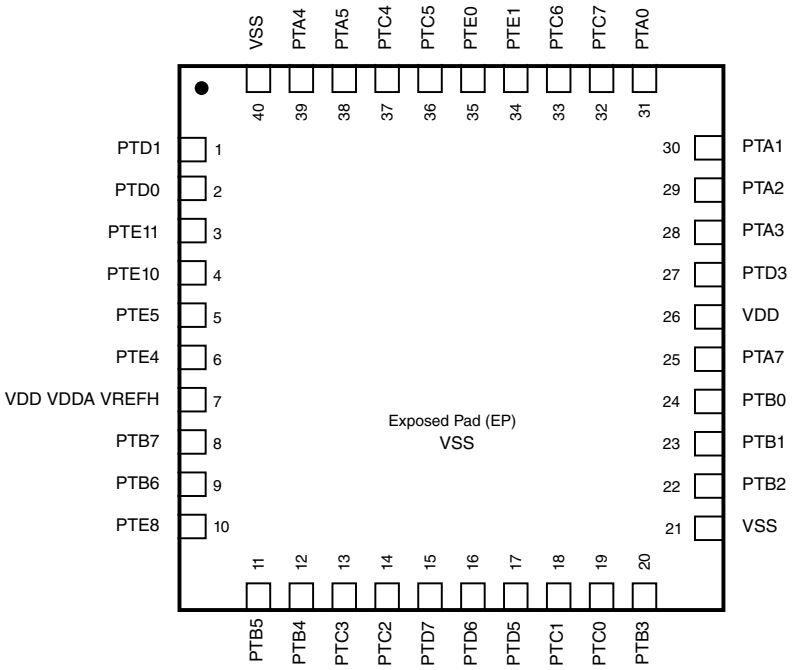



**Figure 7. 40 QFN Pinout Diagram**

## 4.5 Package dimensions

The following hyperlinks (package drawings) show the dimensions of the package options for the devices supported by this document.

- 48-LQFP: 98ASH00962A
- 44-LQFP: 98ASS23225W
- 40-QFN: 98ASA01371D

# 5 Electrical characteristics

## 5.1 Terminology and guidelines

### 5.1.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|---|---|
| Rating | A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:<br>• *Operating ratings* apply during operation of the chip.<br>• *Handling ratings* apply when the chip is not powered.<br>**NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings. |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | A specified value for a technical characteristic that:<br>• Lies within the range of values specified by the operating behavior<br>• Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions<br>**NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed. |

## 5.1.2 Examples

*Operating rating*:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

*Operating requirement*:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

*Operating behavior* that includes a *typical value*:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

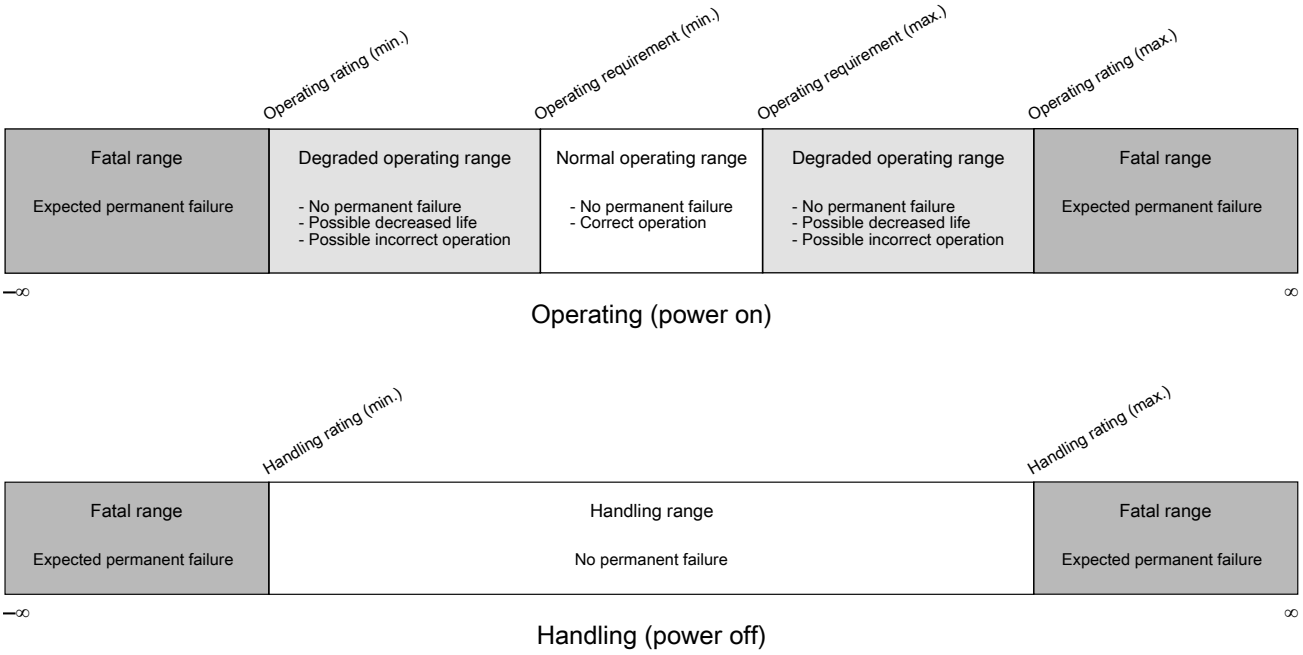


## 5.1.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | Supply voltage | 5.0 | V |

### 5.1.4 Relationship between ratings and operating requirements




### 5.1.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 5.2 Ratings

### 5.2.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 5.2.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 5.2.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | – 6000 | 6000 | V | 1 |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | | | | 2 |
| | All pins except the corner pins | – 500 | 500 | V | |
| | Corner pins only | – 750 | 750 | V | |
| $I_{LAT}$ | Latch-up current at ambient temperature upper limit | – 100 | 100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 5.2.4 Voltage and current operating ratings

**NOTE**

Functional operating conditions appear in the "DC electrical specifications". Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

**Table 23. Voltage and current operating ratings**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.3 | 5.8 [1] | V |
| $I_{DD}$ | Digital supply current | — | | mA |

*Table continues on the next page...*

**Table 23. Voltage and current operating ratings (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{IO}$ | IO pin input voltage | $V_{SS}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.1 | $V_{DD}$ + 0.1 | V |

1. 60s lifetime - No restrictions, i.e. the part can switch.

   10 hours lifetime - Device in reset, i.e. the part cannot switch.

# 5.3 General

## 5.3.1 Nonswitching electrical specifications

### 5.3.1.1 Voltage and current operating requirements

**Table 24. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.7 | 5.5 | V | |
| $V_{DDA}$ | Analog supply voltage | 2.7 | 5.5 | V | |
| $V_{DD}$ – $V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | – 0.1 | 0.1 | V | |
| $V_{SS}$ – $V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | – 0.1 | 0.1 | V | |
| $I_{ICIO}$ | DC injection current — single pin | | | | |
| | $V_{IN} < V_{SS}$ - 0.3 V (Negative current injection) | – 3 | — | mA | 1 |
| | $V_{IN} > V_{DD}$ + 0.3 V (Positive current injection) | — | + 3 | mA | |
| $I_{ICcont}$ | Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins | – 25 | + 25 | mA | |
| $V_{ODPU}$ | Open drain pullup voltage level | $V_{DD}$ | $V_{DD}$ | V | 2 |

1. All pins are internally clamped to $V_{SS}$ and $V_{DD}$ through ESD protection diodes. If $V_{IN}$ is less than $V_{SS}$ – 0.3V or greater than $V_{DD}$ + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{SS} – 0.3V–V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R=[V_{IN}–(V_{DD} + 0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.
2. Open drain outputs must be pulled to $V_{DD}$.

### 5.3.1.2 DC electrical specifications at 3.3 V Range and 5.0 V Range

**Table 25. DC electrical specifications**

| Symbol | Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $V_{DD}$ | I/O Supply Voltage [1]<br>@ $V_{DD}$ = 3.3 V | 2.7 | 3.3 | 4 | V | |
| | @ $V_{DD}$ = 5.0 V | 4 | — | 5.5 | V | |
| $V_{ih}$ | Input Buffer High Voltage<br>@ $V_{DD}$ = 3.3 V | 0.7 × $V_{DD}$ | — | $V_{DD}$ + 0.3 | V | |
| | @ $V_{DD}$ = 5.0 V | 0.65 × $V_{DD}$ | — | $V_{DD}$ + 0.3 | V | |
| $V_{il}$ | Input Buffer Low Voltage<br>@ $V_{DD}$ = 3.3 V | $V_{SS}$ – 0.3 | — | 0.3 × $V_{DD}$ | V | |
| | @ $V_{DD}$ = 5.0 V | $V_{SS}$ – 0.3 | — | 0.35 × $V_{DD}$ | V | |
| $V_{hys}$ | Input Buffer Hysteresis | 0.06 × $V_{DD}$ | — | — | V | |
| Ioh_5 | Normal drive I/O current source capability measured when pad = ($V_{DD}$ – 0.8 V)<br>@ $V_{DD}$ = 3.3 V | 2.8 | — | — | mA | |
| | @ $V_{DD}$ = 5.0 V | 4.8 | — | — | mA | |
| Iol_5 | Normal drive I/O current sink capability measured when pad = 0.8 V<br>@ $V_{DD}$ = 3.3 V | 2.4 | — | — | mA | |
| | @ $V_{DD}$ = 5.0 V | 4.4 | — | — | mA | |
| Ioh_20 | High drive I/O current source capability measured when pad = ($V_{DD}$ – 0.8 V), [2]<br>@ $V_{DD}$ = 3.3 V | 10.8 | — | — | mA | |
| | @ $V_{DD}$ = 5.0 V | 18.5 | — | — | mA [3] | |
| Iol_20 | High drive I/O current sink capability measured when pad = 0.8 V[4]<br>@ $V_{DD}$ = 3.3 V | 10.1 | — | — | mA | |
| | @ $V_{DD}$ = 5.0 V | 18.5 | — | — | mA [3] | |
| I_leak | Hi-Z (Off state) leakage current (per pin) | — | — | 300 | nA | 5, 6 |
| $V_{OH}$ | Output high voltage | | | | | 7 |
| | Normal drive pad (2.7 V ≤ $V_{DD}$ ≤ 4.0 V, $I_{OH}$ = –2.8 mA) | $V_{DD}$ – 0.8 | — | — | V | |
| | Normal drive pad (4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH}$ = –4.8 mA) | $V_{DD}$ – 0.8 | — | — | V | |
| | High drive pad (2.7 V ≤ $V_{DD}$ ≤ 4.0 V, $I_{OH}$ = –10.8 mA) | $V_{DD}$ – 0.8 | — | — | V | |
| | High drive pad (4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH}$ = –18.5 mA) | $V_{DD}$ – 0.8 | — | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | — | 100 | mA | |
| $V_{OL}$ | Output low voltage | | | | | 7 |

*Table continues on the next page...*

## Table 25. DC electrical specifications (continued)

| Symbol | Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| | Normal drive pad (2.7 V ≤ $V_{DD}$ ≤ 4.0 V, $I_{OH}$ = –2.8 mA) | — | — | 0.8 | V | |
| | Normal drive pad (4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH}$ = –4.8 mA) | — | — | 0.8 | V | |
| | High drive pad (2.7 V ≤ $V_{DD}$ ≤ 4.0 V, $I_{OH}$ = –10.8 mA) | — | — | 0.8 | V | |
| | High drive pad (4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH}$ = –18.5 mA) | — | — | 0.8 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) for full temperature range @ $V_{DD}$ = 3.3 V | | | | | 8, 7 |
| | All pins other than high drive port pins | — | 0.002 | 0.5 | µA | |
| | High drive port pins | — | 0.004 | 0.5 | µA | |
| | Input leakage current (per pin) for full temperature range @ $V_{DD}$ = 5.5 V | | | | | |
| | All pins other than high drive port pins | — | 0.005 | 0.5 | µA | |
| | High drive port pins | — | 0.010 | 0.5 | µA | |
| $R_{PU}$ | Internal pull-up resistors @ $V_{DD}$ = 3.3 V | 20 | — | 65 | kΩ | 9 |
| | @ $V_{DD}$ = 5.0 V | 20 | — | 50 | kΩ | |
| $R_{PD}$ | Internal pull-down resistors @ $V_{DD}$ = 3.3 V | 20 | — | 65 | kΩ | 10 |
| | @ $V_{DD}$ = 5.0 V | 20 | — | 50 | kΩ | |

1. Max power supply ramp rate is 500 V/ms.
2. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_5 value given above.
3. The 20 mA I/O pin is capable of switching a 50 pF load at up to 40 MHz.
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_5 value given above.
5. Refers to the current that leaks into the core when the pad is in Hi-Z (Off state).
6. Maximum pin leakage current at the ambient temperature upper limit.
7. PTD0, PTD1, PTB4, PTB5, PTE0 and PTE1 I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
8. Refers to the pin leakage on the GPIOs when they are OFF.
9. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and input V = $V_{SS}$
10. Measured at $V_{DD}$ supply voltage = $V_{DD}$ min and input V = $V_{DD}$

### 5.3.1.3 Voltage regulator electrical characteristics

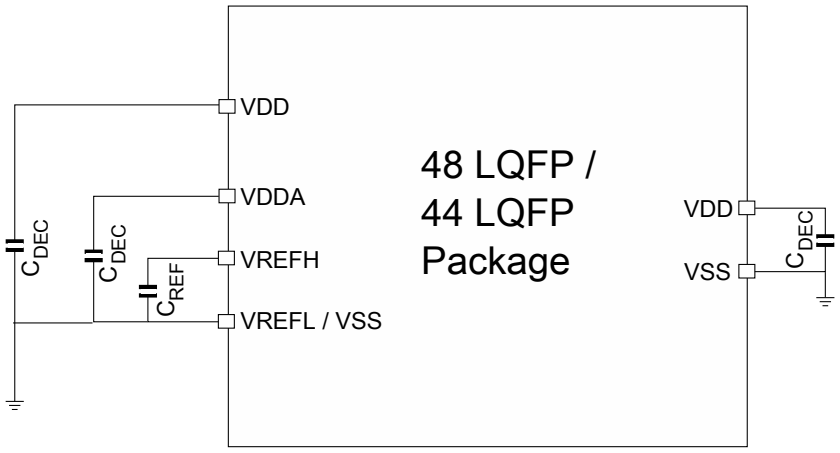



**Figure 8. Pinout decoupling**

**Table 26. Voltage regulator electrical characteristics**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{REF}$[1, 2] | ADC reference high decoupling capacitance | — | 100 | — | nF |
| $C_{DEC}$[2, 3] | Recommended decoupling capacitance | — | 100 | — | nF |

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding $V_{DD}/V_{SS}$ pins.
3. The requirement and value of of $C_{DEC}$ will be decided by the device application requirement.

### 5.3.1.4 LVR, LVD and POR operating requirements

**Table 27. $V_{DD}$ supply LVR, LVD and POR operating requirements**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{POR}$ | Rising and Falling $V_{DD}$ POR detect voltage | 1.1 | 1.6 | 2.0 | V | |
| $V_{LVRX}$ | LVRX falling threshold (RUN and STOP modes) | 2.53 | 2.58 | 2.64 | V | |
| $V_{LVRX\_HYST}$ | LVRX hysteresis | — | 45 | — | mV | 1 |
| $V_{LVRX\_LP}$ | LVRX falling threshold (VLPS/VLPR modes) | 1.97 | 2.12 | 2.44 | V | |
| $V_{LVRX\_LP\_HYST}$ | LVRX hysteresis (VLPS/VLPR modes) | — | 40 | — | mV | |
| $V_{LVD}$ | Falling low-voltage detect threshold | 2.8 | 2.88 | 3 | V | |
| $V_{LVD\_HYST}$ | LVD hysteresis | — | 50 | — | mV | 1 |
| $V_{LVW}$ | Falling low-voltage warning threshold | 4.19 | 4.31 | 4.5 | V | |
| $V_{LVW\_HYST}$ | LVW hysteresis | | 68 | | mV | 1 |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

### 5.3.1.5 Power mode transition operating behaviors

**Table 28. Power mode transition operating behaviors**

| Description | System Clock | Core, Bus, Flash frequency (MHz) | Min. | Typ. (µs)[1] | Max. (µs)[2] |
|---|---|---|---|---|---|
| STOP→RUN | FIRC | 48, 24, 24 | — | 7.41 | 13.4 |
| STOP→RUN | FLL | 48, 24, 24 | — | 10.9 | 16.5 |
| VLPS→RUN | FIRC | 48, 24, 24 | — | 7.41 | 13.4 |
| VLPS→RUN | FLL | 48, 24, 24 | — | 10.4 | 16.9 |
| RUN→VLPR | FLL→SIRC | 48, 24, 24→4, 1, 1 | — | 14.3 | 15 |
| VLPR→RUN | SIRC→FIRC | 4, 1, 1→48, 24, 24 | — | 23.5 | 37.3 |
| VLPR→RUN | SIRC→FLL | 4, 1, 1→48, 24, 24 | — | 27 | 36 |
| WAIT→RUN | FIRC | 48, 24, 24 | — | 0.620 | 0.760 |
| WAIT→RUN | FLL | 48, 24, 24 | — | 0.632 | 0.775 |
| VLPW→VLPR | SIRC | 4, 1, 1 | — | 20.7 | 28 |
| VLPS→VLPR | SIRC | 4, 1, 1 | — | 19.8 | 26 |
| VLPW→RUN | FIRC (reset value) | 48, 24, 24 (reset value) | — | 97.4 | 109 |
| $t_{POR}$[3] | FIRC (reset value) | 48, 24, 24 (reset value) | — | 88.2 | 101 |

1. Typical value is the average of values tested at Temperature=25 ℃ and $V_{DD}$=3.3 V.
2. Max value is mean+6×sigma of tested values at the worst case of ambient temperature range and $V_{DD}$ 2.7 V to 5.5 V.
3. After a POR event, the amount of time from the point $V_{DD}$ reaches the reference voltage 2.7 V to execution of the first instruction, across the operating temperature range of the chip.

### 5.3.1.6 Power consumption

The following table shows the power consumption targets for the device in various modes of operations.

**NOTE**

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**Table 29. Power consumption operating behaviors (48 LQFP and 44 LQFP)**

| Mode | Symbol | Clock Configuration | Description | Temperature | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|---|
| RUN | $I_{DD\_RUN}$ | LPFLL | Running CoreMark in Flash in **Compute Operation** mode.<br>Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 8.09 | 8.23 | mA |
| | | | | 105 ℃ | — | 8.37 | 8.51 | |
| | | LPFLL | Running CoreMark in Flash all peripheral clock disabled. | 25 ℃ | — | 8.76 | 8.90 | |

*Table continues on the next page...*

## Table 29. Power consumption operating behaviors (48 LQFP and 44 LQFP) (continued)

| Mode | Symbol | Clock Configuration | Description | Temperature | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V | 105 ℃ | — | 9.04 | 9.18 | |
| | | LPFLL | Running CoreMark in Flash, all peripheral clock enabled.<br>Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 9.76 | 9.90 | |
| | | | | 105 ℃ | — | 10.06 | 10.20 | |
| | | LPFLL | Running While(1) loop in Flash, all peripheral clock disabled.<br>Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 6.65 | 6.79 | |
| | | | | 105 ℃ | — | 6.91 | 7.05 | |
| | | LPFLL | Running While(1) loop in Flash all peripheral clock enabled.<br>Core@48MHz , bus@24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 7.66 | 7.80 | |
| | | | | 105 ℃ | — | 7.94 | 8.08 | |
| | | IRC48M | Running CoreMark in Flash in **Compute Operation** mode.<br>Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 7.8 | 7.94 | |
| | | | | 105 ℃ | — | 7.97 | 8.11 | |
| | | IRC48M | Running CoreMark in Flash all peripheral clock disabled.<br>Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 8.46 | 8.60 | |
| | | | | 105 ℃ | — | 8.64 | 8.78 | |
| | | IRC48M | Running CoreMark in Flash, all peripheral clock enabled.<br>Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 9.47 | 9.61 | |
| | | | | 105 ℃ | — | 9.64 | 9.78 | |
| | | IRC48M | Running While(1) loop in Flash, all peripheral clock disabled.<br>Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 6.35 | 6.49 | |
| | | | | 105 ℃ | — | 6.55 | 6.69 | |
| VLPR | $I_{DD\_VLPR}$ | IRC8M | Very Low Power Run Core Mark in Flash in **Compute Operation** mode.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 ℃ | — | 1480 | 1522 | µA |
| | | IRC8M | Very Low Power Run Core Mark in Flash all peripheral clock disabled.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 ℃ | — | 1580 | 1622 | |
| | | IRC8M | Very Low Power Run Core Mark in Flash all peripheral clock enabled.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 ℃ | — | 1510 | 1552 | |

*Table continues on the next page...*

## Table 29. Power consumption operating behaviors (48 LQFP and 44 LQFP) (continued)

| Mode | Symbol | Clock Configuration | Description | Temperature | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|---|
| | | IRC8M | Very Low Power Run While(1) loop in Flash all peripheral clock disabled.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 701 | 743 | |
| | | IRC8M | Very Low Power Run While(1) loop in Flash all peripheral clock enabled.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 765 | 807 | |
| | | IRC2M | Very Low Power Run While(1) loop in Flash all peripheral clock disabled.<br>Core@2MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 571 | 613 | |
| | | IRC2M | Very Low Power Run While(1) loop in Flash all peripheral clock enabled.<br>Core@2MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 609 | 651 | |
| WAIT | $I_{DD\_WAIT}$ | LPFLL | core disabled, system@48MHz, bus @24MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled | 25 °C | — | 4.77 | 4.87 | mA |
| | | IRC48M | core disabled, system@48 MHz, bus @24MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled | 25 °C | — | 4.46 | 4.56 | |
| VLPW | $I_{DD\_VLPW}$ | IRC8M | Very Low Power Wait current, core disabled system@4MHz, bus and flash@1MHz, all peripheral clocks disabled, VDD=5V | 25 °C | — | 609 | 644 | µA |
| | | IRC2M | Very Low Power Wait current, core disabled system@2MHz, bus and flash@1MHz, all peripheral clocks disabled, VDD=5V | 25 °C | — | 525 | 560 | |
| STOP | $I_{DD\_STOP}$ | - | Stop mode current, VDD=5V, bias enabled [2], clock bias enabled [3] | 25 °C and below | — | 23 | 25 | µA |
| | | | | 50 °C | — | 25 | 27 | |
| | | | | 85 °C | — | 36 | 39 | |
| | | | | 105 °C | — | 52 | 57 | |
| STOP | $I_{DD\_STOP}$ | - | Stop mode current, VDD=5V, bias enabled [2], clock bias disabled [3] | 25 °C and below | — | 20 | 22 | µA |
| | | | | 50 °C | — | 22 | 25 | |
| | | | | 85 °C | — | 33 | 41 | |
| | | | | 105 °C | — | 48 | 61 | |

*Table continues on the next page...*

## Table 29. Power consumption operating behaviors (48 LQFP and 44 LQFP) (continued)

| Mode | Symbol | Clock Configuration | Description | Temperature | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|---|
| VLPS | $I_{DD\_VLPS}$ | - | Very Low Power Stop current, VDD=5V, bias enabled [2], clock bias enabled [3] | 25 ℃ and below | — | 23 | 25 | µA |
| | | | | 50 ℃ | — | 25 | 27 | |
| | | | | 85 ℃ | — | 36 | 39 | |
| | | | | 105 ℃ | — | 50 | 55 | |
| VLPS | $I_{DD\_VLPS}$ | - | Very Low Power Stop current, VDD=5V, bias enabled [2], clock bias disabled [3] | 25 ℃ and below | — | 20 | 22 | µA |
| | | | | 50 ℃ | — | 22 | 25 | |
| | | | | 85 ℃ | — | 33 | 41 | |
| | | | | 105 ℃ | — | 48 | 61 | |

1. These values are based on characterization but not covered by test limits in production.
2. PMC_REGSC[BIASDIS] is the control bit to enable or disable bias under STOP/VLPS mode.
3. PMC_REGSC[CLKBIASDIS] is the control bit to enable or disable clockbias under STOP/VLPS mode.

## Table 30. Power consumption operating behaviors (40 QFN)

| Mode | Symbol | Clock Configuration | Description | Temperature | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|---|
| RUN | $I_{DD\_RUN}$ | LPFLL | Running CoreMark in Flash in **Compute Operation** mode.<br>Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 8.09 | 8.33 | mA |
| | | | | 105 ℃ | — | 8.37 | 8.62 | |
| | | LPFLL | Running CoreMark in Flash all peripheral clock disabled.<br>Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 8.76 | 9.02 | |
| | | | | 105 ℃ | — | 9.04 | 9.31 | |
| | | LPFLL | Running CoreMark in Flash, all peripheral clock enabled.<br>Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 9.76 | 10.05 | |
| | | | | 105 ℃ | — | 10.06 | 10.36 | |
| | | LPFLL | Running While(1) loop in Flash, all peripheral clock disabled.<br>Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 6.65 | 6.85 | |
| | | | | 105 ℃ | — | 6.91 | 7.12 | |
| | | LPFLL | Running While(1) loop in Flash all peripheral clock enabled.<br>Core@48MHz , bus@24MHz, flash @24MHz, VDD=5V | 25 ℃ | — | 7.66 | 7.89 | |
| | | | | 105 ℃ | — | 7.94 | 8.18 | |
| | | IRC48M | Running CoreMark in Flash in **Compute Operation** mode. | 25 ℃ | — | 7.8 | 8.03 | |
| | | | | 105 ℃ | — | 7.97 | 8.21 | |

*Table continues on the next page...*

## Table 30. Power consumption operating behaviors (40 QFN) (continued)

| Mode | Symbol | Clock Configuration | Description | Temperature | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V | | | | | |
| | | IRC48M | Running CoreMark in Flash all peripheral clock disabled.<br>Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V | 25 °C | — | 8.46 | 8.71 | |
| | | | | 105 °C | — | 8.64 | 8.90 | |
| | | IRC48M | Running CoreMark in Flash, all peripheral clock enabled.<br>Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V | 25 °C | — | 9.47 | 9.75 | |
| | | | | 105 °C | — | 9.64 | 9.93 | |
| | | IRC48M | Running While(1) loop in Flash, all peripheral clock disabled.<br>Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V | 25 °C | — | 6.35 | 6.54 | |
| | | | | 105 °C | — | 6.55 | 6.75 | |
| VLPR | $I_{DD\_VLPR}$ | IRC8M | Very Low Power Run Core Mark in Flash in **Compute Operation** mode.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 1480 | 1670 | µA |
| | | IRC8M | Very Low Power Run Core Mark in Flash all peripheral clock disabled.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 1580 | 1783 | |
| | | IRC8M | Very Low Power Run Core Mark in Flash all peripheral clock enabled.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 1510 | 1704 | |
| | | IRC8M | Very Low Power Run While(1) loop in Flash all peripheral clock disabled.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 701 | 791 | |
| | | IRC8M | Very Low Power Run While(1) loop in Flash all peripheral clock enabled.<br>Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 765 | 863 | |
| | | IRC2M | Very Low Power Run While(1) loop in Flash all peripheral clock disabled.<br>Core@2MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 571 | 644 | |
| | | IRC2M | Very Low Power Run While(1) loop in Flash all peripheral clock enabled.<br>Core@2MHz, bus @1MHz, flash @1MHz, VDD=5V | 25 °C | — | 609 | 687 | |

*Table continues on the next page...*

## Table 30. Power consumption operating behaviors (40 QFN) (continued)

| Mode | Symbol | Clock Configuration | Description | Temperature | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|---|---|
| WAIT | $I_{DD\_WAIT}$ | LPFLL | core disabled, system@48MHz, bus @24MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled | 25 °C | — | 4.77 | 5.37 | mA |
| | | IRC48M | core disabled, system@48 MHz, bus @24MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled | 25 °C | — | 4.46 | 5.02 | |
| VLPW | $I_{DD\_VLPW}$ | IRC8M | Very Low Power Wait current, core disabled system@4MHz, bus and flash@1MHz, all peripheral clocks disabled, VDD=5V | 25 °C | — | 609 | 747 | µA |
| | | IRC2M | Very Low Power Wait current, core disabled system@2MHz, bus and flash@1MHz, all peripheral clocks disabled, VDD=5V | 25 °C | — | 525 | 644 | |
| STOP | $I_{DD\_STOP}$ | - | Stop mode current, VDD=5V, bias enabled [2], clock bias enabled [3] | 25 °C and below | — | 23 | 31 | µA |
| | | | | 50 °C | — | 25 | 51 | |
| | | | | 85 °C | — | 36 | 74 | |
| | | | | 105 °C | — | 52 | 103 | |
| STOP | $I_{DD\_STOP}$ | - | Stop mode current, VDD=5V, bias enabled [2], clock bias disabled [3] | 25 °C and below | — | 20 | 28 | µA |
| | | | | 50 °C | — | 22 | 46 | |
| | | | | 85 °C | — | 33 | 69 | |
| | | | | 105 °C | — | 48 | 100 | |
| VLPS | $I_{DD\_VLPS}$ | - | Very Low Power Stop current, VDD=5V, bias enabled [2], clock bias enabled [3] | 25 °C and below | — | 23 | 31 | µA |
| | | | | 50 °C | — | 25 | 51 | |
| | | | | 85 °C | — | 36 | 74 | |
| | | | | 105 °C | — | 50 | 102 | |
| VLPS | $I_{DD\_VLPS}$ | - | Very Low Power Stop current, VDD=5V, bias enabled [2], clock bias disabled [3] | 25 °C and below | — | 20 | 27 | µA |
| | | | | 50 °C | — | 22 | 46 | |
| | | | | 85 °C | — | 33 | 68 | |
| | | | | 105 °C | — | 48 | 100 | |

1. These values are based on characterization but not covered by test limits in production.
2. PMC_REGSC[BIASDIS] is the control bit to enable or disable bias under STOP/VLPS mode.
3. PMC_REGSC[CLKBIASDIS] is the control bit to enable or disable clockbias under STOP/VLPS mode.

**NOTE**

CoreMark benchmark compiled using IAR 8.30 with optimization level high, optimized for balanced.

#### 5.3.1.6.1 Low power mode peripheral current adder — typical value

| Symbol | Description | Typical |
|---|---|---|
| $I_{LPTMR}$ | LPTMR peripheral adder measured by placing the device in VLPS mode with LPTMR enabled using LPO. Includes LPO power consumption. | 366 nA |
| $I_{CMP}$ | CMP peripheral adder measured by placing the device in VLPS mode with CMP enabled using the 8-bit DAC and a single external input for compare. 8-bit DAC enabled with half VDDA voltage, low speed mode. Includes 8-bit DAC power consumption. | 16 µA |
| $I_{RTC}$ | RTC peripheral adder measured by placing the device in VLPS mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC counter enabled. Includes EXTAL32 (32 kHz external crystal) power consumption. | 312 nA |
| $I_{LPUART}$ | LPUART peripheral adder measured by placing the device in VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. (SIRC 8 MHz) | 79 µA |
| $I_{FTM}$ | FTM peripheral adder measured by placing the device in VLPW mode with selected clock source, outputting the edge aligned PWM of 100 Hz frequency. | 45 µA |
| $I_{ADC}$ | ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in VLPS mode. ADC is configured for low power mode using SIRC clock source, 8-bit resolution and continuous conversions. | 484 µA |
| $I_{LPI2C}$ | LPI2C peripheral adder measured by placing the device in VLPS mode with selected clock source sending START and Slave address, waiting for RX data. Includes the DMA power consumption. | 179 µA |
| $I_{LPIT}$ | LPIT peripheral adder measured by placing the device in VLPS mode with internal SIRC 8 MHz enabled in Stop mode. Includes selected clock source power consumption. | 18 µA |
| $I_{LPSPI}$ | LPSPI peripheral adder measured by placing the device in VLPS mode with selected clock source, output data on SOUT pin with SCK 500 kbit/s. Includes the DMA power consumption. | 565 µA |
| $I_{MSCAN}$ | MSCAN peripheral adder measured by placing the device in RUN mode, CAN baud rate = 125 kbps, loopback mode: MSCAN receives the frame sent by itself continuously. | 2354 µA |
| $I_{TSI}$ | TSI self-cap mode:<br>TSI peripheral adder measured by placing the device in RUN mode, continuous TSI self-cap mode scan with 11.6 kHz switching clock. | 784 µA |
| | TSI mutual-cap mode:<br>TSI peripheral adder measured by placing the device in RUN mode, continuous TSI mutual-cap mode scan with 37.22 kHz switching clock. | 899 µA |

#### 5.3.1.6.2 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- SCG in SOSC for both Run and VLPR modes
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

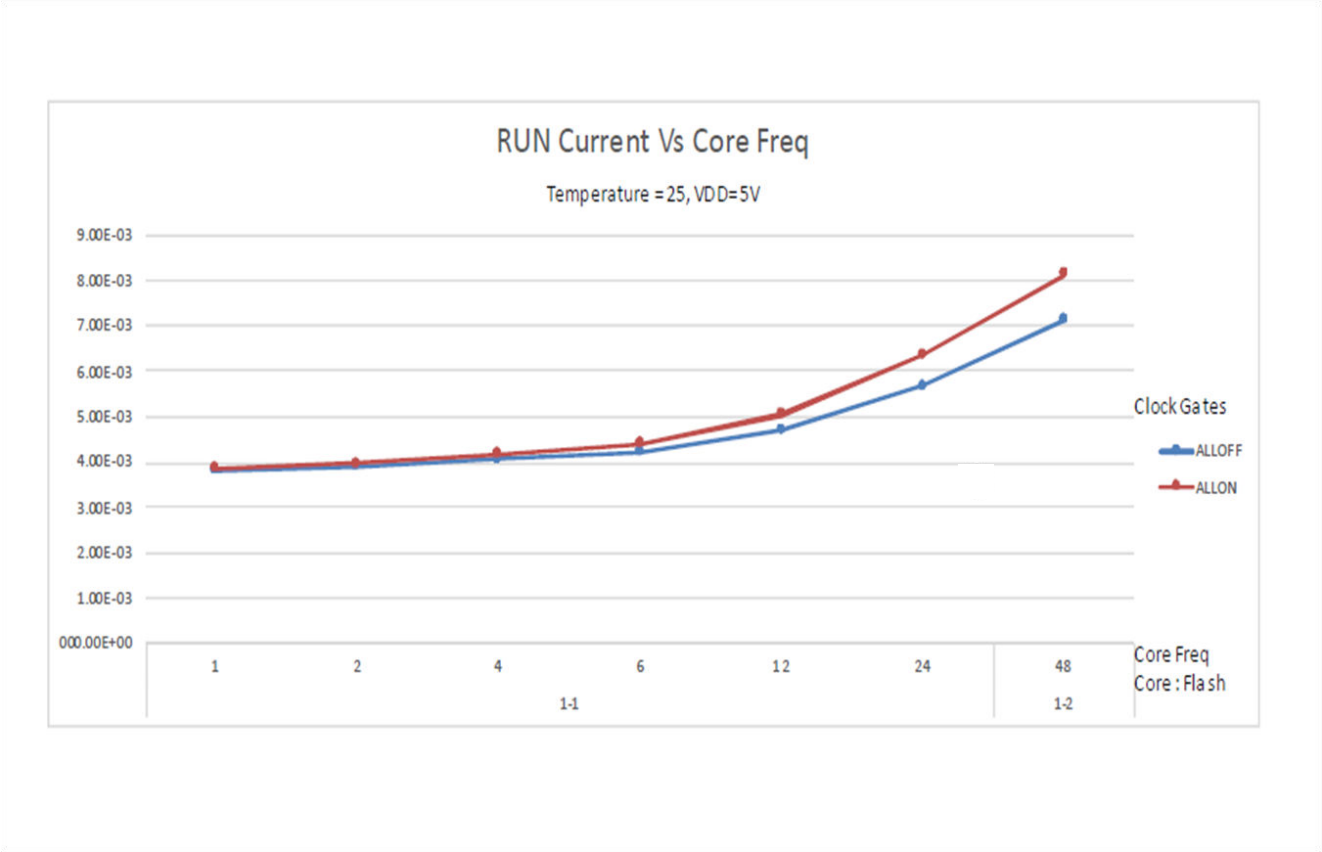



**Figure 9. Run mode supply current vs. core frequency**

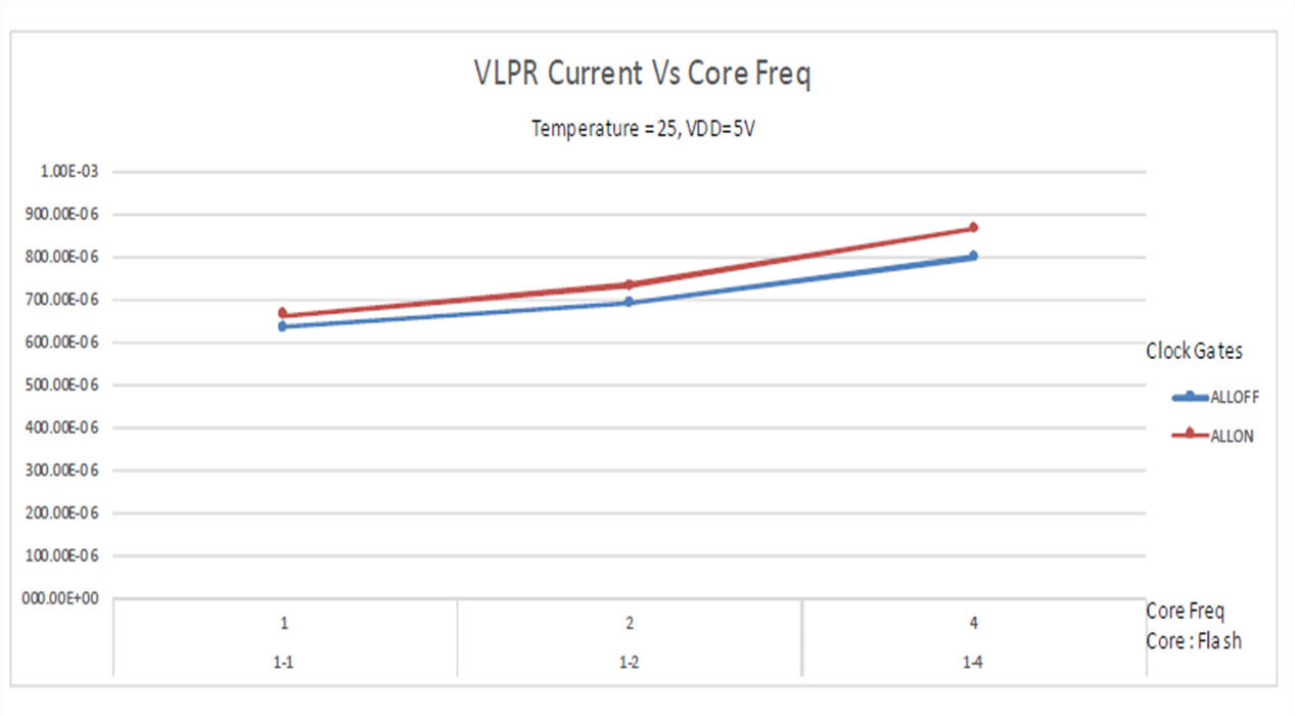



**Figure 10. VLPR mode supply current vs. core frequency**

### 5.3.1.7 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following applications notes, available on http://www.nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

#### 5.3.1.7.1 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

#### 5.3.1.7.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.
3. Select the "Documents" category and find the application notes.

### 5.3.1.8 Capacitance attributes

**Table 31. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN\_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN\_D}$ | Input capacitance: digital pins | — | 7 | pF |

**NOTE**

Please refer to External Oscillator electrical specifications for EXTAL/XTAL pins.

## 5.3.2 Switching specifications

### 5.3.2.1 Device clock specifications

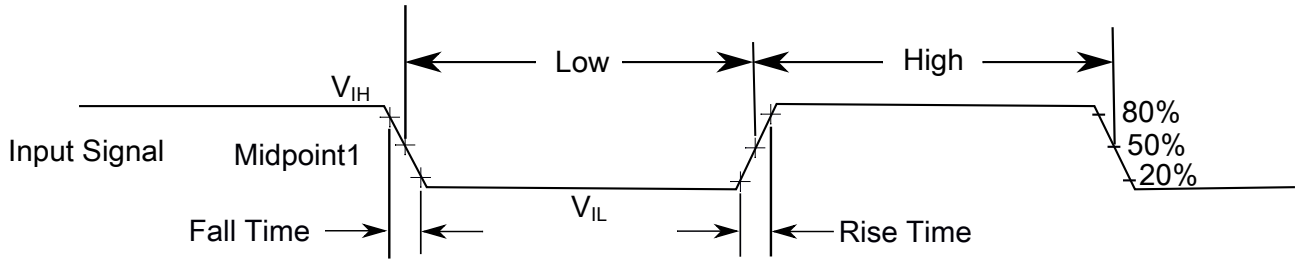
**Table 32. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Normal run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 48 | MHz | |
| $f_{BUS}$ | Bus clock | — | 24 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 25 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 48 | MHz | |
| VLPR / VLPW mode[1] | | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz | |
| $f_{BUS}$ | Bus clock | — | 1 | MHz | |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz | |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz | |
| $f_{LPTMR}$ | LPTMR clock | — | 13 | MHz | |

1. The frequency limitations in VLPR / VLPW mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2.2 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.




The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

**Figure 11. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L$=30 pF loads
- Normal drive strength

### 5.3.2.3 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

**Table 33. General switching specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 3 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path | 50 | — | ns | 4 |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.

### 5.3.2.4 AC specifications at 3.3 V range

**Table 34. Functional pad AC specifications**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| I/O Supply Voltage | Vdd [1] | 2.7 | | 4 | V |

1. Max power supply ramp rate is 500 V/ms.

| Name | Prop Delay (ns) [1] | Rise/Fall Edge (ns) [2] | | Drive Load (pF) |
|---|---|---|---|---|
| | Max | Min | Max | |
| Normal drive I/O pad | 17.5 | 5 | 17 | 25 |
| | 28 | 9 | 32 | 50 |
| High drive I/O pad | 19 | 5 | 17 | 25 |
| | 26 | 9 | 33 | 50 |
| CMOS Input [3] | 4 | 1.2 | 3 | 0.5 |

1. Propagation delay measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

**NOTE**

All measurements were taken accounting for 150 mV drop across VDD and VSS.

### 5.3.2.5 AC specifications at 5 V range

**Table 35. Functional pad AC specifications**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| I/O Supply Voltage | Vdd [1] | 4 | | 5.5 | V |

1. Max power supply ramp rate is 500 V/ms.

| Name | Prop Delay (ns) [1] | Rise/Fall Edge (ns) [2] | | Drive Load (pF) |
|---|---|---|---|---|
| | Max | Min | Max | |
| Normal drive I/O pad | 12 | 3.6 | 10 | 25 |
| | 18 | 8 | 17 | 50 |
| High drive I/O pad | 13 | 3.6 | 10 | 25 |
| | 19 | 8 | 19 | 50 |
| CMOS Input [3] | 3 | 1.2 | 2.8 | 0.5 |

1. As measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

**NOTE**

All measurements were taken accounting for 150 mV drop across VDD and VSS.

## 5.3.3 Thermal specifications

### 5.3.3.1 Thermal operating requirements

**Table 36. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C | |
| $T_A$ | Ambient temperature | –40 | 105 | °C | 1 |

1. Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed maximum $T_J$. The simplest method to determine $T_J$ is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

### 5.3.3.2 Thermal attributes

#### 5.3.3.2.1 Description

The tables in the following sections describe the thermal characteristics of the device.

**NOTE**

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

#### 5.3.3.2.2 Thermal characteristics for the 44-pin LQFP package

**Table 37. Thermal characteristics for the 44-pin LQFP package**

| Rating | Conditions | Symbol | Value | Unit |
|---|---|---|---|---|
| Thermal resistance, Junction to Ambient (Natural Convection)[1, 2] | Single layer board (1s) | $R_{\theta JA}$ | 74 | °C/W |
| Thermal resistance, Junction to Ambient (Natural Convection)[1, 2] | Four layer board (2s2p) | $R_{\theta JA}$ | 52 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3] | Single layer board (1s) | $R_{\theta JMA}$ | 61 | °C/W |

*Table continues on the next page...*

**Table 37. Thermal characteristics for the 44-pin LQFP package (continued)**

| Rating | Conditions | Symbol | Value | Unit |
|---|---|---|---|---|
| Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3] | Four layer board (2s2p) | $R_{\theta JMA}$ | 45 | °C/W |
| Thermal resistance, Junction to Board[4] | — | $R_{\theta JB}$ | 32 | °C/W |
| Thermal resistance, Junction to Case [5] | — | $R_{\theta JC}$ | 19 | °C/W |
| Thermal resistance, Junction to Package Top[6] | Natural Convection | $\psi_{JT}$ | 5 | °C/W |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

### 5.3.3.2.3 Thermal characteristics for the 48-pin LQFP package

**Table 38. Thermal characteristics for the 48-pin LQFP package**

| Rating | Conditions | Symbol | Value | Unit |
|---|---|---|---|---|
| Thermal resistance, Junction to Ambient (Natural Convection)[1, 2] | Single layer board (1s) | $R_{\theta JA}$ | 79 | °C/W |
| Thermal resistance, Junction to Ambient (Natural Convection)[1, 2] | Four layer board (2s2p) | $R_{\theta JA}$ | 55 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3] | Single layer board (1s) | $R_{\theta JMA}$ | 66 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3] | Four layer board (2s2p) | $R_{\theta JMA}$ | 49 | °C/W |
| Thermal resistance, Junction to Board[4] | — | $R_{\theta JB}$ | 33 | °C/W |
| Thermal resistance, Junction to Case [5] | — | $R_{\theta JC}$ | 23 | °C/W |
| Thermal resistance, Junction to Package Top[6] | Natural Convection | $\psi_{JT}$ | 6 | °C/W |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

#### 5.3.3.2.4 Thermal characteristics for the 40-pin QFN package

**Table 39. Thermal characteristics for the 40-pin QFN package**

| Rating | Board Type [1] | Symbol | Value | Unit |
|---|---|---|---|---|
| Junction to Ambient Thermal Resistance [2] | JESD51-9, 2s2p | $R_{\theta JA}$ | 28.6 | °C/W |
| Junction-to-Top of Package Thermal Characterization Parameter [2] | JESD51-9, 2s2p | $\Psi_{JT}$ | 0.2 | °C/W |
| Junction to Case Thermal Resistance [3] | JESD51-9 | $R_{\theta JC}$ | 1.6 | °C/W |

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction-to-Case thermal resistance determined using an isothermal cold plate. Case is defined as the bottom of the packages (exposed pad).

#### 5.3.3.2.5 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, $T_J$, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- $T_A$ = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $P_D$ = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- $T_T$ = thermocouple temperature on top of the package (°C)
- $\Psi_{JT}$ = thermal characterization parameter (°C/W)
- $P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 5.4 Peripheral operating requirements and behaviors

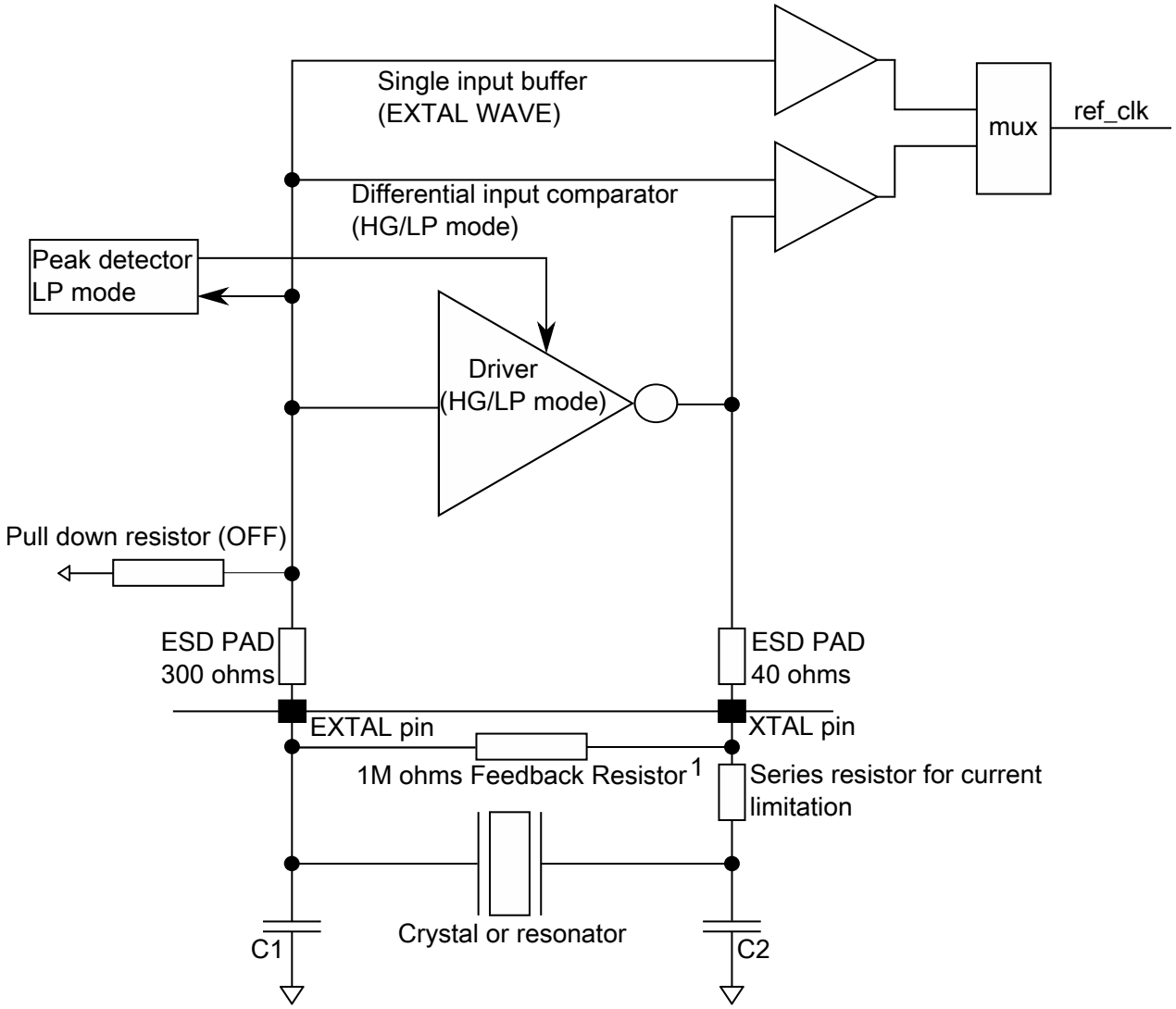
### 5.4.1 System modules

There are no specifications necessary for the device's system modules.

### 5.4.2 Clock interface modules

#### 5.4.2.1 Oscillator electrical specifications

##### 5.4.2.1.1 External Oscillator electrical specifications




NOTE:

1. 1M Feedback resistor is needed only for HG mode.

**Figure 12. Oscillator connections scheme (OSC)**

## NOTE

Data values in the following "External Oscillator electrical specifications" tables are from simulation.

**Table 40. External Oscillator electrical specifications (OSC)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.7 | — | 5.5 | V | |
| $I_{DDOSC}$ | Supply current — low-gain mode (low-power mode) (HGO=0) | | | | | 1 |
| | 4 MHz | — | 200 | — | µA | |
| | 8 MHz | — | 300 | — | µA | |

*Table continues on the next page...*

## Table 40. External Oscillator electrical specifications (OSC) (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | 16 MHz | — | 1.2 | — | mA | |
| | 24 MHz | — | 1.6 | — | mA | |
| | 32 MHz | — | 2 | — | mA | |
| | 40 MHz | — | 2.6 | — | mA | |
| $I_{DDOSC}$ | Supply current — high-gain mode (HGO=1) | | | | | 1 |
| | 32 kHz | — | 25 | — | µA | |
| | 4 MHz | — | 1 | — | mA | |
| | 8 MHz | — | 1.2 | — | mA | |
| | 16 MHz | — | 3.5 | — | mA | |
| | 24 MHz | — | 5 | — | mA | |
| | 32 MHz | — | 5.5 | — | mA | |
| | 40 MHz | — | 6 | — | mA | |
| $g_{mXOSC}$ | Fast external crystal oscillator transconductance | | | | | |
| | 32 kHz, Low Frequency Range, High Gain (32 kHz) | 15 | — | 45 | µA / V | |
| | Medium Frequency Range (4-8 MHz) | 2.2 | — | 9.7 | mA / V | |
| | High Frequency Range (8-40 MHz) | 16 | | 37 | mA / V | |
| $V_{IH}$ | Input high voltage — EXTAL pin in external clock mode | 1.75 | — | $V_{DD}$ | V | |
| $V_{IL}$ | Input low voltage — EXTAL pin in external clock mode | $V_{SS}$ | — | 1.20 | V | |
| $C_1$ | EXTAL load capacitance | — | — | — | | 2 |
| $C_2$ | XTAL load capacitance | — | — | — | | 2 |
| $R_F$ | Feedback resistor | | | | | 3 |
| | Low-frequency, high-gain mode (32 kHz) | — | 10 | — | MΩ | |
| | Medium/high-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz) | — | — | — | MΩ | |
| | Medium/high-frequency, high-gain mode (4-8 MHz, 8-40 MHz) | — | 1 | — | MΩ | |
| $R_S$ | Series resistor | | | | | |
| | Low-frequency, high-gain mode (32 kHz) | — | 200 | — | kΩ | |
| | Medium/high-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz) | — | 0 | — | kΩ | |
| | Medium/high-frequency, high-gain mode (4-8 MHz, 8-40 MHz) | — | 0 | — | kΩ | |
| $V_{pp}$ | Peak-to-peak amplitude of oscillation (oscillator mode) | | | | | 4 |
| | Low-frequency, high-gain mode | — | 3.3 | — | V | |
| | Medium/high-frequency, low-gain mode | — | 1.0 | — | V | |
| | Medium/high-frequency, high-gain mode | — | 3.3 | — | V | |

1. Measured at $V_{DD}$ = 5 V, Temperature = 25 °C. The current consumption is according to the crystal or resonator, loading capacitance.

2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values. And also consider the parasitic capacitance of package and board.
3. When low power mode is selected, $R_F$ is integrated and must not be attached externally.
4. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

#### 5.4.2.1.2 External Oscillator frequency specifications

**Table 41. External Oscillator frequency specifications (OSC)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — Low Frequency, High Gain Mode | 32 | — | 40 | kHz | |
| $f_{osc\_me}$ | Oscillator crystal or resonator frequency — Medium Frequency | 4 | — | 8 | MHz | |
| $f_{osc\_hi}$ | Oscillator crystal or resonator frequency — High Frequency | 8 | — | 40 | | |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | |
| $t_{cst}$ | Crystal startup time — 32 kHz Low Frequency, High-Gain Mode | — | 500 | — | ms | 1 |
| | Crystal startup time — 8 MHz Medium Frequency, Low-Power Mode | — | 1.5 | — | | |
| | Crystal startup time — 8 MHz Medium Frequency, High-Gain Mode | — | 2.5 | — | | |
| | Crystal startup time — 40 MHz High Frequency, Low-Power Mode | — | 2 | — | | |
| | Crystal startup time — 40 MHz High Frequency, High-Gain Mode | — | 2.5 | — | | |

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

### 5.4.2.2 System Clock Generation (SCG) specifications

#### 5.4.2.2.1 Fast internal RC Oscillator (FIRC) electrical specifications

**Table 42. Fast internal RC Oscillator electrical specifications**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $F_{FIRC}$ | Fast internal reference frequency | — | 48 | — | MHz |
| $I_{VDD}$ | Supply current | — | 400 | 500 | µA |
| $F_{Untrimmed}$ | IRC frequency (untrimmed) | $F_{IRC}$× (1-0.3) | — | $F_{IRC}$× (1+0.3) | MHz |

*Table continues on the next page...*

**Table 42. Fast internal RC Oscillator electrical specifications (continued)**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $\Delta F_{OL}$ | Open loop total deviation of IRC frequency over voltage and temperature[1] | | | | |
| | Regulator enable | — | ±0.5 | ±1 | $\%F_{FIRC}$ |
| $T_{Startup}$ | Startup time | | — | 3 | µs[2] |
| $T_{JIT}$ | Period jitter (RMS) | — | 35 | 150 | ps |

1. The limit is respected across process, voltage and full temperature range.
2. Startup time is defined as the time between clock enablement and clock availability for system use.

**NOTE**

Fast internal RC Oscillator is compliant with CAN and LIN standards.

### 5.4.2.2.2 Slow internal RC oscillator (SIRC) electrical specifications

**Table 43. Slow internal RC oscillator (SIRC) electrical specifications**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $F_{SIRC}$ | Slow internal reference frequency | — | 2<br>8 | — | MHz |
| $I_{VDD}$ | Supply current | — | 23 | — | µA |
| $F_{Untrimmed}$ | IRC frequency (untrimmed) | — | — | — | MHz |
| $\Delta F_{OL}$ | Open loop total deviation of IRC frequency over voltage and temperature[1] | | | | |
| | Regulator enable | — | — | ±3 | $\%F_{SIRC}$ |
| $T_{Startup}$ | Startup time | — | 6 | — | µs[2] |

1. The limit is respected across process, voltage and full temperature range.
2. Startup time is defined as the time between clock enablement and clock availability for system use.

### 5.4.2.2.3 Low Power Oscillator (LPO) electrical specifications

**Table 44. Low Power Oscillator (LPO) electrical specifications**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{LPO}$ | Internal low power oscillator frequency | 113 | 128 | 139 | kHz |
| $I_{LPO}$ | Current consumption | 1 | 3 | 7 | µA |
| $T_{startup}$ | Startup Time | — | — | 20 | µs |

#### 5.4.2.2.4 LPFLL electrical specifications

**Table 45. LPFLL electrical specifications**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{avg}$ | Power consumption | | 240 | | µA |
| $T_{start}$ | Start-up time | | 3.6 | | µs |
| $\Delta F_{ol}$ | Frequency accuracy over temperature and voltage in open loop after process trimmed | –10 | — | 10 | % |
| $\Delta F_{cl}$ | Frequency accuracy in closed loop | –1 [1] | — | 1 [1] | % |

1. $\Delta F_{cl}$ is dependent on reference clock accuracy. For example, if locked to crystal oscillator, $\Delta F_{cl}$ is typically limited by trimming ability of the module itself; if locked to other clock source which has 3% accuracy, then $\Delta F_{cl}$ can only be ±3%.

## 5.4.3 Memories and memory interfaces

### 5.4.3.1 Flash memory module (FTFA) electrical specifications

This section describes the electrical characteristics of the flash memory module (FTFA).

#### 5.4.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 46. NVM program/erase timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{hvpgm4}$ | Longword Program high-voltage time | — | 7.5 | 18 | µs | — |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 52 | 452 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

#### 5.4.3.1.2 Flash timing specifications — commands

**Table 47. Flash command timing specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{rd1sec1k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | µs | 1 |
| $t_{pgmchk}$ | Program Check execution time | — | — | 45 | µs | 1 |
| $t_{rdrsrc}$ | Read Resource execution time | — | — | 30 | µs | 1 |
| $t_{pgm4}$ | Program Longword execution time | — | 65 | 145 | µs | — |

*Table continues on the next page...*

**Table 47. Flash command timing specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{ersscr}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| $t_{rd1all}$ | Read 1s All Blocks execution time | — | — | 0.9 | ms | 1 |
| $t_{rdonce}$ | Read Once execution time | — | — | 25 | µs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | µs | — |
| $t_{ersall}$ | Erase All Blocks execution time | — | 70 | 575 | ms | 2 |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | — | — | 30 | µs | 1 |
| $t_{ersallu}$ | Erase All Blocks Unsecure execution time | — | 70 | 575 | ms | 2 |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

#### 5.4.3.1.3 Flash high voltage current behaviors

**Table 48. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

#### 5.4.3.1.4 Reliability specifications

**Table 49. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | — |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | — |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ $T_j$ ≤ 125 °C.

### 5.4.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

# 5.4.5 Analog

## 5.4.5.1 ADC electrical specifications

### 5.4.5.1.1 12-bit ADC operating conditions

**Table 50. 12-bit ADC operating conditions**

| Symbol | Description | Conditions | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Absolute | 2.7 | — | 5.5 | V | |
| $\Delta V_{DDA}$ | Supply voltage | Delta to $V_{DD}$ ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| $\Delta V_{SSA}$ | Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| $V_{REFH}$ | ADC reference voltage high | | 2.5 | $V_{DDA}$ | $V_{DDA}$ + 100m | V | 3 |
| $V_{REFL}$ | ADC reference voltage low | | – 100 | 0 | 100 | mV | 3 |
| $V_{ADIN}$ | Input voltage | | $V_{REFL}$ | — | $V_{REFH}$ | V | |
| $R_S$ | Source impedendance | $f_{ADCK}$ < 4 MHz | — | — | 5 | kΩ | |
| $R_{SW1}$ | Channel Selection Switch Impedance | | — | 0.5 | 1.2 | kΩ | |
| $R_{AD}$ | Sampling Switch Impedance | | — | 2 | 5 | kΩ | |
| $C_{P1}$ | Pin Capacitance | | — | 3 | — | pF | |
| $C_{P2}$ | Analog Bus Capacitance | | — | — | 5 | pF | |
| $C_S$ | Sampling capacitance | | — | 4 | 5 | pF | |
| $f_{ADCK}$ | ADC conversion clock frequency | | 2 | 40 | 48 | MHz | 4, 5 |
| $C_{rate}$ | ADC conversion rate | No ADC hardware averaging[6] Continuous conversions enabled, subsequent conversion time | 20 | — | 1200 | Ksps | 7 |

1. Typical values assume $V_{DDA}$ = 5 V, Temp = 25 °C, $f_{ADCK}$ = 40 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated $V_{REFH}$ and $V_{REFL}$ pins, $V_{REFH}$ is internally tied to $V_{DDA}$, and $V_{REFL}$ is internally tied to $V_{SSA}$.
4. Clock and compare cycle need to be set according the guidelines in the block guide.
5. ADC conversion will become less reliable above maximum frequency.
6. When using ADC hardware averaging, refer to the device *Reference Manual* to determine the most appropriate setting for AVGS.
7. Max ADC conversion rate of 1200 Ksps is with 10-bit mode

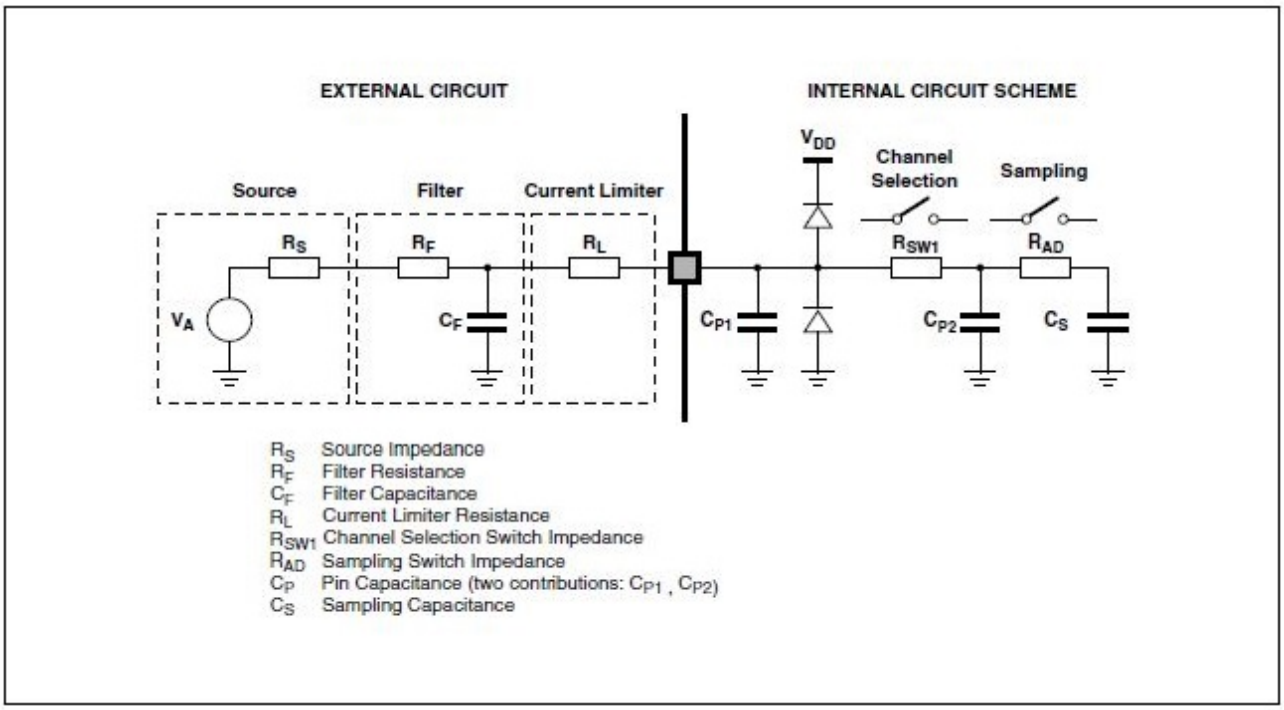



**Figure 13. ADC input impedance equivalency diagram**

#### 5.4.5.1.2 12-bit ADC electrical characteristics

**NOTE**

All the parameters in the table are given assuming system clock as the clocking source for ADC.

**NOTE**

For ADC signals adjacent to VDD/VSS or the XTAL pins some degradation in the ADC performance may be observed.

**NOTE**

All values guarantee the performance of the ADC for the multiple ADC input channel pins. When using the ADC to monitor the internal analogue parameters, please assume minor degradation.

**Table 51. 12-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$)**

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max.[3] | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $I_{DDA\_ADC}$ | Supply current at 2.7 to 5.5 V | | 470 | 515 µA @ 5 V | 560 | µA | 4 |

*Table continues on the next page...*

## Table 51. 12-bit ADC characteristics ($V_{REFH}$ = $V_{DDA}$, $V_{REFL}$ = $V_{SSA}$) (continued)

| Symbol | Description | Conditions[1] | Min. | Typ.[2] | Max.[3] | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | Sample Time | | 275 | — | Refer to the device's *Reference Manual* | ns | |
| TUE | Total unadjusted error at 2.7 to 5.5 V | | — | ±4.5 | ±6.11 | LSB[5] | 6 |
| DNL | Differential non-linearity at 2.7 to 5.5 V | | — | ±0.8 | ±1.07 | LSB[5] | 6 |
| INL | Integral non-linearity at 2.7 to 5.5 V | | — | ±1.4 | ±3.54 | LSB[5] | 6 |
| $E_{FS}$ | Full-scale error at 2.7 to 5.5 V | | — | –2 | -3.60 | LSB[5] | $V_{ADIN}$ = $V_{DDA}$[6] |
| $E_{ZS}$ | Zero-scale error at 2.7 to 5.5 V | | — | –2.7 | -4.24 | LSB[5] | |
| $E_Q$ | Quantization error at 2.7 to 5.5 V | | — | — | ±0.5 | LSB[5] | |
| ENOB | Effective number of bits at 2.7 to 5.5 V | | — | 11.3 | — | bits | 7 |
| SINAD | Signal-to-noise plus distortion at 2.7 to 5.5 V | See ENOB | — | 70 | — | dB | SINAD = 6.02 × ENOB + 1.76 |
| $E_{IL}$ | Input leakage error at 2.7 to 5.5 V | | $I_{In}$ × $R_{AS}$ | | | mV | $I_{In}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
| $V_{TEMP\_S}$ | Temp sensor slope at 2.7 to 5.5 V | Across the full temperature range of the device | 1.492 | 1.564 | 1.636 | mV/°C | 8, 9 |
| $V_{TEMP25}$ | Temp sensor voltage at 2.7 to 5.5 V | 25 °C | 730 | 740.5 | 751 | mV | 8, 9 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$ = $V_{DDA}$
2. Typical values assume $V_{DDA}$ = 5.0 V, Temp = 25 °C, $f_{ADCK}$ = 48 MHz unless otherwise stated.
3. These values are based on characterization but not covered by test limits in production.
4. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
5. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/$2^N$
6. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
7. Input data is 100 Hz sine wave. ADC conversion clock < 40 MHz.
8. ADC conversion clock < 3 MHz
9. The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

### 5.4.5.2 CMP with 8-bit DAC electrical specifications

**Table 52. Comparator with 8-bit DAC electrical specifications**

| Symbol | Description | Min. | Typ. [1] | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.7 | — | 5.5 | V |
| $I_{DDHS}$ | Supply current, High-speed mode[2] | | | | µA |
| | within ambient temperature range | — | 145 | 200 | |
| $I_{DDLS}$ | Supply current, Low-speed mode[2] | | | | µA |
| | within ambient temperature range | — | 5 | 10 | |
| $V_{AIN}$ | Analog input voltage | 0 | 0 - $V_{DDX}$ | $V_{DDX}$ | V |
| $V_{AIO}$ | Analog input offset voltage, High-speed mode | | | | mV |
| | within ambient temperature range | -25 | ±1 | 25 | |
| $V_{AIO}$ | Analog input offset voltage, Low-speed mode | | | | mV |
| | within ambient temperature range | -40 | ±4 | 40 | |
| $t_{DHSB}$ | Propagation delay, High-speed mode[3] | | | | ns |
| | within ambient temperature range | — | 30 | 200 | |
| $t_{DLSB}$ | Propagation delay, Low-speed mode[3] | | | | µs |
| | within ambient temperature range | — | 0.5 | 2 | |
| $t_{DHSS}$ | Propagation delay, High-speed mode[4] | | | | ns |
| | within ambient temperature range | — | 70 | 400 | |
| $t_{DLSS}$ | Propagation delay, Low-speed mode[4] | | | | µs |
| | within ambient temperature range | — | 1 | 5 | |
| $t_{IDHS}$ | Initialization delay, High-speed mode [3] | | | | µs |
| | within ambient temperature range | — | 1.5 | 3 | |
| $t_{IDLS}$ | Initialization delay, Low-speed mode[3] | | | | µs |
| | within ambient temperature range | — | 10 | 30 | |
| $V_{HYST0}$ | Analog comparator hysteresis, Hyst0 ($V_{AIO}$) | | | | mV |
| | within ambient temperature range | — | 0 | — | |
| $V_{HYST1}$ | Analog comparator hysteresis, Hyst1, High-speed mode | | | | mV |
| | within ambient temperature range | — | 16 | 53 | |
| | Analog comparator hysteresis, Hyst1, Low-speed mode | | | | |
| | within ambient temperature range | — | 11 | 30 | |
| $V_{HYST2}$ | Analog comparator hysteresis, Hyst2, High-speed mode | | | | mV |
| | within ambient temperature range | — | 32 | 90 | |
| | Analog comparator hysteresis, Hyst2, Low-speed mode | | | | |
| | within ambient temperature range | — | 22 | 53 | |
| $V_{HYST3}$ | Analog comparator hysteresis, Hyst3, High-speed mode | | | | mV |

*Table continues on the next page...*

## Table 52. Comparator with 8-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. [1] | Max. | Unit |
|---|---|---|---|---|---|
| | within ambient temperature range | — | 48 | 133 | |
| | Analog comparator hysteresis, Hyst3, Low-speed mode | | | | |
| | within ambient temperature range | — | 33 | 80 | |
| $I_{DAC8b}$ | 8-bit DAC current adder (enabled) | — | 10 | 16 | μA |
| INL | 8-bit DAC integral non-linearity | –0.6 | — | 0.5 | LSB[5] |
| DNL | 8-bit DAC differential non-linearity | –0.5 | — | 0.5 | LSB |

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

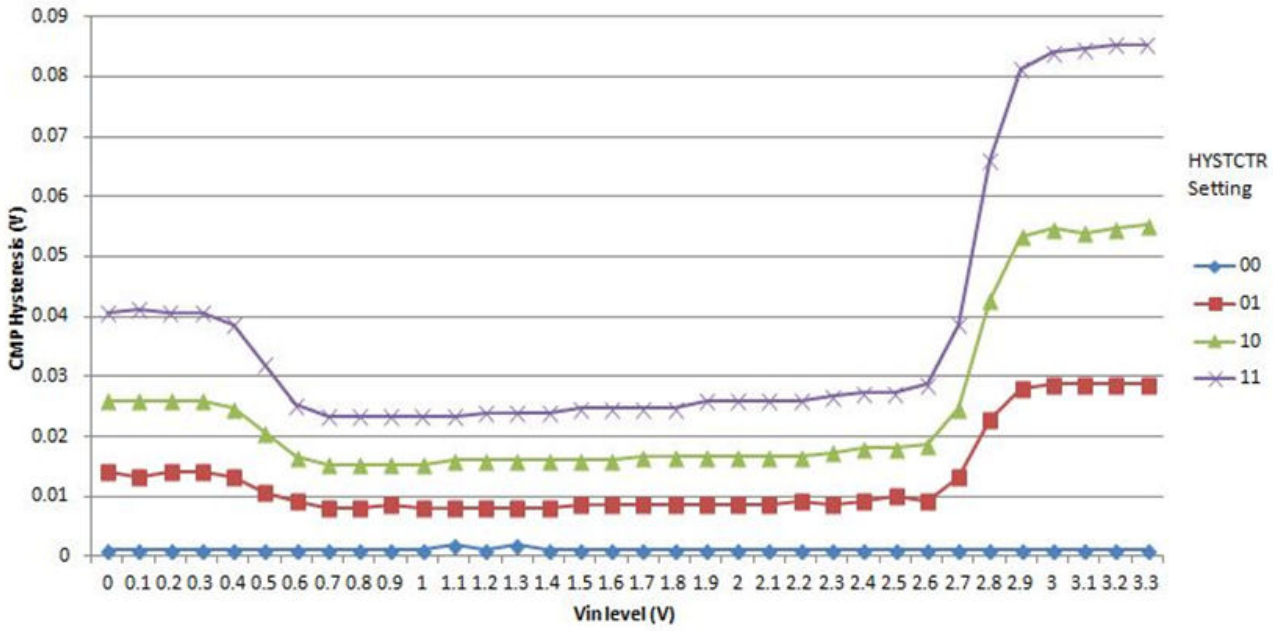



**Figure 14. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**

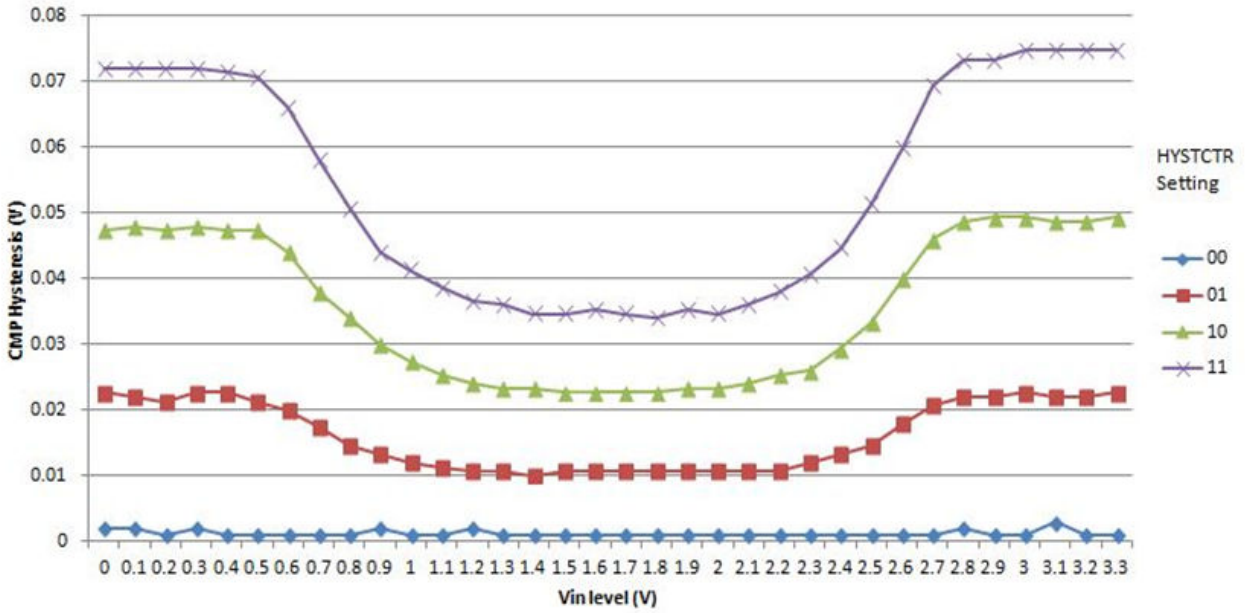



**Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)**

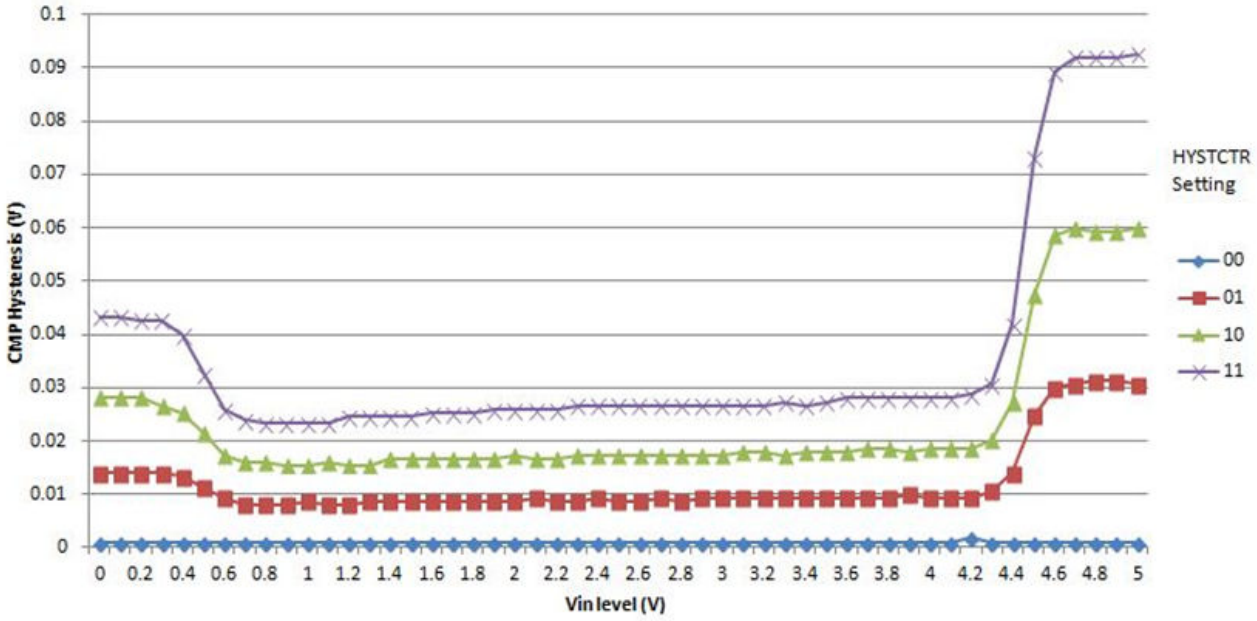



**Figure 16. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 0)**

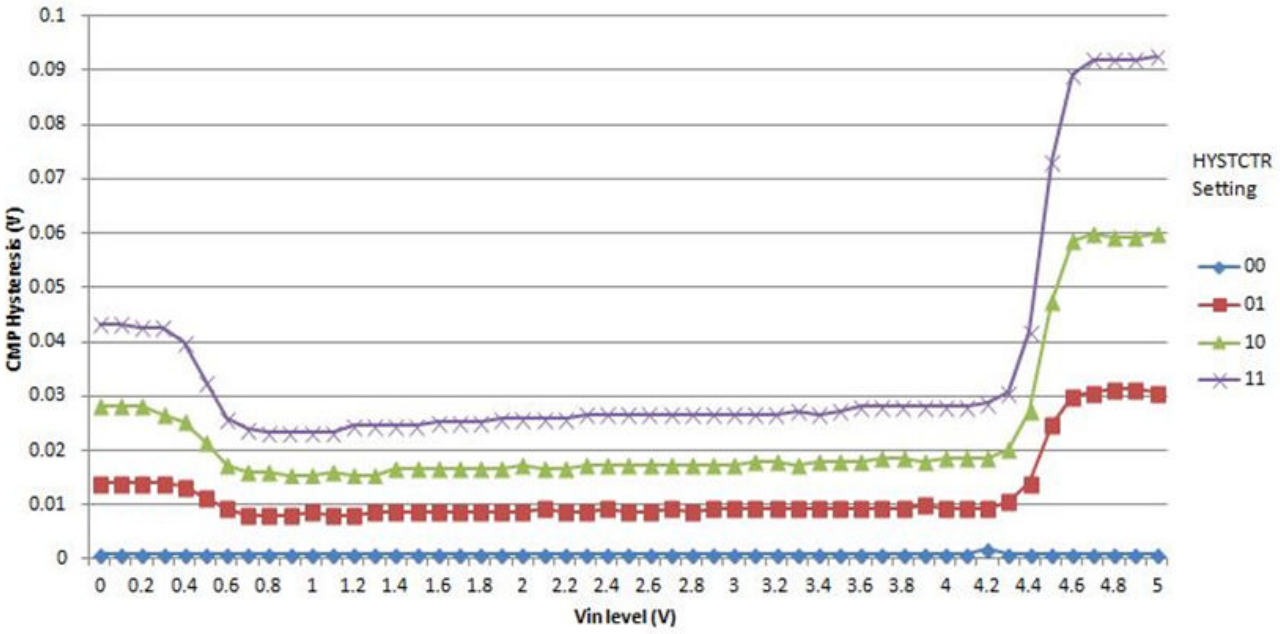



**Figure 17. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 1)**

## 5.4.6 Communication interfaces

### 5.4.6.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

### 5.4.6.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

**Table 53. LPSPI master mode timing**

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{SPSCK}$ | Frequency of SPSCK | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{periph}$ | 2048 x $t_{periph}$ | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |

*Table continues on the next page...*

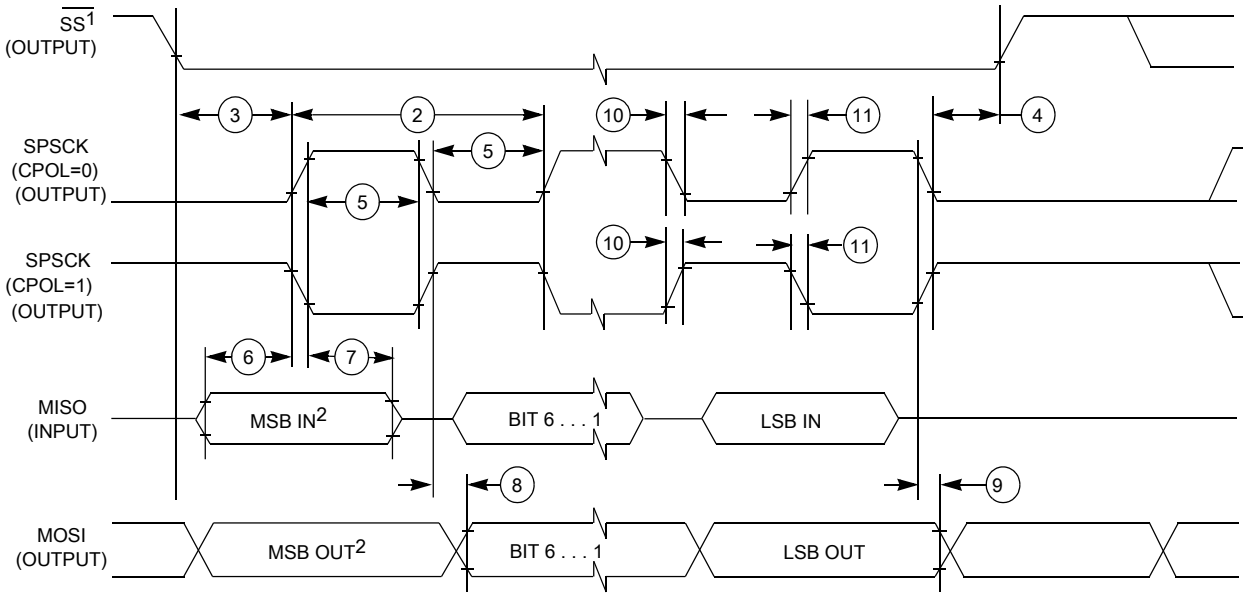
**Table 53. LPSPI master mode timing (continued)**

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | 1024 x $t_{periph}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 18 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_v$ | Data valid (after SPSCK edge) | — | 15 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. $f_{periph}$ is LPSPI peripheral functional clock. On this device, the max value of $f_{SPSCK}$ should not exceed 25 MHz.
2. $t_{periph} = 1/f_{periph}$

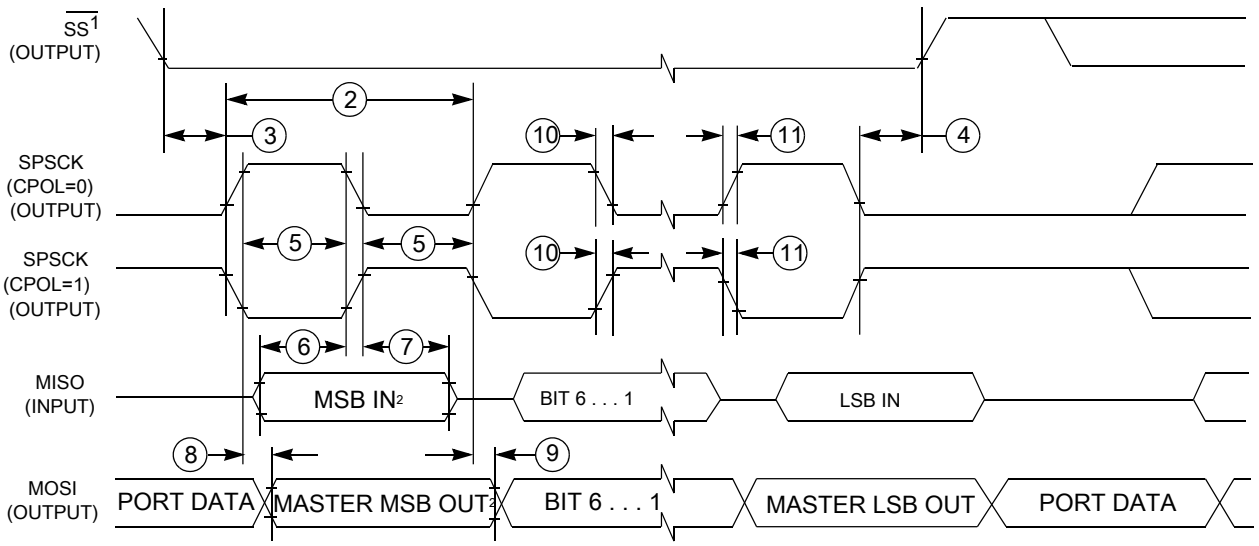
**NOTE**

High drive pin should be used for fast bit rate.




1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 18. LPSPI master mode timing (CPHA = 0)**




1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 19. LPSPI master mode timing (CPHA = 1)**

## Table 54. LPSPI slave mode timing

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | $f_{SPSCK}$ | Frequency of SPSCK | 0 | $f_{periph}/2$ | Hz | 1 |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{periph}$ | — | ns | 2 |
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{periph}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{periph}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{periph}$ | ns | 3 |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{periph}$ | ns | 4 |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 31 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{periph}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

1. $f_{periph}$ is LPSPI peripheral functional clock. On this device, the max value of $f_{SPSCK}$ should not exceed 25 MHz.
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

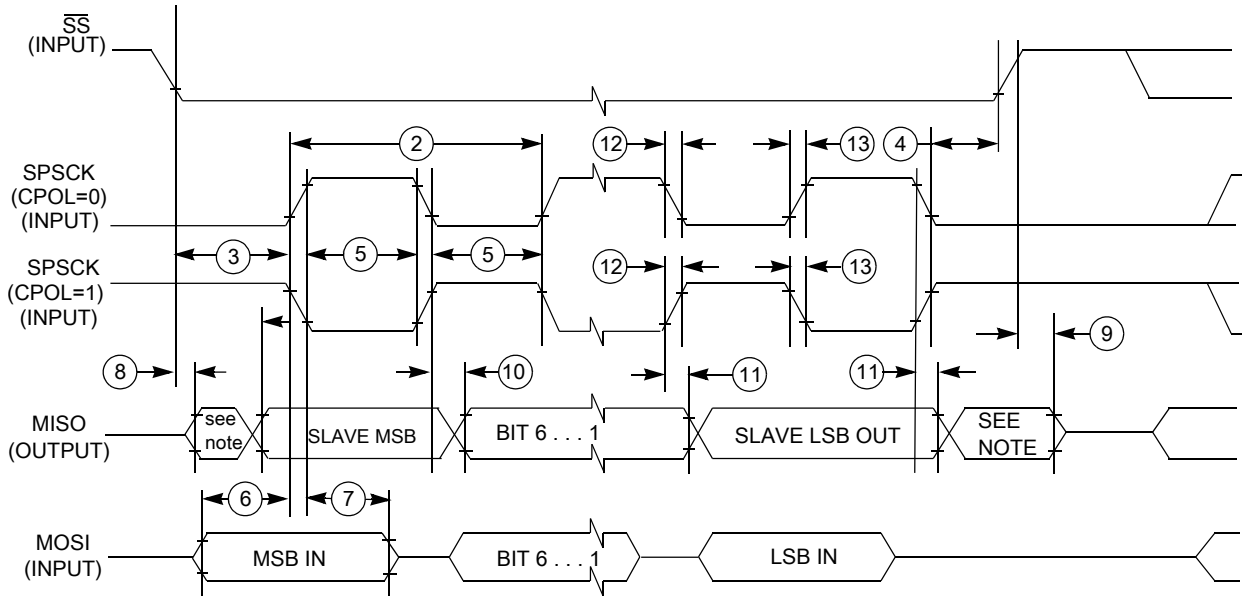



**Figure 20. LPSPI slave mode timing (CPHA = 0)**

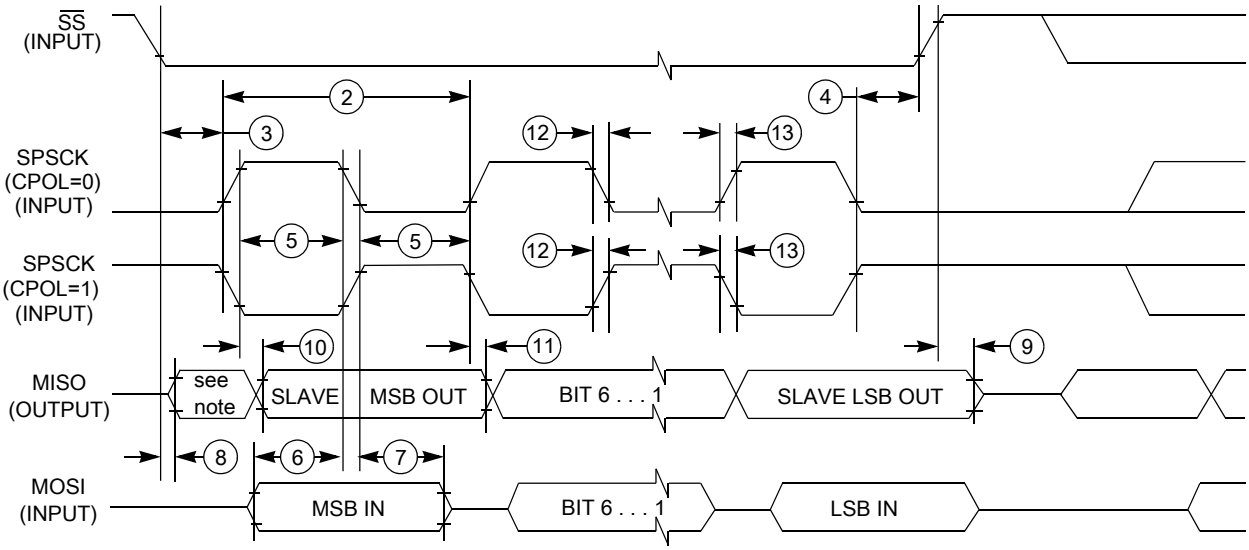



**Figure 21. LPSPI slave mode timing (CPHA = 1)**

## 5.4.6.3 LPI$^2$C

**Table 55. LPI$^2$C specifications**

| Symbol | Description | | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard mode (Sm) | 0 | 100 | kHz | 1, 2, 3 |
| | | Fast mode (Fm) | 0 | 400 | | |
| | | Fast mode Plus (Fm+) | 0 | 1000 | | |
| | | Ultra Fast mode (UFm) | 0 | 5000 | | |
| | | High speed mode (Hs-mode) | 0 | 3400 | | |

1. Hs-mode is only supported in slave mode.
2. The maximum SCL clock frequency in Fast mode with maximum bus loading (400pF) can only be achieved with appropriate pull-up devices on the bus when using the high or normal drive pins across the full voltage range . The maximum SCL clock frequency in Fast mode Plus can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. The maximum SCL clock frequency in Ultra Fast mode can support maximum bus loading (400pF) when using the high drive pins. The maximum SCL clock frequency for slave in High speed mode can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. For more information on the required pull-up devices, see $I^2C$ Bus Specification.
3. See the section "General switching specifications".

## 5.4.6.4 Modular/Scalable Controller Area Network (MSCAN)

**Table 56. MSCAN Timing Parameters**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Baud Rate | $BR_{CAN}$ | — | 1 | Mbit/s |
| CAN Wakeup dominant pulse filtered | $T_{WAKEUP}$ | — | 1.5 | µs |
| CAN Wakeup dominant pulse pass | $T_{WAKEUP}$ | 5 | — | µs |

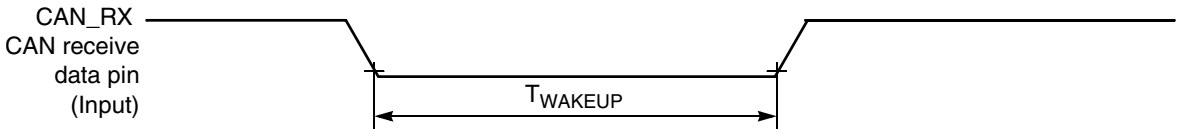



**Figure 22. Bus Wake-up Detection**

## 5.4.7 Human-machine interfaces (HMI)

## 5.4.7.1 Touch sensing input (TSI) electrical specifications

**Table 57. TSI electrical specifications**

| Symbol | Description | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $I_{DD\_EN}$ | Power consumption in operation mode | — | 500 | 600 | µA |
| $I_{DD\_DIS}$ | Power consumption in disable mode | — | 20 | 355 | nA |
| $V_{BG}$ | Internal bandgap reference voltage | — | 1.21 | — | V |
| $V_{PRE}$ | Internal bias voltage | — | 1.51 | — | V |
| $C_I$ | Internal integration capacitance | — | 90 | — | pF |

*Table continues on the next page...*

**Table 57. TSI electrical specifications (continued)**

| Symbol | Description | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $F_{CLK}$ | Internal main clock frequency | — | 16 | — | MHz |

## 5.4.8 Debug modules

### 5.4.8.1 SWD electricals

**Table 58. SWD full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DDA}$ | Operating voltage | 2.7 | 5.5 | V |
| S1 | SWD_CLK frequency of operation | 0 | 25 | MHz |
| S2 | SWD_CLK cycle period | 1/S1 | — | ns |
| S3 | SWD_CLK clock pulse width | 15 | — | ns |
| S4 | SWD_CLK rise and fall times | — | 3 | ns |
| S9 | SWD_DIO input data setup time to SWD_CLK rise | 8 | — | ns |
| S10 | SWD_DIO input data hold time after SWD_CLK rise | 1.4 | — | ns |
| S11 | SWD_CLK high to SWD_DIO data valid | — | 25 | ns |
| S12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

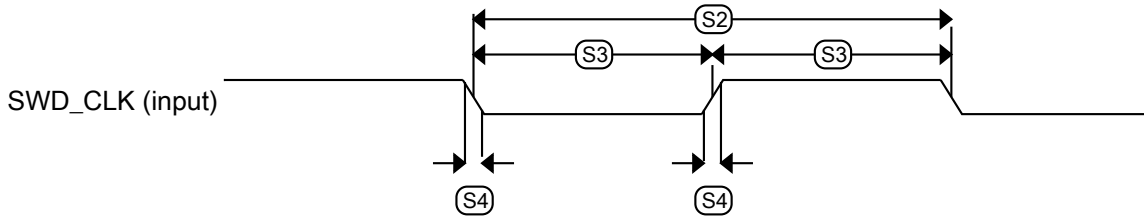



**Figure 23. Serial wire clock input timing**

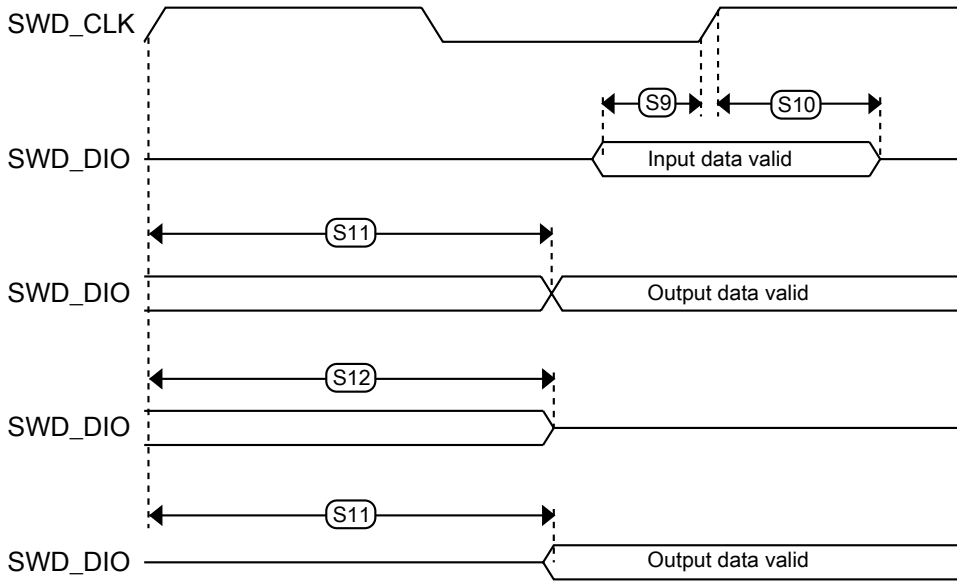



**Figure 24. Serial wire data timing**

# 6 Design considerations

## 6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

### 6.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground. Consider to add ferrite bead or inductor to some sensitive lines.
- Physically isolate analog circuits from digital circuits if possible.

- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

### 6.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Always route the power net as star topology, and make each power trace loop as minimum as possible.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 µF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.

### 6.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

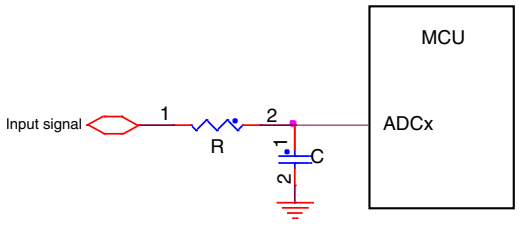



**Figure 25. RC circuit for ADC input**

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. External clamp diodes can be added here to protect against transient over-voltages.

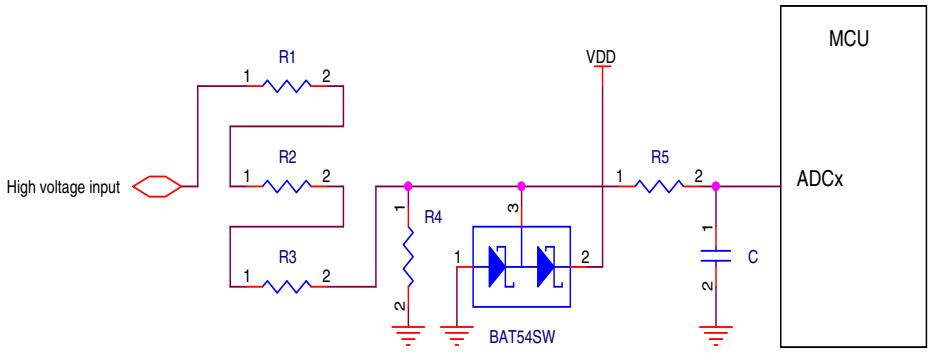



**Figure 26. High voltage measurement with an ADC input**

**NOTE**

For more details of ADC related usage, refer to AN5250: How to Increase the Analog-to-Digital Converter Accuracy in an Application.

### 6.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD+0.3V).

**CAUTION**

Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is a pseudo open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

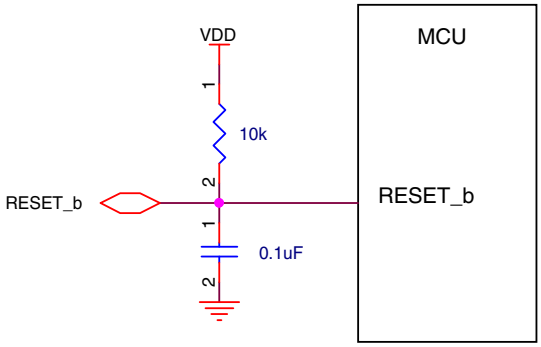



**Figure 27. Reset circuit**

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

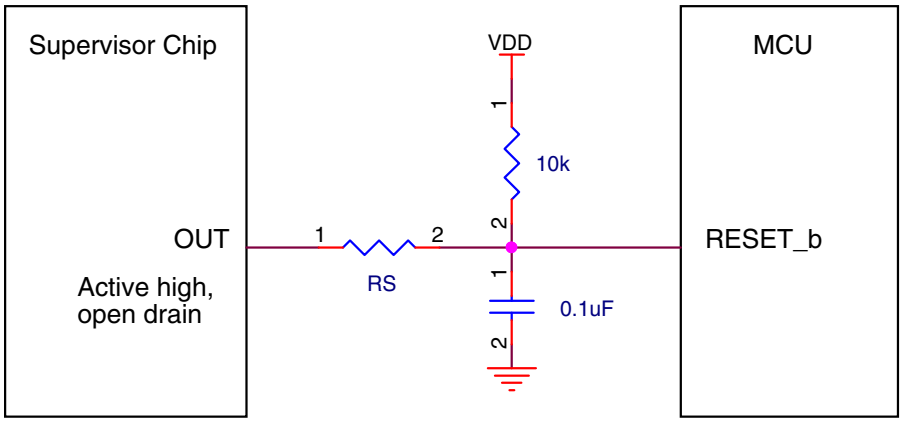



**Figure 28. Reset signal connection to external reset chip**

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

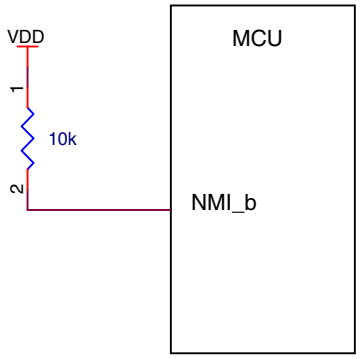



**Figure 29. NMI pin biasing**

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

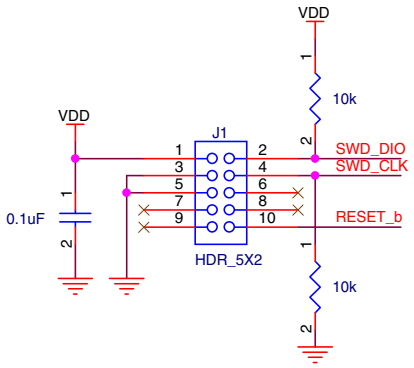



**Figure 30. SWD debug interface**

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

### 6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2 MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2 MHz does not require any series resistance.

**Table 59. External crystal/resonator connections**

| Oscillator mode | Oscillator mode |
|---|---|
| Low frequency (32.768 kHz), high gain | Diagram 3 |
| High frequency (1-32 MHz), low power | Diagram 2 |
| High frequency (1-32 MHz), high gain | Diagram 3 |

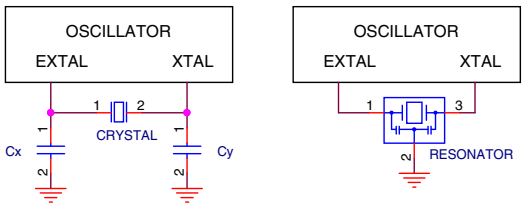



**Figure 31. Crystal connection – Diagram 2**

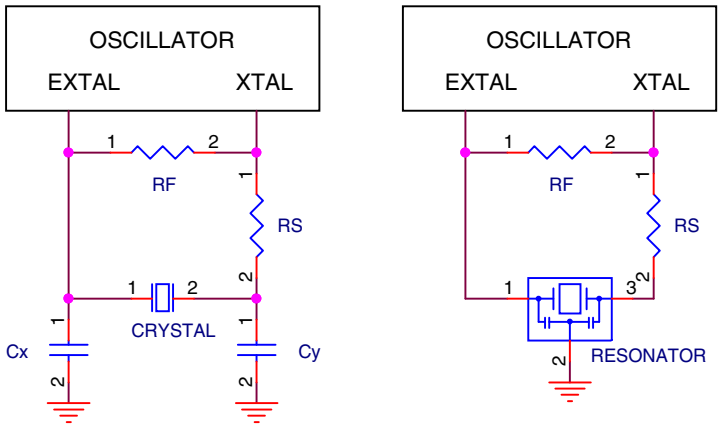



**Figure 32. Crystal connection – Diagram 3**

**NOTE**

For PCB layout, the user could consider to add the guard ring to the crystal oscillator circuit.

## 6.2 Software considerations

All Kinetis MCUs are supported by comprehensive NXP and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.nxp.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Freedom Development Platform: http://www.nxp.com/freedom

IDEs for Kinetis MCUs

- MCUXpresso IDE: https://www.nxp.com/support/developer-resources/software-development-tools/mcuxpresso-software-and-tools/mcuxpresso-integrated-development-environment-ide:MCUXpresso-IDE
- Partner IDEs: http://www.nxp.com/kide

Run-time Software

- MCUXpresso Software Development Kit (SDK): https://www.nxp.com/support/developer-resources/software-development-tools/mcuxpresso-software-and-tools/mcuxpresso-software-development-kit-sdk:MCUXpresso-SDK

For all other partner-developed software and tools, visit http://www.nxp.com/partners.

# 7 Part identification

## 7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 7.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

## 7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

**Table 60. Part number fields description**

| Field | Description | Values |
|---|---|---|
| Q | Qualification status | • M = Fully qualified, general market flow<br>• P = Prequalification |
| KE## | Kinetis family | • KE16, KE15, KE14 |
| A | Key attribute | • Z = Cortex-M0+ |
| FFF | Program flash memory size | • 32 = 32 KB<br>• 64 = 64 KB |
| R | Silicon revision | • (Blank) = Main<br>• A = Revision after main |
| T | Temperature range (°C) | • V = –40 to 105 |
| PP | Package identifier | • LD = 44 LQFP (10 mm x 10 mm)<br>• LF = 48 LQFP (7 mm x 7 mm)<br>• FP = 40 QFN (5 mm x 5 mm) |
| CC | Maximum CPU frequency (MHz) | • 4 = 48 MHz |
| N | Packaging type | • R = Tape and reel<br>• (Blank) = Trays |

## 7.4 Example

This is an example part number:

MKE16Z64VLF4

# 8 Revision history

The following table provides a revision history for this document.

**Table 61. Revision history**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 2 | 01/2019 | Initial public release. |
| 3 | 06/2020 | 40-QFN new package is added. Related sections (Ordering information, Pinout, Package, Power consumption, Thermal characteristics, etc.) are updated. |

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