

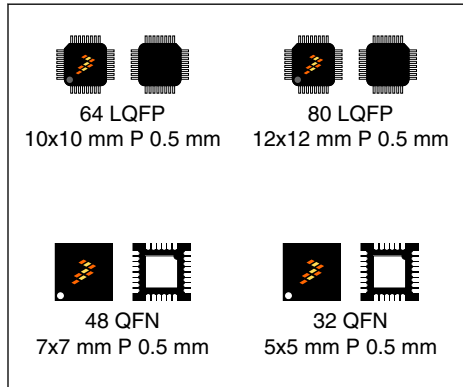
# Kinetis KL13 Microcontroller

48 MHz ARM® Cortex®-M0+ and 64 KB Flash

**MKL13Z32Vxx4**  
**MKL13Z64Vxx4**

The KL13 series is optimized for cost-sensitive and battery-powered applications requiring low-power general purpose connectivity. The product offers:

- Embedded ROM with boot loader for flexible program upgrade
- High accuracy internal voltage and clock reference
- FlexIO to support any standard and customized serial peripheral emulation
- Hardware CRC module
- Down to 60uA/MHz in very low power run mode and 1.83uA in deep sleep mode (RAM + RTC retained)



## Core Processor

- ARM® Cortex®-M0+ core up to 48 MHz

## Memories

- 32/64 KB program flash memory
- 4/8 KB SRAM
- 8 KB ROM with build-in bootloader
- 32-byte backup register

## System

- 4-channel asynchronous DMA controller
- Watchdog
- Low-leakage wakeup unit
- Two-pin Serial Wire Debug (SWD) programming and debug interface
- Micro Trace Buffer
- Bit manipulation engine
- Interrupt controller

## Clocks

- 48 MHz high accuracy (up to 0.5%) internal reference clock
- 8MHz/2MHz high accuracy (up to 3%) internal reference clock
- 1KHz reference clock active under all low-power modes (except VLLS0)
- 32–40KHz and 3–32MHz crystal oscillator

## Peripherals

- One UART module supporting ISO7816, operating up to 1.5 Mbit/s
- Two low-power UART modules supporting asynchronous operation in low-power modes
- Two I2C modules and I2C0 supporting up to 1 Mbit/s
- Two 16-bit SPI modules supporting up to 24 Mbit/s
- One FlexIO module supporting emulation of additional UART, IrDA, SPI, I2C, PWM and other serial modules, etc.
- One 16-bit 818 ksp/s ADC module with high accuracy internal voltage reference (Vref) and up to 20 channels
- High-speed analog comparator containing a 6-bit DAC for programmable reference input
- One 12-bit DAC
- 1.2 V internal voltage reference

## Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- One low-power timer
- Periodic interrupt timer
- Real time clock

### Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

### Packages

- 80 LQFP 12mm x 12mm, 0.5mm pitch, 1.6mm thickness
- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm thickness (Package Your Way)
- 48 QFN 7mm x 7mm, 0.5mm pitch, 0.65mm thickness (Package Your Way)
- 32 QFN 5mm x 5mm, 0.5mm pitch, 0.65mm thickness (Package Your Way)

### Security and Integrity

- 80-bit unique identification number per chip
- Advanced flash security
- Hardware CRC module

### I/O

- Up to 70 general-purpose input/output pins (GPIO) and 4 high-drive pad

### Low Power

- Down to 60uA/MHz in very low power run mode
- Down to 1.83uA in VLLS3 mode (RAM + RTC retained)
- Six flexible static modes

### Ordering Information

| Product      |                       | Memory     |           | Package   |         | IO and ADC channel |                             |                      |
|--------------|-----------------------|------------|-----------|-----------|---------|--------------------|-----------------------------|----------------------|
| Part number  | Marking (Line1/Line2) | Flash (KB) | SRAM (KB) | Pin count | Package | GPIOs              | GPIOs (INT/HD) <sup>1</sup> | ADC channels (SE/DP) |
| MKL13Z32VFM4 | TBD                   | 32         | 4         | 32        | QFN     | 28                 | 28/4                        | 11/2                 |
| MKL13Z64VFM4 | TBD                   | 64         | 8         | 32        | QFN     | 28                 | 28/4                        | 11/2                 |
| MKL13Z32VFT4 | TBD                   | 32         | 4         | 48        | QFN     | 40                 | 40/4                        | 18/3                 |
| MKL13Z64VFT4 | TBD                   | 64         | 8         | 48        | QFN     | 40                 | 40/4                        | 18/3                 |
| MKL13Z32VLH4 | MKL13Z32/VLH4         | 32         | 4         | 64        | LQFP    | 54                 | 54/4                        | 20/4                 |
| MKL13Z64VLH4 | MKL13Z64/VLH4         | 64         | 8         | 64        | LQFP    | 54                 | 54/4                        | 20/4                 |
| MKL13Z32VMP4 | TBD                   | 32         | 4         | 64        | MAPBGA  | 54                 | 54/4                        | 20/4                 |
| MKL13Z64VMP4 | TBD                   | 64         | 8         | 64        | MAPBGA  | 54                 | 54/4                        | 20/4                 |
| MKL13Z32VLK4 | MKL13Z32/VLK4         | 32         | 4         | 80        | LQFP    | 70                 | 70/4                        | 20/4                 |
| MKL13Z64VLK4 | MKL13Z64/VLK4         | 64         | 8         | 80        | LQFP    | 70                 | 70/4                        | 20/4                 |

1. INT: interrupt pin numbers; HD: high drive pin numbers

### NOTE

The 32 QFN, 48 QFN, and 64 MAPBGA packages supporting MKLx3ZxxVFT4, MKLx3ZxxVFM4, and MKLx3ZxxVMP4 part numbers for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit [freescale.com/KPYW](http://freescale.com/KPYW) for more details.

### Related Resources

| Type           | Description  | Resource                         |
|----------------|--|----------------------------------|
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | <a href="#">Solution Advisor</a> |
| Product Brief  | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.   | KL1xPB <sup>1</sup>              |

Table continues on the next page...

### Related Resources (continued)

| Type             | Description  | Resource   |
|------------------|--|--|
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KL13P80M48SF3RM <sup>1</sup>   |
| Data Sheet       | The Data Sheet includes electrical characteristics and signal connections.                                       | This document.   |
| Chip Errata      | The chip mask set Errata provides additional or corrective information for a particular device mask set.         | KINETIS_L_0N01P <sup>1</sup>   |
| Package drawing  | Package dimensions are provided in package drawings.   | <ul style="list-style-type: none"> <li>• 64-LQFP: 98ASS23234W<sup>1</sup></li> <li>• 64 MAPBGA:<br/>98ASA00420D<sup>1</sup></li> <li>• 48 QFN: 98ASA00616D<sup>1</sup></li> <li>• 80 LQFP: 98ASS23174W<sup>1</sup></li> <li>• 32 QFN: 98ASA00615D<sup>1</sup></li> </ul> |

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

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# 1 Ratings

## 1.1 Thermal handling ratings

**Table 1. Thermal handling ratings**

| Symbol           | Description                   | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T <sub>STG</sub> | Storage temperature           | -55  | 150  | °C   | 1     |
| T <sub>SDR</sub> | Solder temperature, lead-free | —    | 260  | °C   | 2     |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

**Table 2. Moisture handling ratings**

| Symbol | Description                | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL    | Moisture sensitivity level | —    | 3    | —    | 1     |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

**Table 3. ESD handling ratings**

| Symbol           | Description   | Min.  | Max.  | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V <sub>HBM</sub> | Electrostatic discharge voltage, human body model     | -2000 | +2000 | V    | 1     |
| V <sub>CDM</sub> | Electrostatic discharge voltage, charged-device model | -500  | +500  | V    | 2     |
| I <sub>LAT</sub> | Latch-up current at ambient temperature of 105 °C     | -100  | +100  | mA   | 3     |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

| Symbol    | Description   | Min.           | Max.           | Unit |
|-----------|---|----------------|----------------|------|
| $V_{DD}$  | Digital supply voltage  | -0.3           | 3.8            | V    |
| $I_{DD}$  | Digital supply current  | —              | 120            | mA   |
| $V_{IO}$  | IO pin input voltage  | -0.3           | $V_{DD} + 0.3$ | V    |
| $I_D$     | Instantaneous maximum current single pin limit (applies to all port pins) | -25            | 25             | mA   |
| $V_{DDA}$ | Analog supply voltage   | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V    |

## 2 General

### 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

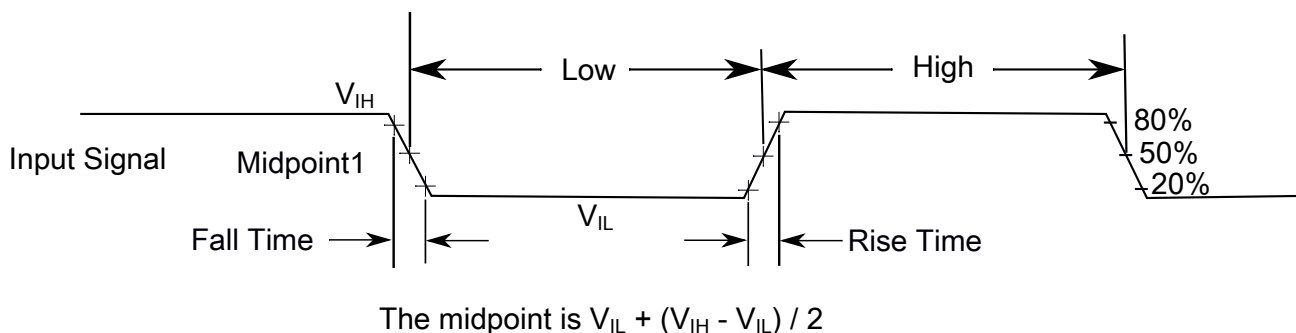


Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30$  pF loads
- Slew rate disabled
- Normal drive strength

### 2.2 Nonswitching electrical specifications

## 2.2.1 Voltage and current operating requirements

**Table 5. Voltage and current operating requirements**

| Symbol             | Description  | Min.                 | Max.                 | Unit | Notes |
|--------------------|--|----------------------|----------------------|------|-------|
| $V_{DD}$           | Supply voltage   | 1.71                 | 3.6                  | V    |       |
| $V_{DDA}$          | Analog supply voltage  | 1.71                 | 3.6                  | V    |       |
| $V_{DD} - V_{DDA}$ | $V_{DD}$ -to- $V_{DDA}$ differential voltage   | -0.1                 | 0.1                  | V    |       |
| $V_{SS} - V_{SSA}$ | $V_{SS}$ -to- $V_{SSA}$ differential voltage   | -0.1                 | 0.1                  | V    |       |
| $V_{IH}$           | Input high voltage<br><ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li>• <math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>     | $0.7 \times V_{DD}$  | —                    | V    |       |
|                    |  | $0.75 \times V_{DD}$ | —                    | V    |       |
| $V_{IL}$           | Input low voltage<br><ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li>• <math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>      | —                    | $0.35 \times V_{DD}$ | V    |       |
|                    |  | —                    | $0.3 \times V_{DD}$  | V    |       |
| $V_{HYS}$          | Input hysteresis   | $0.06 \times V_{DD}$ | —                    | V    |       |
| $I_{ICIO}$         | IO pin negative DC injection current — single pin<br><ul style="list-style-type: none"> <li>• <math>V_{IN} &lt; V_{SS}-0.3\text{V}</math></li> </ul>   | -3                   | —                    | mA   | 1     |
| $I_{ICcont}$       | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins<br><ul style="list-style-type: none"> <li>• Negative current injection</li> </ul> | -25                  | —                    | mA   |       |
| $V_{ODPU}$         | Open drain pullup voltage level  | $V_{DD}$             | $V_{DD}$             | V    | 2     |
| $V_{SRAM}$         | $V_{DD}$ voltage required to retain SRAM   | 1.2                  | —                    | V    |       |

- All I/O pins are internally clamped to  $V_{SS}$  through a ESD protection diode. There is no diode connection to  $V_{DD}$ . If  $V_{IN}$  greater than  $V_{IO\_MIN}$  ( $= V_{SS}-0.3\text{ V}$ ) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R = (V_{IO\_MIN} - V_{IN})/|I_{ICIO}|$ .
- Open drain outputs must be pulled to  $V_{DD}$ .

## 2.2.2 LVD and POR operating requirements

**Table 6.  $V_{DD}$  supply LVD and POR operating requirements**

| Symbol     | Description   | Min. | Typ. | Max. | Unit | Notes |
|------------|---|------|------|------|------|-------|
| $V_{POR}$  | Falling $V_{DD}$ POR detect voltage                           | 0.8  | 1.1  | 1.5  | V    | —     |
| $V_{LVDH}$ | Falling low-voltage detect threshold — high range (LVDV = 01) | 2.48 | 2.56 | 2.64 | V    | —     |
|            | Low-voltage warning thresholds — high range                   |      |      |      |      | 1     |

Table continues on the next page...

**Table 6. V<sub>DD</sub> supply LVD and POR operating requirements (continued)**

| Symbol             | Description   | Min. | Typ. | Max. | Unit | Notes |
|--------------------|---|------|------|------|------|-------|
| V <sub>LVW1H</sub> | <ul style="list-style-type: none"> <li>Level 1 falling (LVWV = 00)</li> </ul>   | 2.62 | 2.70 | 2.78 | V    |       |
| V <sub>LVW2H</sub> | <ul style="list-style-type: none"> <li>Level 2 falling (LVWV = 01)</li> </ul>   | 2.72 | 2.80 | 2.88 | V    |       |
| V <sub>LVW3H</sub> | <ul style="list-style-type: none"> <li>Level 3 falling (LVWV = 10)</li> </ul>   | 2.82 | 2.90 | 2.98 | V    |       |
| V <sub>LVW4H</sub> | <ul style="list-style-type: none"> <li>Level 4 falling (LVWV = 11)</li> </ul>   | 2.92 | 3.00 | 3.08 | V    |       |
| V <sub>HYSH</sub>  | Low-voltage inhibit reset/recover hysteresis — high range   | —    | ±60  | —    | mV   | —     |
| V <sub>LVDL</sub>  | Falling low-voltage detect threshold — low range (LVDV=00)  | 1.54 | 1.60 | 1.66 | V    | —     |
| V <sub>LVW1L</sub> | Low-voltage warning thresholds — low range<br><ul style="list-style-type: none"> <li>Level 1 falling (LVWV = 00)</li> </ul> | 1.74 | 1.80 | 1.86 | V    | 1     |
| V <sub>LVW2L</sub> | <ul style="list-style-type: none"> <li>Level 2 falling (LVWV = 01)</li> </ul>   | 1.84 | 1.90 | 1.96 | V    |       |
| V <sub>LVW3L</sub> | <ul style="list-style-type: none"> <li>Level 3 falling (LVWV = 10)</li> </ul>   | 1.94 | 2.00 | 2.06 | V    |       |
| V <sub>LVW4L</sub> | <ul style="list-style-type: none"> <li>Level 4 falling (LVWV = 11)</li> </ul>   | 2.04 | 2.10 | 2.16 | V    |       |
| V <sub>HYSL</sub>  | Low-voltage inhibit reset/recover hysteresis — low range  | —    | ±40  | —    | mV   | —     |
| V <sub>BG</sub>    | Bandgap voltage reference   | 0.97 | 1.00 | 1.03 | V    | —     |
| t <sub>LPO</sub>   | Internal low power oscillator period — factory trimmed  | 900  | 1000 | 1100 | µs   | —     |

1. Rising thresholds are falling threshold + hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

**Table 7. Voltage and current operating behaviors**

| Symbol           | Description   | Min.   | Max.       | Unit   | Notes |
|------------------|---|--|------------|--------|-------|
| V <sub>OH</sub>  | Output high voltage — normal drive pad<br><ul style="list-style-type: none"> <li>2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OH</sub> = -5 mA</li> <li>1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OH</sub> = -1.5 mA</li> </ul> | V <sub>DD</sub> - 0.5<br>V <sub>DD</sub> - 0.5 | —<br>—     | V<br>V | 1     |
| V <sub>OH</sub>  | Output high voltage — high drive pad<br><ul style="list-style-type: none"> <li>2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OH</sub> = -18 mA</li> <li>1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OH</sub> = -6 mA</li> </ul>    | V <sub>DD</sub> - 0.5<br>V <sub>DD</sub> - 0.5 | —<br>—     | V<br>V | 1     |
| I <sub>OHT</sub> | Output high current total for all ports   | —  | 100        | mA     |       |
| V <sub>OL</sub>  | Output low voltage — normal drive pad<br><ul style="list-style-type: none"> <li>2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OL</sub> = 5 mA</li> <li>1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OL</sub> = 1.5 mA</li> </ul>    | —<br>—   | 0.5<br>0.5 | V<br>V | 1     |
| V <sub>OL</sub>  | Output low voltage — high drive pad   |  |            |        | 1     |

Table continues on the next page...



**Table 7. Voltage and current operating behaviors (continued)**

| Symbol    | Description  | Min. | Max.  | Unit          | Notes |
|-----------|--|------|-------|---------------|-------|
|           | <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 18\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 6\text{ mA}</math></li> </ul> | —    | 0.5   | V             |       |
| $I_{OLT}$ | Output low current total for all ports   | —    | 100   | mA            |       |
| $I_{IN}$  | Input leakage current (per pin) for full temperature range   | —    | 1     | $\mu\text{A}$ | 2     |
| $I_{IN}$  | Input leakage current (per pin) at 25 °C   | —    | 0.025 | $\mu\text{A}$ | 2     |
| $I_{IN}$  | Input leakage current (total all pins) for full temperature range  | —    | 80    | $\mu\text{A}$ | 2     |
| $I_{OZ}$  | Hi-Z (off-state) leakage current (per pin)   | —    | 1     | $\mu\text{A}$ |       |
| $R_{PU}$  | Internal pullup resistors  | 20   | 50    | k $\Omega$    | 3     |

1. PTB0, PTB1, PTC3, and PTD7 I/O have both high drive and normal drive capability selected by the associated PORTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at  $V_{DD} = 3.6\text{ V}$
3. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{SS}$

## 2.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$  and  $VLLSx \rightarrow \text{RUN}$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

**Table 8. Power mode transition operating behaviors**

| Symbol    | Description   | Min. | Typ. | Max. | Unit          | Notes |
|-----------|---|------|------|------|---------------|-------|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | —    | —    | 300  | $\mu\text{s}$ | 1     |
|           | • $VLLS0 \rightarrow \text{RUN}$  | —    | 152  | 166  | $\mu\text{s}$ |       |
|           | • $VLLS1 \rightarrow \text{RUN}$  | —    | 152  | 166  | $\mu\text{s}$ |       |
|           | • $VLLS3 \rightarrow \text{RUN}$  | —    | 93   | 104  | $\mu\text{s}$ |       |
|           | • $LLS \rightarrow \text{RUN}$  | —    | 7.5  | 8    | $\mu\text{s}$ |       |

*Table continues on the next page...*

**Table 8. Power mode transition operating behaviors (continued)**

| Symbol | Description  | Min. | Typ. | Max. | Unit | Notes |
|--------|--|------|------|------|------|-------|
|        | <ul style="list-style-type: none"> <li>VLPS → RUN</li> </ul> | —    | 7.5  | 8    | μs   |       |
|        | <ul style="list-style-type: none"> <li>STOP → RUN</li> </ul> | —    | 7.5  | 8    | μs   |       |

1. Normal boot (FTFA\_FOPT[LPBOOT]=11)

## 2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

### NOTE

The while (1) test is executed with flash cache enabled.

**Table 9. Power consumption operating behaviors**

| Symbol                | Description   | Min.   | Typ.         | Max.         | Unit | Notes |
|-----------------------|---|--------|--------------|--------------|------|-------|
| I <sub>DDA</sub>      | Analog supply current   | —      | —            | See note     | mA   | 1     |
| I <sub>DD_RUNCO</sub> | Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>                    | —<br>— | 4.74<br>4.9  | 4.93<br>5.10 | mA   | 2     |
| I <sub>DD_RUNCO</sub> | Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>               | —<br>— | 3.27<br>3.42 | 3.43<br>3.59 | mA   |       |
| I <sub>DD_RUN</sub>   | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>  | —<br>— | 5.63<br>5.79 | 5.86<br>6.02 | mA   | 2     |
| I <sub>DD_RUN</sub>   | Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul> | —<br>— | 3.47<br>3.63 | 3.61<br>3.78 | mA   | 2,    |

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

| Symbol                 | Description  | Min. | Typ. | Max.   | Unit | Notes |
|------------------------|--|------|------|--------|------|-------|
| I <sub>DD_RUN</sub>    | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>        | —    | 2.37 | 2.56   | mA   | 2     |
| I <sub>DD_RUN</sub>    | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>        | —    | 6.91 | 7.19   | mA   | 2     |
| I <sub>DD_RUN</sub>    | Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul> | —    | 4.14 | 4.31   | mA   |       |
| I <sub>DD_RUN</sub>    | Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul> | —    | 2.7  | 2.92   | mA   |       |
| I <sub>DD_RUN</sub>    | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>  | —    | 1.99 | 2.15   | mA   |       |
| I <sub>DD_RUN</sub>    | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>  | —    | 5.39 | 5.61   | mA   |       |
| I <sub>DD_VLPRCO</sub> | Very Low Power Run Core Mark in Flash in Compute Operation mode: Core@4MHz, Flash @1MHz, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>  | —    | 739  | 827.68 | μA   |       |
| I <sub>DD_VLPRCO</sub> | Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                            | —    | 339  | 406.8  | μA   |       |
| I <sub>DD_VLPRCO</sub> | Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                          | —    | 152  | 197.6  | μA   |       |
| I <sub>DD_VLPR</sub>   | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral  |      |      |        |      |       |

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

| Symbol         | Description   | Min. | Typ. | Max.    | Unit          | Notes |
|----------------|---|------|------|---------|---------------|-------|
|                | clock disable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul>  | —    | 119  | 178.5   | $\mu\text{A}$ |       |
| $I_{DD\_VLPR}$ | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                    | —    | 41   | 89.39   | $\mu\text{A}$ |       |
| $I_{DD\_VLPR}$ | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                          | —    | 277  | 360.1   | $\mu\text{A}$ |       |
| $I_{DD\_VLPR}$ | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                           | —    | 343  | 425.32  | $\mu\text{A}$ |       |
| $I_{DD\_VLPR}$ | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                        | —    | 375  | 450     | $\mu\text{A}$ |       |
| $I_{DD\_VLPR}$ | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                            | —    | 441  | 529.2   | $\mu\text{A}$ |       |
| $I_{DD\_VLPR}$ | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                      | —    | 45   | 103.5   | $\mu\text{A}$ |       |
| $I_{DD\_WAIT}$ | Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul> | —    | 2.14 | 2.50    | mA            |       |
| $I_{DD\_WAIT}$ | Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul> | —    | 1.41 | 1.62    | mA            |       |
| $I_{DD\_VLPW}$ | Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$<br><ul style="list-style-type: none"> <li>at 25 °C</li> </ul>                                       | —    | 193  | 239.023 | $\mu\text{A}$ |       |

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

| Symbol                 | Description   | Min. | Typ.                                  | Max.                                   | Unit | Notes |
|------------------------|---|------|---------------------------------------|--|------|-------|
| I <sub>DD_VLPW</sub>   | Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>      | —    | 78                                    | 124.8                                  | μA   |       |
| I <sub>DD_VLPW</sub>   | Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>  | —    | 39                                    | 78                                     | μA   |       |
| I <sub>DD_PSTOP2</sub> | Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>  | —    | 1.72                                  | 2.06                                   | mA   |       |
| I <sub>DD_PSTOP2</sub> | Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>  | —    | 1.1                                   | 1.32                                   | mA   |       |
| I <sub>DD_STOP</sub>   | Stop mode current at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>  | —    | 161<br>171.9<br>206.8<br>255.9        | 178.2<br>181.17<br>229.72<br>302.01    | μA   |       |
| I <sub>DD_VLPS</sub>   | Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>   | —    | 2.20<br>4.57<br>18.02<br>39.60        | 3.80<br>8.03<br>31.98<br>65.80         | μA   |       |
| I <sub>DD_VLPS</sub>   | Very-low-power stop mode current at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>   | —    | 2.13<br>4.42<br>17.53<br>38.55        | 3.80<br>7.94<br>31.58<br>65.18         | μA   |       |
| I <sub>DD_LLS</sub>    | Low-leakage stop mode current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul> | —    | 1.63<br>2.42<br>4.22<br>7.16<br>15.34 | 2.25<br>3.55<br>7.08<br>10.22<br>22.69 | μA   |       |
| I <sub>DD_LLS</sub>    | Low-leakage stop mode current with RTC current, at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> </ul>   | —    | 2.3                                   | 2.99                                   | μA   |       |

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

| Symbol                | Description  | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|------|------|------|------|-------|
|                       | <ul style="list-style-type: none"> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>  | —    | 3.12 | 4.50 |      |       |
| I <sub>DD_LLS</sub>   | Low-leakage stop mode current with RTC current, at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>               | —    | 2.03 | 2.55 | μA   | 3     |
| I <sub>DD_VLLS3</sub> | Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul> | —    | 1.16 | 1.65 | μA   |       |
| I <sub>DD_VLLS3</sub> | Very-low-leakage stop mode 3 current with RTC current, at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>        | —    | 1.83 | 2.35 | μA   | 3     |
| I <sub>DD_VLLS3</sub> | Very-low-leakage stop mode 3 current with RTC current, at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>        | —    | 1.58 | 1.98 | μA   | 3     |
| I <sub>DD_VLLS1</sub> | Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> </ul>                                       | —    | 0.62 | 1.06 |      |       |
|                       |  | —    | 0.99 | 1.43 | μA   |       |
|                       |  | —    | 1.88 | 2.65 |      |       |
|                       |  | —    | 3.41 | 4.53 |      |       |

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

| Symbol                | Description   | Min. | Typ. | Max.  | Unit | Notes |
|-----------------------|---|------|------|-------|------|-------|
|                       | <ul style="list-style-type: none"> <li>at 85°C</li> <li>at 105 °C</li> </ul>  | —    | 7.89 | 9.99  |      |       |
| I <sub>DD_VLLS1</sub> | Very-low-leakage stop mode 1 current RTC enabled at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50°C</li> <li>at 70°C</li> <li>at 85°C</li> <li>at 105 °C</li> </ul>  | —    | 1.31 | 1.52  | μA   | 3     |
|                       |   | —    | 1.7  | 2.04  |      |       |
|                       |   | —    | 2.6  | 3.20  |      |       |
|                       |   | —    | 4.14 | 4.69  |      |       |
|                       |   | —    | 8.51 | 10.46 |      |       |
| I <sub>DD_VLLS1</sub> | Very-low-leakage stop mode 1 current RTC enabled at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50°C</li> <li>at 70°C</li> <li>at 85°C</li> <li>at 105 °C</li> </ul>  | —    | 1.06 | 1.35  | μA   | 3     |
|                       |   | —    | 1.39 | 1.73  |      |       |
|                       |   | —    | 2.18 | 2.83  |      |       |
|                       |   | —    | 3.54 | 4.60  |      |       |
|                       |   | —    | 7.43 | 9.97  |      |       |
| I <sub>DD_VLLS0</sub> | Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul> | —    | 278  | 385   | nA   |       |
|                       |   | —    | 578  | 1013  |      |       |
|                       |   | —    | 1530 | 2015  |      |       |
|                       |   | —    | 3070 | 3617  |      |       |
|                       |   | —    | 7550 | 9900  |      |       |
| I <sub>DD_VLLS0</sub> | Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>   | —    | 95   | 218   | nA   |       |
|                       |   | —    | 412  | 653   |      |       |
|                       |   | —    | 1350 | 1683  |      |       |
|                       |   | —    | 2900 | 3428  |      |       |
|                       |   | —    | 7380 | 9785  |      |       |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG\_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.20 with optimization level high, optimized for balanced.
3. RTC uses external 32 kHz crystal as clock source, and the current includes ERCLK32K power consumption.

**Table 10. Low power mode peripheral adders — typical value**

| Symbol                     | Description   | Temperature (°C) |     |     |     |     |     | Unit |
|----------------------------|---|------------------|-----|-----|-----|-----|-----|------|
|                            |   | -40              | 25  | 50  | 70  | 85  | 105 |      |
| I <sub>IRC8MHz</sub>       | 8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.   | 85               | 87  | 88  | 88  | 89  | 90  | μA   |
| I <sub>IRC2MHz</sub>       | 2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.   | 28               | 28  | 28  | 28  | 28  | 28  | μA   |
| I <sub>EREFSTEN4MHz</sub>  | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.  | 206              | 224 | 230 | 238 | 245 | 253 | μA   |
| I <sub>EREFSTEN32KHz</sub> | External 32 kHz crystal clock adder by means of setting the OSC0_CR[EREFSTEN and EREFSTEN] bits to 1 and SIM_SOPT1[OSC32KSEL] to 01. Measured by entering all modes with the crystal enabled. <ul style="list-style-type: none"> <li>• VLLS1</li> <li>• VLLS3</li> <li>• LLS</li> <li>• VLPS</li> <li>• STOP</li> </ul> | 440              | 490 | 540 | 560 | 570 | 580 | nA   |
|                            |   | 440              | 490 | 540 | 560 | 570 | 580 |      |
|                            |   | 490              | 490 | 540 | 560 | 570 | 680 |      |
|                            |   | 510              | 560 | 560 | 560 | 610 | 680 |      |
|                            |   | 510              | 560 | 560 | 560 | 610 | 680 |      |
| I <sub>LPTMR</sub>         | LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.   | 30               | 30  | 30  | 85  | 100 | 200 | nA   |
| I <sub>CMP</sub>           | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.   | 16               | 16  | 16  | 16  | 16  | 16  | μA   |
| I <sub>RTC</sub>           | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.  | 582              | 627 | 638 | 662 | 682 | 760 | nA   |
| I <sub>UART</sub>          | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate.   |                  |     |     |     |     |     |      |

Table continues on the next page...



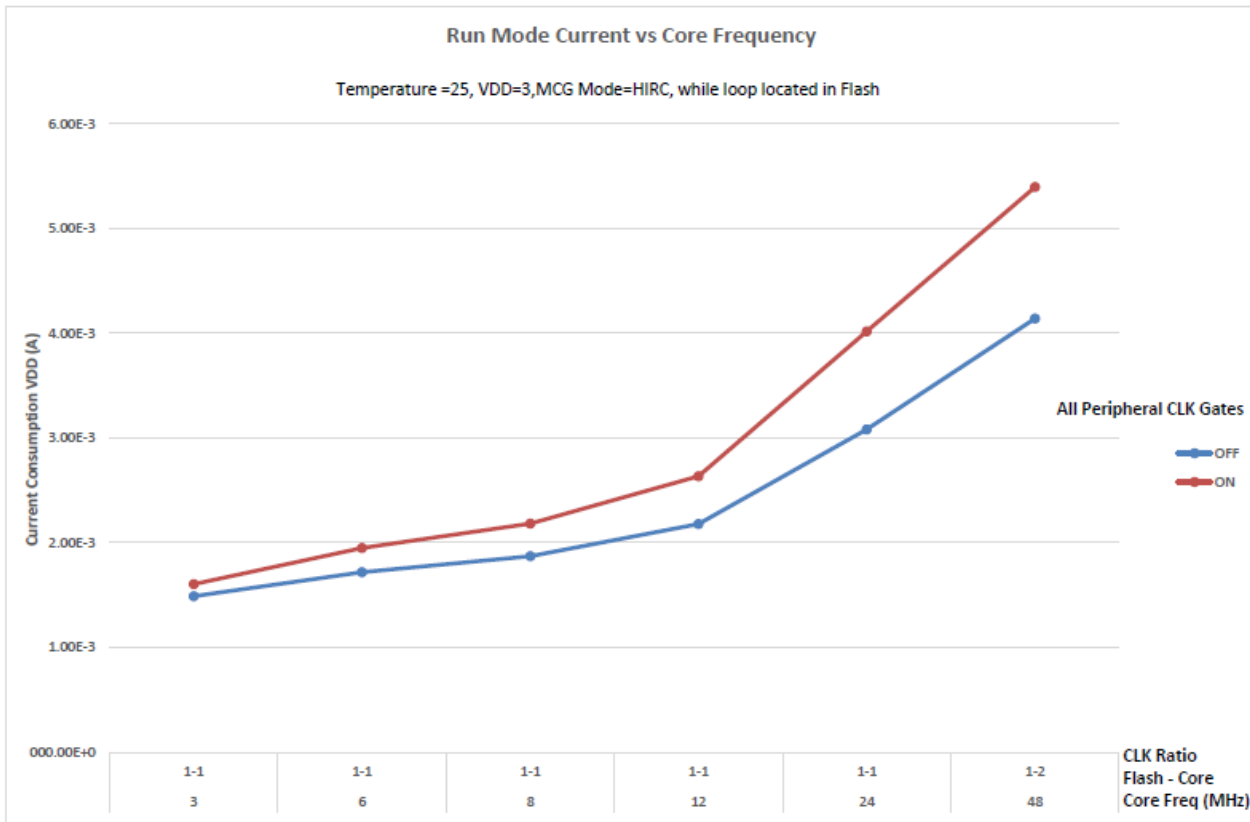
**Table 10. Low power mode peripheral adders — typical value (continued)**

| Symbol           | Description   | Temperature (°C) |           |           |           |           |           | Unit |
|------------------|---|------------------|-----------|-----------|-----------|-----------|-----------|------|
|                  |   | -40              | 25        | 50        | 70        | 85        | 105       |      |
|                  | Includes selected clock source power consumption. <ul style="list-style-type: none"> <li>• IRC8M (8 MHz internal reference clock)</li> <li>• IRC2M (2 MHz internal reference clock)</li> </ul>  | 105<br>34        | 110<br>34 | 110<br>34 | 111<br>34 | 112<br>34 | 114<br>34 | μA   |
| I <sub>TPM</sub> | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. <ul style="list-style-type: none"> <li>• IRC8M (8 MHz internal reference clock)</li> <li>• IRC2M (2 MHz internal reference clock)</li> </ul> | 130<br>40        | 130<br>40 | 130<br>40 | 130<br>40 | 130<br>40 | 130<br>40 | μA   |
| I <sub>BG</sub>  | Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.  | 45               | 45        | 45        | 45        | 45        | 45        | μA   |
| I <sub>ADC</sub> | ADC peripheral adder combining the measured values at V <sub>DD</sub> and V <sub>DDA</sub> by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.  | 320              | 320       | 320       | 320       | 320       | 320       | μA   |

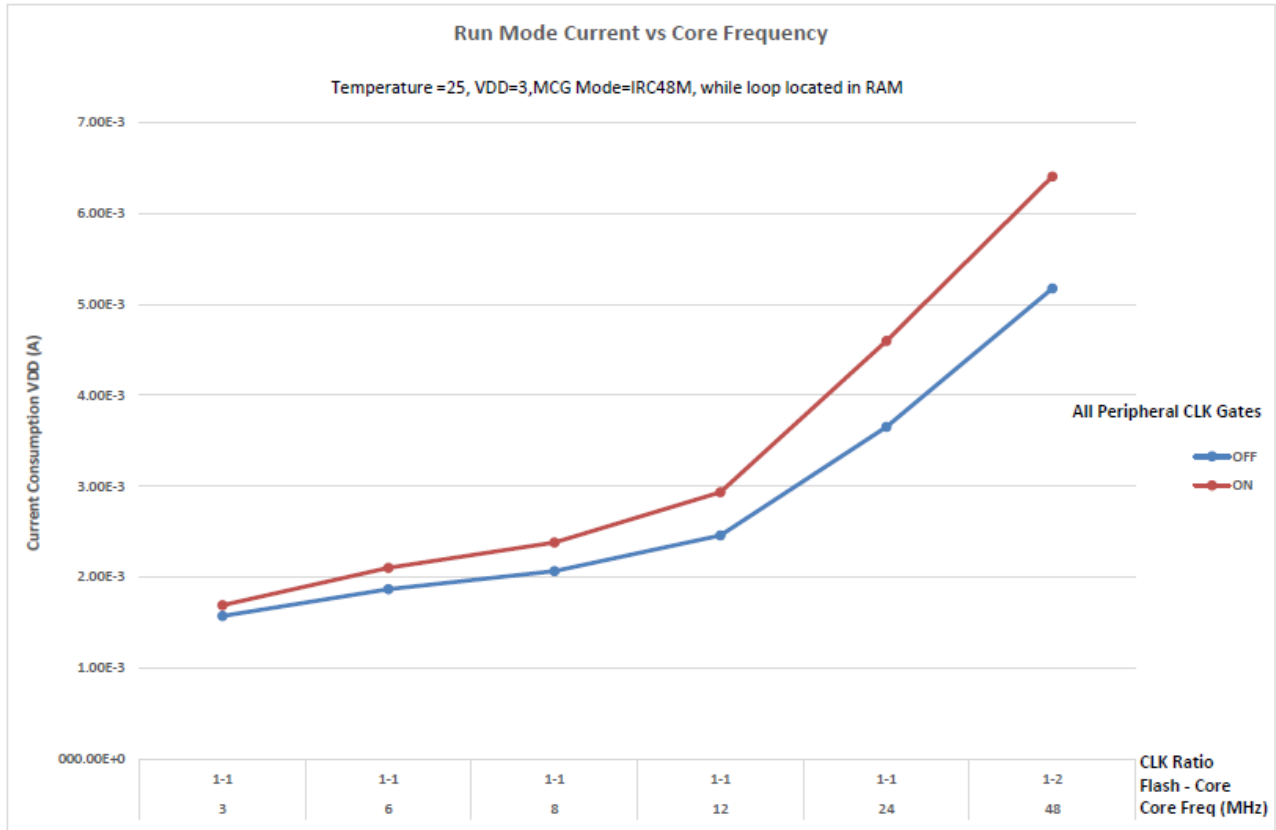
### 2.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



**Figure 2. Run mode supply current vs. core frequency**



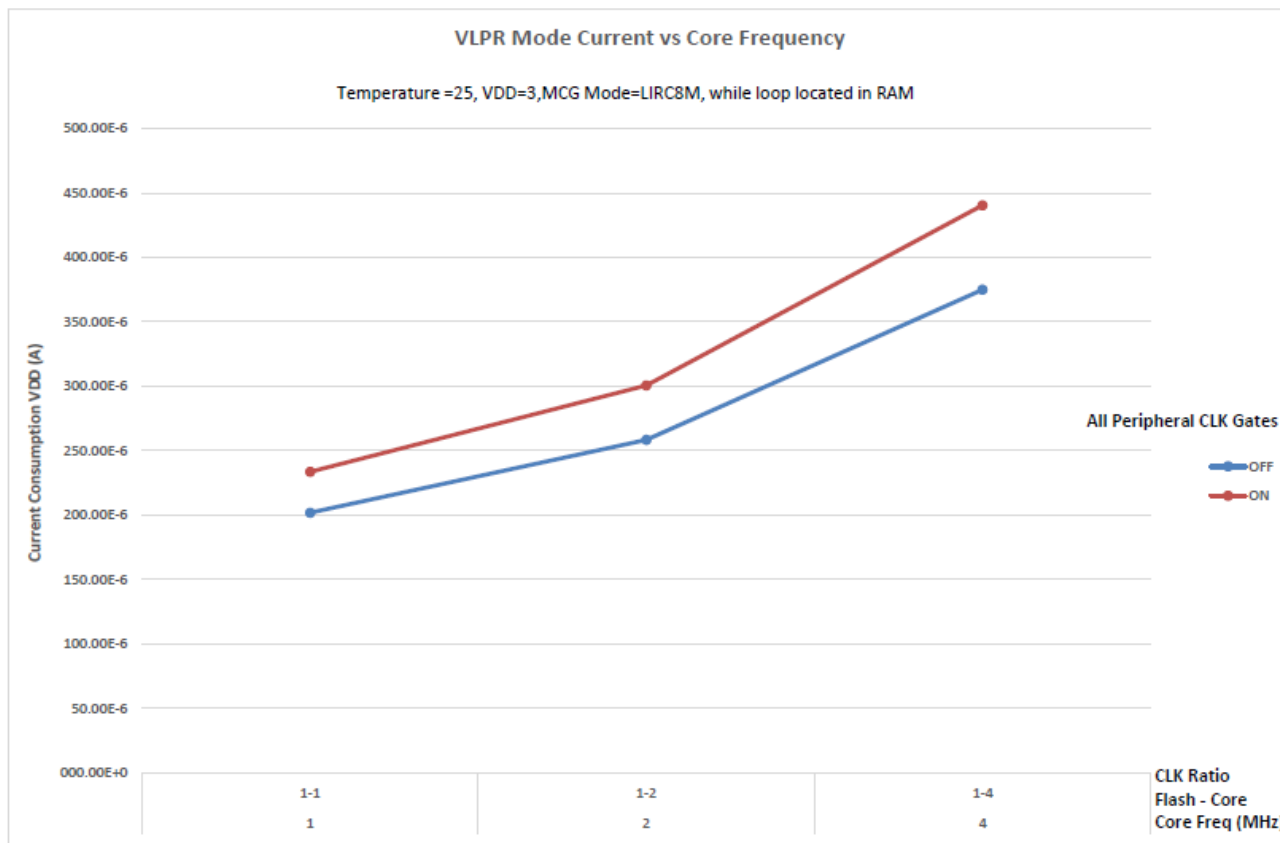


Figure 3. VLPR mode current vs. core frequency

### 2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following Freescale applications notes, available on [freescale.com](http://freescale.com) for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications

- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems
- KL-QRUG (Kinetis L-series Quick Reference).

## 2.2.7 Capacitance attributes

Table 11. Capacitance attributes

| Symbol          | Description       | Min. | Max. | Unit |
|-----------------|-------------------|------|------|------|
| C <sub>IN</sub> | Input capacitance | —    | 7    | pF   |

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

Table 12. Device clock specifications

| Symbol                           | Description   | Min. | Max. | Unit |
|----------------------------------|---|------|------|------|
| Normal run mode                  |   |      |      |      |
| f <sub>SYS</sub>                 | System and core clock   | —    | 48   | MHz  |
| f <sub>BUS</sub>                 | Bus clock   | —    | 24   | MHz  |
| f <sub>FLASH</sub>               | Flash clock   | —    | 24   | MHz  |
| f <sub>LPTMR</sub>               | LPTMR clock   | —    | 24   | MHz  |
| VLPR and VLPS modes <sup>1</sup> |   |      |      |      |
| f <sub>SYS</sub>                 | System and core clock   | —    | 4    | MHz  |
| f <sub>BUS</sub>                 | Bus clock   | —    | 1    | MHz  |
| f <sub>FLASH</sub>               | Flash clock   | —    | 1    | MHz  |
| f <sub>LPTMR</sub>               | LPTMR clock <sup>2</sup>  | —    | 24   | MHz  |
| f <sub>LPTMR_ERCLK</sub>         | LPTMR external reference clock  | —    | 16   | MHz  |
| f <sub>osc_hi_2</sub>            | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | —    | 16   | MHz  |
| f <sub>TPM</sub>                 | TPM asynchronous clock  | —    | 8    | MHz  |
| f <sub>LPUART0/1</sub>           | LPUART0/1 asynchronous clock  | —    | 8    | MHz  |

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

## 2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

**Table 13. General switching specifications**

| Description  | Min. | Max. | Unit             | Notes |
|--|------|------|------------------|-------|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5  | —    | Bus clock cycles | 1     |
| External RESET and NMI pin interrupt pulse width — Asynchronous path               | 100  | —    | ns               | 2     |
| GPIO pin interrupt pulse width — Asynchronous path                                 | 16   | —    | ns               | 2     |
| Port rise and fall time  | —    | 36   | ns               | 3     |

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

## 2.4 Thermal specifications

### 2.4.1 Thermal operating requirements

**Table 14. Thermal operating requirements**

| Symbol         | Description              | Min. | Max. | Unit | Notes |
|----------------|--------------------------|------|------|------|-------|
| T <sub>J</sub> | Die junction temperature | −40  | 125  | °C   |       |
| T <sub>A</sub> | Ambient temperature      | −40  | 105  | °C   | 1     |

1. Maximum T<sub>A</sub> can be exceeded only if the user ensures that T<sub>J</sub> does not exceed the maximum. The simplest method to determine T<sub>J</sub> is:  $T_J = T_A + \theta_{JA} \times \text{chip power dissipation}$ .

### 2.4.2 Thermal attributes

#### NOTE

The 48 QFN, 32 QFN, and 64 MAPBGA packages for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit [freescale.com/KPYW](http://freescale.com/KPYW) for more details.

**Table 15. Thermal attributes**

| Board type        | Symbol           | Description   | 64 LQFP | 80 LQFP | Unit | Notes |
|-------------------|------------------|---|---------|---------|------|-------|
| Single-layer (1S) | $R_{\theta JA}$  | Thermal resistance, junction to ambient (natural convection)                                    | 71      | 58      | °C/W | 1, 2  |
| Four-layer (2s2p) | $R_{\theta JA}$  | Thermal resistance, junction to ambient (natural convection)                                    | 53      | 43      | °C/W | 1, 2  |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed)                                | 60      | 47      | °C/W | 1, 3  |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed)                                | 46      | 37      | °C/W | 1, 3, |
| —                 | $R_{\theta JB}$  | Thermal resistance, junction to board   | 35      | 26      | °C/W | 4     |
| —                 | $R_{\theta JC}$  | Thermal resistance, junction to case  | 21      | 15      | °C/W | 5     |
| —                 | $\Psi_{JT}$      | Thermal characterization parameter, junction to package top outside center (natural convection) | 5       | 3       | °C/W | 6     |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 3 Peripheral operating requirements and behaviors

### 3.1 Core modules

#### 3.1.1 SWD electricals

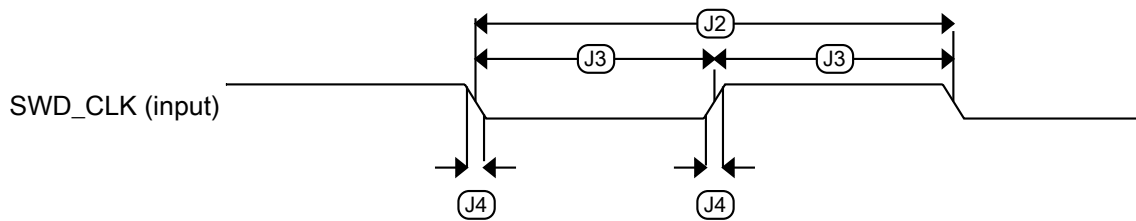
**Table 16. SWD full voltage range electricals**

| Symbol | Description                    | Min. | Max. | Unit |
|--------|--------------------------------|------|------|------|
|        | Operating voltage              | 1.71 | 3.6  | V    |
| J1     | SWD_CLK frequency of operation |      |      |      |

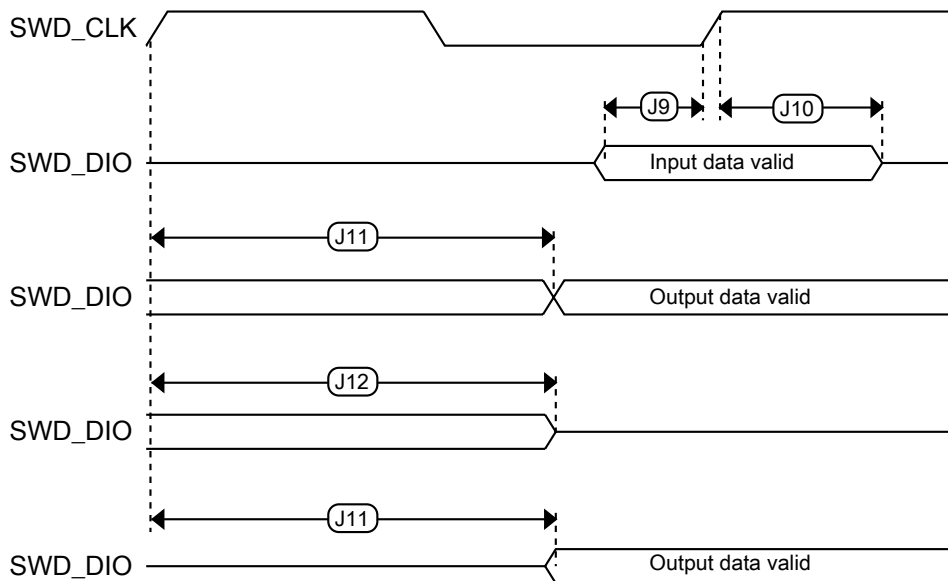
*Table continues on the next page...*

**Table 16. SWD full voltage range electricals (continued)**

| Symbol | Description                                      | Min. | Max. | Unit |
|--------|--|------|------|------|
|        | • Serial wire debug                              | 0    | 25   | MHz  |
| J2     | SWD_CLK cycle period                             | 1/J1 | —    | ns   |
| J3     | SWD_CLK clock pulse width<br>• Serial wire debug | 20   | —    | ns   |
| J4     | SWD_CLK rise and fall times                      | —    | 3    | ns   |
| J9     | SWD_DIO input data setup time to SWD_CLK rise    | 10   | —    | ns   |
| J10    | SWD_DIO input data hold time after SWD_CLK rise  | 0    | —    | ns   |
| J11    | SWD_CLK high to SWD_DIO data valid               | —    | 32   | ns   |
| J12    | SWD_CLK high to SWD_DIO high-Z                   | 5    | —    | ns   |



**Figure 4. Serial wire clock input timing**



**Figure 5. Serial wire data timing**



## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG-Lite specifications

Table 17. IRC48M specifications

| Symbol                      | Description   | Min. | Typ.      | Max.      | Unit           | Notes |
|-----------------------------|---|------|-----------|-----------|----------------|-------|
| $I_{DD48M}$                 | Supply current  | —    | 400       | 500       | $\mu A$        |       |
| $f_{irc48m}$                | Internal reference frequency  | —    | 48        | —         | MHz            |       |
| $\Delta f_{irc48m\_ol\_lv}$ | Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature | —    | $\pm 0.5$ | $\pm 1.5$ | $\%f_{irc48m}$ |       |
| $\Delta f_{irc48m\_ol\_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature | —    | $\pm 0.5$ | $\pm 1.0$ | $\%f_{irc48m}$ |       |
| $J_{cyc\_irc48m}$           | Period Jitter (RMS)   | —    | 35        | 150       | ps             |       |
| $t_{irc48mst}$              | Startup time  | —    | 2         | 3         | $\mu s$        |       |

Table 18. IRC8M/2M specification

| Symbol           | Description                      | Min. | Typ. | Max.    | Unit        | Notes |
|------------------|----------------------------------|------|------|---------|-------------|-------|
| $I_{DD\_2M}$     | Supply current in 2 MHz mode     | —    | 14   | 17      | $\mu A$     | —     |
| $I_{DD\_8M}$     | Supply current in 8 MHz mode     | —    | 30   | 35      | $\mu A$     | —     |
| $f_{IRC\_2M}$    | Output frequency                 | —    | 2    | —       | MHz         | —     |
| $f_{IRC\_8M}$    | Output frequency                 | —    | 8    | —       | MHz         | —     |
| $f_{IRC\_T\_2M}$ | Output frequency range (trimmed) | —    | —    | $\pm 3$ | $\%f_{IRC}$ | —     |
| $f_{IRC\_T\_8M}$ | Output frequency range (trimmed) | —    | —    | $\pm 3$ | $\%f_{IRC}$ | —     |
| $T_{su\_2M}$     | Startup time                     | —    | —    | 12.5    | $\mu s$     | —     |
| $T_{su\_8M}$     | Startup time                     | —    | —    | 12.5    | $\mu s$     | —     |

### 3.3.2 Oscillator electrical specifications

### 3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

| Symbol      | Description   | Min. | Typ. | Max. | Unit       | Notes |
|-------------|---|------|------|------|------------|-------|
| $V_{DD}$    | Supply voltage  | 1.71 | —    | 3.6  | V          |       |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0)   |      |      |      |            | 1     |
|             | • 32 kHz  | —    | 500  | —    | nA         |       |
|             | • 4 MHz   | —    | 200  | —    | $\mu$ A    |       |
|             | • 8 MHz (RANGE=01)  | —    | 300  | —    | $\mu$ A    |       |
|             | • 16 MHz  | —    | 950  | —    | $\mu$ A    |       |
|             | • 24 MHz  | —    | 1.2  | —    | mA         |       |
| $I_{DDOSC}$ | Supply current — high gain mode (HGO=1)   |      |      |      |            | 1     |
|             | • 32 kHz  | —    | 25   | —    | $\mu$ A    |       |
|             | • 4 MHz   | —    | 400  | —    | $\mu$ A    |       |
|             | • 8 MHz (RANGE=01)  | —    | 500  | —    | $\mu$ A    |       |
|             | • 16 MHz  | —    | 2.5  | —    | mA         |       |
|             | • 24 MHz  | —    | 3    | —    | mA         |       |
| $C_x$       | EXTAL load capacitance  | —    | —    | —    |            | 2, 3  |
|             | XTAL load capacitance   | —    | —    | —    |            | 2, 3  |
| $R_F$       | Feedback resistor — low-frequency, low-power mode (HGO=0)                                       | —    | —    | —    | M $\Omega$ | 2, 4  |
|             | Feedback resistor — low-frequency, high-gain mode (HGO=1)                                       | —    | 10   | —    | M $\Omega$ |       |
|             | Feedback resistor — high-frequency, low-power mode (HGO=0)                                      | —    | —    | —    | M $\Omega$ |       |
|             | Feedback resistor — high-frequency, high-gain mode (HGO=1)                                      | —    | 1    | —    | M $\Omega$ |       |
| $R_S$       | Series resistor — low-frequency, low-power mode (HGO=0)   | —    | —    | —    | k $\Omega$ |       |
|             | Series resistor — low-frequency, high-gain mode (HGO=1)   | —    | 200  | —    | k $\Omega$ |       |
|             | Series resistor — high-frequency, low-power mode (HGO=0)  | —    | —    | —    | k $\Omega$ |       |
|             | Series resistor — high-frequency, high-gain mode (HGO=1)  | —    | 0    | —    | k $\Omega$ |       |
| $V_{pp}^5$  | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | —    | 0.6  | —    | V          |       |

Table continues on the next page...

**Table 19. Oscillator DC electrical specifications (continued)**

| Symbol | Description  | Min. | Typ.     | Max. | Unit | Notes |
|--------|--|------|----------|------|------|-------|
|        | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)  | —    | $V_{DD}$ | —    | V    |       |
|        | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | —    | 0.6      | —    | V    |       |
|        | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | —    | $V_{DD}$ | —    | V    |       |

1.  $V_{DD}=3.3$  V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3.  $C_x, C_y$  can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected,  $R_F$  is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 3.3.2.2 Oscillator frequency specifications

**Table 20. Oscillator frequency specifications**

| Symbol           | Description   | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|------|------|-------|
| $f_{osc\_lo}$    | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)               | 32   | —    | 40   | kHz  |       |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)  | 3    | —    | 8    | MHz  |       |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8    | —    | 32   | MHz  |       |
| $f_{ec\_extal}$  | Input clock frequency (external clock mode)   | —    | —    | 48   | MHz  |       |
| $t_{dc\_extal}$  | Input clock duty cycle (external clock mode)  | 40   | 50   | 60   | %    |       |
| $t_{cst}$        | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)                             | —    | 750  | —    | ms   | 1, 2  |
|                  | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)                             | —    | 250  | —    | ms   |       |
|                  | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)          | —    | 0.6  | —    | ms   |       |
|                  | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)          | —    | 1    | —    | ms   |       |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

## 3.4 Memories and memory interfaces

### 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 21. NVM program/erase timing specifications**

| Symbol                | Description                        | Min. | Typ. | Max. | Unit          | Notes |
|-----------------------|------------------------------------|------|------|------|---------------|-------|
| $t_{hvp\text{gm}4}$   | Longword Program high-voltage time | —    | 7.5  | 18   | $\mu\text{s}$ | —     |
| $t_{h\text{versscr}}$ | Sector Erase high-voltage time     | —    | 13   | 113  | ms            | 1     |
| $t_{h\text{versall}}$ | Erase All high-voltage time        | —    | 52   | 452  | ms            | 1     |

1. Maximum time based on expectations at cycling end-of-life.

#### 3.4.1.2 Flash timing specifications — commands

**Table 22. Flash command timing specifications**

| Symbol                       | Description                                   | Min. | Typ. | Max. | Unit          | Notes |
|------------------------------|---|------|------|------|---------------|-------|
| $t_{rd1\text{sec}1\text{k}}$ | Read 1s Section execution time (flash sector) | —    | —    | 60   | $\mu\text{s}$ | 1     |
| $t_{pgm\text{chk}}$          | Program Check execution time                  | —    | —    | 45   | $\mu\text{s}$ | 1     |
| $t_{rd\text{rsrc}}$          | Read Resource execution time                  | —    | —    | 30   | $\mu\text{s}$ | 1     |
| $t_{pgm4}$                   | Program Longword execution time               | —    | 65   | 145  | $\mu\text{s}$ | —     |
| $t_{er\text{sscr}}$          | Erase Flash Sector execution time             | —    | 14   | 114  | ms            | 2     |
| $t_{rd1\text{all}}$          | Read 1s All Blocks execution time             | —    | —    | 0.9  | ms            | 1     |
| $t_{rd\text{once}}$          | Read Once execution time                      | —    | —    | 25   | $\mu\text{s}$ | 1     |
| $t_{pgm\text{once}}$         | Program Once execution time                   | —    | 65   | —    | $\mu\text{s}$ | —     |
| $t_{er\text{sall}}$          | Erase All Blocks execution time               | —    | 70   | 575  | ms            | 2     |
| $t_{vt\text{ykey}}$          | Verify Backdoor Access Key execution time     | —    | —    | 30   | $\mu\text{s}$ | 1     |
| $t_{er\text{sallu}}$         | Erase All Blocks Unsecure execution time      | —    | 70   | 575  | ms            | 2     |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 3.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

| Symbol              | Description   | Min. | Typ. | Max. | Unit |
|---------------------|---|------|------|------|------|
| I <sub>DD_PGM</sub> | Average current adder during high voltage flash programming operation | —    | 2.5  | 6.0  | mA   |
| I <sub>DD_ERS</sub> | Average current adder during high voltage flash erase operation       | —    | 1.5  | 4.0  | mA   |

### 3.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

| Symbol                  | Description                            | Min. | Typ. <sup>1</sup> | Max. | Unit   | Notes |
|-------------------------|--|------|-------------------|------|--------|-------|
| Program Flash           |  |      |                   |      |        |       |
| t <sub>nvmretp10k</sub> | Data retention after up to 10 K cycles | 5    | 50                | —    | years  | —     |
| t <sub>nvmretp1k</sub>  | Data retention after up to 1 K cycles  | 20   | 100               | —    | years  | —     |
| n <sub>nvmcycp</sub>    | Cycling endurance                      | 10 K | 50 K              | —    | cycles | 2     |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at  $-40\text{ °C} \leq T_j \leq 125\text{ °C}$ .

## 3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 3.6 Analog

### 3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

### 3.6.1.1 16-bit ADC operating conditions

Table 25. 16-bit ADC operating conditions

| Symbol            | Description                         | Conditions  | Min.           | Typ. <sup>1</sup> | Max.                   | Unit | Notes |
|-------------------|-------------------------------------|---|----------------|-------------------|------------------------|------|-------|
| V <sub>DDA</sub>  | Supply voltage                      | Absolute  | 1.71           | —                 | 3.6                    | V    | —     |
| ΔV <sub>DDA</sub> | Supply voltage                      | Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> )  | -100           | 0                 | +100                   | mV   | 2     |
| ΔV <sub>SSA</sub> | Ground voltage                      | Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> )  | -100           | 0                 | +100                   | mV   | 2     |
| V <sub>ADIN</sub> | Input voltage                       | <ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>       | VREFL<br>VREFL | —<br>—            | 31/32 * VREFH<br>VREFH | V    | —     |
| C <sub>ADIN</sub> | Input capacitance                   | <ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-bit / 10-bit / 12-bit modes</li> </ul>      | —<br>—         | 8<br>4            | 10<br>5                | pF   | —     |
| R <sub>ADIN</sub> | Input series resistance             |   | —              | 2                 | 5                      | kΩ   | —     |
| R <sub>AS</sub>   | Analog source resistance (external) | 13-bit / 12-bit modes<br>f <sub>ADCK</sub> < 4 MHz  | —              | —                 | 5                      | kΩ   | 3     |
| f <sub>ADCK</sub> | ADC conversion clock frequency      | ≤ 13-bit mode   | 1.0            | —                 | 18.0                   | MHz  | 4     |
| f <sub>ADCK</sub> | ADC conversion clock frequency      | 16-bit mode   | 2.0            | —                 | 12.0                   | MHz  | 4     |
| C <sub>rate</sub> | ADC conversion rate                 | ≤ 13-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000         | —                 | 818.330                | Ksps | 5     |
| C <sub>rate</sub> | ADC conversion rate                 | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time    | 37.037         | —                 | 461.467                | Ksps | 5     |

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25 °C, f<sub>ADCK</sub> = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R<sub>AS</sub>/C<sub>AS</sub> time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

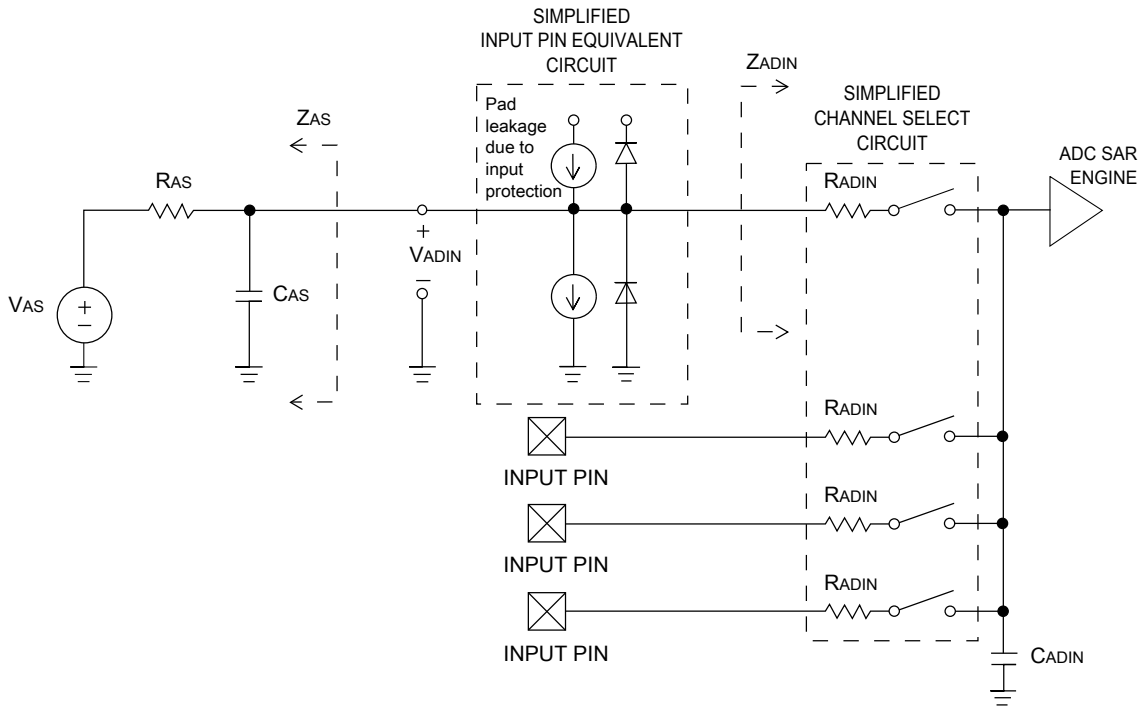


Figure 6. ADC input impedance equivalency diagram

### 3.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

| Symbol         | Description                   | Conditions <sup>1</sup>                       | Min.  | Typ. <sup>2</sup> | Max.                        | Unit             | Notes                     |
|----------------|-------------------------------|---|-------|-------------------|-----------------------------|------------------|---------------------------|
| $I_{DDA\_ADC}$ | Supply current                |   | 0.215 | —                 | 1.7                         | mA               | 3                         |
| $f_{ADACK}$    | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0                        | 1.2   | 2.4               | 3.9                         | MHz              | $t_{ADACK} = 1/f_{ADACK}$ |
|                |                               | • ADLPC = 1, ADHSC = 1                        | 2.4   | 4.0               | 6.1                         | MHz              |                           |
|                |                               | • ADLPC = 0, ADHSC = 0                        | 3.0   | 5.2               | 7.3                         | MHz              |                           |
|                |                               | • ADLPC = 0, ADHSC = 1                        | 4.4   | 6.2               | 9.5                         | MHz              |                           |
|                | Sample Time                   | See Reference Manual chapter for sample times |       |                   |                             |                  |                           |
| TUE            | Total unadjusted error        | • 12-bit modes<br>• <12-bit modes             | —     | ±2.5<br>±1.4      | ±6.8<br>±2.1                | LSB <sup>4</sup> | 5                         |
| DNL            | Differential non-linearity    | • 12-bit modes<br>• <12-bit modes             | —     | ±0.7<br>±0.2      | -1.1 to +1.9<br>-0.3 to 0.5 | LSB <sup>4</sup> | 5                         |
| INL            | Integral non-linearity        | • 12-bit modes                                | —     | ±0.9              | -2.7 to +1.9                | LSB <sup>4</sup> | 5                         |

Table continues on the next page...

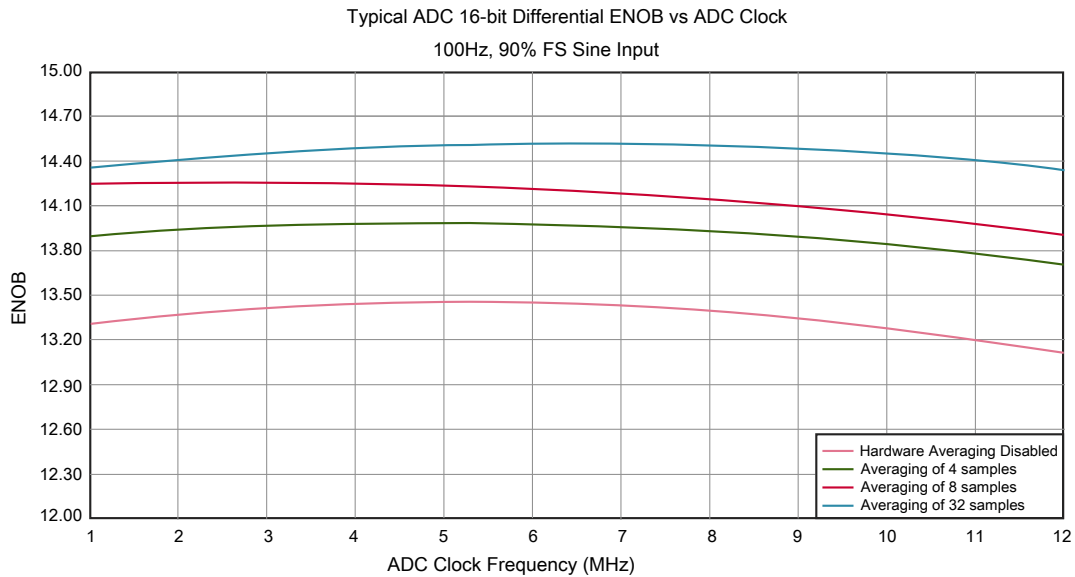
**Table 26. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

| Symbol  | Description                     | Conditions <sup>1</sup>  | Min.                   | Typ. <sup>2</sup> | Max.         | Unit             | Notes   |
|---|---------------------------------|--|------------------------|-------------------|--------------|------------------|---|
|   |                                 | <ul style="list-style-type: none"> <li>&lt;12-bit modes</li> </ul>                       | —                      | ±0.4              | -0.7 to +0.5 |                  |   |
| $E_{FS}$  | Full-scale error                | <ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul> | —                      | -4                | -5.4         | LSB <sup>4</sup> | $V_{ADIN} = V_{DDA}$ <sup>5</sup>   |
| $E_Q$   | Quantization error              | <ul style="list-style-type: none"> <li>16-bit modes</li> <li>≤13-bit modes</li> </ul>    | —                      | -1 to 0           | —            | LSB <sup>4</sup> |   |
| $ENOB$  | Effective number of bits        | 16-bit differential mode   |                        |                   |              |                  | 6   |
|   |                                 | <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>                               | 12.8                   | 14.5              | —            | bits             |   |
|   |                                 | <ul style="list-style-type: none"> <li>Avg = 4</li> </ul>                                | 11.9                   | 13.8              | —            | bits             |   |
|   |                                 | 16-bit single-ended mode   |                        |                   |              |                  |   |
| <ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul> | 12.2                            | 13.9   | —                      | bits              |              |                  |   |
|   |                                 |  | 11.4                   | 13.1              | —            | bits             |   |
| $SINAD$   | Signal-to-noise plus distortion | See ENOB   | 6.02 × ENOB + 1.76     |                   |              | dB               |   |
| $THD$   | Total harmonic distortion       | 16-bit differential mode   |                        |                   |              |                  | 7   |
|   |                                 | <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>                               | —                      | -94               | —            | dB               |   |
|   |                                 | 16-bit single-ended mode   |                        |                   |              |                  |   |
|   |                                 | <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>                               | —                      | -85               | —            | dB               |   |
| $SFDR$  | Spurious free dynamic range     | 16-bit differential mode   |                        |                   |              |                  | 7   |
|   |                                 | <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>                               | 82                     | 95                | —            | dB               |   |
|   |                                 | 16-bit single-ended mode   |                        |                   |              |                  |   |
|   |                                 | <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>                               | 78                     | 90                | —            | dB               |   |
| $E_{IL}$  | Input leakage error             |  | $I_{in} \times R_{AS}$ |                   |              | mV               | $I_{in}$ = leakage current (refer to the MCU's voltage and current operating ratings) |
|   | Temp sensor slope               | Across the full temperature range of the device  | 1.55                   | 1.62              | 1.69         | mV/°C            | 8   |
| $V_{TEMP25}$  | Temp sensor voltage             | 25 °C  | 706                    | 716               | 726          | mV               | 8   |

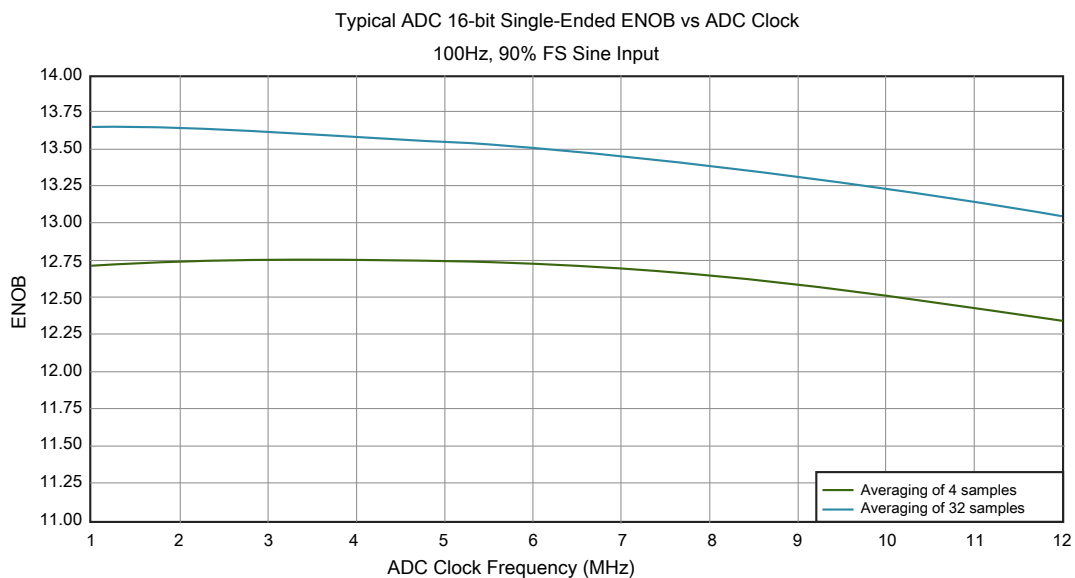
 1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$



2. Typical values assume  $V_{DDA} = 3.0\text{ V}$ ,  $\text{Temp} = 25\text{ }^{\circ}\text{C}$ ,  $f_{\text{ADCK}} = 2.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and `ADC_CFG1[ADLPC]` (low power). For lowest power operation, `ADC_CFG1[ADLPC]` must be set, the `ADC_CFG2[ADHSC]` bit must be clear with 1 MHz ADC conversion clock speed.
4.  $1\text{ LSB} = (V_{\text{REFH}} - V_{\text{REFL}})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (`AVGE = %1`, `AVGS = %11`)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz



**Figure 7. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**



**Figure 8. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

### 3.6.2 Voltage reference electrical specifications

**Table 27. VREF full-range operating requirements**

| Symbol           | Description             | Min.                                      | Max. | Unit | Notes |
|------------------|-------------------------|---|------|------|-------|
| V <sub>DDA</sub> | Supply voltage          |   | 3.6  | V    | —     |
| T <sub>A</sub>   | Temperature             | Operating temperature range of the device |      | °C   | —     |
| C <sub>L</sub>   | Output load capacitance | 100                                       |      | nF   | 1, 2  |

1. C<sub>L</sub> must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C<sub>L</sub> value over the operating temperature range of the device.

Table 28 is tested under the condition of setting VREF\_TRM[CHOPEN], VREF\_SC[REGEN] and VREF\_SC[ICOMPEN] bits to 1.

**Table 28. VREF full-range operating behaviors**

| Symbol                          | Description   | Min.   | Typ.  | Max.   | Unit | Notes |
|---------------------------------|---|--------|-------|--------|------|-------|
| V <sub>out</sub>                | Voltage reference output with factory trim at nominal V <sub>DDA</sub> and temperature=25C          | 1.1915 | 1.195 | 1.1977 | V    | 1     |
| V <sub>out</sub>                | Voltage reference output — factory trim   | 1.1584 | —     | 1.2376 | V    | 1     |
| V <sub>out</sub>                | Voltage reference output — user trim  | 1.193  | —     | 1.197  | V    | 1     |
| V <sub>step</sub>               | Voltage reference trim step   | —      | 0.5   | —      | mV   | 1     |
| V <sub>tdrift</sub>             | Temperature drift (V <sub>max</sub> -V <sub>min</sub> across the full temperature range: 0 to 70°C) | —      | 2     | 15     | mV   | 1     |
| I <sub>bg</sub>                 | Bandgap only current  | —      | —     | 80     | μA   | 1     |
| I <sub>lp</sub>                 | Low-power buffer current  | —      | —     | 360    | uA   | 1     |
| I <sub>hp</sub>                 | High-power buffer current   | —      | —     | 1      | mA   | 1     |
| ΔV <sub>LOAD</sub>              | Load regulation<br>• current = ± 1.0 mA   | —      | 200   | —      | μV   | 1, 2  |
| T <sub>stup</sub>               | Buffer startup time   | —      | —     | 100    | μs   | —     |
| T <sub>chop_osc_st<br/>up</sub> | Internal bandgap start-up delay with chop oscillator enabled  | —      | —     | 35     | ms   | —     |
| V <sub>vdrift</sub>             | Voltage drift (V <sub>max</sub> -V <sub>min</sub> across the full voltage range)                    | —      | 2     | —      | mV   | 1     |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 29. VREF limited-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| $T_A$  | Temperature | 0    | 50   | °C   | —     |

**Table 30. VREF limited-range operating behaviors**

| Symbol    | Description                                | Min.  | Max.  | Unit | Notes |
|-----------|--|-------|-------|------|-------|
| $V_{out}$ | Voltage reference output with factory trim | 1.173 | 1.225 | V    | —     |

### 3.6.3 CMP and 6-bit DAC electrical specifications

**Table 31. Comparator and 6-bit DAC electrical specifications**

| Symbol      | Description  | Min.           | Typ.                | Max.             | Unit                 |
|-------------|--|----------------|---------------------|------------------|----------------------|
| $V_{DD}$    | Supply voltage   | 1.71           | —                   | 3.6              | V                    |
| $I_{DDHS}$  | Supply current, High-speed mode (EN=1, PMODE=1)  | —              | —                   | 200              | μA                   |
| $I_{DDL S}$ | Supply current, low-speed mode (EN=1, PMODE=0)   | —              | —                   | 20               | μA                   |
| $V_{AIN}$   | Analog input voltage   | $V_{SS} - 0.3$ | —                   | $V_{DD}$         | V                    |
| $V_{AIO}$   | Analog input offset voltage  | —              | —                   | 20               | mV                   |
| $V_H$       | Analog comparator hysteresis <sup>1</sup> <ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 00</li> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul> | —              | 5<br>10<br>20<br>30 | —<br>—<br>—<br>— | mV<br>mV<br>mV<br>mV |
| $V_{CMPOH}$ | Output high  | $V_{DD} - 0.5$ | —                   | —                | V                    |
| $V_{CMPOI}$ | Output low   | —              | —                   | 0.5              | V                    |
| $t_{DHS}$   | Propagation delay, high-speed mode (EN=1, PMODE=1)   | 20             | 50                  | 200              | ns                   |
| $t_{DLS}$   | Propagation delay, low-speed mode (EN=1, PMODE=0)  | 80             | 250                 | 600              | ns                   |
|             | Analog comparator initialization delay <sup>2</sup>  | —              | —                   | 40               | μs                   |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled)  | —              | 7                   | —                | μA                   |
| INL         | 6-bit DAC integral non-linearity   | -0.5           | —                   | 0.5              | LSB <sup>3</sup>     |
| DNL         | 6-bit DAC differential non-linearity   | -0.3           | —                   | 0.3              | LSB                  |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6$  V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB =  $V_{reference}/64$

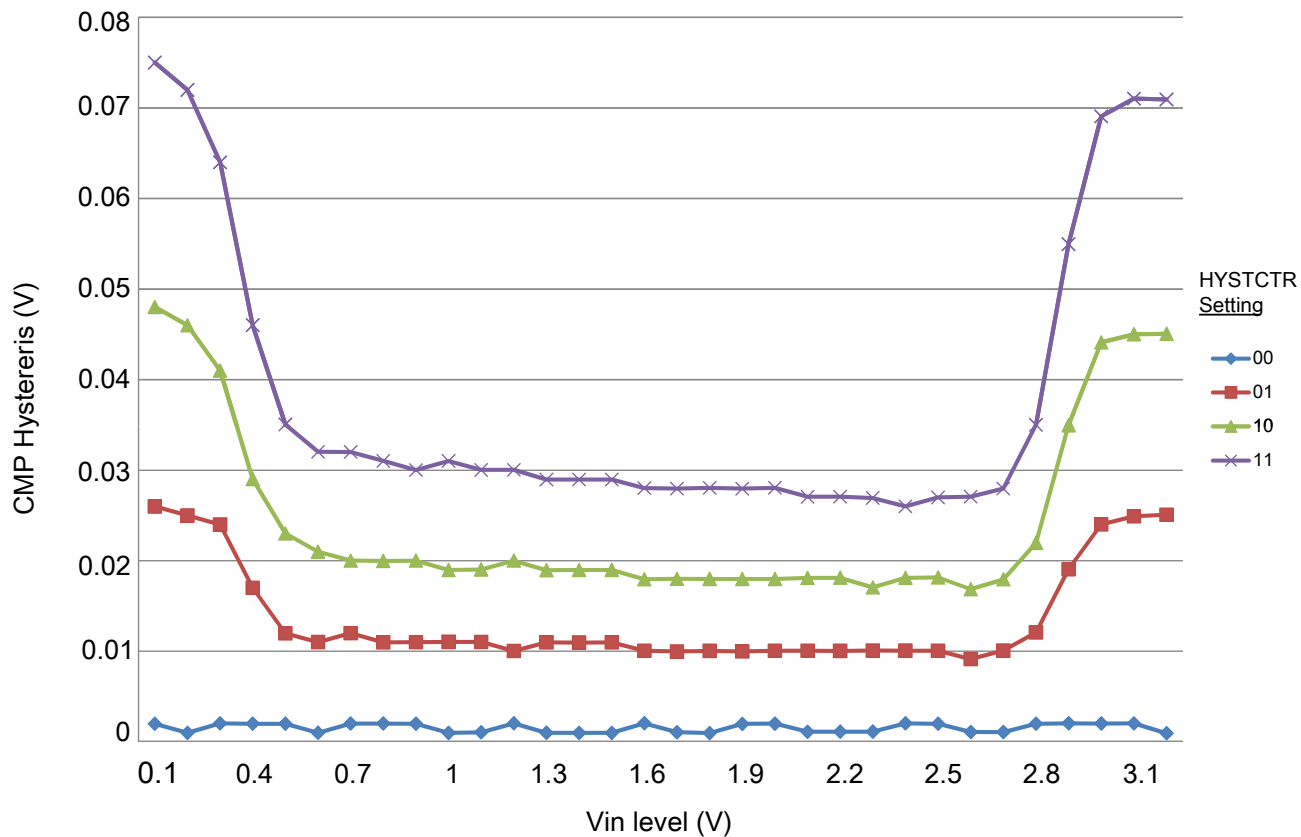


Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

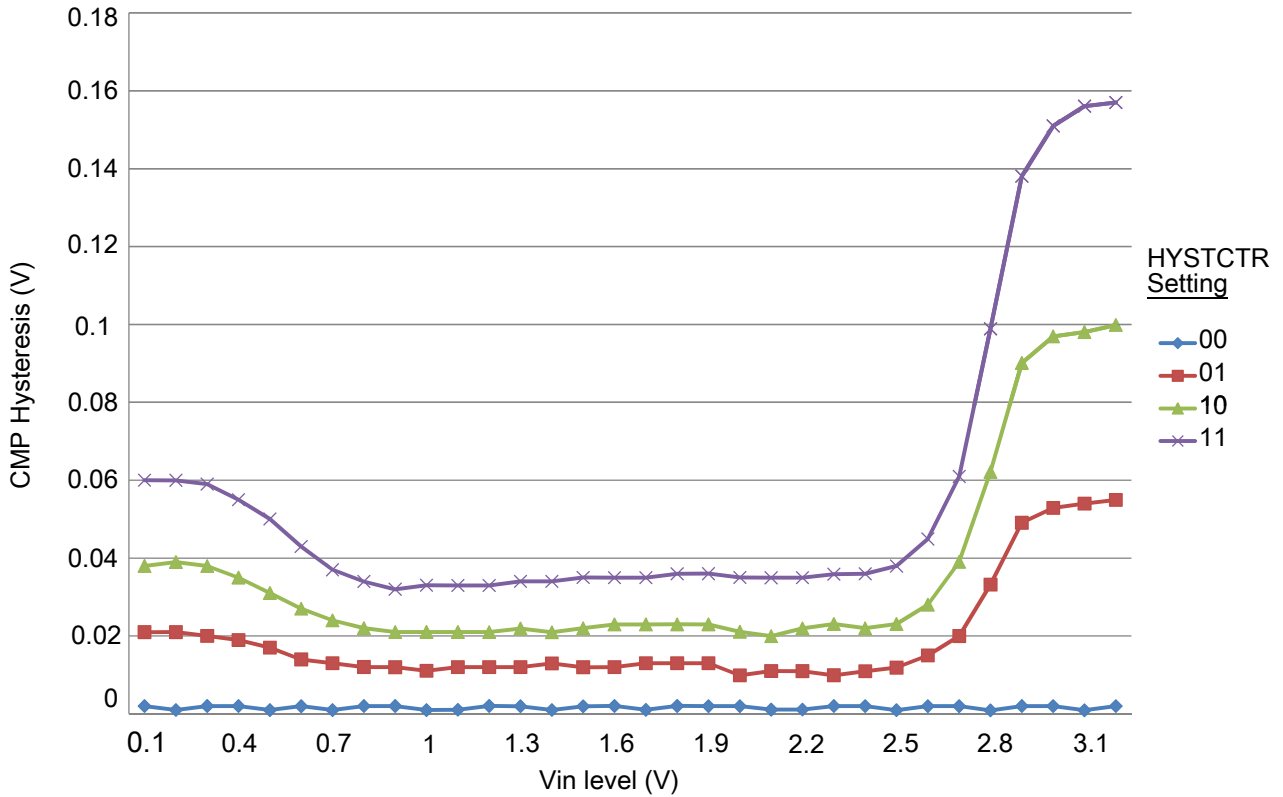


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

### 3.6.4 12-bit DAC electrical characteristics

#### 3.6.4.1 12-bit DAC operating requirements

Table 32. 12-bit DAC operating requirements

| Symbol            | Description             | Min. | Max. | Unit | Notes |
|-------------------|-------------------------|------|------|------|-------|
| V <sub>DDA</sub>  | Supply voltage          |      | 3.6  | V    |       |
| V <sub>DACR</sub> | Reference voltage       | 1.13 | 3.6  | V    | 1     |
| C <sub>L</sub>    | Output load capacitance | —    | 100  | pF   | 2     |
| I <sub>L</sub>    | Output load current     | —    | 1    | mA   |       |

1. The DAC reference can be selected to be V<sub>DDA</sub> or V<sub>REFH</sub>.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

### 3.6.4.2 12-bit DAC operating behaviors

**Table 33. 12-bit DAC operating behaviors**

| Symbol           | Description   | Min.             | Typ.        | Max.       | Unit                   | Notes |
|------------------|---|------------------|-------------|------------|------------------------|-------|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode   | —                | —           | 250        | $\mu\text{A}$          |       |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode  | —                | —           | 900        | $\mu\text{A}$          |       |
| $t_{DACLP}$      | Full-scale settling time (0x080 to 0xF7F) — low-power mode  | —                | 100         | 200        | $\mu\text{s}$          | 1     |
| $t_{DACHP}$      | Full-scale settling time (0x080 to 0xF7F) — high-power mode   | —                | 15          | 30         | $\mu\text{s}$          | 1     |
| $t_{CCDACLP}$    | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode  | —                | 0.7         | 1          | $\mu\text{s}$          | 1     |
| $V_{dacoutl}$    | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000   | —                | —           | 100        | mV                     |       |
| $V_{dacouth}$    | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF  | $V_{DACR} - 100$ | —           | $V_{DACR}$ | mV                     |       |
| INL              | Integral non-linearity error — high speed mode  | —                | —           | $\pm 8$    | LSB                    | 2     |
| DNL              | Differential non-linearity error — $V_{DACR} > 2\text{ V}$  | —                | —           | $\pm 1$    | LSB                    | 3     |
| DNL              | Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$  | —                | —           | $\pm 1$    | LSB                    | 4     |
| $V_{OFFSET}$     | Offset error  | —                | $\pm 0.4$   | $\pm 0.8$  | %FSR                   | 5     |
| $E_G$            | Gain error  | —                | $\pm 0.1$   | $\pm 0.6$  | %FSR                   | 5     |
| PSRR             | Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$   | 60               | —           | 90         | dB                     |       |
| $T_{CO}$         | Temperature coefficient offset voltage  | —                | 3.7         | —          | $\mu\text{V}/\text{C}$ | 6     |
| $T_{GE}$         | Temperature coefficient gain error  | —                | 0.000421    | —          | %FSR/C                 |       |
| $R_{op}$         | Output resistance (load = 3 k $\Omega$ )  | —                | —           | 250        | $\Omega$               |       |
| SR               | Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>• High power (SP<sub>HP</sub>)</li> <li>• Low power (SP<sub>LP</sub>)</li> </ul> | 1.2<br>0.05      | 1.7<br>0.12 | —<br>—     | V/ $\mu\text{s}$       |       |
| BW               | 3dB bandwidth <ul style="list-style-type: none"> <li>• High power (SP<sub>HP</sub>)</li> <li>• Low power (SP<sub>LP</sub>)</li> </ul>               | 550<br>40        | —<br>—      | —<br>—     | kHz                    |       |

1. Settling within  $\pm 1$  LSB
2. The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
3. The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
4. The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4\text{ V}$
5. Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
6.  $V_{DDA} = 3.0\text{ V}$ , reference select set for  $V_{DDA}$  (DACx\_CO:DACRFS = 1), high power mode (DACx\_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

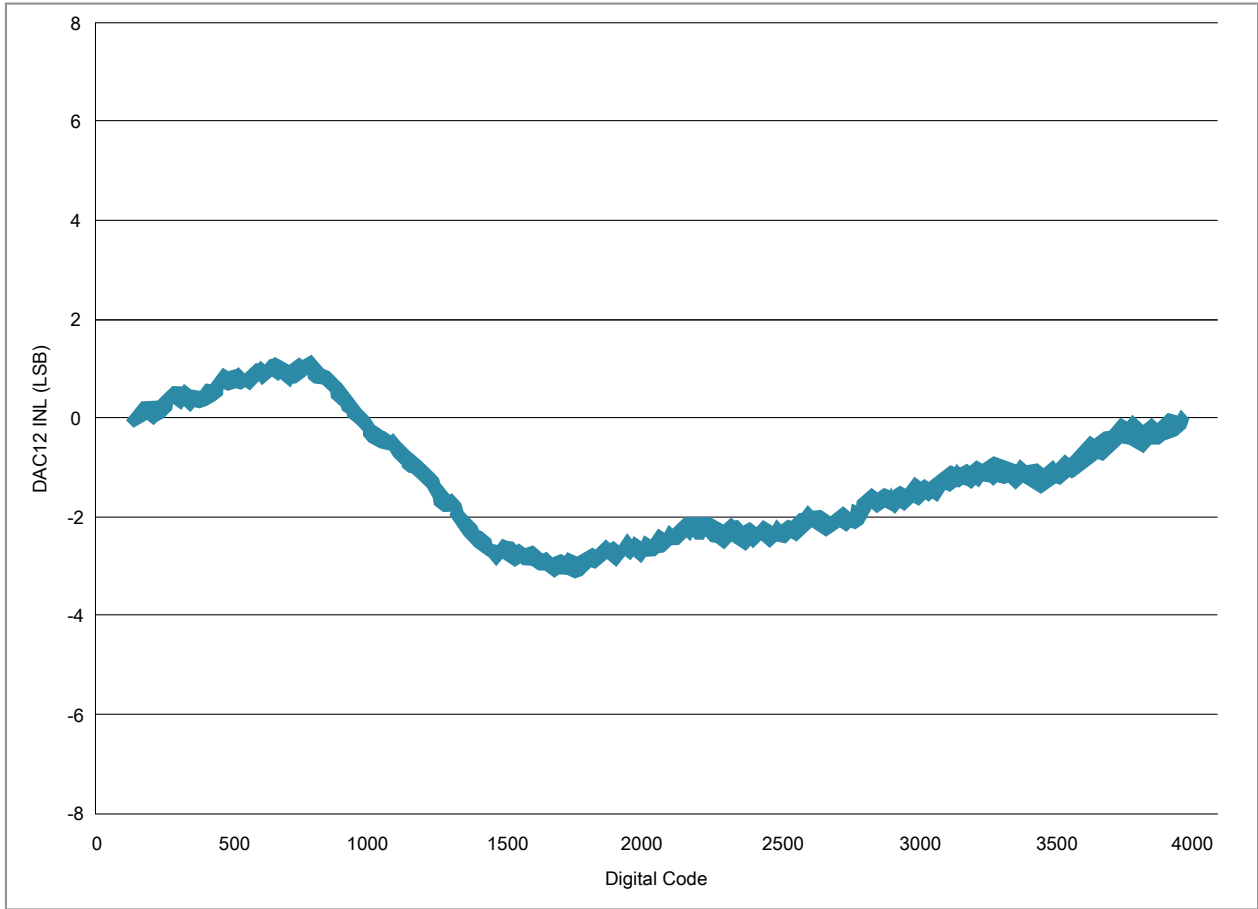


Figure 11. Typical INL error vs. digital code

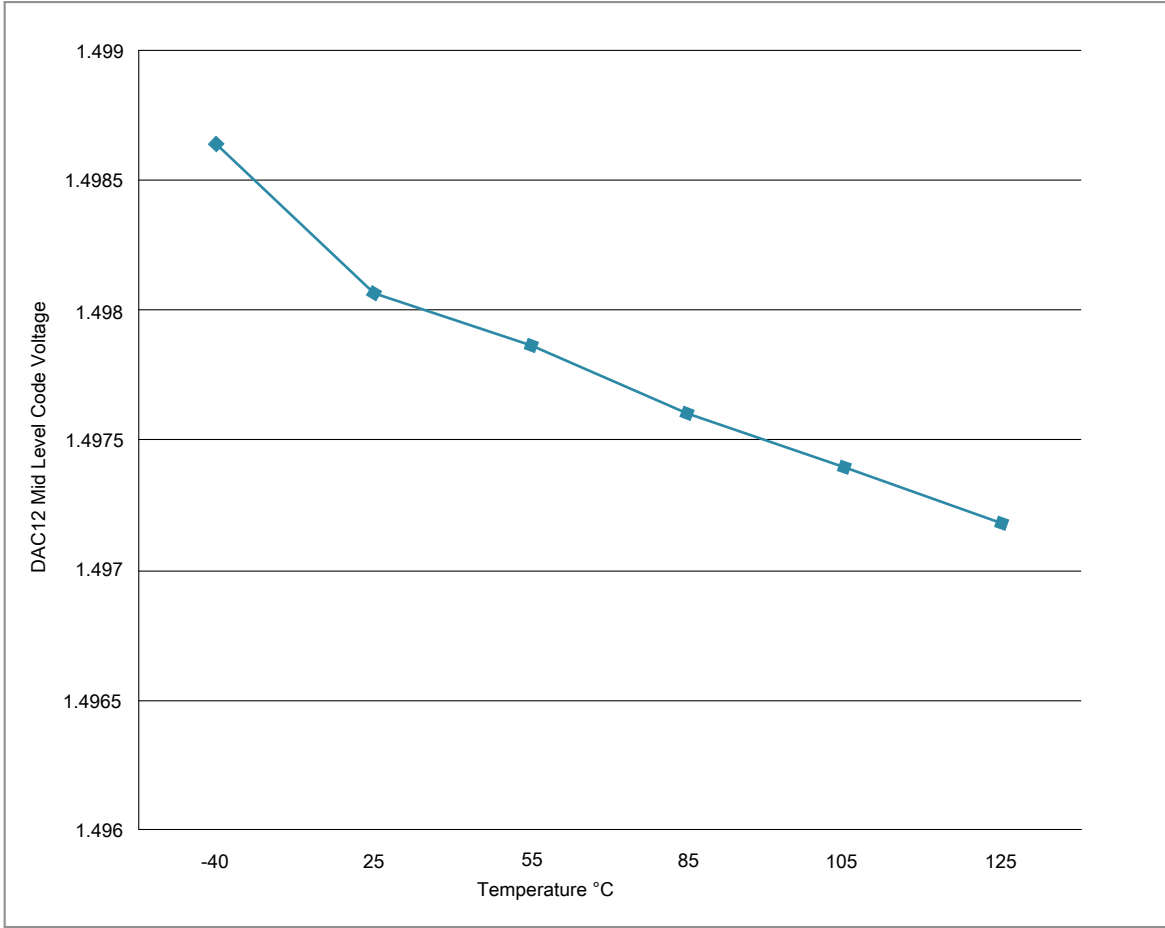


Figure 12. Offset at half scale vs. temperature

## 4 Timers

See [General switching specifications](#).

## 5 Communication interfaces



## 5.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 34. SPI master mode timing on slew rate disabled pads**

| Num. | Symbol       | Description                    | Min.                  | Max.                     | Unit        | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1    | $f_{op}$     | Frequency of operation         | $f_{periph}/2048$     | $f_{periph}/2$           | Hz          | 1    |
| 2    | $t_{SPSCK}$  | SPSCK period                   | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns          | 2    |
| 3    | $t_{Lead}$   | Enable lead time               | 1/2                   | —                        | $t_{SPSCK}$ | —    |
| 4    | $t_{Lag}$    | Enable lag time                | 1/2                   | —                        | $t_{SPSCK}$ | —    |
| 5    | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$     | $1024 \times t_{periph}$ | ns          | —    |
| 6    | $t_{SU}$     | Data setup time (inputs)       | 18                    | —                        | ns          | —    |
| 7    | $t_{HI}$     | Data hold time (inputs)        | 0                     | —                        | ns          | —    |
| 8    | $t_v$        | Data valid (after SPSCK edge)  | —                     | 15                       | ns          | —    |
| 9    | $t_{HO}$     | Data hold time (outputs)       | 0                     | —                        | ns          | —    |
| 10   | $t_{RI}$     | Rise time input                | —                     | $t_{periph} - 25$        | ns          | —    |
|      | $t_{FI}$     | Fall time input                |                       |                          |             |      |
| 11   | $t_{RO}$     | Rise time output               | —                     | 25                       | ns          | —    |
|      | $t_{FO}$     | Fall time output               |                       |                          |             |      |

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$

**Table 35. SPI master mode timing on slew rate enabled pads**

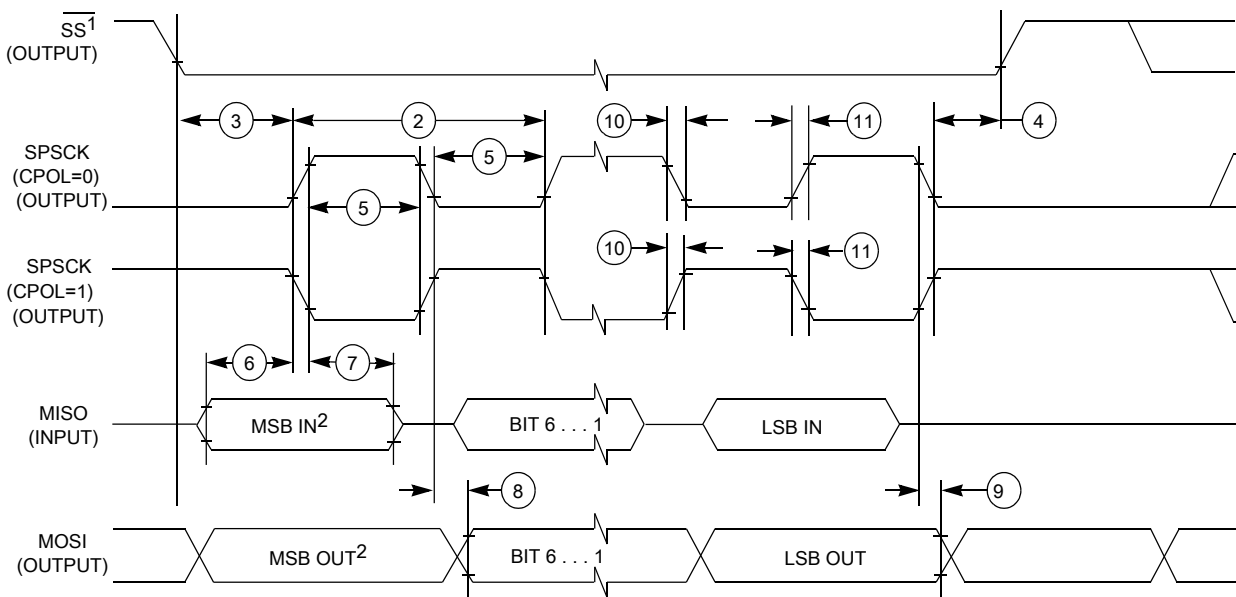
| Num. | Symbol       | Description                    | Min.                  | Max.                     | Unit        | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1    | $f_{op}$     | Frequency of operation         | $f_{periph}/2048$     | $f_{periph}/2$           | Hz          | 1    |
| 2    | $t_{SPSCK}$  | SPSCK period                   | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns          | 2    |
| 3    | $t_{Lead}$   | Enable lead time               | 1/2                   | —                        | $t_{SPSCK}$ | —    |
| 4    | $t_{Lag}$    | Enable lag time                | 1/2                   | —                        | $t_{SPSCK}$ | —    |
| 5    | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$     | $1024 \times t_{periph}$ | ns          | —    |
| 6    | $t_{SU}$     | Data setup time (inputs)       | 96                    | —                        | ns          | —    |
| 7    | $t_{HI}$     | Data hold time (inputs)        | 0                     | —                        | ns          | —    |

Table continues on the next page...

**Table 35. SPI master mode timing on slew rate enabled pads (continued)**

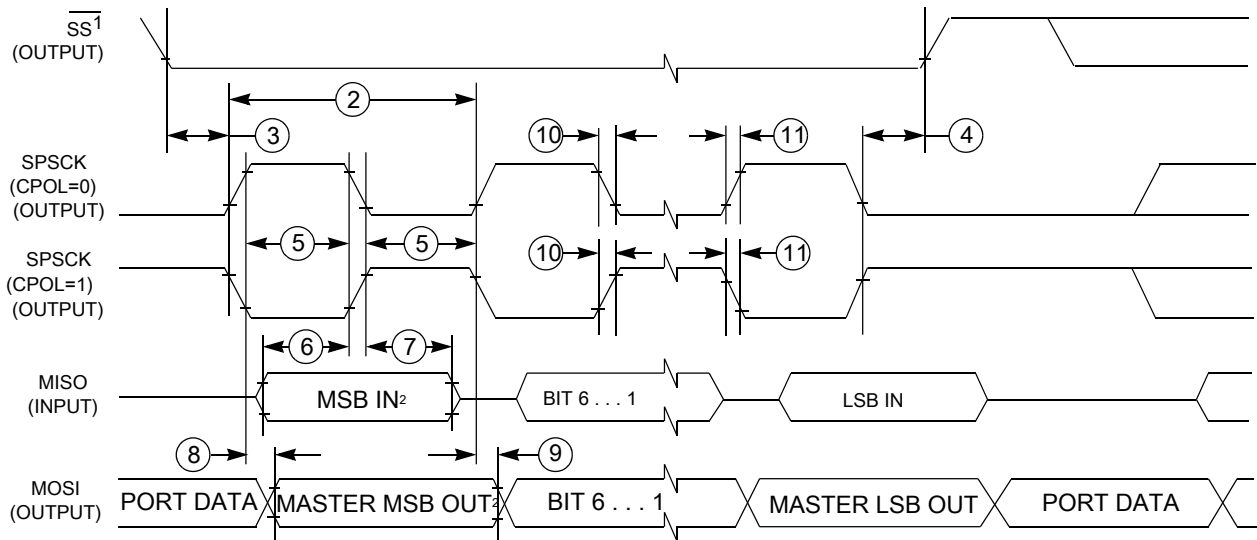
| Num. | Symbol   | Description                    | Min. | Max.              | Unit | Note |
|------|----------|--------------------------------|------|-------------------|------|------|
| 8    | $t_v$    | Data valid (after SPSCCK edge) | —    | 83                | ns   | —    |
| 9    | $t_{HO}$ | Data hold time (outputs)       | 0    | —                 | ns   | —    |
| 10   | $t_{RI}$ | Rise time input                | —    | $t_{periph} - 25$ | ns   | —    |
|      | $t_{FI}$ | Fall time input                |      |                   |      |      |
| 11   | $t_{RO}$ | Rise time output               | —    | 36                | ns   | —    |
|      | $t_{FO}$ | Fall time output               |      |                   |      |      |

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 13. SPI master mode timing (CPHA = 0)**



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA = 1)**

**Table 36. SPI slave mode timing on slew rate disabled pads**

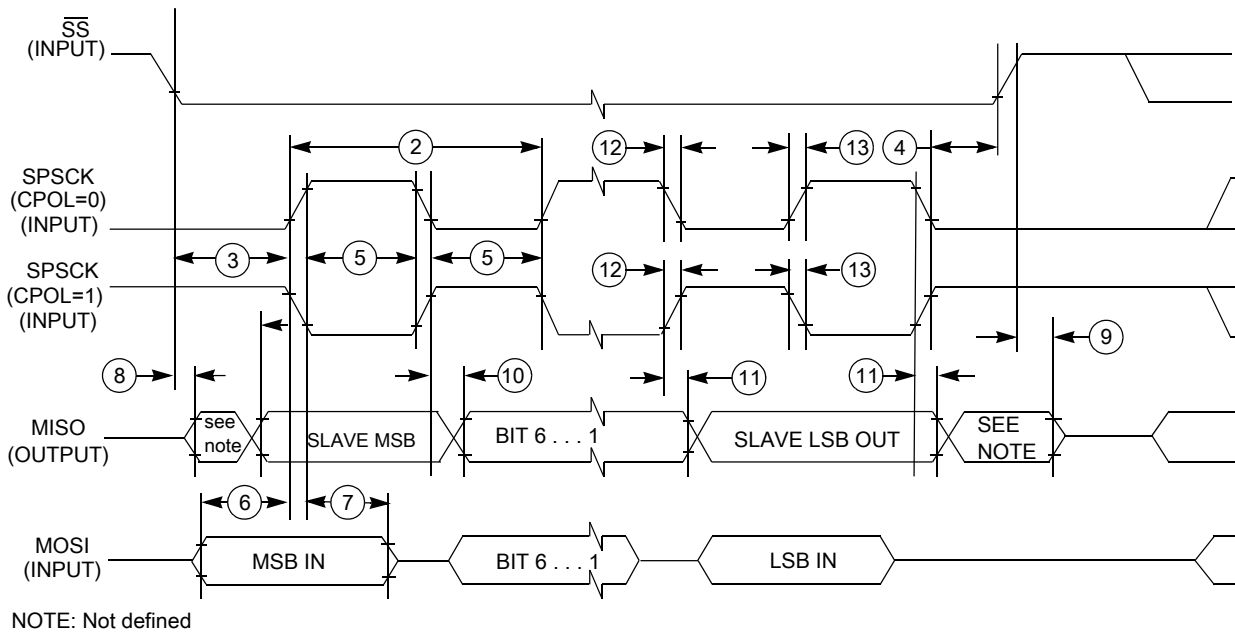
| Num. | Symbol        | Description                     | Min.                  | Max.              | Unit         | Note |
|------|---------------|---------------------------------|-----------------------|-------------------|--------------|------|
| 1    | $f_{op}$      | Frequency of operation          | 0                     | $f_{periph}/4$    | Hz           | 1    |
| 2    | $t_{SPSCCK}$  | SPSCCK period                   | $4 \times t_{periph}$ | —                 | ns           | 2    |
| 3    | $t_{Lead}$    | Enable lead time                | 1                     | —                 | $t_{periph}$ | —    |
| 4    | $t_{Lag}$     | Enable lag time                 | 1                     | —                 | $t_{periph}$ | —    |
| 5    | $t_{WSPSCCK}$ | Clock (SPSCCK) high or low time | $t_{periph} - 30$     | —                 | ns           | —    |
| 6    | $t_{SU}$      | Data setup time (inputs)        | 2.5                   | —                 | ns           | —    |
| 7    | $t_{HI}$      | Data hold time (inputs)         | 3.5                   | —                 | ns           | —    |
| 8    | $t_a$         | Slave access time               | —                     | $t_{periph}$      | ns           | 3    |
| 9    | $t_{dis}$     | Slave MISO disable time         | —                     | $t_{periph}$      | ns           | 4    |
| 10   | $t_v$         | Data valid (after SPSCCK edge)  | —                     | 31                | ns           | —    |
| 11   | $t_{HO}$      | Data hold time (outputs)        | 0                     | —                 | ns           | —    |
| 12   | $t_{RI}$      | Rise time input                 | —                     | $t_{periph} - 25$ | ns           | —    |
|      | $t_{FI}$      | Fall time input                 | —                     |                   |              |      |
| 13   | $t_{RO}$      | Rise time output                | —                     | 25                | ns           | —    |
|      | $t_{FO}$      | Fall time output                | —                     |                   |              |      |

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

**Table 37. SPI slave mode timing on slew rate enabled pads**

| Num. | Symbol       | Description                    | Min.                  | Max.              | Unit         | Note |
|------|--------------|--------------------------------|-----------------------|-------------------|--------------|------|
| 1    | $f_{op}$     | Frequency of operation         | 0                     | $f_{periph}/4$    | Hz           | 1    |
| 2    | $t_{SPSCK}$  | SPSCK period                   | $4 \times t_{periph}$ | —                 | ns           | 2    |
| 3    | $t_{Lead}$   | Enable lead time               | 1                     | —                 | $t_{periph}$ | —    |
| 4    | $t_{Lag}$    | Enable lag time                | 1                     | —                 | $t_{periph}$ | —    |
| 5    | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$     | —                 | ns           | —    |
| 6    | $t_{SU}$     | Data setup time (inputs)       | 2                     | —                 | ns           | —    |
| 7    | $t_{HI}$     | Data hold time (inputs)        | 7                     | —                 | ns           | —    |
| 8    | $t_a$        | Slave access time              | —                     | $t_{periph}$      | ns           | 3    |
| 9    | $t_{dis}$    | Slave MISO disable time        | —                     | $t_{periph}$      | ns           | 4    |
| 10   | $t_v$        | Data valid (after SPSCK edge)  | —                     | 130               | ns           | —    |
| 11   | $t_{HO}$     | Data hold time (outputs)       | 0                     | —                 | ns           | —    |
| 12   | $t_{RI}$     | Rise time input                | —                     | $t_{periph} - 25$ | ns           | —    |
|      | $t_{FI}$     | Fall time input                |                       |                   |              |      |
| 13   | $t_{RO}$     | Rise time output               | —                     | 36                | ns           | —    |
|      | $t_{FO}$     | Fall time output               |                       |                   |              |      |

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state



**Figure 15. SPI slave mode timing (CPHA = 0)**

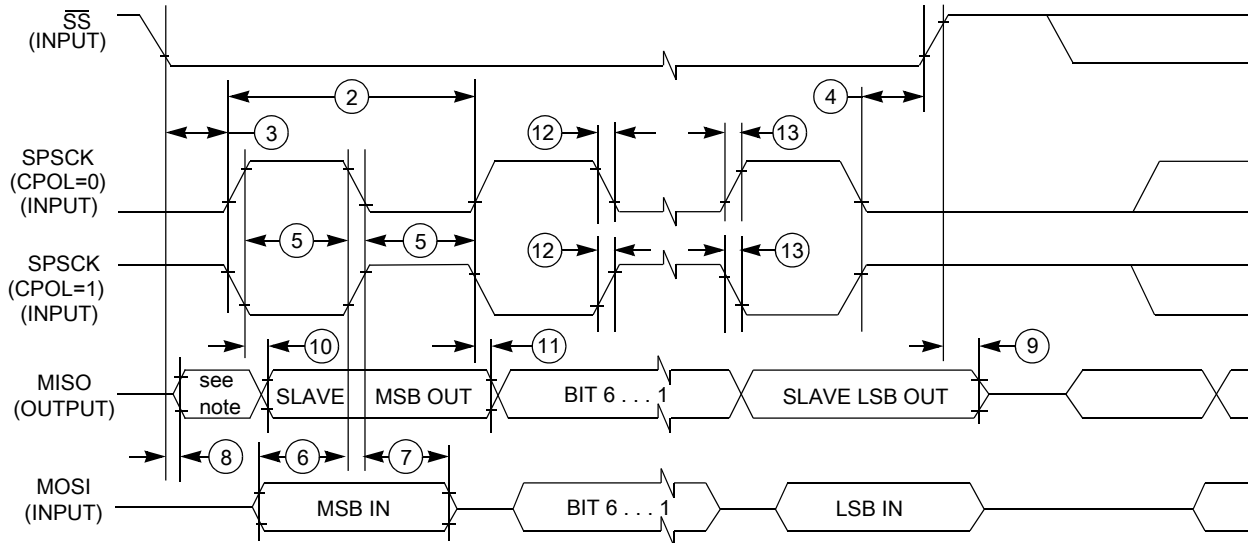


Figure 16. SPI slave mode timing (CPHA = 1)

## 5.2 I<sup>2</sup>C

### 5.2.1 Inter-Integrated Circuit Interface (I<sup>2</sup>C) timing

 Table 38. I<sup>2</sup>C timing

| Characteristic   | Symbol        | Standard Mode    |                   | Fast Mode                  |                  | Unit    |
|--|---------------|------------------|-------------------|----------------------------|------------------|---------|
|  |               | Minimum          | Maximum           | Minimum                    | Maximum          |         |
| SCL Clock Frequency  | $f_{SCL}$     | 0                | 100               | 0                          | 400 <sup>1</sup> | kHz     |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD; STA}$ | 4                | —                 | 0.6                        | —                | $\mu s$ |
| LOW period of the SCL clock  | $t_{LOW}$     | 4.7              | —                 | 1.25                       | —                | $\mu s$ |
| HIGH period of the SCL clock   | $t_{HIGH}$    | 4                | —                 | 0.6                        | —                | $\mu s$ |
| Set-up time for a repeated START condition   | $t_{SU; STA}$ | 4.7              | —                 | 0.6                        | —                | $\mu s$ |
| Data hold time for I <sup>2</sup> C bus devices  | $t_{HD; DAT}$ | 0 <sup>2</sup>   | 3.45 <sup>3</sup> | 0 <sup>4</sup>             | 0.9 <sup>2</sup> | $\mu s$ |
| Data set-up time   | $t_{SU; DAT}$ | 250 <sup>5</sup> | —                 | 100 <sup>3, 6</sup>        | —                | ns      |
| Rise time of SDA and SCL signals   | $t_r$         | —                | 1000              | $20 + 0.1C_b$ <sup>7</sup> | 300              | ns      |
| Fall time of SDA and SCL signals   | $t_f$         | —                | 300               | $20 + 0.1C_b$ <sup>6</sup> | 300              | ns      |
| Set-up time for STOP condition   | $t_{SU; STO}$ | 4                | —                 | 0.6                        | —                | $\mu s$ |
| Bus free time between STOP and START condition   | $t_{BUF}$     | 4.7              | —                 | 1.3                        | —                | $\mu s$ |
| Pulse width of spikes that must be suppressed by the input filter                            | $t_{SP}$      | N/A              | N/A               | 0                          | 50               | ns      |

## Communication interfaces

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and  $VDD \geq 2.7 V$ .
2. The master mode I<sup>2</sup>C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t<sub>HD; DAT</sub> must be met only if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I<sup>2</sup>C bus device can be used in a Standard mode I<sup>2</sup>C bus system, but the requirement  $t_{SU; DAT} \geq 250$  ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line  $t_{max} + t_{SU; DAT} = 1000 + 250 = 1250$  ns (according to the Standard mode I<sup>2</sup>C bus specification) before the SCL line is released.
7.  $C_b$  = total capacitance of the one bus line in pF.

To achieve 1MHz I<sup>2</sup>C clock rates, consider the following recommendations:

- To counter the effects of clock stretching, the I<sup>2</sup>C baud Rate select bits can be configured for faster than desired baud rate.
- Use high drive pad and DSE bit should be set in PORTx\_PCRn register.
- Minimize loading on the I<sup>2</sup>C SDA and SCL pins to ensure fastest rise times for the SCL line to avoid clock stretching.
- Use smaller pull up resistors on SDA and SCL to reduce the RC time constant.

**Table 39. I<sup>2</sup>C 1Mbit/s timing**

| Characteristic   | Symbol               | Minimum                             | Maximum        | Unit |
|--|----------------------|-------------------------------------|----------------|------|
| SCL Clock Frequency  | f <sub>SCL</sub>     | 0                                   | 1 <sup>1</sup> | MHz  |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | t <sub>HD; STA</sub> | 0.26                                | —              | μs   |
| LOW period of the SCL clock  | t <sub>LOW</sub>     | 0.5                                 | —              | μs   |
| HIGH period of the SCL clock   | t <sub>HIGH</sub>    | 0.26                                | —              | μs   |
| Set-up time for a repeated START condition   | t <sub>SU; STA</sub> | 0.26                                | —              | μs   |
| Data hold time for I <sup>2</sup> C bus devices  | t <sub>HD; DAT</sub> | 0                                   | —              | μs   |
| Data set-up time   | t <sub>SU; DAT</sub> | 50                                  | —              | ns   |
| Rise time of SDA and SCL signals   | t <sub>r</sub>       | 20 + 0.1C <sub>b</sub>              | 120            | ns   |
| Fall time of SDA and SCL signals   | t <sub>f</sub>       | 20 + 0.1C <sub>b</sub> <sup>2</sup> | 120            | ns   |
| Set-up time for STOP condition   | t <sub>SU; STO</sub> | 0.26                                | —              | μs   |
| Bus free time between STOP and START condition   | t <sub>BUF</sub>     | 0.5                                 | —              | μs   |
| Pulse width of spikes that must be suppressed by the input filter                            | t <sub>SP</sub>      | 0                                   | 50             | ns   |

1. The maximum SCL Clock Frequency of 1Mbit/s can support maximum bus loading when using the High drive pins across the full voltage range.
2.  $C_b$  = total capacitance of the one bus line in pF.

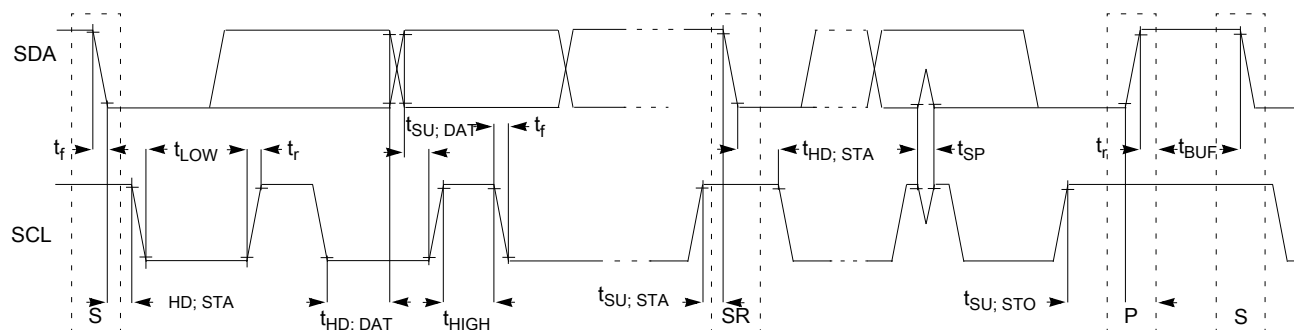


Figure 17. Timing definition for devices on the I<sup>2</sup>C bus

## 5.3 UART

See [General switching specifications](#).

## 6 Design considerations

### 6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

#### 6.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions should be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

## 6.1.2 Power delivery system

Consider the following items in the power delivery system:

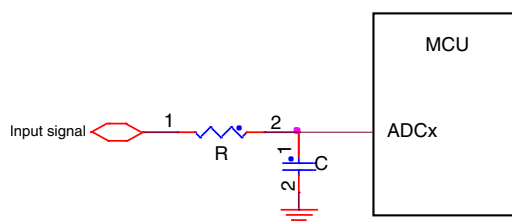
- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10uF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1  $\mu$ F capacitors positioned as near as possible to the package supply pins.
- Take special care to minimize noise levels on the VREFH/VREFL inputs. An option is to use the internal reference voltage (output 1.2V typically) as the ADC reference.

### NOTE

The internal reference voltage output (VREFO) is bonded to the VREFH pin on some packages and to PTE30 on other packages. When the VREFO output is used, a 0.1uF capacitor is required as a filter. Do not connect any other supply voltage to the pin that has VREFO activated.

## 6.1.3 Analog design

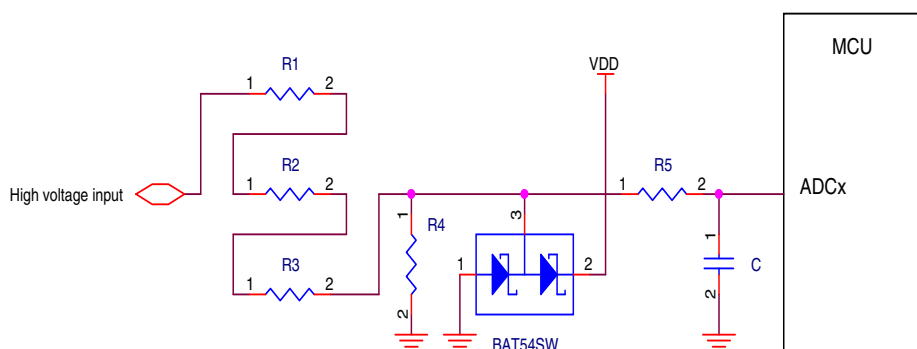
Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be  $R_{AS\ max}$  if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.



**Figure 18. RC circuit for ADC input**



High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.



**Figure 19. High voltage measurement with an ADC input**

### 6.1.4 Digital design

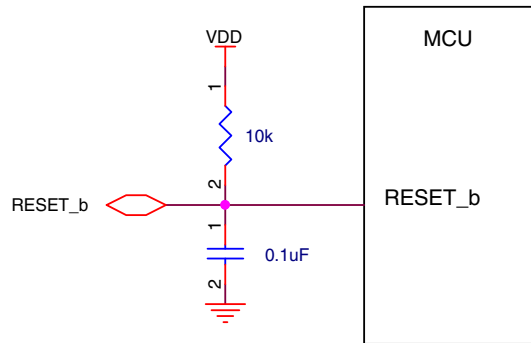
Ensure that all I/O pins cannot get pulled above VDD (max I/O spec is VDD+0.3V).

#### CAUTION

Do not provide power to I/O pins prior to VDD, especially the RESET\_b pin.

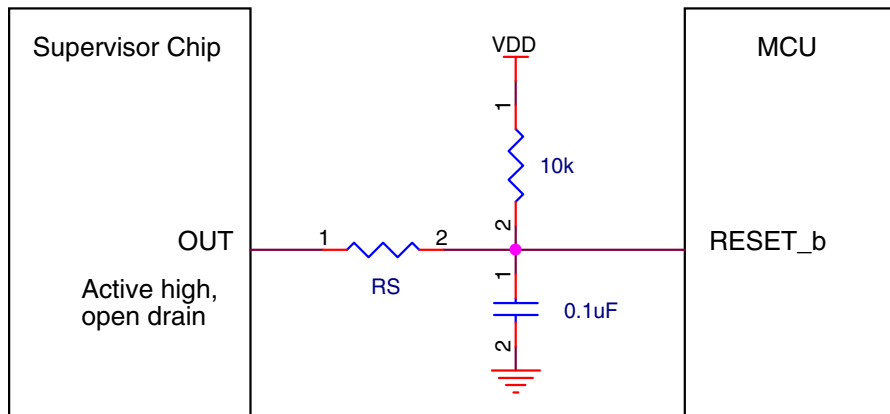
- RESET\_b pin

The RESET\_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 μF. The RESET\_b pin also has a selectable digital filter to reject spurious noise.



**Figure 20. Reset circuit**

When an external supervisor chip is connected to the RESET\_b pin, a series resistor should be used to avoid damaging the supervisor chip or the RESET\_b pin, as shown in Figure 55. The series resistor value ( $R_S$  below) should be in the range of  $100\Omega$  to  $1k\Omega$  depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

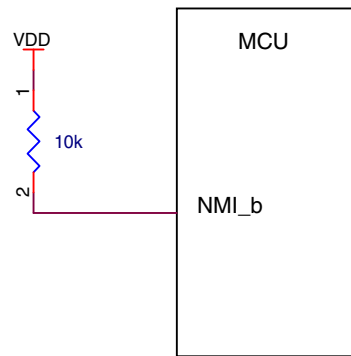


**Figure 21. Reset signal connection to external reset chip**

- NMI pin

Because a low level on the NMI\_b pin will trigger the Non-maskable interrupt, it is not recommended to add a pull-down resistor or capacitor on this pin. When this pin is enabled as the NMI function an external pull-up resistor (10k) as shown in the following figure is recommended for robustness.

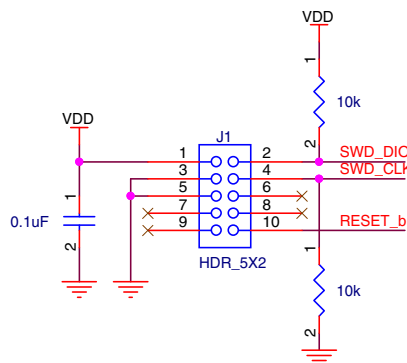
If the NMI\_b pin is used as an I/O pin the Non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI\_DIS] bit to zero.



**Figure 22. NMI pin biasing**

- Debug interface

This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD\_DIO has an internal pull-up and SWD\_CLK has an internal pull-down), external 10kΩ pull resistors are recommended for system robustness. Please note the RESET\_b pin recommendations mentioned above.



**Figure 23. SWD debug interface**

- Low leakage stop mode wakeup

Select low leakage wakeup pins (LLWU\_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). Please refer to the signal multiplexing table for pin selection.

- Unused pin

Unused GPIO pins should be left floating (no electrical connections) with the MUX field of the pin's PORTx\_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

### 6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

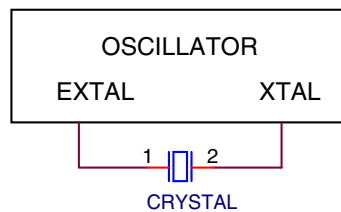
The feedback resistor,  $R_F$ , is incorporated internally with the low power oscillators. An external feedback is required when using high gain ( $HGO=1$ ) mode.

The series resistor,  $R_S$ , is required in high gain ( $HGO=1$ ) mode when the crystal or resonator frequency is below 2MHz. Otherwise, the low power oscillator ( $HGO=0$ ) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2MHz does not require any series resistance.

Internal load capacitors ( $C_x$ ,  $C_y$ ) are provided in the low frequency (32.768kHz) mode. Use the  $SCxP$  bits in the  $OSC0\_CR$  register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16pF are sufficient for 32.768kHz crystals that have a 12.5pF  $CL$  specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

**Table 40. External crystal/resonator connections**

| Oscillator mode                      | Oscillator mode      |
|--------------------------------------|----------------------|
| Low frequency (32.768kHz), low power | Diagram 1            |
| Low frequency (32.768kHz), high gain | Diagram 2, Diagram 4 |
| High frequency (1-32MHz), low power  | Diagram 3            |
| High frequency (1-32MHz), high gain  | Diagram 4            |



**Figure 24. Crystal connection – Diagram 1**

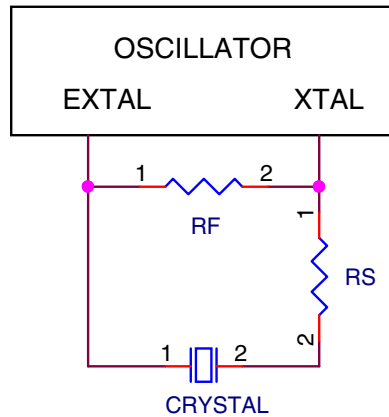


Figure 25. Crystal connection – Diagram 2

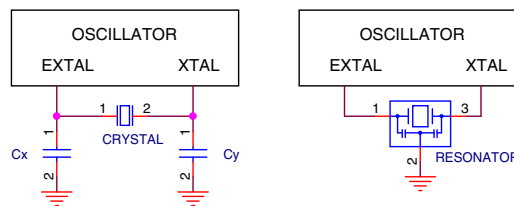


Figure 26. Crystal connection – Diagram 3

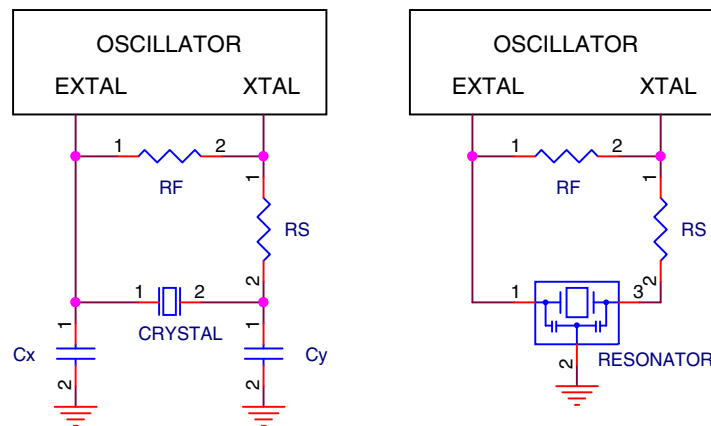


Figure 27. Crystal connection – Diagram 4

## 6.2 Software considerations

All Kinetis MCUs are supported by comprehensive Freescale and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit <http://www.freescale.com/kinetis/sw> for more information and supporting collateral.

### Evaluation and Prototyping Hardware

## Dimensions

- Freescale Freedom Development Platform: <http://www.freescale.com/freedom>
- Tower System Development Platform: <http://www.freescale.com/tower>

## IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: <http://www.freescale.com/kds>
- Partner IDEs: <http://www.freescale.com/kide>

## Development Tools

- PEG Graphics Software: <http://www.freescale.com/peg>
- Processor Expert Software and Embedded Components: <http://www.freescale.com/processorexpert> )

## Run-time Software

- Kinetis SDK: <http://www.freescale.com/ksdk>
- Kinetis Bootloader: <http://www.freescale.com/kboot>
- ARM mbed Development Platform: <http://www.freescale.com/mbed>
- MQX RTOS: <http://www.freescale.com/mqx>

For all other partner-developed software and tools, visit <http://www.freescale.com/partners>.

# 7 Dimensions

## 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://www.freescale.com) and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 32-pin QFN                               | 98ASA00615D                   |
| 48-pin QFN                               | 98ASA00616D                   |
| 64-pin LQFP                              | 98ASS23234W                   |
| 64-pin MAPBGA                            | 98ASA00420D                   |
| 80-pin LQFP                              | 98ASS23174W                   |

## 8 Pinouts and Packaging

### 8.1 KL13 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

#### NOTE

The 32 QFN, 48 QFN, and 64 MAPBGA packages for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit [freescale.com/KPYW](http://freescale.com/KPYW) for more details.

| 80 LQFP | 64 LQFP | 48 QFN | 64 MAP BGA | 32 QFN | Pin Name | Default                        | ALT0                           | ALT1                   | ALT2      | ALT3           | ALT4           | ALT5            | ALT6     | ALT7 |
|---------|---------|--------|------------|--------|----------|--------------------------------|--------------------------------|------------------------|-----------|----------------|----------------|-----------------|----------|------|
| —       | —       | —      | C5         | —      | NC       | NC                             | NC                             |                        |           |                |                |                 |          |      |
| 1       | 1       | —      | A1         | 1      | PTE0     | DISABLED                       |                                | PTE0/<br>CLKOUT32<br>K | SPI1_MISO | LPUART1_<br>TX | RTC_<br>CLKOUT | CMP0_OUT        | I2C1_SDA |      |
| 2       | 2       | —      | B1         | 2      | PTE1     | DISABLED                       |                                | PTE1                   | SPI1_MOSI | LPUART1_<br>RX |                | SPI1_MISO       | I2C1_SCL |      |
| 3       | —       | —      | —          | —      | PTE2     | DISABLED                       |                                | PTE2                   | SPI1_SCK  |                |                |                 |          |      |
| 4       | —       | —      | —          | —      | PTE3     | DISABLED                       |                                | PTE3                   | SPI1_MISO |                |                | SPI1_MOSI       |          |      |
| 5       | —       | —      | —          | —      | PTE4     | DISABLED                       |                                | PTE4                   | SPI1_PCS0 |                |                |                 |          |      |
| 6       | —       | —      | —          | —      | PTE5     | DISABLED                       |                                | PTE5                   |           |                |                |                 |          |      |
| 7       | 3       | 1      | —          | —      | VDD      | VDD                            | VDD                            |                        |           |                |                |                 |          |      |
| 8       | 4       | 2      | C4         | —      | VSS      | VSS                            | VSS                            |                        |           |                |                |                 |          |      |
| 9       | 5       | 3      | E1         | 3      | PTE16    | ADC0_DP1/<br>ADC0_SE1          | ADC0_DP1/<br>ADC0_SE1          | PTE16                  | SPI0_PCS0 | UART2_TX       | TPM_<br>CLKIN0 |                 | FXIO0_D0 |      |
| 10      | 6       | 4      | D1         | 4      | PTE17    | ADC0_<br>DM1/<br>ADC0_<br>SE5a | ADC0_<br>DM1/<br>ADC0_<br>SE5a | PTE17                  | SPI0_SCK  | UART2_RX       | TPM_<br>CLKIN1 | LPTMR0_<br>ALT3 | FXIO0_D1 |      |
| 11      | 7       | 5      | E2         | 5      | PTE18    | ADC0_DP2/<br>ADC0_SE2          | ADC0_DP2/<br>ADC0_SE2          | PTE18                  | SPI0_MOSI |                | I2C0_SDA       | SPI0_MISO       | FXIO0_D2 |      |
| 12      | 8       | 6      | D2         | 6      | PTE19    | ADC0_<br>DM2/<br>ADC0_<br>SE6a | ADC0_<br>DM2/<br>ADC0_<br>SE6a | PTE19                  | SPI0_MISO |                | I2C0_SCL       | SPI0_MOSI       | FXIO0_D3 |      |
| 13      | 9       | 7      | G1         | —      | PTE20    | ADC0_DP0/<br>ADC0_SE0          | ADC0_DP0/<br>ADC0_SE0          | PTE20                  |           | TPM1_CH0       | LPUART0_<br>TX |                 | FXIO0_D4 |      |



## Pinouts and Packaging

| 80 LQFP | 64 LQFP | 48 QFN | 64 MAP BGA | 32 QFN | Pin Name | Default                                     | ALT0                                | ALT1  | ALT2       | ALT3       | ALT4       | ALT5       | ALT6        | ALT7    |
|---------|---------|--------|------------|--------|----------|---|-------------------------------------|-------|------------|------------|------------|------------|-------------|---------|
| 14      | 10      | 8      | F1         | —      | PTE21    | ADC0_DM0/<br>ADC0_SE4a                      | ADC0_DM0/<br>ADC0_SE4a              | PTE21 |            | TPM1_CH1   | LPUART0_RX |            | FXIO0_D5    |         |
| 15      | 11      | —      | G2         | —      | PTE22    | ADC0_DP3/<br>ADC0_SE3                       | ADC0_DP3/<br>ADC0_SE3               | PTE22 |            | TPM2_CH0   | UART2_TX   |            | FXIO0_D6    |         |
| 16      | 12      | —      | F2         | —      | PTE23    | ADC0_DM3/<br>ADC0_SE7a                      | ADC0_DM3/<br>ADC0_SE7a              | PTE23 |            | TPM2_CH1   | UART2_RX   |            | FXIO0_D7    |         |
| 17      | 13      | 9      | F4         | 7      | VDDA     | VDDA  | VDDA                                |       |            |            |            |            |             |         |
| 18      | 14      | 10     | G4         | —      | VREFH    | VREFH                                       | VREFH                               |       |            |            |            |            |             |         |
| 18      | 14      | 10     | G4         | —      | VREFO    | VREFO<br>(1.2V reference,<br>bond to VREFH) | VREFH                               |       |            |            |            |            |             |         |
| 19      | 15      | 11     | G3         | —      | VREFL    | VREFL                                       | VREFL                               |       |            |            |            |            |             |         |
| 20      | 16      | 12     | F3         | 8      | VSSA     | VSSA  | VSSA                                |       |            |            |            |            |             |         |
| 21      | 17      | 13     | H1         | —      | PTE29    | CMP0_IN5/<br>ADC0_SE4b                      | CMP0_IN5/<br>ADC0_SE4b              | PTE29 |            | TPM0_CH2   | TPM_CLKIN0 |            |             |         |
| 22      | 18      | 14     | H2         | 9      | PTE30    | DAC0_OUT/<br>ADC0_SE23/<br>CMP0_IN4         | DAC0_OUT/<br>ADC0_SE23/<br>CMP0_IN4 | PTE30 |            | TPM0_CH3   | TPM_CLKIN1 | LPUART1_TX | LPTMR0_ALT1 |         |
| 23      | 19      | —      | H3         | —      | PTE31    | DISABLED                                    |                                     | PTE31 |            | TPM0_CH4   |            |            |             |         |
| 24      | 20      | 15     | H4         | —      | PTE24    | DISABLED                                    |                                     | PTE24 |            | TPM0_CH0   |            | I2C0_SCL   |             |         |
| 25      | 21      | 16     | H5         | —      | PTE25    | DISABLED                                    |                                     | PTE25 |            | TPM0_CH1   |            | I2C0_SDA   |             |         |
| 26      | 22      | 17     | D3         | 10     | PTA0     | SWD_CLK                                     |                                     | PTA0  |            | TPM0_CH5   |            |            |             | SWD_CLK |
| 27      | 23      | 18     | D4         | 11     | PTA1     | DISABLED                                    |                                     | PTA1  | LPUART0_RX | TPM2_CH0   |            |            |             |         |
| 28      | 24      | 19     | E5         | 12     | PTA2     | DISABLED                                    |                                     | PTA2  | LPUART0_TX | TPM2_CH1   |            |            |             |         |
| 29      | 25      | 20     | D5         | 13     | PTA3     | SWD_DIO                                     |                                     | PTA3  | I2C1_SCL   | TPM0_CH0   |            |            |             | SWD_DIO |
| 30      | 26      | 21     | G5         | 14     | PTA4     | NMI_b                                       |                                     | PTA4  | I2C1_SDA   | TPM0_CH1   |            |            |             | NMI_b   |
| 31      | 27      | —      | F5         | —      | PTA5     | DISABLED                                    |                                     | PTA5  |            | TPM0_CH2   |            |            |             |         |
| 32      | 28      | —      | H6         | —      | PTA12    | DISABLED                                    |                                     | PTA12 |            | TPM1_CH0   |            |            |             |         |
| 33      | 29      | —      | G6         | —      | PTA13    | DISABLED                                    |                                     | PTA13 |            | TPM1_CH1   |            |            |             |         |
| 34      | —       | —      | —          | —      | PTA14    | DISABLED                                    |                                     | PTA14 | SPI0_PCS0  | LPUART0_TX |            |            |             |         |
| 35      | —       | —      | —          | —      | PTA15    | DISABLED                                    |                                     | PTA15 | SPI0_SCK   | LPUART0_RX |            |            |             |         |
| 36      | —       | —      | —          | —      | PTA16    | DISABLED                                    |                                     | PTA16 | SPI0_MOSI  |            |            | SPI0_MISO  |             |         |



| 80 LQFP | 64 LQFP | 48 QFN | 64 MAP BGA | 32 QFN | Pin Name               | Default   | ALT0      | ALT1                   | ALT2      | ALT3        | ALT4       | ALT5      | ALT6        | ALT7    |
|---------|---------|--------|------------|--------|------------------------|-----------|-----------|------------------------|-----------|-------------|------------|-----------|-------------|---------|
| 37      | —       | —      | —          | —      | PTA17                  | DISABLED  |           | PTA17                  | SPI0_MISO |             |            | SPI0_MOSI |             |         |
| 38      | 30      | 22     | G7         | 15     | VDD                    | VDD       | VDD       |                        |           |             |            |           |             |         |
| 39      | 31      | 23     | H7         | 16     | VSS                    | VSS       | VSS       |                        |           |             |            |           |             |         |
| 40      | 32      | 24     | H8         | 17     | PTA18                  | EXTAL0    | EXTAL0    | PTA18                  |           | LPUART1_RX  | TPM_CLKIN0 |           |             |         |
| 41      | 33      | 25     | G8         | 18     | PTA19                  | XTAL0     | XTAL0     | PTA19                  |           | LPUART1_TX  | TPM_CLKIN1 |           | LPTMR0_ALT1 |         |
| 42      | 34      | 26     | F8         | 19     | PTA20                  | RESET_b   |           | PTA20                  |           |             |            |           |             | RESET_b |
| 43      | 35      | 27     | F7         | 20     | PTB0/LLWU_P5           | ADC0_SE8  | ADC0_SE8  | PTB0/LLWU_P5           | I2C0_SCL  | TPM1_CH0    | SPI1_MOSI  | SPI1_MISO |             |         |
| 44      | 36      | 28     | F6         | 21     | PTB1                   | ADC0_SE9  | ADC0_SE9  | PTB1                   | I2C0_SDA  | TPM1_CH1    | SPI1_MISO  | SPI1_MOSI |             |         |
| 45      | 37      | 29     | E7         | —      | PTB2                   | ADC0_SE12 | ADC0_SE12 | PTB2                   | I2C0_SCL  | TPM2_CH0    |            |           |             |         |
| 46      | 38      | 30     | E8         | —      | PTB3                   | ADC0_SE13 | ADC0_SE13 | PTB3                   | I2C0_SDA  | TPM2_CH1    |            |           |             |         |
| 47      | —       | —      | —          | —      | PTB8                   |           |           | PTB8                   | SPI1_PCS0 | EXTRG_IN    |            |           |             |         |
| 48      | —       | —      | —          | —      | PTB9                   |           |           | PTB9                   | SPI1_SCK  |             |            |           |             |         |
| 49      | —       | —      | —          | —      | PTB10                  |           |           | PTB10                  | SPI1_PCS0 |             |            |           |             |         |
| 50      | —       | —      | —          | —      | PTB11                  |           |           | PTB11                  | SPI1_SCK  |             |            |           |             |         |
| 51      | 39      | 31     | E6         | —      | PTB16                  |           |           | PTB16                  | SPI1_MOSI | LPUART0_RX  | TPM_CLKIN0 | SPI1_MISO |             |         |
| 52      | 40      | 32     | D7         | —      | PTB17                  |           |           | PTB17                  | SPI1_MISO | LPUART0_TX  | TPM_CLKIN1 | SPI1_MOSI |             |         |
| 53      | 41      | —      | D6         | —      | PTB18                  |           |           | PTB18                  |           | TPM2_CH0    |            |           |             |         |
| 54      | 42      | —      | C7         | —      | PTB19                  |           |           | PTB19                  |           | TPM2_CH1    |            |           |             |         |
| 55      | 43      | 33     | D8         | —      | PTC0                   | ADC0_SE14 | ADC0_SE14 | PTC0                   |           | EXTRG_IN    |            | CMP0_OUT  |             |         |
| 56      | 44      | 34     | C6         | 22     | PTC1/LLWU_P6/RTC_CLKIN | ADC0_SE15 | ADC0_SE15 | PTC1/LLWU_P6/RTC_CLKIN | I2C1_SCL  |             | TPM0_CH0   |           |             |         |
| 57      | 45      | 35     | B7         | 23     | PTC2                   | ADC0_SE11 | ADC0_SE11 | PTC2                   | I2C1_SDA  |             | TPM0_CH1   |           |             |         |
| 58      | 46      | 36     | C8         | 24     | PTC3/LLWU_P7           |           |           | PTC3/LLWU_P7           | SPI1_SCK  | LPUART1_RX  | TPM0_CH2   | CLKOUT    |             |         |
| 59      | 47      | —      | E3         | —      | VSS                    | VSS       | VSS       |                        |           |             |            |           |             |         |
| 60      | 48      | —      | E4         | —      | VDD                    | VDD       | VDD       |                        |           |             |            |           |             |         |
| 61      | 49      | 37     | B8         | 25     | PTC4/LLWU_P8           |           |           | PTC4/LLWU_P8           | SPI0_PCS0 | LPUART1_TX  | TPM0_CH3   | SPI1_PCS0 |             |         |
| 62      | 50      | 38     | A8         | 26     | PTC5/LLWU_P9           |           |           | PTC5/LLWU_P9           | SPI0_SCK  | LPTMR0_ALT2 |            |           | CMP0_OUT    |         |
| 63      | 51      | 39     | A7         | 27     | PTC6/LLWU_P10          | CMP0_IN0  | CMP0_IN0  | PTC6/LLWU_P10          | SPI0_MOSI | EXTRG_IN    |            | SPI0_MISO |             |         |
| 64      | 52      | 40     | B6         | 28     | PTC7                   | CMP0_IN1  | CMP0_IN1  | PTC7                   | SPI0_MISO |             |            | SPI0_MOSI |             |         |

## Pinouts and Packaging

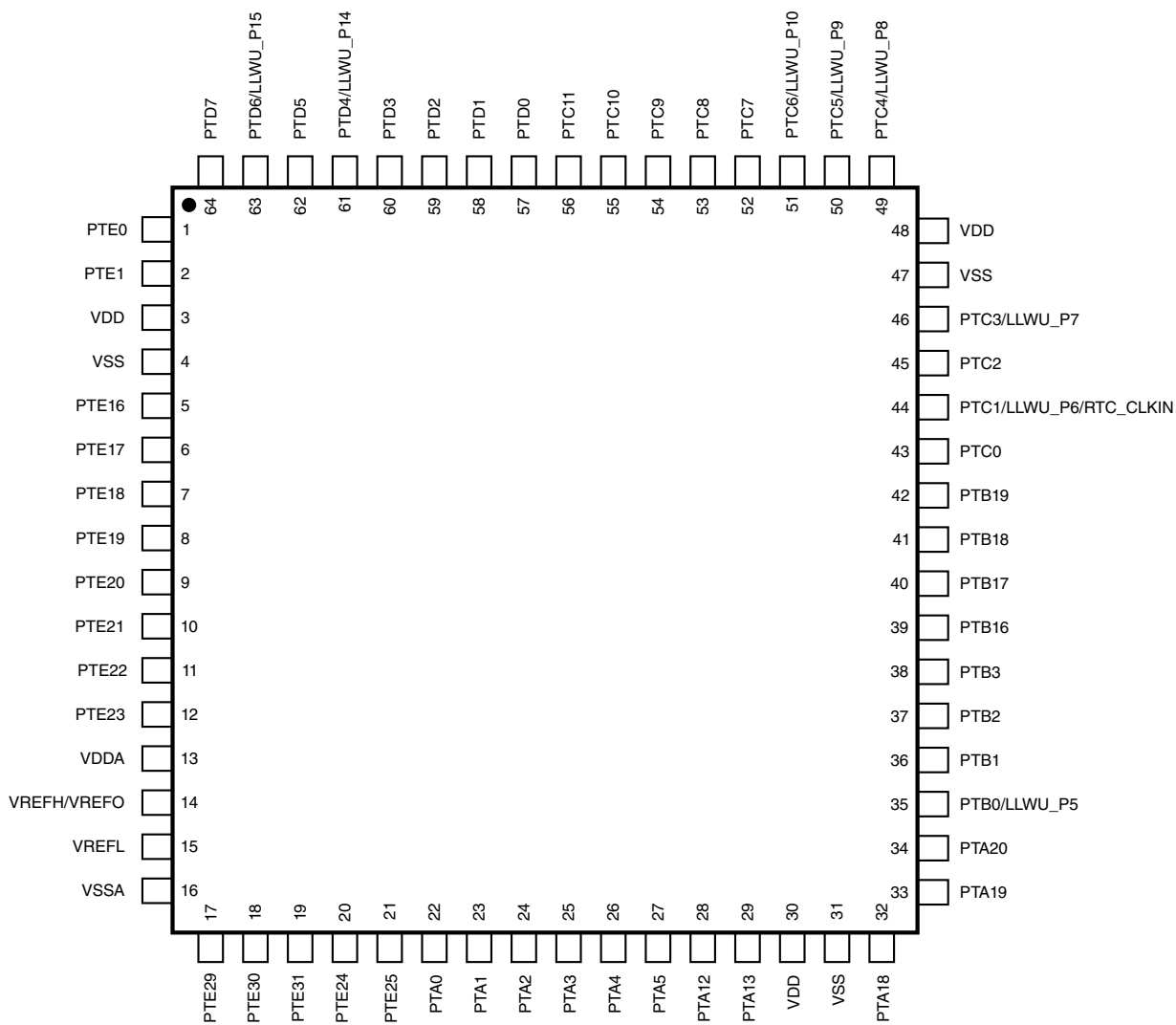
| 80 LQFP | 64 LQFP | 48 QFN | 64 MAP BGA | 32 QFN | Pin Name      | Default   | ALT0      | ALT1          | ALT2      | ALT3       | ALT4       | ALT5      | ALT6     | ALT7 |
|---------|---------|--------|------------|--------|---------------|-----------|-----------|---------------|-----------|------------|------------|-----------|----------|------|
| 65      | 53      | —      | A6         | —      | PTC8          | CMP0_IN2  | CMP0_IN2  | PTC8          | I2C0_SCL  | TPM0_CH4   |            |           |          |      |
| 66      | 54      | —      | B5         | —      | PTC9          | CMP0_IN3  | CMP0_IN3  | PTC9          | I2C0_SDA  | TPM0_CH5   |            |           |          |      |
| 67      | 55      | —      | B4         | —      | PTC10         |           |           | PTC10         | I2C1_SCL  |            |            |           |          |      |
| 68      | 56      | —      | A5         | —      | PTC11         |           |           | PTC11         | I2C1_SDA  |            |            |           |          |      |
| 69      | —       | —      | —          | —      | PTC12         |           |           | PTC12         |           |            | TPM_CLKIN0 |           |          |      |
| 70      | —       | —      | —          | —      | PTC13         |           |           | PTC13         |           |            | TPM_CLKIN1 |           |          |      |
| 71      | —       | —      | —          | —      | PTC16         |           |           | PTC16         |           |            |            |           |          |      |
| 72      | —       | —      | —          | —      | PTC17         |           |           | PTC17         |           |            |            |           |          |      |
| 73      | 57      | 41     | C3         | —      | PTD0          |           |           | PTD0          | SPI0_PCS0 |            | TPM0_CH0   |           | FXIO0_D0 |      |
| 74      | 58      | 42     | A4         | —      | PTD1          | ADC0_SE5b | ADC0_SE5b | PTD1          | SPI0_SCK  |            | TPM0_CH1   |           | FXIO0_D1 |      |
| 75      | 59      | 43     | C2         | —      | PTD2          |           |           | PTD2          | SPI0_MOSI | UART2_RX   | TPM0_CH2   | SPI0_MISO | FXIO0_D2 |      |
| 76      | 60      | 44     | B3         | —      | PTD3          |           |           | PTD3          | SPI0_MISO | UART2_TX   | TPM0_CH3   | SPI0_MOSI | FXIO0_D3 |      |
| 77      | 61      | 45     | A3         | 29     | PTD4/LLWU_P14 |           |           | PTD4/LLWU_P14 | SPI1_PCS0 | UART2_RX   | TPM0_CH4   |           | FXIO0_D4 |      |
| 78      | 62      | 46     | C1         | 30     | PTD5          | ADC0_SE6b | ADC0_SE6b | PTD5          | SPI1_SCK  | UART2_TX   | TPM0_CH5   |           | FXIO0_D5 |      |
| 79      | 63      | 47     | B2         | 31     | PTD6/LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/LLWU_P15 | SPI1_MOSI | LPUART0_RX | I2C1_SDA   | SPI1_MISO | FXIO0_D6 |      |
| 80      | 64      | 48     | A2         | 32     | PTD7          |           |           | PTD7          | SPI1_MISO | LPUART0_TX | I2C1_SCL   | SPI1_MOSI | FXIO0_D7 |      |

## 8.2 KL13 Family Pinouts

Figure below shows the 64 LQFP pinouts:

### NOTE

The 32 QFN, 48 QFN, and 64 MAPBGA packages for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit [freescale.com/KPYW](http://freescale.com/KPYW) for more details.



**Figure 28. 64 LQFP Pinout diagram**

Figure below shows the 80 LQFP pinouts:

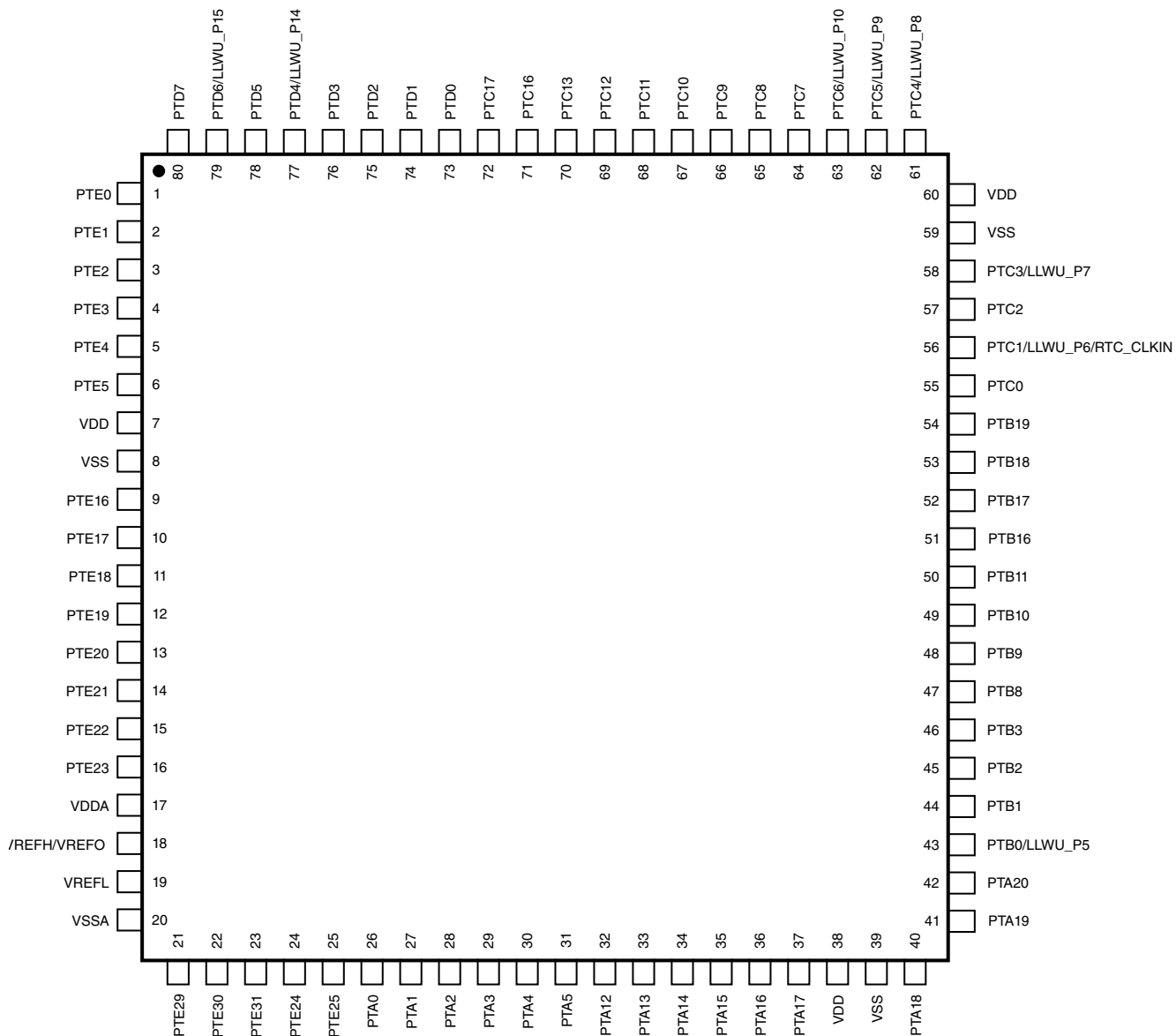


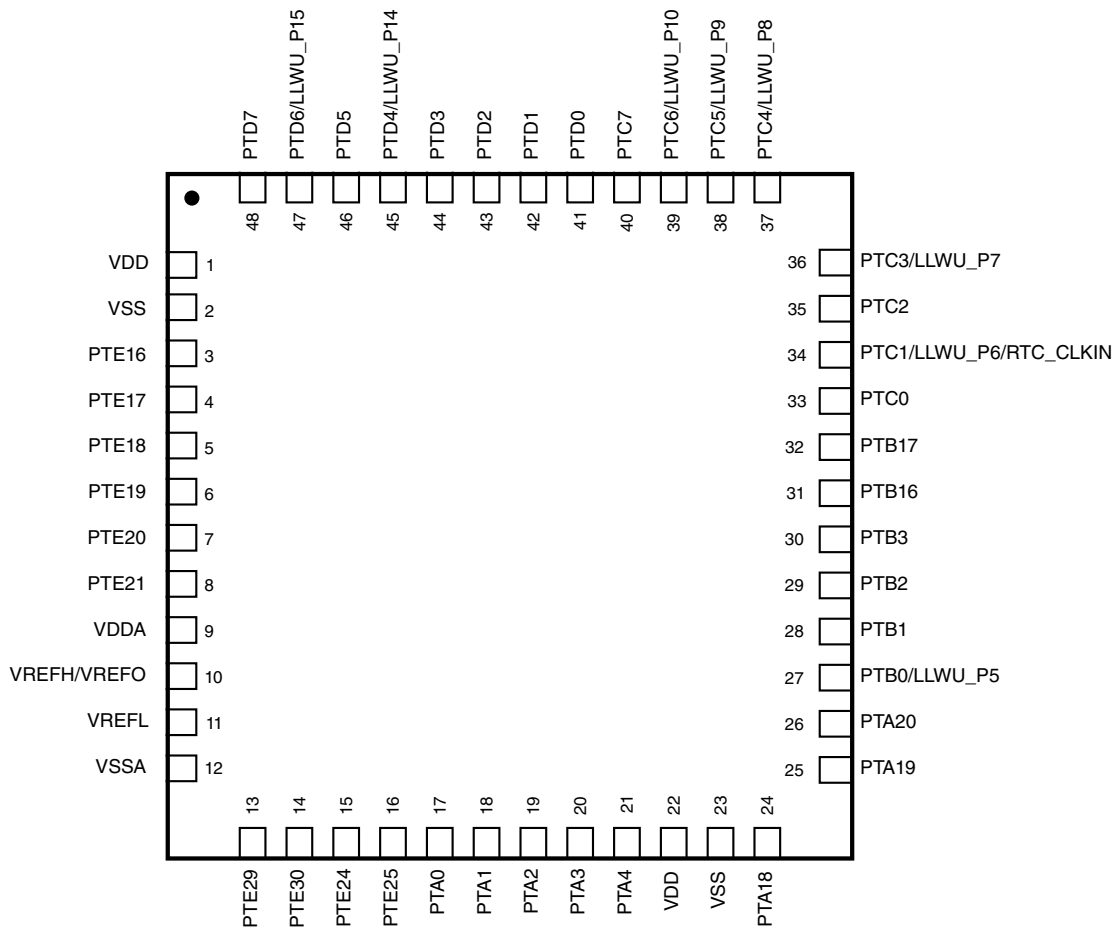
Figure 29. 80 LQFP Pinout diagram

Figure below shows the 64 MAPBGA pinouts:

|   |       |                   |                   |                 |       |                                |                   |                  |   |
|---|-------|-------------------|-------------------|-----------------|-------|--------------------------------|-------------------|------------------|---|
|   | 1     | 2                 | 3                 | 4               | 5     | 6                              | 7                 | 8                |   |
| A | PTE0  | PTD7              | PTD4/<br>LLWU_P14 | PTD1            | PTC11 | PTC8                           | PTC6/<br>LLWU_P10 | PTC5/<br>LLWU_P9 | A |
| B | PTE1  | PTD6/<br>LLWU_P15 | PTD3              | PTC10           | PTC9  | PTC7                           | PTC2              | PTC4/<br>LLWU_P8 | B |
| C | PTD5  | PTD2              | PTD0              | VSS             | NC    | PTC1/<br>LLWU_P6/<br>RTC_CLKIN | PTB19             | PTC3/<br>LLWU_P7 | C |
| D | PTE17 | PTE19             | PTA0              | PTA1            | PTA3  | PTB18                          | PTB17             | PTC0             | D |
| E | PTE16 | PTE18             | VSS               | VDD             | PTA2  | PTB16                          | PTB2              | PTB3             | E |
| F | PTE21 | PTE23             | VSSA              | VDDA            | PTA5  | PTB1                           | PTB0/<br>LLWU_P5  | PTA20            | F |
| G | PTE20 | PTE22             | VREFL             | VREFH/<br>VREFO | PTA4  | PTA13                          | VDD               | PTA19            | G |
| H | PTE29 | PTE30             | PTE31             | PTE24           | PTE25 | PTA12                          | VSS               | PTA18            | H |
|   | 1     | 2                 | 3                 | 4               | 5     | 6                              | 7                 | 8                |   |

**Figure 30. 64 MAPBGA Pinout diagram**

Figure below shows the 48 QFN pinouts:



**Figure 31. 48 QFN Pinout diagram**

Figure below shows the 32 QFN pinouts:

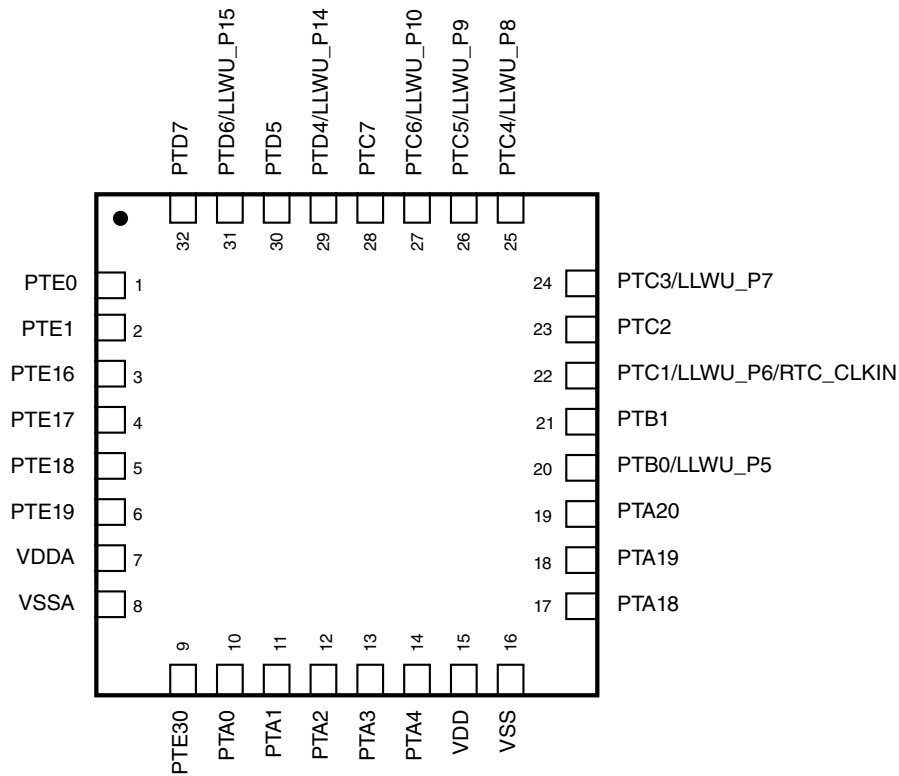


Figure 32. 32 QFN Pinout diagram

## 9 Ordering parts

### 9.1 Determining valid orderable parts

Valid orderable part numbers are provided on the Web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers:

## 10 Part identification

### 10.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 10.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

## 10.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

**Table 41. Part number fields description**

| Field | Description                 | Values  |
|-------|-----------------------------|---|
| Q     | Qualification status        | <ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>  |
| KL##  | Kinetis family              | <ul style="list-style-type: none"> <li>KL13</li> </ul>  |
| A     | Key attribute               | <ul style="list-style-type: none"> <li>Z = Cortex-M0+</li> </ul>  |
| FFF   | Program flash memory size   | <ul style="list-style-type: none"> <li>32 = 32 KB</li> <li>64 = 64 KB</li> </ul>  |
| R     | Silicon revision            | <ul style="list-style-type: none"> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>   |
| T     | Temperature range (°C)      | <ul style="list-style-type: none"> <li>V = -40 to 105</li> </ul>  |
| PP    | Package identifier          | <ul style="list-style-type: none"> <li>FM = 32 QFN (5 mm x 5 mm) <sup>1</sup></li> <li>FT = 48 QFN (7 mm x 7 mm) <sup>1</sup></li> <li>LH = 64 LQFP (10 mm x 10 mm)</li> <li>MP = 64 MAPBGA (5 mm x 5 mm) <sup>1</sup></li> <li>LK = 80 LQFP (12 mm x 12 mm)</li> </ul> |
| CC    | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> <li>4 = 48 MHz</li> </ul>  |
| N     | Packaging type              | <ul style="list-style-type: none"> <li>R = Tape and reel</li> </ul>   |

1. This package for this product is not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit [freescale.com/KPYW](http://freescale.com/KPYW) for more details.

## 10.4 Example

This is an example part number:

MKL13Z32VLH4



## 11 Terminology and guidelines

### 11.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 11.1.1 Example

This is an example of an operating requirement:

| Symbol          | Description               | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V <sub>DD</sub> | 1.0 V core supply voltage | 0.9  | 1.1  | V    |

### 11.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

#### 11.2.1 Example

This is an example of an operating behavior:

| Symbol          | Description                              | Min. | Max. | Unit |
|-----------------|--|------|------|------|
| I <sub>WP</sub> | Digital I/O weak pullup/pulldown current | 10   | 130  | μA   |

## 11.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 11.3.1 Example

This is an example of an attribute:

| Symbol | Description                     | Min. | Max. | Unit |
|--------|---------------------------------|------|------|------|
| CIN_D  | Input capacitance: digital pins | —    | 7    | pF   |

## 11.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

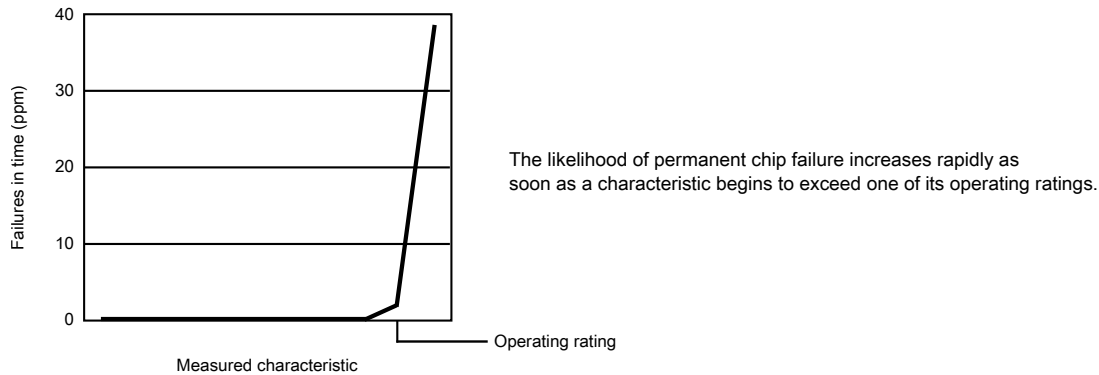
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 11.4.1 Example

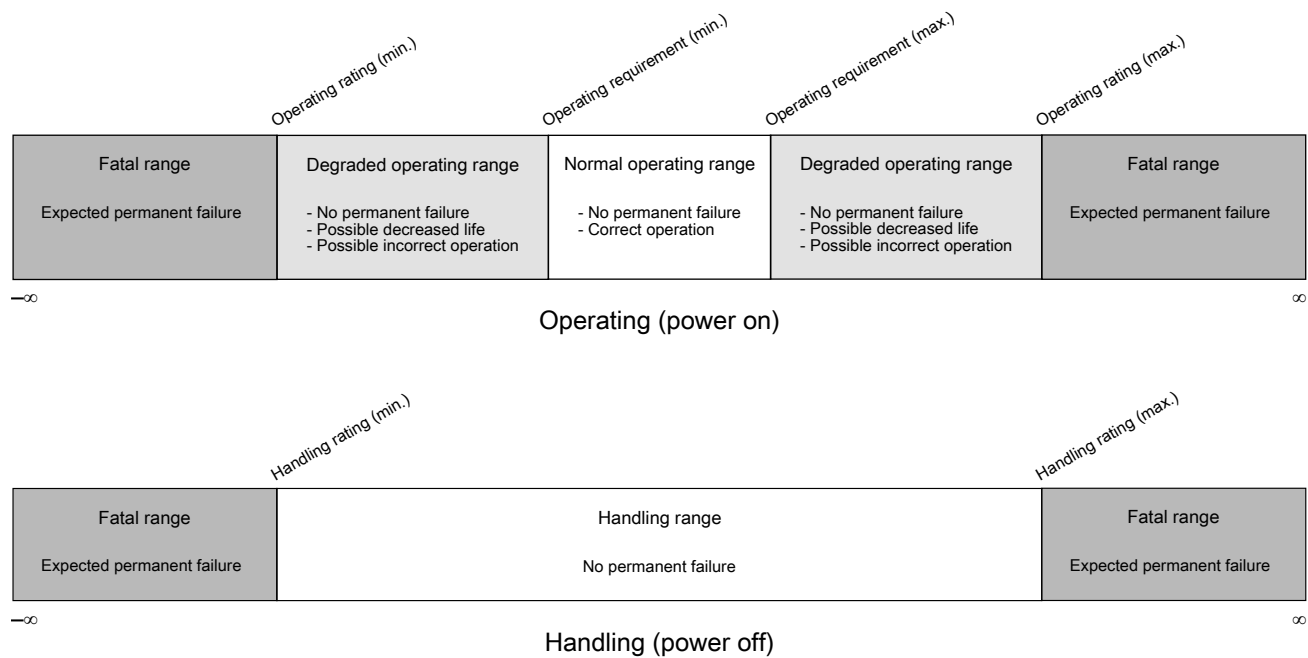
This is an example of an operating rating:

| Symbol          | Description               | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V <sub>DD</sub> | 1.0 V core supply voltage | -0.3 | 1.2  | V    |

## 11.5 Result of exceeding a rating



## 11.6 Relationship between ratings and operating requirements



## 11.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 11.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

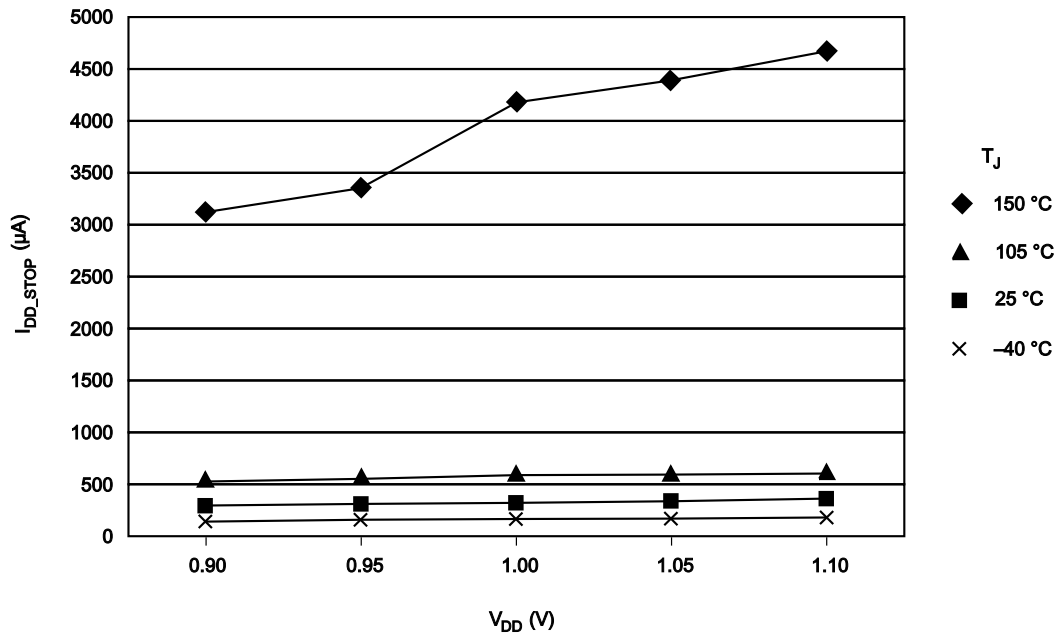
### 11.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol   | Description                              | Min. | Typ. | Max. | Unit    |
|----------|--|------|------|------|---------|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10   | 70   | 130  | $\mu A$ |

### 11.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



## 11.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

**Table 42. Typical value conditions**

| Symbol          | Description          | Value | Unit |
|-----------------|----------------------|-------|------|
| T <sub>A</sub>  | Ambient temperature  | 25    | °C   |
| V <sub>DD</sub> | 3.3 V supply voltage | 3.3   | V    |

## 12 Revision History

The following table provides a revision history for this document.

**Table 43. Revision History**

| Rev. No. | Date             | Substantial Changes  |
|----------|------------------|--|
| 1        | 01 February 2015 | <ul style="list-style-type: none"> <li>Added new topic "Electrical Design Considerations" as Section 6.</li> <li>Added a note in Table 14 - Thermal operating requirements.</li> <li>Footnote 1 in Table 9 was moved in the beginning of the table as text.</li> </ul> |

*Table continues on the next page...*

**Table 43. Revision History (continued)**

| Rev. No. | Date          | Substantial Changes   |
|----------|---------------|---|
| 2        | 18 March 2015 | <ul style="list-style-type: none"> <li>• Updated the features and completed the ordering information.</li> <li>• Removed thickness dimension from package diagrams.</li> <li>• Updated Table 7. Voltage and current operating behaviors.               <ul style="list-style-type: none"> <li>• Specified correct max. value for <math>I_{IN}</math> parameter.</li> </ul> </li> <li>• Updated Table 8. Power mode transition operating behaviors with Typ. and Max. values.</li> <li>• Updated Table 9. Power consumption operating behaviors with Typ. and Max. values.</li> <li>• Updated Table 10. Low power mode peripheral adders — typical value.</li> <li>• Updated EMC Performance information in section 2.2.6.</li> <li>• Updated Table 17. IRC48M specification and Table 18. IRC8M/2M specification.</li> <li>• Updated Typ. values of TUE and INL parameters in Table 26. 16-bit ADC characteristics.</li> <li>• Updated Table 28. VREF full-range operating behaviors.               <ul style="list-style-type: none"> <li>• Removed <math>A_c</math>(Aging coefficient) row.</li> <li>• Added <math>T_{chop\_osc\_stup}</math> parameter.</li> <li>• Updated typical value of the <math>V_{out}</math> parameter.</li> </ul> </li> <li>• Added tables: "I2C timing" and "I2C 1Mbit/s timing" under section - I2C.</li> <li>• Updated Section 6 - Design Considerations.</li> </ul> |



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