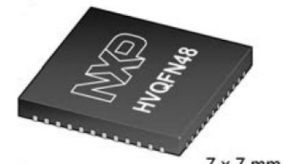


MKW39/38/37 Data Sheet

An ultra low-power, highly integrated Bluetooth® Low Energy 5.0 wireless microcontroller

MKW39A512VFT4
MKW38A512VFT4
MKW38Z512VFT4
MKW37A512VFT4
MKW37Z512VFT4



7 x 7 mm

48 "Wettable" HVQFN
7x7 mm Pitch 0.5 mm

Multi-Standard Radio

- 2.4 GHz Bluetooth Low Energy (Bluetooth LE) version 5.0 compliant supporting up to 8 simultaneous hardware connections and all optional features including:
 - High speed (2M PHY)
 - Long range
 - Advertising Extension
 - High duty cycle non-connectable advertising
 - Channel selection algorithm #2
- Typical Bluetooth LE Receiver Sensitivity
 - Bluetooth LE 2 Mbit/s: -95.5 dBm
 - Bluetooth LE 1 Mbit/s: -98 dBm
 - Bluetooth LE LR 500 kbit/s: -101 dBm
 - Bluetooth LE LR 125 kbit/s: -105 dBm
- Generic FSK modulation
 - Data Rate: 250, 500, 1000 and 2000 kbit/s
 - Modulations: GFSK BT = 0.5, MSK
 - Modulation Index: 0.32, 0.5, 0.7, and 1.0
 - Typical Receiver Sensitivity (250 kbit/s GFSK-BT=0.5, h=0.5) = -101 dBm
- Programmable Transmitter Output Power: -30 dBm to +5 dBm
- Low external component count for low-cost application
- On-chip balun with single ended bidirectional RF port

System peripherals

- Nine MCU low-power modes to provide power optimization based on application requirements
- DC-DC Converter supporting Buck and Bypass operating modes
- Direct Memory Access (DMA) controller
- Computer Operating Properly (COP) watchdog
- Serial Wire Debug (SWD) Interface and Micro Trace buffer
- Bit Manipulation Engine (BME)

Timers

- 16-bit Low-power Timer (LPTMR)
- 3 Timer/PWM Modules (TPM): One 4 channel TPM and two 2 channel TPMs
- Programmable Interrupt Timer (PIT)
- Real-Time Clock (RTC)

Communication interfaces

- 2 Serial Peripheral Interface (SPI) modules
- 2 Inter-integrated Circuit (I2C) modules
- Low-power UART (LPUART) module with LIN support (2x LPUART on KW38)
- Carrier Modulator Timer (CMT)
- FlexCAN module (with CAN FD support up to 3.2 Mbit/s baudrate) on KW38

Analog Modules

- 16-bit Analog-to-Digital Converter (ADC)
- 6-bit High-Speed Analog Comparator (CMP)
- 1.2 V Voltage Reference (VREF)

MCU and Memories

- 256 KB program flash memory plus 256 KB FlexNVM on KW39/38
- 512 KB program flash memory on KW37
- 8 KB FlexRAM supporting EEPROM emulation on KW39/38
- 8 KB program acceleration RAM on KW37
- On-chip 64 KB SRAM
- Up to 48 MHz Arm® Cortex®-M0+ core

Low-power Consumption

- Transceiver current (DC-DC buck mode, 3.6 V supply)
 - Typical Rx current: 6.3 mA
 - Typical Tx current: 5.7 mA
- Low-power Mode (VLLS0) Current: 266.6 nA

Security

- AES-128 Hardware Accelerator (AESA)
- True Random Number Generator (TRNG)
- Advanced flash security on Program Flash
- 80-bit unique identification number per chip
- 40-bit unique Media Access Control (MAC) sub-address
- LE Secure Connections

Clocks

- 26 and 32 MHz supported for Bluetooth LE and Generic FSK modes
- 32.768 kHz Crystal Oscillator

Operating Characteristics

- Voltage range: 1.71 V to 3.6 V
- Ambient temperature range: -40 to 105 °C
- AEC Q100 Grade 2 Automotive Qualification
- Industrial Qualification

Human-machine Interface (HMI)

- General-purpose input/output (GPIO)

KW39/38/37 Part Numbers

| Device | Qualification Tier | CAN FD | 512 KB P-Flash | 256 KB P-Flash/256 KB FlexNVM | Second LPUART with LIN | 8 KB FlexRAM EEPROM | Package |
|---------------|-----------------------|--------|----------------|-------------------------------|------------------------|---------------------|--------------------------------|
| MKW39A512VFT4 | Auto AEC-Q100 Grade 2 | N | N | Y | N | Y | 7X7 mm 48-pin "Wettable" HVQFN |
| MKW38A512VFT4 | Auto AEC-Q100 Grade 2 | Y | N | Y | Y | Y | |
| MKW38Z512VFT4 | Industrial | Y | N | Y | Y | Y | |
| MKW37A512VFT4 | Auto AEC-Q100 Grade 2 | N | Y | N | N | N | |
| MKW37Z512VFT4 | Industrial | N | Y | N | N | N | |

Related Resources

| Type | Description |
|------------------|--|
| Product Selector | The Product Selector lets you find the right Kinetis part for your design. |
| Fact Sheet | The Fact Sheet gives overview of the product key features and its uses. |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. |
| Package drawing | Package dimensions are available in package drawings. |

Table of Contents

| | | | | | |
|-------|--|----|-------|--|----|
| 1 | Introduction..... | 5 | 6.4.1 | Thermal operating requirements..... | 51 |
| 2 | Feature Descriptions..... | 6 | 6.4.2 | Thermal attributes..... | 51 |
| 2.1 | Block Diagram..... | 6 | 6.5 | Peripheral operating requirements and behaviors..... | 52 |
| 2.2 | Radio features..... | 8 | 6.5.1 | Core modules..... | 52 |
| 2.3 | Microcontroller features..... | 9 | 6.5.2 | System modules..... | 53 |
| 2.4 | System features..... | 10 | 6.5.3 | Clock modules..... | 54 |
| 2.5 | Peripheral features..... | 12 | 6.5.4 | Memories and memory interfaces..... | 57 |
| 2.6 | Security Features..... | 17 | 6.5.5 | Security and integrity modules..... | 61 |
| 3 | Transceiver Description..... | 18 | 6.5.6 | Analog..... | 61 |
| 3.1 | Transceiver Functions..... | 18 | 6.5.7 | Timers..... | 68 |
| 3.2 | Key Specifications..... | 19 | 6.5.8 | Communication interfaces..... | 68 |
| 3.3 | Channel Map Frequency Plans | 19 | 6.5.9 | Human-machine interfaces (HMI)..... | 73 |
| 3.3.1 | Channel Plan for Bluetooth Low Energy..... | 19 | 6.6 | DC-DC Converter Operating Requirements..... | 73 |
| 3.3.2 | Other Channel Plans | 21 | 6.7 | Ratings..... | 75 |
| 4 | Transceiver Electrical Characteristics..... | 21 | 6.7.1 | Thermal handling ratings..... | 75 |
| 4.1 | Radio operating conditions..... | 21 | 6.7.2 | Moisture handling ratings..... | 75 |
| 4.2 | Receiver Feature Summary..... | 22 | 6.7.3 | ESD handling ratings..... | 76 |
| 4.3 | Transmit and PLL Feature Summary..... | 26 | 6.7.4 | Voltage and current operating ratings..... | 76 |
| 5 | System and Power Management..... | 31 | 7 | Pin Diagrams and Pin Assignments..... | 76 |
| 5.1 | Power Management..... | 31 | 7.1 | KW39/37 Signal Multiplexing and Pin Assignments..... | 77 |
| 5.1.1 | DC-DC Converter..... | 32 | 7.2 | KW38 Signal Multiplexing and Pin Assignments..... | 79 |
| 5.2 | Modes of Operation..... | 32 | 7.3 | KW39/38/37 Pinouts..... | 82 |
| 5.2.1 | Power modes..... | 32 | 7.4 | Module Signal Description Tables..... | 83 |
| 6 | KW39/38/37 Electrical Characteristics..... | 35 | 7.4.1 | Core Modules..... | 83 |
| 6.1 | AC electrical characteristics..... | 35 | 7.4.2 | Radio Modules..... | 84 |
| 6.2 | Nonswitching electrical specifications..... | 35 | 7.4.3 | System Modules..... | 85 |
| 6.2.1 | Voltage and current operating requirements..... | 35 | 7.4.4 | Clock Modules..... | 85 |
| 6.2.2 | LVD and POR operating requirements..... | 36 | 7.4.5 | Analog Modules..... | 86 |
| 6.2.3 | Voltage and current operating behaviors..... | 37 | 7.4.6 | Timer Modules..... | 87 |
| 6.2.4 | Power mode transition operating behaviors..... | 38 | 7.4.7 | Communication Interfaces..... | 87 |
| 6.2.5 | Power consumption operating behaviors..... | 39 | 7.4.8 | Human-Machine Interfaces(HMI)..... | 89 |
| 6.2.6 | Diagram: Typical IDD_RUN operating behavior..... | 46 | 8 | Package Information..... | 89 |
| 6.2.7 | SoC Power Consumption..... | 48 | 8.1 | Obtaining package dimensions..... | 89 |
| 6.2.8 | Designing with radiated emissions in mind..... | 49 | 9 | Part identification..... | 90 |
| 6.2.9 | Capacitance attributes..... | 49 | 9.1 | Description..... | 90 |
| 6.3 | Switching electrical specifications..... | 49 | 9.2 | Format..... | 90 |
| 6.3.1 | Device clock specifications..... | 49 | 9.3 | Fields..... | 90 |
| 6.3.2 | General switching specifications..... | 50 | 9.4 | Example..... | 91 |
| 6.4 | Thermal specifications..... | 51 | 10 | Revision History..... | 91 |

1 Introduction

The KW39/38/37 wireless microcontrollers (MCU), which includes the KW39A, KW38A/Z and KW37A/Z families of devices, are highly integrated single-chip devices that enable Bluetooth Low Energy 5.0 and Generic FSK connectivity for automotive, and industrial embedded systems. To meet the stringent requirements of automotive applications, the KW39/38/37 is fully AEC Q100 Grade 2 Automotive Qualified. The target applications center on wirelessly bridging the embedded world with mobile devices to enhance the human interface experience, share embedded data between devices and the cloud and enable wireless firmware updates. Leading the automotive applications is the Digital Key, where a smartphone can be used by the owner as an alternative to the key FOB for unlocking and personalizing the driving experience. For a car sharing experience, the owner can provide selective, temporary authorization for access to the car allowing the authorized person to unlock, start, and operate the car using their mobile device using Bluetooth LE.

The KW39/38/37 Wireless MCU integrates an Arm® Cortex-M0+ CPU with up to 512 KB flash and 64 KB SRAM and a 2.4 GHz radio that supports Bluetooth LE 5.0 and Generic FSK modulations. The Bluetooth LE radio supports up to 8 simultaneous connections in any master/slave combination.

The KW38 includes an integrated FlexCAN module enabling seamless integration into a cars in-vehicle or an industrial CAN communication network, enabling communication with external control and sensor monitoring devices over Bluetooth LE. The FlexCAN module can support CAN's flexible data-rate (CAN FD) protocol for increased bandwidth and lower latency required by many automotive applications.

The KW39/38/37 devices can be used as a "BlackBox" modem to add Bluetooth LE or Generic FSK connectivity to an existing host MCU or MPU (microprocessor). The devices may also be used as a standalone smart wireless sensor with embedded application where no host controller is required.

The RF circuit of the KW39/38/37 is optimized to require very few external components, achieving the smallest RF footprint possible on a printed circuit board. Extremely long battery life is achieved through the efficiency of code execution in the Cortex-M0+ CPU core and the multiple low-power operating modes of the KW39/38/37. For power critical applications, an integrated DC-DC converter enables operation from a single coin cell or Li-ion battery with a significant reduction of peak receive and transmit current consumption.

2 Feature Descriptions

This section provides a simplified block diagram and highlights the KW39/38/37 features.

2.1 Block Diagram

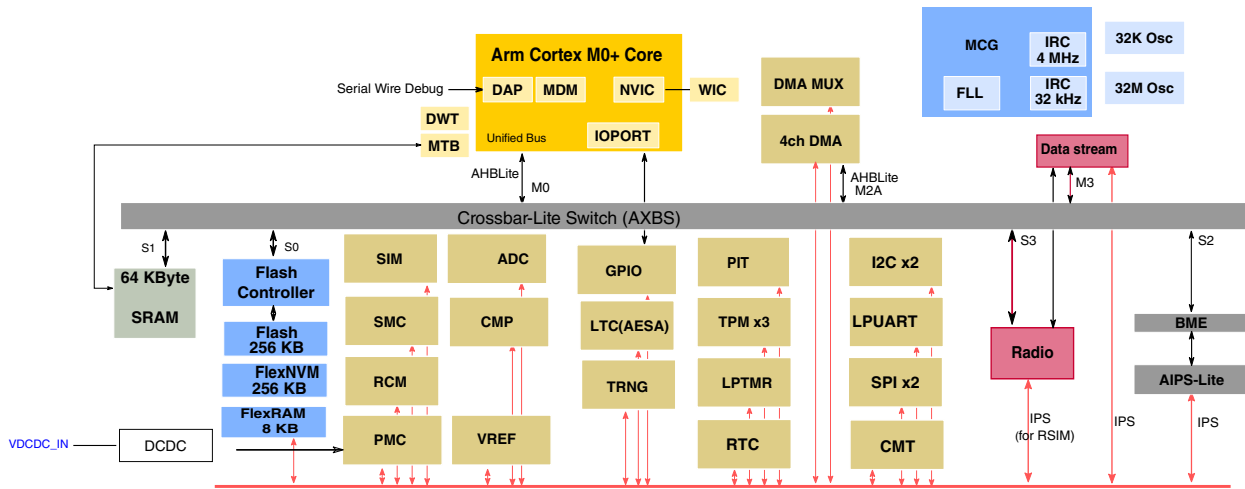


Figure 1. KW39 Detailed Block Diagram

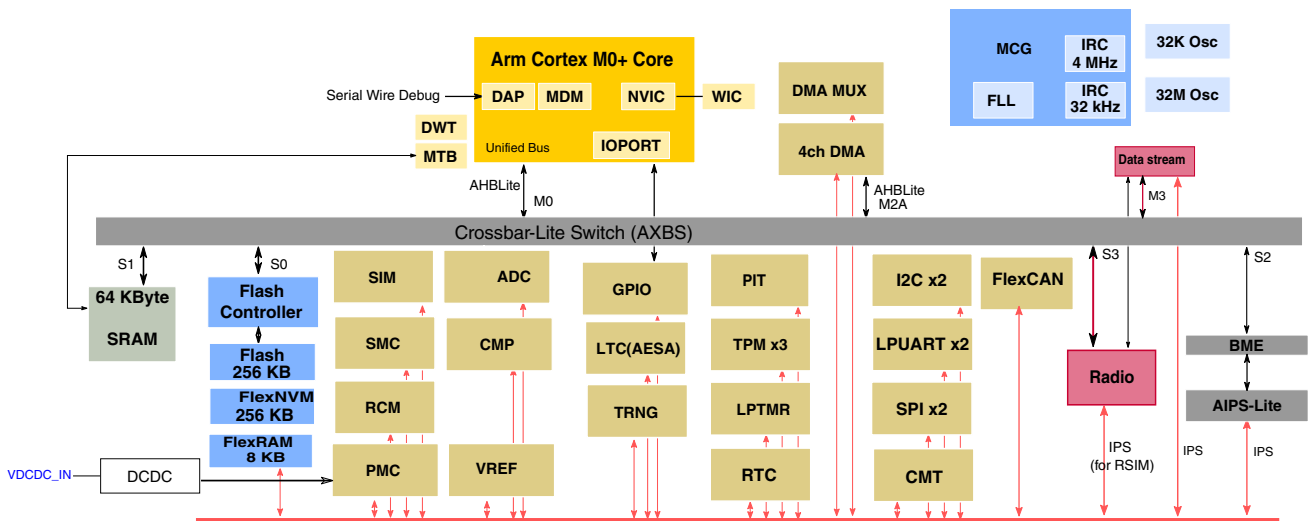


Figure 2. KW38 Detailed Block Diagram

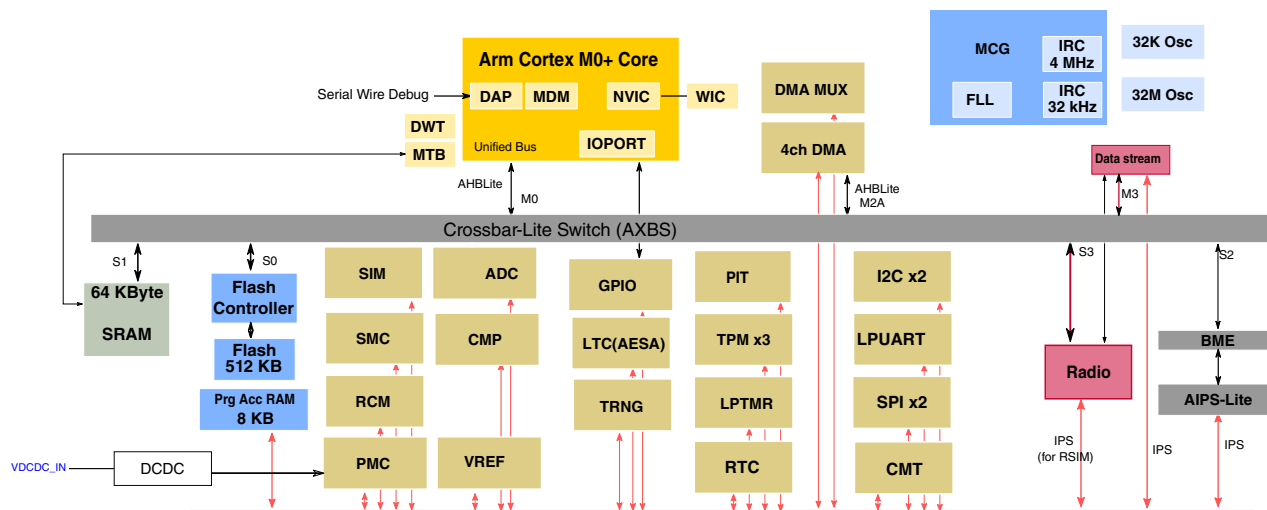


Figure 3. KW37 Detailed Block Diagram

Table 1. List of IPs in block diagrams

| Acronym | Definition |
|---------|--|
| ADC | Analog-to-Digital Converter |
| AESA | Advanced Encryption Standard Accelerator |
| AIPS | Peripheral Bridge |
| BME | Bit Manipulation Engine |
| CMP | Comparator |
| CMT | Carrier Modulator Timer |
| DAP | Debug Access Port |
| DMA | Direct Memory Access |
| DMAMUX | Direct Memory Access Multiplexer |
| DWT | Data Watchpoint and Trace |
| FLL | Frequency-Locked Loop |
| GPIO | General Purpose Input/Output |
| I2C | Inter-integrated Circuit |
| IRC | Internal Reference Clock |
| LPTMR | Low-Power Timer |
| LPUART | Low-Power UART |
| LTC | LP Trusted Cryptography |
| MCG | Multipurpose Clock Generator |
| MDM | Miscellaneous Debug Module |
| MTB | Micro Trace Buffer |
| NVIC | Nested Vectored Interrupt Controller |
| OSC | Oscillator |
| PIT | Periodic Interrupt Timer |

Table continues on the next page...

Table 1. List of IPs in block diagrams (continued)

| Acronym | Definition |
|-------------|------------------------------------|
| PMC | Power Management Control |
| PORT | Port Control and Interrupt |
| Prg Acc RAM | Flash Programming Acceleration RAM |
| RCM | Reset Control Module |
| RSIM | Radio System Integration Module |
| RTC | Real-Time Clock |
| SIM | System Integration Module |
| SMC | System Mode Controller |
| SPI | Serial Peripheral Interface |
| TRNG | True Random Number Generator |
| VREF | Voltage Reference |

2.2 Radio features

Operating frequencies:

- 2.4 GHz ISM band (2400-2483.5 MHz)
- Medical Body Area Network frequency band (MBAN) 2360-2400 MHz

Supported standards:

- Bluetooth Low Energy Version 5.0 compliant radio supporting all mandatory and optional features including:
 - Bluetooth LE 4.2 errata
 - 2 Mbit/s high-speed mode
 - Long range coded PHY (125/500 kbit/s)
 - Advertising Extensions
 - High duty cycle non-connectable advertising
 - Channel selection algorithm #2
- Support for up to 8 simultaneous Bluetooth LE hardware connections in any master, slave combination
- Bluetooth LE Application Profiles
- Generic FSK modulation supporting data rates of 250, 500, 1000 and 2000 kbit/s

Other features:

- Programmable transmit output power up to +5 dBm with greater than 30 dB power control dynamic range

- 26 MHz and 32 MHz crystals supported for Bluetooth LE and Generic FSK modes
- Up to 26 devices supported by whitelist in hardware
- Up to 8 private resolvable addresses supported in hardware
- Supports DMA capture of IQ data and phase for localization applications
- Support for distance estimation and direction finding applications
- Integrated on-chip balun
- Single ended bidirectional RF port shared by transmit and receive
- Low external component count
- Supports transceiver range extension using external PA and/or LNA

2.3 Microcontroller features

Arm Cortex-M0+ CPU

- Up to 48 MHz CPU
- As compared to Cortex-M0, the Cortex-M0+ uses an optimized 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Supports up to 32 interrupt request sources
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Micro Trace Buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory

Nested Vectored Interrupt Controller (NVIC)

- 32 vectored interrupts, 4 programmable priority levels
- Includes a single non-maskable interrupt

Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low-power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected

Debug Controller

Feature Descriptions

- Two-wire Serial Wire Debug (SWD) interface
- Hardware breakpoint unit for 2 code addresses
- Hardware watchpoint unit for 2 data items
- Micro Trace Buffer for program tracing

On-Chip Memory

- Up to 512 KB Flash
 - KW39/38 contains 256 KB program flash with ECC and 256 KB FlexNVM enabling EEPROM emulation.
 - KW37 contains 512 KB program flash with ECC.
 - Flash implemented as two equal blocks each of 256 KB block. Code can execute or read from one block while the other block is being erased or programmed on KW37 only.
 - Firmware distribution protection. Program flash can be marked execute-only on a per-sector (8 KB) basis to prevent firmware contents from being read by third parties.
- 64 KB SRAM
- KW39/38 contains 8 KB FlexRAM enabling EEPROM emulation.
- KW37 contains 8 KB program acceleration RAM.
- Security circuitry to prevent unauthorized access to RAM and flash contents through the debugger

2.4 System features

Power Management Control Unit (PMC)

- Programmable power saving modes
- Available wake-up from power saving modes via internal and external sources
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Individual peripheral clocks can be gated off to reduce current consumption
- Internal Buffered bandgap reference voltage
- Factory programmed trim for bandgap and LVD
- 1 kHz Low-power Oscillator (LPO)

DC-DC Converters

- Internal switched mode power supply supporting Buck and Bypass operating modes
- Buck operation supports external voltage sources of 2.1 V to 3.6 V
- When DC-DC is not used, the device supports an external voltage range of 1.5 V to 3.6 V (1.5 - 3.6 V on VDD_RF1, VDD_RF2, VDD_RF3 and VDD_1P5OUT_PMCIN pins. 1.71 - 3.6 V on VDD_0, VDD_1, and VDDA pins)
- An external inductor is required to support the Buck mode
- The DC-DC Converter VDD_1P8OUT current drive for external devices (MCU in RUN mode, Radio is enabled, other peripherals are disabled)
 - Up to 45 mA in buck mode with VDD_1P8OUT = 1.8 V
 - Up to 27 mA in buck mode with VDD_1P8OUT = 3.0 V

Direct Memory Access (DMA) Controller

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses and transfer size
- Support for enhanced addressing modes
- 4-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Internal data buffer, used as temporary storage to support 16- and 32-byte transfers
- Connections to the crossbar switch for bus mastering the data movement
- Transfer Control Descriptor (TCD) organized to support two-deep, nested transfer operations
- 32-byte TCD stored in local memory for each channel
- An inner data transfer loop defined by a minor byte transfer count
- An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
 - Explicit software initiation
 - Initiation via a channel-to-channel linking mechanism for continuous transfers
 - Peripheral-paced hardware requests, one per channel
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Optional error terminations per channel and logically summed together to form one error interrupt to the interrupt controller
- Optional support for scatter/gather DMA processing
- Support for complex data structures

DMA Channel Multiplexer (DMA MUX)

- 4 independently selectable DMA channel routers
- 2 periodic trigger sources available
- Each channel router can be assigned to 1 of the peripheral DMA sources

COP Watchdog Module

- Independent clock source input (independent from CPU/bus clock)
- Choice between two clock sources
 - LPO oscillator
 - Bus clock

System Clocks

- Both 26 MHz and 32 MHz crystal reference oscillator supported for Bluetooth LE and Generic FSK modes
- MCU can derive its clock either from the crystal reference oscillator or the Frequency-locked Loop (FLL)¹
- 32.768 kHz crystal reference oscillator used to maintain precise Bluetooth Low Energy timing in low-power modes
- Multipurpose Clock Generator (MCG)
- Internal reference clocks — Can be used as a clock source for other on-chip peripherals
 - On-chip RC oscillator range of 31.25 kHz to 39.0625 kHz with 3% accuracy across full temperature range
 - On-chip 4 MHz oscillator with 11% accuracy across full temperature range
- Frequency-locked Loop (FLL) controlled by internal or external reference
 - 20 MHz to 48 MHz FLL output

Unique Identifiers

- 80-bit Unique ID represents a unique identifier for each chip
- 40-bit unique Media Access Control (MAC) address, which can be used to build a unique 48-bit Bluetooth Low Energy MAC address

2.5 Peripheral features

16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with 16-bit resolution
- Output formatted in differential-ended 16-, 13-, 11-, and 9-bit mode

1. Clock options can have restrictions based on the chosen SoC configuration.

- Output formatted in single-ended 16-, 12-, 10-, and 8-bit mode
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion rates in 16-bit mode with no averaging up to ~500Ksamples/sec
- Input clock selection
- Operation in low-power modes for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Automatic compare with interrupt for less-than, or greater than, or equal to programmable value
- Temperature sensor
- Battery voltage measurement
- Hardware average function
- Selectable voltage reverence
- Self-calibration mode

High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Two performance modes:
 - Shorter propagation delay at the expense of higher power
 - Low-power, with longer propagation delay
- Operational in all MCU power modes except VLLS0 mode

Voltage Reference(VREF1)

- Programmable trim register with 0.5 mV steps, automatically loaded with factory trimmed value upon reset
- Programmable buffer mode selection:
 - Off
 - Bandgap enabled/standby (output buffer disabled)
 - High-power buffer mode (output buffer enabled)
- 1.2 V output at room temperature
- VREF_OUT output signal

Low-power Timer (LPTMR)

- One channel
- Operation as timer or pulse counter

Feature Descriptions

- Selectable clock for prescaler/glitch filter
 - 1 kHz internal LPO
 - External low-power crystal oscillator
 - Internal reference clock
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare
- Functional in all power modes

Timer/PWM (TPM)

- TPM0: 4 channels, TPM1 and TPM2: 2 channels each
- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Generation of hardware triggers
- TPM1 and TPM2: Quadrature decoder with input filters
- Global time base mode shares single time base across multiple TPM instances

Programmable Interrupt Timer (PIT)

- Up to 2 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by bus clock frequency

Real-Time Clock (RTC)

- 32-bit seconds counter with 32-bit alarm
 - Can be invalidated on detection of tamper detect
- 16-bit prescaler with compensation
- Register write protection
 - Hard Lock requires MCU POR to enable write access
 - Soft lock requires POR or software reset to enable write/read access
- Capable of waking up the system from low-power modes

Inter-Integrated Circuit (I²C)

- Two channels
- Compatible with I2C bus standard and SMBus Specification Version 2 features
- Up to 400 kHz operation

- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low-power mode

LPUART

- One channel (2 channels on KW38)
- Full-duplex operation
- Standard mark/space Non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Programmable 1 or 2 stop bits
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wake-up methods:
 - Idle line wake-up
 - Address mark wake-up
- Address match feature in receiver to reduce address mark wake-up ISR overhead
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low-power modes
- Hardware Flow Control RTS\CTS
- Functional in Stop/VLPS modes
- Break detect supporting LIN

Serial Peripheral Interface (SPI)

- Two independent SPI channels
- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate

Feature Descriptions

- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Support for both transmit and receive by DMA

Carrier Modulator Timer (CMT)

- Four modes of operation
 - Time; with independent control of high and low times
 - Baseband
 - Frequency shift key (FSK)
 - Direct software control of CMT_IRO signal
- Extended space operation in time, baseband, and FSK modes
- Selectable input clock divider
- Interrupt on end of cycle
- Ability to disable CMT_IRO signal and use as timer interrupt

General Purpose Input/Output (GPIO)

- Hysteresis and configurable pull up device on all input pins
- Independent pin value register to read logic level on digital pin
- All GPIO pins can generate IRQ and wake-up events
- Configurable drive strength on some output pins
- GPIO can be configured to function as a interrupt driven keyboard scanning matrix; in the 48-pin package there are a total of 25 digital pins

FlexCAN (for KW38 only)

- Full implementation of the CAN with Flexible Data Rate (CAN FD) protocol specification and CAN protocol specification, Version 2.0 B
- Flexible Message Buffers (MBs); there are total 32 MBs of 8 bytes data length each, configurable as Rx or Tx, all supporting standard and extended messages
- Programmable clock source to the CAN Protocol Interface, either peripheral clock or oscillator clock
- Capability to select priority between mailboxes and Rx FIFO during matching process

- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 individual masking capability
- Each individual MB forms by 16, 24, 40, or 72 bytes, depending on the quantity of data bytes allocated for the message payload: 8, 16, 32, or 64 data bytes, respectively

2.6 Security Features

Advanced Encryption Standard Accelerator(AES-128 Accelerator)

The Advanced Encryption Standard Accelerator (AESA) module is a standalone hardware coprocessor capable of accelerating the 128-bit advanced encryption standard (AES) cryptographic algorithms.

The AESA engine supports the following cryptographic features.

LTC includes the following features:

- Cryptographic authentication
 - Message Authentication Codes (MAC)
 - Cipher-based MAC (AES-CMAC)
 - Extended cipher block chaining message authentication code (AES-XCBC-MAC)
 - Auto padding
 - Integrity Check Value(ICV) checking
- Authenticated encryption algorithms
 - Counter with CBC-MAC (AES-CCM)
- Symmetric key block ciphers
 - AES (128-bit keys)
 - Cipher modes:
 - AES-128 modes
 - Electronic Codebook (ECB)
 - Cipher Block Chaining (CBC)
 - Counter (CTR)
- Secure scan

True Random Number Generator (TRNG)

True Random Number Generator (TRNG) is a hardware accelerator module that constitutes a high-quality entropy source.

Transceiver Description

- TRNG generates a 512-bit (4x 128-bit) entropy as needed by an entropy-consuming module, such as a deterministic random number generator.
- TRNG output can be read and used by a deterministic pseudo-random number generator (PRNG) implemented in software.
- TRNG-PRNG combination achieves NIST-compliant true randomness and cryptographic-strength random numbers using the TRNG output as the entropy source.
- A fully FIPS 180 compliant solution can be realized using the TRNG together with a FIPS-compliant deterministic random number generator and the SoC-level security.

Flash Memory Protection

The on-chip flash memory controller enables the following useful features:

- Program flash protection scheme prevents accidental program or erase of stored data.
- Automated, built-in, program and erase algorithms with verify.
- Read access to one program flash block is possible while programming or erasing data in the other program flash block.

3 Transceiver Description

- Direct Conversion Receiver (Zero IF)
- Constant Envelope Transmitter
- Low Transmit and Receive Current Consumption
- Low bill of material (BOM) radio

3.1 Transceiver Functions

Receive

The receiver architecture is Zero IF (ZIF) where the received signal after passing through RF front end is down-converted to a baseband signal. The signal is filtered and amplified before it is fed to analog-to-digital converter. The digital signal then decimates to a baseband clock frequency before it digitally processes, demodulates and passes on to packet processing/link-layer processing.

Transmit

The transmitter transmits GFSK/FSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine-tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is routed to a multi-stage amplifier for transmission..

3.2 Key Specifications

KW39/38/37 meets or exceeds all Bluetooth Low Energy version 5.0 performance specifications. The key specifications for the KW39/38/37 are:

Frequency Band:

- ISM Band: 2400 to 2483.5 MHz
- MBAN Band: 2360 to 2400 MHz

Full Bluetooth Low Energy version 5.0 modulation scheme:

- Symbol rate: Uncoded PHY (1, 2 Mbit/s), Coded PHY (125, 500 kbit/s)
- Modulation: GFSK BT=0.5, h=0.5
- Receiver sensitivity: –98 dBm, typical for Bluetooth LE 1 Mbit/s, –105 dBm for Bluetooth LE-LR 125 kbit/s; for all other modes, refer [Receiver Feature Summary](#).
- Programmable transmitter output power: –30 dBm to +5 dBm

Generic FSK modulation scheme:

- Symbol rate: 250, 500, 1000, and 2000 kbit/s
- Modulation(s): GFSK (modulation index = 0.32, 0.5, 0.7, and 1.0, BT = 0.5), and MSK
- Receiver Sensitivity: Mode and data rate dependent. –101 dBm typical for GFSK (r=250 kbit/s, BT = 0.5, h = 0.5)

3.3 Channel Map Frequency Plans

3.3.1 Channel Plan for Bluetooth Low Energy

This section describes the frequency plan / channels associated with 2.4 GHz ISM and MBAN bands for Bluetooth Low Energy.

2.4 GHz ISM Channel numbering:

- $F_c = 2402 + k * 2 \text{ MHz}$, $k=0, \dots, 39$.

MBAN Channel numbering:

- $F_c = 2360 + k \text{ in MHz}$, for $k=0, \dots, 39$

where k is the channel number.

Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations

| 2.4 GHz ISM ¹ | | MBAN ² | | 2.4GHz ISM + MBAN | |
|--------------------------|------------|-------------------|------------|-------------------|------------|
| Channel | Freq (MHz) | Channel | Freq (MHz) | Channel | Freq (MHz) |
| 0 | 2402 | 0 | 2360 | 28 | 2390 |
| 1 | 2404 | 1 | 2361 | 29 | 2391 |
| 2 | 2406 | 2 | 2362 | 30 | 2392 |
| 3 | 2408 | 3 | 2363 | 31 | 2393 |
| 4 | 2410 | 4 | 2364 | 32 | 2394 |
| 5 | 2412 | 5 | 2365 | 33 | 2395 |
| 6 | 2414 | 6 | 2366 | 34 | 2396 |
| 7 | 2416 | 7 | 2367 | 35 | 2397 |
| 8 | 2418 | 8 | 2368 | 36 | 2398 |
| 9 | 2420 | 9 | 2369 | 0 | 2402 |
| 10 | 2422 | 10 | 2370 | 1 | 2404 |
| 11 | 2424 | 11 | 2371 | 2 | 2406 |
| 12 | 2426 | 12 | 2372 | 3 | 2408 |
| 13 | 2428 | 13 | 2373 | 4 | 2410 |
| 14 | 2430 | 14 | 2374 | 5 | 2412 |
| 15 | 2432 | 15 | 2375 | 6 | 2414 |
| 16 | 2434 | 16 | 2376 | 7 | 2416 |
| 17 | 2436 | 17 | 2377 | 8 | 2418 |
| 18 | 2438 | 18 | 2378 | 9 | 2420 |
| 19 | 2440 | 19 | 2379 | 10 | 2422 |
| 20 | 2442 | 20 | 2380 | 11 | 2424 |
| 21 | 2444 | 21 | 2381 | 12 | 2426 |
| 22 | 2446 | 22 | 2382 | 13 | 2428 |
| 23 | 2448 | 23 | 2383 | 14 | 2430 |

Table continues on the next page...

Table 2. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)

| 2.4 GHz ISM ¹ | | MBAN ² | | 2.4GHz ISM + MBAN | |
|--------------------------|------------|-------------------|------------|-------------------|------------|
| Channel | Freq (MHz) | Channel | Freq (MHz) | Channel | Freq (MHz) |
| 24 | 2450 | 24 | 2384 | 15 | 2432 |
| 25 | 2452 | 25 | 2385 | 16 | 2434 |
| 26 | 2454 | 26 | 2386 | 17 | 2436 |
| 27 | 2456 | 27 | 2387 | 18 | 2438 |
| 28 | 2458 | 28 | 2388 | 19 | 2440 |
| 29 | 2460 | 29 | 2389 | 20 | 2442 |
| 30 | 2462 | 30 | 2390 | 21 | 2444 |
| 31 | 2464 | 31 | 2391 | 22 | 2446 |
| 32 | 2466 | 32 | 2392 | 23 | 2448 |
| 33 | 2468 | 33 | 2393 | 24 | 2450 |
| 34 | 2470 | 34 | 2394 | 25 | 2452 |
| 35 | 2472 | 35 | 2395 | 26 | 2454 |
| 36 | 2474 | 36 | 2396 | 27 | 2456 |
| 37 | 2476 | 37 | 2397 | 37 | 2476 |
| 38 | 2478 | 38 | 2398 | 38 | 2478 |
| 39 | 2480 | 39 | 2399 | 39 | 2480 |

1. ISM frequency of operation spans from 2400.0 MHz to 2483.5 MHz
2. Per FCC guideline rules, Bluetooth Low Energy single mode operation is allowed in these channels.

3.3.2 Other Channel Plans

The RF synthesizer can be configured to use any channel frequency between 2.36 and 2.487 GHz.

4 Transceiver Electrical Characteristics

4.1 Radio operating conditions

Table 3. Radio operating conditions

| Characteristic | Symbol | Min | Typ | Max | Unit |
|-----------------|----------|-------|-----|-------|------|
| Input Frequency | f_{in} | 2.360 | — | 2.480 | GHz |

Table continues on the next page...

Table 3. Radio operating conditions (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------|------------------|-----|-----|------|
| Ambient Temperature Range | T_A | -40 | 25 | 105 | °C |
| Maximum RF Input Power | P_{max} | — | — | 10 | dBm |
| Crystal Reference Oscillator Frequency 1 | f_{ref} | 26 MHz or 32 MHz | | | |

1. The recommended crystal accuracy is ± 40 ppm including initial accuracy, mechanical, temperature, and aging factors.

4.2 Receiver Feature Summary

Table 4. Top-Level Receiver Specifications (TA=25 °C, nominal process unless otherwise noted)

| Characteristic ¹ | Symbol | Min. | Typ. | Max. | Unit |
|---|-------------------|-------|-------|----------------|------|
| Receiver General Specifications | | | | | |
| Supply current power down on VDD_RFX supplies | I_{pdn} | — | 200 | 1000 | nA |
| Supply current Rx On with DC-DC converter enable (Buck; $V_{DCDC_IN} = 3.6$ V) · ² | I_{Rxon} | — | 6.36 | — | mA |
| Supply current Rx On with DC-DC converter disabled (Bypass) ² | I_{Rxon} | — | 17.78 | — | mA |
| Input RF Frequency | f_{in} | 2.360 | — | 2.4835 | GHz |
| GFSK Rx Sensitivity(250 kbit/s GFSK-BT=0.5, h=0.5) | $SENS_{GFSK}$ | — | -101 | — | dBm |
| Max Rx RF Input Signal Level | $RF_{in,max}$ | — | — | 10 | dBm |
| Noise Figure for maximum gain mode @ typical sensitivity | NF_{HG} | — | 7.5 | — | dB |
| Receiver Signal Strength Indicator Range ³ | $RSSI_{Range}$ | -100 | — | 5 ⁴ | dBm |
| Receiver Signal Strength Indicator Resolution | $RSSI_{Res}$ | — | 1 | — | dB |
| Typical RSSI variation over frequency | | -2 | — | 2 | dB |
| Typical RSSI variation over temperature | | -2 | — | 2 | dB |
| Narrowband RSSI accuracy ⁵ | $RSSI_{Acc}$ | -3 | — | 3 | dB |
| Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency f_c and spurious power measured in 1 MHz at RF frequency f), where $ f-f_c < 1.6$ MHz | — | — | -54 | — | dBc |
| Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency f_c and spurious power measured in 1 MHz at RF frequency f), where $ f-f_c > 2.5$ MHz ⁶ | — | — | -70 | — | dBc |
| Bluetooth LE coded 125 kbit/s (Long Range, 8x Spreading) | | | | | |
| Bluetooth LE LR 125 kbit/s Sensitivity ⁷ | $SENS_{BLELR125}$ | — | -105 | — | dBm |

Table continues on the next page...

Table 4. Top-Level Receiver Specifications (TA=25 °C, nominal process unless otherwise noted) (continued)

| Characteristic ¹ | Symbol | Min. | Typ. | Max. | Unit |
|--|---------------------------------|------|------|------|------|
| Bluetooth LE LR 125 kbit/s Co-channel Interference (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz). | COSEL _{BLELR125} | | -2 | | dB |
| <i>Adjacent/Alternate Channel Performance⁸</i> | | | | | |
| Bluetooth LE LR 125 kbit/s Adjacent +/-1 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLELR125, 1 MHz} | — | 10 | — | dB |
| Bluetooth LE LR 125 kbit/s Adjacent +/-2 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLELR125, 2 MHz} | — | 50 | — | dB |
| Bluetooth LE LR 125 kbit/s Alternate +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLELR125, 3 MHz} | — | 55 | — | dB |
| Bluetooth LE LR 125 kbit/s Alternate > +/-5 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLELR125, 5+ MHz} | — | 60 | — | dB |
| Bluetooth LE coded 500 kbit/s (Long Range, 2x Spreading) | | | | | |
| Bluetooth LE LR 500 kbit/s Sensitivity ⁷ | SENS _{BLELR500} | — | -101 | — | dBm |
| Bluetooth LE LR 500 kbit/s Co-channel Interference (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz). | COSEL _{BLELR500} | | -4 | | dB |
| <i>Adjacent/Alternate Channel Performance⁸</i> | | | | | |
| Bluetooth LE LR 500 kbit/s Adjacent +/-1 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLELR500, 1 MHz} | — | 9 | — | dB |
| Bluetooth LE LR 500 kbit/s Adjacent +/-2 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLELR500, 2 MHz} | — | 50 | — | dB |
| Bluetooth LE LR 500 kbit/s Alternate +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLELR500, 3 MHz} | — | 55 | — | dB |
| Bluetooth LE LR 500 kbit/s Alternate > +/-5 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLELR500, 5+ MHz} | — | 60 | — | dB |
| Bluetooth LE uncoded 1 Mbit/s | | | | | |
| Bluetooth LE 1 Mbit/s Sensitivity ⁷ | SENS _{BLE1M} | — | -98 | — | dBm |
| Bluetooth LE 1 Mbit/s Co-channel Interference (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz). | COSEL _{BLE1M} | | -7 | | dB |
| <i>Adjacent/Alternate Channel Selectivity Performance⁸</i> | | | | | |
| Bluetooth LE 1 Mbit/s Selectivity +/-1 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLE1M, 1 MHz} | — | 0 | — | dB |

Table continues on the next page...

Table 4. Top-Level Receiver Specifications (TA=25 °C, nominal process unless otherwise noted) (continued)

| Characteristic ¹ | Symbol | Min. | Typ. | Max. | Unit |
|---|------------------------------|------|-------|------|------|
| Bluetooth LE 1 Mbit/s Adjacent +/-2 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLE1M, 2 MHz} | — | 42 | — | dB |
| Bluetooth LE 1 Mbit/s Selectivity +/-3 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLE1M, 3 MHz} | — | 50 | — | dB |
| Bluetooth LE 1 Mbit/s Alternate ≥ +/-5 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.) | SEL _{BLE1M, 5+ MHz} | — | 55 | — | dB |
| <i>Intermodulation Performance</i> | | | | | |
| Bluetooth LE 1 Mbit/s Intermodulation with continuous wave interferer at ± 3 MHz and modulated interferer is at ± 6 MHz (Wanted signal at -67 dBm, BER<0.1%.) | IM3-6 _{BLE1M} | — | -42 | — | dBm |
| Bluetooth LE 1 Mbit/s Intermodulation with continuous wave interferer at ±5 MHz and modulated interferer is at ±10 MHz (Wanted signal at -67 dBm, BER<0.1%.) | IM5-10 _{BLE1M} | — | -23 | — | dBm |
| <i>Blocking Performance</i> | | | | | |
| Bluetooth LE 1 Mbit/s Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at -67 dBm, BER<0.1%. Interferer continuous wave signal.) ^{9, 10} | — | — | 3 | — | dBm |
| Bluetooth LE 1 Mbit/s Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000 MHz (Wanted signal at -67 dBm, BER<0.1%. Interferer continuous wave signal.) | — | — | 3 | — | dBm |
| Bluetooth LE 1 Mbit/s Out of band blocking from 2001 MHz to 2339 MHz and 2484 MHz to 2999 MHz (Wanted signal at -67 dBm, BER<0.1%. Interferer continuous wave signal.) ¹⁰ | — | — | -12 | — | dBm |
| Bluetooth LE 1 Mbit/s Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at -67 dBm, BER<0.1%. Interferer continuous wave signal.) ¹⁰ | — | — | 5 | — | dBm |
| Bluetooth LE uncoded 2 Mbit/s (High Speed) | | | | | |
| Bluetooth LE 2 Mbit/s Sensitivity ⁷ | SENS _{BLE2M} | — | -95.5 | — | dBm |
| Bluetooth LE 2 Mbit/s Co-channel Interference (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 2 MHz). | COSEL _{BLE2M} | — | -7 | — | dB |
| <i>Adjacent/Alternate Channel Performance⁸</i> | | | | | |
| Bluetooth LE 2 Mbit/s Adjacent +/-2 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 2 MHz.) | SEL _{BLE2M, 2 MHz} | — | 3 | — | dB |
| Bluetooth LE 2 Mbit/s Alternate +/-4 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 2 MHz.) | SEL _{BLE2M, 4 MHz} | — | 42 | — | dB |

Table continues on the next page...

Table 4. Top-Level Receiver Specifications (TA=25 °C, nominal process unless otherwise noted) (continued)

| Characteristic ¹ | Symbol | Min. | Typ. | Max. | Unit |
|---|-------------------------------|------|------|------|------|
| Bluetooth LE 2 Mbit/s Selectivity +/-6 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 2 MHz.) | SEL _{BLE2M, 6 MHz} | — | 50 | — | dB |
| Bluetooth LE 2 Mbit/s Selectivity ≥ +/-10 MHz Interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 2 MHz.) | SEL _{BLE2M, 10+ MHz} | — | 55 | — | dB |
| <i>Intermodulation Performance</i> | | | | | |
| Bluetooth LE 2 Mbit/s Intermodulation with continuous wave interferer at ± 6 MHz and modulated interferer is at ± 12 MHz (Wanted signal at -67 dBm, BER<0.1%.) | IM6-12 _{BLE2M} | — | -23 | — | dBm |
| Bluetooth LE 2 Mbit/s Intermodulation with continuous wave interferer at ±10 MHz and modulated interferer is at ±20 MHz (Wanted signal at -67 dBm, BER<0.1%.) | IM10-20 _{BLE2M} | — | -24 | — | dBm |
| <i>Blocking Performance</i> | | | | | |
| Bluetooth LE 2 Mbit/s Out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at -67 dBm, BER<0.1%. Interferer continuous wave signal.) ^{9, 10} | — | — | 3 | — | dBm |
| Bluetooth LE 2 Mbit/s Out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000 MHz (Wanted signal at -67 dBm, BER<0.1%. Interferer continuous wave signal.) | — | — | -6 | — | dBm |
| Bluetooth LE 2 Mbit/s Out of band blocking from 2001 MHz to 2339 MHz and 2484 MHz to 2999 MHz (Wanted signal at -67 dBm, BER<0.1%. Interferer continuous wave signal.) ¹⁰ | — | — | -12 | — | dBm |
| Bluetooth LE 2 Mbit/s Out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at -67 dBm, BER<0.1%. Interferer continuous wave signal.) ¹⁰ | — | — | 5 | — | dBm |

1. All the Rx parameters are measured at the KW39/38/37 RF pins.
2. Transceiver power consumption.
3. Narrow-band RSSI mode.
4. With RSSI_CTRL_0.RSSI_ADJ field calibrated to account for antenna to RF input losses.
5. With one point calibration over frequency and temperature.
6. Exceptions allowed for twice the reference clock frequency(fref) multiples.
7. Measured at 0.1% BER using 37 byte long packets in maximum gain mode and nominal conditions.
8. Bluetooth LE adjacent and alternate selectivity performance is measured with modulated interference signals.
9. Exceptions allowed for carrier frequency sub harmonics.
10. Exceptions allowed for carrier frequency harmonics.

Table 5. Receiver Specifications with Generic FSK Modulations

| Modulation type | Data rate (kb/s) | Channel BW (kHz) | Typical sensitivity (dBm) | Adjacent/Alternate channel selectivity (dB) ¹ | | | | | Co-channel |
|-------------------------|------------------|------------------|---------------------------|--|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|------------|
| | | | | Desired signal level (dBm) | Interferer at ±1* channel BW offset | Interferer at ±2* channel BW offset | Interferer at ±3* channel BW offset | Interferer at ±4* channel BW offset | |
| GFSK BT = 0.5, h = 0.32 | 2000 | 2000 | -90.5 | -67 | 39 | 48 | 52 | 54 | -9 |
| | 1000 | 1000 | -93.5 | -67 | 36 | 47 | 50 | 53 | -8 |
| GFSK BT = 0.5, h = 0.5 | 2000 | 4000 | -94 | -67 | 46 | 56 | 59 | 60 | -7 |
| | 1000 | 2000 | -97 | -67 | 44 | 56 | 59 | 60 | -7 |
| | 500 | 1000 | -98.5 | -85 | 43 | 49 | 56 | 57 | -6 |
| | 250 | 500 | -100 | -85 | 39 | 43 | 46 | 50 | -6 |
| GFSK, BT = 0.5, h = 0.7 | 2000 | 4000 | -95 | -85 | 44 | 53 | 56 | 59 | -6 |
| | 1000 | 2000 | -97.5 | -85 | 47 | 55 | 59 | 61 | -5 |
| GFSK, BT = 0.5, h = 1.0 | 1000 | 1600 | -96 | -85 | 50 | 58 | 61 | 64 | -4 |

1. Selectivity measured with an unmodulated blocker.

4.3 Transmit and PLL Feature Summary

- Supports constant envelope modulation of 2.4 GHz ISM and 2.36 GHz MBAN frequency bands
- Fast PLL Lock time: < 25 μs
- Reference Frequency:
 - 26 MHz and 32 MHz crystals supported for Bluetooth LE and Generic FSK modes

Table 6. Top-Level Transmitter Specifications (TA=25 °C, nominal process unless otherwise noted)

| Characteristic ¹ | Symbol | Min. | Typ. | Max. | Unit |
|--|------------------------|------|------|------|------|
| Transmitter General Specifications | | | | | |
| Supply current power down on VDD_RFX supplies | I _{pdn} | — | 200 | — | nA |
| Supply current Tx On with P _{RF} = 0 dBm and DC-DC converter enabled (Buck; VDD _{DCDC_in} = 3.6 V) ² | I _{TX0dBm} | — | 5.7 | — | mA |
| Supply current Tx On with P _{RF} = 0 dBm and DC-DC converter disabled (Bypass) ² | I _{TX0dBmb} | — | 16 | — | mA |
| Supply current Tx On with P _{RF} = +3.5 dBm and DC-DC converter enabled (Buck; VDD _{DCDC_in} = 3.6 V) ² | I _{TX3.5dBm} | — | 6.9 | — | mA |
| Supply current Tx On with P _{RF} = +3.5 dBm and DC-DC converter disabled (Bypass) ² | I _{TX3.5dBmb} | — | 19 | — | mA |

Table continues on the next page...

Table 6. Top-Level Transmitter Specifications (TA=25 °C, nominal process unless otherwise noted) (continued)

| Characteristic ¹ | Symbol | Min. | Typ. | Max. | Unit |
|---|---------------------------|-------|------|--------|---------|
| Supply current Tx On with P _{RF} = +5 dBm and DC-DC converter enabled (Buck; VDD _{DCDC_in} = 3.6 V, LDO-HF bumped) ² | I _{TX5dBm} | — | 8.0 | — | mA |
| Supply current Tx On with P _{RF} = +5 dBm and DC-DC converter disabled (Bypass, LDO-HF bumped) ² | I _{TX5dBmb} | — | 21 | — | mA |
| Output RF Frequency | f _{RFout} | 2.360 | — | 2.4835 | GHz |
| Maximum RF Output Power; LDO-HF bumped ³ | P _{RF,maxV} | — | +5 | — | dBm |
| Maximum RF Output power, nominal power supply ⁴ | P _{RF,maxn} | — | +3.5 | — | dBm |
| Minimum RF Output power, nominal power supply ⁴ | P _{RF,minn} | — | -30 | — | dBm |
| RF Output power control range | P _{RF,CR} | — | 35 | — | dB |
| Bluetooth LE Maximum Deviation of the Center Frequency ⁵ | F _{cdev,BLE} | — | ±3 | — | kHz |
| Bluetooth LE Frequency Hopping Support | | | YES | | |
| Second Harmonic of Transmit Carrier Frequency (P _{out} = P _{RF,max}) ⁶ | TXH2 | — | -46 | — | dBm/MHz |
| Third Harmonic of Transmit Carrier Frequency (P _{out} = P _{RF,max}) ⁶ | TXH3 | — | -50 | — | dBm/MHz |
| Bluetooth LE uncoded 1 Mbit/s / coded 125 kbit/s / coded 500 kbit/s | | | | | |
| Bluetooth LE 1 Mbit/s Tx Output Spectrum 20dB BW | TXBW _{BLE1M} | 1.0 | | — | MHz |
| Bluetooth LE 1 Mbit/s average frequency deviation using a 00001111 modulation sequence | Δf _{1,avg,BLE1M} | | 250 | | kHz |
| Bluetooth LE 1 Mbit/s average frequency deviation using a 01010101 modulation sequence | Δf _{2,avg,BLE1M} | | 220 | | kHz |
| Bluetooth LE 1 Mbit/s RMS FSK Error | FSK _{err,BLE1M} | | 3% | | |
| Bluetooth LE 1 Mbit/s Adjacent Channel Transmit Power at 2 MHz offset ⁷ | P _{RF2MHz,BLE1M} | — | — | -53 | dBm |
| Bluetooth LE 1 Mbit/s Adjacent Channel Transmit Power at ≥ 3 MHz offset ⁷ | P _{RF3MHz,BLE1M} | — | — | -59 | dBm |
| Bluetooth LE uncoded 2 Mbit/s | | | | | |
| Bluetooth LE 2 Mbit/s Tx Output Spectrum 20dB BW | TXBW _{BLE2M} | 2.2 | | — | MHz |
| Bluetooth LE 2 Mbit/s average frequency deviation using a 00001111 modulation sequence | Δf _{1,avg,BLE2M} | | 500 | | kHz |
| Bluetooth LE 2 Mbit/s average frequency deviation using a 01010101 modulation sequence | Δf _{2,avg,BLE2M} | | 420 | | kHz |
| Bluetooth LE RMS FSK Error | FSK _{err,BLE2M} | | 4% | | |
| Bluetooth LE 2 Mbit/s Adjacent Channel Transmit Power at 4 MHz offset ⁷ | P _{RF2MHz,BLE2M} | — | — | -57 | dBm |
| Bluetooth LE 2 Mbit/s Adjacent Channel Transmit Power at ≥ 6 MHz offset ⁷ | P _{RF3MHz,BLE2M} | — | — | -60 | dBm |

1. All the Tx parameters are measured at test hardware SMA connector.
2. Transceiver power consumption.

Transceiver Electrical Characteristics

3. Measured at KW39/38/37 RF pins, with Vdd_RFX over 1.44 V and assuming an average Tx duty cycle <=24%. For Tx output over +3.5 dBm, powered Vdd_RFX has to be higher than 1.44 V.
4. Measured at the KW39/38/37 RF pins.
5. Maximum drift of carrier frequency of the PLL during a Bluetooth LE packet with a nominal 32 MHz reference crystal.
6. Harmonic levels based on recommended 2 component match. Transmit harmonic levels depend on the quality of matching components. Additional harmonic margin using a third matching component (1x shunt capacitor) is possible.
7. Measured at P_{out} = +5 dBm and recommended Tx match.

Transmit PA driver output as a function of the PA_POWER[5:0] field when measured at the IC pins is as follows:

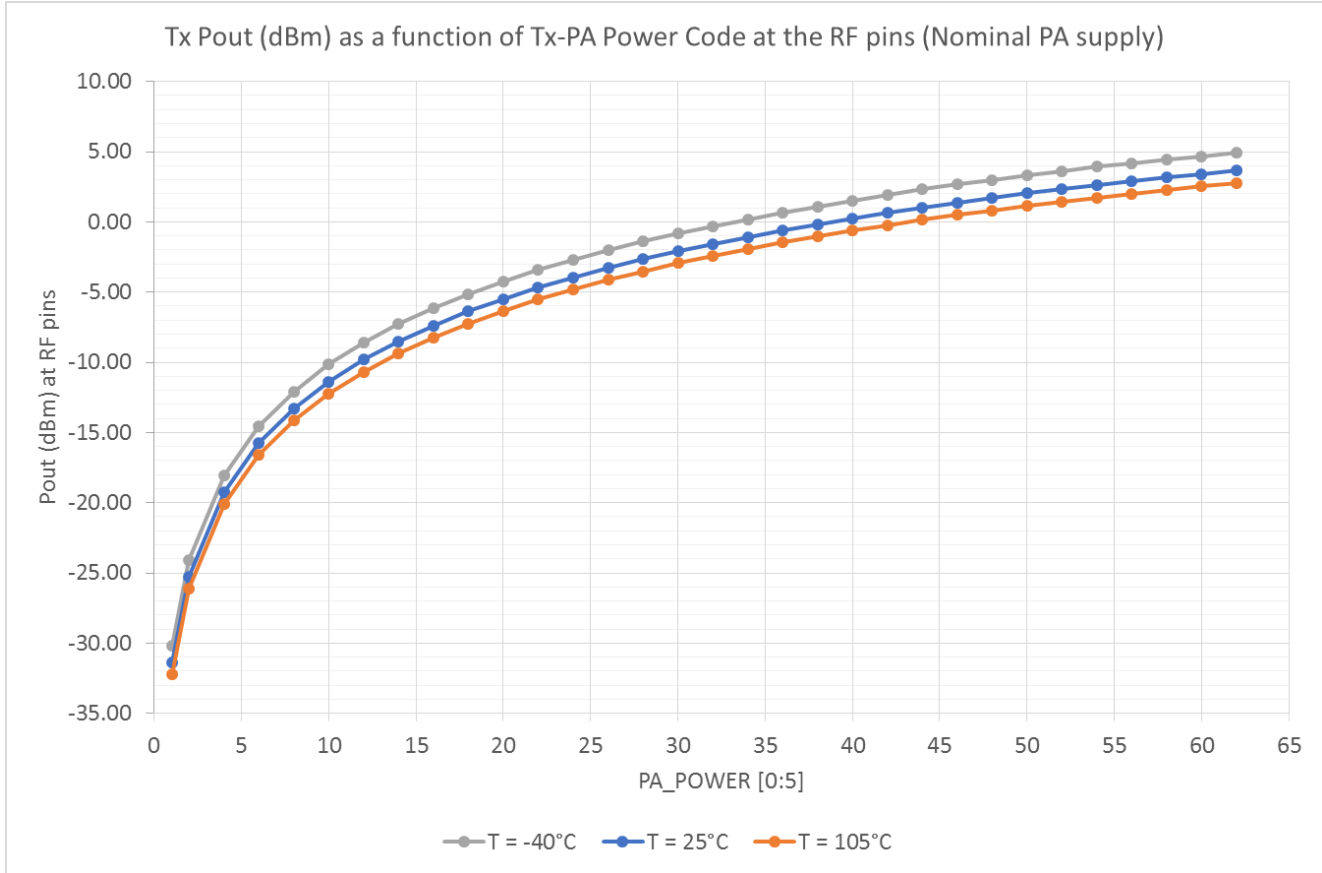


Figure 4. TX Pout (dBm) as function TX-PA Power Code at RF pins

Table 7. Transmit Output Power as a function of PA_POWER[5:0]

| PA_POWER[5:0] | TX Pout (dBm) ¹ | | |
|---------------|----------------------------|-----------|------------|
| | T = -40 °C | T = 25 °C | T = 105 °C |
| 1 | -30.15 | -31.38 | -32.25 |
| 2 | -24.05 | -25.25 | -26.09 |
| 4 | -18.06 | -19.26 | -20.11 |
| 6 | -14.56 | -15.76 | -16.61 |
| 8 | -12.08 | -13.29 | -14.15 |

Table continues on the next page...

Table 7. Transmit Output Power as a function of PA_POWER[5:0] (continued)

| PA_POWER[5:0] | TX Pout (dBm) ¹ | | |
|---------------|----------------------------|-----------|------------|
| | T = -40 °C | T = 25 °C | T = 105 °C |
| 10 | -10.16 | -11.39 | -12.24 |
| 12 | -8.59 | -9.82 | -10.67 |
| 14 | -7.27 | -8.50 | -9.36 |
| 16 | -6.16 | -7.39 | -8.24 |
| 18 | -5.15 | -6.38 | -7.24 |
| 20 | -4.25 | -5.48 | -6.34 |
| 22 | -3.44 | -4.67 | -5.53 |
| 24 | -2.70 | -3.94 | -4.81 |
| 26 | -2.02 | -3.26 | -4.14 |
| 28 | -1.39 | -2.64 | -3.52 |
| 30 | -0.81 | -2.06 | -2.95 |
| 32 | -0.34 | -1.58 | -2.45 |
| 34 | 0.18 | -1.07 | -1.95 |
| 36 | 0.66 | -0.59 | -1.48 |
| 38 | 1.10 | -0.15 | -1.04 |
| 40 | 1.52 | 0.27 | -0.64 |
| 42 | 1.92 | 0.65 | -0.24 |
| 44 | 2.30 | 1.03 | 0.14 |
| 46 | 2.67 | 1.39 | 0.49 |
| 48 | 2.99 | 1.71 | 0.80 |
| 50 | 3.32 | 2.04 | 1.14 |
| 52 | 3.63 | 2.35 | 1.44 |
| 54 | 3.92 | 2.64 | 1.74 |
| 56 | 4.19 | 2.91 | 2.00 |
| 58 | 4.44 | 3.17 | 2.27 |
| 60 | 4.68 | 3.41 | 2.51 |
| 62 | 4.90 | 3.64 | 2.74 |

1. Tx continuous wave power output at the RF pins with the recommended matching components mounted on PCB.

Transceiver Electrical Characteristics

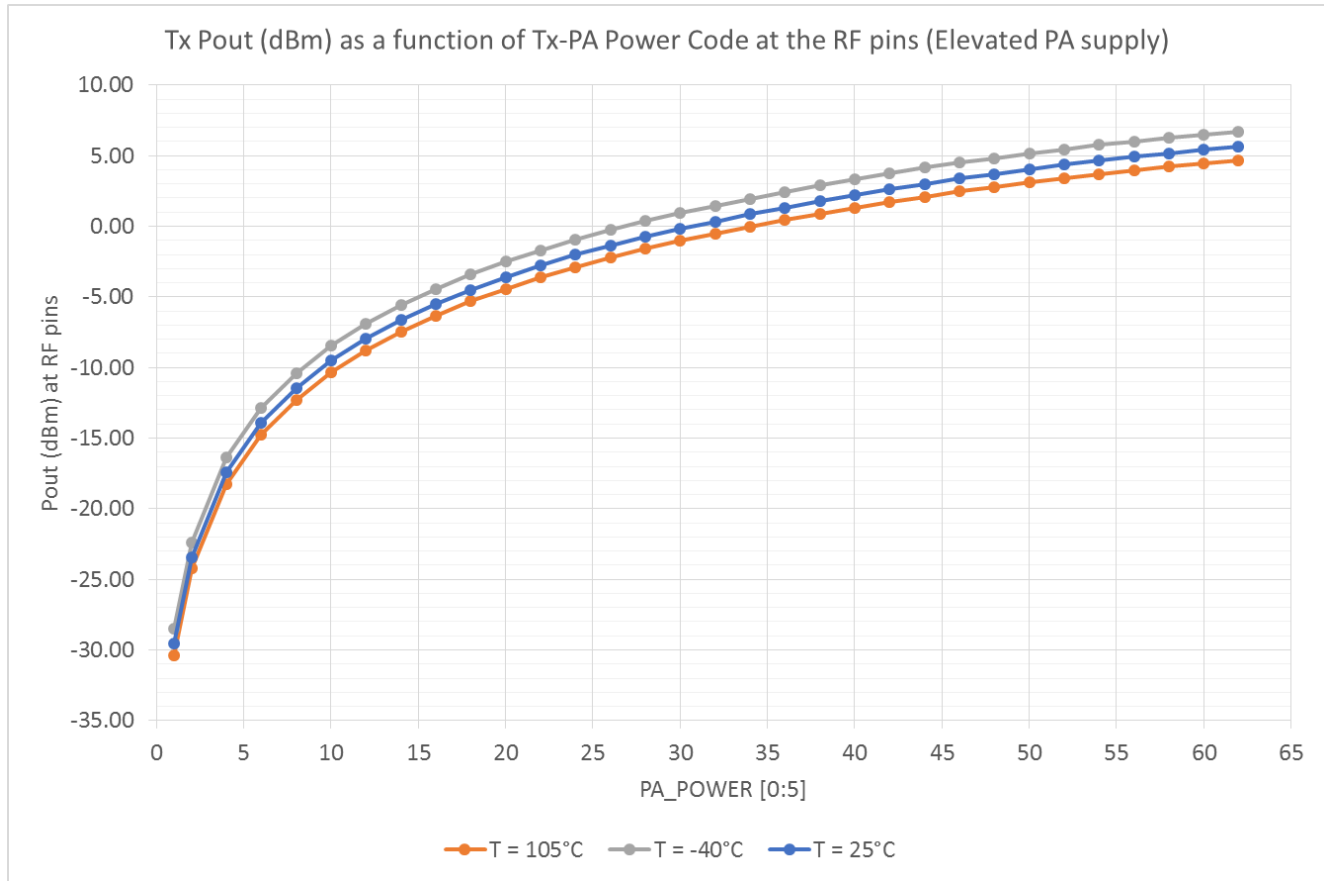


Figure 5. TX Pout (dBm) as function TX-PA Power Code at RF pins (LDO-HF bumped)

Table 8. Transmit Output Power as a function of PA_POWER[5:0] at elevated PA supply

| PA_POWER[5:0] | TX Pout (dBm) ¹ | | |
|---------------|----------------------------|-----------|------------|
| | T = -40 °C | T = 25 °C | T = 105 °C |
| 1 | -28.48 | -29.55 | -30.38 |
| 2 | -22.37 | -23.43 | -24.23 |
| 4 | -16.39 | -17.45 | -18.26 |
| 6 | -12.88 | -13.94 | -14.75 |
| 8 | -10.38 | -11.45 | -12.27 |
| 10 | -8.46 | -9.53 | -10.36 |
| 12 | -6.89 | -7.96 | -8.79 |
| 14 | -5.56 | -6.63 | -7.47 |
| 16 | -4.43 | -5.50 | -6.34 |
| 18 | -3.41 | -4.49 | -5.33 |
| 20 | -2.51 | -3.59 | -4.43 |
| 22 | -1.69 | -2.77 | -3.62 |
| 24 | -0.94 | -2.03 | -2.89 |

Table continues on the next page...

Table 8. Transmit Output Power as a function of PA_POWER[5:0] at elevated PA supply (continued)

| PA_POWER[5:0] | TX Pout (dBm) ¹ | | |
|---------------|----------------------------|-----------|------------|
| | T = -40 °C | T = 25 °C | T = 105 °C |
| 26 | -0.26 | -1.35 | -2.22 |
| 28 | 0.36 | -0.72 | -1.60 |
| 30 | 0.96 | -0.14 | -1.03 |
| 32 | 1.44 | 0.34 | -0.54 |
| 34 | 1.95 | 0.85 | -0.04 |
| 36 | 2.42 | 1.32 | 0.44 |
| 38 | 2.88 | 1.77 | 0.88 |
| 40 | 3.32 | 2.20 | 1.31 |
| 42 | 3.74 | 2.62 | 1.71 |
| 44 | 4.14 | 3.01 | 2.09 |
| 46 | 4.50 | 3.38 | 2.45 |
| 48 | 4.83 | 3.71 | 2.78 |
| 50 | 5.16 | 4.04 | 3.11 |
| 52 | 5.46 | 4.35 | 3.41 |
| 54 | 5.75 | 4.64 | 3.70 |
| 56 | 6.02 | 4.91 | 3.96 |
| 58 | 6.26 | 5.16 | 4.22 |
| 60 | 6.49 | 5.40 | 4.45 |
| 62 | 6.71 | 5.62 | 4.67 |

1. Tx continuous wave power output at the RF pins with the recommended matching components mounted on PCB.

5 System and Power Management

5.1 Power Management

The KW39/38/37 includes internal power management features that can be used to control the power usage. The power management of the KW39/38/37 includes Power Management Controller (PMC) and a DC-DC converter which can operate in a buck or bypass configuration. The PMC is designed such that the RF radio remains in state-retention while the core is in various stop modes. It makes sure that the device can stay in low current consumption mode while the RF radio can wake-up quick enough for communication.

5.1.1 DC-DC Converter

The features of the DC-DC converter include the following:

- Single inductor, multiple outputs.
- Buck mode (pin selectable; CFG=VDCDC_IN).
- Continuous or pulsed operation (hardware/software configurable).
- Power switch input to allow external control of power up, and to select DC-DC bypass mode in which all the SoC power supplies (see [Table 4](#)) are externally provided.
- Output signal to indicate power stable. Purpose is for the rest of the chip to be used as a POR.
- Scaled battery output voltage suitable for SAR ADC utilization.
- Internal oscillator for support when the reference oscillator is not present.

5.2 Modes of Operation

The Arm Cortex-M0+ core in the KW39/38/37 has three primary modes of operation: Run, Wait, and Stop modes. For each run mode, there is a corresponding wait and stop mode. Wait modes are similar to Arm sleep modes. Stop modes are similar to Arm deep sleep modes. The very low-power run (VLPR) operation mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The WFI instruction invokes both wait and stop modes. The primary modes are augmented in a number of ways to provide lower power based on application needs.

5.2.1 Power modes

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, various stop modes are available that provide state retention, partial power down, or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode, there is a corresponding wait and stop mode. Wait modes are similar to Arm sleep modes. Stop modes (VLPS, STOP) are similar to Arm sleep deep mode. The very-low-power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait, and stop. The WFI instruction invokes either wait or stop depending on the SLEEPDEEP bit in Cortex-M0+ System Control Register. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 9. Power modes (At 25 deg C)

| Power mode | Description | CPU recovery method | Radio |
|--|--|---------------------|---|
| Normal Run (all peripherals clock off) | Allows maximum performance of chip. | — | Radio can be active |
| Normal Wait - via WFI | Allows peripherals to function, while allowing CPU to go to sleep reducing power. | Interrupt | |
| Normal Stop - via WFI | Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. | Interrupt | |
| PStop2 (Partial Stop 2) | Core and system clocks are gated. Bus clock remains active. Masters and slaves clocked by bus clock remain in Run or VLPRun mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode. | Interrupt | |
| PStop1 (Partial Stop 1) | Core, system clocks, and bus clock are gated. All bus masters and slaves enter Stop mode. The clock generators in MCG and the on-chip regulator in the PMC also remain in Run or VLPRun mode. | Interrupt | |
| VLPR (Very Low-power Run) (all peripherals off) | Reduced frequency (1 MHz) Flash access mode, regulator in low-power mode, LVD off. Internal oscillator can provide low-power 4 MHz source for core. (Values @2 MHz core/ 1 MHz bus and flash, module off, execution from flash). Biasing is disabled when DC-DC is configured for continuous mode in VLPR/W | — | Radio operation is possible only when DC-DC is configured for continuous mode. ¹ However, there may be insufficient MIPS with a 4 MHz MCU to support much in the way of radio operation. |
| VLPW (Very Low-power Wait) - via WFI (all peripherals off) | Similar to VLPR, with CPU in sleep to further reduce power. (Values @4 MHz core/ 1 MHz bus, module off) Biasing is disabled when DC-DC is configured for continuous mode in VLPR/W | Interrupt | |
| VLPS (Very Low-power Stop) via WFI | Places MCU in static state with LVD operation off. Lowest power mode with ADC and all pin interrupts functional. LPTMR, RTC, CMP can be operational. | Interrupt | |

Table continues on the next page...

Table 9. Power modes (At 25 deg C) (continued)

| Power mode | Description | CPU recovery method | Radio |
|--|---|---------------------|--|
| | Biasing is disabled when DC-DC is configured for continuous mode in VLPS. | | |
| LLS3 (Low Leakage Stop) | State retention power mode. LLWU, LPTMR, RTC, CMP can be operational. All of the radio Sea of Gates(SOG) logic is in state retention. | Wake-up Interrupt | Radio SOG is in state retention in LLSx. The Bluetooth LE/Generic FSK DSM ² logic can be active using the 32 kHz clock |
| LLS2 (Low Leakage Stop) | State retention power mode. LLWU, LPTMR, RTC, CMP can be operational. 16 KB or 32 KB of programmable RAM can be powered on. All of the radio SOG logic is in state retention. | Wake-up Interrupt | |
| VLLS3 (Very Low Leakage Stop3) | Full SRAM retention. LLWU, LPTMR, RTC, CMP can be operational. Radio SoG logic is power gated and Radio Tx/Rx RAM keeps state retention. | Wake-up Reset | Radio SoG is power gated in VLLS3/2. Radio Tx/Rx RAM keeps state retention in VLLS3 and can be configurable power gated in VLLS2. The Bluetooth LE/Generic FSK DSM logic can be active using the 32 KHz clock. |
| VLLS2 (Very Low Leakage Stop2) | Partial SRAM retention. 16 KB or 32 KB of programmable RAM can be powered on. LLWU, LPTMR, RTC, CMP can be operational. All of the Radio SoG logic is power gated. Radio Tx/Rx SRAM can be configurable power gated. | Wake-up Reset | |
| VLLS1 (Very Low Leakage Stop1) with RTC + 32 kHz OSC | All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP can be operational. Radio logic is power gated. | Wake-up Reset | Radio operation not supported. The Radio SOG is power-gated in VLLS1. Radio state is lost at VLLS1 and lower power states. |
| VLLS1 (Very Low Leakage Stop1) with LPTMR + LPO | All SRAM powered off. The 32-byte system register file remains powered for customer-critical data. LLWU, LPTMR, RTC, CMP can be operational. | Wake-up Reset | |
| VLLS0 (Very Low Leakage Stop0) with Brown-out Detection | VLLS0 is not supported with DC-DC. The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection enabled, Pin interrupt only. Radio logic is power gated. | Wake-up Reset | Radio operation not supported. The Radio digital is power-gated in VLLS0. |
| VLLS0 (Very Low Leakage Stop0) without Brown-out Detection | VLLS0 is not supported with DC-DC buck configuration but is supported with bypass configuration. The 32-byte system register file remains powered for customer-critical data. Disable all analog modules in PMC and retains I/O state and DGO state. LPO disabled, POR brown-out detection disabled, Pin interrupt only. Radio logic is power gated. | Wake-up Reset | |

1. Biasing is disabled, but the Flash is in a low-power mode for VLPx, so this configuration can realize some power savings over use of Run/Wait/Stop.
2. DSM refers to Radio's deep sleep mode. DSM does not refer to the Arm sleep deep mode.

6 KW39/38/37 Electrical Characteristics

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

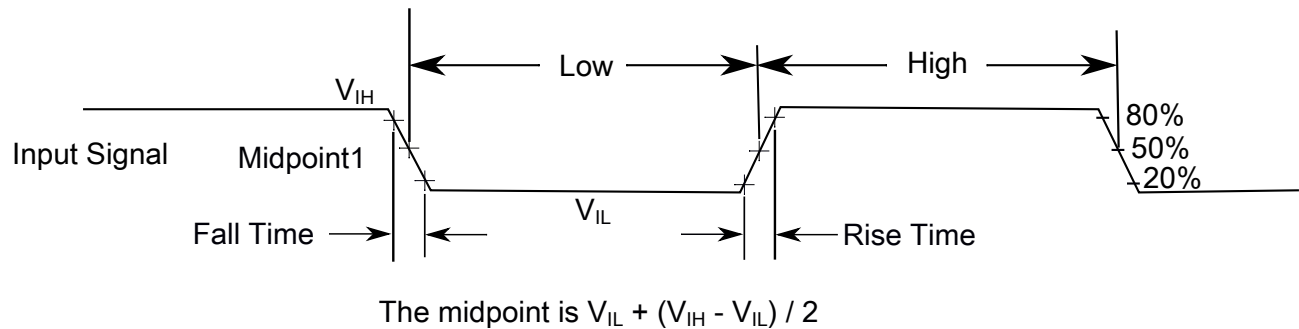


Figure 6. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

6.2 Nonswitching electrical specifications

6.2.1 Voltage and current operating requirements

Table 10. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------------|--|-------|------|------|-------|
| V_{DD} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DD_1P5} | DCDC V_{DD_1P5} output pin | 1.425 | 3.6 | V | 1 |
| V_{DDA} | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | 0.1 | V | |
| $V_{SS} - V_{SSA}$ | V_{SS} -to- V_{SSA} differential voltage | -0.1 | 0.1 | V | |

Table continues on the next page...

Table 10. Voltage and current operating requirements (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|---------------------|---|------------------------|------------------------|------|-------|
| V _{IH} | Input high voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V | 0.7 × V _{DD} | — | V | |
| | | 0.75 × V _{DD} | — | V | |
| V _{IL} | Input low voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V | — | 0.35 × V _{DD} | V | |
| | | — | 0.3 × V _{DD} | V | |
| V _{HYS} | Input hysteresis | 0.06 × V _{DD} | — | V | |
| I _{ICIO} | IO pin negative DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}–0.3V | –3 | — | mA | 2 |
| I _{ICcont} | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins <ul style="list-style-type: none"> • Negative current injection | –25 | — | mA | |
| V _{ODPU} | Open drain pullup voltage level | V _{DD} | V _{DD} | V | 3 |
| V _{RAM} | V _{DD} voltage required to retain RAM | 1.2 | — | V | |

1. This limit applies in any DCDC mode.
2. All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.
3. Open drain outputs must be pulled to V_{DD}.

6.2.2 LVD and POR operating requirements

Table 11. V_{DD} supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------------|---|------|------|------|------|-------|
| V _{POR} | Falling V _{DD} POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| V _{POR_VDD_1P5} | V _{DD_1P5} POR threshold | 1.25 | 1.31 | 1.37 | V | |
| V _{LVDH} | Falling low-voltage detect threshold — high range (LVDV = 01) | 2.48 | 2.56 | 2.64 | V | |
| | Low-voltage warning thresholds — high range | | | | | 1 |
| V _{LVW1H} | • Level 1 falling (LVWV = 00) | 2.62 | 2.70 | 2.78 | V | |
| V _{LVW2H} | • Level 2 falling (LVWV = 01) | 2.72 | 2.80 | 2.88 | V | |
| V _{LVW3H} | • Level 3 falling (LVWV = 10) | 2.82 | 2.90 | 2.98 | V | |
| V _{LVW4H} | • Level 4 falling (LVWV = 11) | 2.92 | 3.00 | 3.08 | V | |

Table continues on the next page...

Table 11. V_{DD} supply LVD and POR operating requirements (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|------|------|------|------|-------|
| V _{HYSH} | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | |
| V _{LVDL} | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| V _{LVW1L} | Low-voltage warning thresholds — low range | | | | | 1 |
| | • Level 1 falling (LVWV = 00) | 1.74 | 1.80 | 1.86 | V | |
| V _{LVW2L} | • Level 2 falling (LVWV = 01) | 1.84 | 1.90 | 1.96 | V | |
| V _{LVW3L} | • Level 3 falling (LVWV = 10) | 1.94 | 2.00 | 2.06 | V | |
| V _{LVW4L} | • Level 4 falling (LVWV = 11) | 2.04 | 2.10 | 2.16 | V | |
| V _{HYSL} | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | |
| V _{BG} | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| t _{LPO} | Internal low-power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising thresholds are falling threshold + hysteresis voltage

6.2.3 Voltage and current operating behaviors

Table 12. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|------------------------|------|------|-------|
| V _{OH} | Output high voltage — Normal drive pad (except RESET_b) | | | | 1, 2 |
| | • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -5 mA | V _{DD} - 0.5 | — | V | |
| | • 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -2.5 mA | V _{DD} - 0.5 | — | V | |
| | • 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -1 mA | V _{DD} - 0.35 | — | V | |
| V _{OH} | Output high voltage — High drive pad (except RESET_b) | | | | 1, 2 |
| | • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -20 mA | V _{DD} - 0.5 | — | V | |
| | • 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -10 mA | V _{DD} - 0.5 | — | V | |
| I _{OHT} | Output high current total for all ports | — | 100 | mA | |
| V _{OL} | Output low voltage — Normal drive pad | | | | 1 |
| | • 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 5 mA | — | 0.5 | V | |
| | • 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 2.5 mA | — | 0.5 | V | |
| V _{OL} | Output low voltage — High drive pad | | | | 1 |
| | | — | 0.5 | V | |

Table continues on the next page...

Table 12. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|---|------|-------|------------------|-------|
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 20\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 10\text{ mA}$ | — | 0.5 | V | |
| I_{OLT} | Output low current total for all ports | — | 100 | mA | |
| I_{IN} | Input leakage current (per pin) for full temperature range | — | 500 | nA | 3 |
| I_{IN} | Input leakage current (per pin) at 25 °C | — | 0.025 | μA | 3 |
| I_{IN} | Input leakage current (total all pins) for full temperature range | — | 5 | μA | 3 |
| R_{PU} | Internal pullup resistors | 20 | 50 | $\text{k}\Omega$ | 4 |

1. PTB0-1, PTC1-4, PTC6-7, PTC16-19 I/O have both high drive and normal drive capability selected by the associated PTX_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull-up device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at $V_{DD} = 3.6\text{ V}$.
4. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$.

6.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and $VLLSx \rightarrow \text{RUN}$ recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 13. Power mode transition operating behaviors

| Symbol | Description | Max. | Unit | Notes |
|-----------|---|-------|---------------|-------|
| t_{POR} | After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | 300 | μs | 1 |
| | <ul style="list-style-type: none"> • $VLLS0 \rightarrow \text{RUN}$ | 169.0 | μs | |
| | <ul style="list-style-type: none"> • $VLLS1 \rightarrow \text{RUN}$ | 168.9 | μs | |
| | <ul style="list-style-type: none"> • $VLLS2 \rightarrow \text{RUN}$ | 97.3 | μs | |

Table continues on the next page...

Table 13. Power mode transition operating behaviors (continued)

| Symbol | Description | Max. | Unit | Notes |
|--------|---------------|------|------|-------|
| | • VLLS3 → RUN | 97.3 | μs | |
| | • LLS → RUN | 6.3 | μs | |
| | • VLPS → RUN | 6.2 | μs | |
| | • STOP → RUN | 6.2 | μs | |

1. Normal boot (FTFA_FOPT[LPBOOT]=11). When the DC-DC converter is in bypass mode, TPOR will not meet the 300 μs spec when 1) VDD_1P5 < 1.6 V at 25 °C and 125 °C. 2) 1.5V ≤ VDD_1P5 ≤ 1.8 V. For the bypass mode special case where VDD_1P5 = VDD_1P8, TPOR did not meet the 300 μs maximum spec when the supply slew rate ≤ 100 V/s.

6.2.5 Power consumption operating behaviors

Table 14. Power consumption operating behaviors - Bypass Mode

| Mode# | Symbol | Description | Typ. | Max. | Unit | Notes |
|-------|--------------------------|---|------|----------|------|---------|
| 0 | I _{DDA} | Analog supply current | — | See note | mA | 1 |
| 1 | I _{DD_RUNCO_CM} | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus disabled, LPTMR running using LPO clock at 1kHz, CoreMark benchmark code executing from flash at 3.0 V | 6.73 | 9.94 | mA | 2, 3 |
| 2 | I _{DD_RUNCO} | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V | 3.84 | 6.95 | mA | 3, 4 |
| 3 | I _{DD_RUN_CM} | Run mode current - 48 MHz core/24 MHz bus and flash, all peripheral clocks disabled, CoreMark benchmark code executing from flash at 3.0 V | 6.72 | 9.93 | mA | 2, 3 |
| 4 | I _{DD_RUN} | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V | 4.46 | 7.50 | mA | 3, 4 |
| 5 | I _{DD_RUN} | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V | | | | 3, 4, 5 |
| | | at 25 °C | 5.59 | 6.03 | mA | |
| | | at 70 °C | 5.72 | 6.96 | mA | |
| | | at 105 °C | 6.22 | 8.60 | mA | |

Table continues on the next page...

Table 14. Power consumption operating behaviors - Bypass Mode (continued)

| Mode# | Symbol | Description | Typ. | Max. | Unit | Notes |
|-------|---------------------------|---|----------------------------|------------------------------|----------------|-------|
| 6 | I _{DD_WAIT} | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V | 2.48 | 5.70 | mA | 4 |
| 7 | I _{DD_WAIT} | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V | 1.95 | 5.20 | mA | 4 |
| 8 | I _{DD_PSTOP2} | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V | 2.31 | 5.60 | mA | 4 |
| 9 | I _{DD_VLPRCO_CM} | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running using LPO clock at 1 kHz reference clock, CoreMark benchmark code executing from flash at 3.0 V | 750.90 | 2162.15 | μA | 6 |
| 10 | I _{DD_VLPRCO} | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V | 157.56 | 1197.82 | μA | 7 |
| 11 | I _{DD_VLPR_CM} | Very-low-power run mode current -4 MHz core/0.8 MHz bus and flash, all peripheral clocks disabled, CoreMark benchmark code executing from flash at 3.0 V | 749.12 | 2169.25 | μA | 7 |
| 12 | I _{DD_VLPR} | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V | 176.75 | 1217.35 | μA | 7 |
| 13 | I _{DD_VLPR} | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V | 225.92 | 1261.85 | μA | 5, 7 |
| 14 | I _{DD_VLPW} | Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V | 115.97 | 988.58 | μA | 7 |
| 15 | I _{DD_STOP} | Stop mode current at 3.0 V at 25 °C at 70 °C at 105 °C | 233.19 334.36 714.91 | 395.00 1238.67 2854.74 | μA μA μA | |
| 16 | I _{DD_VLPS} | Very-low-power stop mode current at Bypass mode(3.0 V), at 25 °C at 70 °C at 105 °C | 5.99 44.41 181.39 | 37.86 239.01 740.69 | μA μA μA | |

Table continues on the next page...

Table 14. Power consumption operating behaviors - Bypass Mode (continued)

| Mode# | Symbol | Description | Typ. | Max. | Unit | Notes |
|-------|--------------------------------------|--|-------|--------|------|-------|
| 17 | I _{DD_LLS3} | Low-leakage stop mode 3 current at Bypass mode(3.0 V), | | | | |
| | | at 25 °C | 3.04 | 7.96 | μA | |
| | | at 70 °C | 16.27 | 54.57 | μA | |
| | | at 105 °C | 61.37 | 185.22 | μA | |
| 18 | I _{DD_LLS2} | Low-leakage stop mode 2 current at Bypass mode(3.0 V), | | | | |
| | | at 25 °C | 2.67 | 6.17 | μA | |
| | | at 70 °C | 13.39 | 49.00 | μA | |
| | | at 105 °C | 50.32 | 142.43 | μA | |
| 19 | I _{DD_VLLS3} | Very-low-leakage stop mode 3 current at Bypass mode(3.0 V), | | | | |
| | | at 25 °C | 2.23 | 5.35 | μA | |
| | | at 70 °C | 12.14 | 46.10 | μA | |
| | | at 105 °C | 46.73 | 126.37 | μA | |
| 20 | I _{DD_VLLS2_16KB} | Very-low-leakage stop mode 2 current at Bypass mode(3.0 V), | | | | |
| | | at 25 °C | 1.67 | 2.53 | μA | |
| | | at 70 °C | 6.58 | 25.82 | μA | |
| | | at 105 °C | 25.32 | 57.92 | μA | |
| 21 | I _{DD_VLLS2_32KB} | Very-low-leakage stop mode 2 current at Bypass mode (3.0 V) (set SMC_STOPCTRL[RAM2PO]=1 based on IDD_VLLS2_16KB configuration), | | | | |
| | | at 25 °C | 1.84 | — | μA | |
| | | at 70 °C | 8.10 | — | μA | |
| | | at 105 °C | 29.47 | — | μA | |
| 22 | I _{DD_VLLS2_16KB_RF_Tx_RAM} | Very-low-leakage stop mode 2 current at Bypass mode (3.0 V) (set RSIM_CONTROL[TXRAMPO]=1 based on IDD_VLLS2_16KB configuration), | | | | |
| | | at 25 °C | 1.75 | — | μA | |
| | | at 70 °C | 7.83 | — | μA | |
| | | at 105 °C | 28.32 | — | μA | |
| 23 | I _{DD_VLLS2_16KB_RF_Rx_RAM} | Very-low-leakage stop mode 2 current at Bypass mode (3.0 V) (set RSIM_CONTROL[RXRAMPO]=1 based on IDD_VLLS2_16KB configuration), | | | | |
| | | at 25 °C | 1.75 | — | μA | |
| | | at 70 °C | 7.65 | — | μA | |
| | | at 105 °C | 27.73 | — | μA | |

Table continues on the next page...

Table 14. Power consumption operating behaviors - Bypass Mode (continued)

| Mode# | Symbol | Description | Typ. | Max. | Unit | Notes | | |
|----------|-----------------------|---|-----------------------|---|--------|--------|----|---|
| 24 | I _{DD_VLLS1} | Very-low-leakage stop mode 1 current at Bypass mode(3.0 V), | | | | | | |
| | | at 25 °C | 917.42 | 1355.71 | nA | | | |
| | | at 70 °C | 3.24 | 13.32 | μA | | | |
| | | at 105 °C | 15.62 | 32.08 | μA | | | |
| | | 25 | I _{DD_VLLS0} | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V | | | | |
| | | | | at 25 °C | 467.55 | 998.32 | nA | |
| at 70 °C | 2.78 | | | 13.05 | μA | | | |
| | | at 105 °C | 15.11 | 31.48 | μA | | | |
| | | 26 | I _{DD_VLLS0} | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V | | | | 8 |
| | | | | at 25 °C | 266.64 | 737.22 | nA | |
| at 70 °C | 2.54 | | | 13.02 | μA | | | |
| | | at 105 °C | 14.78 | 31.12 | μA | | | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See specifications of each module for its supply current.
2. MCG configured for FEI mode. CoreMark benchmark compiled using IAR 7.70 with optimization level high, optimized for balanced.
3. Radio is off.
4. MCG configured for FEI mode.
5. Incremental current consumption from peripheral activity is not included.
6. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 7.70 with optimization level high, optimized for balanced.
7. MCG configured for BLPI mode.
8. No brownout.

Table 15. Power consumption operating behaviors - Buck Mode

| Mode# | Symbol | Description | Typ. | Max. | Unit | Notes |
|-------|--------------------------|--|------|----------|------|-------|
| 0 | I _{DDA} | Analog supply current | — | See note | mA | 1 |
| 1 | I _{DD_RUNCO_CM} | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, LPTMR running using LPO clock at 1 kHz, CoreMark benchmark code executing from flash at 3.0 V | 4.97 | — | mA | 2, 3 |
| 2 | I _{DD_RUNCO} | Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V | 3.13 | — | mA | 2, 3 |
| 3 | I _{DD_RUN_CM} | Run mode current - 48 MHz core/24 MHz bus and flash, all peripheral clocks disabled, CoreMark benchmark code executing from flash at 3.0 V | 4.88 | — | mA | 2, 3 |

Table continues on the next page...

Table 15. Power consumption operating behaviors - Buck Mode (continued)

| Mode# | Symbol | Description | Typ. | Max. | Unit | Notes |
|-------|---------------------------|---|--------|-------|------|---------|
| 4 | I _{DD_RUN} | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V | 3.37 | — | mA | 2, 3 |
| 5 | I _{DD_RUN} | Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V | | | | 2, 3, 4 |
| | | at 25 °C | 4.09 | — | mA | |
| | | at 70 °C | 4.22 | — | mA | |
| | | at 105 °C | 4.60 | — | mA | |
| 6 | I _{DD_WAIT} | Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V | 2.36 | — | mA | 2 |
| 7 | I _{DD_WAIT} | Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V | 2.09 | — | mA | 2 |
| 8 | I _{DD_PSTOP2} | Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus at 3.0 V | 2.32 | — | mA | 2 |
| 9 | I _{DD_VLPRCO_CM} | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, CoreMark benchmark code executing from flash at 3.0 V | 563.18 | — | µA | 5 |
| 10 | I _{DD_VLPRCO} | Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash at 3.0 V | 152.88 | — | µA | 5 |
| 11 | I _{DD_VLPR_CM} | Very-low-power run mode current - 4 MHz core/0.8 MHz bus and flash, all peripheral clocks disabled, CoreMark benchmark code executing from flash at 3.0 V | 558.88 | — | µA | 5 |
| 12 | I _{DD_VLPR} | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash at 3.0 V | 150.33 | — | µA | 5 |
| 13 | I _{DD_VLPR} | Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash at 3.0 V | 207.02 | — | µA | 4, 5 |
| 14 | I _{DD_VLPW} | Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled at 3.0 V | 113.53 | — | µA | 5 |
| 15 | I _{DD_STOP} | Stop mode current at 3.0 V | | | | |
| | | at 25 °C | 1.65 | 2.712 | mA | |
| | | at 70 °C | 1.82 | 4.728 | mA | |
| | | at 105 °C | 2.15 | 7.686 | mA | |

Table continues on the next page...

Table 15. Power consumption operating behaviors - Buck Mode (continued)

| Mode# | Symbol | Description | Typ. | Max. | Unit | Notes |
|-------|--------------------------------------|--|--------|---------|------|-------|
| 16 | I _{DD_VLPS} | Very-low-power stop mode current at Buck mode(3.0 V), | | | | |
| | | at 25 °C | 7.34 | 39.203 | μA | |
| | | at 70 °C | 58.34 | 252.935 | μA | |
| | | at 105 °C | 276.96 | 836.252 | μA | |
| 17 | I _{DD_LLS3} | Low-leakage stop mode 3 current at Buck mode(3.0 V), | | | | |
| | | at 25 °C | 2.95 | 7.547 | μA | |
| | | at 70 °C | 20.42 | 58.722 | μA | |
| | | at 105 °C | 86.84 | 210.696 | μA | |
| 18 | I _{DD_LLS2} | Low-leakage stop mode 2 current at Buck mode(3.0 V), | | | | |
| | | at 25 °C | 2.61 | 5.975 | μA | |
| | | at 70 °C | 13.90 | 49.512 | μA | |
| | | at 105 °C | 47.87 | 139.983 | μA | |
| 19 | I _{DD_VLLS3} | Very-low-leakage stop mode 3 current at Buck mode(3.0 V), | | | | |
| | | at 25 °C | 2.17 | 5.283 | μA | |
| | | at 70 °C | 11.14 | 45.099 | μA | |
| | | at 105 °C | 40.37 | 120.006 | μA | |
| 20 | I _{DD_VLLS2_16KB} | Very-low-leakage stop mode 2 current at Buck mode(3.0 V), | | | | |
| | | at 25 °C | 1.41 | 2.236 | μA | |
| | | at 70 °C | 5.69 | 24.923 | μA | |
| | | at 105 °C | 21.24 | 53.843 | μA | |
| 21 | I _{DD_VLLS2_32KB} | Very-low-leakage stop mode 2 current at Buck mode (3.0 V) (set SMC_STOPCTRL[RAM2PO]=1 based on IDD_VLLS2_16KB configuration), | | | | |
| | | at 25 °C | 1.85 | — | μA | |
| | | at 70 °C | 7.92 | — | μA | |
| | | at 105 °C | 28.84 | — | μA | |
| 22 | I _{DD_VLLS2_16KB_RF_TX_RAM} | Very-low-leakage stop mode 2 current at Buck mode (3.0 V) (set RSIM_CONTROL[TXRAMPO]=1 based on IDD_VLLS2_16KB configuration), | | | | |
| | | at 25 °C | 1.68 | — | μA | |
| | | at 70 °C | 7.56 | — | μA | |
| | | at 105 °C | 27.97 | — | μA | |

Table continues on the next page...

Table 15. Power consumption operating behaviors - Buck Mode (continued)

| Mode# | Symbol | Description | Typ. | Max. | Unit | Notes |
|-------|--------------------------------------|--|--------|----------|------|-------|
| 23 | I _{DD_VLLS2_16KB_RF_Rx_RAM} | Very-low-leakage stop mode 2 current at Buck mode (3.0 V) (set RSIM_CONTROL[RXRAMPO]=1 based on IDD_VLLS2_16KB configuration), | | | | |
| | | at 25 °C | 1.91 | — | μA | |
| | | at 70 °C | 6.81 | — | μA | |
| | | at 105 °C | 25.64 | — | μA | |
| 24 | I _{DD_VLLS1} | Very-low-leakage stop mode 1 current at Buck mode(3.0 V), | | | | |
| | | at 25 °C | 976.17 | 1414.459 | nA | |
| | | at 70 °C | 2.98 | 13.053 | μA | |
| | | at 105 °C | 13.18 | 29.640 | μA | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See specification of each module for its supply current.
2. MCG configured for FEI mode.
3. Radio is off.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.

Table 16. Low power mode peripheral adders — typical value (Bypass Mode)

| Adder# | Symbol | Description | Temperature (°C) | | | | | Unit |
|--------|----------------------------|---|------------------|-------|-------|-------|-------|------|
| | | | -40 | 25 | 50 | 70 | 85 | |
| 1 | I _{IREFSTEN4MHZ} | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 47.50 | 47.50 | 47.51 | 47.39 | 47.12 | μA |
| 2 | I _{IREFSTEN32KHZ} | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 92.82 | 92.82 | 92.61 | 91.89 | 91.91 | μA |
| 3 | I _{IREFSTEN32KHZ} | External 32 kHz crystal clock adder by means of the RTC bits. Measured by entering all modes with the crystal enabled. | | | | | | |
| | | VLLS1 | 1.24 | 1.23 | 1.25 | 1.29 | 1.25 | μA |
| | | VLLS2 | 1.23 | 1.22 | 1.23 | 1.16 | 1.26 | |
| | | VLLS3 | 1.22 | 1.22 | 1.12 | 1.16 | 1.21 | |
| | | LLS2 | 1.22 | 1.21 | 1.12 | 1.28 | 1.30 | |
| LLS3 | 1.21 | 1.21 | 1.22 | 1.32 | 1.26 | | | |
| 4 | I _{CMP} | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 21.15 | 21.15 | 21.39 | 21.55 | 21.76 | μA |

Table continues on the next page...

Table 16. Low power mode peripheral adders — typical value (Bypass Mode) (continued)

| Adder# | Symbol | Description | Temperature (°C) | | | | | Unit |
|--------|---------------------|---|------------------|--------|--------|--------|--------|------|
| | | | -40 | 25 | 50 | 70 | 85 | |
| 5 | I _{RTC} | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption. | 1.25 | 1.24 | 1.25 | 1.32 | 1.31 | μA |
| 6 | I _{LPUART} | LPUART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for Rx data at 115200 baud rate. Includes selected clock source power consumption. MCGIRCLK (4 MHz internal reference clock) | 58.73 | 58.73 | 59.13 | 59.32 | 59.67 | μA |
| 7 | I _{LPTMR} | LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO. | 31.32 | 31.30 | 34.49 | 65.73 | 100.58 | nA |
| 8 | I _{TPM} | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. MCGIRCLK (4 MHz internal reference clock) | 56.93 | 56.92 | 56.99 | 56.92 | 56.84 | μA |
| 9 | I _{BG} | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 90.49 | 90.48 | 91.85 | 91.74 | 88.16 | μA |
| 10 | I _{ADC} | ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low-power mode using the internal clock and continuous conversions. | 347.96 | 347.96 | 346.12 | 347.88 | 346.43 | μA |

6.2.6 Diagram: Typical IDD_RUN operating behavior

The following data is measured from previous devices with same MCU core (Arm® Cortex-M0+) under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

NOTE

The results in the following graphs are obtained using the device in Bypass mode.

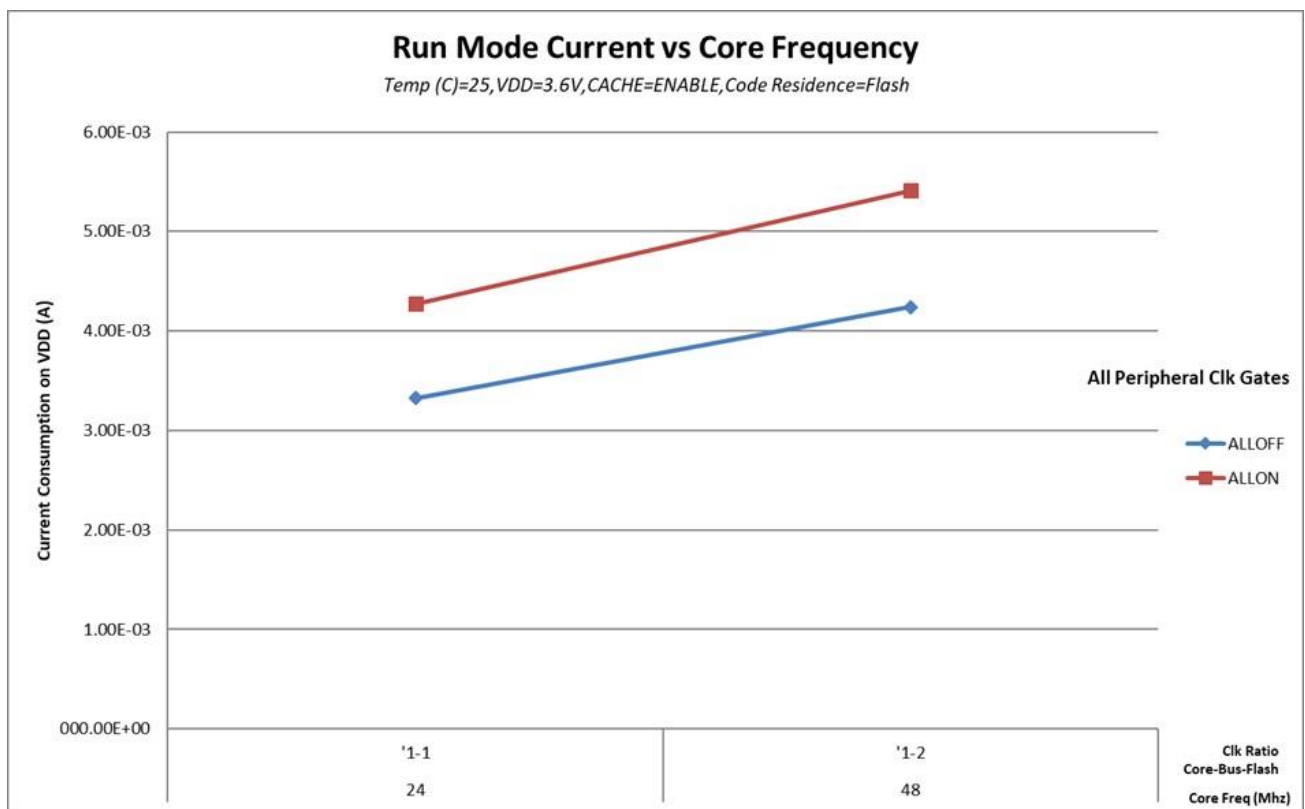


Figure 7. Run mode supply current vs. core frequency

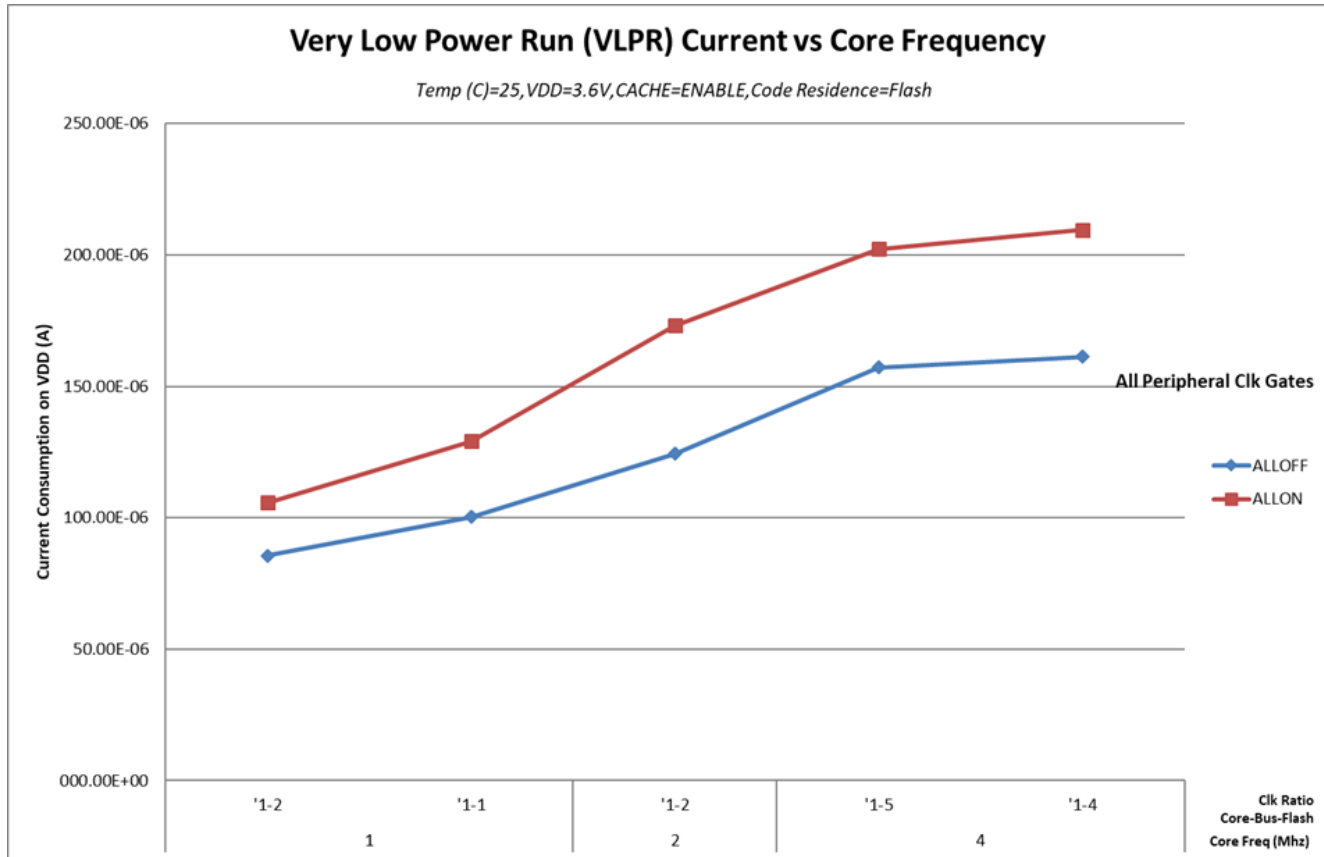


Figure 8. VLPR mode current vs. core frequency

6.2.7 SoC Power Consumption

Full KW39/38/37 system-on-chip (SoC) power consumption is a function of the many configurations possible for the MCU platform and its peripherals including the 2.4 GHz radio and the DC-DC converter. A few measured SoC configurations are as follows:

Table 17. SoC Power Consumption

| MCU State | Flash State | Radio State | DC-DC State | Typical Average IC current | Unit |
|-----------|-------------|-----------------------------|------------------------------------|----------------------------|------|
| STOP | Doze | Rx | Buck (V _{DCDC_IN} =3.6 V) | 8.5 | mA |
| STOP | Doze | Tx (at 0 dBm) | Buck (V _{DCDC_IN} =3.6 V) | 7.8 | mA |
| STOP | Doze | Tx (at +3.5 dBm) | Buck (V _{DCDC_IN} =3.6 V) | 9.2 | mA |
| STOP | Doze | Tx (at +5 dBm) ¹ | Buck (V _{DCDC_IN} =3.6 V) | 10.3 | mA |
| RUN | Enabled | Rx | Buck (V _{DCDC_IN} =3.6 V) | 10.4 | mA |
| RUN | Enabled | Tx (at 0 dBm) | Buck (V _{DCDC_IN} =3.6 V) | 9.9 | mA |

Table continues on the next page...

Table 17. SoC Power Consumption (continued)

| MCU State | Flash State | Radio State | DC-DC State | Typical Average IC current | Unit |
|-----------|-------------|-----------------------------|------------------------------|----------------------------|------|
| RUN | Enabled | Tx (at +3.5 dBm) | Buck ($V_{DCDC_IN}=3.6$ V) | 11.7 | mA |
| RUN | Enabled | Tx (at +5 dBm) ¹ | Buck ($V_{DCDC_IN}=3.6$ V) | 12.8 | mA |
| STOP | Doze | Rx | Disabled/Bypass | 17.3 | mA |
| STOP | Doze | Tx (at 0 dBm) | Disabled/Bypass | 15.9 | mA |
| STOP | Doze | Tx (at +3.5 dBm) | Disabled/Bypass | 18.3 | mA |
| STOP | Doze | Tx (at +5 dBm) ¹ | Disabled/Bypass | 20.3 | mA |
| RUN | Enabled | Rx | Disabled/Bypass | 21.5 | mA |
| RUN | Enabled | Tx (at 0 dBm) | Disabled/Bypass | 19.9 | mA |
| RUN | Enabled | Tx (at +3.5 dBm) | Disabled/Bypass | 22.4 | mA |
| RUN | Enabled | Tx (at +5 dBm) ¹ | Disabled/Bypass | 24.4 | mA |

1. MCU configured to use an FLL-based 20 MHz clock.

6.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com
2. Perform a keyword search for “KW38, HW guideline, RF system evaluation.”

6.2.9 Capacitance attributes

Table 18. Capacitance attributes

| Symbol | Description | Min. | Max. | Unit |
|----------|-------------------|------|------|------|
| C_{IN} | Input capacitance | — | 7 | pF |

6.3 Switching electrical specifications

6.3.1 Device clock specifications

Table 19. Device clock specifications

| Symbol | Description | Min. | Max. | Unit |
|----------------------------------|--------------------------------|------|------|------|
| Normal run mode | | | | |
| f_{SYS} | System and core clock | — | 48 | MHz |
| f_{BUS} | Bus clock | — | 24 | MHz |
| f_{FLASH} | Flash clock | — | 24 | MHz |
| f_{LPTMR} | LPTMR clock | — | 24 | MHz |
| VLPR and VLPS modes ¹ | | | | |
| f_{SYS} | System and core clock | — | 4 | MHz |
| f_{BUS} | Bus clock | — | 1 | MHz |
| f_{FLASH} | Flash clock | — | 1 | MHz |
| f_{LPTMR} | LPTMR clock ² | — | 24 | MHz |
| f_{ERCLK} | External reference clock | — | 16 | MHz |
| f_{LPTMR_ERCLK} | LPTMR external reference clock | — | 16 | MHz |
| f_{TPM} | TPM asynchronous clock | — | 8 | MHz |
| $f_{LPUART0}$ | LPUART0 asynchronous clock | — | 12 | MHz |

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

6.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, CAN (for KW38 only), CMT and I²C signals.

Table 20. General switching specifications

| Description | Min. | Max. | Unit | Notes |
|--|------|------|------------------|-------|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| NMI_b pin interrupt pulse width (analog filter enabled) — Asynchronous path | 200 | — | ns | 3 |
| GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path | 20 | — | ns | 3 |
| External RESET_b input pulse width (digital glitch filter disabled) | 100 | — | ns | |
| Port rise and fall time(high drive strength) | | | | 4, 5 |
| • Slew enabled | — | 25 | ns | |
| | — | 16 | ns | |

Table continues on the next page...

Table 20. General switching specifications (continued)

| Description | Min. | Max. | Unit | Notes |
|--|------|------|------|-------|
| <ul style="list-style-type: none"> • $1.71 \leq VDD \leq 2.7 V$ • $2.7 \leq VDD \leq 3.6 V$ | — | 8 | ns | |
| <ul style="list-style-type: none"> • Slew disabled • $1.71 \leq VDD \leq 2.7 V$ • $2.7 \leq VDD \leq 3.6 V$ | — | 6 | ns | |
| Port rise and fall time(low drive strength) | | | | 6, 7 |
| <ul style="list-style-type: none"> • Slew enabled • $1.71 \leq VDD \leq 2.7 V$ • $2.7 \leq VDD \leq 3.6 V$ | — | 24 | ns | |
| <ul style="list-style-type: none"> • Slew disabled • $1.71 \leq VDD \leq 2.7 V$ • $2.7 \leq VDD \leq 3.6 V$ | — | 16 | ns | |
| | — | 10 | ns | |
| | — | 6 | ns | |

1. This is the minimum pulse width that guarantees to pass through the pin synchronization circuitry in run modes.
2. The greater of synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that guarantees to be recognized.
4. PTB0, PTB1, PTC1, PTC2, PTC3, PTC4, PTC6, PTC7, PTC16, PTC17, PTC18, PTC19.
5. 75 pF load.
6. Ports A, B, and C.
7. 25 pF load.

6.4 Thermal specifications

6.4.1 Thermal operating requirements

Table 21. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--------------------------|------|------|------|-------|
| T_J | Die junction temperature | −40 | 125 | °C | |
| T_A | Ambient temperature | −40 | 105 | °C | 1 |

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

6.4.2 Thermal attributes

Table 22. Thermal attributes

| Board type | Symbol | Description | 48-pin "Wettable" HVQFN | Unit | Notes |
|-------------------|-----------------|--|-------------------------------|------|-------|
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 21.4 | °C/W | 1, 2 |
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top (natural convection) | 0.2 | °C/W | 1, 3 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board construction.
2. Determined according to JEDEC Standard JESD51-2A.
3. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2A.

The thermal characterization parameter (Ψ_{JT}) is used to determine the junction temperature with a measurement of the temperature at the top of the package case using the following equation:

$$T_J = T_T + \Psi_{JT} \times \text{chip power dissipation}$$

where T_T is the thermocouple temperature at the top of the package.

6.5 Peripheral operating requirements and behaviors

6.5.1 Core modules

6.5.1.1 SWD electricals

Table 23. SWD full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | SWD_CLK frequency of operation <ul style="list-style-type: none"> • Serial wire debug | 0 | 25 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width <ul style="list-style-type: none"> • Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |

Table continues on the next page...

Table 23. SWD full voltage range electricals (continued)

| Symbol | Description | Min. | Max. | Unit |
|--------|---|------|------|------|
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

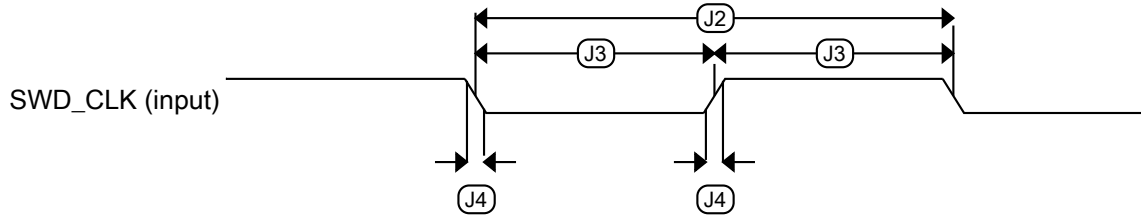


Figure 9. Serial wire clock input timing

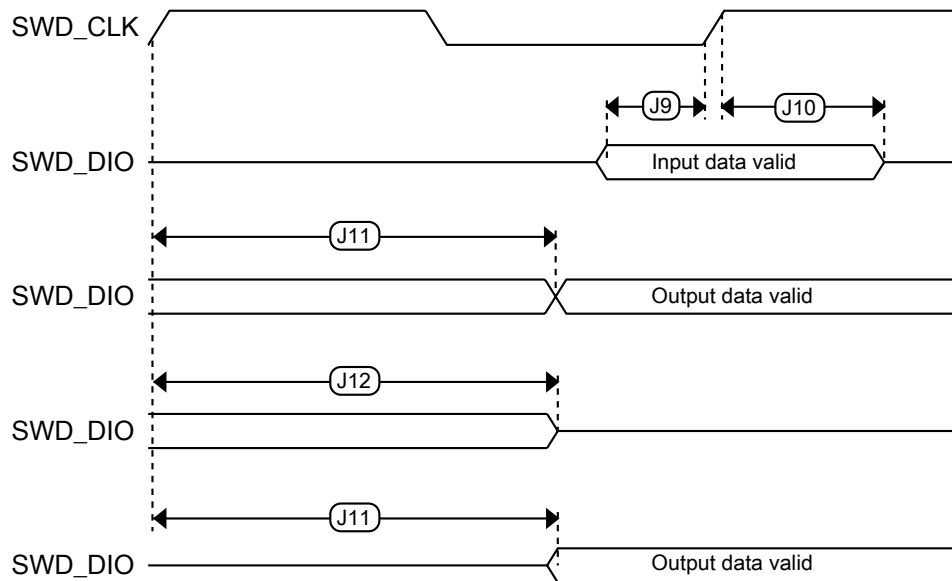


Figure 10. Serial wire data timing

6.5.2 System modules

There are no specifications necessary for the device's system modules.

6.5.3 Clock modules

6.5.3.1 MCG specifications

Table 24. MCG specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes | |
|---------------------------------|--|---|-----------|-----------|-------------------------|-------|------|
| $f_{\text{ints_ft}}$ | Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C | — | 32.768 | — | kHz | | |
| $f_{\text{ints_t}}$ | Internal reference frequency (slow clock) — user trimmed | 31.25 | — | 39.0625 | kHz | | |
| $\Delta f_{\text{dco_res_t}}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM] | — | ± 0.3 | ± 0.6 | % f_{dco} | 1 | |
| $\Delta f_{\text{dco_t}}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | — | +0.5/−0.7 | ± 3 | % f_{dco} | 1, 2 | |
| $\Delta f_{\text{dco_t}}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C | — | ± 0.4 | ± 1.5 | % f_{dco} | 1, 2 | |
| $f_{\text{intf_ft}}$ | Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C | — | 4 | — | MHz | | |
| $\Delta f_{\text{intf_ft}}$ | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C | — | +1/−2 | ± 11 | % $f_{\text{intf_ft}}$ | 2 | |
| $f_{\text{intf_t}}$ | Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C | 3 | — | 5 | MHz | | |
| $f_{\text{loc_low}}$ | Loss of external clock minimum frequency — RANGE = 00 | $(3/5) \times f_{\text{ints_t}}$ | — | — | kHz | | |
| $f_{\text{loc_high}}$ | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | $(16/5) \times f_{\text{ints_t}}$ | — | — | kHz | | |
| FLL | | | | | | | |
| $f_{\text{fll_ref}}$ | FLL reference frequency range | 31.25 | — | 39.0625 | kHz | | |
| f_{dco} | DCO output frequency range | Low range (DRS = 00) $640 \times f_{\text{fll_ref}}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS = 01) $1280 \times f_{\text{fll_ref}}$ | 40 | 41.94 | 48 | MHz | |
| $f_{\text{dco_t_DMX3}_2}$ | DCO output frequency | Low range (DRS = 00) $732 \times f_{\text{fll_ref}}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS = 01) $1464 \times f_{\text{fll_ref}}$ | — | 47.97 | — | MHz | |
| $J_{\text{cyc_fll}}$ | FLL period jitter • $f_{\text{VCO}} = 48$ MHz | — | 180 | — | ps | 7 | |
| $t_{\text{fll_acquire}}$ | FLL target frequency acquisition time | — | — | 1 | ms | 8 | |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft} .
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the following changes: FLL reference source or reference divider, trim value, DMX32 bit, DRS bits, or FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is used as the reference, this specification assumes it is already running.

6.5.3.2 Reference Oscillator Specification

The KW39/38/37 has been designed to meet targeted standard specifications for frequency error over the life of the part, which includes the temperature, mechanical and aging effects.

The table below lists the recommended crystal specifications. Note that these are recommendations only and deviation may be allowed. However, deviations may result in degraded RF performance or possibly a failure to meet RF protocol certification standards. Designers must ensure that the crystal(s) they use meet the requirements of their application.

Table 25. Recommended Crystal and Oscillator Specification

| Symbol | Description | F0 = 32.0 MHz | | | F0 = 26.0 MHz | | | Unit | Notes |
|----------|--|---------------|------|-------|---------------|------|-------|------|-------|
| | | Min | Typ | Max | Min | Typ | Max | | |
| T_A | Operating Temperature | -40 | — | 105 | -40 | — | 105 | °C | 1 |
| | Crystal initial frequency tolerance | -10 | — | 10 | -10 | — | 10 | ppm | 2,3 |
| | Crystal frequency stability and aging | -25 | — | 25 | -25 | — | 24 | ppm | 2,4 |
| | Oscillator variation | -12 | — | 15 | -12 | — | 16 | ppm | 5 |
| | Total reference oscillator tolerance for Bluetooth LE applications | -50 | — | 50 | -50 | — | 50 | ppm | 6 |
| C_L | Load capacitance | 7 | 10 | 13 | 7 | 10 | 13 | pF | 2, 7 |
| C_0 | Shunt capacitance | 0.469 | 0.67 | 0.871 | 0.42 | 0.6 | 0.78 | pF | 2,7 |
| C_{m1} | Motional capacitance | 1.435 | 2.05 | 2.665 | 1.435 | 2.05 | 2.665 | fF | 2,7 |
| L_{m1} | Motional inductance | 8.47 | 12.1 | 15.73 | 12.81 | 18.3 | 23.79 | mH | 2,7 |

Table continues on the next page...

Table 25. Recommended Crystal and Oscillator Specification (continued)

| Symbol | Description | F0 = 32.0 MHz | | | F0 = 26.0 MHz | | | Unit | Notes |
|------------------|------------------------------|---------------|------|-------|---------------|------|-------|--------|-------|
| | | Min | Typ | Max | Min | Typ | Max | | |
| Rm1 | Motional resistance | — | 25 | 50 | — | 35 | 50 | Ohms | 2 |
| ESR | Equivalent series resistance | — | — | 60 | — | — | 60 | Ohms | 2,8 |
| P _d | Maximum crystal drive | — | 10 | 200 | — | 10 | 200 | uW | 2 |
| T _S | Trim sensitivity | 6.30 | 9.00 | 11.70 | 6.39 | 9.12 | 11.86 | ppm/pF | 2,7 |
| T _{osc} | Oscillator Startup Time | — | 500 | — | — | 500 | — | μs | 9 |

1. Full temperature range of this device. A reduced range can be chosen to meet application needs.
2. Recommended crystal specification.
3. Measured at 25 °C.
4. Combination of frequency stability variation over desired temperature range and frequency variation due to aging over desired lifetime of system.
5. Variation due to temperature, process, and aging of MCU.
6. Sum of crystal initial frequency tolerance, crystal frequency stability and aging, oscillator variation, and PCB manufacturing variation must not exceed this value.
7. Typical is target. 30% tolerances shown.
8. $ESR = Rm1 * (1 + [C_0/C_L])^2$.
9. Time from oscillator enable to clock ready. Dependent on the complete hardware configuration of the oscillator.

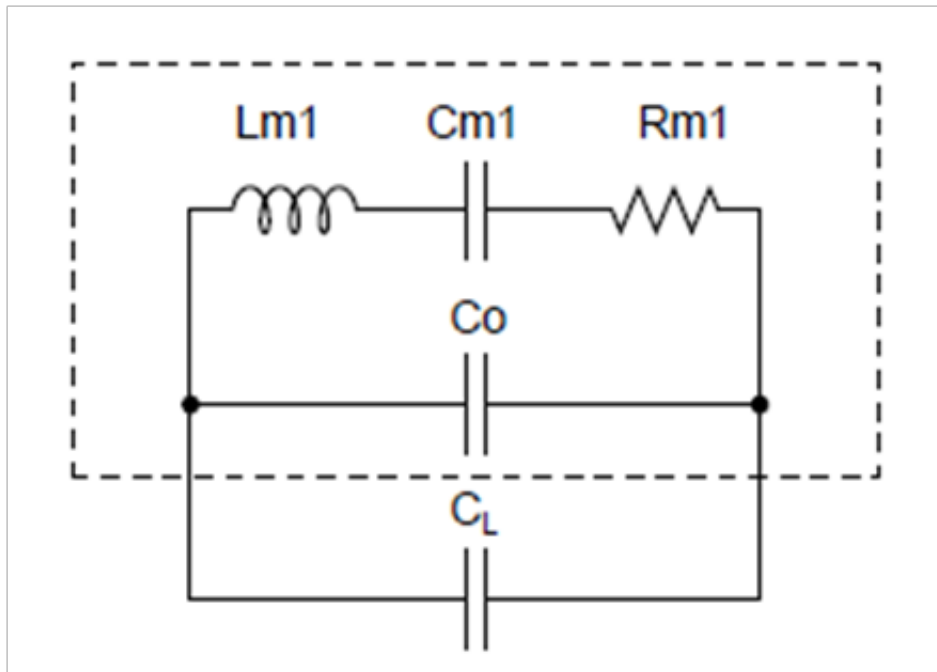


Figure 11. Crystal Electrical Model

6.5.3.3 32 kHz Oscillator Frequency Specifications

Table 26. 32 kHz Crystal and Oscillator Specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------|-----------------------------------|------|--------|----------|-------|-------|
| f_{osc_lo} | Crystal frequency | — | 32.768 | — | kHz | |
| T_A | Operating temperature | -40 | — | 105 | °C | 1 |
| | Total crystal frequency tolerance | -500 | — | 500 | ppm | 2,3 |
| C_L | Load capacitance | — | 12.5 | — | pF | 2 |
| ESR | Equivalent series resistance | — | — | 80 | kOhms | 2 |
| t_{start} | Crystal start-up time | — | 1000 | — | ms | 4 |
| $f_{ec_extal32}$ | External input clock frequency | — | 32.768 | — | kHz | 5 |
| $V_{ec_extal32}$ | External input clock amplitude | 0.7 | — | V_{DD} | V | 6 |

1. Full temperature range of this device. A reduced range can be chosen to meet application needs.
2. Recommended crystal specification.
3. Sum of crystal initial frequency tolerance, crystal frequency stability, and aging tolerances given by crystal vendor.
4. Time from oscillator enable to clock stable. Dependent on the complete hardware configuration of the oscillator.
5. External oscillator connected to EXTAL32K. XTAL32K must be unconnected.
6. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of VSS to VDD.

6.5.4 Memories and memory interfaces

6.5.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

6.5.4.1.1 Flash timing specifications — commands

Table 27. Flash command timing specifications

| Symbol | Description ¹ | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|------|------|-------|
| $t_{rd1blk256k}$ | Read 1s Block execution time • 256 KB program/data flash | — | — | 2 | ms | |
| $t_{rd1sec2k}$ | Read 1s Section execution time (2 KB flash) | — | — | 75 | μs | |
| t_{pgmchk} | Program Check execution time | — | — | 95 | μs | |

Table continues on the next page...

Table 27. Flash command timing specifications (continued)

| Symbol | Description ¹ | Min. | Typ. | Max. | Unit | Notes |
|-------------------|--|------|------|------|---------|-------|
| t_{rdsrc} | Read Resource execution time | — | — | 40 | μ s | |
| t_{pgm8} | Program Phrase execution time | — | 90 | 225 | μ s | |
| $t_{ersblk256k}$ | Erase Flash Block execution time • 256 KB program/data flash | — | 125 | 2125 | ms | 2 |
| t_{ersscr} | Erase Flash Sector execution time | — | 12 | 130 | ms | 2 |
| $t_{pgmsec2k}$ | Program Section execution time (2 KB flash) | — | 10 | — | ms | |
| $t_{rd1allx}$ | Read 1s All Blocks execution time • FlexNVM devices | — | — | 3.5 | ms | |
| $t_{rd1alln}$ | • Program flash only devices | — | — | 3.5 | ms | |
| t_{rdonce} | Read Once execution time | — | — | 30 | μ s | |
| $t_{pgmonce}$ | Program Once execution time | — | 90 | — | μ s | |
| t_{ersall} | Erase All Blocks execution time | — | 262 | 4380 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 35 | μ s | |
| $t_{ersallu}$ | Erase All Blocks Unsecure execution time | — | 262 | 4380 | ms | 2 |
| $t_{swapx01}$ | Swap Control execution time • control code 0x01 | — | 280 | — | μ s | |
| $t_{swapx02}$ | • control code 0x02 | — | 100 | 235 | μ s | |
| $t_{swapx04}$ | • control code 0x04 | — | 100 | 235 | μ s | |
| $t_{swapx08}$ | • control code 0x08 | — | — | 35 | μ s | |
| $t_{swapx10}$ | • control code 0x10 | — | 100 | 235 | μ s | |
| $t_{pgmpart32k}$ | Program Partition for EEPROM execution time • 32 KB EEPROM backup | — | 252 | — | ms | |
| $t_{pgmpart256k}$ | • 256 KB EEPROM backup | — | 262 | — | ms | |
| $t_{setramff}$ | Set FlexRAM Function execution time: • Control Code 0xFF | — | 115 | — | μ s | |
| $t_{setram32k}$ | • 32 KB EEPROM backup | — | 0.8 | 1.2 | ms | |
| $t_{setram256k}$ | • 256 KB EEPROM backup | — | 4.5 | 6.1 | ms | |
| $t_{eewr8b32k}$ | Byte-write to FlexRAM execution time: • 32 KB EEPROM backup | — | 385 | 1700 | μ s | 3 |
| $t_{eewr8b256k}$ | • 256 KB EEPROM backup | — | 1015 | 3800 | μ s | |
| $t_{eewr16b32k}$ | 16-bit write to FlexRAM execution time: • 32 KB EEPROM backup | — | 385 | 1700 | μ s | 3 |
| $t_{eewr16b256k}$ | • 256 KB EEPROM backup | — | 1015 | 3800 | μ s | |
| $t_{eewr32bers}$ | 32-bit write to erased FlexRAM location execution time | — | 360 | 2000 | μ s | 3 |

Table continues on the next page...

Table 27. Flash command timing specifications (continued)

| Symbol | Description ¹ | Min. | Typ. | Max. | Unit | Notes |
|--------------------------|--|------|------|------|---------------|-------|
| $t_{\text{eewr32b32k}}$ | 32-bit write to FlexRAM execution time: • 32 KB EEPROM backup | — | 630 | 2000 | μs | 3 |
| $t_{\text{eewr32b256k}}$ | • 256 KB EEPROM backup | — | 1890 | 4100 | μs | |

1. All command times assume 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. First time EERAM writes after a Reset or SETRAM command may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.

NOTE

Under certain circumstances maximum times for writes to FlexRAM may be exceeded. In this case the user or application may wait, or assert reset to the FTFE module to stop the operation.

6.5.4.1.2 Reliability specifications (Automotive)**Table 28. NVM reliability specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|--|----------------|--------|--------|------------------|---------|
| Program and Data Flash | | | | | | |
| t_{nvmet1k} | Data retention after up to 1 K cycles | 20 | — | — | years | 1 |
| n_{nvmyc} | Cycling endurance | 1 K | — | — | cycles | 2 |
| FlexRAM as Emulated EEPROM | | | | | | |
| t_{nvmetee} | Data retention | 5 | — | — | years | 1, 3 |
| $n_{\text{nvmyree16}}$ $n_{\text{nvmyree256}}$ | Write endurance • EEPROM backup to FlexRAM used ratio = 16 • EEPROM backup to FlexRAM used ratio = 256 | 100 K 1.6 M | — — | — — | writes writes | 4, 5, 6 |

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase are supported across product temperature specification. Cycling endurance is per flash sector.
3. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.
4. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across product temperature specification. Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
5. For usage of any EEE driver other than the FlexMemory feature, the endurance specification falls back to the Data Flash endurance value of 1 K.
6. [FlexMemory calculator tool](#) is available on the NXP web site for help in estimating the maximum write endurance achievable at specific EEPROM/FlexRAM ratios. The "In Spec" portions of the online calculator refer to the NVM reliability specifications section of the data sheet. This calculator only applies to the Kinetis FlexMemory feature.

6.5.4.1.3 Reliability specifications (Industrial)

Table 29. NVM reliability specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------|--|--------|-------------------|------|--------|-------|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcyop}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| Data Flash | | | | | | |
| $t_{nvmretd10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | |
| $t_{nvmretd1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | |
| $n_{nvmcyod}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| FlexRAM as EEPROM | | | | | | |
| $t_{nvmretee100}$ | Data retention up to 100% of write endurance | 5 | 50 | — | years | |
| $t_{nvmretee10}$ | Data retention up to 10% of write endurance | 20 | 100 | — | years | |
| $n_{nvmcycee}$ | Cycling endurance for EEPROM backup | 20 K | 50 K | — | cycles | 2 |
| | Write endurance | | | | | 3 |
| $n_{nvmwree16}$ | • EEPROM backup to FlexRAM ratio = 16 | 140 K | 400 K | — | writes | |
| $n_{nvmwree128}$ | • EEPROM backup to FlexRAM ratio = 128 | 1.26 M | 3.2 M | — | writes | |
| $n_{nvmwree512}$ | • EEPROM backup to FlexRAM ratio = 512 | 5 M | 12.8 M | — | writes | |
| $n_{nvmwree2k}$ | • EEPROM backup to FlexRAM ratio = 2,048 | 20 M | 50 M | — | writes | |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.
3. Write endurance represents the number of writes to each FlexRAM location at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$ influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

6.5.4.1.4 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFE to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application.

6.5.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.5.6 Analog

6.5.6.1 ADC electrical specifications

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications. The following specification is defined with the DC-DC converter operating in Bypass mode.

6.5.6.1.1 16-bit ADC operating conditions

Table 30. 16-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------------|-------------------------------------|--|------------------------|-------------------|---------------------------------------|------------|-------|
| V_{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| ΔV_{DDA} | Supply voltage | Delta to V_{DD} ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| ΔV_{SSA} | Ground voltage | Delta to V_{SS} ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| V_{REFH} | ADC reference voltage high | | 1.13 | V_{DDA} | V_{DDA} | V | 3 |
| V_{REFL} | ADC reference voltage low | | V_{SSA} | V_{SSA} | V_{SSA} | V | 3 |
| V_{ADIN} | Input voltage | <ul style="list-style-type: none"> 16-bit differential mode All other modes | V_{SSA} V_{SSA} | — — | $31/32 \times V_{REFH}$ V_{REFH} | V | |
| C_{ADIN} | Input capacitance | <ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes | — — | 8 4 | 10 5 | pF | |
| R_{ADIN} | Input series resistance | | — | 2 | 5 | k Ω | |
| R_{AS} | Analog source resistance (external) | 13-bit / 12-bit modes $f_{ADCK} < 4$ MHz | — | — | 5 | k Ω | 4 |
| f_{ADCK} | ADC conversion clock frequency | \leq 13-bit mode | 1.0 | — | 18.0 | MHz | 5 |

Table continues on the next page...

Table 30. 16-bit ADC operating conditions (continued)

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------|--------------------------------|---|--------|-------------------|---------|------|-------|
| f_{ADCK} | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 5 |
| C_{rate} | ADC conversion rate | ≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | kS/s | 6 |
| C_{rate} | ADC conversion rate | 16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | kS/s | 6 |

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^\circ\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA} , and V_{REFL} is internally tied to V_{SSA} .
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet are derived from a system that had $< 8\ \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to $< 1\text{ ns}$.
5. To use the maximum ADC conversion clock frequency, $\text{CFG2}[\text{ADHSC}]$ must be set and $\text{CFG1}[\text{ADLPC}]$ must be clear.
6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

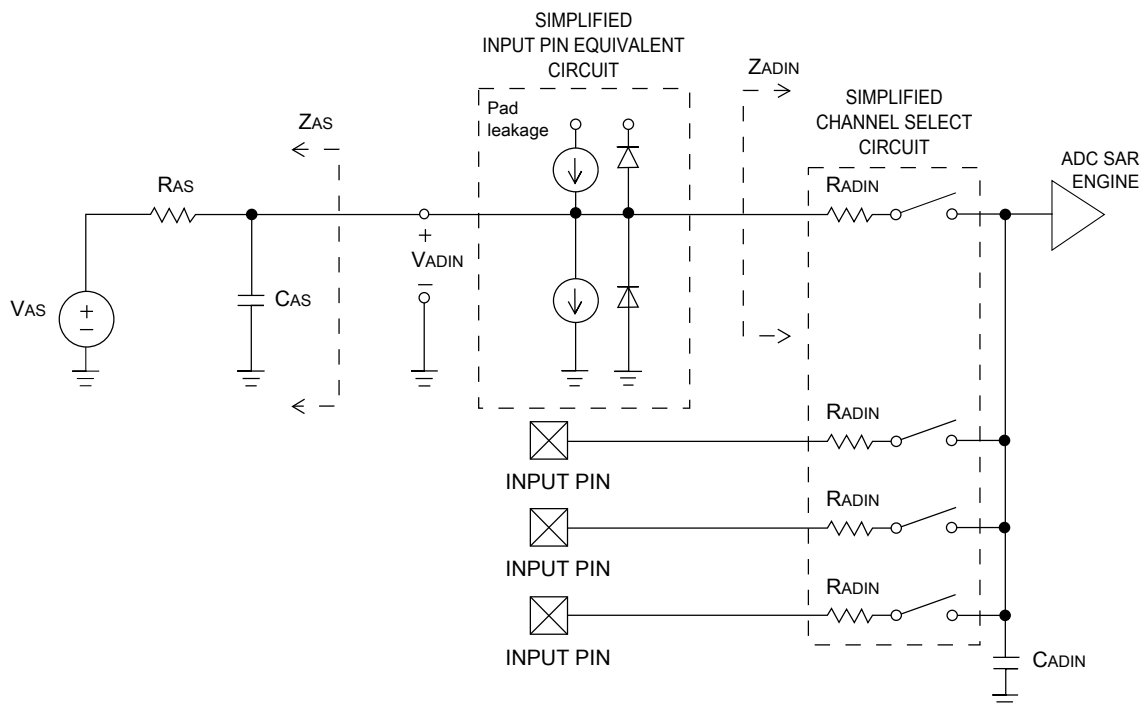


Figure 12. ADC input impedance equivalency diagram

6.5.6.1.2 16-bit ADC electrical characteristics

Table 31. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|----------------|-------------------------------|---|-------|-------------------|--------------|------------------|-----------------------------------|
| I_{DDA_ADC} | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| f_{ADACK} | ADC asynchronous clock source | <ul style="list-style-type: none"> ADLPC=1, ADHSC=0 ADLPC=1, ADHSC=1 ADLPC=0, ADHSC=0 ADLPC=0, ADHSC=1 | 1.2 | 2.4 | 3.9 | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | <ul style="list-style-type: none"> 12-bit modes <12-bit modes | — | ±4 | ±6.8 | LSB ⁴ | 5 |
| DNL | Differential non-linearity | <ul style="list-style-type: none"> 12-bit mode; Buck Mode⁶ 12-bit mode; Bypass Mode | — | ±0.7 | -1.1 to +1.9 | LSB ⁴ | 5 |
| INL | Integral non-linearity | <ul style="list-style-type: none"> 12-bit mode; Buck Mode⁶ 12-bit mode; Bypass Mode | — | ±1.0 | -2.7 to +1.9 | LSB ⁴ | 5 |
| E_{FS} | Full-scale error | <ul style="list-style-type: none"> 12-bit modes <12-bit modes | — | -4 | -5.4 | LSB ⁴ | $V_{ADIN} = V_{DDA}$ ⁵ |
| E_Q | Quantization error | <ul style="list-style-type: none"> 16-bit modes ≤13-bit modes | — | -1 to 0 | — | LSB ⁴ | |
| ENOB | Effective number of bits | 16-bit differential mode; Buck Mode ⁶ <ul style="list-style-type: none"> Avg = 32 Avg = 4 16-bit single-ended mode; Buck Mode ⁶ <ul style="list-style-type: none"> Avg = 32 Avg = 4 16-bit differential mode; Bypass Mode <ul style="list-style-type: none"> Avg = 32 Avg = 4 16-bit single-ended mode; Bypass Mode | 12 | 12.75 | — | bits | 7 |
| | | | 11.25 | 11.75 | — | | |
| | | | 11 | 11.5 | — | | |
| | | | 9.5 | 10.5 | — | | |
| | | | 12.5 | 13 | — | | |
| | | | 11.25 | 12 | — | | |
| | | | 11 | 11.75 | — | | |

Table continues on the next page...

Table 31. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|-----------------|--|---|------------------------|-------------------|------|-------|--|
| | | <ul style="list-style-type: none"> Avg = 32 Avg = 4 | 10 | 10.5 | — | | |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode; Buck Mode ⁶ <ul style="list-style-type: none"> Avg = 32 | — | −90 | — | dB | 8 |
| | | 16-bit single-ended mode; Buck Mode ⁶ <ul style="list-style-type: none"> Avg = 32 | — | −88 | — | | |
| | | 16-bit differential mode; Bypass Mode <ul style="list-style-type: none"> Avg = 32 | — | −89 | — | | |
| | | 16-bit single-ended mode; Bypass Mode <ul style="list-style-type: none"> Avg = 32 | — | −87 | — | | |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | |
| SFDR | Spurious free dynamic range distortion | 16-bit differential mode; Buck Mode ⁶ <ul style="list-style-type: none"> Avg = 32 | 85 | 89 | — | dB | 8 |
| | | 16-bit single-ended mode; Buck Mode ⁶ <ul style="list-style-type: none"> Avg = 32 | 85 | 87 | — | | |
| | | 16-bit differential mode; Bypass Mode <ul style="list-style-type: none"> Avg = 32 | 87 | 94 | — | | |
| | | 16-bit single-ended mode; Bypass Mode <ul style="list-style-type: none"> Avg = 32 | 85 | 88 | — | | |
| E _{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I _{in} = leakage current (see Voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.67 | 1.74 | 1.81 | mV/°C | 9 |

Table continues on the next page...

Table 31. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|--------------|---------------------|-------------------------|------|-------------------|------|------|-------|
| V_{TEMP25} | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 9 |

- All accuracy numbers assume that the ADC is calibrated with $V_{REFH} = V_{DDA}$.
- Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low-power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$.
- ADC conversion clock < 16 MHz, maximum hardware averaging (AVGE = %1, AVGS = %11).
- V_{REFH} = Output of Voltage Reference(VREF).
- Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- ADC conversion clock < 3 MHz.

6.5.6.2 Voltage reference electrical specifications

Table 32. VREF full-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|-------------------------|------------|------|------|-------|
| V_{DDA} | Supply voltage | 1.71 | 3.6 | V | |
| T_A | Temperature | -40 to 105 | | °C | |
| C_L | Output load capacitance | 100 | | nF | 1, 2 |

- C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
- The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 33. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------|---|--------|--------|--------|------|-------|
| V_{out} | Voltage reference output with factory trim at nominal V_{DDA} and temperature=25 °C | 1.190 | 1.1950 | 1.2 | V | 1 |
| V_{out} | Voltage reference output with user trim at nominal V_{DDA} and temperature=25 °C | 1.1945 | 1.1950 | 1.1955 | V | 1 |
| V_{step} | Voltage reference trim step | — | 0.5 | — | mV | 1 |
| V_{tdrift} | Temperature drift ($V_{max} - V_{min}$ across the full temperature range) | — | — | 20 | mV | 1 |
| I_{bg} | Bandgap only current | — | — | 80 | μA | |
| I_{lp} | Low-power buffer current | — | — | 360 | uA | 1 |
| I_{hp} | High-power buffer current | — | — | 1 | mA | 1 |
| ΔV_{LOAD} | Load regulation | | | | μV | 1, 2 |

Table continues on the next page...

Table 33. VREF full-range operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------------------|--|------|------|------|---------------|-------|
| | • current = ± 1.0 mA | — | 200 | — | | |
| T_{stup} | Buffer startup time | — | — | 100 | μs | |
| $T_{\text{chop_osc_st up}}$ | Internal bandgap start-up delay with chop oscillator enabled | — | — | 35 | ms | |
| V_{vdrift} | Voltage drift ($V_{\text{max}} - V_{\text{min}}$ across the full voltage range) | — | 2 | — | mV | 1 |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 34. VREF limited-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|--------------------|-------|
| T_A | Temperature | 0 | 70 | $^{\circ}\text{C}$ | |

Table 35. VREF limited-range operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|---------------------|---|------|------|------|-------|
| V_{tdrift} | Temperature drift ($V_{\text{max}} - V_{\text{min}}$ across the limited temperature range) | — | 15 | mV | |

6.5.6.3 CMP and 6-bit DAC electrical specifications

Table 36. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|--|-----------------------|---------------------|------------------|----------------------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V |
| I_{DDHS} | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | μA |
| $I_{\text{DDL S}}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | μA |
| V_{AIN} | Analog input voltage | $V_{\text{SS}} - 0.3$ | — | V_{DD} | V |
| V_{AIO} | Analog input offset voltage | — | — | 20 | mV |
| V_{H} | Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 | — | 5 10 20 30 | — — — — | mV mV mV mV |
| V_{CMPOh} | Output high | $V_{\text{DD}} - 0.5$ | — | — | V |
| V_{CMPOI} | Output low | — | — | 0.5 | V |

Table continues on the next page...

Table 36. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-------------|---|------|------|------|------------------|
| t_{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| t_{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay ² | — | — | 40 | μ s |
| I_{DAC6b} | 6-bit DAC current adder (enabled) | — | 7 | — | μ A |
| INL | 6-bit DAC integral non-linearity | -0.5 | — | 0.5 | LSB ³ |
| DNL | 6-bit DAC differential non-linearity | -0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

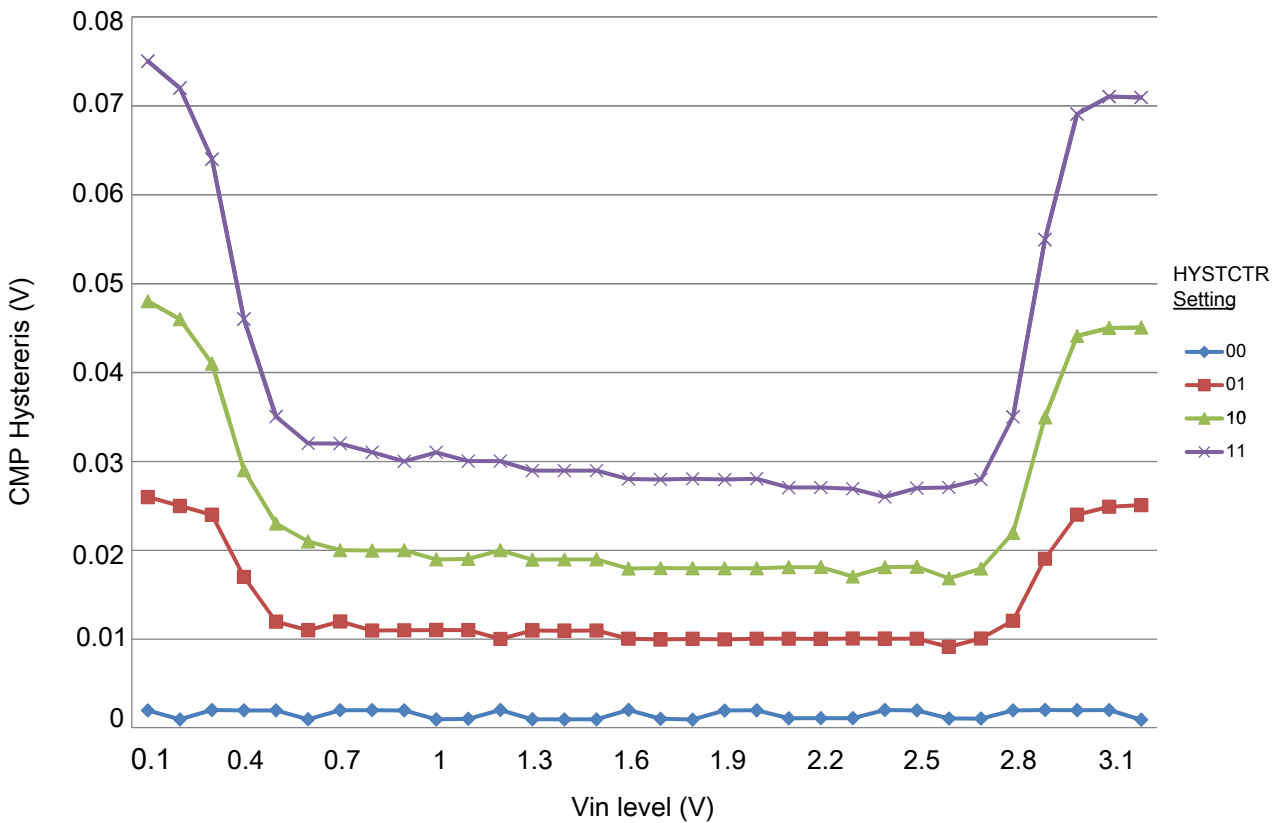


Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

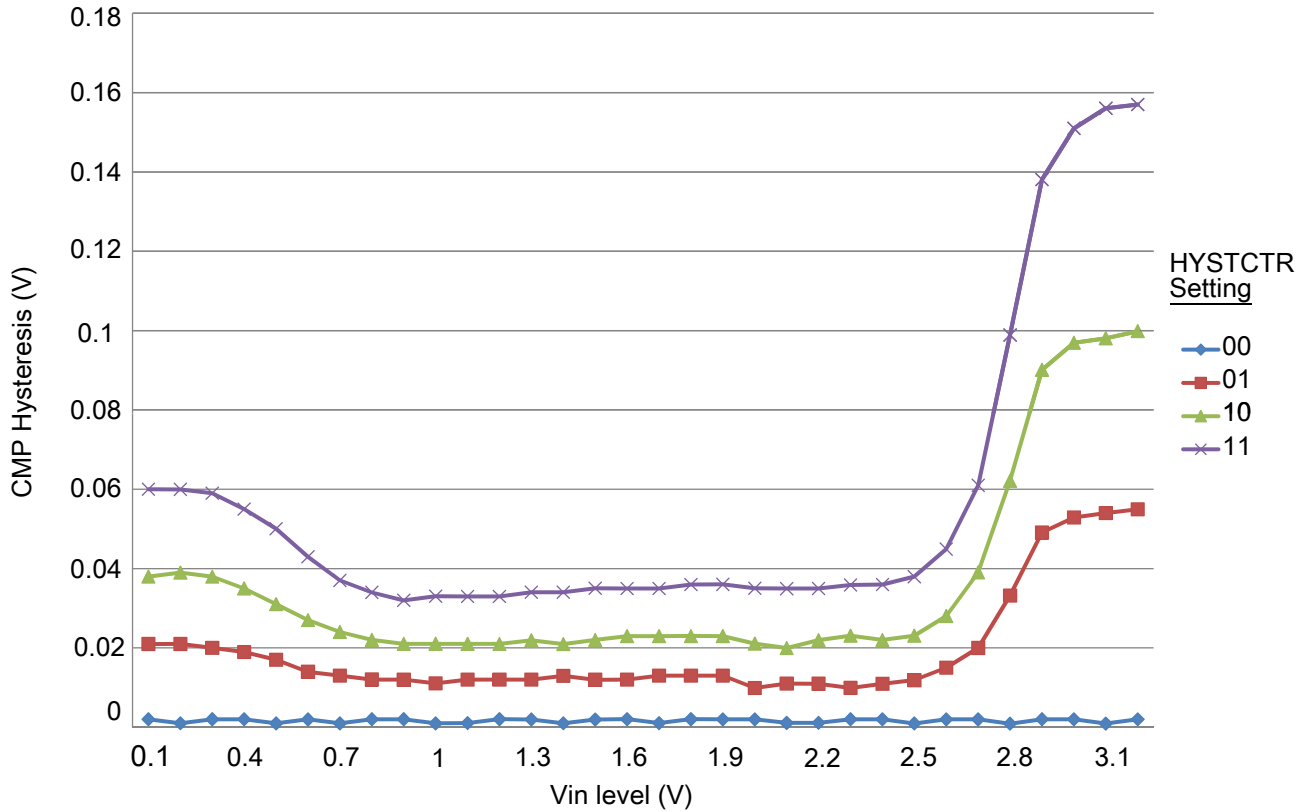


Figure 14. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.5.7 Timers

See [General switching specifications](#).

6.5.8 Communication interfaces

6.5.8.1 CAN switching specifications

See [General switching specifications](#).

6.5.8.2 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. See the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 37. Master mode DSPI timing (limited voltage range)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|-------------------------------------|--------------------------|-------------------|------|-------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 12 | MHz | |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns | |
| DS3 | DSPI_PCSn valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 2$ | — | ns | 1 |
| DS4 | DSPI_SCK to DSPI_PCSn invalid delay | $(t_{BUS} \times 2) - 2$ | — | ns | 2 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 8.5 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -2 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 16.2 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The delay is programmable in SPIx_CTARn[PCSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

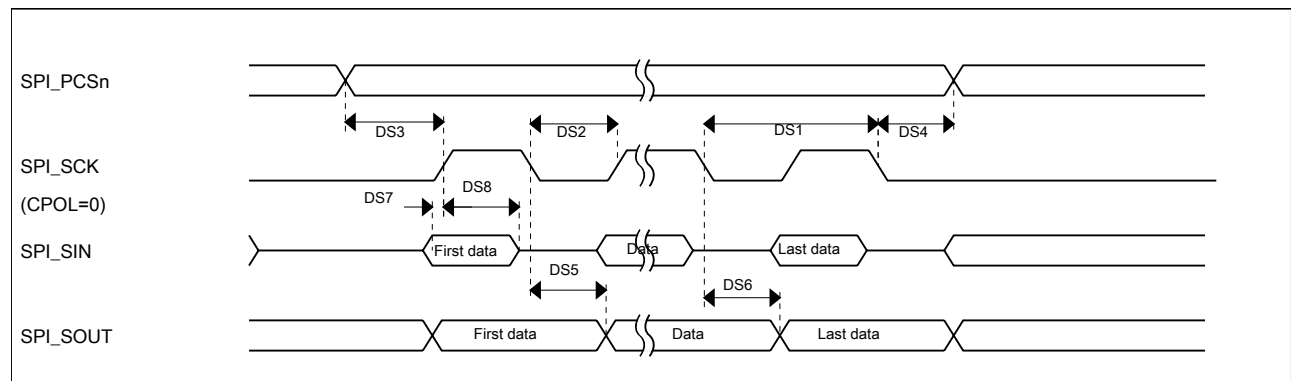


Figure 15. DSPI classic SPI timing — master mode

Table 38. Slave mode DSPI timing (limited voltage range)

| Num | Description | Min. | Max. | Unit |
|-----|------------------------|------|------|------|
| | Operating voltage | 2.7 | 3.6 | V |
| | Frequency of operation | | 6 | MHz |

Table continues on the next page...

Table 38. Slave mode DSPI timing (limited voltage range) (continued)

| Num | Description | Min. | Max. | Unit |
|------|--|--------------------|-------------------|------|
| DS9 | DSPI_SCK input cycle time | $4 \times t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 21.4 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.6 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7.0 | — | ns |
| DS15 | DSPI_SS active to DSPI_SOUT driven | — | 14 | ns |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | — | 14 | ns |

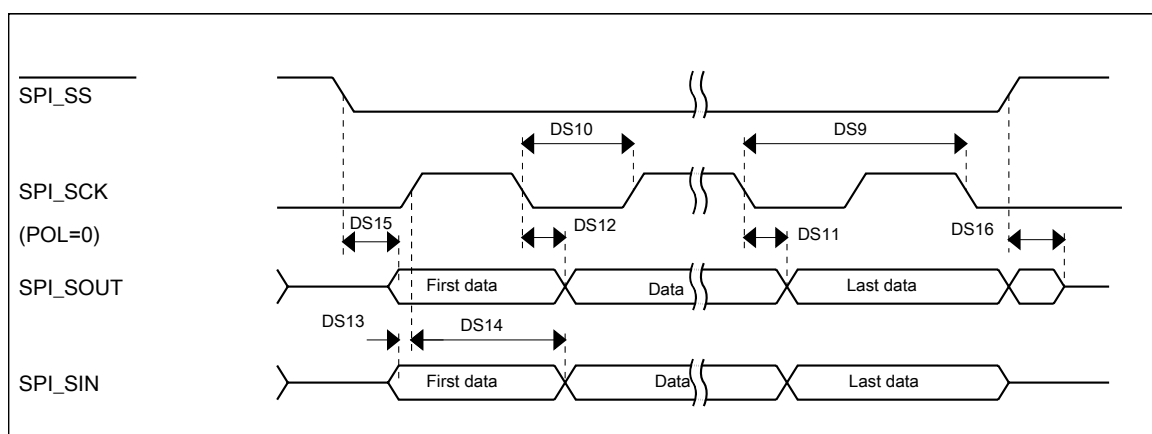


Figure 16. DSPI classic SPI timing — slave mode

6.5.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. See the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 39. Master mode DSPI timing (full voltage range)

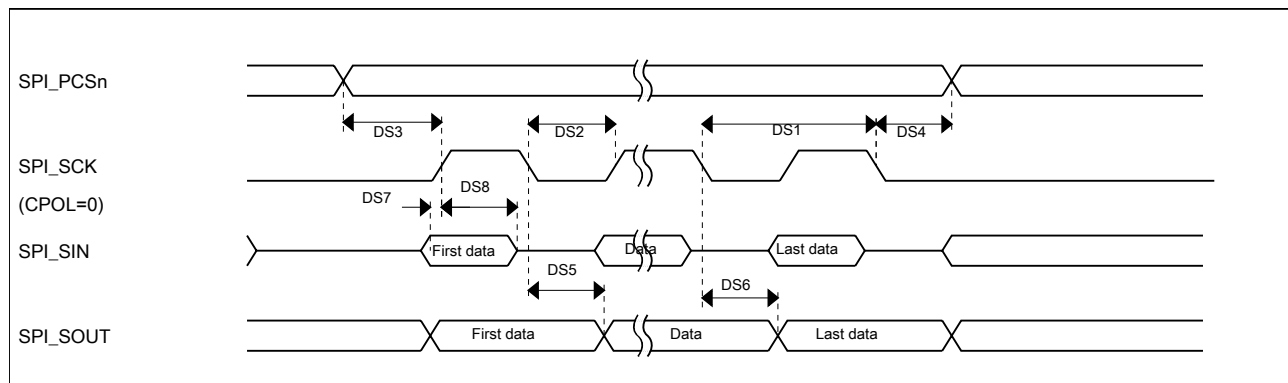
| Num | Description | Min. | Max. | Unit | Notes |
|-----|-------------------------------|--------------------|-------------------|------|-------|
| | Operating voltage | 1.71 | 3.6 | V | 1 |
| | Frequency of operation | — | 12 | MHz | |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | — | ns | |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns | |

Table continues on the next page...

Table 39. Master mode DSPI timing (full voltage range) (continued)

| Num | Description | Min. | Max. | Unit | Notes |
|-----|-------------------------------------|--------------------------|------|------|-------|
| DS3 | DSPI_PCSn valid to DSPI_SCK delay | $(t_{BUS} \times 2) - 4$ | — | ns | 2 |
| DS4 | DSPI_SCK to DSPI_PCSn invalid delay | $(t_{BUS} \times 2) - 4$ | — | ns | 3 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | 10 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -1.2 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 23.3 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | — | ns | |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PCSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

**Figure 17. DSPI classic SPI timing — master mode****Table 40. Slave mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit |
|------|---|--------------------|-------------------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 6 | MHz |
| DS9 | DSPI_SCK input cycle time | $4 \times t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 29.1 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 3.2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7.0 | — | ns |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | — | 25 | ns |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | — | 25 | ns |

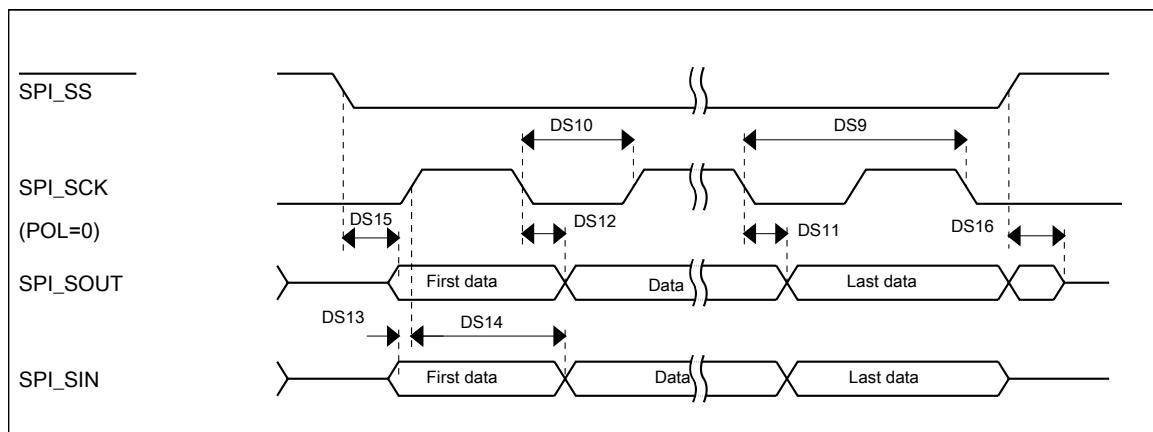


Figure 18. DSPI classic SPI timing — slave mode

6.5.8.4 Inter-Integrated Circuit Interface (I²C) timing

Table 41. I²C timing

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|--|----------------------|------------------|-------------------|--|------------------|------|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | f _{SCL} | 0 | 100 | 0 | 400 | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | t _{HD; STA} | 4 | — | 0.6 | — | μs |
| LOW period of the SCL clock | t _{LOW} | 4.7 | — | 1.3 | — | μs |
| HIGH period of the SCL clock | t _{HIGH} | 4 | — | 0.6 | — | μs |
| Set-up time for a repeated START condition | t _{SU; STA} | 4.7 | — | 0.6 | — | μs |
| Data hold time for I ² C bus devices | t _{HD; DAT} | 0 ¹ | 3.45 ² | 0 ³ | 0.9 ¹ | μs |
| Data set-up time | t _{SU; DAT} | 250 ⁴ | — | 100 ^{2, 5} | — | ns |
| Rise time of SDA and SCL signals | t _r | — | 1000 | 20 + 0.1C _b ^{5, 6} | 300 | ns |
| Fall time of SDA and SCL signals | t _f | — | 300 | 20 + 0.1C _b ^{5, 6} | 300 | ns |
| Set-up time for STOP condition | t _{SU; STO} | 4 | — | 0.6 | — | μs |
| Bus free time between STOP and START condition | t _{BUF} | 4.7 | — | 1.3 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t _{SP} | N/A | N/A | 0 | 50 | ns |

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum t_{HD; DAT} must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF.
4. Set-up time in slave-transmitter mode is 1 IP Bus clock period, if the TX FIFO is empty.

5. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement $t_{SU; DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

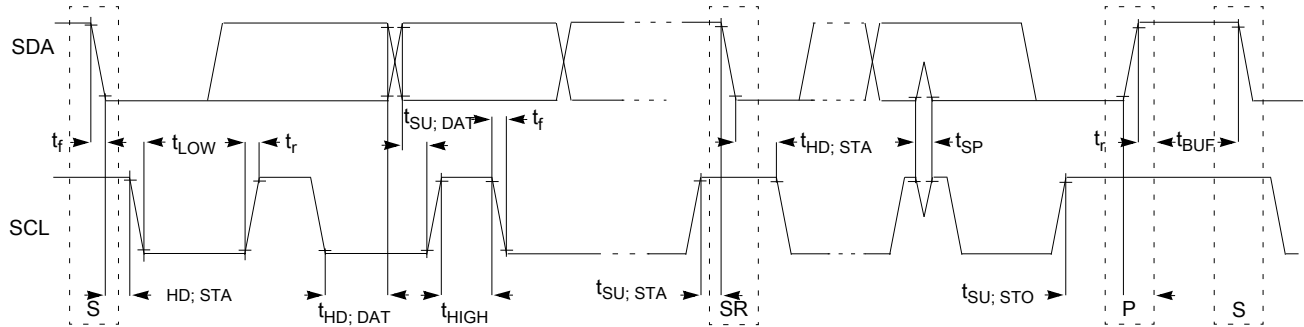


Figure 19. Timing definition for fast and standard mode devices on the I²C bus

6.5.8.5 LPUART

See [General switching specifications](#).

6.5.9 Human-machine interfaces (HMI)

6.5.9.1 GPIO

The maximum input voltage on PTC0/1/2/3 is VDD+0.3V. For rest of the GPIO specification, see [General switching specifications](#).

6.6 DC-DC Converter Operating Requirements

Table 42. DC-DC Converter operating conditions

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---|-------|-----|-----|------|
| Bypass Mode Supply Voltage (RF and Analog) | VDD _{RF1} , VDD _{RF2} , VDD _{RF3} , VDD _{1P5} | 1.425 | — | 3.6 | Vdc |
| Bypass Mode Supply Voltage (Digital) | VDD _X , V _{DCDC_IN} , VDD _A | 1.71 | — | 3.6 | Vdc |
| Buck Mode Supply Voltage ^{1, 2} | V _{DCDC_IN} | 2.1 | — | 3.6 | Vdc |
| DC-DC Inductor | | | | | |
| Value | | — | 10 | — | μH |

Table continues on the next page...

Table 42. DC-DC Converter operating conditions (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|------|------|------|
| ESR | | — | <0.2 | <0.5 | Ohms |

- In Buck mode, DC-DC converter needs 2.1 V minimum to start, the supply can drop to 1.8 V after DC-DC converter settles.
- In Buck mode, DC-DC converter generates 1.8 V at VDD_1P8OUT and 1.5 V at VDD_1P5OUT_PMCIN pins. VDD_1P8OUT should supply to VDD₁, VDD₂ and VDD_A. VDD_1P5OUT_PMCIN should supply to VDD_RF₁ and VDD_RF₂. VDD_RF₃ can be either supplied by 1.5 V or 1.8 V.

Table 43. DC-DC Converter Specifications

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|--|--|-------------------------------|------|------------------|---|------|
| DC-DC Converter Output Power (total power output of 1p8V and 1p5V) | V _{DCDC_IN} above 2.7 V | Pdcdc_out1 | — | — | 195 ¹ | mW |
| | V _{DCDC_IN} below 2.7 V | Pdcdc_out2 | — | — | 140 ¹ | mW |
| Switching Frequency ² | | DCDC_FREQ | — | 2 | — | MHz |
| Half FET Threshold | | I_half_FET | — | 5 | — | mA |
| Double FET Threshold | | I_double_FET | — | 40 | — | mA |
| Buck Mode | | | | | | |
| DC-DC Conversion Efficiency | | DCDC_EFF_buck | — | 90% | — | — |
| 1.8 V Output Voltage | | VDD_1P8_buck | 1.71 | — | min(VDCDC_IN_buck, 3.5) ^{3, 4} | Vdc |
| 1.8 V Output Current ^{5, 6} | VDD_1P8 = 3.0 V 1.5 V ≤ VDC_1P5 ≤ 1.7 V V _{DCDC_IN} =3.1 V | IDD_1P8_buck1 | — | — | 39 | mA |
| | VDD_1P8 = 2.65 V 1.5 V ≤ VDC_1P5 ≤ 1.7 V V _{DCDC_IN} =2.7 V | IDD_1P8_buck2 | — | — | 45 | mA |
| | VDD_1P8 = 1.8 V 1.5 V ≤ VDC_1P5 ≤ 1.7 V V _{DCDC_IN} =2.1 V | IDD_1P8_buck3 | — | — | 35 | mA |
| 1.5 V Output Voltage | Consumed by Radio | VDD_1P5_buck | 1.5 | — ⁷ | 1.8 | Vdc |
| 1.5 V Output Current ^{5, 8} | | IDD_1P5_buck | — | — | 45 | mA |
| DC-DC Transition Operating Behavior | LSS→Run | t_DCDCbuck_LSS→RUN | — | 50 | — | μs |
| DC-DC Turn on Time | | T _{DCDC_ON} | — | 2.2 ⁹ | — | ms |
| DC-DC Settling Time for increasing voltage | | T _{DCDC_SETTLE_buck} | — | 3.11 | — | ms/V |

Table continues on the next page...

Table 43. DC-DC Converter Specifications (continued)

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|--|--|--------------------------|-----|------------------|-----|------|
| DC-DC Settling Time for decreasing voltage | C = capacitance attached to the DC-DC V1P8 output rail. V1 = the initial output voltage of the DC-DC V2 = the final output voltage of the DC-DC I2 = the load on the DC-DC output expressed in Amperes. | $T_{DCDC_SETTLE_buck}$ | — | $(C*(V1-V2)/I2)$ | — | s |

1. This is the steady state DC output power. Excessive transient current load from external device will cause 1p8V and 1P5 output voltage unregulated temporary.
2. This is the frequency that is observed at LN and LP pins.
3. The voltage output level can be controlled by programming DCDC_VDD1P8CTRL_TRG field in DCDC_REG3.
4. In Buck mode, the maximum VDD_1P8 output is the minimum of either VDCDC_IN_BUCK minus 50 mV or 3.5 V. For example, if VDCDC_IN = 2.1 V, maximum VDD_1P8 is 2.05 V. If VDCDC_IN = 3.6 V, maximum VDD_1P8 is 3.5 V.
5. The output current specification in buck mode represents the maximum current the DC-DC converter can deliver. The KW39/38/37 radio and MCU blocks current consumption is not excluded. The maximum output power of the DC-DC converter is 140 mW when V_{DCDC_IN} is below 2.7 V and 195 mW when V_{DCDC_IN} is above 2.7 V. The available supply current for external device depends on the energy consumed by the internal peripherals in KW39/38/37.
6. When using DC-DC in low-power mode (pulsed mode), current load must be less than 1 mA.
7. User needs to program DCDC_VDD1P5CTRL_TRG_BUCK field in DCDC_REG3 register to ensure that a worst case minimum of 1.5 V is available as VDD_1P5_buck. VDD_1P5 must not be programmed higher than VDD_1P8.
8. 1.5 V is intended to supply power to KW39/38/37. It is not designed to supply power to an external device.
9. Turn on time is measured from the application of power (to DCDC_IN) till the DCDC_REG0[DCDC_STS_DC_OK] bit is set. Code execution may begin before the DCDC_REG0[DCDC_STS_DC_OK] bit is set. The full device specification is not guaranteed until the bit sets.

6.7 Ratings

6.7.1 Thermal handling ratings

Table 44. Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|-------------------------------|------|------|------|-------|
| T_{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T_{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.7.2 Moisture handling ratings

Table 45. Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.7.3 ESD handling ratings

Table 46. ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V_{HBM} | Electrostatic discharge voltage, human body model | −2000 | +2000 | V | 1 |
| V_{CDM} | Electrostatic discharge voltage, charged-device model | | | | 2 |
| | All pins except the corner pins | −500 | 500 | V | |
| | Corner pins only | −750 | 750 | V | |
| I_{LAT} | Latch-up current at ambient temperature of 105 °C | −100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JS001, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JS002, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

6.7.4 Voltage and current operating ratings

Table 47. Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|-----------------------|---|-----------------------|-----------------------|------|
| V_{DD} | Digital supply voltage | −0.3 | 3.8 | V |
| I_{DD} | Digital supply current | — | 120 | mA |
| V_{IO} | IO pin input voltage | −0.3 | $V_{\text{DD}} + 0.3$ | V |
| I_{D} | Instantaneous maximum current single pin limit (applies to all port pins) | −25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{\text{DD}} - 0.3$ | $V_{\text{DD}} + 0.3$ | V |
| $V_{\text{IO_DCDC}}$ | IO pins in the DC-DC voltage domain (DCDC_CFG and PSWITCH) | GND | VDCDC | V |

7 Pin Diagrams and Pin Assignments

7.1 KW39/37 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control and Interrupt module is used to select the functionality for each GPIO pin. ALT0 is reserved for analog functions on some GPIO pins. ALT1 – ALT9 are assigned to the available digital functions on each GPIO pin. GPIO pins with a default of “disabled” are high impedance after reset – their input and output buffers are disabled.

| 48 "Wett able" HVQ FN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | ALT8 | ALT9 |
|-----------------------------------|---------------------------|---------------------------|---------------------------|--------------------------------------|-----------|----------|----------|----------------|------|---------|------|------|
| 1 | PTA0 | SWD_DIO | | PTA0/ RF_ACTIVE | SPI0_PCS1 | | | TPM1_CH0 | | SWD_DIO | | |
| 2 | PTA1 | SWD_CLK | | PTA1/ RF_ STATUS | SPI1_PCS0 | | | TPM1_CH1 | | SWD_CLK | | |
| 3 | PTA2 | RESET_b | | PTA2 | | | | TPM0_CH3 | | RESET_b | | |
| 4 | PTA16 | DISABLED | | PTA16/ LLWU_P4 | SPI1_SOUT | | | TPM0_CH0 | | | | |
| 5 | PTA17 | DISABLED | | PTA17/ LLWU_P5 | SPI1_SIN | | | TPM_ CLKIN1 | | | | |
| 6 | PTA18 | DISABLED | | PTA18/ LLWU_P6 | SPI1_SCK | | | TPM2_CH0 | | | | |
| 7 | PTA19 | ADC0_SE5 | ADC0_SE5 | PTA19/ LLWU_P7 | SPI1_PCS0 | | | TPM2_CH1 | | | | |
| 8 | PSWITCH | PSWITCH | PSWITCH | | | | | | | | | |
| 9 | DCDC_ CFG/ VDCDC_IN | DCDC_ CFG/ VDCDC_IN | DCDC_ CFG/ VDCDC_IN | | | | | | | | | |
| 10 | DCDC_LP | DCDC_LP | DCDC_LP | | | | | | | | | |
| 11 | DCDC_GND | DCDC_GND | DCDC_GND | | | | | | | | | |
| 12 | DCDC_LN | DCDC_LN | DCDC_LN | | | | | | | | | |
| 13 | VDD_ 1P8OUT | VDD_ 1P8OUT | VDD_ 1P8OUT | | | | | | | | | |
| 14 | DCDC_LN | DCDC_LN | DCDC_LN | | | | | | | | | |
| 15 | VDD_ 1P5OUT_ PM CIN | VDD_ 1P5OUT_ PM CIN | VDD_ 1P5OUT_ PM CIN | | | | | | | | | |
| 16 | PTB0 | DISABLED | | PTB0/ LLWU_P8/ RF_ RFOSC_EN | | I2C0_SCL | CMPO_OUT | TPM0_CH1 | | CLKOUT | | |

Pin Diagrams and Pin Assignments

| 48 "Wett able" HVQ FN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | ALT8 | ALT9 |
|-----------------------------------|--------------------|-----------------------|-----------------------|---|---------------|----------|-------------------|----------|------|----------------|-----------|------|
| 17 | PTB1 | ADC0_SE1/ CMP0_IN5 | ADC0_SE1/ CMP0_IN5 | PTB1/ RF_ PRIORITY | DTM_RX | I2C0_SDA | LPTMR0_ ALT1 | TPM0_CH2 | | CMT_IRO | | |
| 18 | PTB2 | ADC0_SE3/ CMP0_IN3 | ADC0_SE3/ CMP0_IN3 | PTB2/ RF_NOT_ ALLOWED/ LLWU_P9 | | DTM_TX | TPM0_CH0 | TPM1_CH0 | | | TPM2_CH0 | |
| 19 | PTB3 | ADC0_SE2/ CMP0_IN4 | ADC0_SE2/ CMP0_IN4 | PTB3/ ERCLK32K/ RF_ACTIVE | | TPM0_CH1 | CLKOUT | TPM1_CH1 | | RTC_ CLKOUT | TPM2_CH1 | |
| 20 | VDD_0 | VDD_0 | VDD_0 | | | | | | | | | |
| 21 | PTB16 | EXTAL32K | EXTAL32K | PTB16 | | I2C1_SCL | | TPM2_CH0 | | | | |
| 22 | PTB17 | XTAL32K | XTAL32K | PTB17 | | I2C1_SDA | | TPM2_CH1 | | | | |
| 23 | PTB18 | NMI_b | ADC0_SE4/ CMP0_IN2 | PTB18 | | I2C1_SCL | TPM_ CLKIN0 | TPM0_CH0 | | NMI_b | | |
| 24 | ADC0_DP0 | ADC0_DP0/ CMP0_IN0 | ADC0_DP0/ CMP0_IN0 | | | | | | | | | |
| 25 | ADC0_DM0 | ADC0_DM0/ CMP0_IN1 | ADC0_DM0/ CMP0_IN1 | | | | | | | | | |
| 26 | VREFL/ VSSA | VREFL/ VSSA | VREFL/ VSSA | | | | | | | | | |
| 27 | VREFH/ VREF_OUT | VREFH/ VREF_OUT | VREFH/ VREF_OUT | | | | | | | | | |
| 28 | VDDA | VDDA | VDDA | | | | | | | | | |
| 29 | XTAL_OUT | XTAL_OUT | XTAL_OUT | | | | | | | | | |
| 30 | EXTAL | EXTAL | EXTAL | | | | | | | | | |
| 31 | XTAL | XTAL | XTAL | | | | | | | | | |
| 32 | VDD_RF3 | VDD_RF3 | VDD_RF3 | | | | | | | | | |
| 33 | ANT | ANT | ANT | | | | | | | | | |
| 34 | GANT | GANT | GANT | | | | | | | | | |
| 35 | VDD_RF2 | VDD_RF2 | VDD_RF2 | | | | | | | | | |
| 36 | VDD_RF1 | VDD_RF1 | VDD_RF1 | | | | | | | | | |
| 37 | PTC1 | DISABLED | | PTC1/ RF_EARLY_ WARNING | ANT_B | I2C0_SDA | LPUART0_ RTS_b | TPM0_CH2 | | | SPI1_SCK | |
| 38 | PTC2 | DISABLED | | PTC2/ LLWU_P10 | TX_ SWITCH | I2C1_SCL | LPUART0_ RX | CMT_IRO | | DTM_RX | SPI1_SOUT | |
| 39 | PTC3 | DISABLED | | PTC3/ LLWU_P11 | RX_ SWITCH | I2C1_SDA | LPUART0_ TX | TPM0_CH1 | | DTM_TX | SPI1_SIN | |
| 40 | PTC4 | DISABLED | | PTC4/ LLWU_P12/ RF_ACTIVE | ANT_A | EXTRG_IN | LPUART0_ CTS_b | TPM1_CH0 | | I2C0_SCL | SPI1_PCS0 | |

| 48 "Wett able" HVQ FN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | ALT8 | ALT9 |
|-----------------------------------|----------|----------|-------|--|-----------|-----------------|-------------------|----------|------|--------|------|------|
| 41 | PTC5 | DISABLED | | PTC5/ LLWU_P13/ RF_NOT_ ALLOWED/ RF_ PRIORITY | | LPTMR0_ ALT2 | LPUART0_ RTS_b | TPM1_CH1 | | | | |
| 42 | PTC6 | DISABLED | | PTC6/ LLWU_P14/ RF_ RFOSC_EN | | I2C1_SCL | LPUART0_ RX | TPM2_CH0 | | | | |
| 43 | PTC7 | DISABLED | | PTC7/ LLWU_P15 | SPI0_PCS2 | I2C1_SDA | LPUART0_ TX | TPM2_CH1 | | | | |
| 44 | VDD_1 | VDD_1 | VDD_1 | | | | | | | | | |
| 45 | PTC16 | DISABLED | | PTC16/ LLWU_P0/ RF_ STATUS | SPI0_SCK | I2C0_SDA | LPUART0_ RTS_b | TPM0_CH3 | | | | |
| 46 | PTC17 | DISABLED | | PTC17/ LLWU_P1/ RF_EXT_ OSC_EN | SPI0_SOUT | I2C1_SCL | LPUART0_ RX | | | DTM_RX | | |
| 47 | PTC18 | DISABLED | | PTC18/ LLWU_P2 | SPI0_SIN | I2C1_SDA | LPUART0_ TX | | | DTM_TX | | |
| 48 | PTC19 | DISABLED | | PTC19/ LLWU_P3/ RF_EARLY_ WARNING | SPI0_PCS0 | I2C0_SCL | LPUART0_ CTS_b | | | | | |
| 49 | Ground | NA | | | | | | | | | | |

7.2 KW38 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control and Interrupt module is used to select the functionality for each GPIO pin. ALT0 is reserved for analog functions on some GPIO pins. ALT1 – ALT9 are assigned to the available digital functions on each GPIO pin. GPIO pins with a default of “disabled” are high impedance after reset – their input and output buffers are disabled.

Pin Diagrams and Pin Assignments

| 48 "Wett able" HVQ FN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | ALT8 | ALT9 |
|-----------------------------------|---------------------------|---------------------------|---------------------------|---|-------------------|-------------------|-----------------|----------------|------|----------------|----------|------|
| 1 | PTA0 | SWD_DIO | | PTA0/ RF_ACTIVE | SPI0_PCS1 | | | TPM1_CH0 | | SWD_DIO | | |
| 2 | PTA1 | SWD_CLK | | PTA1/ RF_STATUS | SPI1_PCS0 | | | TPM1_CH1 | | SWD_CLK | | |
| 3 | PTA2 | RESET_b | | PTA2 | | | | TPM0_CH3 | | RESET_b | | |
| 4 | PTA16 | DISABLED | | PTA16/ LLWU_P4 | SPI1_SOUT | LPUART1_ RTS_b | | TPM0_CH0 | | | | |
| 5 | PTA17 | DISABLED | | PTA17/ LLWU_P5 | SPI1_SIN | LPUART1_ RX | CAN0_TX | TPM_ CLKIN1 | | | | |
| 6 | PTA18 | DISABLED | | PTA18/ LLWU_P6 | SPI1_SCK | LPUART1_ TX | CAN0_RX | TPM2_CH0 | | | | |
| 7 | PTA19 | ADC0_SE5 | ADC0_SE5 | PTA19/ LLWU_P7 | SPI1_PCS0 | LPUART1_ CTS_b | | TPM2_CH1 | | | | |
| 8 | PSWITCH | PSWITCH | PSWITCH | | | | | | | | | |
| 9 | DCDC_CFG/ VDCDC_IN | DCDC_CFG/ VDCDC_IN | DCDC_CFG/ VDCDC_IN | | | | | | | | | |
| 10 | DCDC_LP | DCDC_LP | DCDC_LP | | | | | | | | | |
| 11 | DCDC_GND | DCDC_GND | DCDC_GND | | | | | | | | | |
| 12 | DCDC_LN | DCDC_LN | DCDC_LN | | | | | | | | | |
| 13 | VDD_ 1P8OUT | VDD_ 1P8OUT | VDD_ 1P8OUT | | | | | | | | | |
| 14 | DCDC_LN | DCDC_LN | DCDC_LN | | | | | | | | | |
| 15 | VDD_ 1P5OUT_ PM CIN | VDD_ 1P5OUT_ PM CIN | VDD_ 1P5OUT_ PM CIN | | | | | | | | | |
| 16 | PTB0 | DISABLED | | PTB0/ LLWU_P8/ RF_ RFOSC_EN | | I2C0_SCL | CMP0_OUT | TPM0_CH1 | | CLKOUT | CAN0_TX | |
| 17 | PTB1 | ADC0_SE1/ CMP0_IN5 | ADC0_SE1/ CMP0_IN5 | PTB1/ RF_ PRIORITY | DTM_RX | I2C0_SDA | LPTMR0_ ALT1 | TPM0_CH2 | | CMT_IRO | CAN0_RX | |
| 18 | PTB2 | ADC0_SE3/ CMP0_IN3 | ADC0_SE3/ CMP0_IN3 | PTB2/ RF_NOT_ ALLOWED/ LLWU_P9 | | DTM_TX | TPM0_CH0 | TPM1_CH0 | | | TPM2_CH0 | |
| 19 | PTB3 | ADC0_SE2/ CMP0_IN4 | ADC0_SE2/ CMP0_IN4 | PTB3/ ERCLK32K/ RF_ACTIVE | LPUART1_ RTS_b | TPM0_CH1 | CLKOUT | TPM1_CH1 | | RTC_ CLKOUT | TPM2_CH1 | |
| 20 | VDD_0 | VDD_0 | VDD_0 | | | | | | | | | |
| 21 | PTB16 | EXTAL32K | EXTAL32K | PTB16 | LPUART1_ RX | I2C1_SCL | | TPM2_CH0 | | | | |
| 22 | PTB17 | XTAL32K | XTAL32K | PTB17 | LPUART1_ TX | I2C1_SDA | | TPM2_CH1 | | | | |

Pin Diagrams and Pin Assignments

| 48 "Wett able" HVQ FN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | ALT8 | ALT9 |
|-----------------------------------|--------------------|-----------------------|-----------------------|--|-------------------|-----------------|-------------------|----------|------|----------|-----------|---------|
| 23 | PTB18 | NMI_b | ADC0_SE4/ CMP0_IN2 | PTB18 | LPUART1_ CTS_b | I2C1_SCL | TPM_ CLKIN0 | TPM0_CH0 | | NMI_b | | |
| 24 | ADC0_DP0 | ADC0_DP0/ CMP0_IN0 | ADC0_DP0/ CMP0_IN0 | | | | | | | | | |
| 25 | ADC0_DM0 | ADC0_DM0/ CMP0_IN1 | ADC0_DM0/ CMP0_IN1 | | | | | | | | | |
| 26 | VREFL/ VSSA | VREFL/ VSSA | VREFL/ VSSA | | | | | | | | | |
| 27 | VREFH/ VREF_OUT | VREFH/ VREF_OUT | VREFH/ VREF_OUT | | | | | | | | | |
| 28 | VDDA | VDDA | VDDA | | | | | | | | | |
| 29 | XTAL_OUT | XTAL_OUT | XTAL_OUT | | | | | | | | | |
| 30 | EXTAL | EXTAL | EXTAL | | | | | | | | | |
| 31 | XTAL | XTAL | XTAL | | | | | | | | | |
| 32 | VDD_RF3 | VDD_RF3 | VDD_RF3 | | | | | | | | | |
| 33 | ANT | ANT | ANT | | | | | | | | | |
| 34 | GANT | GANT | GANT | | | | | | | | | |
| 35 | VDD_RF2 | VDD_RF2 | VDD_RF2 | | | | | | | | | |
| 36 | VDD_RF1 | VDD_RF1 | VDD_RF1 | | | | | | | | | |
| 37 | PTC1 | DISABLED | | PTC1/ RF_EARLY_ WARNING | ANT_B | I2C0_SDA | LPUART0_ RTS_b | TPM0_CH2 | | | SPI1_SCK | |
| 38 | PTC2 | DISABLED | | PTC2/ LLWU_P10 | TX_SWITCH | I2C1_SCL | LPUART0_ RX | CMT_IRO | | DTM_RX | SPI1_SOUT | |
| 39 | PTC3 | DISABLED | | PTC3/ LLWU_P11 | RX_ SWITCH | I2C1_SDA | LPUART0_ TX | TPM0_CH1 | | DTM_TX | SPI1_SIN | CAN0_TX |
| 40 | PTC4 | DISABLED | | PTC4/ LLWU_P12/ RF_ACTIVE | ANT_A | EXTRG_IN | LPUART0_ CTS_b | TPM1_CH0 | | I2C0_SCL | SPI1_PCS0 | CAN0_RX |
| 41 | PTC5 | DISABLED | | PTC5/ LLWU_P13/ RF_NOT_ ALLOWED/ RF_ PRIORITY | | LPTMR0_ ALT2 | LPUART0_ RTS_b | TPM1_CH1 | | | | |
| 42 | PTC6 | DISABLED | | PTC6/ LLWU_P14/ RF_ RFOSC_EN | | I2C1_SCL | LPUART0_ RX | TPM2_CH0 | | | | |
| 43 | PTC7 | DISABLED | | PTC7/ LLWU_P15 | SPI0_PCS2 | I2C1_SDA | LPUART0_ TX | TPM2_CH1 | | | | |
| 44 | VDD_1 | VDD_1 | VDD_1 | | | | | | | | | |

Pin Diagrams and Pin Assignments

| 48 "Wettable" HVQFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | ALT8 | ALT9 |
|---------------------------|----------|----------|------|--|-----------|----------|-------------------|----------|------|--------|-------------------|------|
| 45 | PTC16 | DISABLED | | PTC16/ LLWU_P0/ RF_STATUS | SPI0_SCK | I2C0_SDA | LPUART0_ RTS_b | TPM0_CH3 | | | LPUART1_ RTS_b | |
| 46 | PTC17 | DISABLED | | PTC17/ LLWU_P1/ RF_EXT_ OSC_EN | SPI0_SOUT | I2C1_SCL | LPUART0_ RX | | | DTM_RX | LPUART1_ RX | |
| 47 | PTC18 | DISABLED | | PTC18/ LLWU_P2 | SPI0_SIN | I2C1_SDA | LPUART0_ TX | | | DTM_TX | LPUART1_ TX | |
| 48 | PTC19 | DISABLED | | PTC19/ LLWU_P3/ RF_EARLY_ WARNING | SPI0_PCS0 | I2C0_SCL | LPUART0_ CTS_b | | | | LPUART1_ CTS_b | |
| 49 | Ground | NA | | | | | | | | | | |

7.3 KW39/38/37 Pinouts

KW39/38/37 device pinouts are shown in the figure below.

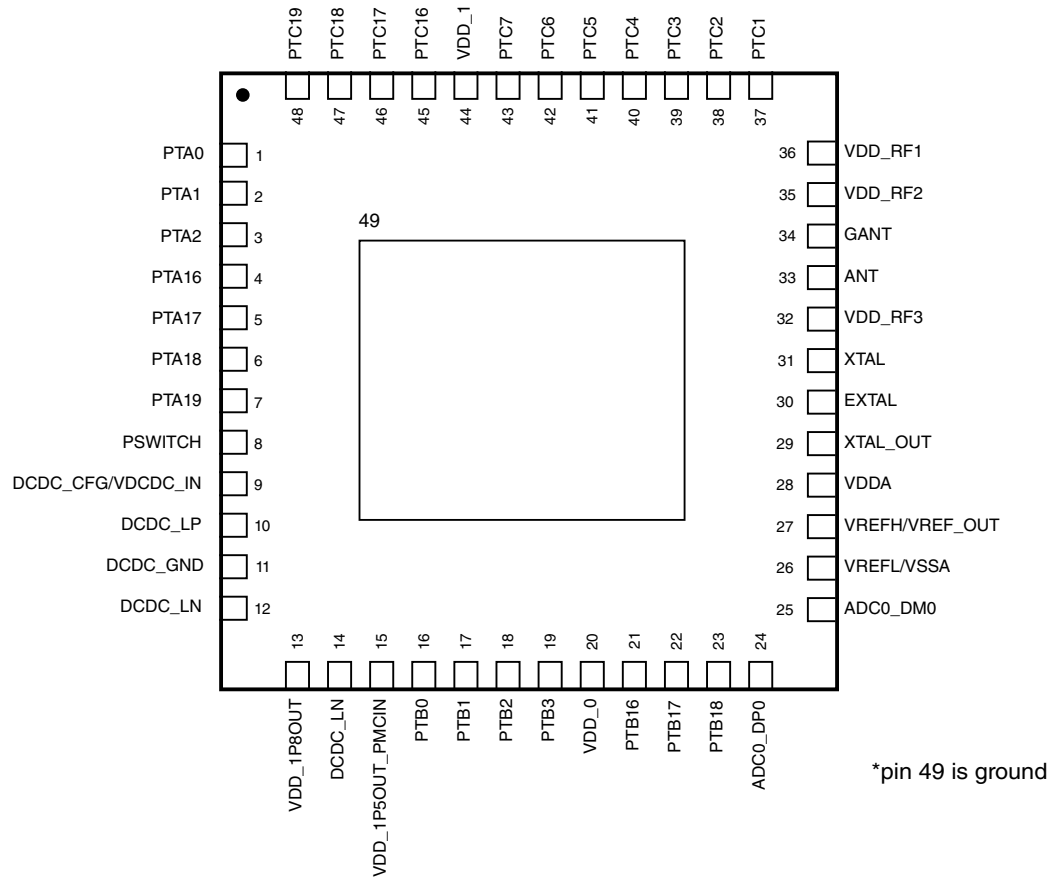


Figure 20. 48-pin "Wettable" HVQFN pinout diagram

7.4 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the chapter of the module. They also briefly describe the signal function and direction.

7.4.1 Core Modules

This section contains tables describing the core module signal descriptions.

Table 48. SWD Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|--|-----|
| SWD_DIO | SWD_DIO | Serial Wire Debug Data Input/Output ¹ | I/O |
| SWD_CLK | SWD_CLK | Serial Wire Clock ² | I |

1. Pulled up internally by default

2. Pulled down internally by default

7.4.2 Radio Modules

This section contains tables describing the radio signals.

Table 49. Radio Module Signal Descriptions

| Module Signal Name | Pin Direction | Pin Name | Pin Description |
|--------------------|---------------|------------------|---|
| ANT | O | ANT | Antenna |
| ANT_A | O | ANT_A | Antenna selection A for Front End Module support |
| ANT_B | O | ANT_B | Antenna selection B for Front End Module support |
| RF_ACTIVE | O | RF_ACTIVE | An output which is asserted prior to any Radio event and remains asserted for the duration of the event. |
| DTM_RX | I | DTM_RX | Direct Test Mode Receive |
| DTM_TX | O | DTM_TX | Direct Test Mode Transmit |
| GANT | I | GANT | Antenna ground |
| RF_STATUS | O | RF_STATUS | An output which indicates when the Radio is in an Rx or Tx event; software can also control this signal directly. |
| RF_PRIORITY | O | RF_PRIORITY | An output which indicates to the external WiFi device that the Radio event is a high priority and it needs access to the 2.4 GHz antenna. |
| RF_EARLY_WARNING | O | RF_EARLY_WARNING | Bluetooth LE LL generated signal which can be used to wake an external sensor to make a measurement before a Bluetooth LE event. |
| RF_NOT_ALLOWED | I | RF_NOT_ALLOWED | External signal which causes the internal Radio to cease radio activity. |
| RF_TX_CONF | I | RF_TX_CONF | Signal from an external Radio which indicates the availability of the 2.4 GHz antenna to the internal Radio. NOTE: This is a GPIO, not a dedicated PIN. |
| RX_SWITCH | O | RX_SWITCH | Front End Module receive mode signal. |
| TX_SWITCH | O | TX_SWITCH | Front End Module transmit mode signal. |

Table 50. Radio Module Miscellaneous Pin Descriptions

| Pin Name | Pad Direction | Pin Name | Pin Description |
|---------------|---------------|---------------|---|
| RF_INT_OSC_EN | I | RF_RFOSC_EN | External request to turn on the Radio's internal RF oscillator. |
| RF_EXT_OSC_EN | O | RF_EXT_OSC_EN | Internal request to turn on an External oscillator for use by the internal Radio. The request can also be from the SoC if it is using the RF oscillator as its clock. |

7.4.3 System Modules

This section contains tables describing the system signals.

Table 51. System Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|------------------|--------------------|--|-----|
| NMI_b | — | Non-maskable interrupt | I |
| RESET_b | — | Reset bidirectional signal | I/O |
| VDD_[1:0] | VDD | Power supply | I |
| Ground | VSS | Ground | I |
| VDD_RF[3:1] | VDD_RF | Radio power supply | I |
| VDCDC_IN | VDCDC_IN | VDCDC_IN | I |
| VDD_1P8OUT | VDD_1P8 | DC-DC 1.8 V Regulated Output / Input in bypass | I/O |
| VDD_1P5OUT_PMCIN | VDD_1P5/VDD_PMC | DC-DC 1.5 V Regulated Output / PMC Input in bypass | I/O |
| PSWITCH | PSWITCH | DC-DC enable switch | I |
| DCDC_CFG | DCDC_CFG | DC-DC switch mode select | I |
| DCDC_LP | DCDC_LP | DC-DC inductor input positive | I/O |
| DCDC_LN | DCDC_LN | DC-DC inductor input negative | I/O |
| DCDC_GND | DCDC_GND | DC-DC ground | I |

Table 52. LLWU Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|----------------|-----|
| LLWU_P[15:0] | LLWU_P[15:0] | Wake-up inputs | I |

7.4.4 Clock Modules

This section contains tables for Clock signal descriptions.

Table 53. Clock Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|--|-----|
| EXTAL | EXTAL | 26 MHz/32 MHz External clock/Oscillator input | I |
| XTAL | XTAL | 26 MHz/32 MHz Oscillator input | I |
| XTAL_OUT | XTAL_OUT | 26 MHz/32 MHz Clock output | O |
| XTAL_OUT_EN | XTAL_OUT_ENABLE | 26 MHz/32 MHz Clock output enable for XTAL_OUT | I |
| EXTAL32K | EXTAL32K | 32 kHz External clock/Oscillator input | I |
| XTAL32K | XTAL32K | 32 kHz Oscillator input | I |
| CLKOUT | CLKOUT | Internal clocks monitor | O |

7.4.5 Analog Modules

This section contains tables for Analog signal descriptions.

Table 54. ADC0 Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|---|-----|
| ADC0_DM0 | DADM0 | ADC Channel 0 Differential Input Negative | I |
| ADC0_DP0 | DADP0 | ADC Channel 0 Differential Input Positive | I |
| ADC0_SE[5:1] | AD[5:1] | ADC Channel 0 Single-ended Input n | I |
| VREFH | V _{REFSH} | Voltage Reference Select High | I |
| VDDA | V _{DDA} | Analog Power Supply | I |
| VSSA | V _{SSA} | Analog Ground | I |

Table 55. CMP0 Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|-----------------------|-----|
| CMP0_IN[5:0] | IN[5:0] | Analog voltage inputs | I |
| CMP0_OUT | CMP0 | Comparator output | O |

Table 56. VREF Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|---|-----|
| VREF_OUT | VREF_OUT | Internally generated voltage reference output | O |

7.4.6 Timer Modules

This section contains tables describing timer module signals.

Table 57. TPM0 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|----------------|-----|
| TPM_CLKIN[1:0] | TPM_EXTCLK | External clock | I |
| TPM0_CH[3:0] | TPM_CH[3:0] | TPM channel | I/O |

Table 58. TPM1 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|----------------|-----|
| TPM_CLKIN[1:0] | TPM_EXTCLK | External clock | I |
| TPM1_CH[1:0] | TPM_CH[1:0] | TPM channel | I/O |

Table 59. TPM2 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|----------------|-----|
| TPM_CLKIN[1:0] | TPM_EXTCLK | External clock | I |
| TPM2_CH[1:0] | TPM_CH[1:0] | TPM channel | I/O |

Table 60. LPTMR0 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|-------------------------|-----|
| LPTMR0_ALT[2:1] | LPTMR0_ALT[2:1] | Pulse counter input pin | I |

Table 61. RTC Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|-------------------------|-----|
| RTC_CLKOUT | RTC_CLKOUT | 1 Hz square-wave output | O |

7.4.7 Communication Interfaces

This section contains tables for the signal descriptions for the communication modules.

Table 62. SPI0 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|--------------------------|-----|
| SPI0_PCS0 | PCS0/SS | Chip Select/Slave Select | I/O |
| SPI0_PCS[2:1] | PCS[2:1] | Chip Select | O |
| SPI0_SCK | SCK | Serial Clock | I/O |
| SPI0_SIN | SIN | Data In | I |
| SPI0_SOUT | SOUT | Data Out | O |

Table 63. SPI1 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|--------------------------|-----|
| SPI1_PCS0 | SPI1_PCS0 | Chip Select/Slave Select | I/O |
| SPI1_SCK | SCK | Serial Clock | I/O |
| SPI1_SIN | SIN | Data In | I |
| SPI1_SOUT | SOUT | Data Out | O |

Table 64. I2C0 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|-----------------------|-----|
| I2C0_SCL | SCL | I2C serial clock line | I/O |
| I2C0_SDA | SDA | I2C serial data line | I/O |

Table 65. I2C1 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|-----------------------|-----|
| I2C1_SCL | SCL | I2C serial clock line | I/O |
| I2C1_SDA | SDA | I2C serial data line | I/O |

Table 66. CAN0 Signal Descriptions (KW38 only)

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|------------------|-----|
| CAN0_RX | CAN RX | CAN Receive Pin | I |
| CAN0_TX | CAN TX | CAN Transmit Pin | O |

Table 67. LPUART0 Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|----------------------------|-----|
| LPUART0_CTS_b | LPUART CTS | Clear To Send | I |
| LPUART0_RTS_b | LPUART RTS | Request To Send | O |
| LPUART0_RX | LPUART RxD | Receive Data | I |
| LPUART0_TX | LPUART TxD | Transmit Data ¹ | I/O |

1. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data

Table 68. LPUART1 Module Signal Descriptions (KW38 only)

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|----------------------------|-----|
| LPUART1_CTS_b | LPUART CTS | Clear To Send | I |
| LPUART1_RTS_b | LPUART RTS | Request To Send | O |
| LPUART1_RX | LPUART RxD | Receive Data | I |
| LPUART1_TX | LPUART TxD | Transmit Data ¹ | I/O |

1. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data

7.4.8 Human-Machine Interfaces(HMI)

This section contains tables describing the HMI signals.

Table 69. GPIO Module Signal Descriptions

| SoC Signal Name | Module Signal Name | Description | I/O |
|-----------------|--------------------|----------------------------------|-----|
| PTA[19:16][2:0] | PORTA19-16, 2-0 | General Purpose Input/ Output | I/O |
| PTB[18:16][3:0] | PORTB18-16, 3-0 | General Purpose Input/ Output | I/O |
| PTC[19:16][7:1] | PORTC19-16, 7-1 | General Purpose Input/ Output | I/O |

8 Package Information

8.1 Obtaining package dimensions

Package dimensions are available in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the document number of the drawing:

Table 70. Packaging Dimensions

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 48-pin "Wettable" HVQFN (7x7) | 98ASA01307D |

9 Part identification

9.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

9.2 Format

Part numbers for this device have the following format:

Q KW## A FFF R T PP CC N

9.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 71. Part number fields descriptions

| Field | Description | Values |
|-------|-------------------------|--|
| Q | Qualification status | <ul style="list-style-type: none"> • M = Fully qualified, general market flow • P = Prequalification |
| KW## | Kinetis Wireless family | <ul style="list-style-type: none"> • KW39 • KW38 • KW37 |

Table continues on the next page...

Table 71. Part number fields descriptions (continued)

| Field | Description | Values |
|-------|-----------------------------|--|
| A | Key attribute | <ul style="list-style-type: none"> A = Automotive Qualification Z = Industrial Qualification |
| FFF | Program flash memory size | <ul style="list-style-type: none"> 512 = 512 KB |
| T | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 C = -40 to 85 |
| PP | Package identifier | <ul style="list-style-type: none"> FT = 48 "Wettable" HVQFN (7 mm x 7 mm) |
| CC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> 4 = 48 MHz |
| N | Packaging type | <ul style="list-style-type: none"> (Blank) = Tray R = Tape and reel |

9.4 Example

This is an example part number:

MKW38A512VFT4

10 Revision History

Table 72. Revision History

| Rev. No. | Date | Substantial Changes |
|----------|---------|--|
| Rev 7 | 03/2020 | <ul style="list-style-type: none"> Replaced VDD_XTAL with VDD_RF3. Preceded Tx output power value, 5 dBm, with a plus "+" sign. Added "256 KB P-Flash" to the fifth column name in the KW39/38/37 Part Numbers table. Corrected Figure 3 to show Prg Acc RAM 8 KB in place of FlexRAM 8 KB. Also added "Prg Acc RAM" entry in Table 1. Corrected accuracy percentage of on-chip 4 MHz oscillator to 11% in System Clocks. Updated minimum and typical values in Table 4 - Top-Level Receiver Specifications. Updated maximum and typical values in Table 6 - Top-Level Transmitter Specifications. Also updated footnote 3 as follows: "Measured at KW39/38/37 RF pins, with Vdd_RFx over 1.44 V and assuming an average Tx duty cycle <=24%. For Tx output over +3.5 dBm, powered Vdd_RFx has to be higher than 1.44 V." Added V_{DD_1P5} specification in Voltage and current operating requirements. Added V_{POR_VDD_1P5} specification in LVD and POR operating requirements. Updated maximum value of Frequency deviation of internal reference clock to ± 11 in MCG specifications. In Power consumption operating behaviors : <ul style="list-style-type: none"> Removed the following note: "The maximum values specified in the following tables represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma)." Updated maximum values of Power consumption operating behaviors - Bypass and Buck Modes in Table 14 and Table 15. |

Table continues on the next page...

Table 72. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|----------|---------|--|
| | | <ul style="list-style-type: none"> Added V_{DD_1P5} symbol to "Bypass Mode Supply Voltage (RF and Analog)" in DC-DC Converter operating conditions. Updated minimum value to 1.5 V and removed typical value in "1.5 V Voltage Output" in Table 43. Also updated the corresponding footnote with the correct value of 1.5 V. |
| Rev 6 | 01/2020 | <ul style="list-style-type: none"> Updated Low-power Mode (VLLS0) current value to 266.6 nA in front page features under "Low-power Consumption" section. Updated through out typical value of Bluetooth LE Receiver Sensitivity (2 Mbit/s and 1 Mbit/s) to -95.5 dBm and -98 dBm respectively. Updated typical values of Top-level receiver specifications in Table 4. Updated typical and maximum values in Table 14 and Table 15. Updated typical values of Tx (at 5 dBm) radio state at STOP and RUN MCU states in SoC Power Consumption. Updated V_{CDM} ratings in ESD handling ratings. Also updated the JEDEC standard to JS001 and JS002. |
| Rev 5 | 12/2019 | <ul style="list-style-type: none"> Editorial fixes. Specified typical value of Rx current as 6.3 mA in front page features of the Data sheet (under Low-power Consumption section). Also added 256 KB FlexNVM column in KW39/38/37 Part Numbers table. Added Table 1. Corrected accuracy percentage of RC oscillator and on-chip 4 MHz oscillator to 3% and 6% respectively in System Clocks. Updated receiver sensitivity value to -101 dBm in Key Specifications. In section 4.2 - Receiver Feature Summary: <ul style="list-style-type: none"> Specified typical values of I_{RXon} with respect to DC-DC converter buck and bypass modes in Table 4. Updated receiver specifications with generic FSK modulations in Table 5. Updated V_{OH} - Normal drive pad in Voltage and current operating behaviors to include output high voltage at -1 mA. Added the following paragraph to Power consumption operating behaviors : "The maximum values specified in the following tables represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma)." Also updated units of I_{DD_VLLS1} typical values in Table 15. Updated maximum values in Table 14 and Table 15. Also updated mode# 20 and 21, IDD_VLLS2 and $IDD_VLLS2_16KB_16KB$, to IDD_VLLS2_16KB and IDD_VLLS2_32KB. Updated Run mode supply current/VLPR mode current vs. core frequency images in Diagram: Typical IDD_RUN operating behavior. Updated Table 26 to include operating temperature (T_A), load capacitance (C_L), and ESR specifications. Updated value of V_{DCDC_IN} to 2.1 V for IDD_1P8_buck3 in 1.8V Output Current row in Table 43. |
| Rev 4 | 08/2019 | <ul style="list-style-type: none"> Updated value of Typical Receiver Sensitivity to -101 dBm. Corrected radio block in KW39 Detailed Block Diagram. Also M1 port (connected from AXBS to Data Stream) corrected to M3. Added new item ("<i>Each individual MB is formed by 16, 24,</i>") to the list of features in FlexCAN section in Peripheral features. Updated typical values in Receiver Feature Summary. In Transmit and PLL Feature Summary : <ul style="list-style-type: none"> Specified typical value of "Bluetooth LE 2 Mbit/s Adjacent Channel Transmit Power at 4 MHz and ≥ 6 MHz offset". Updated Figure 4. TX Pout (dBm) as function TX-PA Power Code at RF pins. |

Table continues on the next page...

Table 72. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|----------|---------|--|
| | | <ul style="list-style-type: none"> Updated numbers of "Transmit Output Power as a function of PA_POWER[5:0]" in Table 7 and Table 8. Added Figure 5. TX Pout (dBm) as function TX-PA Power Code at RF pins (LDO-HF bumped). Updated numbers in Table 16. Replaced "EMC design" with "KW38, HW guideline, RF system evaluation" in Designing with radiated emissions in mind. Updated maximum value of $\Delta f_{\text{intf_ft}}$ to ± 6 in MCG specifications. Updated Table 43 with the following: <ul style="list-style-type: none"> Added conditions, $V_{\text{DCDC_IN}}$ above 2.7 V and below 2.7 V, in the first row, "DC-DC Converter Output Power". Updated conditions in the "1.8 V Output Current" row. Also added IDD_1P8_buck3 condition to the row and updated maximum values. Updated "1.5 V Output Current" maximum value to 45 mA. Updated footnote 5 as follows: "The output current specification in buck mode represents..... Note that the maximum output power of the DC-DC converter is 140 mW when $V_{\text{DCDC_IN}}$ is below 2.7 V and 195 mW when $V_{\text{DCDC_IN}}$ is above 2.7 V.....". |
| Rev 3 | 06/2019 | <ul style="list-style-type: none"> Removed "Input Voltage High/Low" rows from Radio operating conditions. Removed the following footnote from Table 14 - "Supported through the connectivity software in its pre-defined Deep Sleep Modes". Also updated Typical values in Table 14 and Table 15. Removed "Flash timing specifications – program and erase" and "Flash high voltage current behaviors" tables. Updated 48-pin "Wettable" HVQFN pinout diagram - added ground pin 49 to the diagram. |
| Rev 2 | 04/2019 | <ul style="list-style-type: none"> Updated typical value of Bluetooth LE Receiver sensitivity at 2 Mbit/s from -94 to -95 dBm. Updated pin package drawing. Updated Low-power Mode (VLLS0) Current value to 252 nA and typical value of Tx current to 5.7 mA. Added "512 KB P-Flash" column to this table. Also modified column name to "8 KB FlexRAM EEPROM" from 8 KB EEPROM. Replaced "Prg Acc RAM 8 KB" with "FlexRAM 8 KB" in KW37 Detailed Block Diagram. Removed "Galois counter mode (AES-GCM)" and "DES modes" features of LTC from Security Features. Updated typical values in Receiver Feature Summary. Also updated measurement resolution to 2 MHz from 1 MHz in "Bluetooth LE uncoded 2 Mbit/s (High Speed)" section. Updated typical values in Table 5. Updated typical values of I_{TX0dBm}, I_{TX0dBmB}, $I_{\text{TX3.5dBm}}$, $I_{\text{TX3.5dBmB}}$, I_{TX5dBm}, and I_{TX5dBmB}. Also updated minimum value of $\text{TXBW}_{\text{BLE2M}}$ to 2.2 MHz in Table 6. Removed 48-pin LQFN package from Thermal attributes and specified values for HVQFN48. Also replaced JESD51-2 standard with JESD51-2A in footnotes. In Table 14 and Table 15 : <ul style="list-style-type: none"> Added "Mode#" column. Added the following measurements—IDD_RUN_CM, IDD_VLPR_CM, IDD_VLLS2_16KB_16KB, IDD_VLLS2_16KB_RF_Tx_RAM, IDD_VLLS2_16KB_RF_Rx_RAM. Updated typical values. Added "Adder#" column to Table 16. Updated minimum and maximum values of "1.5 V Output Voltage" in Table 43. Also specified the condition as "Consumed by Radio." Removed support of DIAG1-3 signals and updated "DEFAULT" column to correct "DISABLED" status of PTA19, PTB1/2/3 pin names in Signal Multiplexing and Pin Assignments tables. |

Table continues on the next page...

Table 72. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|-------------|---------|---|
| Rev 1 | 12/2018 | <ul style="list-style-type: none"> • Updated Features list on the front page: <ul style="list-style-type: none"> • Updated Typical Receiver Sensitivity value of BLE LR 500 kbit/s from -99 to -101 dBm. • Added 0.7 in the Generic FSK modulation index. • Updated topic Radio features. • Restructured section 3 Transceiver Description. • Updated Full Bluetooth Low Energy version 5.0 modulation and Generic FSK modulation values in Key Specifications. • Updated Table 4, Table 5, and Table 6. Added Table 8. • Added the following footnote in : "Tx continuous wave power output at the RF pins with the recommended matching components mounted on PCB." |
| Rev 1 Draft | 11/2018 | <ul style="list-style-type: none"> • Removed the following part numbers: MKW38A512VHT4, MKW38Z512VHT4, and MKW37Z512VHT4. • Added the following part numbers: MKW38Z512VFT4 and MKW37Z512VFT4. • Removed 48-pin LQFN package. • Changed 48 "Wettable" QFN to 48 "Wettable" HVQFN throughout. • Applied new NXP Brand Guidelines for Bluetooth Low Energy. Removed references of BLE and replaced with Bluetooth LE. • Updated Features list on the front page: <ul style="list-style-type: none"> • Corrected Typical Receiver Sensitivity value of BLE LR 500 kbit/s from -100.5 to -99 dBm. • Corrected Typical Receiver Sensitivity (250 kbit/s GFSK-BT=0.5, h=0.5) from -100 to -103 dBm. • Added 8 KB program acceleration RAM on KW37 to MCU and Memories section. • Updated topic 2.2 Radio Features. • Updated topic 2.3 Microcontroller features in the "On-Chip Memory" section to include support of EEPROM emulation. • Updated values of VDD_1P8OUT=1.8 V and VDD_1P8OUT=3.0 V to 45 mA and 27 mA. • Updated maximum value of Programmable transmitter output power to 5 dBm. • Updated typical value of RF Output power control range to 35 dB in Table 5. Top level Transmitter Specifications. • Removed silicon revision (R) field from Table 71. Part number fields descriptions. |
| Rev 0 | 09/2018 | Initial Internal Release |

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