

# 1.0 A 6.8 V H-Bridge Motor Driver IC

The 17511 is a monolithic H-Bridge designed to be used in portable electronic applications to control small DC motors or bipolar step motors. End applications include head positioners (CDROM or disk drive), camera focus motors, and camera shutter solenoids.

The 17511 can operate efficiently with supply voltages as low as 2.0 V to as high as 6.8 V. Its low  $R_{DS(ON)}$  H-Bridge output MOSFETs (0.46  $\Omega$  typical) can provide continuous motor drive currents of 1.0 A and handle peak currents up to 3.0 A. It is easily interfaced to low-cost MCUs via parallel 3.0 V or 5.0 V compatible logic. The device can be pulse width modulated (PWMed) at up to 200 kHz.

This device contains an integrated charge pump and level shifter (for gate drive voltages), integrated shoot-through current protection (cross-conduction suppression logic and timing), and undervoltage detection and shutdown circuitry.

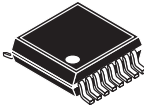
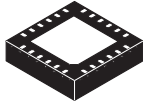
The 17511 has four operating modes: Forward, Reverse, Brake, and Tri-state (high-impedance).

### Features

- 2.0 to 6.8 V continuous operation
- Output current 1.0 A (DC), 3.0 A (peak)
- MOSFETs < 600 m $\Omega$   $R_{DS(ON)}$  @ 25 °C guaranteed
- 3.0 V/5.0 V TTL/CMOS compatible logic inputs
- PWM frequencies up to 200 kHz
- Undervoltage shutdown
- Low power consumption
- Integrated charge pump
- Shoot-through current protection
- External MOSFET control circuit

17511

H-BRIDGE MOTOR DRIVER IC

 <b>EV SUFFIX)</b> <b>98ASA10614D</b> <b>16-Pin VMFP</b>	 <b>EP SUFFIX</b> <b>98ARL10577D</b> <b>24-PIN QFN</b>
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ORDERING INFORMATION		
Device	Temperature Range (T <sub>A</sub> )	Package
MPC17511EP/R2	-20 to 65 °C	24 QFN
MPC17511EV/EL		16 VMFP

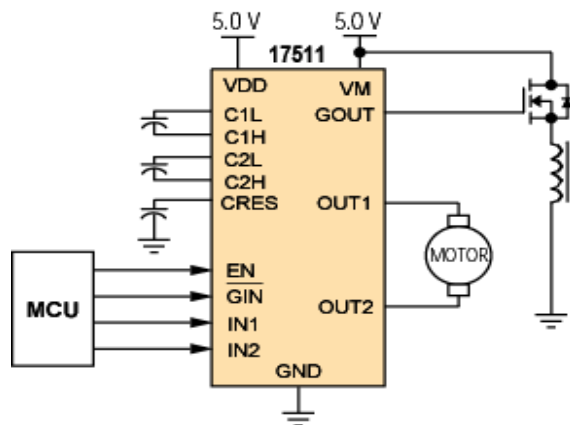


Figure 1. 17511 Simplified Application Diagram

### INTERNAL BLOCK DIAGRAM

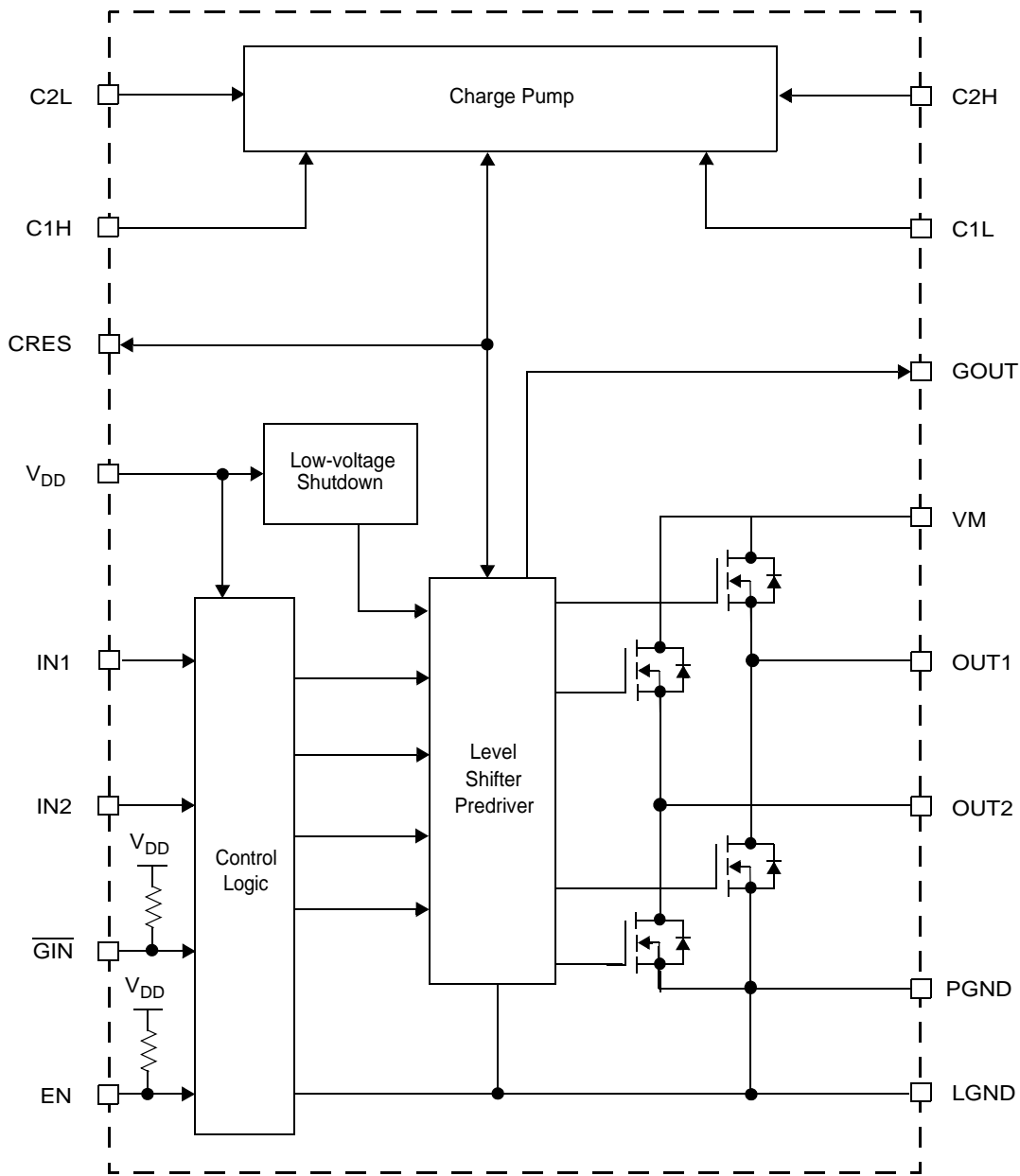


Figure 2. 17511 Simplified Internal Block Diagram

## PIN CONNECTIONS

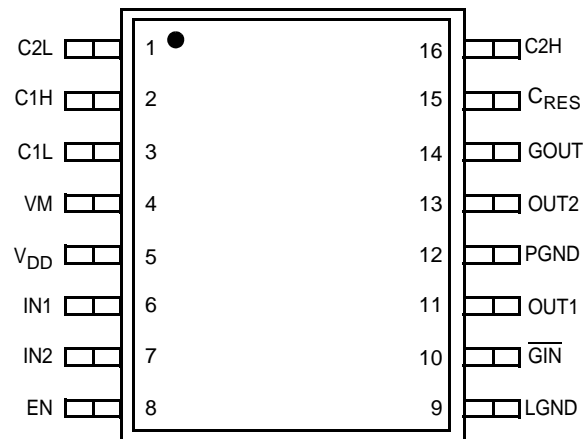


Figure 3. VMFP Pin Connections

Table 1. 17511 VMFP Pin Function Description

Pin Number	Pin Name	Formal Name	Definition
1	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
2	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
3	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
4	VM	Motor Drive Power Supply	Driver power supply voltage input pin.
5	V <sub>DD</sub>	Logic Supply	Control circuit power supply pin.
6	IN1	Input Control 1	Control signal input 1
7	IN2	Input Control 2	Control signal input 2.
8	EN	Enable Control	Enable control signal input pin.
9	LGND	Logic Ground	Logic ground pin.
10	$\overline{\text{GIN}}$	Gate Driver Input	LOW True control signal for GOUT pin.
11	OUT1	H-Bridge Output 1	Driver output 1 (right half of H-Bridge).
12	PGND	Power Ground	Driver ground pin.
13	OUT2	H-Bridge Output 2	Driver output 2 (left half of H-Bridge).
14	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
15	C <sub>RES</sub>	Charge Pump Output Capacitor Connection	Charge pump reservoir capacitor pin.
16	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).

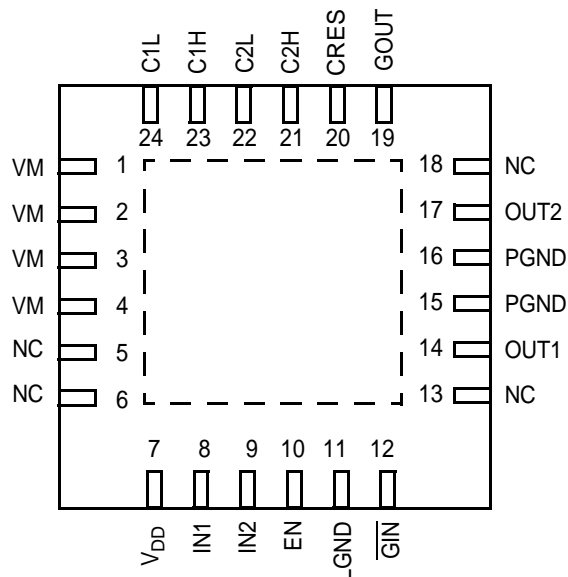


Figure 4. QFN Pin Connections

Table 2. 17511 QFN Pin Function Description

Pin Number	Pin Name	Formal Name	Definition
1, 2, 3, 4	VM	Motor Drive Power Supply	Driver power supply voltage input pin.
5, 6, 13, 18	NC	No Connect	This pin is not used.
7	V <sub>DD</sub>	Logic Supply	Control circuit power supply pin.
8	IN1	Logic Input Control 1	Control signal input 1.
9	IN2	Logic Input Control 2	Control signal input 2.
10	EN	Enable Control	Enable control signal input pin.
11	LGND	Logic Ground	Logic ground pin.
12	$\overline{\text{GIN}}$	Gate Driver Input	LOW = True control signal for GOUT pin.
14	OUT1	Output 1	Driver output 1 (right half of H-Bridge).
15, 16	PGND	Power Ground	Driver ground pin.
17	OUT2	Output 2	Driver output 2 (left half of H-Bridge).
19	GOUT	Gate Driver Output	Output gate driver signal to external MOSFET switch.
20	CRES	Pre-Driver Power Supply	Pre-driver circuit power supply pin.
21	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
22	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
23	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
24	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).

## ELECTRICAL CHARACTERISTICS

### MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	$V_M$	-0.5 to 8.0	V
Charge Pump Output Voltage	$V_{CRESP}$	-0.5 to 14.0	V
Logic Supply Voltage	$V_{DD}$	-0.5 to 7.0	V
Signal Input Voltage (EN, IN1, IN2, $\overline{GIN}$ )	$V_{IN}$	-0.5 to $V_{DD}+0.5$	V
Driver Output Current			A
Continuous	$I_O$	1.0	
Peak <sup>(1)</sup>	$I_{OPK}$	3.0	
ESD Voltage <sup>(2)</sup>			V
Human Body Model	$V_{ESD1}$	±1800	
Machine Model	$V_{ESD2}$	±100	
Storage Temperature Range	$T_{STG}$	-55 to 150	°C
Operating Junction Temperature	$T_J$	-20 to 150	°C
Thermal Resistance <sup>(3)</sup>	$R_{\theta JA}$		°C/W
24 Pin QFN		50	
16 Pin VMFP		150	
Power Dissipation <sup>(4)</sup>	$P_D$		mW
24 Pin QFN		2500	
16 Pin VMFP		830	
Soldering Temperature <sup>(5)</sup>	$T_{SOLDER}$	245	°C
Peak Package Reflow Temperature During Reflow <sup>(6), (7)</sup>	$T_{PPRT}$	Note 7	°C

**Notes**

- $T_A = 25\text{ °C}$ , 10 ms pulse width at 200 ms intervals.
- ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP} = 100\text{ pF}$ ,  $R_{ZAP} = 1500\text{ }\Omega$ ), ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP} = 200\text{ pF}$ ,  $R_{ZAP} = 0\text{ }\Omega$ ).
- QFN24: 45 x 30 x 1 [mm] glass EPOXY board mount. (See: recommended heat pattern) VMFP16: 37 x 50 x 1.6 [mm] glass EPOXY board mount. When the exposed pad is bonded, R<sub>sj</sub> is not performed.
- Maximum at  $T_A = 25\text{ °C}$ . When the exposed pad is bonded, R<sub>sj</sub> is not performed.
- Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.

### STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_M = V_{DD} = 5.0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>POWER</b>					
Driver Circuit Power Supply Voltage	$V_M$	2.0	5.0	6.8	V
Logic Supply Voltage	$V_{DD}$	2.7	5.0	5.7	V
Capacitor for Charge Pump	C1, C2, C3	0.01	0.1	1.0	$\mu\text{F}$
Standby Power Supply Current					
Motor Supply Standby Current	$I_{VMSTBY}$	–	–	1.0	$\mu\text{A}$
Logic Supply Standby Current <sup>(8)</sup>	$I_{VDDSTBY}$	–	–	1.0	mA
Operating Power Supply Current					
Logic Supply Current <sup>(9)</sup>	$I_{VDD}$	–	–	3.0	mA
Charge Pump Circuit Supply Current	$I_{CRES}$	–	–	0.7	mA
Low $V_{DD}$ Detection Voltage <sup>(10)</sup>	$V_{DDDET}$	1.5	2.0	2.5	V
Driver Output ON Resistance <sup>(11)</sup>	$R_{DS(ON)}$	–	0.46	0.60	$\Omega$
<b>GATE DRIVE</b>					
Gate Drive Voltage <sup>(12)</sup> No Current Load	$V_{CRES}$	12	13	13.5	V
Gate Drive Ability (Internally Supplied) $I_{CRES} = -1.0\text{ mA}$	$V_{CRESLOAD}$	10	11.2	–	V
Gate Drive Output $I_{OUT} = -50\text{ }\mu\text{A}$ $I_{IN} = 50\text{ }\mu\text{A}$	$V_{GOUTHIGH}$ $V_{GOUTLOW}$	$V_{CRES-0.5}$ LGND	$V_{CRES-0.1}$ LGND+0.1	$V_{CRES}$ LGND+0.5	V
<b>CONTROL LOGIC</b>					
Logic Input Voltage	$V_{IN}$	0	–	$V_{DD}$	V
Logic Input Function ( $2.7\text{ V} < V_{DD} < 5.7\text{ V}$ )					
High-level Input Voltage	$V_{IH}$	$V_{DD} \times 0.7$	–	–	V
Low-level Input Voltage	$V_{IL}$	–	–	$V_{DD} \times 0.3$	V
High-level Input Current	$I_{IH}$	–	–	1.0	$\mu\text{A}$
Low-level Input Current	$I_{IL}$	-1.0	–	–	$\mu\text{A}$
Pull-Up Resistance ( $\overline{EN}$ , $\overline{GIN}$ )	$R_{PU}$	50	100	200	k $\Omega$

Notes

8.  $I_{VDDSTBY}$  includes current to the predriver circuit.
9.  $I_{VDD}$  includes current to the predriver circuit.
10. Detection voltage is defined as when the output becomes high-impedance after  $V_{DD}$  drops below the detection threshold. When the gate voltage  $V_{CRES}$  is applied from an external source,  $V_{CRES} = 7.5\text{ V}$ .
11.  $I_O = 1.0\text{ A}$  source + sink.
12. Input logic signal not present.

### DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 5. Dynamic Electrical Characteristics**

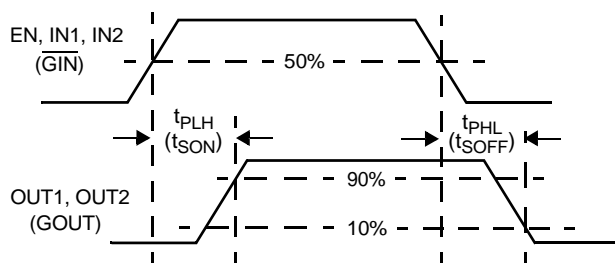
Characteristics noted under conditions  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_M = V_{DD} = 5.0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^\circ\text{C}$  under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>INPUT (EN, IN1, IN2, GIN)</b>					
Pulse Input Frequency	$f_{IN}$	–	–	200	kHz
Input Pulse Rise Time <sup>(13)</sup>	$t_R$	–	–	1.0 <sup>(14)</sup>	$\mu\text{s}$
Input Pulse Fall Time <sup>(15)</sup>	$t_F$	–	–	1.0 <sup>(14)</sup>	$\mu\text{s}$
<b>OUTPUT</b>					
Propagation Delay Time					$\mu\text{s}$
Turn-ON Time	$t_{PLH}$	–	0.55	1.0	
Turn-OFF Time	$t_{PHL}$	–	0.55	1.0	
GOUT Propagation Delay Time					$\mu\text{s}$
Turn-ON Time	$t_{SON}$	–	0.15	0.5	
Turn-OFF Time	$t_{SOFF}$	–	0.15	0.5	
Charge Pump Circuit <sup>(16)</sup>	$t_{V_{CRESON}}$				ms
Rise Time <sup>(17)</sup>		–	0.1	3.0	
Low-Voltage Detection Time	$t_{VDDDET}$	–	–	10	ms

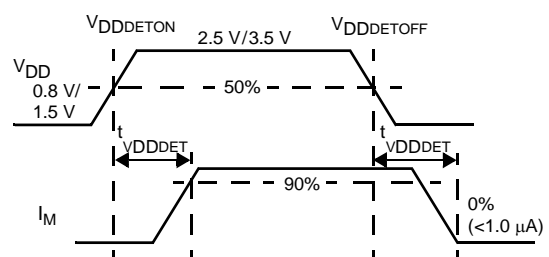
**Notes**

13. Time is defined between 10% and 90%.
14. That is, the input waveform slope must be steeper than this.
15. Time is defined between 90% and 10%.
16. When  $C1 = C2 = C3 = 0.1\text{ }\mu\text{F}$ .
17. Time to charge  $C_{RES}$  to 11 V after application of  $V_{DD}$ .

### TIMING DIAGRAMS



**Figure 5.  $t_{PLH}$ ,  $t_{PHL}$ , and  $t_{PZH}$  Timing**



**Figure 6. Low-Voltage Detection**

**Table 6. Truth Table**

INPUT				OUTPUT		
EN	IN1	IN2	$\overline{\text{GIN}}$	OUT1	OUT2	GOUT
H	H	H	X	L	L	X
H	H	L	X	H	L	X
H	L	H	X	L	H	X
H	L	L	X	Z	Z	X
L	X	X	X	L	L	L
H	X	X	H	X	X	L
H	X	X	L	X	X	H

H = High.  
 L = Low.  
 Z = High-impedance.  
 X = Don't care.



## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 17511 is a monolithic H-Bridge power IC applicable to small DC motors used in portable electronics. The 17511 can operate efficiently with supply voltages as low as 2.0 V to as high as 6.8 V, and it can provide continuous motor drive currents of 1.0 A while handling peak currents up to 3.0 A. It is easily interfaced to low-cost MCUs via parallel 3.0 V or 5.0 V compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz. The 17511 has four operating modes: Forward, Reverse, Brake, and Tri-State (high-impedance).

Basic protection and operational features (direction, dynamic braking, PWM control of speed and torque, main power supply undervoltage detection and shutdown, logic power supply undervoltage detection and shutdown), in addition to the 1.0 A rms output current capability, make the 17511 a very attractive, cost-effective solution for controlling a broad range of small DC motors. In addition, a pair of 17511 devices can be used to control bipolar step motors. The 17511 can also be used to excite transformer primary

windings with a switched square wave to produce secondary winding AC currents.

As shown in [Figure 2](#), the 17511 is a monolithic H-Bridge with built-in charge pump circuitry. For a DC motor to run, the input conditions need to be set as follows: enable input logic HIGH, one Input logic LOW, and the other input logic HIGH (to define output polarity). The 17511 can execute dynamic braking by setting both IN1 and IN2 logic HIGH, causing both low side MOSFETs in the output H-Bridge to turn ON. Dynamic braking can also be implemented by taking the enable logic LOW. The output of the H-Bridge can be set to an open-circuit high-impedance (Z) condition by taking both IN1 and IN2 logic LOW. (refer to [Table 6](#)).

The 17511 outputs are capable of providing a continuous DC load current of up to 1.2 A. An internal charge pump supports PWM frequencies to 200 kHz. The EN pin also controls the charge pump, turning it off when EN = LOW, thus placing the 17511 in a power-conserving sleep mode.

### FUNCTIONAL PIN DESCRIPTION

#### OUT1 AND OUT2

The OUT1 and OUT2 pins provide the connection to the internal power MOSFET H-Bridge of the IC. A typical load connected between these pins would be a small DC motor. These outputs connect to either VM or PGND, depending on the states of the control inputs (refer to [Table 6](#)).

#### PGND AND LGND

The power and logic ground pins (PGND and LGND) should be connected together with a very low-impedance connection.

#### CRES

The CRES pin provides the connection for the external reservoir capacitor (output of the charge pump). Alternatively this pin can also be used as an input to supply gate-drive voltage from an external source via a series current-limiting resistor. The voltage at the CRES pin is approximately three times the  $V_{DD}$  voltage, as the internal charge pump utilizes a voltage tripler circuit. The  $V_{CRES}$  voltage is used by the IC to supply gate drive for the internal power MOSFET H-Bridge.

#### VM

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the load attached between OUT1 and OUT2. All VM pins must be connected together on the printed circuit board with as short as possible traces offering as low-impedance as possible between pins.

VM has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

#### IN1, IN2, AND EN

The IN1, IN2, and EN pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1, IN2, and EN work together to control OUT1 and OUT2 (refer to [Table 6](#)).

#### $\overline{\text{GIN}}$

The  $\overline{\text{GIN}}$  input controls the GOUT pin. When  $\overline{\text{GIN}}$  is set logic LOW, GOUT supplies a level-shifted high side gate drive signal to an external MOSFET. When  $\overline{\text{GIN}}$  is set logic HIGH, GOUT is set to GND potential.

#### C1L AND C1H, C2L AND C2H

These two pairs of pins, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1  $\mu\text{F}$ .

#### GOUT

The GOUT output pin provides a level-shifted, high side gate drive signal to an external MOSFET with  $C_{ISS}$  up to 500 pF.

### $V_{DD}$

The VDD pin carries the 5.0 V supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state

condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

## TYPICAL APPLICATIONS

Figure 7 shows a typical application for the 17511. When applying the gate voltage to the CRES pin from an external

source, be sure to connect it via a resistor equal to, or greater than,  $R_G = V_{CRES}/0.02 \Omega$ .

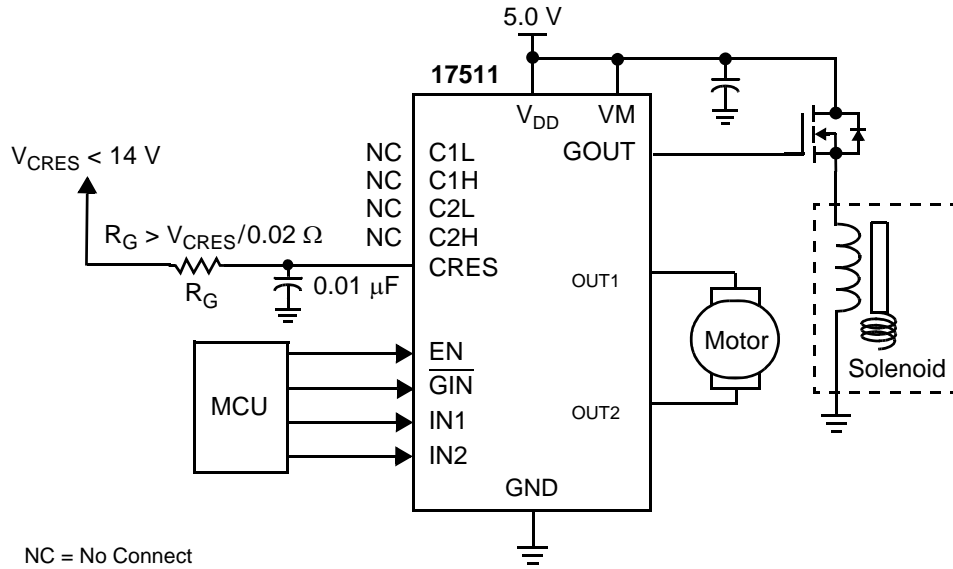


Figure 7. 17511 Typical Application Diagram

### CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients via placing a capacitor or zener at the supply pin (VM) (see Figure 8).

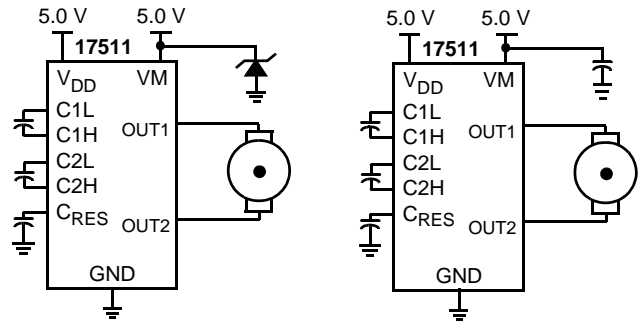
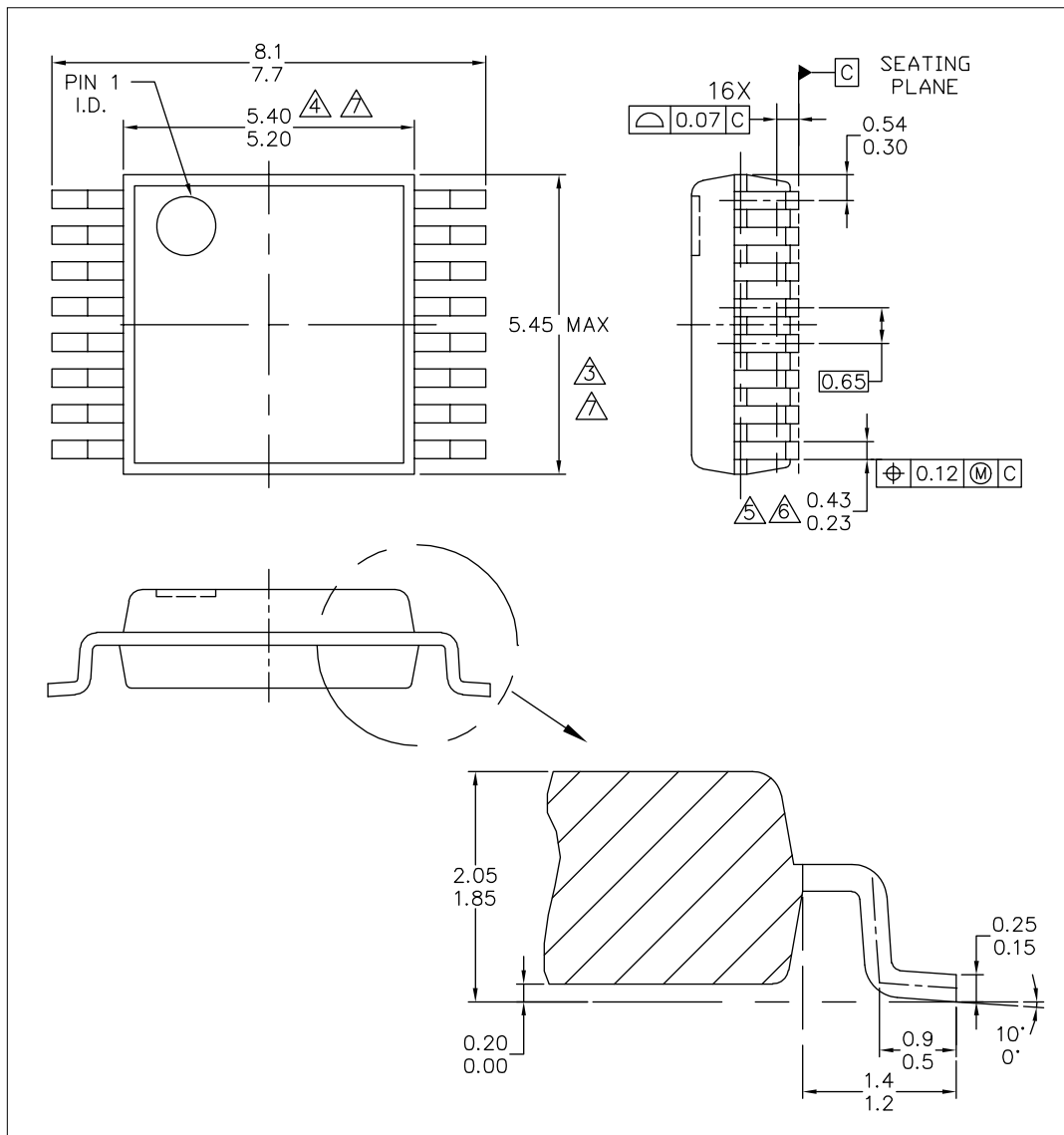


Figure 8. CEMF Snubbing Techniques

## PACKAGING

### PACKAGE DIMENSIONS

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TITLE: 16LD VMFP, 5.30 X 5.45 PKG 0.65 PITCH CASE OUTLINE	DOCUMENT NO: 98ASA10614D	REV: B
	CASE NUMBER: 1563-02	07 NOV 2007
	STANDARD: NON-JEDEC	

**EV (PB-FREE) SUFFIX**  
16-PIN VMFP  
98ASA10614D  
ISSUE B

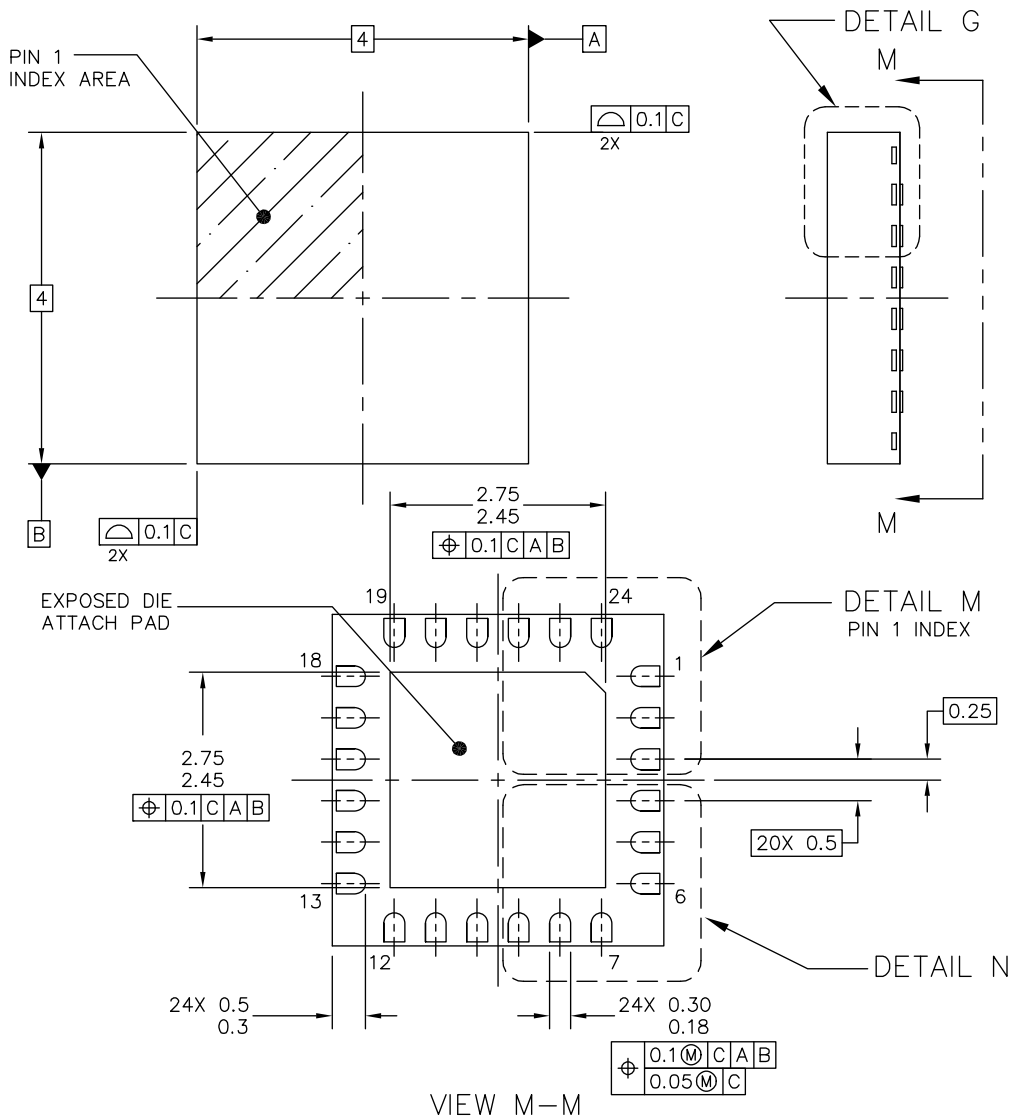
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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	CASE NUMBER: 1563-02	07 NOV 2007	
	STANDARD: NON-JEDEC		

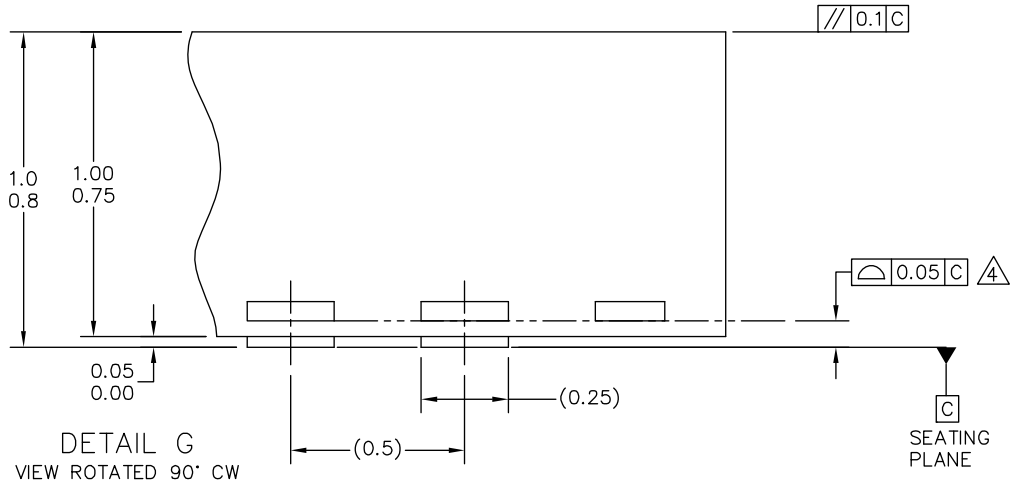
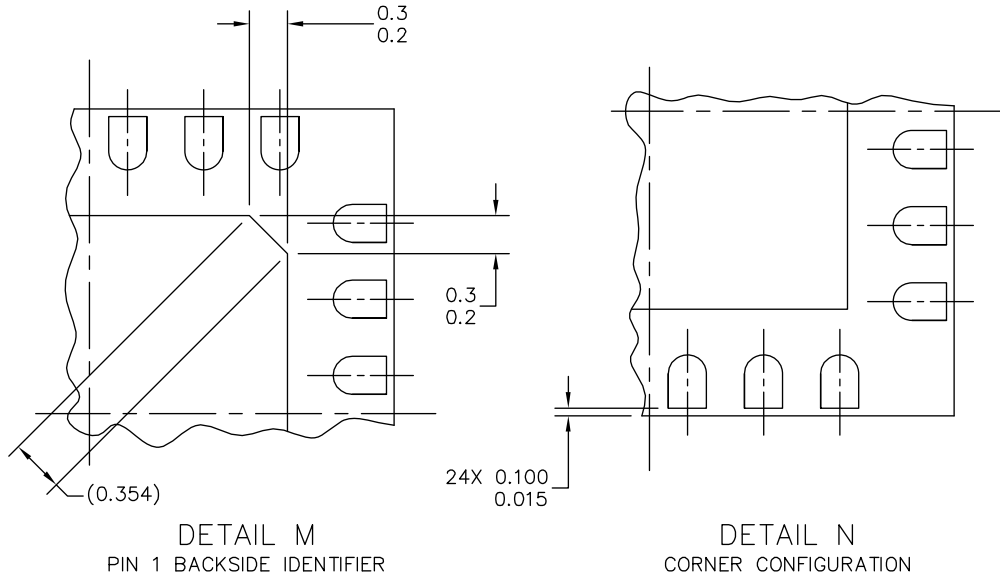
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PACKAGE DIMENSIONS (CONTINUED)



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	CASE NUMBER: 1508-02	28 DEC 2005
	STANDARD: NON-JEDEC	


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	CASE NUMBER: 1508-02	28 DEC 2005	
	STANDARD: NON-JEDEC		

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NOTES:

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2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFN.
4.  COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP SHOULD BE 0.2MM.

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TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 24 TERMINAL, 0.5 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARL10577D	REV: B	
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	STANDARD: NON-JEDEC		

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ISSUE B



## REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	7/2006	<ul style="list-style-type: none"><li>• Implemented Revision History page</li><li>• Converted to Freescale format</li></ul>
2.0	5/2010	<ul style="list-style-type: none"><li>• Updated Figures 1 and 2 to reflect correct pin names</li></ul>
3.0	10/2013	<ul style="list-style-type: none"><li>• Corrected Ordering information to MPC17511EP and MPC17511EV/EL</li><li>• Corrected packaging drawings to 98ASA10614D and 98ARL10577D</li><li>• Corrected Figure 1 and some text for <u>GIN</u></li><li>• Corrected page footers to 17511</li><li>• Corrected Table 6 - now on 1 page.</li></ul>



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