

MPC5748G EVB User Guide

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1. Introduction

This user guide details the setup and configuration of the Freescale MPC5748G customer Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy evaluation of the MPC5748G family of microcontrollers, and to facilitate hardware and software development. Various daughtercards are available which connect to the EVB via two high density connectors. Please consult your Freescale representative for more details on daughtercard pricing and availability.

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

This product contains components that may be damaged by electrostatic discharge. Observe precautions for handling electrostatic sensitive devices when using this EVB and associated microcontroller.

The user manual is intended to be read alongside the respective MCU documentation available at www.freescale.com and includes:

- Reference Manuals
- Product Data Sheets
- Application notes
- Chip Errata

1.1. Peripheral Daughtercards

The EVB has connectors for various peripheral daughtercards (for example MLB) that provide additional peripheral functionality. These are not supplied with the EVB and must be sourced separately. Please contact your Freescale representative for pricing and availability.

2. EVB Features

The EVB provides the following key features:

- Single 10-14 V DC external power supply input with on-board regulators to provide all of the necessary EVB and MCU voltages. Power may be supplied to the EVB via a 2.1 mm barrel style power jack or a 2-way screw type connector. 12 V operation allows in-car use if desired.
- Master power switch and regulator status LED's.
- USB Serial interface
- 2 x High Speed CAN transceiver routed to 3-way headers
- 2 x LIN interfaces routed to standard Molex headers
- Main clock supplied from on board crystal or SMA connector
- User reset switch with reset status LED's
- Ethernet PHY and RJ45 socket configurable as RMII or MII
- USB Type A Host interface
- USB Type AB (micro USB) OTG interface

- 2 x FlexRay interfaces with standard 2-pin connectors
- 14-pin JTAG and 50 pin Nexus (Trace) connectors
- 2 x High Density daughter card connectors allowing an MCU specific daughtercard to be fitted¹
- MLB daughtercard connector
- SAI Audio board connectors (2 x 0.1 inch pitch headers and 2 x TWRPI style headers)
- SD connector (mounted to the underside of the board) supporting hardware write protect and card detection
- 4 user LEDs wired to MCU ports, also available at a user header
- 4 user pushbutton switches wired to MCU ports, also available at a user header
- Hexadecimal encoded switch wired to 4 MCU ports, also available at a user header
- Simple potentiometer connected to analogue input channel

NOTE

To alleviate confusion between jumpers and connector headers, all EVB jumpers are 2 mm pitch whereas headers are 0.1 inch (2.54 mm). This prevents inadvertently fitting a jumper to a header.

¹ There is no MCU fitted to the EVB. A daughtercard must be fitted before the EVB can be used.

3. Configuration Overview

Throughout this document, all of the default jumper and switch settings are clearly marked with “(D)” and are shown in blue text. This allows a more rapid return to the default state of the EVB if required. Note that the default configuration for 3-way jumpers is a header fitted between pins 1 and 2. On the EVB, 2-way, and 3-way jumpers have been aligned such that pin1 is either to the top or to the left of the jumper. On 2-way jumpers, the source of the signal is connected to pin1.

The EVB has been designed with ease of use in mind and has been segmented into functional blocks as shown below. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

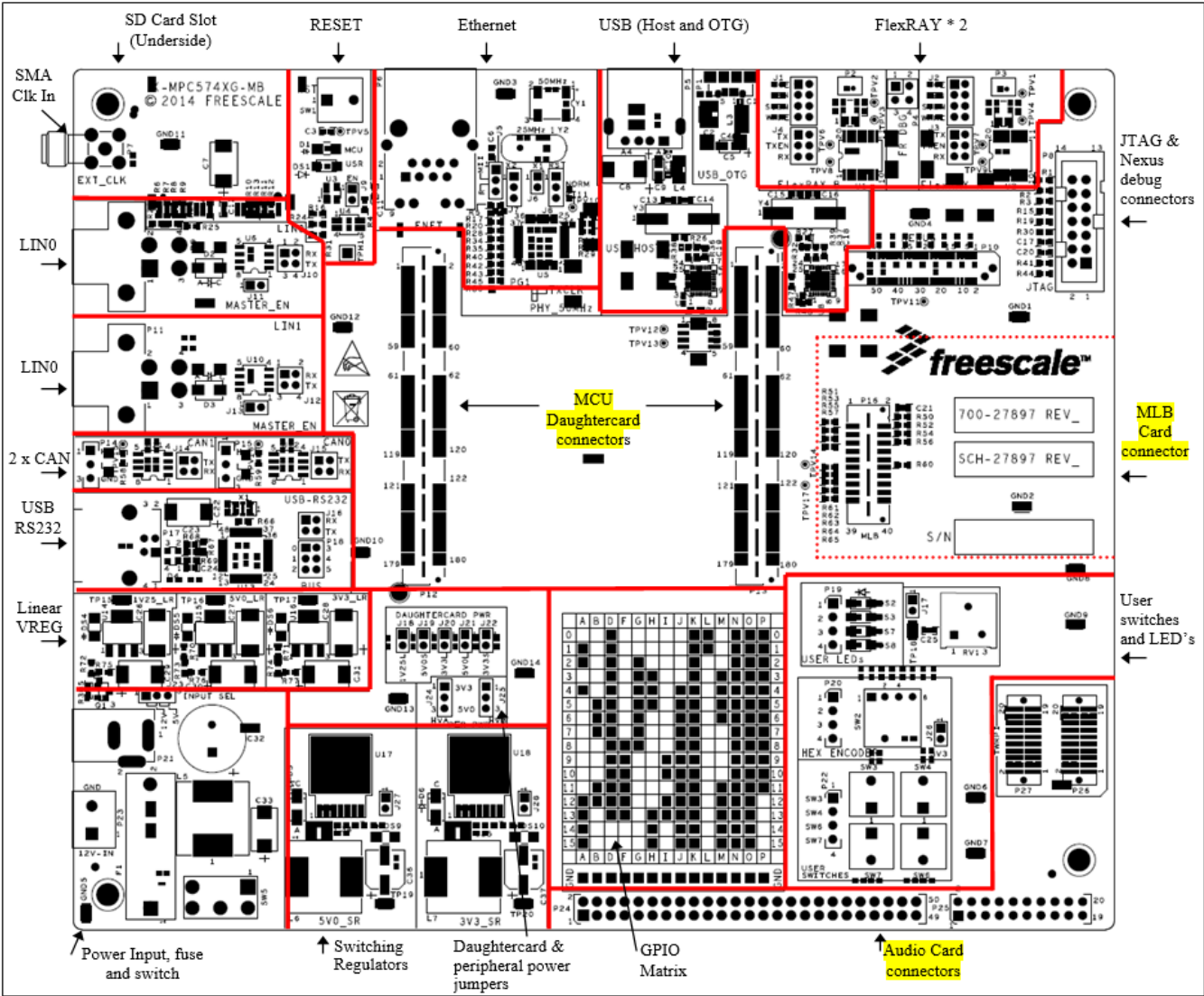


Figure 1. EVB Functional Blocks

4. MCU Daughtercard information

In order to use the EVB, an MCU daughtercard must be fitted as described in the following section. Before fitting or removing a daughtercard, ensure the EVB is powered OFF

4.1. Fitting a daughtercard

Gently place the daughtercard on the EVB connectors ensuring the correct orientation as shown in the following figure. The connectors are polarized so the daughtercard will only fit in one orientation (with the jumpers at the bottom of the daughtercard). Once the connectors have been located correctly, firmly push down all four corners of the daughter card simultaneously in order to ensure the connectors are mated. (The following picture also shows the default jumper positions for the 256BGA daughtercard)



Figure 2. Daughtercard Fitted to EVB

4.2. Removing a daughtercard

In order to prevent damage to the daughtercard connectors, it is important to remove the daughtercard correctly. Carefully lift either the top or bottom edge of the daughtercard and it should easily lift off as shown in the following figure (viewed from the left side of the EVB).



Figure 3. Removing a daughtercard

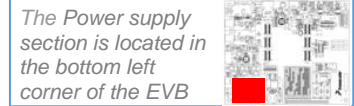
CAUTION

Do not attempt to lift the left or right edge of the daughtercard as this will result in connector damage.

5. Initial Configuration

This section details the power, reset, clocks, and debug configuration which is the minimum configuration needed in order to power ON the EVB.

5.1. Power Supply Configuration



The EVB requires an external power supply voltage of between 10 V-14 V DC (nominal 12 V), minimum 2 A. This allows the EVB to be used in a vehicle if required. The 12 V input is regulated on the EVB using two switching and three linear regulators to provide the required voltages of 5.0 V, 3.3 V (both linear and switcher) and 1.25 V (linear). For flexibility, there are two power supply input connectors on the EVB as detailed below:

5.1.1. Power Supply Connectors (P21, P23)

- **2.1 mm Barrel Connector – P21**

This connector should be used to connect the supplied wall-plug mains adapter. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1 mm plug uses the correct polarisation as shown below:

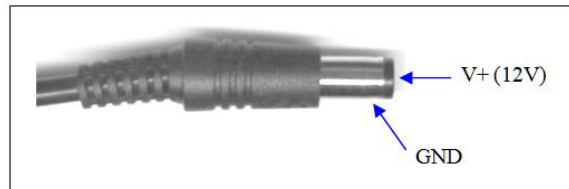


Figure 4. 2.1mm Power Connector

- **2-Way Screw Type Connector – P23**

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarisation of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

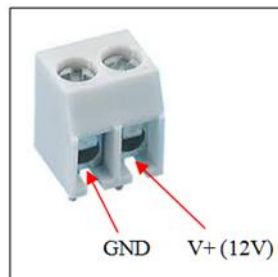


Figure 5. 2-Lever Power Connector

5.1.2. Power Switch (SW5)

Slide switch SW5 can be used to isolate the power supply input from the EVB voltage regulators if required.

- Moving the slide switch to the right (away from the fuse) will turn the EVB OFF.
- Moving the slide switch to the left (towards the fuse) will turn the EVB ON.

5.1.3. Regulator Power Jumper (J23)

All of the regulators are permanently powered from the main 12 V supply line and active with the exception of the 1.25 V linear regulator which has a 3-way jumper to allow selection of the input voltage.

The table below details the jumper configurations for the linear 1.25 V regulator source voltage. By default, the regulator is powered from the 12 V supply line.

Table 1. 1.25 V Linear Regulator Source Select (J23)

Jumper	Position	PCB Legend	Description
J23 (INPUT SEL)	1-2 (D)	12V	1.25V Linear regulator is powered from main 12V
	2-3	5V	1.25V Linear regulator is powered from 5V switching regulator output
	Removed		1.25V Linear regulator is not powered (disabled)

5.1.4. Power Status LED's and Fuse

When power is applied to the EVB, five green LED's adjacent to the voltage regulators show the presence of the supply voltages as follows:

- LED DS4 – Indicates that the 1.25V linear regulator is enabled and working correctly
- LED DS5 – Indicates that the 5.0V linear regulator is enabled and working correctly
- LED DS6 – Indicates that the 3.3V linear regulator is enabled and working correctly
- LED DS9 – Indicates that the 5.0V switching regulator is enabled and working correctly
- LED DS10 – Indicates that the 3.3V switching regulator is enabled and working correctly

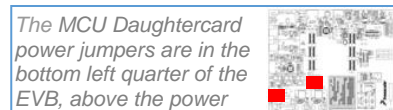
If no LED's are illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch SW5 is in the "OFF" position or that the fuse F1 has blown. The fuse is provided to protect the external power supply and for EVB circuitry reverse-bias protection. If the fuse has blown, check the polarity of your power supply and replace the fuse with a 20 mm 1.5 A fast blow fuse.

Note that the fuse will not protect against one of the EVB regulators being shorted. If this happens, damage is likely to occur to the EVB and / or components.

CAUTION

In the event of a short in the regulator output, the regulator and/or the shorted component may be hot

5.1.5. MCU Power Supply Jumpers (J18, J19, J20, J21, J22, J23)



All of the regulated power supplies are routed to the MCU daughtercard via jumpers. This allows each power supply to be individually isolated and facilitates current measurement at the respective jumper. Note that only the daughtercard is connected to the power lines after the jumpers so MCU current measurements are accurate. There are an additional two jumpers that control the voltages used by EVB peripherals connected to the VDD_HV_A and VDD_HV_B domains as described in section 5.1.7.

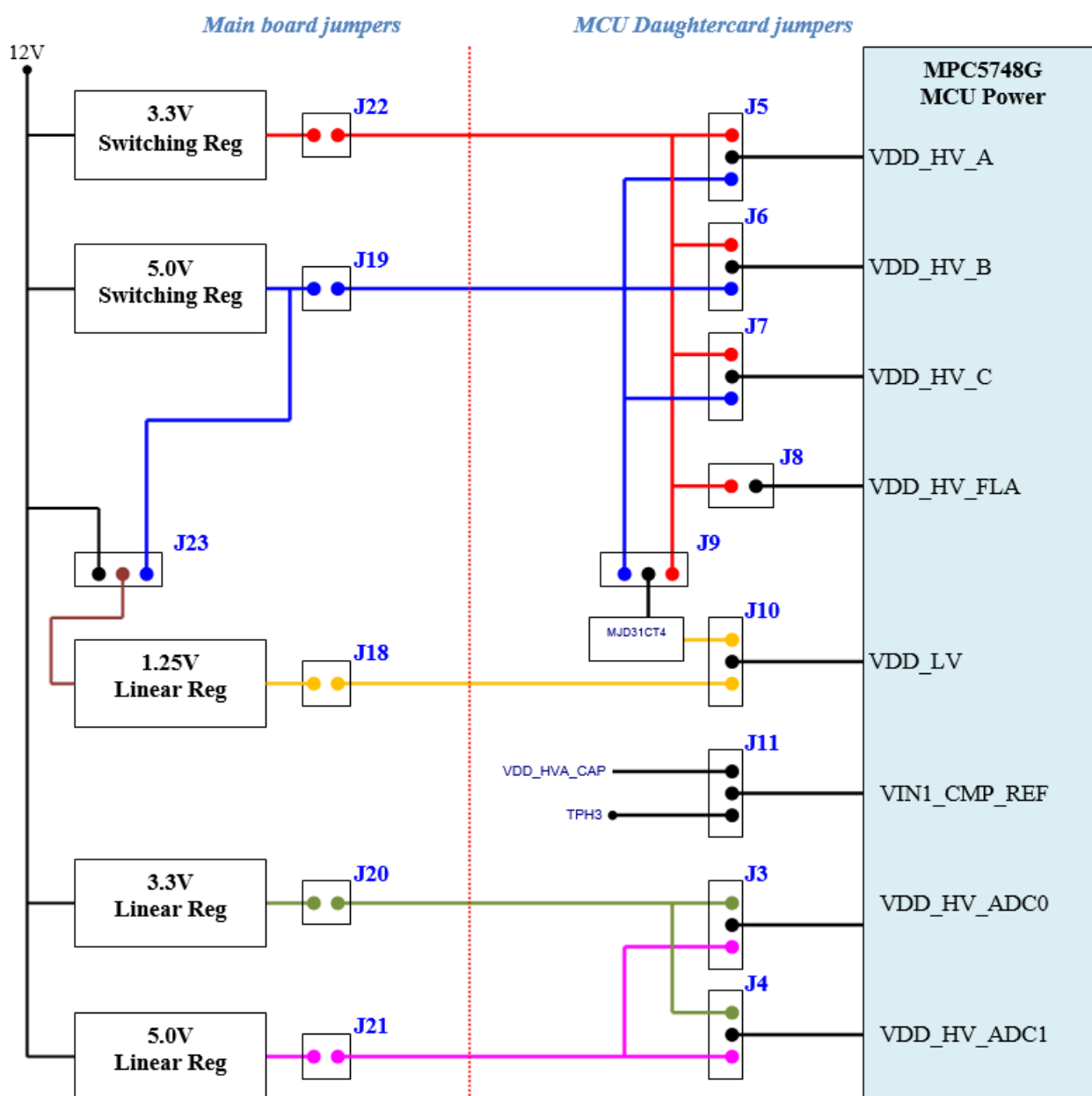


Figure 6. Power Supply Jumper Schematic

The power supply jumper description table is shown in the following table:

Table 2. Daughter Card Power Supply Jumpers (on main board)

Jumper	Position	PCB Legend	Description
J18 1V25L	Fitted (D)		1.25V Linear regulator output is routed to daughter card
	Removed		1.25V Linear regulator output is disconnected from daughtercard
J19 5V0S	Fitted (D)		5.0V Switching regulator output is routed to daughter card
	Removed		5.0V Switching regulator output is disconnected from daughtercard
J20 3V3L	Fitted (D)		3.3V Linear regulator output is routed to daughter card
	Removed		3.3V Linear regulator output is disconnected from daughtercard
J21 5V0L	Fitted (D)		5.0V Linear regulator output is routed to daughter card
	Removed		5.0V Linear regulator output is disconnected from daughtercard
J22 3V3S	Fitted (D)		3.3V Switching regulator output is routed to daughter card
	Removed		3.3V Switching regulator output is disconnected from daughtercard
J23 INPUT SEL (Above Power Jack)	1-2 (D)	12V	1.25v Linear regulator is powered by main 12V input
	2-3	5V	1.25v Linear regulator is powered by output from 5.0V switching reg
	Removed		1.25v Linear regulator is not powered (disabled)

5.1.6. Daughtercard Power Jumpers (J3 to J11)

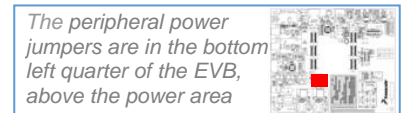
The following power control jumpers are located on the MCU daughtercard. Note that not all of the jumpers will be on each daughtercard variant.

Table 3. MCU Power Supply Jumpers (on daughtercard)

Jumper	Position	PCB Legend	Description
J3 ADC0	1-2 (D)	3V3	MCU ADC0 pin is connected to 3.3V (Linear)
	2-3	5V0	MCU ADC0 pin is connected to 5.0V (Linear)
	Removed		MCU ADC0 pin is not connected to power
J4 ADC1	1-2 (D)	3V3	MCU ADC1 pin is connected to 3.3V (Linear)
	2-3	5V0	MCU ADC1 pin is connected to 5.0V (Linear)
	Removed		MCU ADC1 pin is not connected to power
J5 HVA	1-2 (D)	3V3	MCU VDD_HV_A domain is connected to 3.3V (Switching Regulator)
	2-3	5V0	MCU VDD_HV_A domain is connected to 5.0V (Switching Regulator)
	Removed		MCU VDD_HV_A domain is not connected to power
J6 HVB	1-2 (D)	3V3	MCU VDD_HV_B domain is connected to 3.3V (Switching Regulator)
	2-3	5V0	MCU VDD_HV_B domain is connected to 5.0V (Switching Regulator)
	Removed		MCU VDD_HV_B domain is not connected to power
J7 HVC	1-2 (D)	3V3	MCU VDD_HV_C domain is connected to 3.3V (Switching Regulator)
	2-3	5V0	MCU VDD_HV_C domain is connected to 5.0V (Switching Regulator)
	Removed		MCU VDD_HV_C domain is not connected to power

Jumper	Position	PCB Legend	Description
J8² FLA	Fitted (D) Removed		MCU VDD_HV_FL A pin is connected to 3.3v (Switching Regulator) MCU VDD_HV_C domain is connected to 5.0V (Switching Regulator)
J9 REG	1-2 (D) 2-3 Removed	3V3 5V0	MCU ballast transistor collector is connected to 3.3V (Switching) MCU ballast transistor collector is connected to 5.0V(Switching) MCU ballast transistor collector is not connected to power
J10 VDDL V	1-2 (D) 2-3 Removed	REG 1V25L	MCU VDD_LV domain is powered from ballast transistor MCU VDD_LV domain is powered from 1.25V Linear regulator MCU VDD_LV domain is not powered
J11 DAC	1-2 (D) 2-3 Removed	HVA USR	MCU VIN1_CMP_REF is powered from VDD_HV_A MCU VIN1_CMP_REF is powered from user testpoint (TPH3) MCU VIN1_CMP_REF is not powered

5.1.7. Peripheral Power Supply Jumpers (J24, J25)



There are two additional power supply jumpers controlling the I/O voltage for the peripherals on the EVB in the HVA and HVB voltage domains.

The settings on these jumpers must match the VDD_HV_A and VDD_HV_B jumper voltage setting on the MCU daughtercard.

The default configuration matches the MCU daughtercard default configuration with both jumpers set to 3.3V.

Table 4. Peripheral Power Control (J24, J25)

Jumper	Position	PCB Legend	Description
J24 HVA	1-2 (D) 2-3 Removed	3V3 5V0	EV B peripherals in HVA domain are set to use I/O voltage of 3.3V EV B peripherals in HVA domain are set to use I/O voltage of 5.0V Invalid Configuration, avoid!
J25 HVB	1-2 (D) 2-3 Removed	3V3 5V0	EV B peripherals in HVB domain are set to use I/O voltage of 3.3V EV B peripherals in HVB domain are set to use I/O voltage of 5.0V Invalid Configuration, avoid!

5.1.8. EVB Voltage Regulators

The following table shows the usage of each EVB voltage regulator. This provides a useful cross reference point should any regulator be disabled. In addition, the distribution of the peripheral voltages HVA (J24) and HVB (J25) are shown.

² Note that jumper J8 (FLA) jumper must only be fitted when VDD_HV_A (J5) is connected to 3.3V.

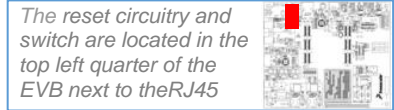
Table 5. Power Supply Distribution

Regulator	Used On
12V (Unregulated) P12V	All voltage regulators (switching and Linear, jumper selectable on 1.25V linear) 1.25V linear regulator LED supply via FET MCU Daughtercard connector MLB Daughtercard connector FlexRay transceiver VBAT pin
5.0V Switcher 5V0_SR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link) Peripheral power control jumpers (position 2-3) CAN transceivers VCC (main power) USB RS232 (FTDI) transceiver (main power and protection diode) USB Host / OTG transceiver power (VBAT) pin FlexRay Transceiver power pins (VCC / VBUF) SAI Audio connector Input to 1.25V linear regulator (in alternate jumper configuration)
3.3V Switcher 3V3_SR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link) Peripheral power control jumpers (position 1-2) Reset LED's (user and target) USB HOST / OTG transceiver I/O voltage (USB operation is fixed at 3.3V) ³ Ethernet Transceiver supply and I/O (Ethernet operation is fixed at 3.3V) ³ SAI Audio connector MLB Daughtercard connector SD Card power supply / pullup resistors (SD Card operation is fixed at 3.3V) ³ User LED's supply voltage Hex encoder switch supply voltage User pushbutton switches supply voltage
5.0V Linear 5V0_LR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link)
3.3V Linear 3V3_LR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link) MLB Daughtercard connector ADC Input Pot (user variable resistor)
1.25V Linear 1V25_LR	Daughtercard connector (post daughtercard power jumper) Daughtercard connector (direct feed via zero ohm link)
J24 PER_HVA	Reset control circuitry (including reset pullup) JTAG Pullup resistors & reference voltage CAN Transceiver I/O Voltage select LIN Transceiver Enable (and I/O voltage select) USB RS232 (FTDI) transceiver I/O voltage select FlexRay Transceiver I/O Voltage select (and pullups)
J25 PER_HVB	Nexus Connector reference voltage and Pullups

³ These voltages are fixed due to device specifications and cannot be changed.

Note that the JTAG pins are in domain VDD_HV_A whereas the Nexus pins are VDD_HV_B. Normally this would mean that for trace, the HVA and HVB domains should be at the same voltage however some development tools can automatically adapt to the voltages on the trace signals. Please consult your tools vendor for further details.

5.2. Reset Control (J9, SW1)



The MCU has a single bi-directional open drain Reset pin. Rather than connect multiple devices to the reset pin directly, a reset-in and reset-out buffering scheme has been implemented on the EVB as shown in Figure 7 below. The reset “in” from the reset switch (SW1) and the debug connectors are logically OR’d together using an AND gate and then connected to the buffer to provide an open-drain output.

The “reset-out” circuitry provides a buffered reset signal that can be used to drive any circuitry requiring a reset control from the MCU.

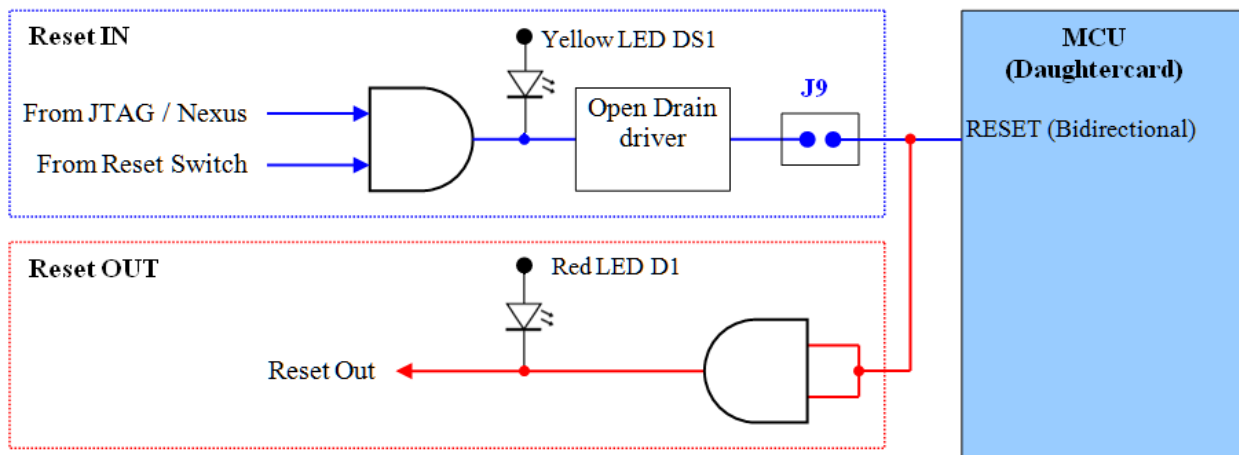


Figure 7. EVB Reset Control

Jumper J9 is used to disconnect the reset signal from the external reset sources if required.

Table 6. Reset Control (J9)

Jumper	Position	PCB Legend	Description
J9 (EN)	Fitted (D)		Reset from reset switch and debug connectors is active
	Removed		Reset from reset switch and debug connectors is inactive

Note that removing jumper J9 will mean that an external reset source will not reset the MCU. This will impact most debuggers which will typically issue a reset before establishing a debug connection.

5.2.1. Reset LEDs

As can be seen in Figure 7 above, there are two reset LED’s that can be used to identify the source / cause of a reset:

RED LED D1 (titled “MCU”) will illuminate if:

- The MCU issues a reset (in this condition ONLY this LED will be illuminated and LED DS1 will be off)
- There is a target reset (ie from the reset switch or from the debugger in which case LED DS1 will be ON)

YELLOW LED DS1 (titled “USR”) will illuminate when an external hardware device issues a reset to the MCU:

- The reset switch is pressed
- There is a reset being driven from one of the debug connectors

Table 7. Reset LED Decoding

LED DS1 (Yellow)	LED D1 (Red)	Description
OFF	OFF	No Reset being issued from MCU or external logic
OFF	ON	MCU has issued a reset
ON	OFF	External reset issued from switch or debug BUT not being issued to MCU (check J9 is fitted on the EVB)
ON	ON	External reset issued from reset switch or debug and has been issued to MCU.

5.3. MCU Clock Configuration

There are 2 clock configuration jumpers on the daughtercard and an external clock input connector on the main board to allow an externally generated clock to be supplied if desired. See Figure 8 below.

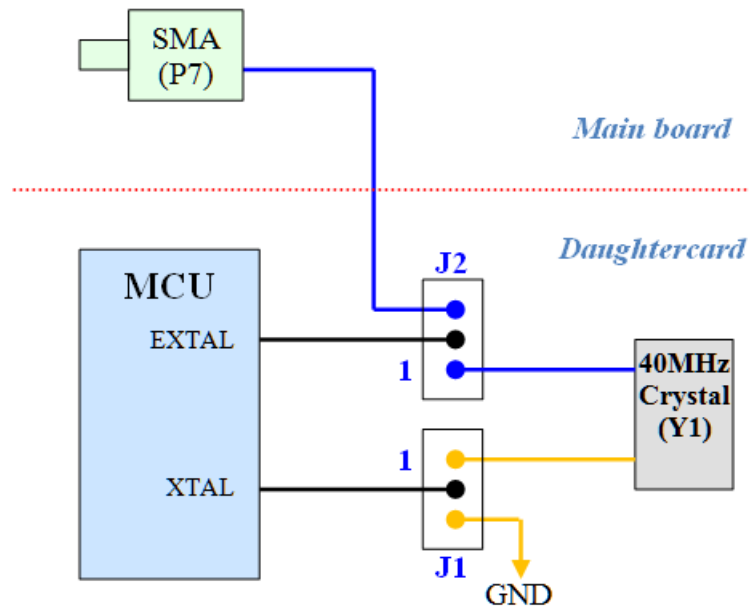


Figure 8. EVB Clock Selection

5.3.1. External Clock Input (P7)



The external clock input on the EVB is applied via SMA connector P7. When driving an external clock into the SMA connector, the jumpers on the daughtercard must be reconfigured to route the external clock to the MCU.

Note that the following conditions must be met when supplying an external clock:

- The clock frequency must be between 8MHz and 40MHz
- The amplitude of the clock input should not exceed the voltage being driven into the VDD_HV_A pins. This is selectable between 3.3V and 5.0V on the daughtercard.

5.3.2. MCU Clock Configuration (J1, J2 on Daughtercard)

There are two external clock crystals on the MPC5748G daughtercards:

- 40MHz fast external crystal for clocking the main system clock
- 32KHz slow external crystal for accurate time of day keeping

The 40MHz crystal is connected to the MCU XTAL and EXTAL pins via 3-way jumper headers as shown in the diagram above. These jumpers allow an external clock to be routed from the SMA connector (P7) on the main board if desired. The default configuration is with both daughtercard jumpers (J1 and J2) set to position 1-2 which routes the external 40MHz crystal to the MCU pins. If you wish to supply a clock via the SMA connector on the main EVB, move the daughtercard jumpers J1 and J2 to position 2-3.

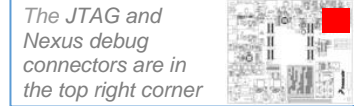
The 32 KHz external crystal is permanently connected to the MCU EXTAL32 and XTAL32 pins and has no configuration options.

Table 8. EXTAL Clock Source Selection (J1, J2 Daughtercard)

Jumper	Position	PCB Legend	Description
J1 (XTAL)	1-2 (D)	Y1	MCU XTAL signal is routed to crystal Y1
	2-3	GND	MCU XTAL signal is Grounded (for ext clock mode) ⁴
J2 (EXTAL)	1-2 (D)	Y1	MCU EXTAL signal is routed to crystal Y1
	2-3	EXT	MCU EXTAL signal is routed from EVB SMA P7

⁴ Note that the XTAL pin is left open by default with J1 in position 2-3. Resistor R34 must be populated with a zero ohm resistor in order to ground the XTAL pin.

5.4. Debug Connectors (P8, P10)



The EVB provides two debug connectors:

- Standard 14 pin JTAG
- 50 Pin Nexus connector (Samtec ASP-148422-01, Nexus Standard HP50 connector)

There is no user configuration required to use the connectors however the following points should be noted:

- The JTAG connector is routed to the JTAG signals in the default position which are powered from the MCU VDD_HV_A power domain. The Nexus signals are located in the VDD_HV_B power domain. If you are using Nexus, you may have to ensure that the VDD_HV_A and VDD_HV_B domains are at the same voltage. Consult your tools vendor for specific information
- The Nexus signals are not bonded out in every MCU package. Before using Nexus, please ensure the MCU fitted to the EVB (via the daughtercard) supports the Nexus signals.

5.4.1. Debug Connector Pinouts

The following tables list the pinouts for each of the debug connectors used on the EVB

Table 9. 14-Pin JTAG Debug Connector Pinout

Pin No	Function	Connection	Pin No	Function	Connection
1	TDI	PC0	2	GND	GND
3	TDO	PC1	4	GND	GND
5	TCLK	PH9	6	GND	GND
7	EVTI	PL8	8	N/C	---
9	RESET	JTAG-RSTx	10	TMS	PH10
11	VREF	PER_HVA	12	GND	GND
13	RDY	---	14	JCOMP	10K Pulldown

Table 10. 50-pin Samtec (Nexus) Debug Connector Pinout

Pin No	Function	Connection	Pin No	Function	Connection
1	MSEO_0	PL9	2	VREF	PER_HVB
3	MSEO_1	PL11	4	TCK	PH9
5	GND	GND	6	TMS	PH10
7	MDO0	PL2	8	TDI	PC0
9	MDO1	PL3	10	TDO	PC1
11	GND	GND	12	JCOMP	10K Pulldown
13	MDO2	PL4	14	RDY	---
15	MDO3	PL5	16	EVTI	PL8
17	GND	GND	18	EVTO	PL12
19	MCKO	PL10	20	RESET	DEBUG_RST
21	MDO4	PL6	22	RST_OUT	MCU_RST
23	GND	GND	24	GND	GND
25	MDO5	PL7	26	CLKOUT	Test Point
27	MDO6	PL13	28	TD/WT	---
29	GND	GND	30	GND	GND

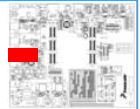
Pin No	Function	Connection	Pin No	Function	Connection
31	MDO7	PL14	32	DAI1	---
33	MDO8	PL15	34	DAI2	---
35	GND	GND	36	GND	GND
37	MDO9	PM0	38	ARBREQ	---
39	MDO10	PM1	40	ARBGRT	---
41	GND	GND	42	GND	GND
43	MD011	PM2	44	MDO13	PM8
45	MDO12	PM7	46	MDO14	PM9
47	GND	GND	48	GND	GND
49	MDO15	PM10	50	N/C	---

6. Communications & Memory Interfaces:

This section details the communication interface and storage peripherals that are implemented on the EVB.

6.1. CAN Interfaces (P14, P15, J14, J15)

The CAN Physical interface circuits are located on the left edge of the EVB



The EVB incorporates two identical CAN interface circuits connected to MCU CAN0 and CAN1 using MC33901 transceivers. Both transceivers are configured for high speed operation by pulling pin 8 to GND via a 4.7K Ohm resistor. There are test points to allow the Select pin to be driven high if desired. The MC33901 is pin compatible with other CAN transceivers supporting full CAN FD data rates.

For flexibility, the CAN transceiver I/O is connected to a standard 0.1" connector (P14 for CAN1 / P15 for CAN0) rather than using non standard DB9 connectors. The pinout of these headers is shown below and is also detailed on the PCB silkscreen

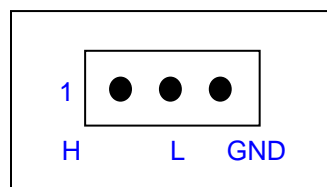


Figure 9. CAN Physical Interface Connectors

The CAN0 and CAN1 MCU TX/RX signals are jumpered as shown in the table below to allow the transceivers to be isolated from the respective MCU pin if desired. The default configuration is with all jumper headers fitted routing the TX and RX signals to the MCU.

Table 11. CAN Control Jumpers (J51, J53)

Jumper	Position	PCB Legend	Description
J15 (CAN0) Posn 1-2	FITTED (D) Removed	TX	MCU CAN0_TX signal (PB0) is routed to CAN interface MCU CAN0_TX signal (PB0) is not routed to CAN interface
J15 (CAN0) Posn 3-4	FITTED (D) Removed	RX	MCU CAN0_RX signal (PB1) is routed to CAN interface MCU CAN0_RX signal (PB1) is not routed to CAN interface
J14 (CAN1) Posn 1-2	FITTED (D) Removed	TX	MCU CAN1_TX signal (PC10) is routed to CAN interface MCU CAN1_TX signal (PC10) is not routed to CAN interface
J14 (CAN1) Posn 3-4	FITTED (D) Removed	RX	MCU CAN1_RX signal (PC11) is routed to CAN interface MCU CAN1_RX signal (PC11) is not routed to CAN interface


NOTE

Care should be taken when fitting the jumper headers to the 2x2 jumper blocks J14 and J15 as they can easily be fitted in the incorrect orientation. Jumper headers should be fitted **horizontally**.

The CAN TX / RX MCU pins are powered from the VDD_HV_A domain, which is configured between 3.3V and 5.0V on the daughtercard using jumper J5. The CAN transceivers I/O voltage is connected to the PER_HVA net configured with jumper J24 on the main EVB. Care must be taken to ensure that the MCU VDD_HV_A and PER_HVA supplies are the same when using the CAN transceiver.

6.2. LIN Interfaces (P9, P11, J10, J12)

The LIN Physical interface circuits are located on the left edge of the EVB



The EVB incorporates two identical LIN transceiver circuits connected to MCU LIN0 and LIN1 using a Freescale MC33662LEF transceiver supporting both master and slave mode (jumper selectable)

The output from the LIN transceiver is connected to a standard 4-pin Molex connector as used on most other Freescale EVB's supporting LIN as shown in the following figure:

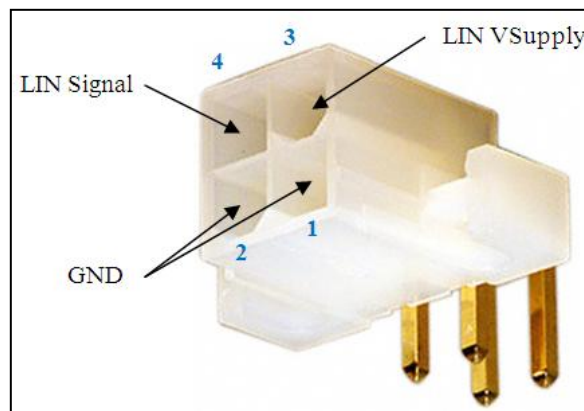


Figure 10. LIN Molex Physical Interface Connector

The LIN0 and LIN1 MCU TX/RX signals are jumpered as shown in the following to allow the transceivers to be isolated from the respective MCU pin if desired. The default configuration is with all jumper headers fitted routing the TX and RX signals to the MCU.

Each transceiver also has a master mode enable jumper which is fitted by default to configure the transceiver for Master mode. To configure the transceiver for slave mode, remove the respective “Master_EN” jumper.

Table 12. LIN Control Jumpers (J10, J11, J12, J13)

Jumper	Position	PCB Legend	Description
J10 (LIN0) Posn 1-2	FITTED (D) Removed	RX	MCU LIN0_RX signal (PB3) is routed to LIN0 interface MCU LIN0_RX signal (PB3) is not routed to LIN0 interface
J10 (LIN0) Posn 3-4	FITTED (D) Removed	TX	MCU LIN0_TX signal (PB2) is routed to LIN0 interface MCU LIN0_TX signal (PB2) is not routed to LIN0 interface
J11 (Master_EN)	FITTED (D) Removed		LIN0 is configured in Master Mode LIN0 is configured in Slave Mode
J12 (LIN1) Posn 1-2	FITTED (D) Removed	RX	MCU LIN1_TX signal (PC7) is routed to LIN1 interface MCU LIN1_TX signal (PC7) is not routed to LIN1 interface
J12 (LIN1) Posn 3-4	FITTED (D) Removed	TX	MCU LIN1_RX signal (PC6) is routed to LIN interface MCU LIN1_RX signal (PC6) is not routed to LIN interface
J13 (Master_EN)	FITTED (D) Removed		LIN1 is configured in Master Mode LIN1 is configured in Slave Mode

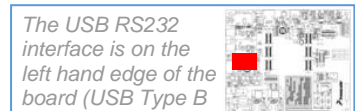
NOTE

Care should be taken when fitting the jumper headers to the 2x2 jumper blocks J10 and J12 as they can easily be fitted in the incorrect orientation. Jumper headers should be fitted **horizontally**

The LIN TX / RX MCU pins are powered from the VDD_HV_A domain, which is configured between 3.3V and 5.0V on the daughtercard using jumper J5. The LIN transceivers enable pin is connected to the PER_HVA net configured with jumper J24 on the main EVB. Care must be taken to ensure that the MCU VDD_HV_A and PER_HVA supplies are the same when using the LIN transceiver.

Note that in order for the LIN transceiver to function, external power must be supplied via pin 3 of the molex connector as detailed in Figure 10.

6.3. USB RS232 Serial Interface (P17, J16)



The EVB incorporates a USB RS232 serial interface providing RS232 connectivity via a direct USB connection between the PC and the EVB. The circuit contains an FTDI FT2232D USB to Serial interface which should automatically install the drivers for two additional COM ports on your PC. Note that only one of these is used so you will need to try both (usually the higher numbered COM port is the active one). For more information on the USB drivers and general fault finding, consult the FTDI website at <http://www.ftdichip.com/>

The MCU LIN2 signals are routed to the FTDI transceiver via a 2-way jumper header (J16) allowing the transceiver to be isolated from the MCU pin if desired. The default configuration is with the jumper

header fitted, routing the TX and RX signals from the MCU to the FTDI transceiver. No other configuration is required.

Table 13. USB RS232 Control Jumpers

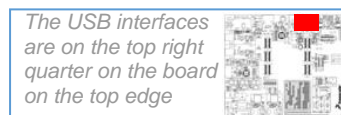
Jumper	Position	PCB Legend	Description
J16 Posn 1-2	FITTED (D) Removed	RX	MCU LIN2_RX signal (PC9) is routed to the FTDI interface MCU LIN2_RX signal (PC9) is not routed to the FTDI interface
J16 Posn 3-4	FITTED (D) Removed	TX	MCU LIN2_TX signal (PC8) is routed to the FTDI interface MCU LIN2_TX signal (PC8) is not routed to the FTDI interface

NOTE

Care should be taken when fitting the jumper headers to the 2x2 jumper block J16 as they can easily be fitted in the incorrect orientation. Jumper headers should be fitted **horizontally**.

The MCU LIN2 (SCI) pins are powered from the VDD_HV_A domain, which is configured between 3.3V and 5.0V on the daughtercard using jumper J5. The FTDI transceiver I/O voltage pin is connected to the PER_HVA net configured with jumper J24 on the main EVB. Care must be taken to ensure that the MCU VDD_HV_A and PER_HVA supplies are the same when using the FTDI transceiver.

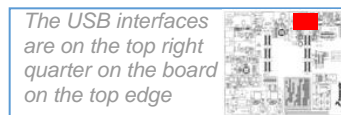
6.4. USB HOST / OTG Interfaces



The EVB includes Type A (Host) and Type AB (OTG) USB interfaces, routed to standard and micro USB sockets respectively. Each USB circuit contains a USB83340 transceiver with a shared USB power switch. There is no user configuration required on either of the USB circuits.

The USB transceivers have a 3.3V (only) interface. All of the USB0 (connected to the OTG transceiver) and USB1 (connected to the HOST transceiver) signals are in the VDD_HV_A domain and must be configured as 3.3V via daughtercard jumper J5. If VDD_HV_A is set to 5V, the USB0 and USB1 MCU signals should be left tri-stated to prevent damage to the USB transceivers.

6.5. Ethernet (P6, J5, J6, J7, J8, R45, R80)



The MPC5748G supports both MII and RMII Ethernet interfaces. The EVB incorporates a DP83848c transceiver supporting both MII and RMII modes. The transceiver is connected to a pulse J1011F21PNL RJ45 connector which includes a built-in isolation transformer.

The default configuration, with all 2-way jumpers fitted and all 3-way jumpers in position 1-2, configures the transceiver for MII mode with the reset signal to the PHY being driven from the MCU Reset out (eg any reset causing the MCU Reset line to assert will reset the PHY)

In order to configure the EVB for RMII mode, jumpers J5, J6 and J7 need to be changed as described in Table 14 below. In addition, a surface mount 0Ω resistor needs to be de-soldered and moved as shown in the figure below. This option is fitted as a resistor instead of a jumper to maintain signal integrity on the Ethernet clock signal.

For MII mode (default) R45 should have a jumper populated as shown. For RMII mode, remove R45 and fit it between R45 and R80

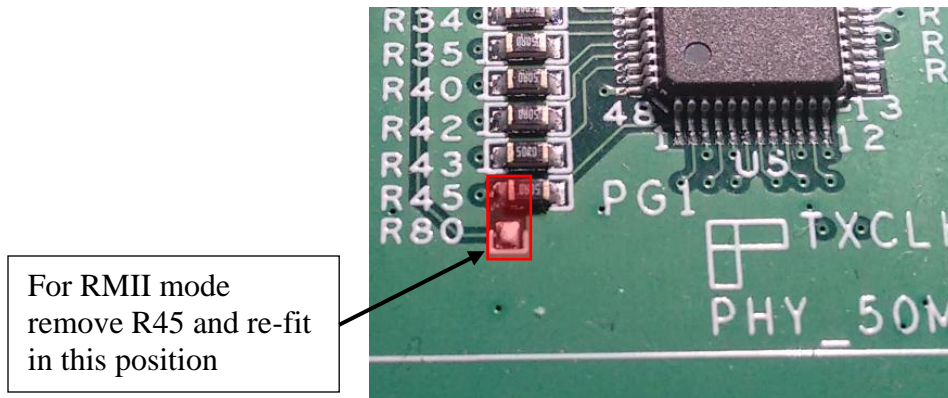


Figure 11. MII / RMII Clock Selection Resistor

To change the reset routing so that the Ethernet PHY can be reset via MCU pin PI11 (rather than being tied to the MCU reset), jumper J8 should be moved to position 2-3

Table 14. Ethernet Control jumpers (J5, J6, J7, J8, R45, R80)

Jumper	Position	PCB Legend	Description
J5	1-2 (D)	MII	Ethernet PHY is configured in MII mode
	2-3	R	Ethernet PHY is configured in RMII mode
	Removed		Invalid Configuration, avoid!
J6 (X1)	1-2 (D)		Ethernet PHY X2 clock is connected to 25MHz xtal
	2-3		Ethernet PHY X2 clock is not connected to 25MHz xtal ^{5, 6}
J7 (X2)	1-2 (D)		Ethernet PHY X1 clock is connected to 25MHz xtal
	2-3		Ethernet PHY X1 clock is driven from 50MHz xtal
	Removed		Ethernet PHY X1 clock is disconnected (invalid configuration, avoid)
J8 (RST)	1-2 (D)	NORM	The Ethernet PHY will be reset along with MCU reset
	2-3	PI11	The Ethernet PHY reset is controlled via MCU pin PI11 (Pulled high)
	Removed		Invalid Configuration, avoid!
R45 (R80)	Fitted R45		MII Mode – Clock is supplied from PHY to MCU
	R45 to R80		RMII Mode – Clock is supplied from external 50MHz oscillator to MCU

The MCU Ethernet signals are all in the VDD_HV_B domain. The Ethernet PHY will ONLY function with 3.3V I/O so VDD_HV_B must be set to 3.3V on the MCU daughtercard before the Ethernet is used. If VDD_HV_B is set to 5V, the signals routed to the Ethernet PHY (see the EVB schematics) must be left as tristate.

⁵ If jumper J7 is in position 1-2 (25MHz XTAL), J6 must be fitted and R45 must be fitted.

⁶ If jumper J7 is in position 2-3 (50MHz oscillator), J6 must be removed and R45 must be removed and placed between R45 and R80

6.6. FlexRay (P2, P3, J1, J2, J3, J4)



The EVB incorporates two FlexRay TJA1080TS/N interfaces connected to MCU FlexRay channels A and B and routed to two Molex 1.25mm pitch PicoBlade shrouded headers (standard on many Freescale EVB's). Jumpers are provided to disconnect the MCU signals from the FlexRay interface if required as well as providing general configuration.

By default, all of the jumper headers are fitted which routes the MCU signals to the FlexRay physical interface as well as configuring the controller for a default mode of operation (Transmitter enabled, Receiver enabled, not in low power mode). Please consult the FlexRay transceiver and general FlexRay specifications before changing any of the mode jumpers.

Table 15. FlexRay Configuration Jumpers (J1, J2, J3, J4)

Jumper	Position	PCB Legend	Description
FlexRay A			
J3 Posn 1-2	FITTED (D) Removed	TX	MCU PC5 is connected to FlexRay A transceiver TX MCU PC5 is not connected to FlexRay A transceiver TX
J3 Posn 3-4	FITTED (D) Removed	TXEN	MCU PE2 is connected to FlexRay A transceiver TXEN MCU PE2 is not connected to FlexRay A transceiver TXEN
J3 Posn 5-6	FITTED (D) Removed	RX	MCU PE3 is connected to FlexRay A transceiver RX MCU PE3 is not connected to FlexRay A transceiver RX
J2 Posn 1-2	FITTED (D) Removed	BGE	FlexRay A PHY Bus Guardian Enable (Transmitter is enabled) FlexRay A PHY transmitter is disabled (Receive only mode)
J2 Posn 3-4	FITTED (D) Removed	EN	FlexRay A PHY is enabled FlexRay A PHY is disabled
J2 Posn 5-6	FITTED (D) Removed	STBN	FlexRay A PHY will not enter Standby Mode FlexRay A PHY will enter Standby Mode
J2 Posn 7-8	FITTED (D) Removed	WAKE	FlexRay A PHY Wakeup signal pulled low FlexRay A PHY Wakeup signal pulled high
FlexRay B			
J4 Posn 1-2	FITTED (D) Removed	TX	MCU PE4 is connected to FlexRay B transceiver TX MCU PE4 is not connected to FlexRay B transceiver TX
J4 Posn 3-4	FITTED (D) Removed	TXEN	MCU PC4 is connected to FlexRay B transceiver TXEN MCU PC4 is not connected to FlexRay B transceiver TXEN
J4 Posn 5-6	FITTED (D) Removed	RX	MCU PE5 is connected to FlexRay B transceiver RX MCU PE5 is not connected to FlexRay B transceiver RX
J1 Posn 1-2	FITTED (D) Removed	BGE	FlexRay B PHY Bus Guardian Enable (Transmitter is enabled) FlexRay B PHY transmitter is disabled (Receive only mode)
J1 Posn 3-4	FITTED (D) Removed	EN	FlexRay B PHY is enabled FlexRay B PHY is disabled
J1 Posn 5-6	FITTED (D) Removed	STBN	FlexRay B PHY will not enter Standby Mode FlexRay B PHY will enter Standby Mode
J1 Posn 7-8	FITTED (D) Removed	WAKE	FlexRay B PHY Wakeup signal pulled low FlexRay B PHY Wakeup signal pulled high

The MCU FlexRay pins are powered from the VDD_HV_A domain, which is configured between 3.3V and 5.0 V on the daughtercard using jumper J5. The FlexRay transceivers I/O voltage pin is connected to the PER_HVA net configured with jumper J24 on the main EVB. Care must be taken to ensure that the MCU VDD_HV_A and PER_HVA supplies are the same when using the FlexRay transceiver.

Important:

The EVB daughtercards are supplied with a 40 MHz crystal which is a requirement for FlexRay in order to generate the correct clock timing. If you have changed the default crystal on the daughtercard and wish to use FlexRay, you must ensure a 40 MHz crystal is fitted.

6.7. SD Card Socket (P200)

The SD socket is mounted on the underside of the board in the top left



The EVB supports a 4-bit SD interface (note that MPC5748G supports 8-bit SD data) which is routed to a full sized SD card connector on the underside of the EVB. There is no user configuration required.

The SD socket has hardware card detection (routed to PA0) and write protection (routed to PH8) status outputs which will be grounded when active.

The MCU SD card signals are all in the VDD_HV_A domain. The SD card specification is for an interface voltage of between 2.7V and 3.6V so the SD card can only be used when VDD_HV_A is set to 3.3V (PER_HVA has no impact on the voltage on the SD card)

CAUTION

If VDD_HV_A is set to 5V, damage may be caused to an SD card if an attempt is made to access it in software. If you need to leave the SD card in the socket with VDD_HV_A set to 5V, ensure all the SD card pads are left as high impedance

7. AV Interface Connectors

This section details the Audio / Video interface connectors on the EVB. Each of these connectors can be used to add additional daughtercards (not supplied) to add functionality.

7.1. SAI Audio Connectors (P24, P25)

The SAI audio connector is on the bottom edge of the EVB



The EVB includes two 0.1" headers that can be used to interface to an SAI audio board (available separately, please consult your Freescale representative). There is no EVB configuration required when using these connectors other than to ensure the EVB is switched off prior to fitting or removing the daughtercard.

The pinout of the connectors is shown below for reference and these connectors can also be used for GPIO connectivity

Table 16. 50-pin SAI Audio Daughtercard Connector P24

Pin No	Function	Connection	Pin No	Function	Connection
1	3.3V	3V3_SR	2	GND	GND
3	SAI0_DATA3	PF2	4	GND	GND
5	SAI0_DATA2	PF3	6	GND	GND
7	SAI0_DATA1	PF4	8	GND	GND
9	SAI0_DATA0	PF5	10	GND	GND
11	SAI0_BCLK	PF1	12	GND	GND
13	SAI0_SYNC	PB10	14	GND	GND
15	SAI0_MCLK	PF0	16	GND	GND
17	eMIOS1_7H	PH5	18	GND	GND
19	I2C_SCL3	PE11	20	GND	GND
21	I2C_SDA3	PE10	22	GND	GND
23	SAI1_DATA0	PJ2	24	GND	GND
25	SAI1_BCLK	PJ3	26	GND	GND
27	eMIOS1_6H	PH4	28	GND	GND
29	SAI1_SYNC	PF6	30	GND	GND
31	SAI1_MCLK	PF7	32	GND	GND
33	I2C_SCL2	PE9	34	GND	GND
35	I2C_SDA2	PE8	36	GND	GND
37	SAI2_DATA0	PI14	38	GND	GND
39	SAI2_BCLK	PJ1	40	GND	GND
41	SAI2_SYNC	PJ0	42	GND	GND
43	SAI2_MCLK	PI15	44	GND	GND
45	eMIOS1_5H	PH3	46	GND	GND
47	GPIO Control	PA5	48	GND	GND
49	5.0V	5V0_SR	50	GND	GND

Table 17. 20-pin SAI Audio Daughtercard Connector P25

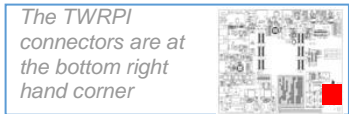
Pin No	Function	Connection	Pin No	Function	Connection
1	N/C	N/C	2	GND	GND
3	DSPI0_SIN	PA12	4	GND	GND
5	DSPI0_SOUT	PA13	6	GND	GND
7	DSPI0_SCK	PA14	8	GND	GND
9	DSPI0_SS0	PA15	10	GND	GND
11	DSPI3_SOUT	PG2	12	GND	GND
13	DSPI3_SS3	PG3	14	GND	GND
15	DSPI3_SCK	PG4	16	GND	GND
17	DSPI3_SIN	PG5	18	GND	GND
19	N/C	N/C	20	GND	GND

Note that connector P25 is not populated and must be fitted if required

CAUTION

Before the daughtercard is installed or removed, the EVB must be powered OFF to prevent potential damage to the EVB or daughter card components.

7.2. TWRPI Connectors (P26, P27)



The EVB includes two fine pitch TWRPI headers that can be used to interface to an SAI audio board (available separately, please consult your Freescale representative) along with the 0.1” headers mentioned in the section above. There is no EVB configuration required when using these connectors other than to ensure the EVB is switched off prior to fitting or removing the daughtercard. The pinout of the connectors is shown below for reference.

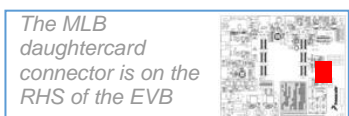
Table 18. TWRPI Connector P26

Pin No	Function	Connection	Pin No	Function	Connection
1	5V	5V0_SR	2	3.3V	3V3_SR
3	GND	GND	4	3.3V	3V3_LR
5	GND	GND	6	GND	GND
7	GND	GND	8	ADC0	PD5
9	ADC1	PD6	10	GND	GND
11	GND	GND	12	ADC2	PD4
13	GND	GND	14	GND	GND
15	GND	GND	16	GND	GND
17	ID0	PD7 ⁷	18	ID1 ⁷	PD8
19	GND	GND	20		

Table 19. TWRPI Connector P27

Pin No	Function	Connection	Pin No	Function	Connection
1	GND	GND	2	GND	GND
3	I2C0_SCL	PO0	4	I2C0_SDA	PO1
5	GND	GND	6	GND	GND
7	GND	GND	8	GND	GND
9	DSPIO_SIN	PA12	10	DSPIO_SOUT	PA13
11	DSPIO_SS0	PA15	12	DSPIO_SCK	PA14
13	GND	GND	14	GND	GND
15	GPIO0/IRQ	PK3	16	GPIO1	PK0
17	GPIO2	PK1	18	GPIO3	PK2
19	GPIO4	PK4	20	N/C	N/C

7.3. MLB Daughtercard Connector (P16)



There is a 40-pin interface connector on the EVB for connecting an MLB (Media Local Bus) daughtercard. There is no hardware configuration possible at EVB level for this connector.

MLB Daughtercards are available direct from SMSC

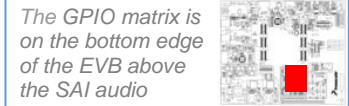
As with all daughtercards, the EVB must be powered OFF to prevent damage to the EVB or daughter card components.

⁷ ID0 and ID1 have a 10K pullup to 3V3

8. User Interface (I/O)

This section details the user I/O available on the EVB and includes the GPIO matrix, switches, LED's and the ADC variable resistor.

8.1. GPIO Matrix



All of the available GPIO pins (those not already used for existing EVB peripherals) are available at the GPIO matrix shown below. The matrix provides an easy to follow, intuitive, space saving grid of 0.1" header through-hole pads. Users can solder wires, fit headers or simply insert a scope probe into the respective pad.

To use the matrix, simply read the port letter from the top or bottom row of text then the pad number from the columns on the left or right of the matrix. For example, the 1st pad available on Port B is PB5 as highlighted in green below.

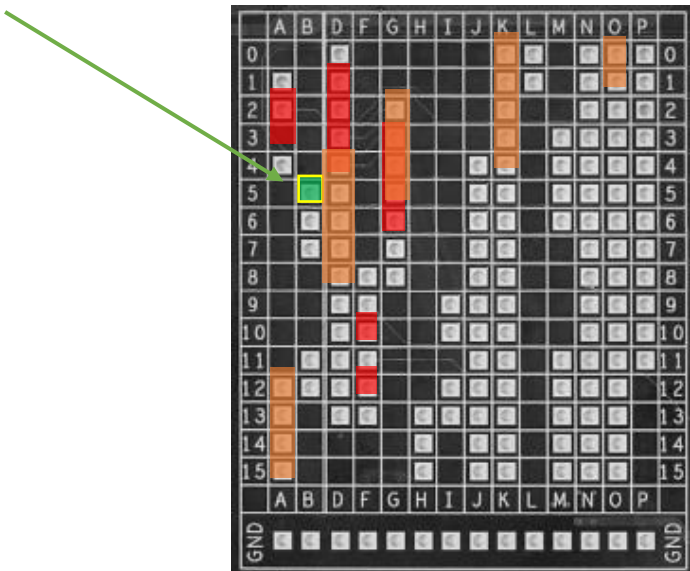


Figure 12. GPIO Matrix

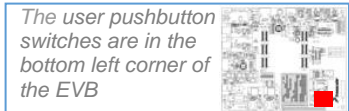
If a pad is populated in the matrix, it means this is available for exclusive use as GPIO. The exception to this are the port pins detailed below which are also shared with switches or user LED's (shaded red in the matrix diagram above).

- PG2, PG3, PG4, PG5 – User LED's 1..4
- PD0, PD1, PD2, PD3 – HEX Encoder Switch
- PA1, PA2, PF9, PF11 – User pushbutton Switches

In addition there are GPIO pins that are shared with the SAI Audio and TWRPI connectors as detailed below and shaded orange. These are totally available unless the SAI / TWRPI headers are being used.

PA[12..15], PD[4..8], PG[2..5], PK[0..4], PO[0..1]

8.2. User Switches (SW3, SW4, SW6, SW7, P22)



There are 4 active high (pulled low, driven to 3.3V) pushbutton switches (SW3, SW4, SW6, SW7) connected to a 4 way header (P22) in a box titled “User Switches”. The switches are also directly connected to MCU ports so no additional wiring is required unless you require to route these to a different GPIO port.

The switches are connected as follows:

Table 20. User Pushbutton Switches (SW3, SW4, SW6, SW7)

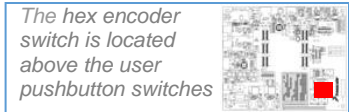
Switch	Number	MCU Pin	P18 Connection Pin
SW3	1	PA1	Pin1 (UpperMost)
SW4	2	PA2	Pin2
SW6	3	PF9	Pin3
SW7	4	PF11	Pin4

NOTE

The MCU ports used on the user pushbutton switches are also routed to the GPIO matrix.

There are zero ohm resistors on the direct connections between each switch and the MCU pins. These can be removed if required to isolate the switch from the respective MCU pin (useful if the switch is being manually routed to another pin on the GPIO matrix).

8.3. Hex Encoder Switch (SW2, J26, P20)



The hex encoder switch is located above the user pushbutton switches

There is a single hex encoded 16 position rotary switch on the EVB. This outputs a binary encoded hex value (active high) on 4 MCU ports (Port D[0..3]) as well as a 4 pin header P20. There is a jumper J26 which can be used to isolate the supply to the hex encoder if required. This prevents any voltage being asserted on the MCU pins irrespective of the position of the switch

Table 21. Hex Encoder Switch (SW2)

Position	HEX_SW4 (PD3, P20-4)	HEX_SW3 (PD2, P20-3)	HEX_SW2 (PD1, P20-2)	HEX_SW1 (PD0, P20-1)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

Table 22. Hex Encoder Switch Power Jumper (J26)

Jumper	Position	PCB Legend	Description
J26 (3V3)	FITTED (D) Removed		The hex encoder switch is powered with 3.3V (functional) The hex encoder switch is not powered and will not drive outputs

NOTE

The MCU ports used on the user pushbutton switches are also routed to the GPIO matrix.

There are zero ohm resistors on the direct connections between the switch output and the MCU pins. These can be removed if required to isolate the switch from the respective MCU pin (useful if the switch is being manually routed to another pin on the GPIO matrix).

8.4. User LED's (DS2, DS3, DS7, DS8, P19)

The user LED's are above the user switches in the lower right quarter



There are four active low user LED's connected directly to 4 MCU ports (PG[2..5]) as well as to a 4 pin header.

Table 23. User LEDs (DS2, DS3, DS7, DS8, P19)

Switch	Number	MCU Pin	P19 Connection Pin
DS2	1	PG2	Pin1 (Upper Pin)
DS3	2	PG3	Pin2
DS7	3	PG4	Pin3
DS8	4	PG5	Pin4

NOTE

The MCU ports used on the LEDs are also routed to the GPIO matrix.

There are zero ohm resistors on the direct connections between each LED and the MCU pins. These can be removed if required to isolate the LED from the respective MCU pin (useful if the LED is being manually routed to another pin on the GPIO matrix).

8.5. ADC Input Potentiometer (J17, RV1)

The ADC Pot is to the right of the user LED's in the lower right corner



There is a small variable resistor RV1 on the EVB which routes a voltage between 0v and 3.3V to MCU pin PB4. This is useful for quick ADC testing. Jumper J17 which is fitted by default can be removed to disconnect MCU PB4 from RV1 if desired.

Table 24. ADC Input Potentiometer Enable (J19)

Jumper	Position	PCB Legend	Description
J17	FITTED (D) Removed		Output from RV1 is routed to MCU PB4 pin MCU PB4 is not connected to RV1

There is also a test point TP18 connected to the variable resistor output for monitoring purposes.

9. MCU Port Pin EVB Functions

The table below shows what each MCU pin is used for on the EVB. Note that not all MCU pins will be available depending on the device package being used.

Table 25. Port Pin Functions

No	PortA	PortB	PortC	PortD	PortE	PortF	PortG	PortH
0	SD Card	CAN0	JTAG	GPIO ³	MLB	SAI Audio	Ethernet	Ethernet
1	GPIO ²	CAN0	JTAG	GPIO ³	MLB	SAI Audio	Ethernet	Ethernet
2	GPIO ²	LIN0	USB1	GPIO ³	FlexA	SAI Audio	GPIO ^{4,5}	Ethernet
3	Ethernet	LIN0	USB1	GPIO ³	FlexA	SAI Audio	GPIO ^{4,5}	SAI Audio
4	GPIO	ADC Pot	FlexB	GPIO ⁵	FlexB	SAI Audio	GPIO ^{4,5}	SAI Audio
5	SAI Audio	GPIO	FlexA	GPIO ⁵	FlexB	SAI Audio	GPIO ^{4,5}	SAI Audio
6	MLB	GPIO	LIN1	GPIO ⁵	SD Card	SAI Audio	GPIO	MLB
7	Ethernet	GPIO	LIN1	GPIO ⁵	SD Card	SAI Audio	GPIO	MLB
8	Ethernet	EXTAL32	RS232	GPIO ⁵	SAI Audio	GPIO	GPIO	SD Card
9	Ethernet	XTAL32	RS232	GPIO	SAI Audio	GPIO ²	MLB	JTAG
10	Ethernet	SAI Audio	CAN1	GPIO	SAI Audio	GPIO	USB1	JTAG
11	Ethernet	GPIO	CAN1	GPIO	SAI Audio	GPIO ²	USB1	USB1
12	GPIO ⁵	GPIO	Flex	GPIO	Ethernet	GPIO	Ethernet	USB1
13	GPIO ⁵	MLB	Flex	GPIO ¹	Ethernet	GPIO	Ethernet	GPIO
14	GPIO ⁵	MLB	Flex	MLB	USB1	Ethernet	USB1	GPIO
15	GPIO ⁵	MLB	Flex	MLB	USB1	Ethernet	USB1	GPIO

No	PortI	PortJ	PortK	PortL	PortM	PortN	PortO	PortP	PortQ
0	SD Card	SAI Audio	GPIO ⁵	GPIO	NEXUS	GPIO	GPIO ⁵	GPIO	USB0
1	SD Card	SAI Audio	GPIO ⁵	GPIO	NEXUS	GPIO	GPIO ⁵	GPIO	USB0
2	SD Card	SAI Audio	GPIO ⁵	NEXUS	NEXUS	GPIO	GPIO	GPIO	USB0
3	SD Card	SD Card	GPIO ⁵	NEXUS	GPIO	GPIO	GPIO	GPIO	USB0
4	USB1	GPIO	GPIO ⁵	NEXUS	GPIO	GPIO	GPIO	GPIO	USB0
5	USB1	GPIO	GPIO	NEXUS	GPIO	GPIO	GPIO	GPIO	USB0
6	USB0	GPIO	GPIO	NEXUS	GPIO	GPIO	GPIO	GPIO	USB0
7	USB1	GPIO	GPIO	NEXUS	NEXUS	GPIO	GPIO	GPIO	USB0
8	MLB	GPIO	GPIO	JTAG	NEXUS	GPIO	GPIO	GPIO	-
9	GPIO	GPIO	GPIO	NEXUS	NEXUS	GPIO	GPIO	GPIO	-
10	GPIO	GPIO	GPIO	NEXUS	NEXUS	GPIO	GPIO	GPIO	-
11	Ethernet	GPIO	GPIO	NEXUS	GPIO	GPIO	GPIO	GPIO	-
12	GPIO ¹	GPIO	GPIO	NEXUS	GPIO	GPIO	GPIO	USB0	-
13	GPIO ¹	GPIO	GPIO	NEXUS	GPIO	GPIO	GPIO	USB0	-
14	SAI Audio	GPIO	GPIO	NEXUS	GPIO	GPIO	GPIO	USB0	-
15	SAI Audio	GPIO	GPIO	NEXUS	GPIO	GPIO	GPIO	USB0	-

¹ Shared with MLB header (via no populated zero ohm resistors)

² Shared with user switches

³ Shared with Hex Encoder Switch

⁴ Shared with user LED's

⁵ Shared with TWRPI (P26, P27) or SAI Audio P25

10. Default Jumper Summary Table

The following tables detail the default (D) jumper configuration of the EVB and daughtercards

Table 26. Default Jumper Positions (Main Board)

Jumper	Default Posn	PCB Legend	Description
J1 Posn 1-2	Fitted (D)	BGE	FlexRay B PHY Bus Guardian Enable (Transmitter is enabled)
J1 Posn 3-4	Fitted (D)	EN	FlexRay B PHY is enabled
J1 Posn 5-6	Fitted (D)	STBN	FlexRay B PHY will not enter Standby Mode
J1 Posn 7-8	Fitted (D)	WAKE	FlexRay B PHY Wakeup signal pulled low
J2 Posn 1-2	Fitted (D)	BGE	FlexRay A PHY Bus Guardian Enable (Transmitter is enabled)
J2 Posn 3-4	Fitted (D)	EN	FlexRay A PHY is enabled
J2 Posn 5-6	Fitted (D)	STBN	FlexRay A PHY will not enter Standby Mode
J2 Posn 7-8	Fitted (D)	WAKE	FlexRay A PHY Wakeup signal pulled low
J3 Posn 1-2	Fitted (D)	TX	MCU PC5 is connected to FlexRay A transceiver TX
J3 Posn 3-4	Fitted (D)	TXEN	MCU PE2 is connected to FlexRay A transceiver TXEN
J3 Posn 5-6	Fitted (D)	RX	MCU PE3 is connected to FlexRay A transceiver RX
J4 Posn 1-2	Fitted (D)	TX	MCU PE4 is connected to FlexRay B transceiver TX
J4 Posn 3-4	Fitted (D)	TXEN	MCU PC4 is connected to FlexRay B transceiver TXEN
J4 Posn 5-6	Fitted (D)	RX	MCU PE5 is connected to FlexRay B transceiver RX
J5	1-2 (D)	MII	Ethernet PHY is configured in MII mode
J6 (X1)	1-2 (D)		Ethernet PHY X2 clock is connected to 25MHz xtal
J7 (X2)	1-2 (D)		Ethernet PHY X1 clock is connected to 25MHz xtal
J8 (RST)	1-2 (D)	NORM	The Ethernet PHY will be reset along with MCU reset
J9 (EN)	Fitted (D)		Reset from reset switch and debug connectors is active
J10 (LIN0) 1-2	Fitted (D)	RX	MCU LIN0_RX signal (PB3) is routed to LIN0 interface
J10 (LIN0) 3-4	Fitted (D)	TX	MCU LIN0_TX signal (PB2) is routed to LIN0 interface
J11 (Master_EN)	Fitted (D)		LIN0 is configured in Master Mode
J12 (LIN1) 1-2	Fitted (D)	RX	MCU LIN1_TX signal (PC7) is routed to LIN1 interface
J12 (LIN1) 3-4	Fitted (D)	TX	MCU LIN1_RX signal (PC6) is routed to LIN interface
J13 (Master_EN)	Fitted (D)		LIN1 is configured in Master Mode
J14 (CAN1) 1-2	Fitted (D)	TX	MCU CAN1_TX signal (PC10) is routed to CAN interface
J14 (CAN1) 3-4	Fitted (D)	RX	MCU CAN1_RX signal (PC11) is routed to CAN interface
J15 (CAN0) 1-2	Fitted (D)	TX	MCU CAN0_TX signal (PB0) is routed to CAN interface
J15 (CAN0) 3-4	Fitted (D)	RX	MCU CAN0_RX signal (PB1) is routed to CAN interface
J16 Posn 1-2	Fitted (D)	RX	MCU LIN2_RX signal (PC9) is routed to the FTDI interface
J16 Posn 3-4	Fitted (D)	TX	MCU LIN2_TX signal (PC8) is routed to the FTDI interface
J17	Fitted (D)		Output from RV1 is routed to MCU PB4 pin
J18 (1V25L)	Fitted (D)		1.25V Linear regulator output is routed to daughter card
J19 (5V0S)	Fitted (D)		5.0V Switching regulator output is routed to daughter card
J20 (3V3L)	Fitted (D)		3.3V Linear regulator output is routed to daughter card
J21 (5V0L)	Fitted (D)		5.0V Linear regulator output is routed to daughter card
J22 (3V3S)	Fitted (D)		3.3V Switching regulator output is routed to daughter card
J23 (INPUT SEL)	1-2 (D)	12V	1.25V Linear regulator is powered from main 12V
J24 (HVA)	1-2 (D)	3V3	EVB peripherals in HVA domain are set to use I/O voltage of 3.3V
J25 (HVB)	1-2 (D)	3V3	EVB peripherals in HVB domain are set to use I/O voltage of 3.3V
J26 (3V3)	Fitted (D)		The hex encoder switch is powered with 3.3V (functional)

Table 27. Default Jumper Positions (Daughterboards)

Jumper	Default Posn	PCB Legend	Description
J1 (XTAL)	1-2 (D)	Y1	MCU XTAL signal is routed to crystal Y1
J2 (EXTAL)	1-2 (D)	Y1	MCU EXTAL signal is routed to crystal Y1
J3 (ADC0)	1-2 (D)	3V3	MCU ADC0 pin is connected to 3.3V (Linear)
J4 (ADC1)	1-2 (D)	3V3	MCU ADC1 pin is connected to 3.3V (Linear)
J5 (HVA)	1-2 (D)	3V3	MCU VDD_HV_A domain is connected to 3.3V (Switching Regulator)
J6 (HVB)	1-2 (D)	3V3	MCU VDD_HV_B domain is connected to 3.3V (Switching Regulator)
J7 (HVC)	1-2 (D)	3V3	MCU VDD_HV_C domain is connected to 3.3V (Switching Regulator)
J8 (FLA)	Fitted (D)		MCU VDD_HV_FLA pin is connected to 3.3v (Switching Regulator)
J9 (REG)	1-2 (D)	3V3	MCU ballast transistor collector is connected to 3.3V (Switching)
J10 (VDDL)	1-2 (D)	REG	MCU VDD_LV domain is powered from ballast transistor
J11 (DAC)	1-2 (D)	HVA	MCU VIN1_CMP_REF is powered from VDD_HV_A
J12	Fitted (D)		Ballast collector supply is enabled (jumper can be used for current measure)
J13	1-2 (D)		** Only valid on certain devices – External Ballast enabled.

Note that not all jumpers will be present on all of the daughterboards.

11. Default Jumper Diagram

The diagram below shows the location and configuration of the default jumpers of the main board and provides an easy to use cross reference. By default all of the jumpers are fitted to the daughtercard (3 way jumpers in position 1-2).

NOTE

Following figure is of an older board revision however there were no additional jumpers and no jumpers have moved position.

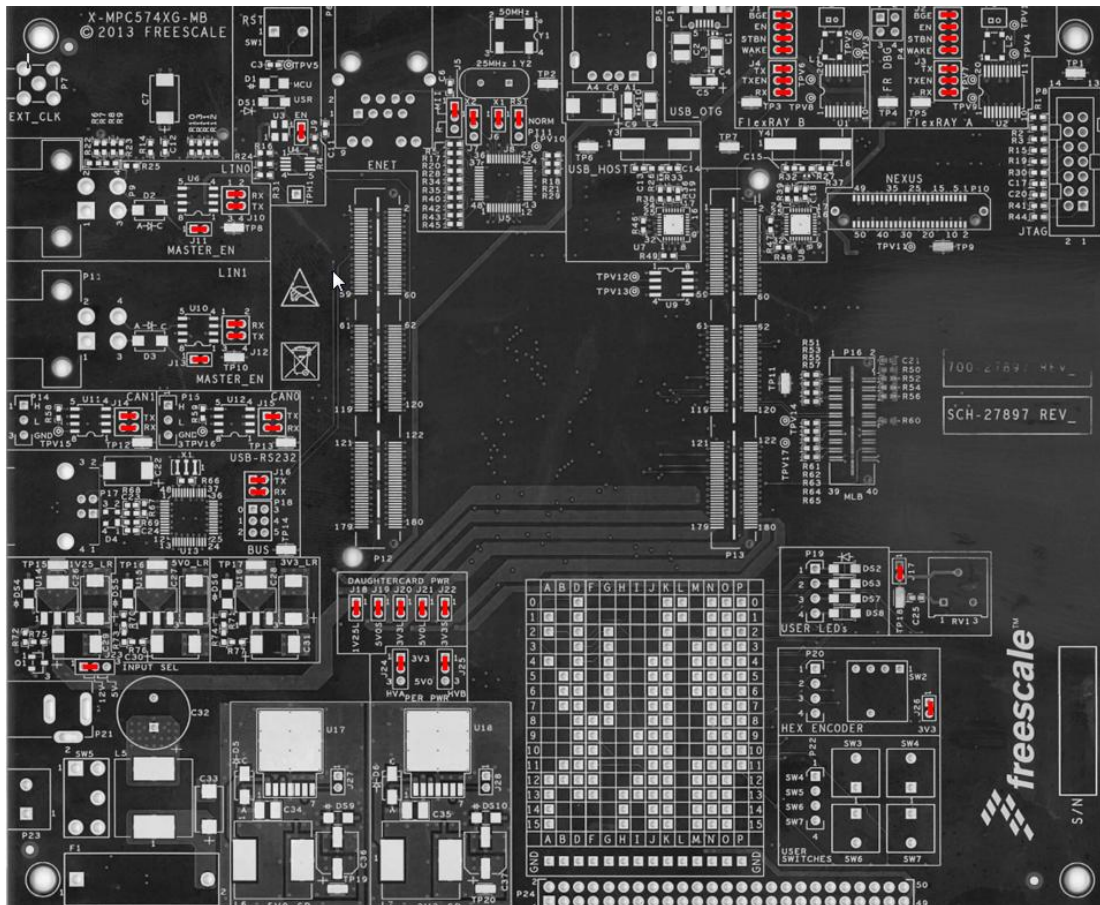


Figure 13. Default Jumper Position

12. Revision History

Date	Substantial changes
August 2015	Initial release

13. Appendix

The following EVB schematics are detailed in the following sections:

- Main EVB (motherboards)
- 324BGA Daughtercard
- 256BGA Daughtercard
- 176QFP Daughtercard
- 100QFP Daughtercard (MPC5746C only)



Main EVB



MPC574xx Customer Evaluation Board (X-MPC574xx)

Table Of Contents:

Power - Main input and Linear voltage regulators	Sheet 2
Power - Switching voltage regulators	Sheet 3
Daughter Card Connectors (Sockets)	Sheet 4
Reset and External Clock Input	Sheet 5
JTAG and Nexus Connectors	Sheet 6
Comms - CAN and LIN	Sheet 7
Comms - RS232 (USB FTDI interface)	Sheet 8
Comms - USB Interfaces	Sheet 9
Comms - Ethernet	Sheet 10
Comms - FlexRAY	Sheet 11
Audio - SAI Audio. AVB and TWRPI headers	Sheet 12
AV - MOST Interface	Sheet 13
Memory - SD Card Slot	Sheet 14
User - Switches, LED's and Potentiometer	Sheet 15
User - GPIO Pin Matrix	Sheet 16

Caution:

These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale MPC574xG family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in *ITALICS*

Revision Information

Rev	Date	Designer	Comment
0.1	01 Feb 2012	Alasdair Robertson	Start of cap
X1	19 Feb 2012	Alasdair Robertson	1st release
X2	28 Feb 2012	Alasdair Robertson	2nd release
X3	11 Mar 2013	Alasdair Robertson	Final review
X4	13 Mar 2013	Alasdair Robertson	Version sen
X5	14 Mar 2013	Alasdair Robertson	Component
X6	29 Mar 2013	Alasdair Robertson	Changes ma
X7	02 Apr 2013	Alasdair Robertson	LAY RefD
A	17 Apr 2013	Alasdair Robertson	Post Layout
AX1	24 Jun 2013	Alasdair Robertson	Fixes and c
AX2	10 July 2013	Alasdair Robertson	Added CAN
AX3	12 July 2013	Alasdair Robertson	Corrected g
B	12 July 2013	Alasdair Robertson	Production
BX1	20 Aug 2013	Alasdair Robertson	Change to E
C	20 Aug 2013	Alasdair Robertson	Production
CX1	18 Dec 2013	Alasdair Robertson	CAN trans
CX2	05 May 2014	Alasdair Robertson	Added com
CX3	25 June 2014	Alasdair Robertson	PH3..5 now
CX4	26 June 2014	Alasdair Robertson	Minor chan
CX5	26 June 2014	Alasdair Robertson	Part Manag
CX6	18 Aug 2014	Alasdair Robertson	Added addi
CX7	03 Sept 2014	Alasdair Robertson	Added addi
D	24 Sept 2014	Alasdair Robertson	Released to
D1	14 Aug 2015	Alasdair Robertson	Tidy up Sch

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hole Pad Large (for standard 0.1" header).
Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop



This document is for procurement or

Designer:
A. Robertson

Drawn by:
A. Robertson

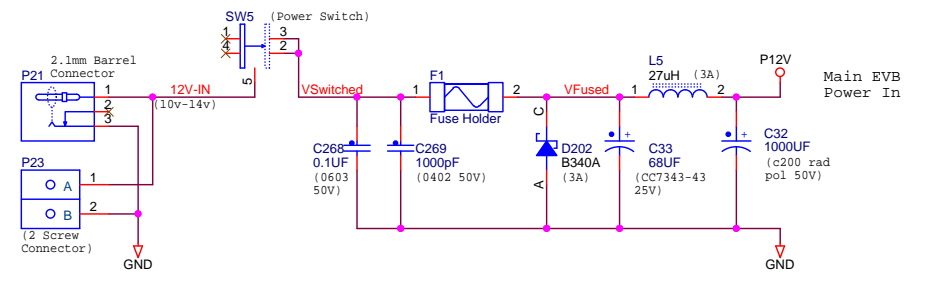
Approved:
A. Robertson



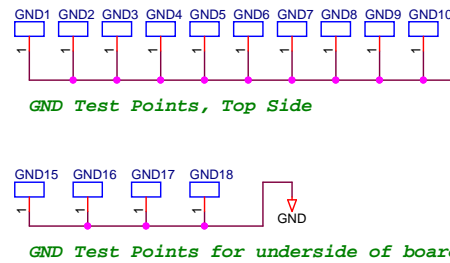
Input and Linear Voltage Regulators

at 12V DC nominal (range 10v - 14v)
 See note on schematic sheet 3 regarding 3.3V regulator when running at < 11V)

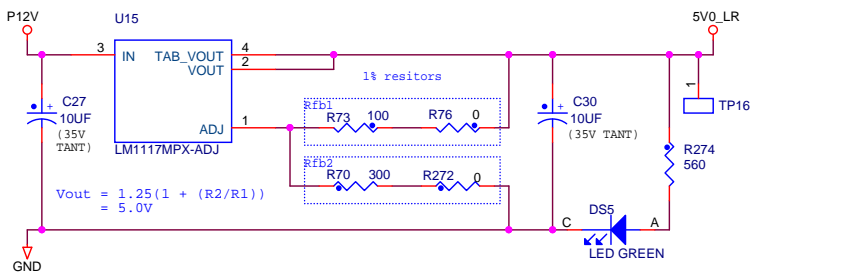
Power Supply Input and Filter



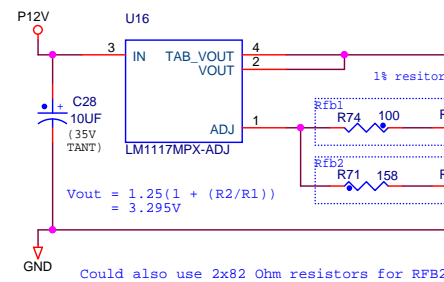
Test and reference points



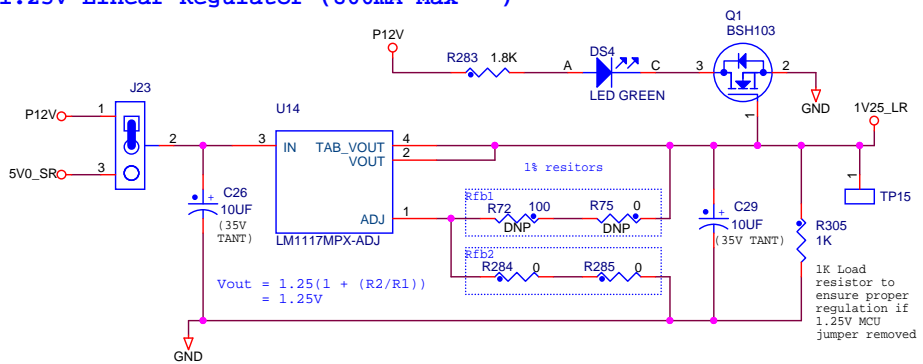
5.0V Linear Regulator (800mA Max **)



3.3V Linear Regulator (800mA Max **)



1.25V Linear Regulator (800mA Max **)



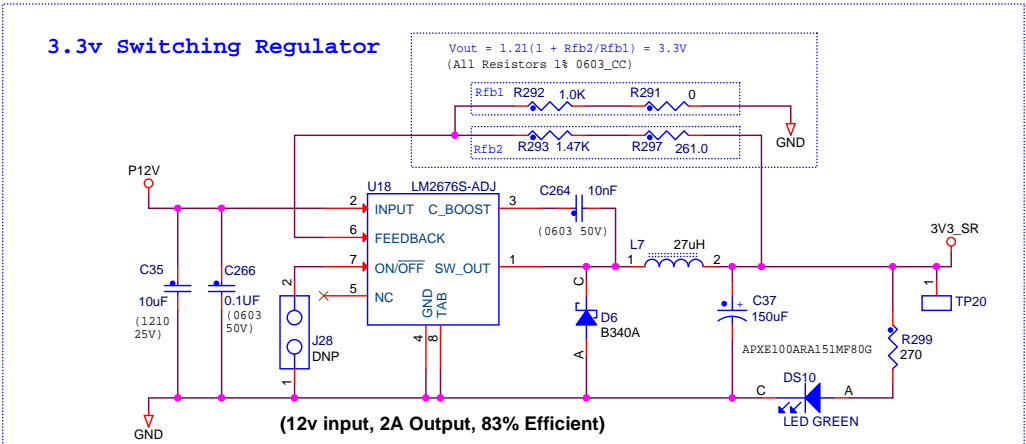
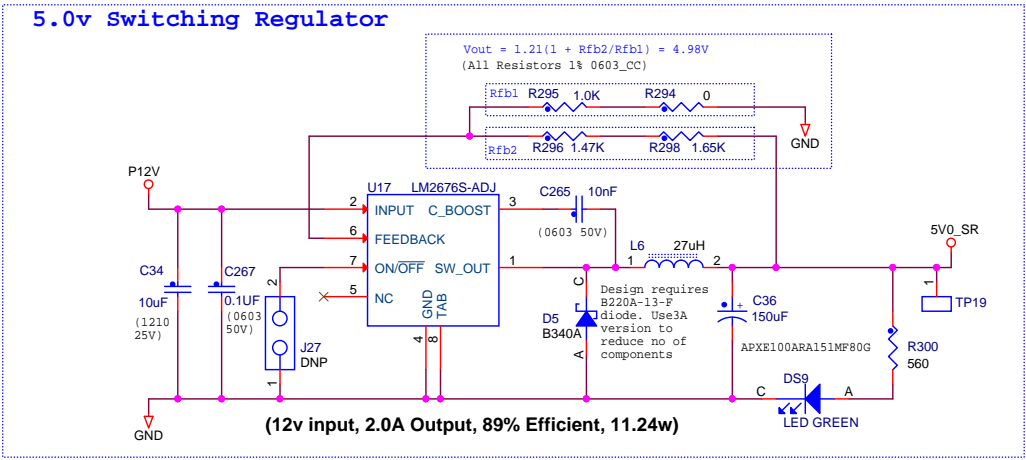
** Notes on Linear Regulator LM1117

The LM1117 linear regulators provide a maximum current of 800mA in ideal conditions. The current requirement for each regulator is in the range of mA (significantly under the maximum rating). These regulators will run cool on the EVB.

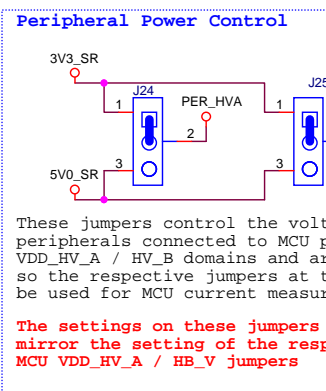
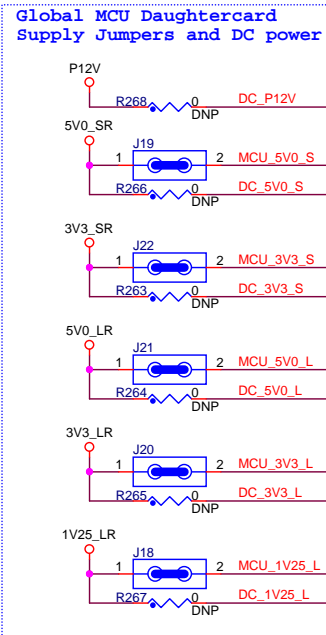
1.25V for External core supply. Simpler to use linear rather than switcher so can safely power from 5V switcher (slight ripple not an issue) for reduced heat dissipation



5V Voltage Regulators and Supply Jumpers



Caution The 3.3v regulator design is optimised for an input voltage of 12V. If the input voltage drops below approx 11V, the 3.3v output voltage ripple may increase. This can be reduced by increasing the bulk storage capacitor if required.



Using Adjustable version of LM2676 rather than fixed 3.3V / 5V regulators to reduce number of components in BOM.

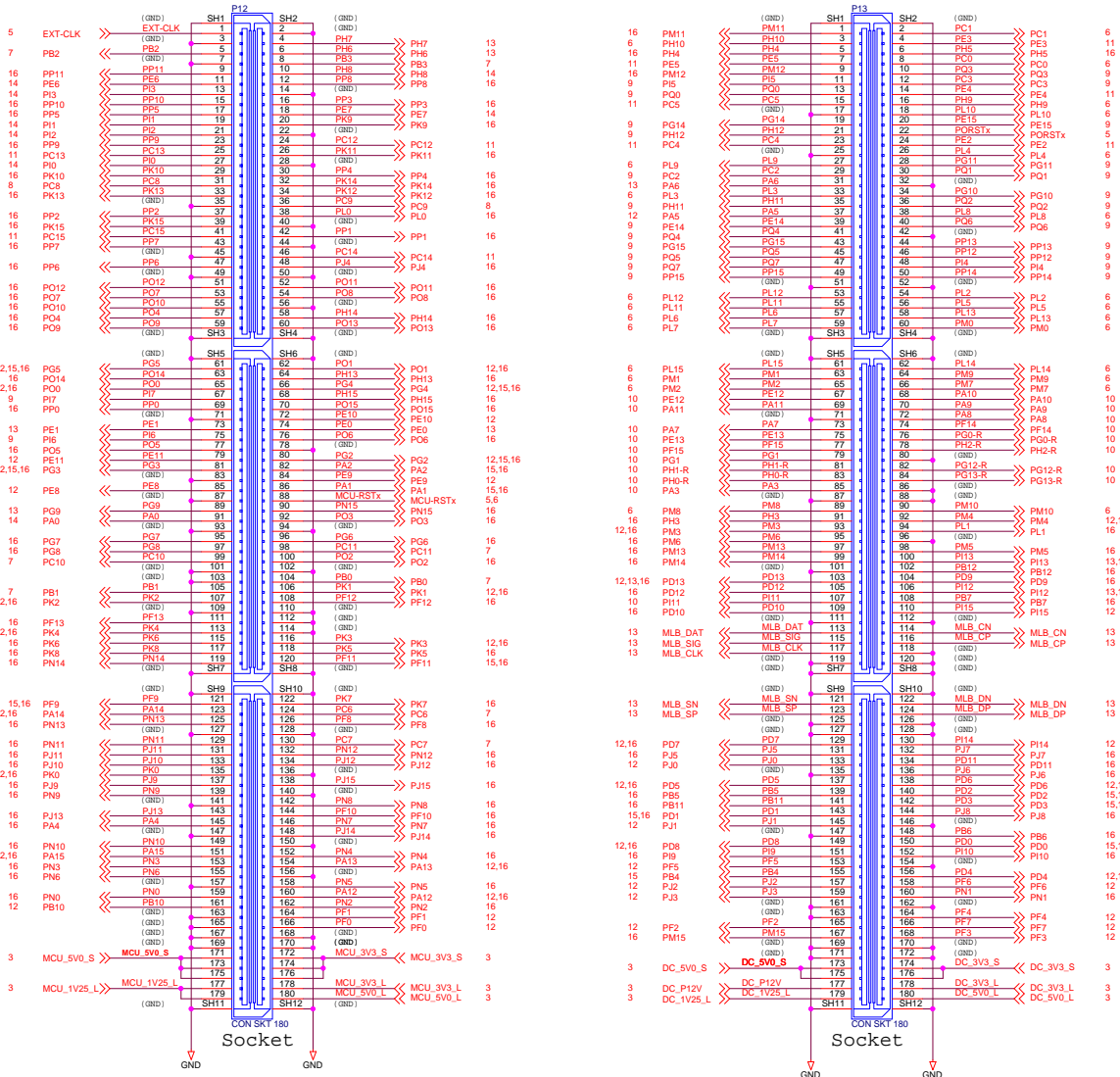
Where possible, components have been shared across the regulator designs to further reduce component count.



Board Connectors (Sockets)

way to fit these connectors onto a B sized sheet so unfortunately the sheet size has been .ll need to be printed on larger paper.

- The MCU Clock circuitry (apart from external clock) is local to the daughtercard so not pinned out on the connectors
- Power is supplied to the daughtercard via MCU specific jumpered supplies (left connector) or direct supplies from the regulators (right connector)



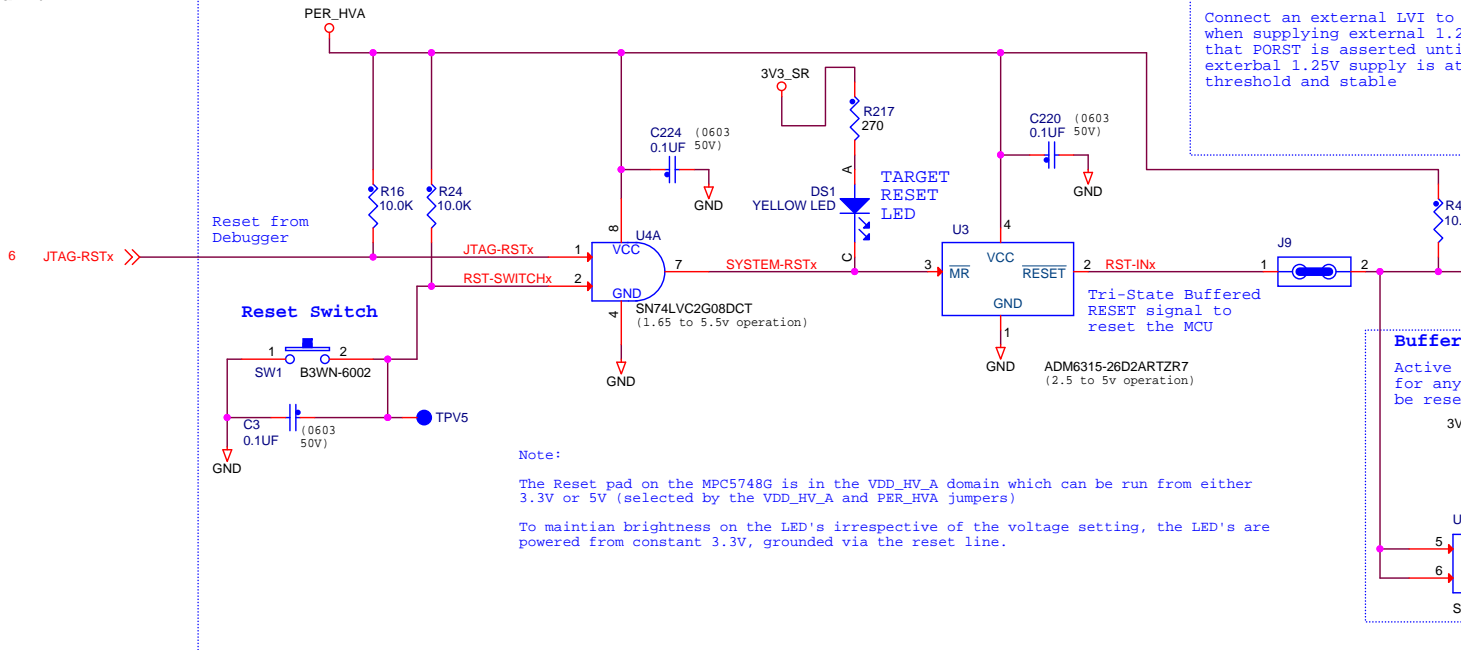
Not routed through the connectors:
 - Crystal signals
 - Specific MCU power pins (Power supplies are however taken to daughtercard)



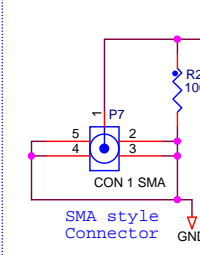
Reset External Clock In

VDD_HVA domain.

Reset Input / Output

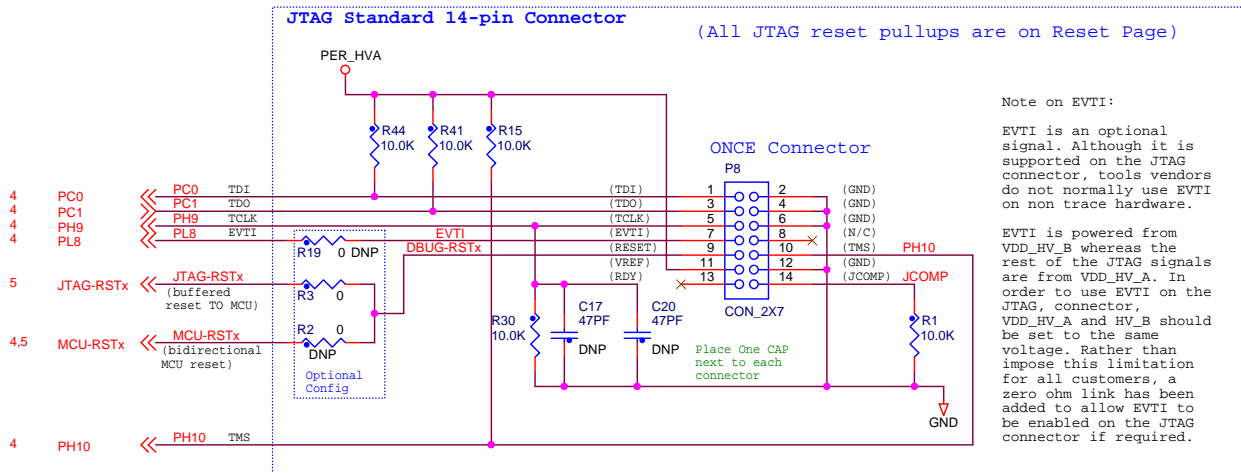


External Clock





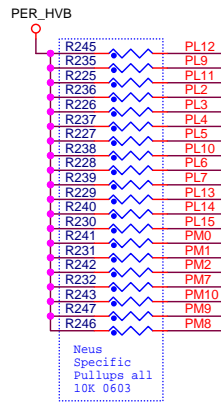
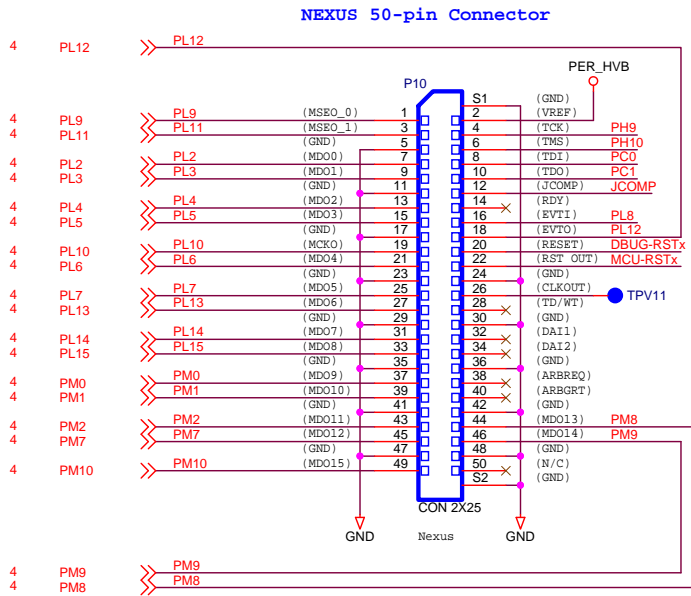
Connectors (JTAG and NEXUS)



Voltage Domain

All of the sig...
 exception of E...
 the VDD_HV_A d...
 signals used f...
 VDD_HV_B.

If you are usi...
 the VDD_HV_A a...
 same voltage a...
 peripheral sup...
 VDD_HV_A / B...
 configuration

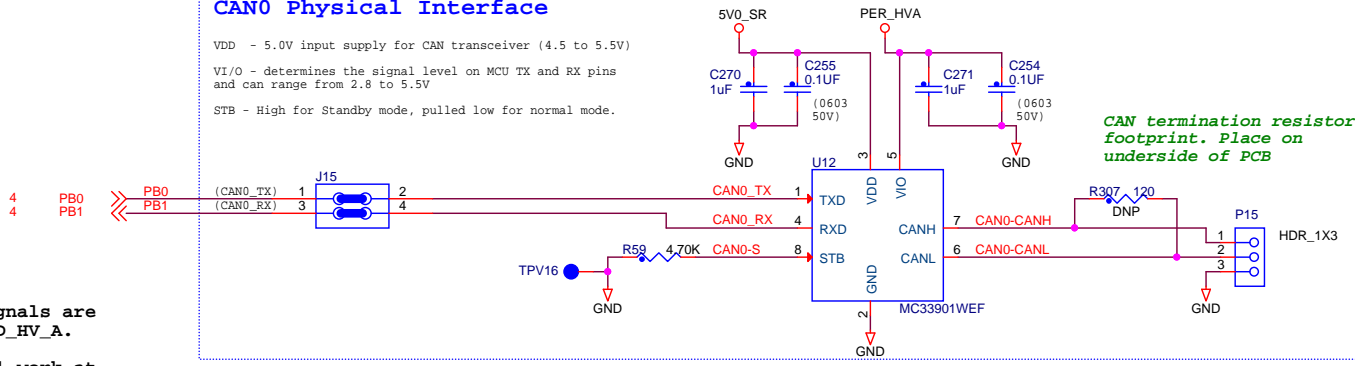




CAN Physical

CAN0 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)
 VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V
 STB - High for Standby mode, pulled low for normal mode.



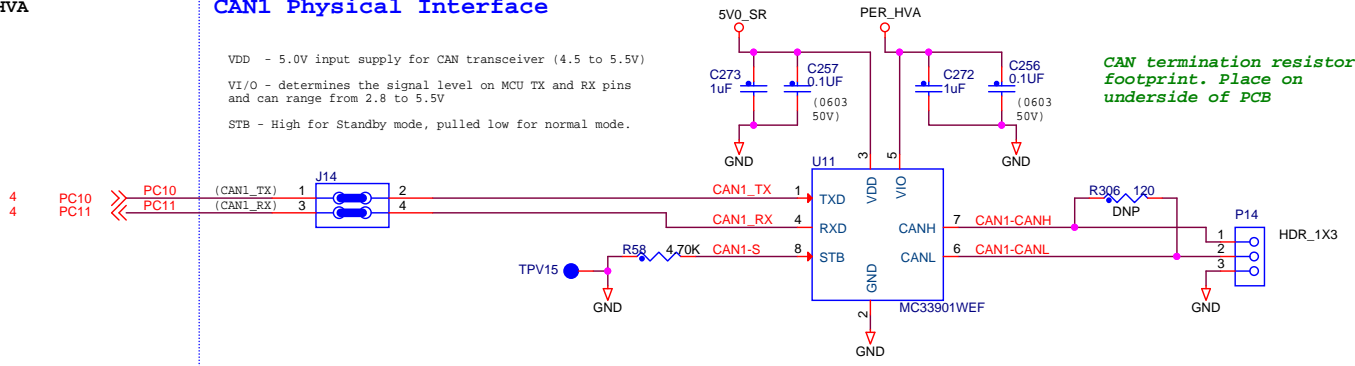
CAN termination resistor footprint. Place on underside of PCB

All CAN and LIN signals are in power domain VDD_HV_A.

All interfaces will work at 3.3V or 5.0V (PER_HVA jumper)

CAN1 Physical Interface

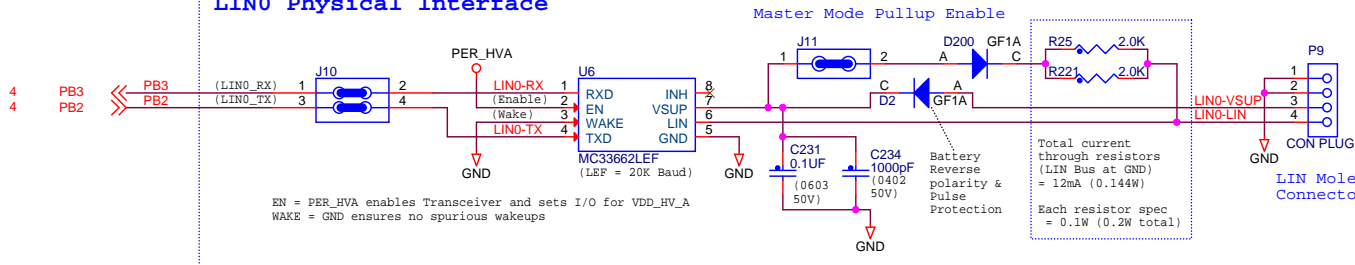
VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)
 VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V
 STB - High for Standby mode, pulled low for normal mode.



CAN termination resistor footprint. Place on underside of PCB

LINO Physical Interface

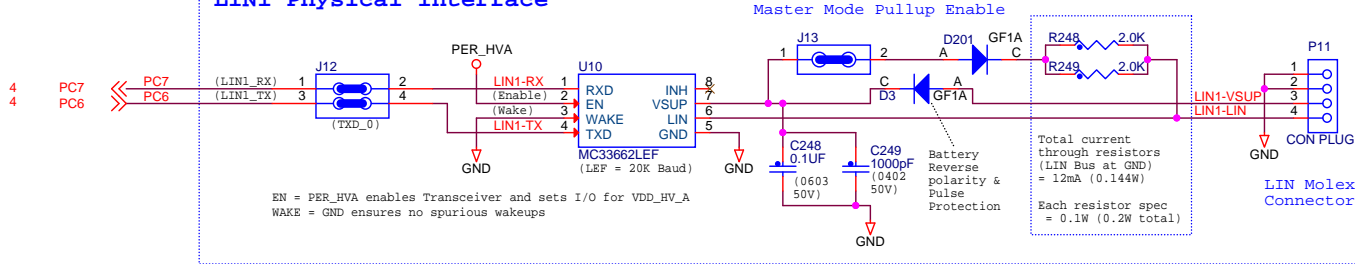
EN = PER_HVA enables Transceiver and sets I/O for VDD_HV_A
 WAKE = GND ensures no spurious wakeups



Total current through resistors (LIN Bus at GND) = 12mA (0.144W)
 Each resistor spec = 0.1W (0.2W total)

LIN1 Physical Interface

EN = PER_HVA enables Transceiver and sets I/O for VDD_HV_A
 WAKE = GND ensures no spurious wakeups



Total current through resistors (LIN Bus at GND) = 12mA (0.144W)
 Each resistor spec = 0.1W (0.2W total)



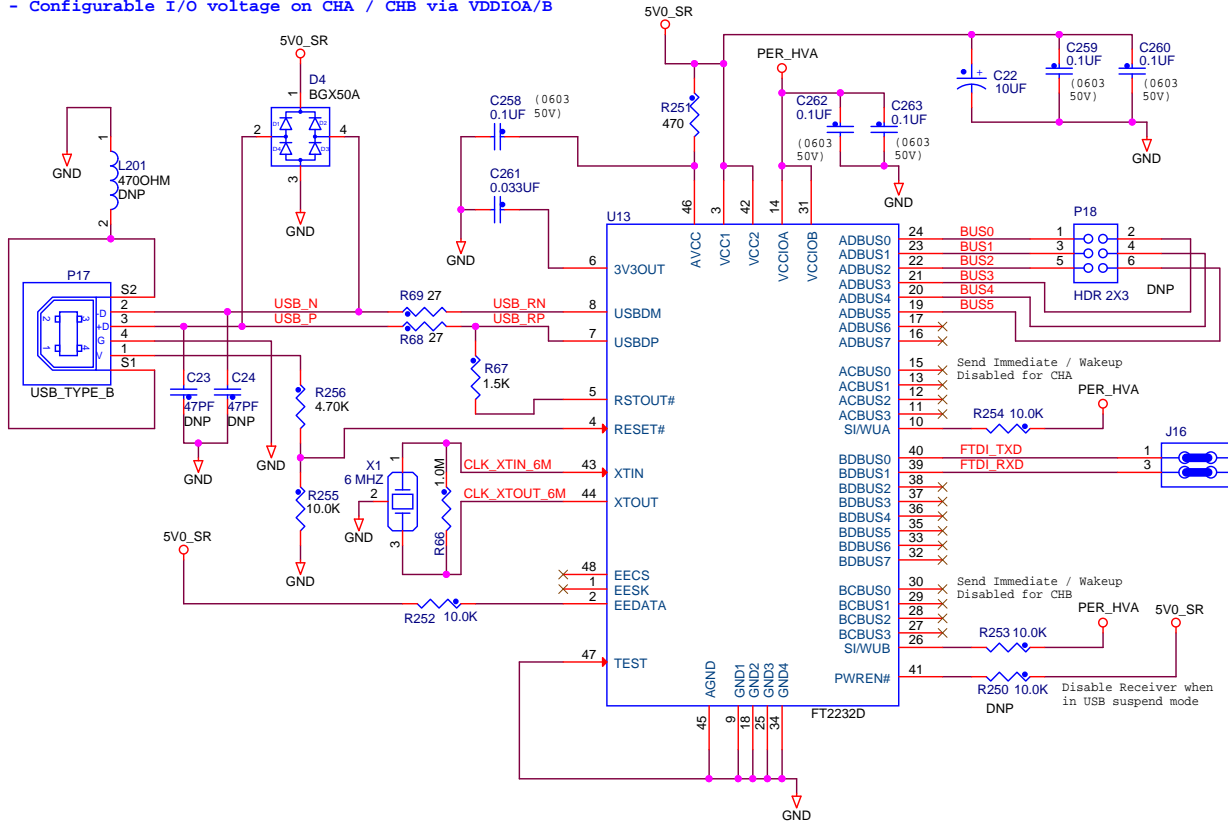
USB2 (serial) Interface

All Signals are in power domain VDD_HV_A.

FTDI interface will work at 3.3V or 5.0V (PER_HVA jumper)

FTDI USB <-> Serial Interface

- Self Powered mode. No power is taken from USB
- Device defaults to Dual serial (RS232) mode ie RS232 on both A and B
- Configurable I/O voltage on CHA / CHB via VDDIOA/B



P1
40
39
FT
15
FT
cc
FT
15
de
MC

J16
1
2
3
4

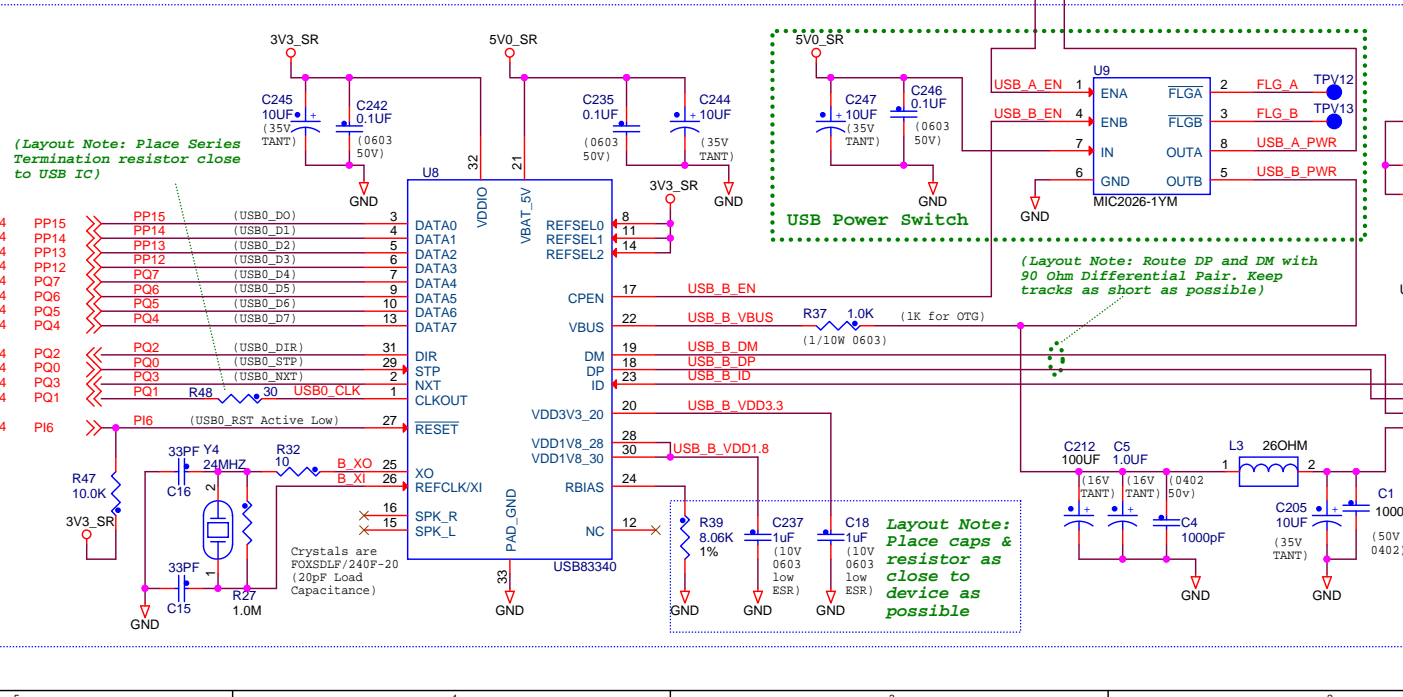
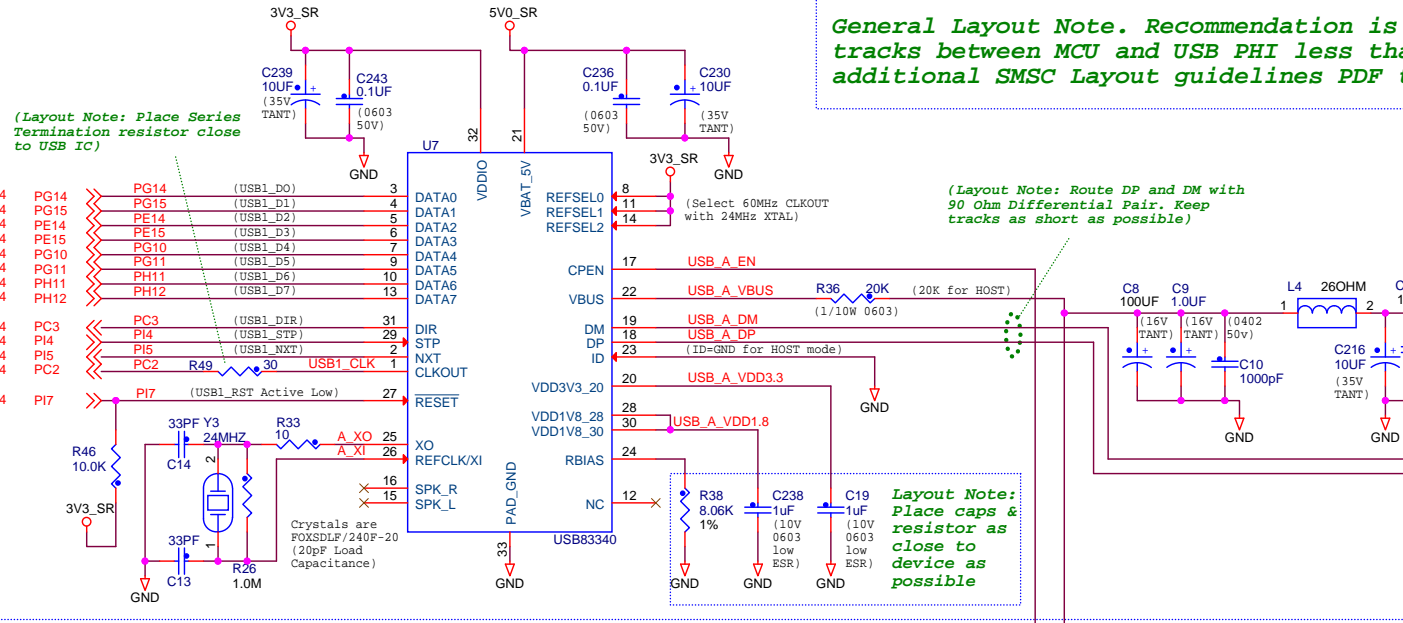
AGND
GND1
GND2
GND3
GND4



A Host and Type AB OTG

power domain VDD_HV_A

The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups.

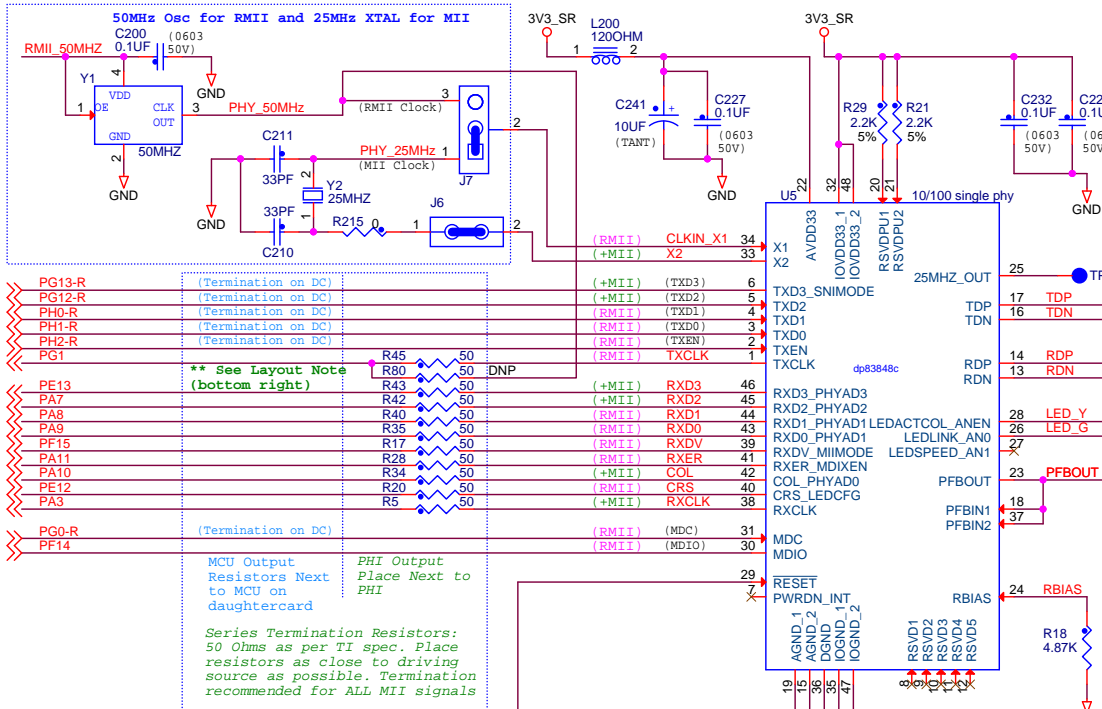




All Ethernet Signals are in power domain VDD_HV_B

The Ethernet interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, Ethernet MCU pads must be left as tri-state with no pullups.

- 4 PG13-R
- 4 PG12-R
- 4 PH0-R
- 4 PH1-R
- 4 PH2-R
- 4 PG1
- 4 PE13
- 4 PA7
- 4 PA8
- 4 PA9
- 4 PF15
- 4 PA11
- 4 PA10
- 4 PE12
- 4 PA3
- 4 PG0-R
- 4 PF14



50MHz Osc for RMII and 25MHz XTAL for MII

PHY 50MHz (RMII Clock)

PHY 25MHz (MII Clock)

Termination on DC

** See Layout Note (bottom right)

MCU Output Resistors Next to MCU on daughtercard

PHI Output Place Next to PHI

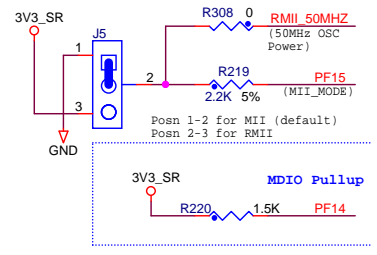
Series Termination Resistors: 50 Ohms as per TI spec. Place resistors as close to driving source as possible. Termination recommended for ALL MII signals

Boot Configuration (using PHY internal Pulls)

- Auto Negotiation Enable (All speeds / duplex supported) (AN_EN, AN0 and AN1 all Internal PullUP)
- Operating Mode (MII or RMII) (SNI_Mode Internal PullDown, MII_Mode control via jumper)
- LED Configuraiton (Model) (LED_CFG Internal PullUp)
- MDIX Enable (Auto MDIX Enabled) (MDIX_EN Internal PullUp)
- Physical Address (set to 0b00001) (PHYAD[0] Internal PullUp, PHYAD[1..4] Internal PullDown)

Layout Note:

MII Mode resistor (MII / RMII mode) and the MDIP ullup resistor should be placed as close as possible to the PF15 / PF14 tracks to reduce the effect of a stub on the transmission line.

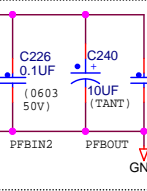


**** Layout Note - Place resistors as shown with shared pad on PG1 side of resistors**

For RMII mode, remove resistor between PG1 and TXCLK and place between PG1 and PHY_50MHz

Layout Note - Place resistors as shown with shared pad on PG1 side of resistors

Layout Note - Place resistors as shown with shared pad on PG1 side of resistors

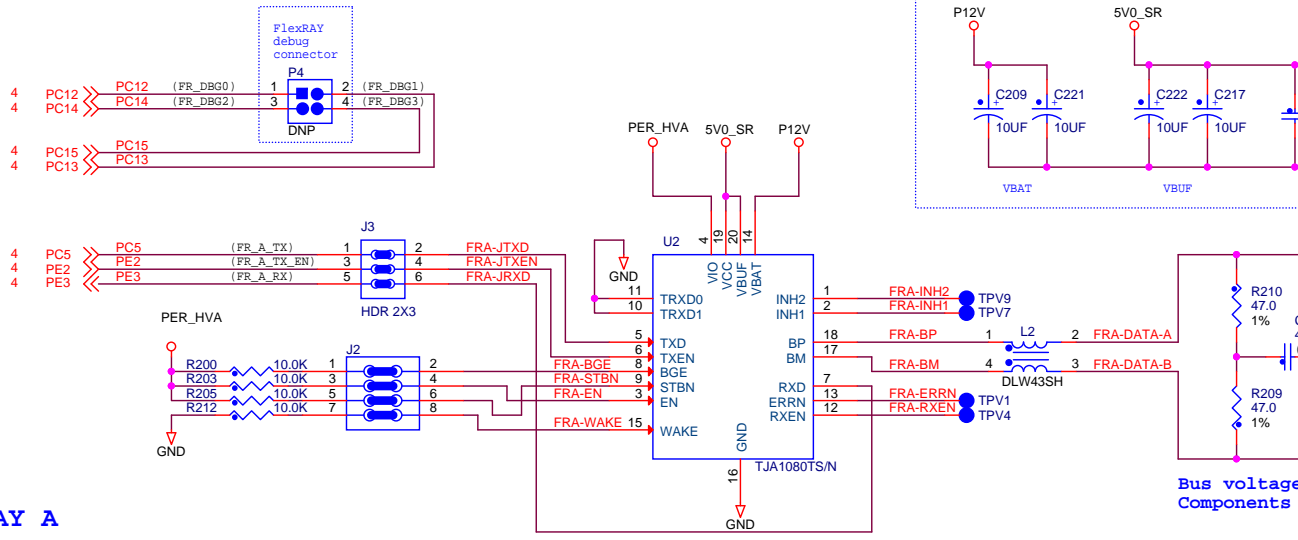




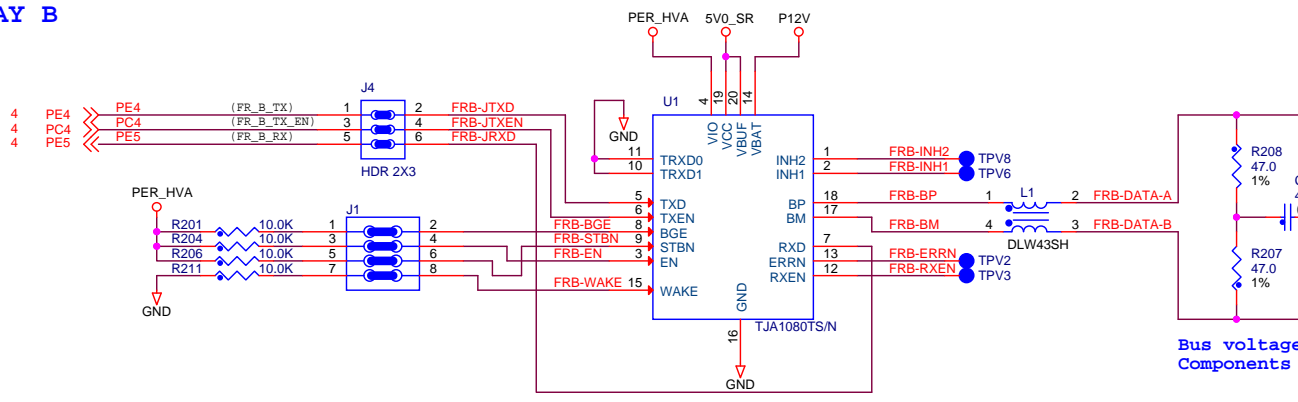
Physical Interface

All Signals are in power domain VDD_HV_A.
 FlexRAY interface will work at 3.3V or 5.0V (PER_HVA jumper)

Decoupling Caps for BOTH IC's. Pl



FlexRAY A



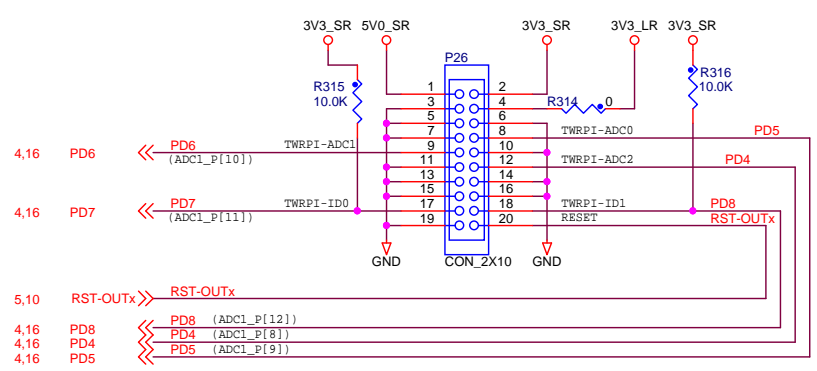
FlexRAY B

MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0

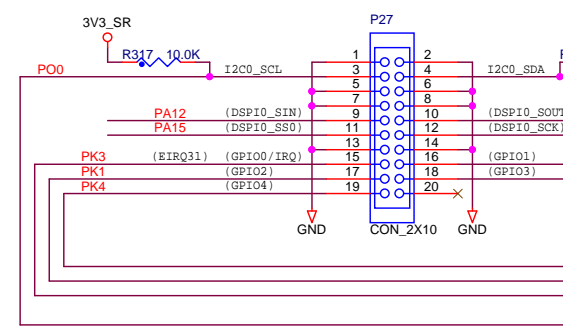


Lo, AVB & TWRPI Connectors

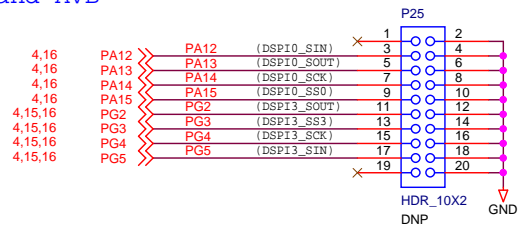
Purpose TWRPI



Note: Ports PD[4..8] are shared with the GPIO Matrix

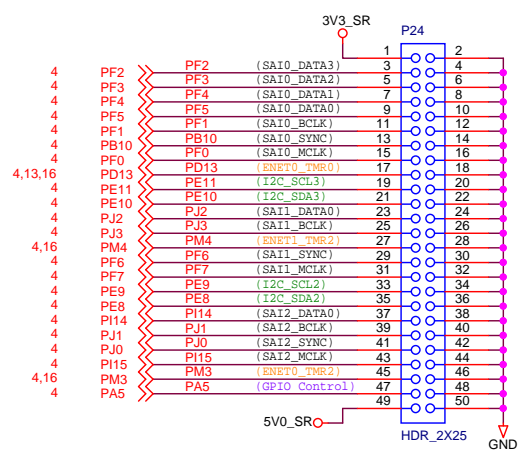


SAI Audio and AVB



Pins used on this header are also at GPIO Matrix

- PA12 - DSP10_SIN (Also shared with TWRPI)
- PA13 - DSP10_SOUT (Also shared with TWRPI)
- PA14 - DSP10_SCK (Also shared with TWRPI)
- PA15 - DSP10_SS0 (Also shared with TWRPI)
- PG2 - DSP13_SOUT (Also shared with User LED)
- PG3 - DSP13_SS3 (Also shared with User LED)
- PG4 - DSP13_SCK (Also shared with User LED)
- PG5 - DSP13_SIN (Also shared with User LED)



Differences to RevC
 Pin 17 was PH5, now PD13** (PH5 now routed to GPIO Matrix)
 Pin 27 was PH4, now PM4 (PH4 now routed to GPIO Matrix)
 Pin 45 was PH3, now PM3 (PH3 now routed to GPIO Matrix)

** Note PD13 is also routed to MLB header via DNP link

Black - SAI Channels
 Green - I2C Channels
 Orange - ENET TMRx channels



3C) Daughtercard Connector

MLB track lengths should be < 80mm
(from MCU through daughter card to connector)

All MLB Signals are in power domain VDD_HV_C.

The MLB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVC is set to 5V, MLB MCU pads must be left as tri-state with no pullups.

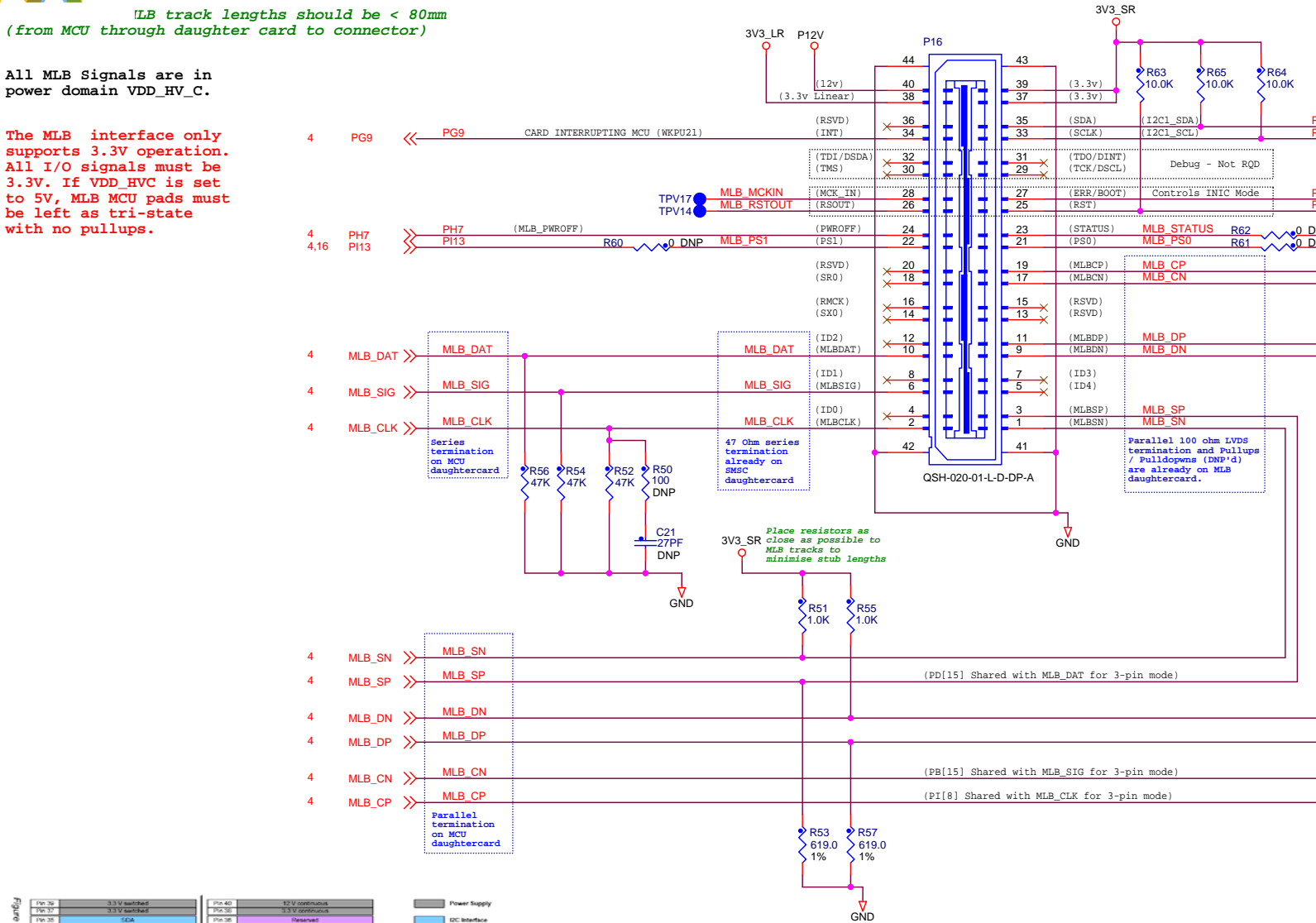


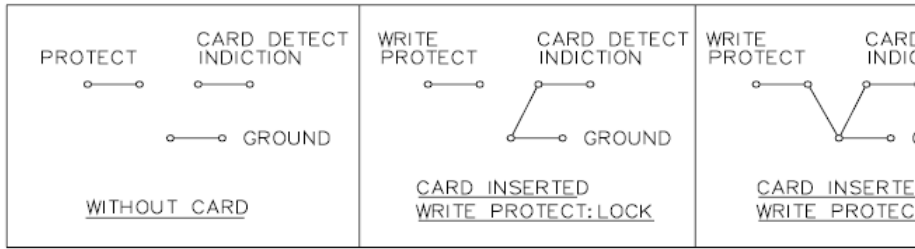
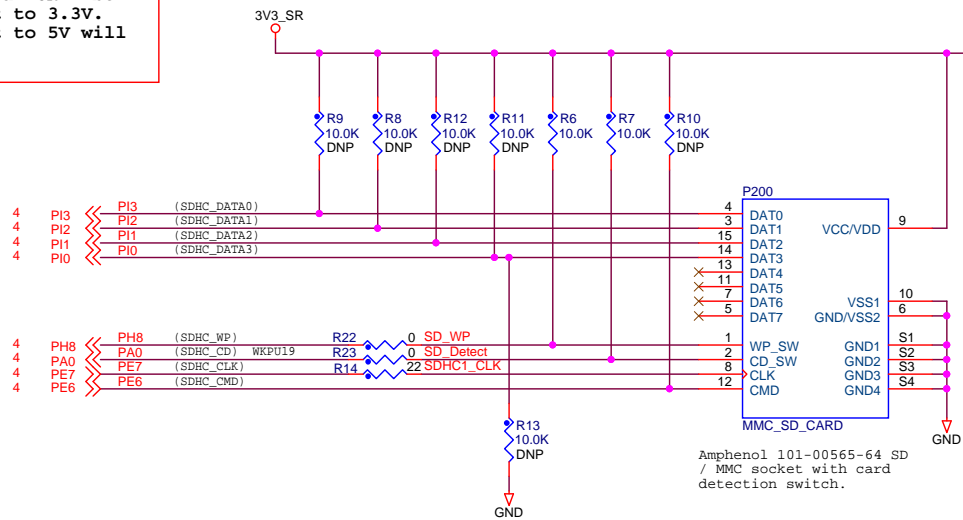
Figure 5-7: Connector Interface to Main Board

Pin 39	3.3V switched	Pin 40	3.3V switched
Pin 37	3.3V switched	Pin 38	3.3V switched
Pin 35	SDA	Pin 36	Reserved
Pin 33	RS	Pin 34	RS
Pin 31	TDO/DINT	Pin 32	TDO/SDA
Pin 29	TCK/DSC/L	Pin 30	TMS
Pin 27	EMERGENCY	Pin 28	MCK_IN
Pin 25	RST	Pin 26	RSOUT
Pin 23	STATUS (shunt/undervoltage)	Pin 24	PS1/PS0
Pin 21	PS0	Pin 22	PS1
Pin 19	Reserved	Pin 20	Reserved
Pin 17	Reserved (MCKST_R0P)	Pin 18	Reserved
Pin 15	Reserved (MCKST_R0P)	Pin 16	RMCK
Pin 13	Reserved (MCKST_R0P)	Pin 14	Reserved
Pin 11	RSVD	Pin 12	RSVD
Pin 9	RSVD	Pin 10	RSVD
Pin 7	RSVD	Pin 8	RSVD
Pin 5	RSVD	Pin 6	RSVD
Pin 3	RSVD	Pin 4	RSVD
Pin 1	RSVD	Pin 2	RSVD

- Power Supply
- IC Interface
- Debug & JTAG Interface
- Misc Signals
- Board ID
- Network Interface
- RMCK
- DS Interface
- MediaLB 3-Pin

Caution

The SD card specification details an operating voltage of between 2.7 and 3.6V. If using the SD card, it can ONLY be used when VDD_HV_A (and PER_HVA) jumpers are set to 3.3V. Inserting an SD card with VDD_HV_A / PER_HVA set to 5V will result in card damage.

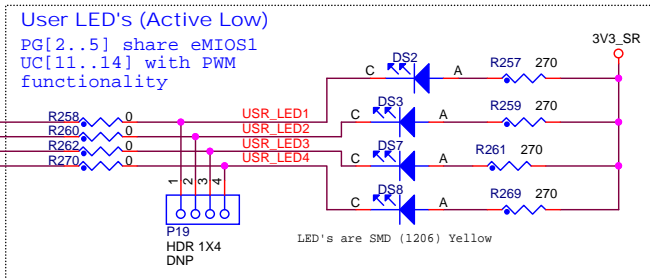


Card Detect: Grounded when Card Inserted, Pulled high when card removed
 Write Protect: Grounded when NOT protected, Pulled high when protected (or card removed)

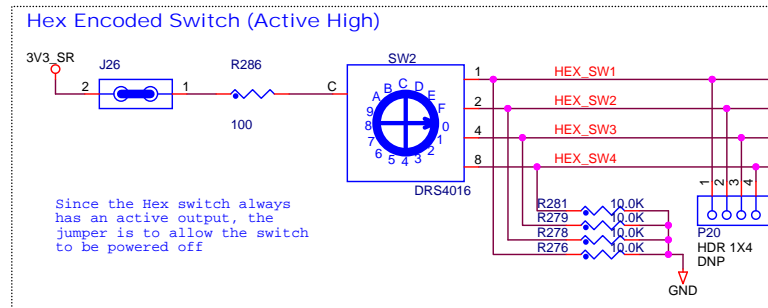
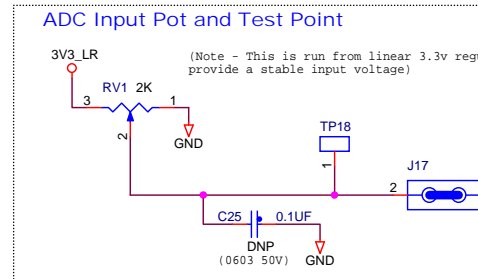


Peripherals, Audio Controls and GPIO

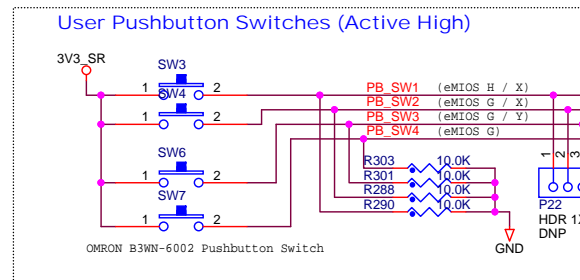
The ADC is hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)
 The LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains
 The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage



Note that LED2 and LED4 (PG3 and PG5) can be controlled in LPU_RUN mode (and also have pad keepers in LPU_STANDBY)



The LED's, Hex switches and push-button switches are connected to MCU pads vvia zero ohm links. If desired these can be removed and direct connection made to the LED or switch. All of the ports used for LED's / Switches are also bonded out to the GPIO matrix

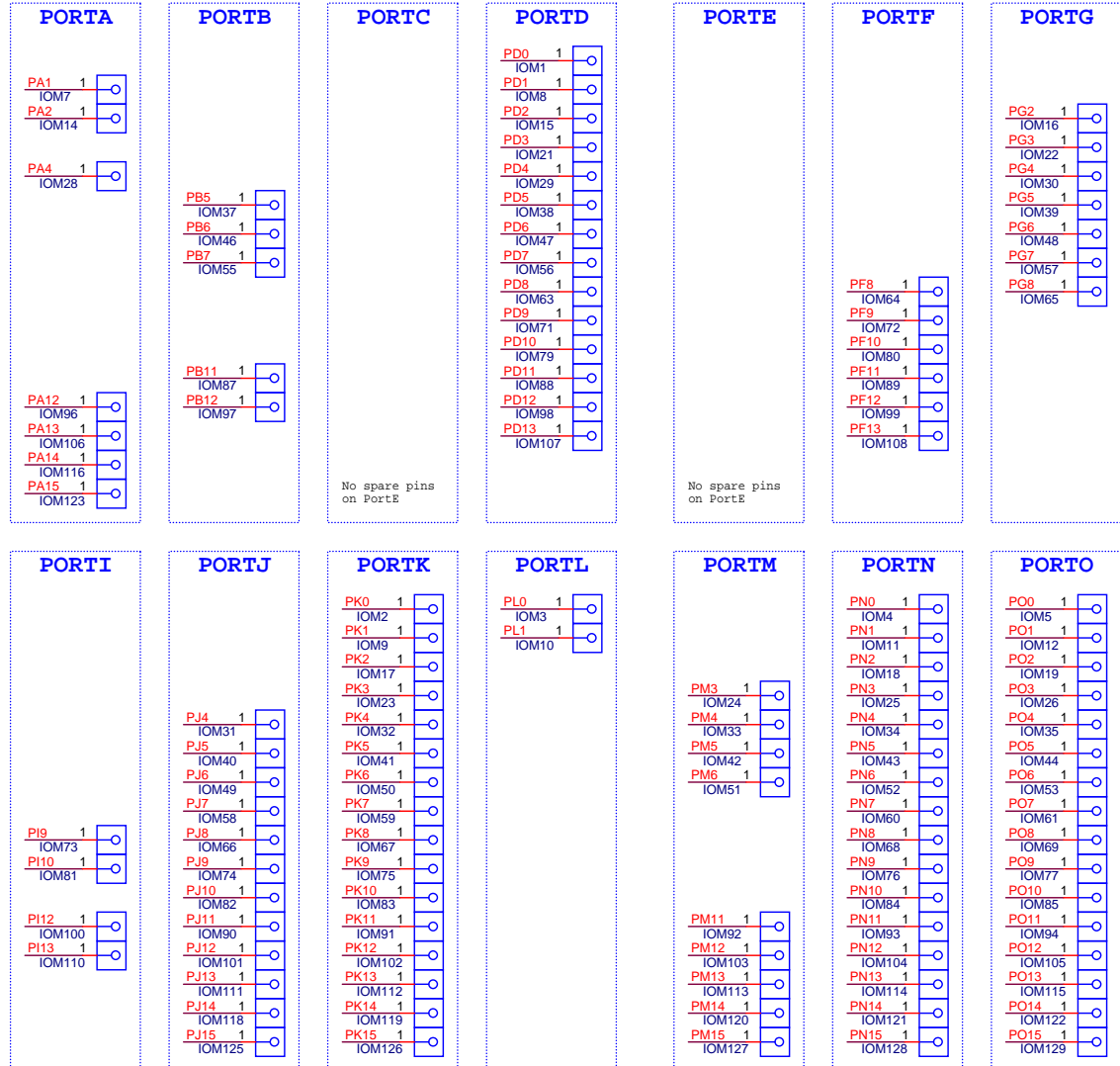




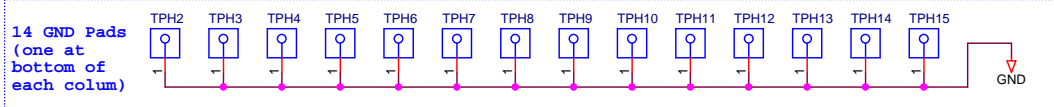
Matrix

All pads are DNP (Do Not Populate) 0.1" pitch headers placed on a 0.1" grid

PA[1,2] shared with user switches	4,15	PA1	PA1
	4,15	PA2	PA2
	4	PA4	PA4
PA[12..15] shared with SAI Audio and TWRPI	4,12	PA12	PA12
	4,12	PA13	PA13
	4,12	PA14	PA14
	4,12	PA15	PA15
	4	PB5	PB5
	4	PB6	PB6
	4	PB7	PB7
	4	PB11	PB11
	4	PB12	PB12
PD[0..3] shared with Hex Switch	4,15	PD0	PD0
	4,15	PD1	PD1
	4,15	PD2	PD2
	4,15	PD3	PD3
PD[4..8] shared with TWRPI connector with pullup on PD[7], PD[8]	4,12	PD4	PD4
	4,12	PD5	PD5
	4,12	PD6	PD6
	4,12	PD7	PD7
	4,12	PD8	PD8
	4	PD9	PD9
	4	PD10	PD10
	4	PD11	PD11
	4	PD12	PD12
	4	PD13	PD13
PD[13] shared with SAI Audio and MLB headers	4,12,13	PD13	PD13
PI[12,13] shared with MLB header	4	PI9	PI9
	4	PI10	PI10
	4,13	PI12	PI12
	4,13	PI13	PI13
	4	PJ4	PJ4
	4	PJ5	PJ5
	4	PJ6	PJ6
	4	PJ7	PJ7
	4	PJ8	PJ8
	4	PJ9	PJ9
	4	PJ10	PJ10
	4	PJ11	PJ11
	4	PJ12	PJ12
	4	PJ13	PJ13
	4	PJ14	PJ14
	4	PJ15	PJ15
PK[0..4] shared with TWRPI header	4,12	PK0	PK0
	4,12	PK1	PK1
	4,12	PK2	PK2
	4,12	PK3	PK3
	4,12	PK4	PK4
	4	PK5	PK5
	4	PK6	PK6
	4	PK7	PK7
	4	PK8	PK8
	4	PK9	PK9
	4	PK10	PK10
	4	PK11	PK11
	4	PK12	PK12
	4	PK13	PK13
	4	PK14	PK14
	4	PK15	PK15
	4	PL0	PL0
	4	PL1	PL1



Busses are not used on ports as it makes it harder to see which pins are shared with other functions



- Layout Notes:**
- Pads must be placed in a 13 x 16 matrix pattern, 2.54 mm pitch
 - 13 wide (one column for each port EXCLUDING those with no available pads ie C, E, H, Q)
 - 16 tall (1 row for each port number from 0 to 15).
 - GND pad at bottom of each column
 - After production, pads should be through hole (not solder filled)



324 BGA DC



MCU Power Connections

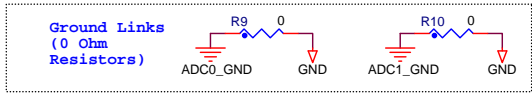
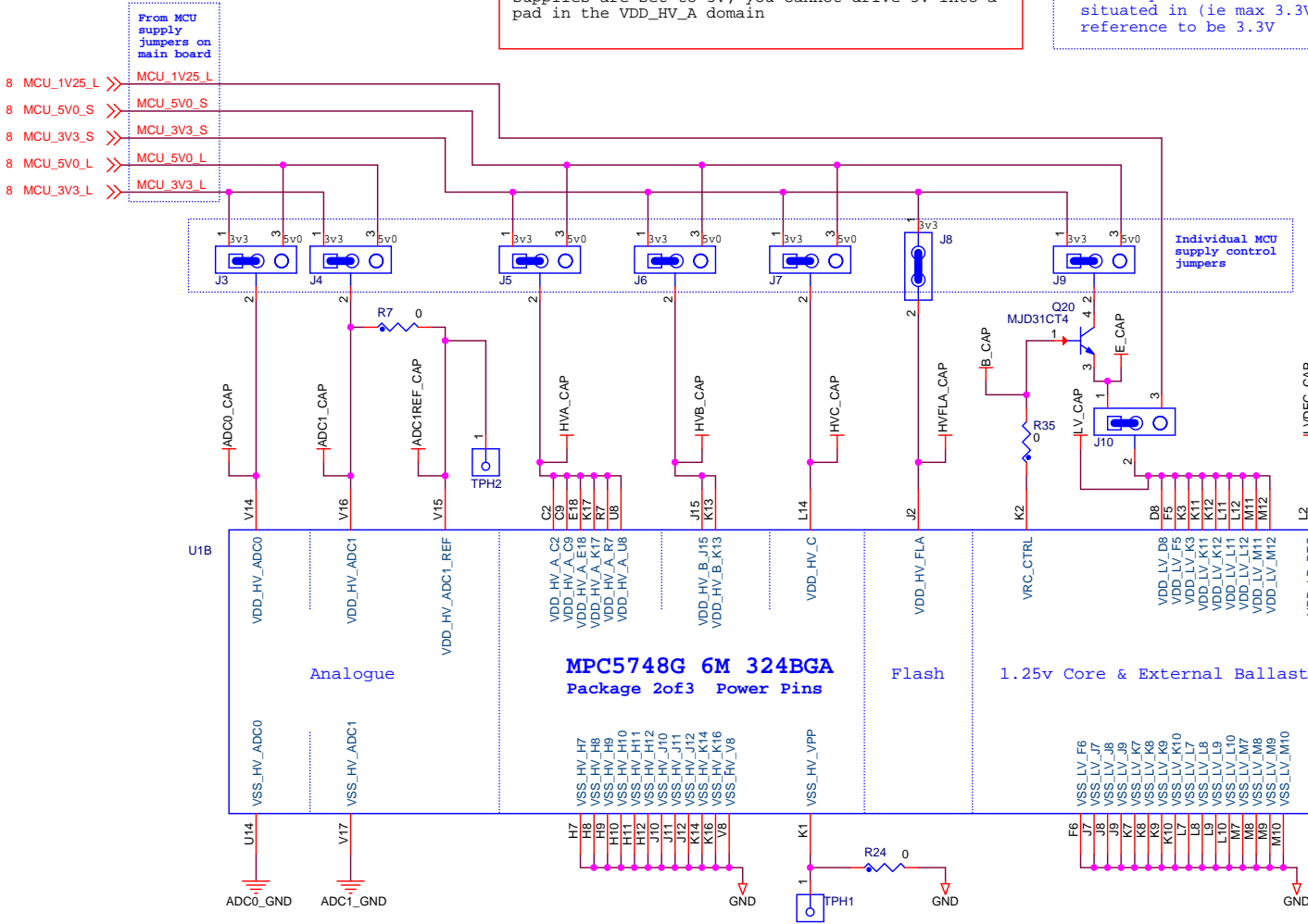
Caution:

- If VDD_HV_A is driven from 5V, the VDD_HV_FL A pin must not be supplied from 3.3V (remove the HVA_FL A jumper)
- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuraiton:

- ALL MCU supply voltage
- VDD_HV_B, VDD_HV_C, VBAI
- VDD_HV_FL A = External
- VDD_LV Supplied from K

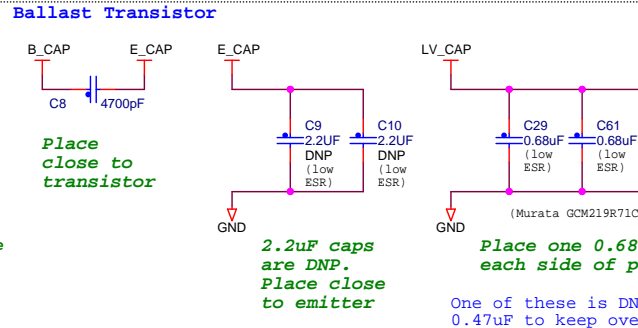
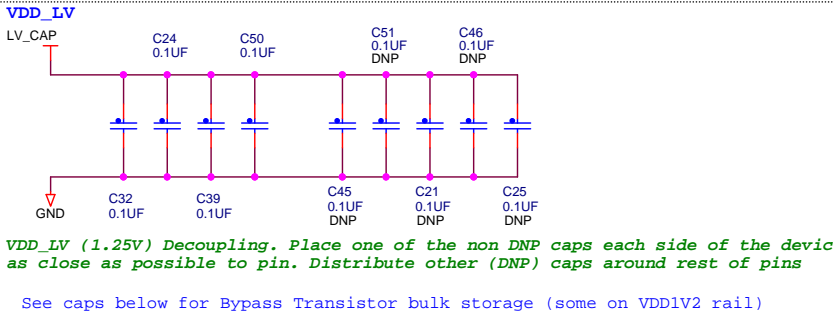
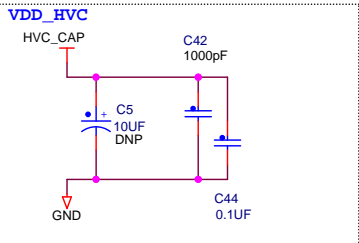
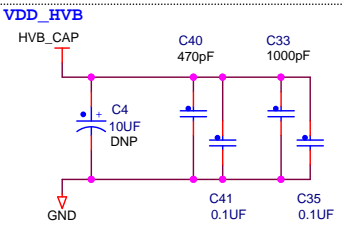
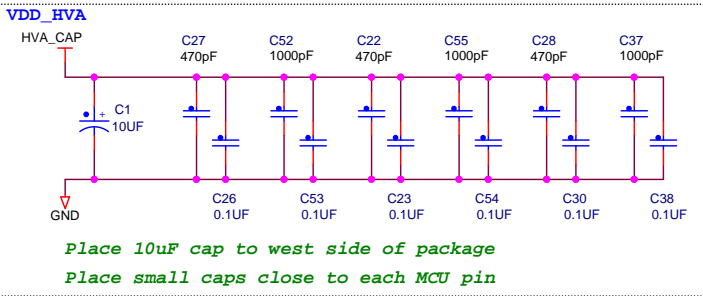
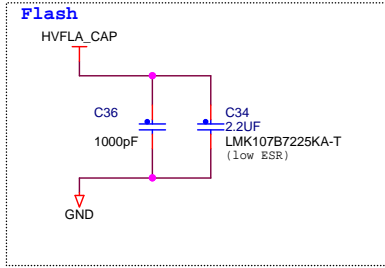
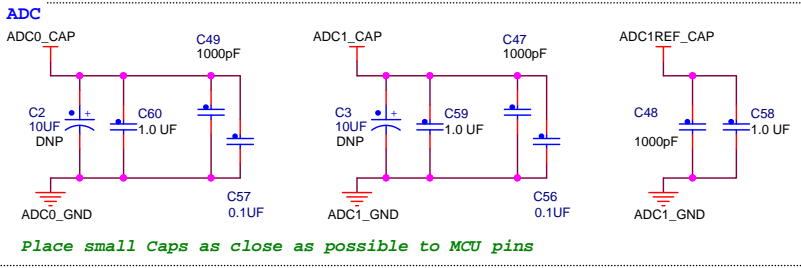
This is not necessarily VDD_HV_x domains have at 3.3V. Therefore the defa can only be driven to th situated in (ie max 3.3V reference to be 3.3V





MCU Decoupling and bulk storage

Capacitance values:
 470pF
 1000pF
 4700pF
 0.01uF
 0.1uF
 0.68uF
 1.0uF
 2.2uF
 4.7uF
 10uF
 4.7uF
 7343-10





GPIO 1 of 2

** PA1 is also NMI. Routed to I/O Matrix

(WKPU2 / NMIO) (WKPU3)

8	PA0	((SD_CD - WKPU9) PA0	L5
8	PA1	((SW1 & GPIO**) PA1	K6
8	PA2	((SW2 & GPIO) PA2	J6
8	PA3	((MII_RXCLK) PA3	M17
8	PA4	((CMP1_13 / IO) PA4	P6
8	PA5	((SAL_GPIO) PA5	A14
8	PA6	((MLB_GPIO) PA6	A13
8	PA7	((MII_RXD2) PA7	F17
8	PA8	((RMI1_RXD1) PA8	F18
8	PA9	((RMI1_RXD0) PA9	E17
8	PA10	((MII_COL) PA10	D18
8	PA11	((RMI1_RXER) PA11	D17
8	PA12	((CMP1_15 / IO) PA12	N8
8	PA13	((CMP1_14 / IO) PA13	P7
8	PA14	((CMP1_12 / IO) PA14	T3
8	PA15	((CMP1_10 / IO) PA15	N7

Key to text colours:

- Purple - Connect physical interfaces
- Orange - Other peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg LED)
- Green - I/O Matrix (dedicated)

8	PB0	((CAN0_TX) PB0	N1
8	PB1	((CAN0_RX) PB1	N2
8	PB2	((LINO_TX) PB2	G9
8	PB3	((LINO_RX) PB3	G8
8	PB4	((ADC_POT) PB4	N11
8	PB5	((GPIO) PB5	R14
8	PB6	((GPIO) PB6	N12
8	PB7	((GPIO) PB7	P14
6	PB8	((XTAL32) PB8	V10
6	PB9	((EXTAL32) PB9	V9
8	PB10	((SAIO_SYNC) PB10	P9
8	PB11	((GPIO) PB11	P13
8	PB12	((GPIO) PB12	N13
8	PB13	((MLB_DN) PB13	T18
7	PB14	((MLB_SN) PB14	R17
7	PB15	((MLB_CN / SIG) PB15	R18

8	PC0	((TDI) PC0	F9
8	PC1	((TDO) PC1	F10
8	PC2	((USB1_CLK) PC2	C13
8	PC3	((USB1_DIR) PC3	D11
8	PC4	((FR_A_TX_EN) PC4	B12
8	PC5	((FR_A_TX) PC5	A11
8	PC6	((LINI_TX) PC6	R3
8	PC7	((LINI_RX) PC7	U2
8	PC8	((RS232_TX) PC8	D5
8	PC9	((RS232_RX) PC9	D4
8	PC10	((CAN1_TX) PC10	M5
8	PC11	((CAN1_RX) PC11	M4
8	PC12	((FR_DBG0) PC12	D6
8	PC13	((FR_DBG1) PC13	E6
8	PC14	((FR_DBG2) PC14	B2
8	PC15	((FR_DBG3) PC15	C3

8	PD0	((HEX1 & GPIO) PD0	R12
8	PD1	((HEX2 & GPIO) PD1	T13
8	PD2	((HEX3 & GPIO) PD2	T14
8	PD3	((HEX4 & GPIO) PD3	R13
8	PD4	((GPIO) PD4	P11
8	PD5	((GPIO) PD5	T15
8	PD6	((GPIO) PD6	U15
8	PD7	((GPIO) PD7	R15
8	PD8	((GPIO) PD8	F12
8	PD9	((GPIO) PD9	N15
8	PD10	((GPIO) PD10	P15
8	PD11	((GPIO) PD11	V18
8	PD12	((GPIO) PD12	N16
8	PD13	((GPIO & MLB_ST) PD13	N14
7	PD14	((MLB_DP) PD14	T17
7	PD15	((MLB_SF / DAT) PD15	P17

8	MCU-RSTx	((MCU-RSTx) L1	RESET
8	PORSTx	((PORSTx) C12	PORST
6	MCU-XTAL	((MCU-XTAL) V6	XTAL
6	MCU-EXTAL	((MCU-EXTAL) V7	EXTAL

U1A

MPC5748G 324 BGA Package Iof3 GPIO Pins1

PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7	PA8	PA9	PA10	PA11	PA12	PA13	PA14	PA15
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PE0	PE1	PE2	PE3	PE4	PE5	PE6	PE7	PE8	PE9	PE10	PE11	PE12	PE13	PE14	PE15
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------

PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7	PB8/XTAL32	PB9/EXTAL32	PB10	PB11	PB12	PB13	PB14	PB15
-----	-----	-----	-----	-----	-----	-----	-----	------------	-------------	------	------	------	------	------	------

N9	PF0	PF1	PF2	PF3	PF4	PF5	PF6	PF7	PF8	PF9	PF10	PF11	PF12	PF13	PF14	PF15
----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------

PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7	PC8	PC9	PC10	PC11	PC12	PC13	PC14	PC15
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------

H18	PG0	PG1	PG2	PG3	PG4	PG5	PG6	PG7	PG8	PG9	PG10	PG11	PG12	PG13	PG14	PG15
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------

PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	PD9	PD10	PD11	PD12	PD13	PD14	PD15
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------

L17	PH0	PH1	PH2	PH3	PH4	PH5	PH6	PH7	PH8	PH9	PH10	PH11	PH12	PH13	PH14	PH15
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	------	------



MPC5748G GPIO 2 of 2

Legend

- Orange - Various peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg LED)
- Green - I/O Matrix (dedicated)

U1C

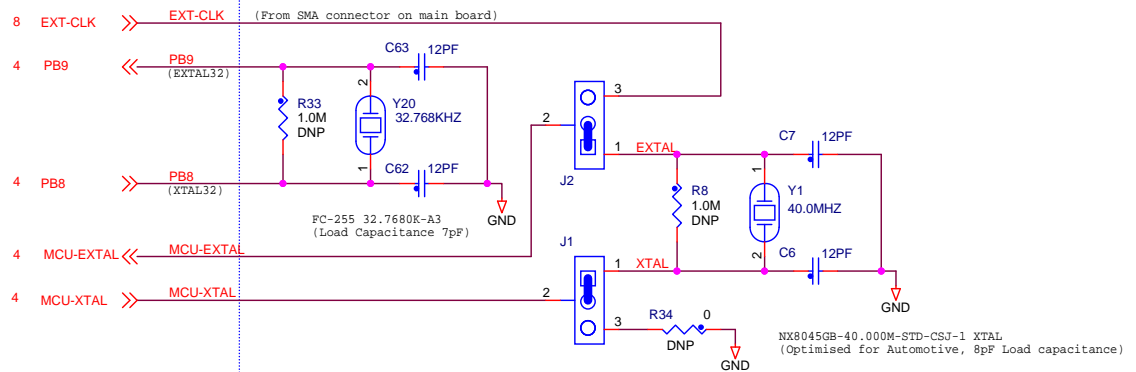
MPC5748G 324 BGA
 Package 3of3 GPIO Pins2

8	PI0	((SD_D3))	PI0	C6	PI0
8	PI1	((SD_D2))	PI1	E7	PI1
8	PI2	((SD_D1))	PI2	C7	PI2
8	PI3	((SD_D0))	PI3	C8	PI3
8	PI4	((USB1_STP))	PI4	A18	PI4
8	PI5	((USB1_NXT))	PI5	E11	PI5
8	PI6	((USB0_RST))	PI6	H4	PI6
8	PI7	((USB1_RST))	PI7	G3	PI7
8	PI8	((MLB_CP / CLK))	PI8	P18	PI8
8	PI9	((GPIO))	PI9	T12	PI9
8	PI10	((GPIO))	PI10	U12	PI10
8	PI11	((ENET_RST))	PI11	N18	PI11
8	PI12	((GPIO & MLB_PS0))	PI12	N17	PI12
8	PI13	((GPIO & MLB_PS1))	PI13	M16	PI13
8	PI14	((SAI2_D0))	PI14	R16	PI14
8	PI15	((SAI2_MCLK))	PI15	P16	PI15
8	PJ0	((SAI2_SYNC))	PJ0	U18	PJ0
8	PJ1	((SAI2_BCLK))	PJ1	V13	PJ1
8	PJ2	((SAI1_D0))	PJ2	R11	PJ2
8	PJ3	((SAI1_BCLK))	PJ3	U11	PJ3
8	PJ4	((GPIO))	PJ4	A1	PJ4
8	PJ5	((GPIO))	PJ5	T16	PJ5
8	PJ6	((GPIO))	PJ6	U16	PJ6
8	PJ7	((GPIO))	PJ7	U17	PJ7
8	PJ8	((GPIO))	PJ8	U13	PJ8
8	PJ9	((GPIO))	PJ9	V5	PJ9
8	PJ10	((GPIO))	PJ10	V4	PJ10
8	PJ11	((GPIO))	PJ11	U3	PJ11
8	PJ12	((GPIO))	PJ12	V3	PJ12
8	PJ13	((GPIO))	PJ13	T6	PJ13
8	PJ14	((GPIO))	PJ14	R6	PJ14
8	PJ15	((GPIO))	PJ15	U4	PJ15
8	PK0	((GPIO))	PK0	T4	PK0
8	PK1	((GPIO))	PK1	N3	PK1
8	PK2	((GPIO))	PK2	N4	PK2
8	PK3	((GPIO))	PK3	P1	PK3
8	PK4	((GPIO))	PK4	P2	PK4
8	PK5	((GPIO))	PK5	P3	PK5
8	PK6	((GPIO))	PK6	P4	PK6
8	PK7	((GPIO))	PK7	R1	PK7
8	PK8	((GPIO))	PK8	R2	PK8
8	PK9	((GPIO))	PK9	B7	PK9
8	PK10	((GPIO))	PK10	A6	PK10
8	PK11	((GPIO))	PK11	B6	PK11
8	PK12	((GPIO))	PK12	A5	PK12
8	PK13	((GPIO))	PK13	B5	PK13
8	PK14	((GPIO))	PK14	C5	PK14
8	PK15	((GPIO))	PK15	A4	PK15
8	PL0	((GPIO))	PL0	B4	PL0
8	PL1	((GPIO))	PL1	L15	PL1
8	PL2	((MDO0))	PL2	E15	PL2
8	PL3	((MDO1))	PL3	E14	PL3
8	PL4	((MDO2))	PL4	F13	PL4
8	PL5	((MDO3))	PL5	F14	PL5
8	PL6	((MDO4))	PL6	F15	PL6
8	PL7	((MDO5))	PL7	G13	PL7
8	PL8	((EVT1))	PL8	D15	PL8
8	PL9	((MSE00))	PL9	E13	PL9
8	PL10	((MCK0))	PL10	G12	PL10
8	PL11	((MSE01))	PL11	E16	PL11
8	PL12	((EVT0))	PL12	D16	PL12
8	PL13	((MDO6))	PL13	F16	PL13
8	PL14	((MDO7))	PL14	G16	PL14
8	PL15	((MDO8))	PL15	G15	PL15
8	PQ0	((USB0_STP))	PQ0	C11	PQ0
8	PQ1	((USB0_CLK))	PQ1	B13	PQ1
8	PQ2	((USB0_DIR))	PQ2	B14	PQ2
8	PQ3	((USB0_NXT))	PQ3	F11	PQ3
8	PQ4	((USB0_D7))	PQ4	A15	PQ4
8	PQ5	((USB0_D6))	PQ5	A16	PQ5
8	PQ6	((USB0_D5))	PQ6	B15	PQ6
8	PQ7	((USB0_D4))	PQ7	A17	PQ7

PM0	G14	PM0	(MDO9)
PM1	H13	PM1	(MDO10)
PM2	H15	PM2	(MDO11)
PM3	L13	PM3	(GPIO)
PM4	K15	PM4	(GPIO)
PM5	M14	PM5	(GPIO)
PM6	L16	PM6	(GPIO)
PM7	H16	PM7	(MDO12)
PM8	J13	PM8	(MDO13)
PM9	H14	PM9	(MDO14)
PM10	J14	PM10	(MDO15)
PM11	G10	PM11	(GPIO)
PM12	G11	PM12	(GPIO)
PM13	M13	PM13	(GPIO)
PM14	M15	PM14	(GPIO)
PM15	T10	PM15	(GPIO)
PN0	T9	PN0	(GPIO)
PN1	V11	PN1	(GPIO)
PN2	U9	PN2	(GPIO)
PN3	T8	PN3	(GPIO)
PN4	U7	PN4	(GPIO)
PN5	R8	PN5	(GPIO)
PN6	P8	PN6	(GPIO)
PN7	U6	PN7	(GPIO)
PN8	U5	PN8	(GPIO)
PN9	T5	PN9	(GPIO)
PN10	T7	PN10	(GPIO)
PN11	V2	PN11	(GPIO)
PN12	U1	PN12	(GPIO)
PN13	R4	PN13	(GPIO)
PN14	L4	PN14	(GPIO)
PN15	L4	PN15	(GPIO)
PO0	G1	PO0	(GPIO)
PO1	F1	PO1	(GPIO)
PO2	M6	PO2	(GPIO)
PO3	L6	PO3	(GPIO)
PO4	E1	PO4	(GPIO)
PO5	H6	PO5	(GPIO)
PO6	H5	PO6	(GPIO)
PO7	D1	PO7	(GPIO)
PO8	D2	PO8	(GPIO)
PO9	E3	PO9	(GPIO)
PO10	D3	PO10	(GPIO)
PO11	C1	PO11	(GPIO)
PO12	B1	PO12	(GPIO)
PO13	E4	PO13	(GPIO)
PO14	F4	PO14	(GPIO)
PO15	G6	PO15	(GPIO)
PP0	G5	PP0	(GPIO)
PP1	B3	PP1	(GPIO)
PP2	C4	PP2	(GPIO)
PP3	F7	PP3	(GPIO)
PP4	E5	PP4	(GPIO)
PP5	G7	PP5	(GPIO)
PP6	A2	PP6	(GPIO)
PP7	A3	PP7	(GPIO)
PP8	B8	PP8	(GPIO)
PP9	A7	PP9	(GPIO)
PP10	A8	PP10	(GPIO)
PP11	B9	PP11	(GPIO)
PP12	B17	PP12	(USB0_D3)
PP13	B16	PP13	(USB0_D2)
PP14	C17	PP14	(USB0_D1)
PP15	B18	PP15	(USB0_D0)



Oscillators and External Clock

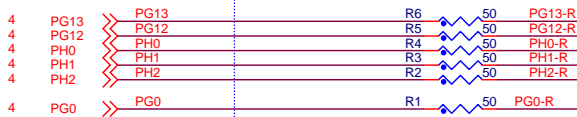




Speed Signal Termination

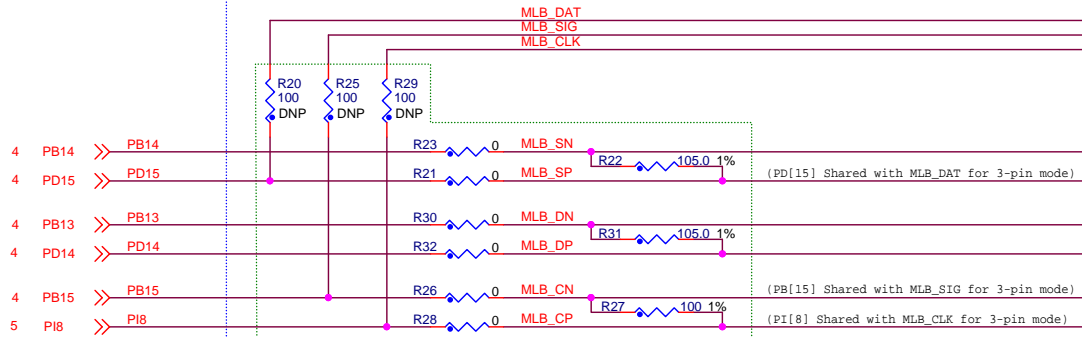
5 4 3 2

Ethernet Termination



Place resistors as close as possible to MCU

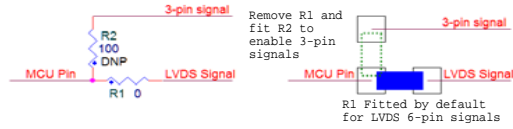
MLB Termination



Place resistors as close as possible to MCU

From MCU

Layout Note - Place resistors as shown with shared pad (as close to MCU as possible)



5 4 3 2



256 BGA DC



MPC5748G Customer EVB 256BGA [6M/3M] Daughter Card (X-MP

Table Of Contents:	
Power - MPC5748G power pins footprint	Sheet 2
Power - MPC5748G Decoupling Capacitors	Sheet 3
GPIO - MPC5748G GPIO pins 1 of 2	Sheet 4
GPIO - MPC5748G GPIO pins 2 of 2	Sheet 5
Clocks	Sheet 6
Bus Termination	Sheet 7
Daughtercard Connectors	Sheet 8

Revision Information

Rev	Date	Designer	Comments
X1	11 Mar 2013	Alasdair Robertson	Initial release
X2	13 Mar 2013	Alasdair Robertson	Version sent
X3	15 Mar 2013	Alasdair Robertson	Component c
X4	29 Mar 2013	Alasdair Robertson	Changes mad
X5	15 Apr 2013	Alasdair Robertson	LAY RefDes
A	15 Apr 2013	Alasdair Robertson	Post Layout (
X1	16 Mar 2014	Jesus Sanchez	Changes on M SCH-27899 d
A	18 Apr 2014	Jesus Sanchez	Post Layout.
A1	18 Aug 2015	Alasdair Robertson	Tidy up Sche

Caution:

These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale MPC5748G family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points are denoted TPx
- Test point Vias are denoted TPVx

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in *ITALICS*



This document is for procurement or

Designer:
A. Robertson / J. Sand

Drawn by:
A. Robertson

Approved:
A. Robertson / J. Sand



MCU Power Connections

Caution:

- If VDD_HV_A is driven from 5V, the VDD_HV_FL A pin must not be supplied from 3.3V (remove the HVA_FL A jumper)

- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuraiton:

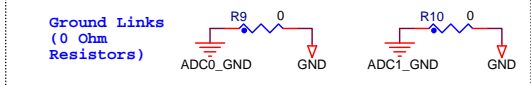
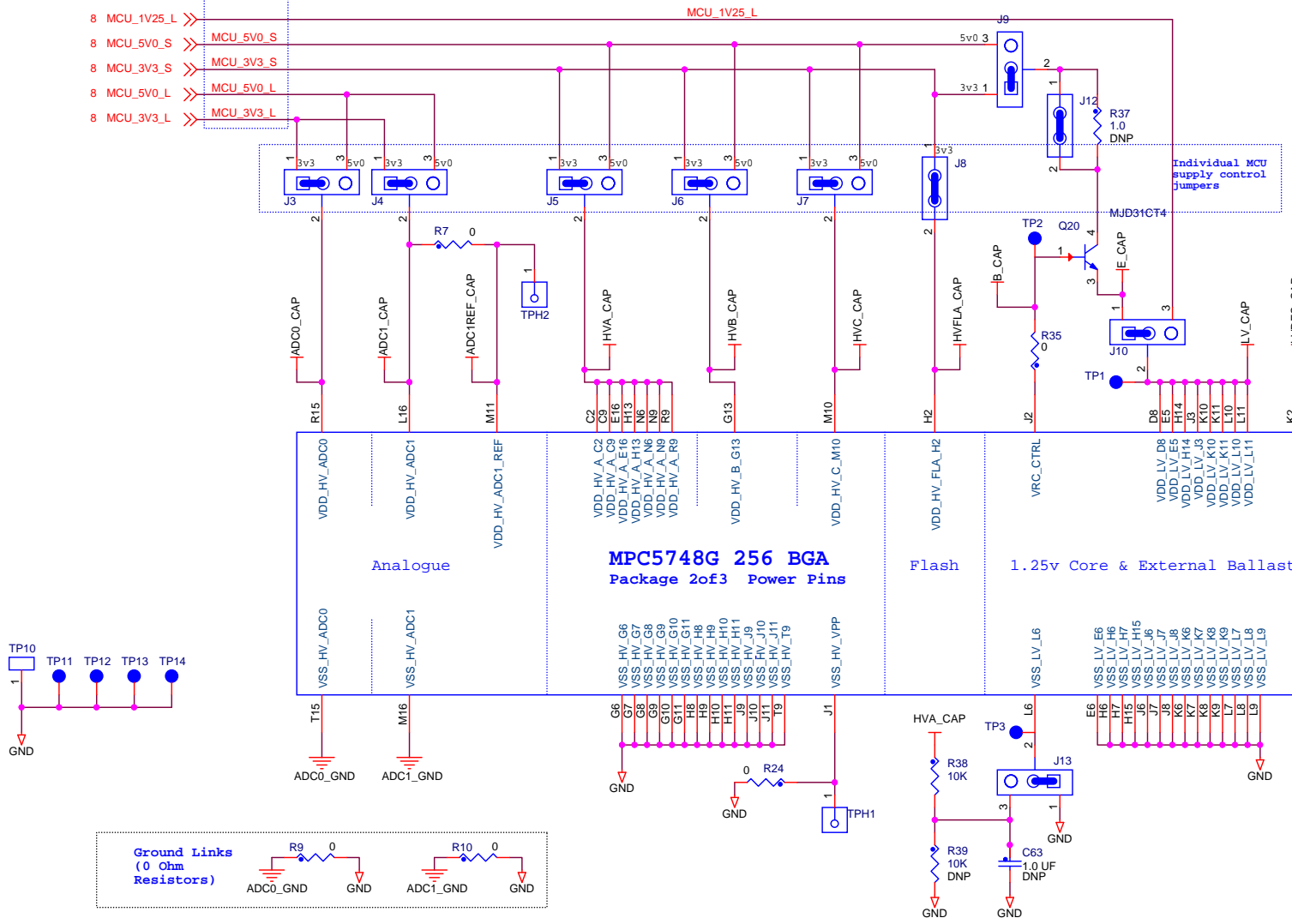
- ALL MCU supply voltage
- VDD_HV_B, VDD_HV_C, VBAI
- VDD_HV_FL A = External
- VDD_LV Supplied from K

This is not necessarily VDD_HV_x domains have at 3.3V. Therefore the defa can only be driven to th situated in (ie max 3.3V reference to be 3.3V

From MCU supply jumpers on main board

- 8 MCU_1V25_L >> MCU_1V25_L
- 8 MCU_5V0_S >> MCU_5V0_S
- 8 MCU_3V3_S >> MCU_3V3_S
- 8 MCU_5V0_L >> MCU_5V0_L
- 8 MCU_3V3_L >> MCU_3V3_L

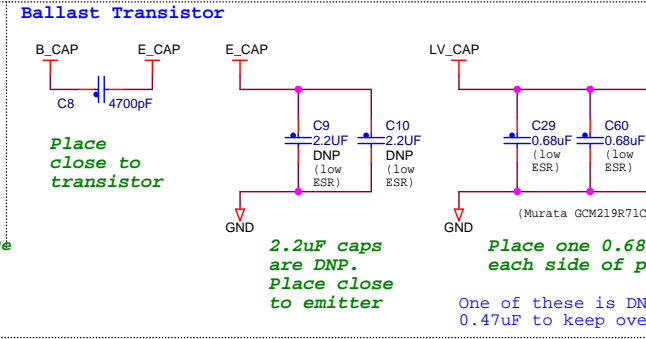
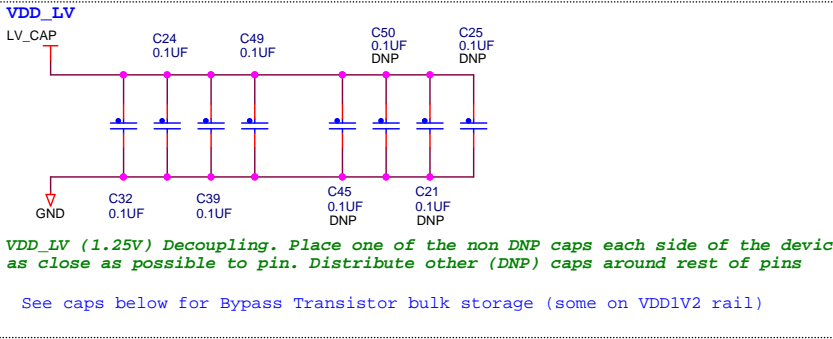
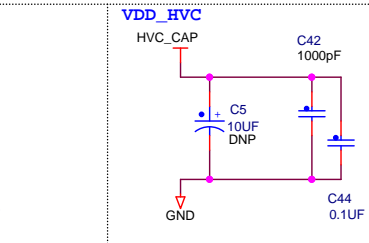
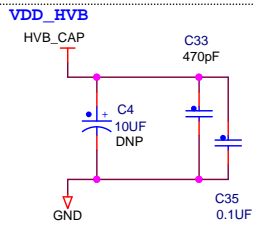
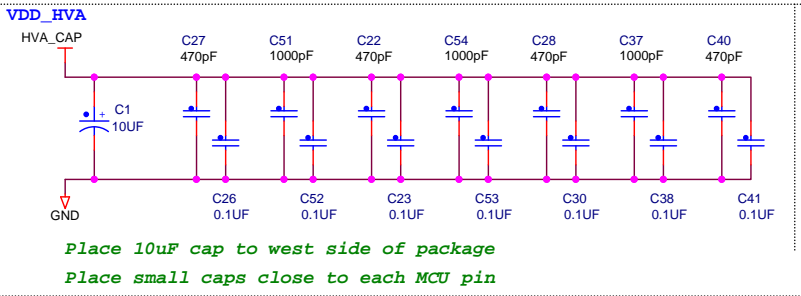
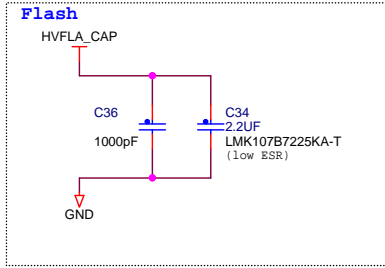
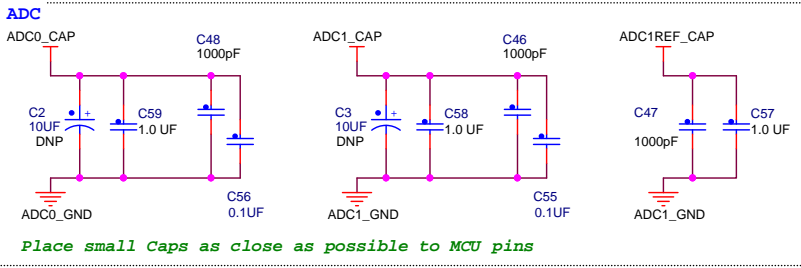
Individual MCU supply control jumpers





MCU Decoupling and bulk storage

Capacitance values:
 470pF
 1000pF
 4700pF
 0.01uF
 0.1uF
 0.68uF
 1.0uF
 2.2uF
 4.7uF
 10uF
 4.7uF
 7343-10

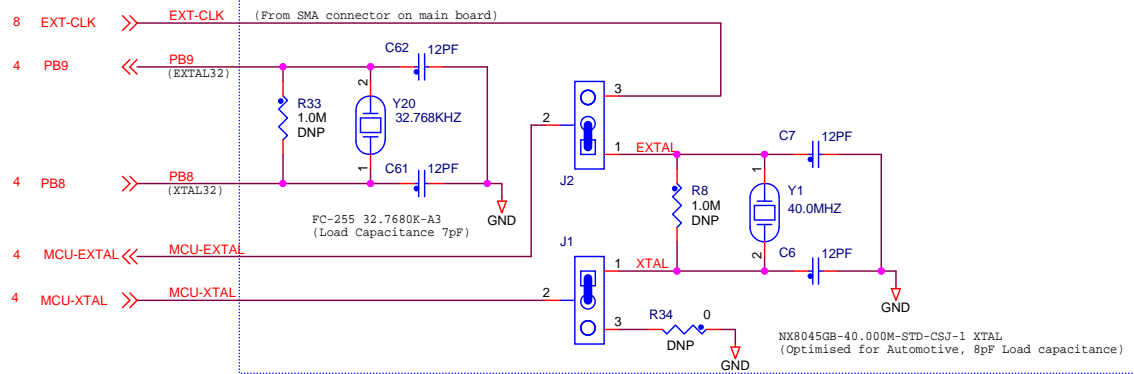


Differences to 324BGA

- 1 more VDD_HV_A capacitor pair
- 1 fewer VDD_HV_B capacitor pair
- 1 fewer VDD_LV capacitor (one of DNP caps)



Oscillators and External Clock

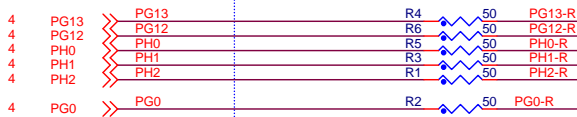




Speed Signal Termination

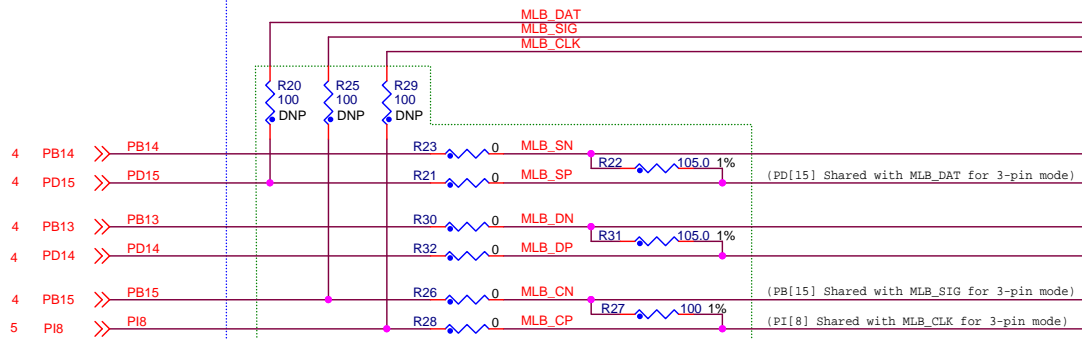
5 4 3 2

Ethernet Termination



Place resistors as close as possible to MCU

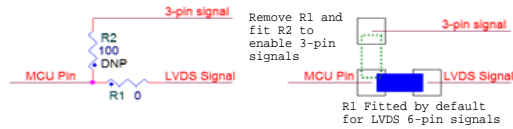
MLB Termination



Place resistors as close as possible to MCU

From MCU

Layout Note - Place resistors as shown with shared pad (as close to MCU as possible)



5 4 3 2



176 QFP DC



MCU Power Connections

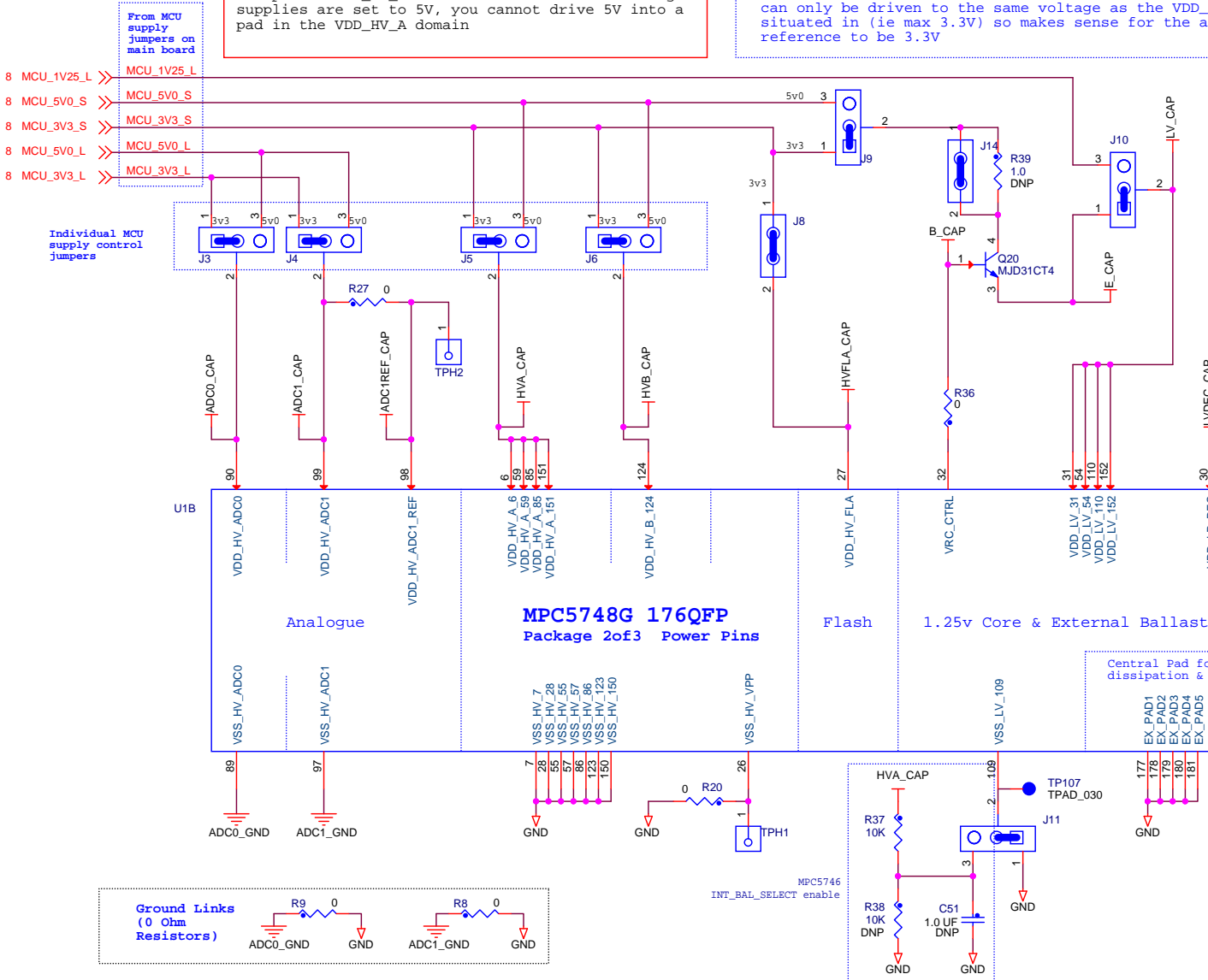
Caution:

- If VDD_HV_A is driven from 5V, the VDD_HV_FL A pin must not be supplied from 3.3V (remove the HVA_FL A jumper)
- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuraiton:

- ALL MCU supply voltages are set to 3.3V (ADC0, A VDD_HV_B, VDD_HV_C, VBallast)
- VDD_HV_FL A = External 3.3V supplied (jumper fitted)
- VDD_LV Supplied from ballast transistor

This is not necessarily the same as the default sh VDD_HV_x domains have at least one peripheral that 3.3V. Therefore the default is to run these from 3 can only be driven to the same voltage as the VDD_ situated in (ie max 3.3V) so makes sense for the a reference to be 3.3V



From MCU supply jumpers on main board

Individual MCU supply control jumpers

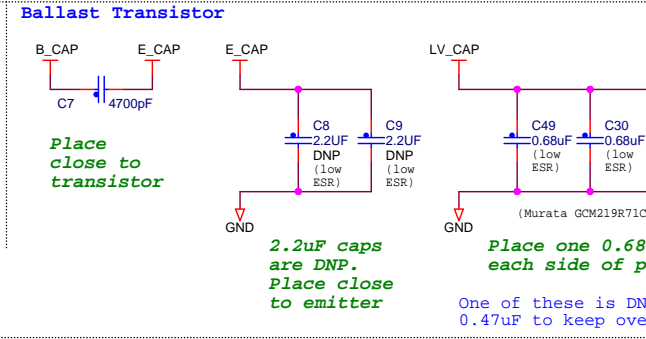
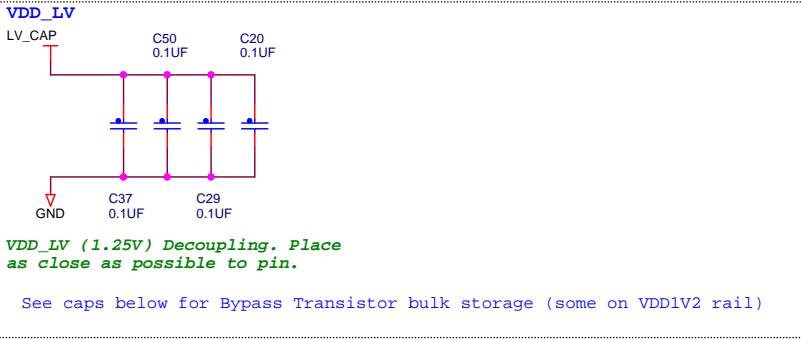
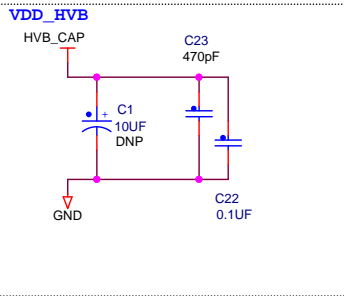
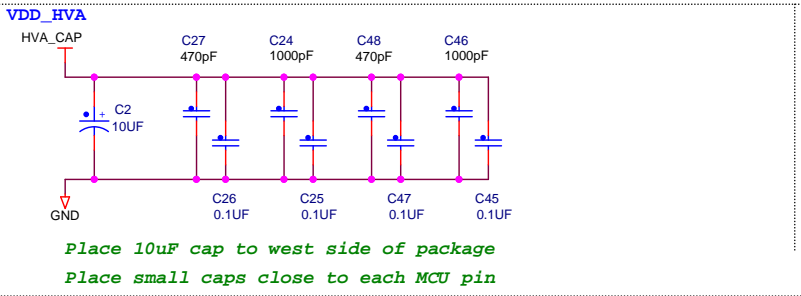
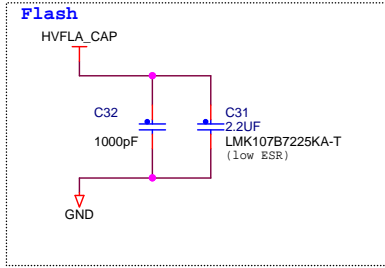
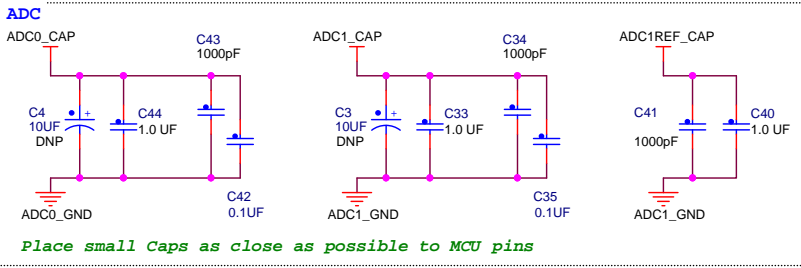
Ground Links (0 Ohm Resistors)

Central Pad for dissipation &



MCU Decoupling and bulk storage

Capacitance values:
 470pF
 1000pF
 4700pF
 0.01uF
 0.1uF
 0.68uF
 1.0uF
 2.2uF
 4.7uF
 10uF
 4.7uF
 7343-10



- Differences to 324BGA
- 2 Fewer VDD_HV_A capacitor pairs
 - 1 fewer VDD_HV_B capacitor pair
 - No VDD_HV_C capacitor pairs
 - 5 fewer VDD_LV capacitor pairs



GPIO 1 of 2

** PA1 is also NMI. Routed to I/O Matrix (WKPU2 / NMIO) (WKPU3)

Key to text colours:

- Purple - Games Physical Interfaces
- Orange - Other Peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg LED)
- Green - I/O Matrix (dedicated)

8	PA0	<<< (SD_CD - WKPU9) PA0	24
8	PA1	<<< (SW1 & GPIO**) PA1	19
8	PA2	<<< (SW2 & GPIO) PA2	17
8	PA3	<<< (MII_RXCLK) PA3	114
8	PA4	<<< (CMP1_13 / IO) PA4	51
8	PA5	<<< (SAL_GPIO) PA5	146
8	PA6	<<< (MLB_GPIO) PA6	147
8	PA7	<<< (MII_RXD2) PA7	128
8	PA8	<<< (RMI1_RXD1) PA8	129
8	PA9	<<< (RMI1_RXD0) PA9	130
8	PA10	<<< (MII_COL) PA10	131
8	PA11	<<< (RMI1_RXER) PA11	132
8	PA12	<<< (CMP1_15 / IO) PA12	53
8	PA13	<<< (CMP1_14 / IO) PA13	52
8	PA14	<<< (CMP1_12 / IO) PA14	50
8	PA15	<<< (CMP1_10 / IO) PA15	48
8	PB0	<<< (CAN0_TX) PB0	39
8	PB1	<<< (CAN0_RX) PB1	40
8	PB2	<<< (LINO_TX) PB2	176
8	PB3	<<< (LINO_RX) PB3	1
8	PB4	<<< (ADC_POT) PB4	88
8	PB5	<<< (GPIO) PB5	91
8	PB6	<<< (GPIO) PB6	92
8	PB7	<<< (GPIO) PB7	93
6	PB8	<<< (XTAL32) PB8	61
6	PB9	<<< (EXTAL32) PB9	60
8	PB10	<<< (SAIO_SYNC) PB10	62
8	PB11	<<< (GPIO) PB11	96
8	PB12	<<< (GPIO) PB12	101
8	PB13	<<< (MLB_DN) PB13	103
7	PB14	<<< (MLB_SN) PB14	105
7	PB15	<<< (MLB_CN / SIG) PB15	107
8	PC0	<<< (TDI) PC0	154
8	PC1	<<< (TDO) PC1	149
8	PC2	<<< (USB1_CLK) PC2	145
8	PC3	<<< (USB1_DIR) PC3	144
8	PC4	<<< (FR_A_TX_EN) PC4	159
8	PC5	<<< (FR_A_TX) PC5	158
8	PC6	<<< (LINI_TX) PC6	44
8	PC7	<<< (LINI_RX) PC7	45
8	PC8	<<< (RS232_TX) PC8	175
8	PC9	<<< (RS232_RX) PC9	2
8	PC10	<<< (CAN1_TX) PC10	36
8	PC11	<<< (CAN1_RX) PC11	35
8	PC12	<<< (FR_DBG0) PC12	173
8	PC13	<<< (FR_DBG1) PC13	174
8	PC14	<<< (FR_DBG2) PC14	3
8	PC15	<<< (FR_DBG3) PC15	4
8	PD0	<<< (HEX1 & GPIO) PD0	77
8	PD1	<<< (HEX2 & GPIO) PD1	78
8	PD2	<<< (HEX3 & GPIO) PD2	79
8	PD3	<<< (HEX4 & GPIO) PD3	80
8	PD4	<<< (GPIO) PD4	81
8	PD5	<<< (GPIO) PD5	82
8	PD6	<<< (GPIO) PD6	83
8	PD7	<<< (GPIO) PD7	84
8	PD8	<<< (GPIO) PD8	87
8	PD9	<<< (GPIO) PD9	94
8	PD10	<<< (GPIO) PD10	95
8	PD12	<<< (GPIO) PD12	100
6	PD13	<<< (GPIO & MLB_ST) PD13	102
7	PD14	<<< (MLB_DP) PD14	104
7	PD15	<<< (MLB_SF / DAT) PD15	106
8	MCU-RSTx	<<< MCU-RSTx	29
8	PORSTx	<<< PORSTx	153
6	MCU-XTAL	<<< MCU-XTAL	56
6	MCU-EXTAL	<<< MCU-EXTAL	58

U1A

MPC5748G 176QFP Package Iof3 GPIO Pins1

PE0	18	PE0	(MLB_I2C1_SCL)
PE1	20	PE1	(MLB_I2C1_SDA)
PE2	156	PE2	(FR_A_TX_EN)
PE3	157	PE3	(FR_A_RX)
PE4	160	PE4	(FR_B_TX)
PE5	161	PE5	(FR_B_RX)
PE6	167	PE6	(SD_CMD)
PE7	168	PE7	(SD_CLK)
PE8	21	PE8	(SAI_I2C2_SDA)
PE9	22	PE9	(SAI_I2C2_SCL)
PE10	23	PE10	(SAI_I2C3_SDA)
PE11	25	PE11	(SAI_I2C3_SCL)
PE12	133	PE12	(MII_CRS)
PE13	127	PE13	(MII_RXD3)
PE14	136	PE14	(USB1_D2)
PE15	137	PE15	(USB1_D3)
PF0	63	PF0	(SAIO_MCLK)
PF1	64	PF1	(SAIO_BCLK)
PF2	65	PF2	(SAIO_D3)
PF3	66	PF3	(SAIO_D2)
PF4	67	PF4	(SAIO_D1)
PF5	68	PF5	(SAIO_D0)
PF6	69	PF6	(SAI1_SYNC)
PF7	70	PF7	(SAI1_MCLK)
PF8	42	PF8	(GPIO)
PF9	41	PF9	(SW3 & GPIO) WKPU22
PF10	46	PF10	(CMP1_8 / IO)
PF11	47	PF11	(SW4 & GPIO) WKPU15
PF12	43	PF12	(GPIO)
PF13	49	PF13	(CMP1_11 / IO)
PF14	126	PF14	(RMI1_MDIO)
PF15	125	PF15	(RMI1_RXDV)
PG0	122	PG0	(RMI1_MDC)
PG1	121	PG1	(RMI1_TXCLK)
PG2	16	PG2	(LED1 & GPIO)
PG3	15	PG3	(LED2 & GPIO)
PG4	14	PG4	(LED3 & GPIO)
PG5	13	PG5	(LED4 & GPIO)
PG6	38	PG6	(CLKOUT0 GPIO)
PG7	37	PG7	(CLKOUT0 GPIO)
PG8	34	PG8	(GPIO)
PG9	33	PG9	(MLB_IRQ - WKPU21)
PG10	138	PG10	(USB1_D4)
PG11	139	PG11	(USB1_D5)
PG12	116	PG12	(MII_TXD2)
PG13	115	PG13	(MII_TXD3)
PG14	134	PG14	(USB1_D0)
PG15	135	PG15	(USB1_D1)
PH0	117	PH0	(RMI1_TXD1)
PH1	118	PH1	(RMI1_TXD0)
PH2	119	PH2	(RMI1_TXEN)
PH3	120	PH3	(eMIOS1_UC_5H)
PH4	162	PH4	(eMIOS1_UC_6H)
PH5	163	PH5	(eMIOS1_UC_7H)
PH6	164	PH6	(MLB_RST)
PH7	165	PH7	(MLB_PRR)
PH8	166	PH8	(SD_WP)
PH9	155	PH9	(TCK)
PH10	148	PH10	(TMS)
PH11	140	PH11	(USB1_D6)
PH12	141	PH12	(USB1_D7)
PH13	9	PH13	(GPIO)
PH14	10	PH14	(GPIO)
PH15	8	PH15	(GPIO)
		RESET	
		PORST	
		XTAL	
		EXTAL	



MPC5748G GPIO 2 of 2

Key to text colours:

- Purple - Comms Physical Interfaces
- Orange - Other Peripherals and I/O
- Blue - Debug (JTAG & Nexus)
- Black - Clock, Reset and Control
- RED - I/O Matrix and other functions (eg LED)
- Green - I/O Matrix (dedicated)

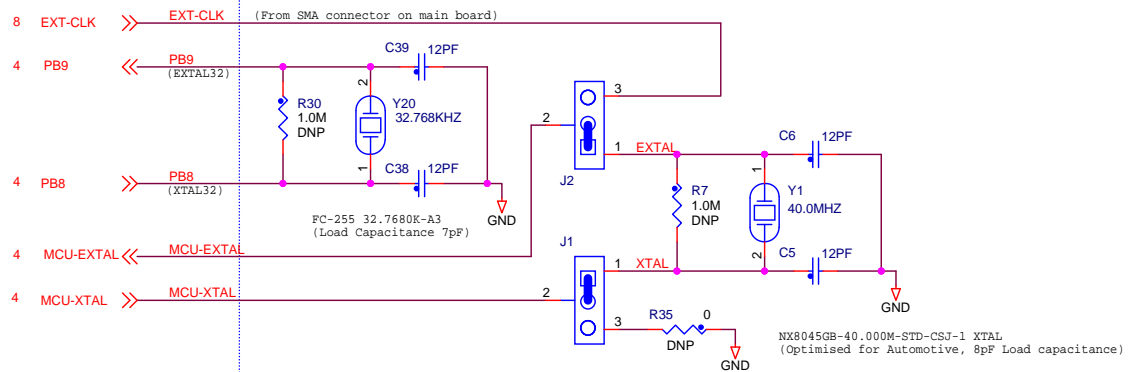
8	PI0	<<<	(SD_D3)	PI0	172	
8	PI1	<<<	(SD_D2)	PI1	171	
8	PI2	<<<	(SD_D1)	PI2	170	
8	PI3	<<<	(SD_D0)	PI3	169	
8	PI4	<<<	(USB1_STP)	PI4	143	
8	PI5	<<<	(USB1_NXT)	PI5	142	
8	PI6	<<<	(USB0_RST)	PI6	11	
8	PI7	<<<	(USB1_RST)	PI7	12	
7	PI8	<<<	(MLB_CP / CLK)	PI8	108	
			(GPIO)			
8	PI11	<<<	(ENET_RST)	PI11	111	
8	PI12	<<<	(GPIO & MLB_PS0)	PI12	112	PI11
8	PI13	<<<	(GPIO & MLB_PS1)	PI13	113	PI12
8	PI14	<<<	(SAI2_D0)	PI14	76	PI13
8	PI15	<<<	(SAI2_MCLK)	PI15	75	PI14
						PI15
8	PJ0	<<<	(SAI2_SYNC)	PJ0	74	
8	PJ1	<<<	(SAI2_BCLK)	PJ1	73	PJ0
8	PJ2	<<<	(SAI1_D0)	PJ2	72	PJ1
8	PJ3	<<<	(SAI1_BCLK)	PJ3	71	PJ2
8	PJ4	<<<	(GPIO)	PJ4	5	PJ3
						PJ4

U1C

MPC5748G 176QFP
 Package 3of3 GPIO Pins2



Oscillators and External Clock

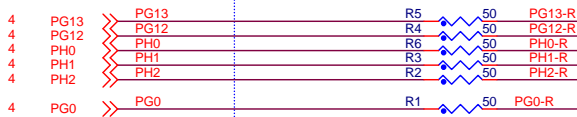




Speed Signal Termination

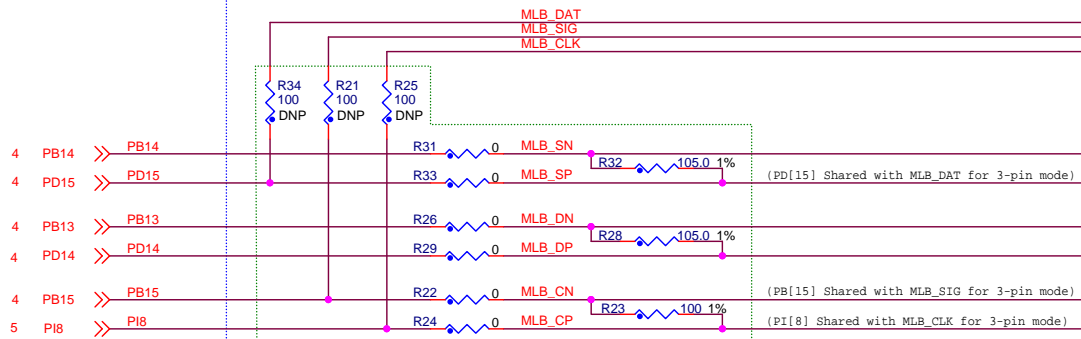
5 4 3 2

Ethernet Termination



Place resistors as close as possible to MCU

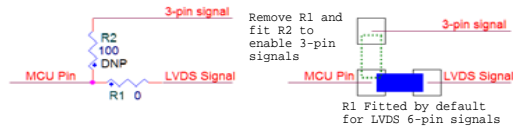
MLB Termination



Place resistors as close as possible to MCU

From MCU

Layout Note - Place resistors as shown with shared pad (as close to MCU as possible)



5 4 3 2



100 QFP DC



MPC5746C Customer EVB 100 BGA Daughter Card (MPC5746C)

Table Of Contents:	
Power - MPC5746C power pins footprint	Sheet 2
Power - MPC5746C Decoupling Capacitors	Sheet 3
GPIO - MPC5746C GPIO pins 1 of 2	Sheet 4
GPIO - MPC5746C GPIO pins 2 of 2	Sheet 5
Clocks	Sheet 6
Bus Termination	Sheet 7
Daughtercard Connectors	Sheet 8

Revision Information

Rev	Date	Designer	Comments
X1	05 Jan 2014	Alasdair Robertson	Initial release
X2	07 Jan 2014	Alasdair Robertson	Post review c
A	30 Jan 2014	Alasdair Robertson	Prototype bui
A1	18 Aug 2015	Alasdair Robertson	Tidy up Sche

Caution:

These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale MPC5746C family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points are denoted TPx
- Test point Vias are denoted TPVx

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in *ITALICS*



This document is for procurement or

Designer:
A. Robertson

Drawn by:
A. Robertson

Approved:
A. Robertson



MCU Power Connections

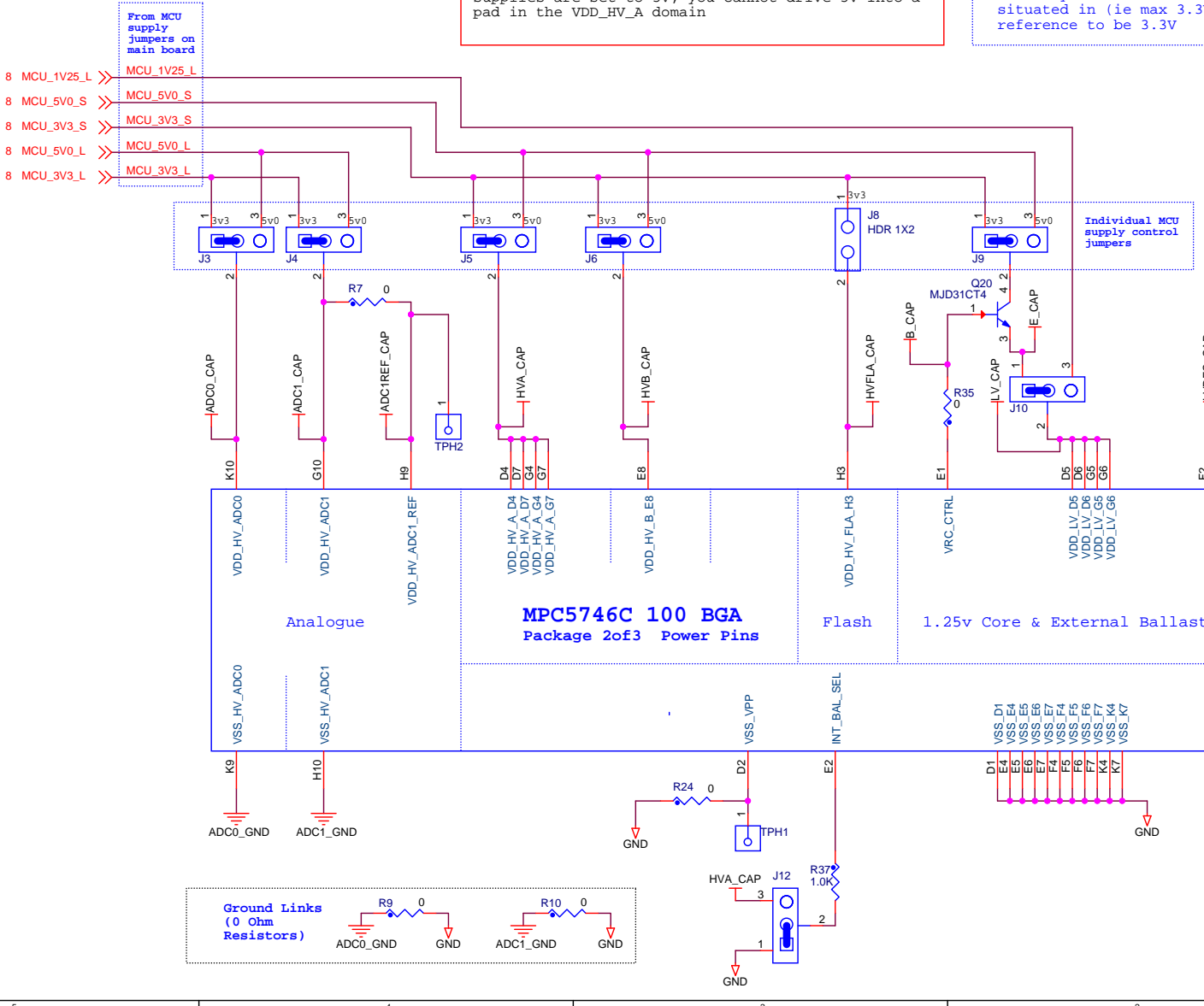
Caution:

- If VDD_HV_A is driven from 5V, the VDD_HV_FL A pin must not be supplied from 3.3V (remove the HVA_FL A jumper)
- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuraiton:

- ALL MCU supply voltage
- VDD_HV_B, VDD_HV_C, VBAI
- VDD_HV_FL A = External
- VDD_LV Supplied from K

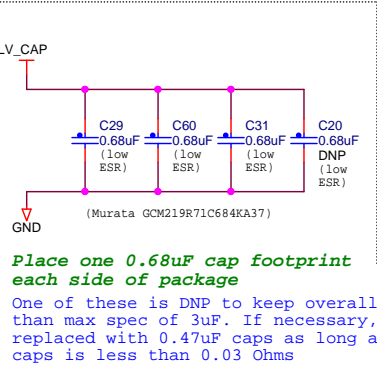
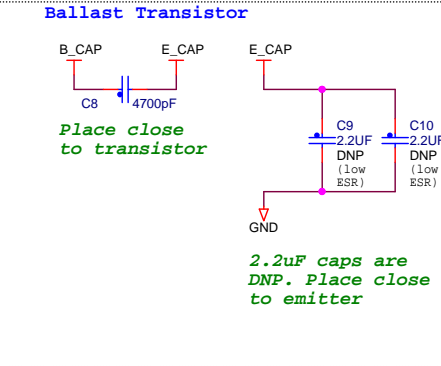
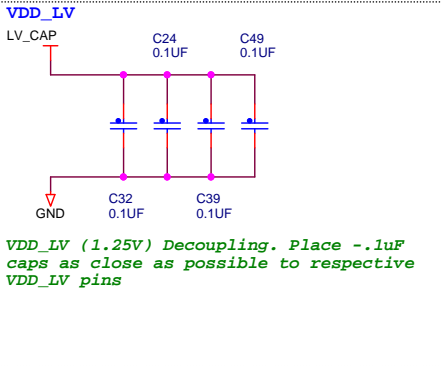
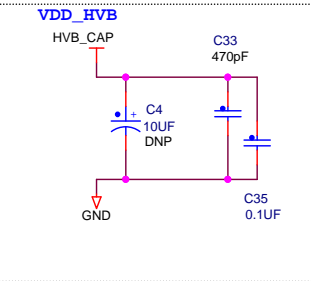
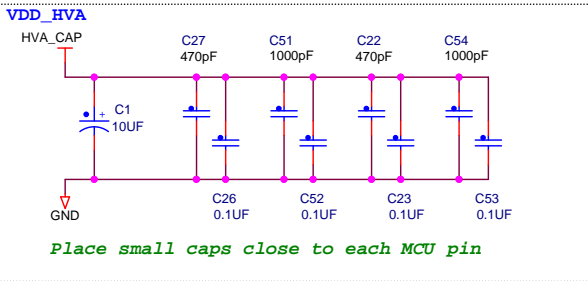
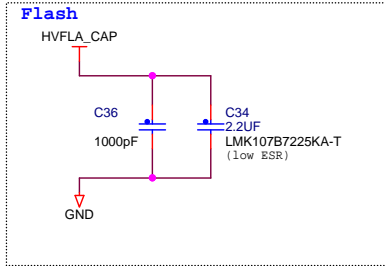
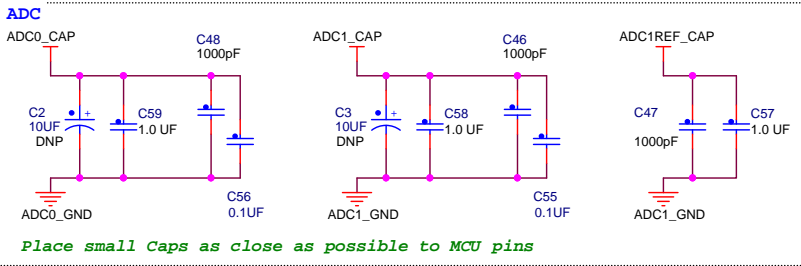
This is not necessarily VDD_HV_x domains have at 3.3V. Therefore the default can only be driven to the situated in (ie max 3.3V reference to be 3.3V





MCU Decoupling and bulk storage

Capacitance values:
 470pF
 1000pF
 4700pF
 0.01uF
 0.1uF
 0.68uF
 1.0uF
 2.2uF
 4.7uF
 10uF
 4.7uF
 7343-10



D
C
B
A



GPIO 1 of 2

** PA1 is also NMI. Routed to I/O Matrix (WKPU2 / NMIO) (WKPU3)

Key to text colours:	
Purple	- Comms Physical Interfaces
Orange	- Other Peripherals and I/O
Blue	- Debug (JTAG & Nexus)
Black	- Clock, Reset and Control
RED	- I/O Matrix and other functions (eg LED)
Green	- I/O Matrix (dedicated)

8	PA0	<< (SD_CD - WKPU19)	PA0	H4	PA0
8	PA1	<< (SW1 & GPIO**)	PA1	G3	PA1
8	PA2	<< (SW2 & GPIO)	PA2	F3	PA2
8	PA3	<< (MII_RXCLK)	PA3	C10	PA3
8	PA4	<< (CMP1_13 / IO)	PA4	J3	PA4
8	PA5	<< (SAI_GPIO)	PA5	A5	PA5
8	PA6	<< (MLB_GPIO)	PA6	B4	PA6
8	PA7	<< (MII_RXD2)	PA7	A10	PA7
8	PA8	<< (RMII_RXD1)	PA8	B10	PA8
8	PA9	<< (RMII_RXD0)	PA9	B9	PA9
8	PA10	<< (MII_COL)	PA10	B8	PA10
8	PA11	<< (RMII_RXER)	PA11	C8	PA11
8	PA12	<< (CMP1_15 / IO)	PA12	J7	PA12
8	PA13	<< (CMP1_14 / IO)	PA13	J6	PA13
8	PA14	<< (CMP1_12 / IO)	PA14	J5	PA14
8	PA15	<< (CMP1_10 / IO)	PA15	J4	PA15
8	PB0	<< (CAN0_TX)	PB0	H2	PB0
8	PB1	<< (CAN0_RX)	PB1	H1	PB1
8	PB10	<< (SAI0_SYNC)	PB10	K8	PB10
8	PC0	<< (TDI)	PC0	C5	PC0/TDI
8	PC1	<< (TDO)	PC1	C6	PC1/TDO
8	PC5	<< (FR_A_TX)	PC5	E3	PC5
8	PC10	<< (CAN1_TX)	PC10	G2	PC10
8	PC11	<< (CAN1_RX)	PC11	G1	PC11
8	PD1	<< (HEX2 & GPIO)	PD1	J10	PD1
8	PD13	<< (GPIO & MLB_ST)	PD13	G9	PD13
8	MCU-RSTx	<< MCU-RSTx	F1	RESET	
8	PORSTx	<< PORSTx	A4	PORST	
6	MCU-XTAL	<< MCU-XTAL	K5	XTAL	
6	MCU-EXTAL	<< MCU-EXTAL	K6	EXTAL	

U1A

MPC5746C 100 BGA Package 1 of 3 GPIO Pins1

PE2	C3	PE2	(FR_A_TX_EN)	>>>
PE3	D3	PE3	(FR_A_RX)	>>>
PE8	C2	PE8	(SAI_I2C2_SDA)	>>>
PE9	C1	PE9	(SAI_I2C2_SCL)	>>>
PE13	A9	PE13	(MII_RXD3)	>>>
PE15	A6	PE15	(USB1_D3)	>>>
PF0	J8	PF0	(SAI0_MCLK)	>>>
PF5	G8	PF5	(SAI0_D0)	>>>
PF8	J2	PF8	(GPIO)	>>>
PF9	J1	PF9	(SW3 & GPIO) WKPU22	>>>
PF10	K1	PF10	(CMP1_8 / IO)	>>>
PF14	D9	PF14	(RMII_MDIO)	>>>
PF15	A8	PF15	(RMII_RXDV)	>>>
PG0	F9	PG0	(RMII_MDC)	>>>
PG1	F10	PG1	(RMII_TXCLK)	>>>
PG2	B1	PG2	(LED1 & GPIO)	>>>
PG3	B2	PG3	(LED2 & GPIO)	>>>
PG6	H6	PG6	(CLKOUT1 GPIO)	>>>
PG7	H5	PG7	(CLKOUT0 GPIO)	>>>
PG11	B6	PG11	(USB1_D5)	>>>
PG12	D10	PG12	(MII_TXD2)	>>>
PG13	D8	PG13	(MII_TXD3)	>>>
PG14	A7	PG14	(USB1_D0)	>>>
PG15	B7	PG15	(USB1_D1)	>>>
PH0	E10	PH0	(RMII_TXD1)	>>>
PH1	E9	PH1	(RMII_TXD0)	>>>
PH2	C9	PH2	(RMII_TXEN)	>>>
TCK/PH9	C4	PH9	(TCK)	>>>
TMS/PH10	C7	PH10	(TMS)	>>>
PH12	B5	PH12	(USB1_D7)	>>>

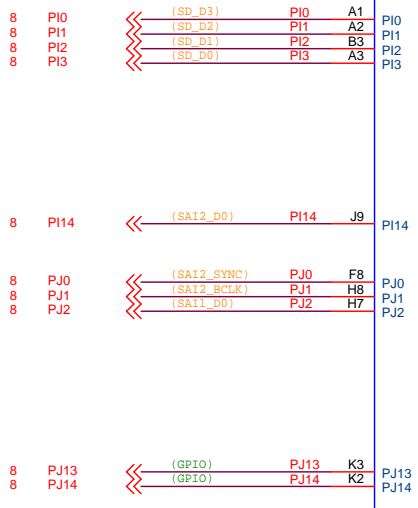
SKT BGA 100 TH + MPC574XG-100



GPIO 2 of 2

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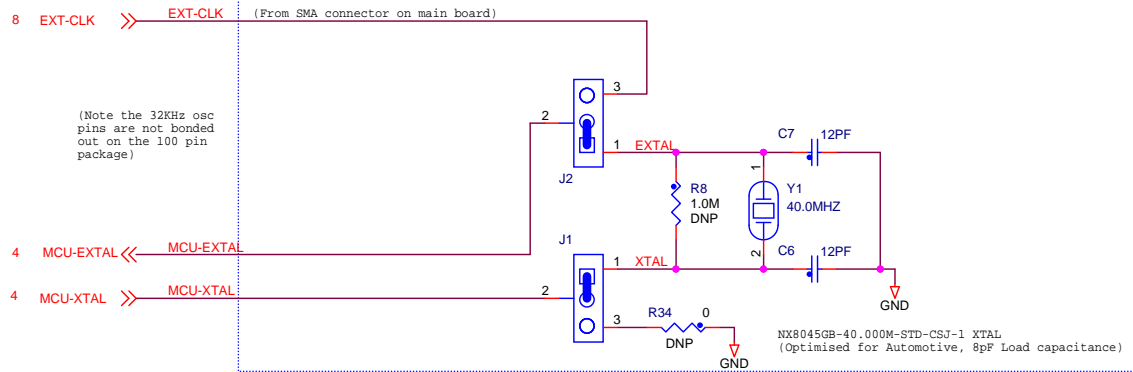
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SKT BGA 100 TH + MPC574XG-100

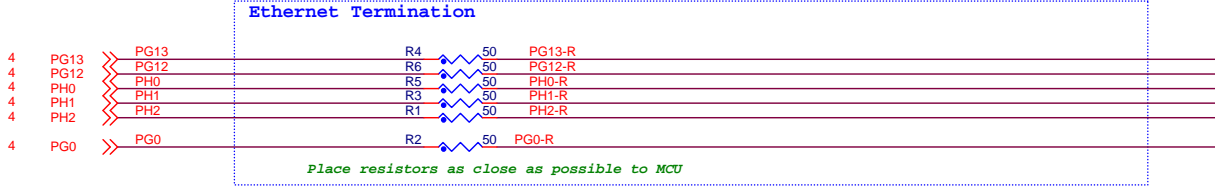


Oscillators and External Clock





Speed Signal Termination



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