

# MPC5777C EVB User Guide

## Prototype Board

by: NXP Semiconductors

### 1. Introduction

This user guide details the setup and configuration of the NXP MPC5777C Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the MPC57xx family of microprocessors, and to facilitate hardware and software development.

At the time of writing this document, the MPC57xx family consists of the 55nm powertrain and safety devices. For the latest product information, please speak to your NXP representative or consult the MPC57xx website at [www.nxp.com](http://www.nxp.com)

The EVB is intended for bench or laboratory use and has been designed using normal temperature specified components (+70°C).

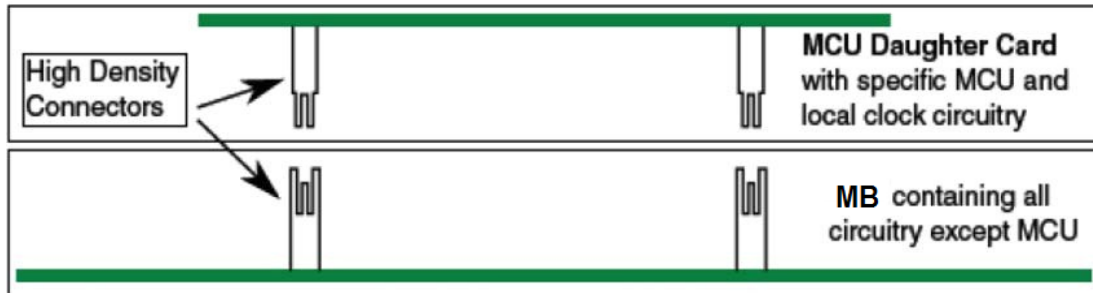
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## 1.1 Modular Concept

For maximum flexibility and simplicity, the EVB has been designed as a modular development platform. The EVB main board does not contain an MCU. Instead, the MCU is fitted to an MCU daughter card (occasionally referred to as an adapter board). This approach means that the same EVB platform can be used for multiple packages and MCU derivatives within the MPC57xx family. High density connectors provide the interface between the EVB and MCU daughter cards as shown [Figure 1](#) See [Section 4&5, “Configuration — MPC5777C-516DS Daughter card”](#) for more details on the daughter cards and [Section 6, “Board Interface Connector”](#) for more details on the interface connectors.



**Figure 1: Modular concept – Mother Board (MB) and MCU daughter card**

Please consult the MPC57xx website at [www.nxp.com](http://www.nxp.com) or speak to your NXP representative for more details on the availability of MCU daughter cards.

The EVB is designed to be used with the motherboard and standalone configurations

### NOTE

For details on your specific daughter card, please consult the instructions included with the daughter card.

## 1.2 Daughter Card Availability

A number of compatible daughter cards are available for the motherboard across a number of devices. [Table 1](#) gives an overview of daughter cards that can be used with MPC57xx motherboard (Part Number: MPC57XXXMB) and associated MPC5777C devices, package sizes and part numbers.

**Table 1: Daughter Card Overview**

Daughter card number	Device	Package	Socket	Nexus
MPC5777C-416DS	MPC5777C	416 BGA	Yes	Yes
MPC5777C-516DS	MPC5777C	516 BGA	Yes	Yes

All daughter cards will be similar in design and concept. For details on the daughter cards please refer to [Section 4&5, “Configuration — MPC5777C-416DS Daughter card, Configuration — MPC5777C-516DS Daughter card”](#).

## 2. EVB features

The EVB system consists of a motherboard and a daughter card, both with distinct features.

The Mother Board provides the following key features:

- Support provided for different MPC57xx MCUs by utilizing MCU daughter cards
- Single 12 V external power supply input with four on-board regulators providing all of the necessary EVB and MCU voltages; power supplied to the EVB via a 2.1mm barrel style power jack or a 2-way level connector; 12 V operation allows in-car use if desired
- Master power switch and regulator status LEDs
- Two 240-way high-density daughter card expansion connectors allowing connection of the MCU daughter card or a custom board for additional application specific circuitry
- All MCU signals readily accessible at a port-ordered group of 0.1inch pitch headers
- RS232/SCI physical interface and standard DB9 connector
- LINFlexD interface , Ethernet interface
- 2 CAN interfaces, one configurable to be connected to one out of two CAN modules, and one connected to a dedicated third CAN module
- Variable resistor, driving between 5 V and ground
- 4 user switches and 4 user LEDs, freely connectable
- Liberal scattering of GND test points (surface mount loops) placed throughout the EVB

\*\*Mother Board has FlexRAY connector, but this feature is not used on MPC5777C

The daughter cards provide the following features:

- MCU (soldered or through a socket)
- 40MHz onboard clock oscillator circuit in EVB for MCU Clocking
- User reset switch with reset status LEDs and Power Indication LEDs
- Standard 14-pin JTAG debug connector and 50-pin SAMTEC Nexus connector
- USB (Type B) / UART transceiver to interface with MCU
- Liberal scattering of ground and test points (surface mount loops) placed throughout the EVB
- Power SBC for standalone function of Daughter Card
- 1 CAN and 1 LIN connector supported by Power SBC

#### **NOTE**

To alleviate confusion between jumpers and headers, all EVB jumpers are implemented as 2 mm pitch whereas headers are 0.1in. (2.54 mm). This prevents inadvertently fitting a jumper to a header.

#### **CAUTION**

Before the EVB is used or power is applied, please fully read the following sections on how to correctly configure the board. Failure to correctly configure the board may cause irreparable component, MCU or EVB damage.

### **3. Configuration — Motherboard**

This section details the configuration of each of the Mother Board functional blocks.

The Mother Board has been designed with ease of use in mind and has been segmented into functional blocks as shown in Figure 2. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

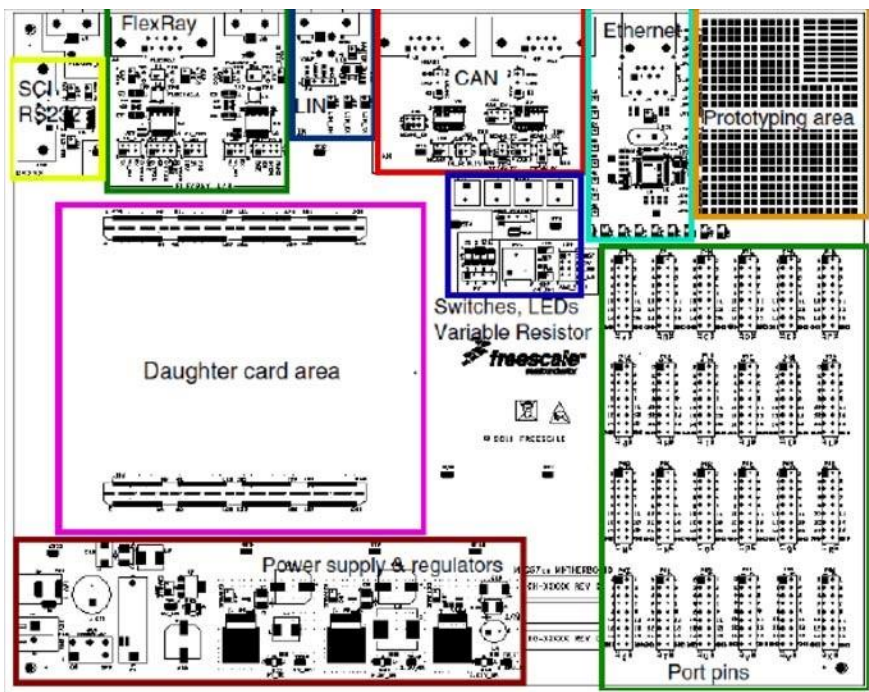


Figure 2: Mother Board - Functional Blocks

### 3.1 Power Supply Configuration

The EVB requires an external power supply voltage of 12 V DC, minimum 1 A. This allows the EVB to be easily used in a vehicle if required. The single input voltage is regulated on-board using three switching regulators to provide the necessary EVB and MCU operating voltages of 5.0 V, 3.3 V, 1.25 V and one 5 V linear regulator for the ADC supplies and references.

For flexibility there are two different power supply input connectors on the motherboard as detailed below. There is also a power supply option on the daughter card to use the daughter card in standalone mode. Please refer to Section 4.1.2, 4.1.3 “Daughter Card Standalone Power Input -External & Daughter Card Standalone Power Input –Power SBC” for details on the daughter card power input.

### 3.1.1 Motherboard Power Supply Connectors

#### 2.1 mm Barrel Connector – P26:



Figure 3: 2.1 mm Power Connector

#### 2-Way Lever Connector – P33:

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarization of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

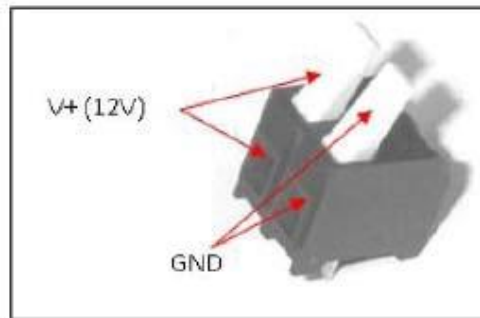


Figure 4: Lever Power Connector

### 3.1.2 Regulator Power Jumpers

There are four power regulator circuits on the MPC57xx motherboard that supply the required voltages to operate the MCUs:

- 5V\_SR: 5 V switching regulator to supply the power management controller, I/O and peripherals
- 3.3V\_SR: 3.3 V switching regulator for Ethernet, debug and I/O
- 5V\_LR: 5 V linear regulator for ADC supply and reference

All of the regulators have the option of being disabled/ enabled if they are not required. By default (jumpers are off), all of the switching regulators are enabled and the 5 V linear regulator is disabled. The regulators can be enabled individually by the following jumper settings:

- Connecting J57 enables the 5 V linear regulator
- Disconnecting J58 enables the 5 V switching regulator
- Disconnecting J59 enables the 3.3 V switching regulator
- Disconnecting J60 enables the 1.25 V switching regulator

The regulators supply power to the daughter cards through the board connector. The individual selection and configuration of the MCU supplies are done on the daughter cards.

**NOTE**

Not all the supported daughter card MCUs require all the supplies to be switched on. Please refer to [Section 4 “Configuration — MPC5777C-416DS Daughter card”](#) for details.

**3.1.3 Power Switch, Status LEDs and Fuse**

The main power switch (slide switch SW5) can be used to isolate the power supply input from the EVB Voltage regulators if required.

- Moving the slide switch to the right (away from connector P33) will turn the EVB on
- Moving the slide switch to the left (towards connector P33) will turn the EVB off

When power is applied to the EVB, four green power LEDs adjacent to the voltage regulators show the presence of the supply voltages as follows:

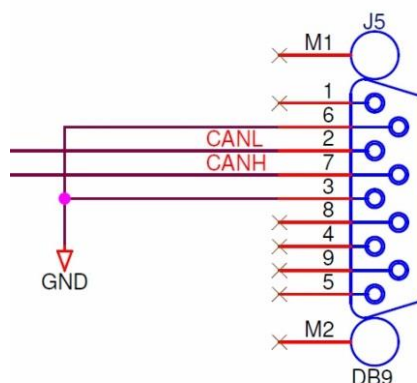
- LED D9 – Indicates that the 5.0 V linear regulator is enabled and working correctly
- LED D11 – Indicates that the 5.0 V switching regulator is enabled and working correctly
- LED D12 – Indicates that the 3.3 V switching regulator is enabled and working correctly
- LED D13 – Indicates that the 1.25 V switching regulator is enabled and working correctly

If no LED is illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch SW5 is in the “OFF” position or that the fuse F1 has blown. The fuse will blow if power is applied to the EVB in reverse-bias, where a protection diode ensures that the main fuse blows rather than causing damage to the EVB circuitry. If the fuse has blown, check the bias of your power supply connection then replace fuse F1 with a 20mm 1.5A fast blow fuse.

**3.2 CAN Configuration**

The EVB has two NXP TJA1041T high speed CAN transceivers and two standard DB9 connectors to provide physical CAN interfaces for the MCU.

The pinout of the DB9 connectors (J5/J6) is shown in [Figure 5](#).



**Figure 5: CAN DB9 connector Pin out**

For flexibility, the CAN transceiver I/Os are also connected to two standard 0.1 in. connectors (P4 and P5) at the top side of the PCB. The pin-out for these connectors is shown in Figure 6.

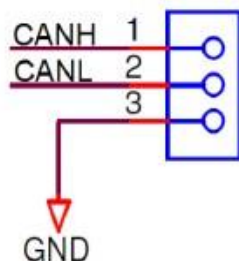


Figure 6: CAN 3pin header interface connector

By default the CAN interfaces are not enabled. To enable the CAN interfaces the jumpers detailed in Table 2 need to be placed,

Table 2: CAN control jumpers

Jumper	Label	Description
J23	CAN2_EN	PHY U2 configuration 1-2: WAKE to GND 3-4: STB to 5V 5-6: EN to 5V
J32	CAN2	1-2: PHY TX to MCU 3-4: PHY RX to MCU
J33	CAN-PWR	1-2: 5.0V_SR to PHY U2 VCC 3-4: 12V to PHY U2 VBAT
J34	—	PHY U2 signal out 1: ERR 2: INH
J21	CAN_EN	PHY U1 configuration 1-2: WAKE to GND 3-4: STB to 5V 5-6: EN to 5V
J35	CAN	1-2: PHY TX to J37-2 3-4: PHY RX to J38-2
J37	CAN	PHY U1 TX to MCU 1-2: MCAN1 TX 2-3: TTCAN TX
J38	—	PHY U1 RX to MCU 1-2: MCAN1 RX 2-3: TTCAN RX
J36	—	PHY U1 signal out 1: ERR 2: INH

### 3.3 RS232 Configuration

DB9 connector J19 and TR3221 RS232 transceiver device provide a physical RS232 interface, allowing a direct RS232 connection to a PC or terminal.

The pin-out of these connectors is detailed in [Figure 7](#) Note that hardware flow control is not supported on this implementation.

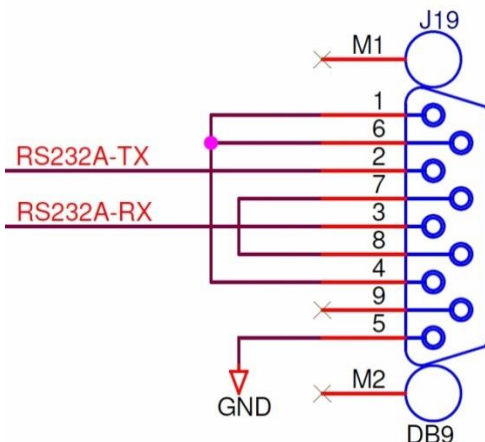


Figure 7: RS232 physical interface connector

On default the RS232 interface is not enabled. To enable the RS232 interface the user needs to place the jumpers detailed in [Table 3](#).

Table 3: RS232 control jumpers

Jumper	Label	Description
J13	SCI TX	TX enable
J14	SCI RX	RX enable
J25	SCI_PWR	Transceiver power on

### 3.4 LIN Configuration

The EVB is fitted with a NXP MC33662LEF LIN transceiver (U50) and two different style connectors: A standard LIN Molex connector (J4) at the edge of the board and a standard 0.1 in. connector (P3).

The pin-out of the Molex connector J4 is shown in [Figure 8](#).



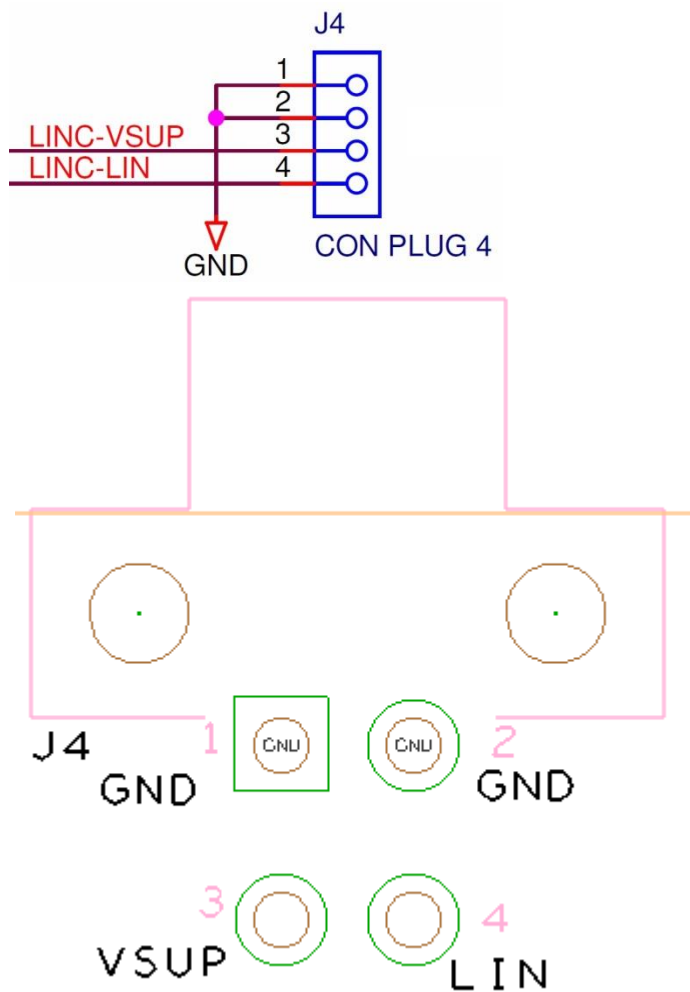


Figure 8: LIN Molex connector

For flexibility, the LIN transceiver is also connected to a standard 0.1 in. connector (P3) at the top side of the PCB as shown in Figure 9. For ease of use, the 12 V EVB supply is fed to pin1 of P3 and the LIN transceiver power input to pin2. This allows the LIN transceiver to be powered directly from the EVB supply by simply linking pins 1 and 2 of connector P3 using a 0.1 in. jumper shunt.

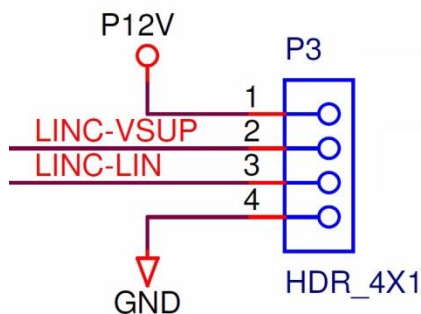


Figure 9: LIN 4pin header interface connector

By default the LIN interface is not enabled. To enable the LIN interface the jumpers detailed in [Table 4](#) need to be placed.

**Table 4: LIN control Jumpers**

Jumper	Label	Description
J15	LIN_EN	LIN PHY (U50) enable
J16	LIN_RX	LIN RX enable
J17	LIN_TX	LIN TX enable

### 3.5 Ethernet Configuration

The EVB is fitted with a standard RJ45 Ethernet connector (J7) and a DP83848C 10/100 Ethernet transceiver (U6).

By default, the Ethernet interface is enabled. The Ethernet interface the jumpers are detailed in

[Table 5](#).

**Table 5: Ethernet control jumpers**

Jumpe	Description
J22	PHY power(3.3V_SR) on (jumper placed on default)
J18	RXCLK
J20	CRS_LEDCFG
J24	RXER_MDIXEN
J26	RXDV_MIIMODE
J39	RXD0_PHYAD1
J40	RXD1_PHYAD1
J41	RXD2_PHYAD2
J42	RXD3_PHYAD3
J44	COL_PHYAD0
J45	TXEN
J46	TXCLK
J47	TXD0
J48	TXD1
J49	TXD2
J50	TXD3_SNIMODE
J51	MDC
J52	MDIO

### 3.6 User Area

There is a rectangular prototype area on the EVB top right corner, consisting of a 0.1in. pitch array of through-hole plated pads. Power from all the three switching regulators is readily accessible along with GND through JP1 – JP16 next to the prototyping area. This area is ideal for the addition of any custom circuitry.

## Configuration—Motherboard

There are four active low user LEDs D2, D3, D4 and D5, these are driven by connecting a logic 0 signal to the corresponding pin on 0.1in. header P7 (USER LEDS). The LED inputs are pulled to VDD\_HV\_IO\_MAIN through 10 k $\Omega$  resistors.

There are 4 active high pushbutton switches SW1, SW2, SW3 and SW4 which will drive 5V onto the respective pins on 0.1in. Connector P6 when pressed. The switch outputs are pulled to GND via 10 k $\Omega$ .

Potentiometer RV1 can be connected to port pin PB[0] via J53 and is adjustable between GND and 5 V from the linear regulator. Power from all regulators can be connected to port pins as through J54:

- 1-2: 1.25V\_SR to PB[1]
- 3-4: 3.3V\_SR to PB[2]
- 5-6: 5.0V\_SR\_SR to PB[3]
- 7-8: 5V\_LR to PB[4]

The P12V rail from the 12 V input is scaled to 4.3V through the voltage divider of R81 and R82 and the scaled voltage can be connected to PB[5] via J55.

### 3.7 Test points — Motherboard

A number of test points of different shape and functionality is scattered around the EVB to allow easy access to MCU and reference signals. This chapter summarizes and describes the available test points. Motherboard test points are listed and detailed in [Table 6](#).

**Table 6: Test Points- Mother Board**

Signal	TP name	Shape	Description
GND	GT1	Hook	Ground reference
GND	GT2	Hook	Ground reference
GND	GT3	Hook	Ground reference
GND	GT4	Hook	Ground reference
GND	GT5	Hook	Ground reference
GND	GT6	Hook	Ground reference
GND	GT7	Hook	Ground reference
GND	GT8	Hook	Ground reference
GND	GT9	Hook	Ground reference
GND	GT10	Hook	Ground reference
GND	GT11	Hook	Ground reference
1.25V_SR	JP1	Pin	1.25V_SR reference

## Configuration—Motherboard

Signal	TP name	Shape	Description
1.25V_SR	JP2	Pin	1.25V_SR reference
1.25V_SR	JP3	Pin	1.25V_SR reference
1.25V_SR	JP4	Pin	1.25V_SR reference
3.3V_SR	JP5	Pin	3.3V_SR reference
3.3V_SR	JP6	Pin	3.3V_SR reference
3.3V_SR	JP7	Pin	3.3V_SR reference
3.3V_SR	JP8	Pin	3.3V_SR reference
5V_SR	JP9	Pin	5V_SR reference
5V_SR	JP10	Pin	5V_SR reference
5V_SR	JP11	Pin	5V_SR reference
5V_SR	JP12	Pin	5V_SR reference
GND	JP13	Pin	Ground reference
GND	JP14	Pin	Ground reference
GND	JP15	Pin	Ground reference
GND	JP16	Pin	Ground reference
5V_SR	TP15	Hook	5V_SR reference
5V_LR	TP14	Hook	5V_LR reference
3.3V_SR	TP16	Hook	3.3V_SR reference
1.25V_SR	TP17	Hook	1.25V_SR reference
FRA-INH2	TP5	Pad	Unused
FRA-INH1	TP1	Pad	Unused
FRA-ERRN	TP2	Pad	Unused
FRA-RXEN	TP6	Pad	Unused
FRB-INH2	TP7	Pad	Unused

## Configuration—Motherboard

Signal	TP name	Shape	Description
FRB-INH1	TP3	Pad	Unused
FRB-ERRN	TP4	Pad	Unused
FRB-RXEN	TP8	Pad	Unused
FR_DBG0	TP10	Pad	Unused
FR_DBG1	TP11	Pad	Unused
FR_DBG2	TP12	Pad	Unused
FR_DBG3	TP13	Pad	Unused
FEC 25MHz	TP9	Pad	Ethernet clock

## 4. Configuration — MPC5777C-416DS Daughter card

This section details the configuration of each of the **MPC5777C-416DS** daughter card's functional blocks.

The daughter card has been designed with ease of use in mind and has been segmented into functional blocks as shown in [Figure 10](#). Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

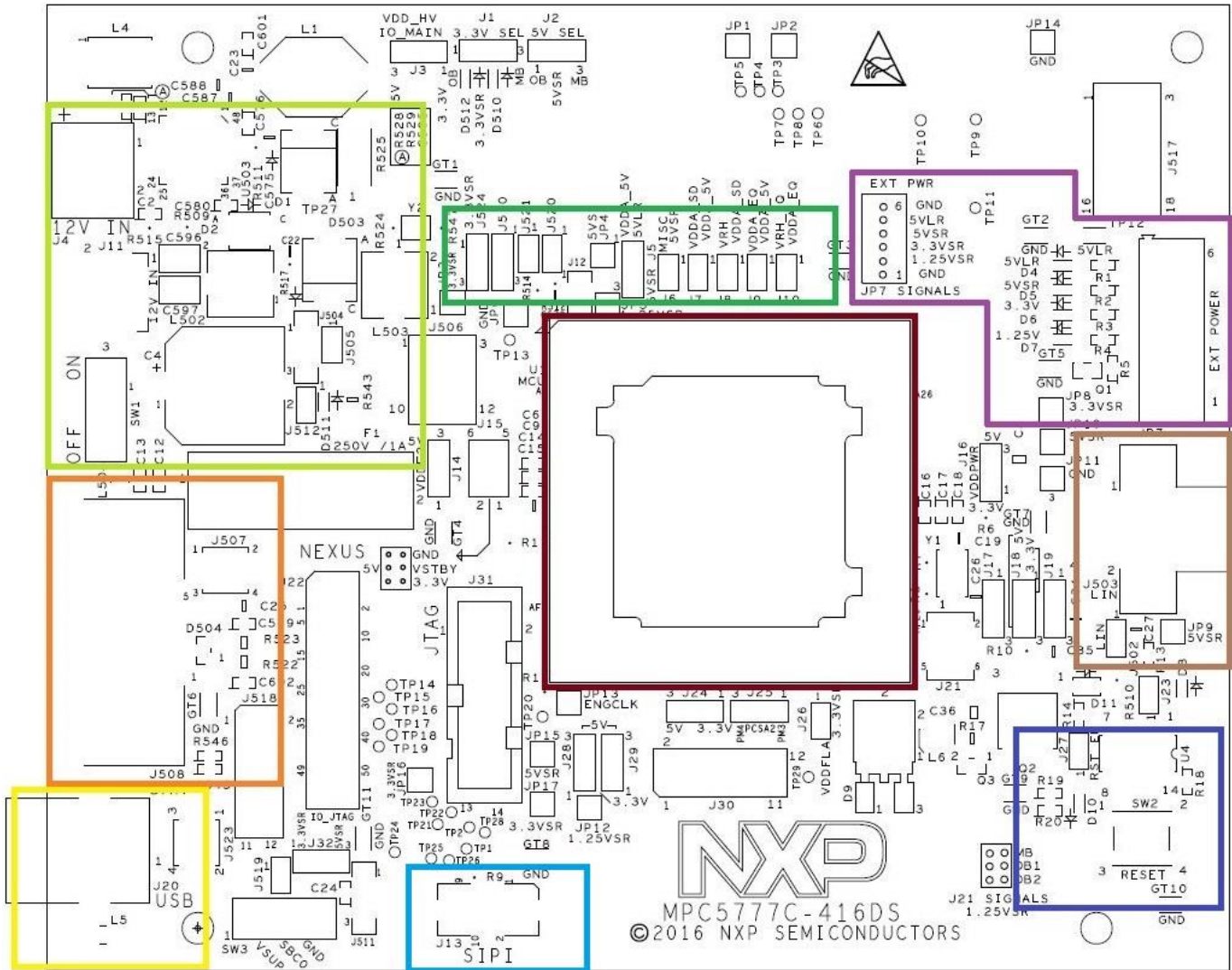


Figure 10: MPC5777C-416DS Daughter card — functional blocks

## 4.1 MCU Power

### 4.1.1 Supply Routing and Jumpers

The different MCU supplies are connected to the regulators on the Mother Board through the interface connector. Also daughter card has option to connect MCU supplies to either Mother Board supplies or onboard regulators. Figure 11 shows how the MCU power domains are connected to the regulators.

## Board Interface Connector

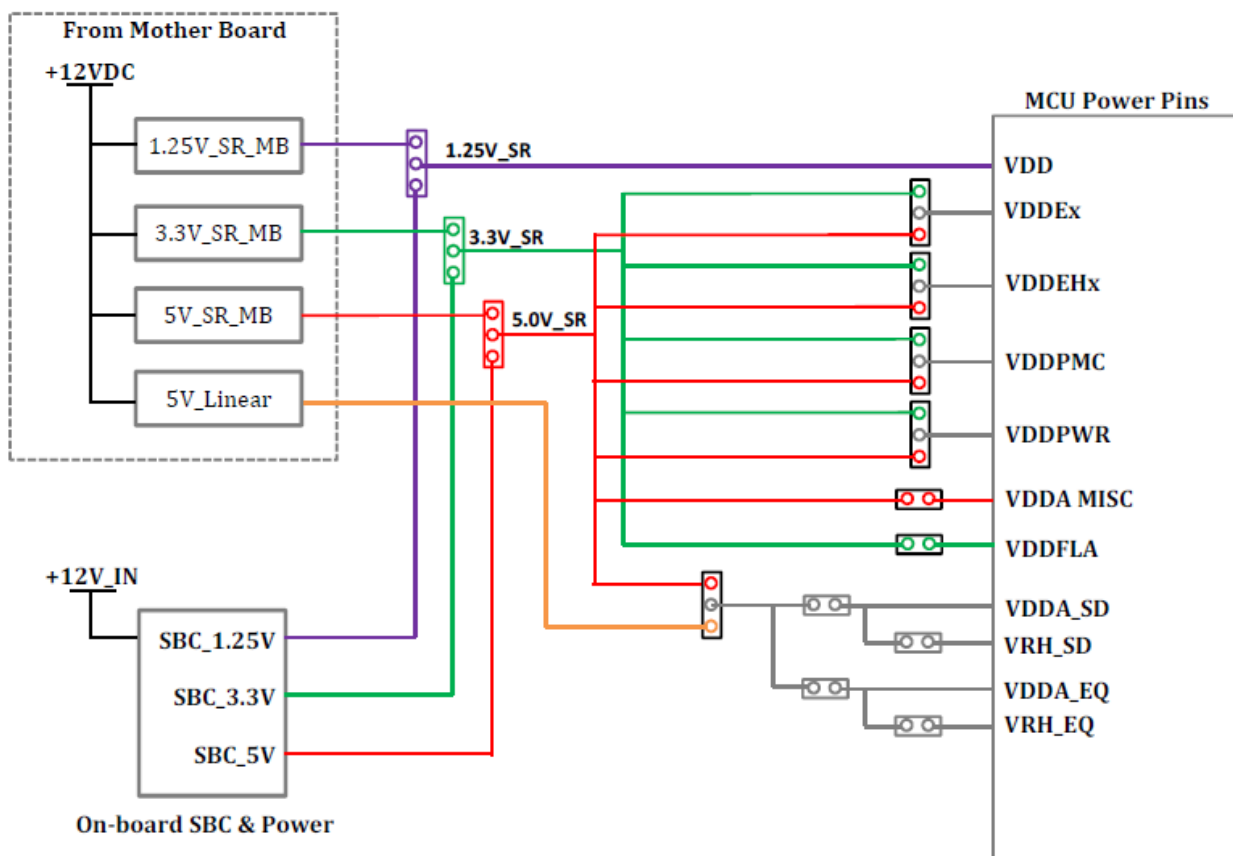


Figure 11: Daughter card power distribution

Available power supply modes of MPC577C are listed in [Table 7](#)

Table 7: Power modes of MPC5777C

Configuration	Mode Name	3.3V Flash Supply	1.2V Regulator controller	REGSEL	VDDFLA	VDDPMC&V DDPWR
Internal 3.3V Flash regulator with 1.2V linear regulator controller	LDO5V	Internal Regulator	Internal Linear Mode	Low/GND	Bypass caps	External 5V supply
Internal 3.3V regulator with 1.2V SMPS regulator controller	SMPS5V	Internal Regulator	Internal SMPS	High/5V	Bypass caps	External 5V supply
External 3.3V regulator with internal 1.2V linear regulator controller	LDO3V	External	Internal Linear Mode	Low/GND	External 3.3V supply	External 3.3V supply
External 3.3V regulator with internal 1.2V SMPS regulator controller	SMPS3V	External	Internal SMPS	High/3.3V	External 3.3V supply	External 3.3V supply
External supplies with on-chip low voltage detect	External	External	External Supply	Low/GND	External 3.3V supply	External 3.3V supply
External supplies, except flash powered by internal regulator	External	Internal Regulator	External Supply	Low/GND	Bypass caps	External 5V supply

Jumper options to achieve the above power supply modes are shown in [Table 8](#):

**Table 8: Jumper options for various power modes**

Mode name	J17 (REGSEL_TO_GND)	J26 (VDDFLA_SEL)	J16 (VDDPWR_SEL)	J18 (VDDPMC_SEL)	J19 (REGCTL_SEL)	J21 (1V25_SR_MB_SEL) and J12 (SBC_1V25) <sup>1</sup>
LDO5V	2&3 -GND	OPEN - Bypass caps	2&3 - 5V_SR	2&3 - 5V_SR	2&3 for LV Linear Regulator	J21 - 3&4 for 1.25V_SR_OB1 (LR) J12 - Open
SMPS5V	1&2 - HIGH - 5V	OPEN - Bypass caps	2&3 - 5V_SR	2&3 - 5V_SR	1&2 for LV SPMS	J21 - 5&6 for 1.25V_SR_OB2(SR) J12 - Open
LDO3V	2&3 -GND	CLOSED - VDDPWR& VDDPMC	1&2 - 3V3_SR	1&2 - 3V3_SR	2&3 for LV Linear Regulator	J21 - 3&4 for 1.25V_SR_OB1 (LR) J12 - Open
SMPS3V	1&2 - HIGH - 3V3	CLOSED - VDDPWR& VDDPMC	1&2 - 3V3_SR	1&2 - 3V3_SR	1&2 for LV SPMS	J21 - 5&6 for 1.25V_SR_OB2(SR) J12 - Open
External	2&3 -GND	CLOSED - VDDPWR& VDDPMC	1&2 - 3V3_SR	1&2 - 3V3_SR	N/C	J21 - 1&2 for 1.25V_SR_MB -OR- J12-1&2 for SBC_1V25
External	2&3 -GND	OPEN - Bypass caps	2&3 - 5V_SR	2&3 - 5V_SR	N/C	J21 - 1&2 for 1.25V_SR_MB -OR- J12-1&2 for SBC_1V25

The connection of any power domain to a regulator has to be enabled by a dedicated jumper as described in [Table 9](#).

**Table 9: MCU power selection jumpers (416DC)**

Jumper	Description	Jumper Setting (* - Default)
J1	3.3V Selection	1-2: 3.3V from onboard Power SBC 2-3: 3.3V from Mother Board*
J2	5V Selection	1-2: 5V from onboard Power SBC 2-3: 5V from Mother Board*
J3	IO Levels in the Mother Board - VDD_HV_IO_MAIN	1-2: Select 3.3V 2-3: Select 5V*
J5	ADC Analog Supply Selection	1-2: Select 5V from Linear Regulator* 2-3: Select 5V from Switching Regulator
J6	Connect TRNG, Internal RC oscillator Supply - VDDA_MISC	1-2: Connect VDDA_MISC to 5V_SR*
J7 & J8	Connect SD ADC supply & Reference -VDDA_SD, VRH_SD	J7, 1-2: Connect VDDA_SD* J8, 1-2: Connect VRH_SD*
J9 & J10	Connect eQADC supply & Reference - VDDA_EQ, VRH_EQ	J9, 1-2: Connect VDDA_EQ* J10, 1-2: Connect VRH_EQ*

<sup>1</sup>**CAUTION:** For 1.25 V source selection, a single jumper must be installed on either J21 or J12, but not on both at a time.



## Board Interface Connector

Jumper	Description	Jumper Setting (* - Default)
J14	Fast I/O Pads supply selection - VDDE2	1-2: Select 3.3V* 2-3: Select 5V
J15	RAM Standby supply selection -VSTBY	1-3: Select 3.3V 5-3: Select GND* 4-3: Select 5V
J16	SMPS Driver Supply Selection - VDDPWR	1-2: Select 3.3V 2-3: Select 5V*
J17	Core Supply generation, Regulation Mode - REGSEL	1-2: Select SMPS Configuration (VDD_PMC) 2-3: Select Linear Configuration (GND)*
J18	PMC Supply Selection – VDDPMC	1-2: Select 3.3V 2-3: Select 5V*
J19	Core Supply generation, Regulator Control -REGCTL	1-2: Select SMPS to derive (1.25V_SR_OB2) 2-3: Select Linear to derive (1.25V_SR_OB1)*
J21	VDD Core Supply Selection	1-2: 1.25V from Mother Board* 3-4: 1.25V onboard Regulator (Linear Mode) 5-6: 1.25V onboard Regulator (Switching Mode)
J12	VDD Core Supply Selection	1-2: 1.25V from onboard Power SBC
J24	Medium I/O Pads supply selection – VDDEH3A	1-2: Select 3.3V 2-3: Select 5V*
J26	Connect Flash Core Supply - VDDFLA	1-2: Connect VDDFLA to 3.3V_SR
J28	Fast I/O Pads supply selection - VDDE2A	1-2: Select 3.3V* 2-3: Select 5V
J29	Medium I/O Pads supply selection - VDDEHx	1-2: Select 3.3V 2-3: Select 5V*
J30	Medium I/O Pads supply enable – VDDEHx	1-2: Connect VDDEH1* 3-4: Connect VDDEH3* 5-6: Connect VDDEH4* 7-8: Connect VDDEH5* 9-10: Connect VDDEH6* 11-12: Connect VDDEH7* All jumpers in J30 placed by Default
J32	JTAG IO Level - VDD_HV_IO_JTAG	1-2: Select 3.3V* 2-3: Select 5V
J520	Connect LED for ETPUA0	1-2: Connect LED with Signal ETPUA0*
J521	Connect LED for ETPUA1	1-2: Connect LED with Signal ETPUA1*

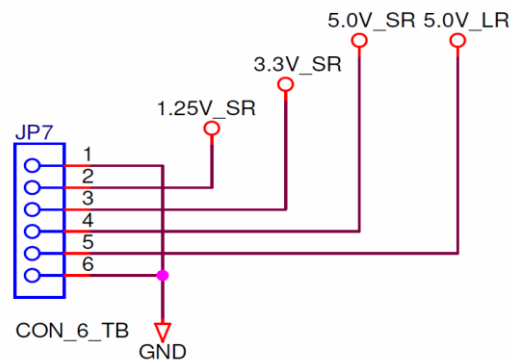
### 4.1.2 Daughter Card Standalone Power Input -External

A terminal power input is provided on the daughter card to enable use of the daughter card without the motherboard.

When power is applied to the Daughter Card from Motherboard or External Terminal input or PowerSBC with respective jumper selection, four green power LEDs adjacent to the terminal power input connector (JP7) show the presence of the supply voltages as follows:

- LED D4 – Indicates that the 5.0 V linear regulator is enabled and working correctly
- LED D5 – Indicates that the 5.0 V switching regulator is enabled and working correctly
- LED D6 – Indicates that the 3.3 V switching regulator is enabled and working correctly
- LED D7 – Indicates that the 1.25 V switching regulator is enabled and working correctly

The connections of the JP7 power terminal are detailed in [Figure 12](#).



**Figure 12: Terminal power input connections**

### 4.1.3 Daughter Card Standalone Power Input -Power SBC

Daughter Card has been designed to have onboard Power System Basis Chip (SBC), [MC33FS6522LAE](#). This chip adds following options in the card,

- SMPS Pre-regulators
- Linear Regulators
- SPI Interface
- Fail Safe Output
- RESET output to MCU (RSTB)
- Interrupt Pulses to MCU (INTB)
- High Speed CAN Transceiver
- LIN Transceiver
- Debug Mode

Power Switch SW1 should be in ON position to use Daughter card in standalone mode which enables the use Power SBC supplies to MCU power domain.

## Board Interface Connector

The connection of any power domain and interfaces to Power SBC has to be enabled by respective jumper as described in [Table 10](#).

**Table 10: MCU power selection jumpers with PowerSBC**

Jumper	Description	Jumper Setting
J1	3.3V Selection	1-2: 3.3 V from onboard Power SBC to MCU
J2	5V Selection	1-2: 5 V from onboard Power SBC to MCU
J5	ADC Analog Supply Selection	2-3: Select 5 V from Switching Regulator
J12	VDD Core Supply Selection	1-2: 1.25 V from onboard Power SBC to MCU
J504 & J505	PowerSBC VCCA selection & Current Driving Capability	<u>J504: 2-3, J505:1-2:</u> SBC_3V3 with External PNP Transistor (upto 300mA) <u>J504: 1-2, J505: Open:</u> SBC_3V3 with internal MOSFET (up to 100mA)
J511	MISO Buffer Supply (SPI Bus level to connect with MCU)	1-2: Select SBC 3.3 V 2-3: Select SBC 5 V*
J512	SBC Debug Mode	Open: Normal Operation Short: Enters into Debug Mode at Start-up
J517	SPI Bus Selection from SBC/ Mother Board	<u>Connect Power SBC SPI to MCU:</u> 1-2, 4-5, 7-8, 10-11, 13-14, 16-17 <u>Connect MB SPI to MCU:</u> 3-2, 6-5, 7-8, 12-11, 15-14
J523	SBC RESET & Interrupt Signals	1-2: Connect SBC Interrupt to MCU 3-4: Connect SBC RESET Output to MCU

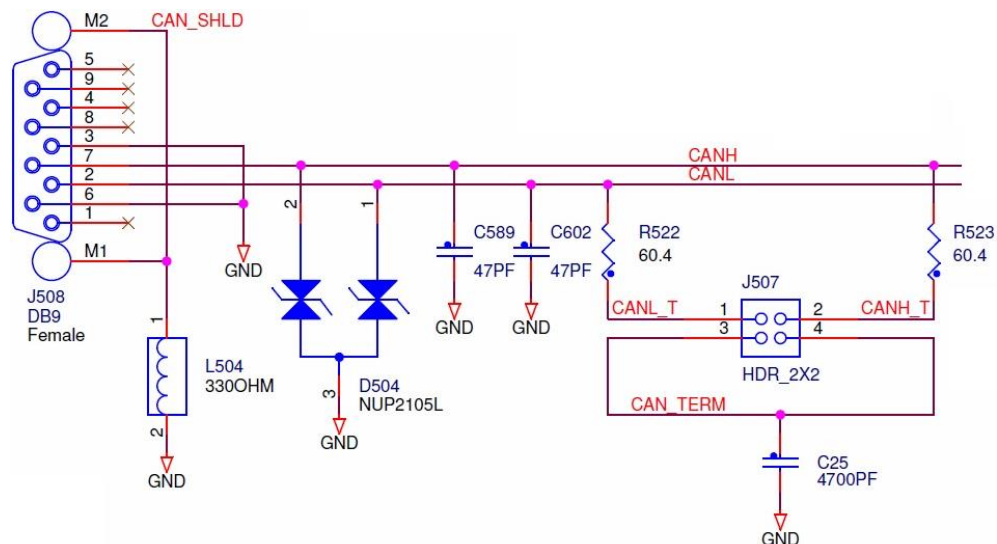
### NOTE

The PowerSBC does not connect to the 5.0V\_LR power rail which is powered by 5 V linear regulator when used with the motherboard. This rail is powering the VDDA\_SD & VDDA\_EQ (ADC supply) and VRH\_SD, VRH\_SEQ (ADC reference voltage). When using the daughter card standalone (without the motherboard) it is required to connect the 5.0V\_LR and the 5.0V\_SR rail as mentioned in [Table 10](#) in order for the microcontroller to come out of reset.

Power SBC has High Speed CAN Transceiver & LIN Transceiver. CAN bus from SBC is terminated with DB9 connector (J508) and LIN is terminated with 4-pin Molex connector (J503) in the Daughter Card.

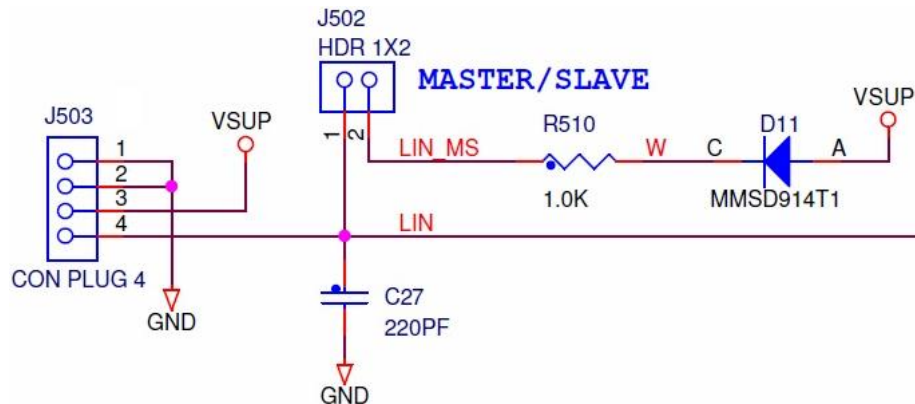
The connections of the J508 (CAN) from PowerSBC are detailed in [Figure 13](#).

## Board Interface Connector



**Figure 13: PowerSBC CAN Bus Circuit**

The connections of the J503 (LIN) from PowerSBC are detailed in Figure 14.



**Figure 14: PowerSBC LIN Interface**

The connection of CAN and LIN interface from Power SBC to MCU has to be enabled by respective jumper as described in Table 11.

**Table 11: PowerSBC CAN & LIN jumper selection**

Jumper	Description	Jumper Setting (* - Default)
J502	LIN Master/Slave Selection	1-2: Master Mode* Open: Slave Mode
J506	CAN/LIN Selection SBC/ Mother Board	2-3, 5-6 : Select CAN from Mother Board* 8-9, 11-12: Select LIN from Mother Board*  1-2, 4-5 : Select CAN from PowerSBC 7-8, 10-11: Select LIN from PowerSBC
J507	CAN Termination	1-3: Enable CANL Termination* 2-4: Enable CANH Termination*

## 4.2 Reset Circuit

To enable standalone use, the reset circuitry is placed on the daughter card. It consists of a reset switch (SW2) that is connected to reset pins RESET\_B via jumpers. It is also connected to the signal RST-SW\_B that is connected to the mother board to reset peripherals and RST\_B from PowerSBC is connected to MCU RESET\_B via jumper in order to assert RESET from PowerSBC. RSTOUT\_B from MCU is connected with LED to indicate the individual reset situations.

Due to the existence of chip internal Low Voltage Detect (LVD) and High Voltage Detect (HVD) circuits the EVB does not provide external voltage monitoring.

The EVB reset circuit provides the following functionality: It is indicated if the device is in reset through the red LED D8. The reset switch SW2 can be used to reset the MCU. The reset switch signal is connected to the MCU reset signals RESET (through jumper J23, J27) and the connections can be released by lifting the respective jumper. Pushing the reset switch will also reset peripherals that are connected to the board reset signal RST-SW. Orange LED D10 indicates when this signal is driven low by the reset switch (SW2).

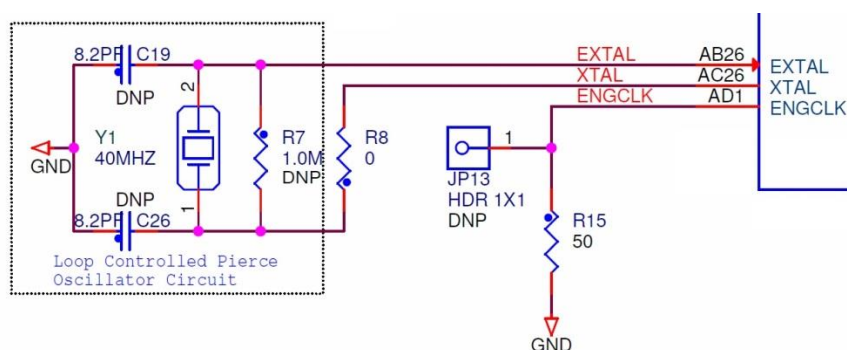
Additionally Power SBC has option to reset the MCU by setting jumper J523 (3-4). Various jumpers setting to reset MCU are detailed in [Table 12](#).

**Table 12: Reset circuit jumper settings**

Jumper	Description	Jumper Setting
J23 & J27	Connect reset switch circuit to RESET pin	1-2: connect to MCU RESET_B
J523	Connect Power SBC reset to MCU Reset	3-4: SBC_RSTB connect to RESET_B

## 4.3 MCU External Clock Circuit

In addition to the internal 16 MHz oscillator, the MCU can also be clocked by external oscillator (Y1). The clock circuitry for the 40 MHz crystal is shown in [Figure 15](#).



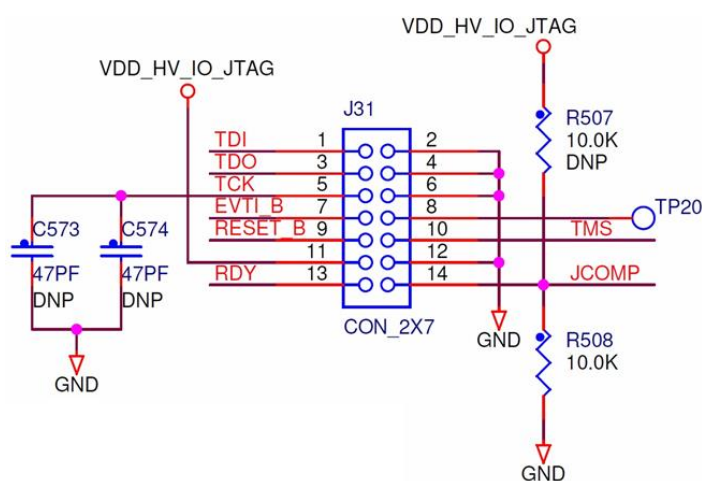
**Figure 15: 40 MHz crystal circuit**

## 4.4 JTAG Connector

The EVB is fitted with 14-pin JTAG debug connector. The [Figure 16](#) shows the 14-pin JTAG connector pinout (0.1in. keyed header). Jumper **J32** sets VDD\_HV\_IO\_JTAG to either 3.3V or 5V supply. JTAG jumper setting is detailed in [Table 13](#).

**Table 13: JTAG jumper settings**

Jumper	Description	Jumper Setting
J32	JTAG Power	1-2: Connect 3.3V to VDD_HV_IO_JTAG 2-3: Connect 5.0V to VDD_HV_IO_JTAG



**Figure 16: JTAG connector point**

## 4.5 Nexus Connector

[Table 14](#) Shows the pinout of the 50-pin SAMTEC connector for the MPC5777C (emulation device)

**Table 14: Trace Connector Pinout**

Pin No	Function	Pin No	Function
1	MSEO0_B	2	3.3V_SR
3	MSEO1_B	4	TCK
5	GND	6	TMS
7	MDO0	8	TDI
9	MDO1	10	TDO
11	GND	12	JCOMP
13	MDO2	14	RDY
15	MDO3	16	EVTI_B
17	GND	18	EVTO_B
19	MCKO	20	RESET_B
21	MDO4	22	RST_OUT_B

23	GND	24	GND
25	MDO5	26	Test Point
27	MDO6	28	Test Point
29	GND	30	GND
31	MDO7	32	Test Point
33	MDO8	34	Test Point
35	GND	36	GND
37	MDO9	38	Test Point
39	MDO10	40	Test Point
41	GND	42	GND
43	MDO11	44	MDO13
45	MDO12	46	MDO14
47	GND	48	GND
49	MDO15	50	NC
S1	GND	S2	GND

### 4.6 USB/UART Transceiver

USB to UART transceiver interface provided on the daughter card. USB TYPE B connector interfaced with FT232RQ, USB to serial UART chip (U502).

The USB to serial UART connection is shown in Figure 17.

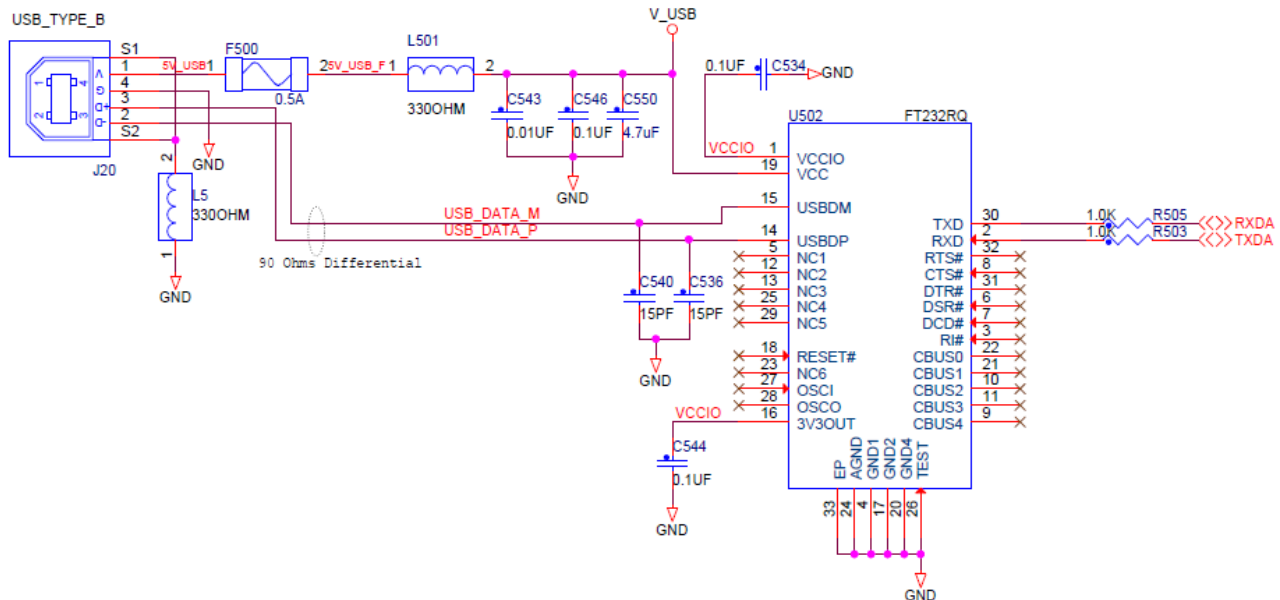


Figure 17: USB/UART Transceiver Circuit

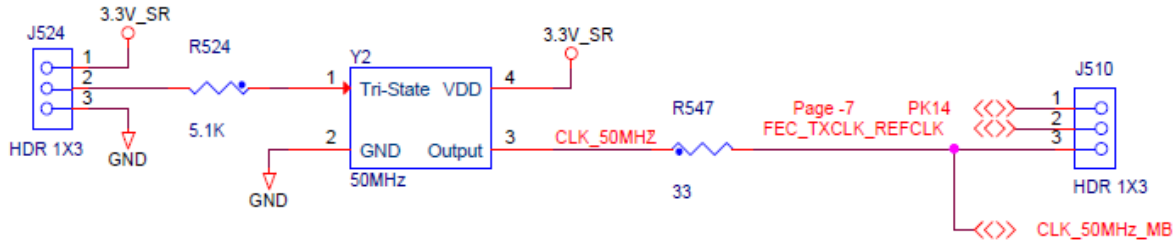
### 4.7 Ethernet (FEC) Interface

The signals from the MCU's Fast Ethernet Controller are terminated to Mother Board interface connector, J501. Further these signals are connected with Ethernet Physical Interface in the Mother Board. Also, in order to support Reduced Media-Independent Interface (RMII) mode, the Daughter

## Board Interface Connector

Card has the option to connect with an on-board clock oscillator circuit. For MII-Lite mode, the clock from the Ethernet Physical (PHY) interface on the Mother Board is available.

The FEC Clock Oscillator Circuit & Jumpers in the Daughter card is shown in the [Figure 18](#).



**Figure 18: FEC Clock Circuit**

Jumper settings for the FEC section are detailed in the [Table 15](#).

**Table 15: FEC Interface Jumper Details**

Jumper	Description	Jumper Setting – MII-Lite Mode	Jumper Setting – RMII Mode
J25	FEC_TXD2 Selection	2-3: Connect with PM4 (TXD2) from Mother Board	1-2: Connect with PM3 (RXER_MDIXEN) from MB.
J510	FEC Clock Selection	1-2: Connect with Mother Board	2-3: Connect with On Board 50MHz Oscillator
J524	On Board FEC 50MHz CLK Enable	1-2: Clock Oscillator in Tri-state	2-3: Clock Oscillator in Normal Operation

## 4.8 Zipwire Interface

The MCU features a bus for communicating between two devices over a high speed (240 MHz) serial interface called Zipwire. It is implemented using a Serial Inter-Processor Interface (SIPI) over an LVDS Fast synchronous Serial Transmission Interface (LFAST). The SIPI module controls the higher level protocol of the interface, and the LFAST controls the physical interface.

This interface consists of five signals:

- a pair of LVDS transmits pins,
- a pair of receive LVDS pins and
- a clock. The clock is unidirectional and is defined to be an output on the Slave and an input on the Master node.

The daughter card SIPI connector (J13) interface signal diagram is shown in [Figure 19](#).



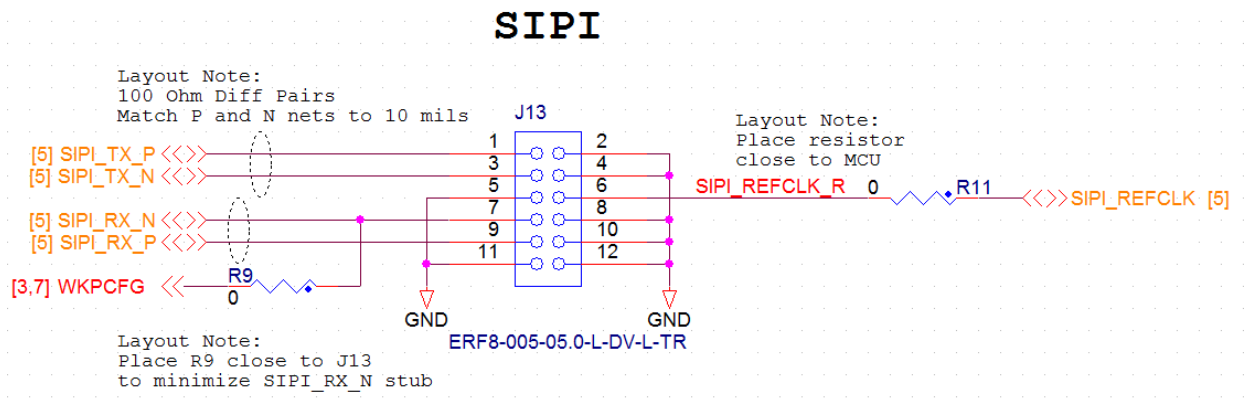


Figure 19: SIPI Interface connections Figure 19

The connector used in the daughter card and its mating Zipwire cable is detailed in Table 16.

Table 16: Connector and its mating Cable Details

S.No	Connector/Cable	Manufacturer	Manufacturer Part Number
1	Connector on the Daughter card	SAMTEC	ERF8-005-05.0-L-DV-L-TR
2	Zipwire Cable Assembly	NXP	SIPI-ERM8-ZIPCBL

**Reference:** For more information about the ZIP wire Interface is available at [www.nxp.com](http://www.nxp.com) Application Note AN5134 “Introduction to the Zipwire Interface”.

**CAUTION**

Zipwire is intended to be used between two devices on the same printed circuit board. This connector and cable is only intended for evaluation of products and not for actual customer implementations.

### 4.9 MCU Interfaces with Mother Board

The Signals interfaces from the MCU are connected with High Density connector which connects with Mother Board for user access. Following interfaces can be access in the Mother Board through 0.1inch pitch 18-pin Headers,

- ADC channels
- Enhanced Modular IO Subsystem (eMIOS)
- Enhanced Time Processing Unit (eTPU)
- Deserial Serial Peripheral Interface (DSPI)

### 4.10 Test points — 416 Daughter Card

MPC5777C-416DS Daughter card test points are listed and detailed in

Table 17.

Table 17: Test points – 416 daughter card

Signal	TP name	Shape	Description
MB PL11	TP3	Pad	Motherboard connection PL11
MB PL13	TP4	Pad	Motherboard connection PL13
MB PL15	TP5	Pad	Motherboard connection PL15
MB PJ5	TP6	Pad	Motherboard connection PJ5
MB PL9	TP7	Pad	Motherboard connection PL9
MB PJ7	TP8	Pad	Motherboard connection PJ7
MB PD7	TP9	Pad	Motherboard connection PD7
MB PF13	TP10	Pad	Motherboard connection PF13
MB PD6	TP11	Pad	Motherboard connection PD6
5.0V_LR	TP12	Hook	5V linear regulator output
RST_OUT_B	TP13	Pad	Reset out from U1
J22 26	TP14	Pad	NEXUS connection J22 26
J22 28	TP15	Pad	NEXUS connection J22 28
J22 32	TP16	Pad	NEXUS connection J22 32
J22 34	TP17	Pad	NEXUS connection J22 34
J22 38	TP18	Pad	NEXUS connection J22 38
J22 40	TP19	Pad	NEXUS connection J22 40
J31 8	TP20	Pad	JTAG connection J31 8
MB PA8	TP21	Pad	Motherboard connection PA8
MB PA14	TP22	Pad	Motherboard connection PA14
MB PA6	TP23	Pad	Motherboard connection PA6
MB PA5	TP24	Pad	Motherboard connection PA5
MB PA7	TP25	Pad	Motherboard connection PA7
MB PA9	TP26	Pad	Motherboard connection PA9
SBC_5V	TP27	Pad	SBC_5V
GND	GT1 to GT11	Hook	Ground Reference
5.0V_SR	JP1	Pin	5.0V Switching Regulator
GND	JP2	Pin	Ground Reference
3.3V_SR	JP3	Pin	3.3V Switching Regulator
5.0V_SR	JP4	Pin	5.0V Switching Regulator
1.25V_SR	JP5	Pin	1.25V Switching Regulator
GND	JP6	Pin	Ground Reference
3.3V_SR	JP8	Pin	3.3V Switching Regulator

Signal	TP name	Shape	Description
5.0V_SR	JP9	Pin	5.0V Switching Regulator
1.25V_SR	JP10	Pin	1.25V Switching Regulator
GND	JP11	Pin	Ground Reference
1.25V_SR	JP12	Pin	1.25V Switching Regulator
ENGCLK	JP13	Pin	ENGCLK
GND	JP14	Pin	Ground Reference
5.0V_SR	JP15	Pin	5.0V Switching Regulator
3.3V_SR	JP16	Pin	3.3V Switching Regulator
3.3V_SR	JP17	Pin	3.3V Switching Regulator

## 4.11 Configuring the Daughter Card for Standalone Use

It is possible to use the daughter cards without the motherboard to run code on the microcontroller. Power to the daughter cards must be supplied through the terminal power connector JP7 – EXT PWR. It is required to connect all three voltages (1.25 V, 3.3 V, 5V SR and 5 V LR) and ground as explained in [Section 4.1.2 “Daughter Card Standalone Power Input -External”](#)(or)

The Daughter Card can be used in standalone by enabling PowerSBC with its respective jumpers as described in the [Section 4.1.3 “Daughter Card Standalone Power Input –Power SBC”](#).

Additional to enabling PowerSBC power supply it is required to connect the 5V\_SR power rail to the Analog power rail of the daughter card that powers the VDDA\_SD & VDDA\_EQ (ADC supply) and VRH\_SD, VRH\_SEQ (ADC reference voltage) pins. It is recommended to do that by installing a jumper connecting J5 (2-3) (5.0V\_SR) to Analog Supply Rail.

## 5. Configuration — MPC5777C-516DS Daughter card

This section details the configuration of each of the **MPC5777C-516DS** daughter card’s functional blocks.

The daughter card has been designed with ease of use in mind and has been segmented into functional blocks as shown in . Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

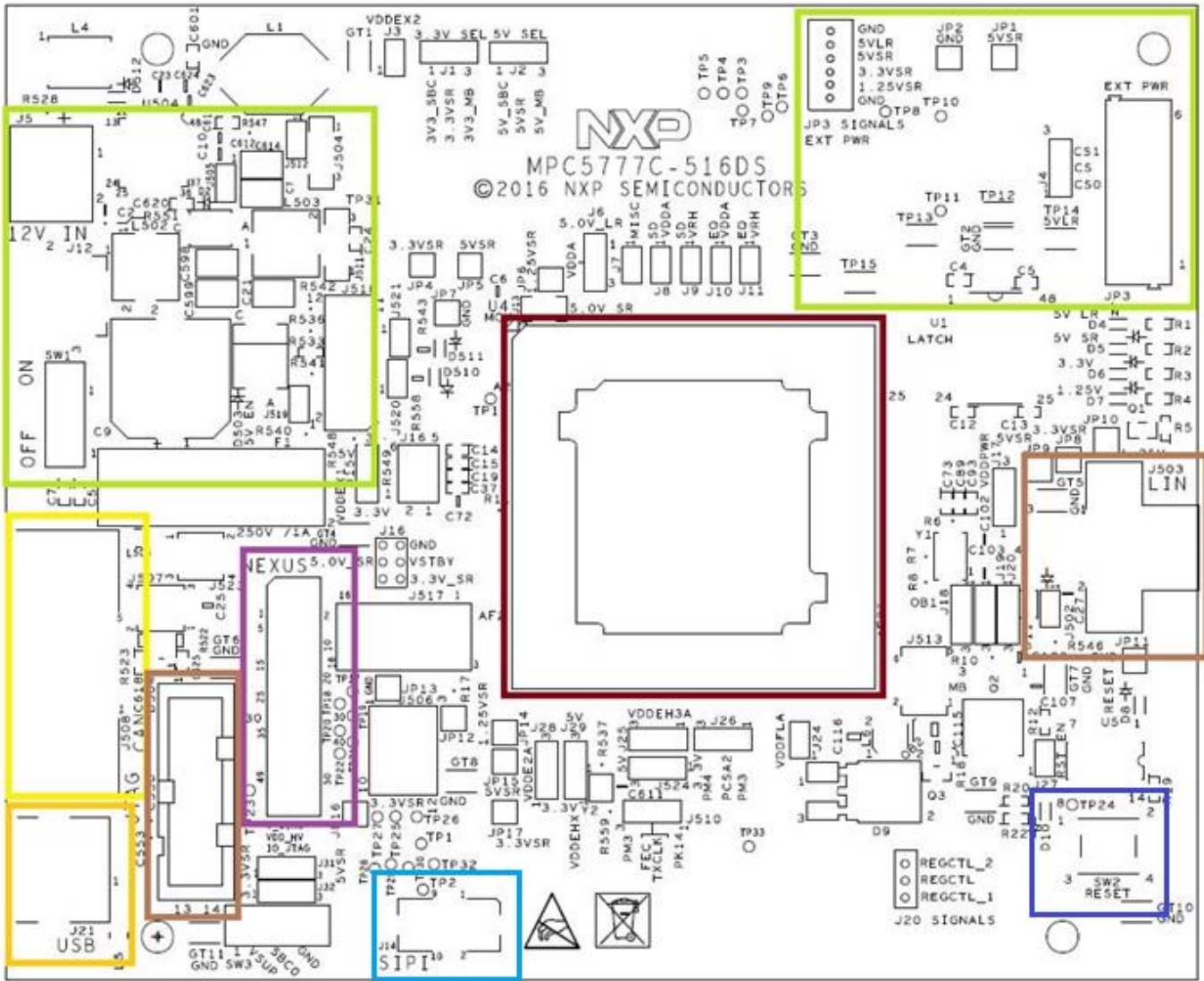


Figure 20: MPC5777C-516DS Daughter card — functional blocks

## 5.1 MCU Power

### 5.1.1 Supply Routing and Jumpers

The different MCU supplies are connected to the regulators on the Mother Board through the interface connector. Also daughter card has option to connect MCU supplies to either Mother Board supplies or onboard regulators.

The connection of any power domain to a regulator has to be enabled by a dedicated jumper as described in [Table 18](#).

Jumper options to achieve the above power supply modes:

Table 18: Jumper options for various power modes

Mode name	J18 (REGSEL_TO_GND)	J24 (VDDFLA_SEL)	J17 (VDDPWR_SEL)	J19 (VDDPMC_SEL)	J20 (REGCTL_SEL)	J513 (1V25_SR_MB_SEL) and J13 (SBC_1V25) <sup>2</sup>
LDO5V	2&3 -GND	OPEN - Bypass caps	2&3 - 5V_SR	2&3 - 5V_SR	2&3 for LV Linear Regulator	J513- 3&4 for 1.25V_SR_OB1 (LR) J13 - Open
SMPS5V	1&2 - HIGH - 5V	OPEN - Bypass caps	2&3 - 5V_SR	2&3 - 5V_SR	1&2 for LV SPMS	J513- 5&6 for 1.25V_SR_OB2(SR) J13 - Open
LDO3V	2&3 -GND	CLOSED - VDDPWR& VDDPMC	1&2 - 3V3_SR	1&2 - 3V3_SR	2&3 for LV Linear Regulator	J513- 3&4 for 1.25V_SR_OB1 (LR) J13 - Open
SMPS3V	1&2 - HIGH - 3V3	CLOSED - VDDPWR& VDDPMC	1&2 - 3V3_SR	1&2 - 3V3_SR	1&2 for LV SPMS	J513- 5&6 for 1.25V_SR_OB2(SR) J13 - Open
External	2&3 -GND	CLOSED - VDDPWR& VDDPMC	1&2 - 3V3_SR	1&2 - 3V3_SR	N/C	J513- 1&2 for 1.25V_SR_MB -OR- J13-1&2 for SBC_1V25
External	2&3 -GND	OPEN - Bypass caps	2&3 - 5V_SR	2&3 - 5V_SR	N/C	J513-1&2 for 1.25V_SR_MB -OR- J13-1&2 for SBC_1V25

Other Power supply Jumper settings:

Table 19: MCU power selection jumpers

Jumper	Description	Jumper Setting (* - default)
J1	3.3V Selection	1-2: 3.3V from onboard Power SBC 2-3: 3.3V from Mother Board*
J2	5V Selection	1-2: 5V from onboard Power SBC 2-3: 5V from Mother Board*
J32	IO Levels in the Mother Board - VDD_HV_IO_MAIN	1-2: Select 3.3V 2-3: Select 5V*
J6	ADC Analog Supply Selection	1-2: Select 5V from Linear Regulator* 2-3: Select 5V from Switching Regulator
J7	Connect TRNG, Internal RC oscillator Supply -VDDA_MISC	1-2: Connect VDDA_MISC to 5V_SR*
J8 & J9	Connect SD ADC supply & Reference –VDDA_SD, VRH_SD	J7, 1-2: Connect VDDA_SD* J8, 1-2: Connect VRH_SD*
J10 & J11	Connect eQADC supply & Reference – VDDA_EQ, VRH_EQ	J9, 1-2: Connect VDDA_EQ* J10, 1-2: Connect VRH_EQ*
J15	Fast I/O Pads supply selection - VDDE2	1-2: Select 3.3V* 2-3: Select 5V

<sup>2</sup>**CAUTION:** For 1.25 V source selection, a single jumper must be installed on either J513 or J13, but not on both at a time.

## Board Interface Connector

Jumper	Description	Jumper Setting (* - default)
J16	RAM Standby supply selection - VSTBY	1-3: Select 3.3 V 5-3: Select GND* 4-3: Select 5 V
J17	SMPS Driver Supply Selection - VDDPWR	1-2: Select 3.3 V 2-3: Select 5 V*
J18	Core Supply generation, Regulation Mode - REGSEL	1-2: Select SMPS Configuration (VDD_PMC) 2-3: Select Linear Configuration (GND)*
J19	PMC Supply Selection – VDDPMC	1-2: Select 3.3 V 2-3: Select 5 V*
J20	Core Supply generation, Regulator Control -REGCTL	1-2: Select SMPS to derive (1.25V_SR_OB2) 2-3: Select Linear to derive (1.25V_SR_OB1)*
J513	VDD Core Supply Selection	1-2: 1.25 V from Mother Board* 3-4: 1.25 V onboard Regulator (Linear Mode) 5-6: 1.25 V onboard Regulator (Switching Mode)
J13	VDD Core Supply Selection	1-2: 1.25 V from onboard Power SBC
J25	Medium I/O Pads supply selection – VDDEH3A	1-2: Select 3.3 V 2-3: Select 5 V*
J24	Connect Flash Core Supply - VDDFLA	1-2: Connect VDDFLA to 3.3V_SR
J28	Fast I/O Pads supply selection - VDDE2A	1-2: Select 3.3 V* 2-3: Select 5 V
J29	Medium I/O Pads supply selection - VDDEHx	1-2: Select 3.3 V 2-3: Select 5 V*
-	Medium I/O Pads supply enable – VDDEHx	1-2: Connect VDDEH1* 3-4: Connect VDDEH3* 5-6: Connect VDDEH4* 7-8: Connect VDDEH5* 9-10: Connect VDDEH6* 11-12: Connect VDDEH7* All jumpers in J30 placed by Default
J31	JTAG IO Level - VDD_HV_IO_JTAG	1-2: Select 3.3 V* 2-3: Select 5 V
J520	Connect LED for ETPUA0	1-2: Connect LED with Signal ETPUA0*
J521	Connect LED for ETPUA1	1-2: Connect LED with Signal ETPUA1*
J32	VDD_HV_IO_MAIN_SEL	2-3: For 5 V
		1-2: For 3.3 V

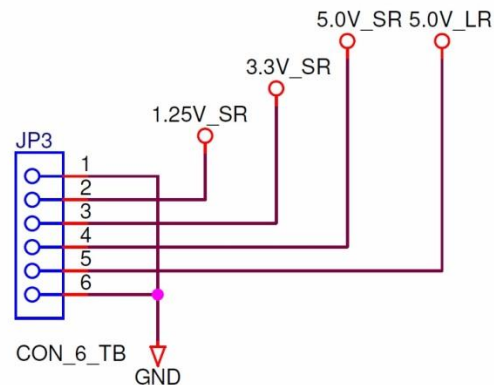
### 5.1.2 Daughter Card Standalone Power Input -External

A terminal power input is provided on the daughter card to enable use of the daughter card without the motherboard.

When power is applied to the Daughter Card from Motherboard or External Terminal input or PowerSBC with respective jumper selection, four green power LEDs adjacent to the terminal power input connector (JP3) show the presence of the supply voltages as follows:

- LED D4 – Indicates that the 5.0 V linear regulator is enabled and working correctly
- LED D5 – Indicates that the 5.0 V switching regulator is enabled and working correctly
- LED D6 – Indicates that the 3.3 V switching regulator is enabled and working correctly
- LED D7 – Indicates that the 1.25 V switching regulator is enabled and working correctly

The connections of the JP7 power terminal are detailed in [Figure 21](#).



**Figure 21: Terminal power input connections**

### 5.1.3 Daughter Card Standalone Power Input –Power SBC

Daughter Card has been designed to have onboard Power System Basis Chip (SBC), [MC33FS6522LAE](#). This chip adds following options in the card,

- SMPS Pre-regulators
- Linear Regulators
- SPI Interface
- Fail Safe Output
- RESET output to MCU (RSTB)
- Interrupt Pulses to MCU (INTB)
- High Speed CAN Transceiver
- LIN Transceiver
- Debug Mode

Power Switch SW1 should be in ON position to use Daughter card in standalone mode which enables the use Power SBC supplies to MCU power domain.

The connection of any power domain and interfaces to Power SBC has to be enabled by respective jumper as described in [Table 20](#).

**Table 20: MCU power selection jumpers with PowerSBC**

Jumper	Description	Jumper Setting
J1	3.3V Selection	1-2: 3.3 V from onboard Power SBC to MCU
J2	5V Selection	1-2: 5 V from onboard Power SBC to MCU
<u>J6</u>	ADC Analog Supply Selection	2-3: Select 5 V from Switching Regulator
<u>J13</u>	VDD Core Supply Selection	1-2: 1.25 V from onboard Power SBC to MCU
J504 & J505	PowerSBC VCCA selection & Current Driving Capability	<u>J504: 2-3, J505:1-2:</u> SBC_3V3 with External PNP Transistor (upto 300mA) <u>J504: 1-2, J505: Open:</u> SBC_3V3 with internal MOSFET (up to 100mA)
J511	MISO Buffer Supply (SPI Bus level to connect with MCU)	1-2: Select SBC 3.3 V 2-3: Select SBC 5 V
J512	SBC Debug Mode	Open: Normal Operation Short: Enters into Debug Mode at Start-up
J517	SPI Bus Selection from SBC/ Mother Board	<u>Connect Power SBC SPI to MCU:</u> 1-2, 4-5, 7-8, 10-11, 13-14, 16-17 <u>Connect MB SPI to MCU:</u> 3-2, 6-5, 7-8, 12-11, 15-14
J523	SBC RESET & Interrupt Signals	1-2: Connect SBC Interrupt to MCU 3-4: Connect SBC RESET Output to MCU

### NOTE

The PowerSBC does not connect to the 5.0V\_LR power rail which is powered by 5 V linear regulator when used with the motherboard. This rail is powering the VDDA\_SD & VDDA\_EQ (ADC supply) and VRH\_SD, VRH\_SEQ (ADC reference voltage). When using the daughter card standalone (without the motherboard) it is required to connect the 5.0V\_LR and the 5.0V\_SR rail as mentioned in [Table 10](#) in order for the microcontroller to come out of reset.

Power SBC has High Speed CAN Transceiver & LIN Transceiver. CAN bus from SBC is terminated with DB9 connector (J508) and LIN is terminated with 4-pin Molex connector (J503) in the Daughter Card.

The connections of the J508 (CAN) from PowerSBC are detailed in [Figure 22](#).



## Board Interface Connector

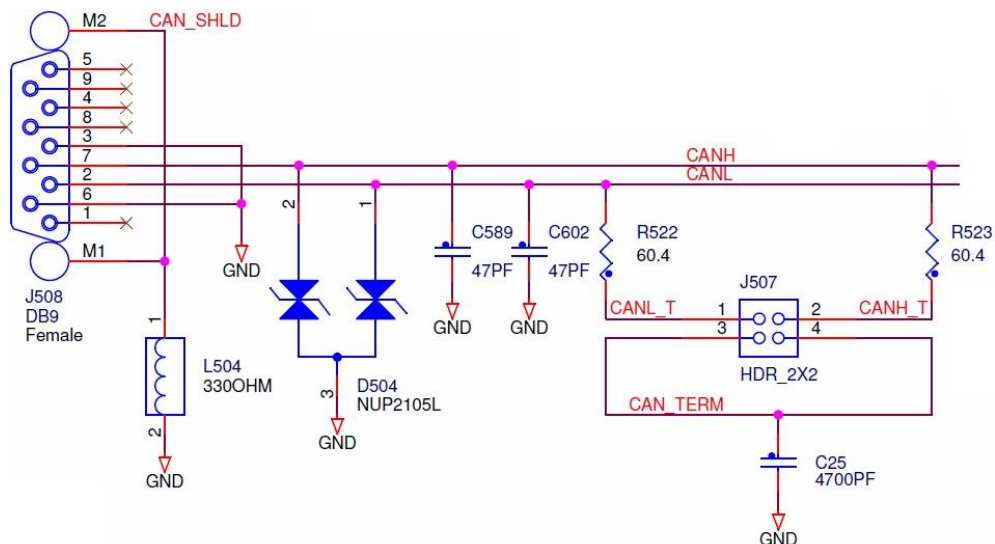


Figure 22: PowerSBC CAN Bus Circuit1

The connections of the J503 (LIN) from PowerSBC are detailed in Figure 23.

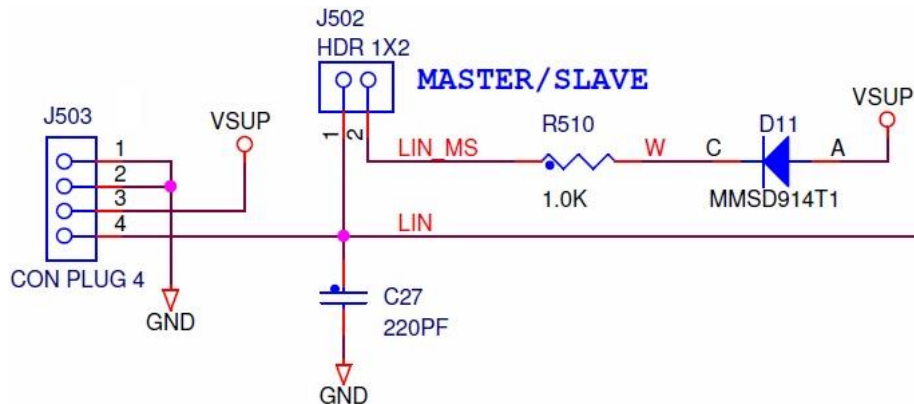


Figure 23: PowerSBC LIN Interface

The connection of CAN and LIN interface from Power SBC to MCU has to be enabled by respective jumper as described in Table .

Table 21: PowerSBC CAN & LIN jumper selection

Jumper	Description	Jumper Setting (* - Default)
J502	LIN Master/Slave Selection	1-2: Master Mode* Open: Slave Mode
J506	CAN/LIN Selection SBC/ Mother Board	2-3, 5-6 : Select CAN from Mother Board* 8-9, 11-12: Select LIN from Mother Board* 1-2, 4-5 : Select CAN from PowerSBC
J507	CAN Termination	1-3: Enable CANL Termination* 2-4: Enable CANH Termination*

## 5.2 Reset Circuit

To enable standalone use, the reset circuitry is placed on the daughter card. It consists of a reset switch (SW2) that is connected to reset pins RESET\_B via jumpers. It is also connected to the signal RST-SW\_B that is connected to the mother board to reset peripherals and RST\_B from PowerSBC is connected to MCU RESET\_B via jumper in order to assert RESET from PowerSBC. RSTOUT\_B from MCU is connected with LED to indicate the individual reset situations.

Due to the existence of chip internal Low Voltage Detect (LVD) and High Voltage Detect (HVD) circuits the EVB does not provide external voltage monitoring.

The EVB reset circuit provides the following functionality: It is indicated if the device is in reset through the red LED D8. The reset switch SW2 can be used to reset the MCU. The reset switch signal is connected to the MCU reset signals RESET (through jumper J27) and the connections can be released by lifting the respective jumper. Pushing the reset switch will also reset peripherals that are connected to the board reset signal RST-SW. Orange LED D10 indicates when this signal is driven low by the reset switch (SW2).

Additionally Power SBC has option to reset the MCU by setting jumper J523 (3-4). Various jumpers setting to reset MCU are detailed in [Table 19](#).

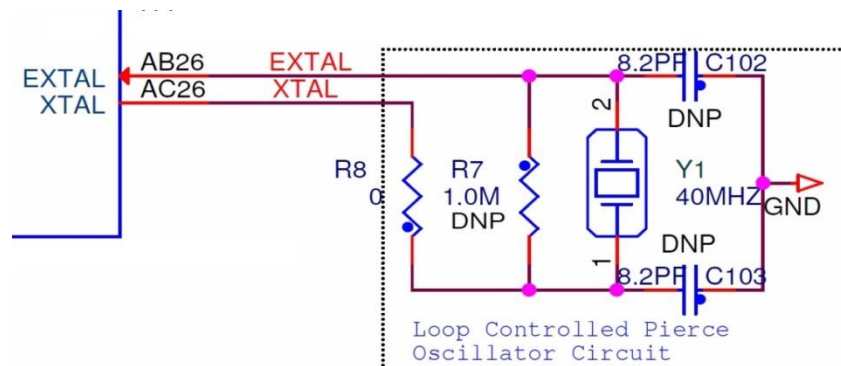
**Table 192: Reset circuit jumper settings**

Jumper	Description	Jumper Setting
J27	Connect reset switch circuit to RESET pin	1-2: connect to MCU RESET_B
J523	Connect Power SBC reset to MCU Reset	3-4: SBC_RSTB connect to RESET_B

## 5.3 MCU External Clock Circuit

In addition to the internal 16 MHz oscillator, the MCU can also be clocked by external oscillator (Y1).

The clock circuitry for the 40 MHz crystal is shown in [Figure 24](#).



**Figure 24: 40 MHz crystal circuit**

## 5.4 JTAG Connector

The EVB is fitted with 14-pin JTAG debug connector. The [Figure 25](#) shows the 14-pin JTAG connector pinout (0.1in. keyed header). Jumper **J31** sets VDD\_HV\_IO\_JTAG to either 3.3V or 5V supply. JTAG jumper setting is detailed in [Table 20](#).

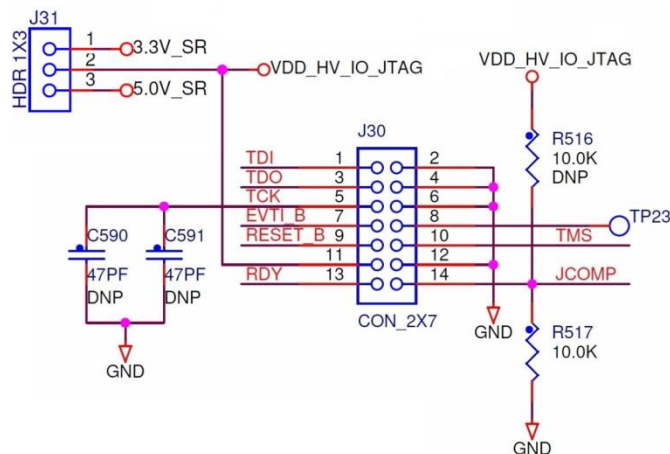


Figure 25: JTAG connector point

Table 203: JTAG jumper settings

Jumper	Description	Jumper Setting
J31	JTAG Power	1-2: Connect 3.3V to VDD_HV_IO_JTAG 2-3: Connect 5.0V to VDD_HV_IO_JTAG

## 5.5 Nexus Connector

[Table](#) Shows the pinout of the 50-pin SAMTEC connector for the MPC5777C (emulation device)

Table 24: Trace Connector Pinout

Pin No	Function	Pin No	Function
1	MSEO0_B	2	3.3V_SR
3	MSEO1_B	4	TCK
5	GND	6	TMS
7	MDO0	8	TDI
9	MDO1	10	TDO
11	GND	12	JCOMP
13	MDO2	14	RDY
15	MDO3	16	EVTI_B
17	GND	18	EVTO_B
19	MCKO	20	RESET_B
21	MDO4	22	RST_OUT_B
23	GND	24	GND
25	MDO5	26	Test Point

## Board Interface Connector

27	MDO6	28	Test Point
29	GND	30	GND
31	MDO7	32	Test Point
33	MDO8	34	Test Point
35	GND	36	GND
37	MDO9	38	Test Point
39	MDO10	40	Test Point
41	GND	42	GND
43	MDO11	44	MDO13
45	MDO12	46	MDO14
47	GND	48	GND
49	MDO15	50	NC
S1	GND	S2	GND

## 5.6 USB/UART Transceiver

USB to UART transceiver interface provided on the daughter card. USB TYPE B connector interfaced with FT232RQ, USB to serial UART chip (U502).

The USB to serial UART connection is shown in Figure 26.

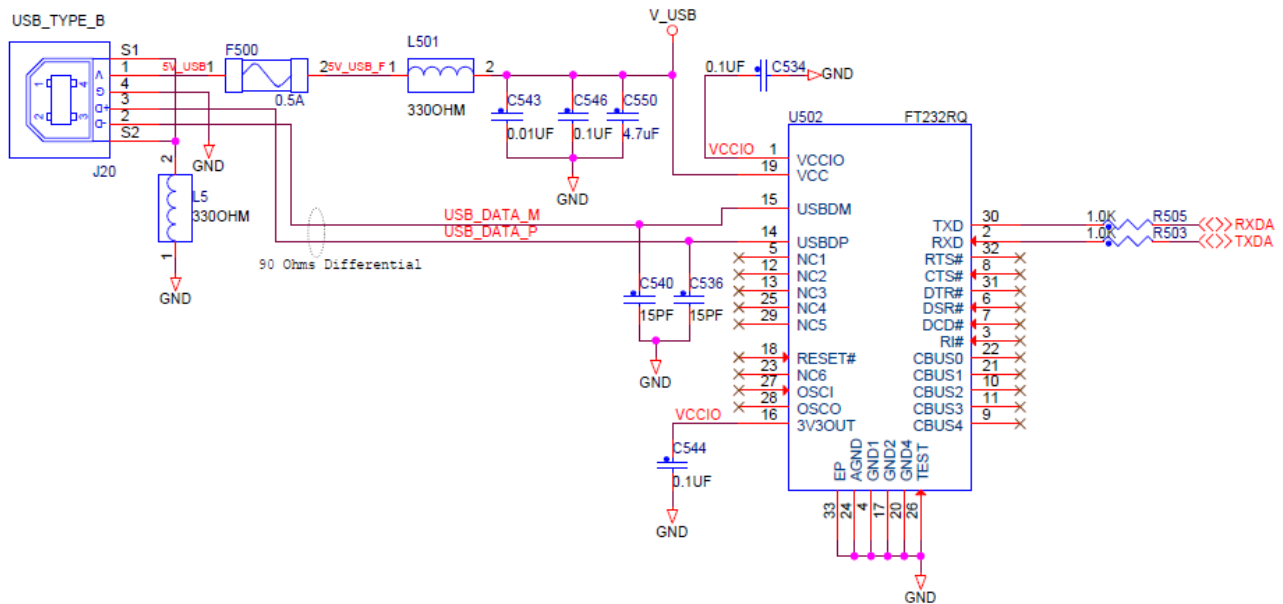


Figure 26: USB/UART Transceiver Circuit

## 5.7 Ethernet (FEC) Interface

The signals from the MCU's Fast Ethernet Controller are terminated to Mother Board interface connector, J501. Further these signals are connected with Ethernet Physical Interface in the Mother Board. Also, in order to support Reduced Media-Independent Interface (RMII) mode, the Daughter

Card has the option to connect with an on-board clock oscillator circuit. For MII-Lite mode, the clock from the Ethernet Physical (PHY) interface on the Mother Board is available.

Jumper settings for the FEC section are detailed in the [Table 21](#).

**Table 215: FEC Interface Jumper Details**

Jumper	Description	Jumper Setting – MII-Lite Mode	Jumper Setting – RMII Mode
J26	FEC_TXD2 Selection	2-3: Connect with PM4 (TXD2) from Mother Board	1-2: Connect with PM3 (RXER_MDIXEN) from MB.
J510	FEC Clock Selection	1-2: Connect with Mother Board	2-3: Connect with On Board 50MHz Oscillator
J524	On Board FEC 50MHz CLK Enable	1-2: Clock Oscillator in Tri-state	2-3: Clock Oscillator in Normal Operation

## 5.8 External Bus Interface (EBI)

External Bus Interface (EBI) is not available on 416 BGA. It is available only on the 516 BGA. The EBI is interfaced with Cypress’ 4Mbit SRAM on MPC5777C-516DS Daughter Card as shown in [Figure 27](#). J4 allows connection of SRAM’s chip select with MCU ship select D\_CS0 or D\_CS1.

**Table 226 FEC Interface Jumper Details**

Jumper	Description	Jumper Setting
J4	SRAM Chip Select	1-2: D_CS0 from MCU 2-3: D_CS1 from MCU*

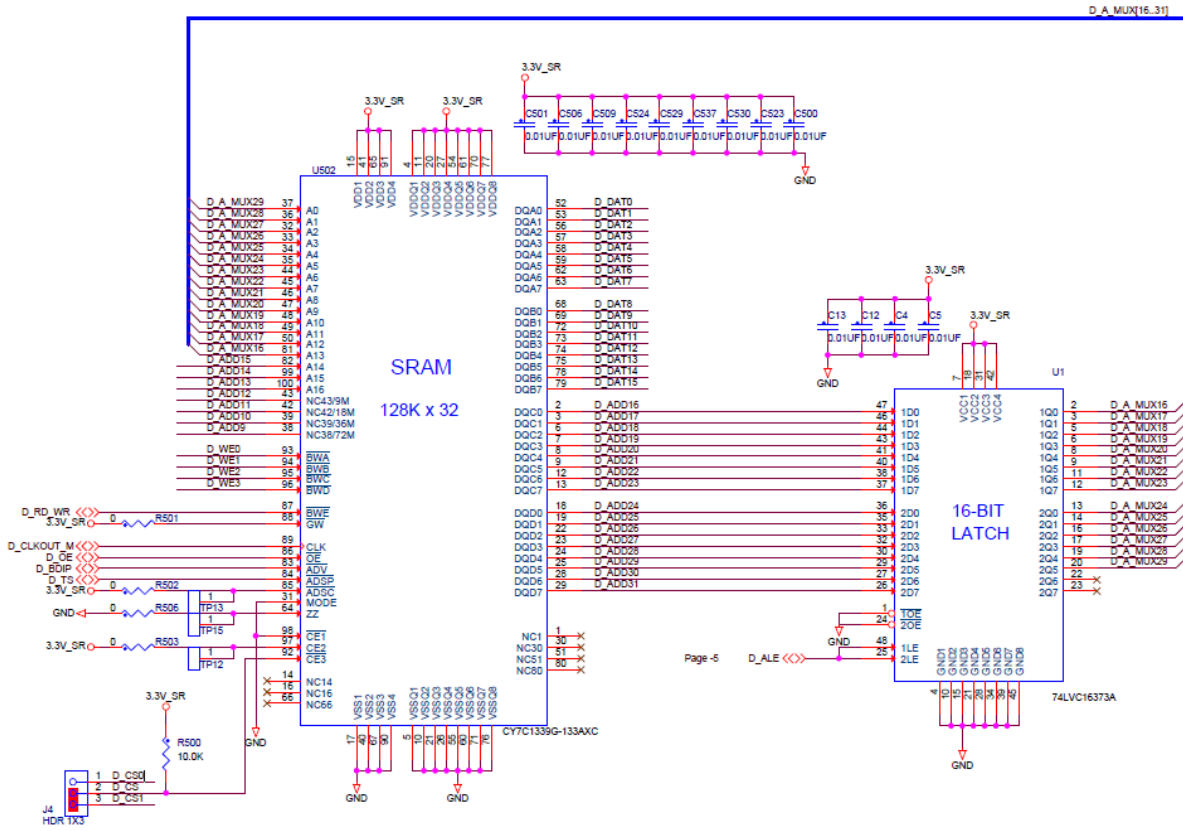


Figure 27: EBI-SRAM Interface

## 5.9 Zipwire Interface

The MCU features a bus for communicating between two devices over a high speed (240 MHz) serial interface called Zipwire. It is implemented using a Serial Inter-Processor Interface (SIPI) over an LVDS Fast synchronous Serial Transmission Interface (LFAST). The SIPI module controls the higher level protocol of the interface, and the LFAST controls the physical interface.

This interface consists of five signals:

- a pair of LVDS transmits pins,
- a pair of receive LVDS pins and
- a clock. The clock is unidirectional and is defined to be an output on the Slave and an input on the Master node.

The daughter card SIPI connector (J14) interface signal diagram is shown in Figure 28.

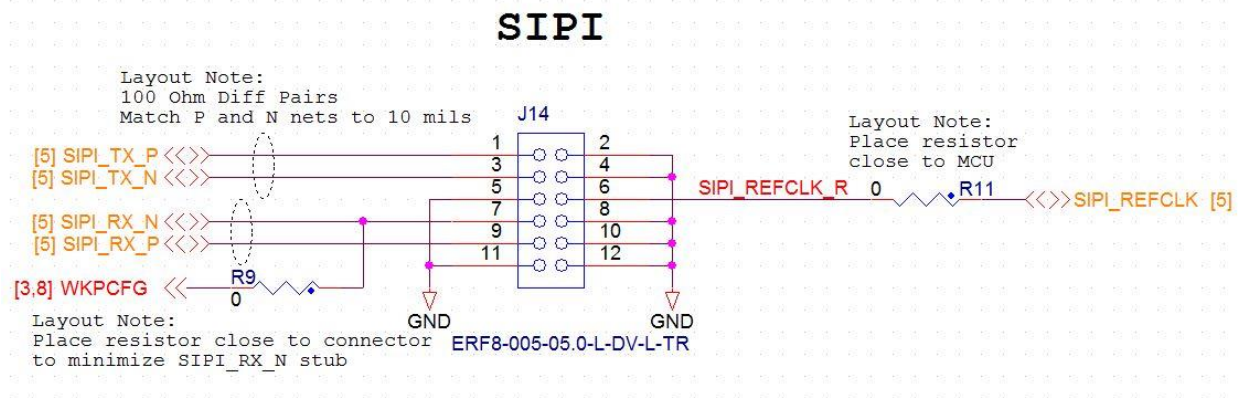


Figure 28: SIPI Interface connections

The connector used in the daughter card and its mating Zipwire cable is detailed in Table 23.

Table 237: Connector and its mating Cable Details

S.No	Connector/Cable	Manufacturer	Manufacturer Part Number
1	Connector on the Daughter card	SAMTEC	ERF8-005-05.0-L-DV-L-TR
2	Zipwire Cable Assembly	NXP	SIPI-ERM8-ZIPCBL

**Reference:** For more information about the ZIP wire Interface is available at [www.nxp.com](http://www.nxp.com) Application Note AN5134 “Introduction to the Zipwire Interface”.

**CAUTION**

Zipwire is intended to be used between two devices on the same printed circuit board. This connector and cable is only intended for evaluation of products and not for actual customer implementations.

### 5.10 MCU Interfaces with Mother Board

The Signals interfaces from the MCU are connected with High Density connector which connects with Mother Board for user access. Following interfaces can be access in the Mother Board through 0.1inch pitch 18-pin Headers,

- ADC channels
- Enhanced Modular IO Subsystem (eMIOS)
- Enhanced Time Processing Unit (eTPU)
- Deserial Serial Peripheral Interface (DSPI)

### 5.11 Test points — 516 Daughter Card

MPC5777C-516DS Daughter card test points are listed and detailed in Table .

Table 28: Test points — 516 daughter card

Signal	TP name	Shape	Description
MB PL11	TP3	Pad	Motherboard connection PL11
MB PL13	TP4	Pad	Motherboard connection PL13
MB PL15	TP5	Pad	Motherboard connection PL15
MB PJ5	TP6	Pad	Motherboard connection PJ 5
MB PL9	TP7	Pad	Motherboard connection PL 9
MB PF13	TP8	Pad	Motherboard connection PF13
MB PJ7	TP9	Pad	Motherboard connection PJ7
MB PD7	TP10	Pad	Motherboard connection PD 7
MB PD6	TP11	Pad	Motherboard connection PD6
CE2	TP12	Hook	Chip enable 2 input of SRAM (U502)
ADSC	TP13	Hook	Address strobe from MCU to SRAM
5V_LR	TP14	Hook	5V linear regulator
ZZ	TP15	Hook	Sleep input of SRAM
RST_OUT_B	TP16	Pad	Reset out of U4
J23 26	TP17	Pad	NEXUS connection J23 26
J23 28	TP18	Pad	NEXUS connection J23 28
J23 32	TP19	Pad	NEXUS connection J23 32
J23 34	TP20	Pad	NEXUS connection J23 34
J23 38	TP21	Pad	NEXUS connection J23 38
J23 40	TP22	Pad	NEXUS connection J23 40
J30 8	TP23	Pad	JTAG connector J30 8
U5 8	TP24	Pad	IC U5 PIN 8
MB PA8	TP25	Pad	Motherboard connection PA8
MB PA14	TP26	Pad	Motherboard connection PA14
MB PA6	TP27	Pad	Motherboard connection PA6
MB PA5	TP28	Pad	Motherboard connection PA5
MB PA7	TP29	Pad	Motherboard connection PA7
MB PA9	TP30	Pad	Motherboard connection PA9
SBC_5V	TP31	Pad	SBC_5V
GND	GT1 to GT11	Hook	Ground Reference
5.0V_SR	JP1	Pin	5.0V Switching Regulator
GND	JP2	Pin	Ground Reference
3.3V_SR	JP4	Pin	3.3V Switching Regulator
5.0V_SR	JP5	Pin	5.0V Switching Regulator
1.25V_SR	JP6	Pin	1.25V Switching Regulator
GND	JP7	Pin	Ground Reference
3.3V_SR	JP8	Pin	3.3V Switching Regulator



Signal	TP name	Shape	Description
5.0V_SR	JP9	Pin	5.0V Switching Regulator
1.25V_SR	JP10	Pin	1.25V Switching Regulator
GND	JP11	Pin	Ground Reference
ENGCLK	JP12	Pin	ENGCLK
GND	JP13	Pin	Ground Reference
1.25V_SR	JP14	Pin	1.25V Switching Regulator
5.0V_SR	JP15	Pin	5.0V Switching Regulator
3.3V_SR	JP16	Pin	3.3V Switching Regulator
3.3V_SR	JP17	Pin	3.3V Switching Regulator

## 5.12 Configuring the 516 Daughter Card for Standalone Use

It is possible to use the daughter cards without the motherboard to run code on the microcontroller. Power to the daughter cards must be supplied through the terminal power connector JP3 – EXT PWR. It is required to connect all three voltages (1.25 V, 3.3 V, 5V SR and 5 V LR) and ground as explained in [Section 5.1.2](#) (or)

The Daughter Card can be used in standalone by enabling PowerSBC with its respective jumpers as described in the [Section 5.1.3](#).

Additional to enabling PowerSBC power supply it is required to connect the 5V\_SR power rail to the Analog power rail of the daughter card that powers the VDDA\_SD & VDDA\_EQ (ADC supply) and VRH\_SD, VRH\_SEQ (ADC reference voltage) pins. It is recommended to do that by installing a jumper connecting J5 (2-3) (5.0V\_SR) to Analog Supply Rail.

## 6. Board Interface Connector

This chapter provides a useful cross reference to see the connection from the motherboard to the board interface connector, and what MCU pins are connected to the interface connector on the daughter card.

[Table 24](#) lists all the connections to the board interface connector on both motherboard and daughter card. The columns on the left lists the 240 connections for J43 & J56

- The column “Daughter Card” shows the 516/416 Daughter card connections to the interface connectors like power supply connections and user area port pins.
- The column “Motherboard” shows the corresponding motherboard connections to the interface connectors like power supply connections and user area port pins.
- Ground signals are not listed here. A solid ground connection is achieved through the middle bar of the interface connector.

Table 249: Board interface connector details

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
Connector IDs ==>	J501A	J56A	
1.25_SR_MB	1	1	1.25V_SR
1.25_SR_MB	2	2	1.25V_SR
1.25_SR_MB	3	3	1.25V_SR
1.25_SR_MB	4	4	1.25V_SR
TCRCLKA	5	5	PA0
x	6	6	PA1
TCRCLKB	7	7	PA2
x	8	8	PA3
TCRCLKC	9	9	PA4
TP28/TP24	10	10	PA5
TP27/TP23	11	11	PA6
TP29/TP25	12	12	PA7
TP25/TP21	13	13	PA8
TP30/TP26	14	14	PA9
CNTXB	15	15	PA10
CNRXB	16	16	PA11
x	17	17	PA12
x	18	18	PA13
TP26/TP22	19	19	PA14
CLK_50MHz_B	20	20	PA15
5.0V_SR_MB	21	21	5.0V_SR
5.0V_SR_MB	22	22	5.0V_SR
5.0V_SR_MB	23	23	5.0V_SR
5.0V_SR_MB	24	24	5.0V_SR
x	25	25	PC0
BOOTCFG0	26	26	PC1
PCSA3	27	27	PC2
PCSB4	28	28	PC3
WKPCFG	29	29	PC4
PLLCFG1	30	30	PC5
BOOTCFG1	31	31	PC6
PLLCFG2	32	32	PC7
MB_CAN_RXD	33	33	PC8
MB_CAN_TXD	34	34	PC9
PCSA4	35	35	PC10
x	36	36	PC11
FEC_RDx0	37	37	PC12

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
FEC_RDY1	38	38	PC13
FEC_TX_EN	39	39	PC14
FEC_TXD0	40	40	PC15
3.3_SR_MB	41	41	3.3V_SR
3.3_SR_MB	42	42	3.3V_SR
3.3_SR_MB	43	43	3.3V_SR
3.3_SR_MB	44	44	3.3V_SR
x	45	45	PE0
x	46	46	PE1
x	47	47	PE2
x	48	48	PE3
x	49	49	PE4
CNTXD	50	50	PE5
MB_LIN_RXD	51	51	PE6
MB_LIN_TXD	52	52	PE7
x	53	53	PE8
x	54	54	PE9
x	55	55	PE10
x	56	56	PE11
FEC_TXD1	57	57	PE12
x	58	58	PE13
x	59	59	PE14
x	60	60	PE15
1.25V_SR_MB	61	61	1.25V_SR
1.25V_SR_MB	62	62	1.25V_SR
1.25V_SR_MB	63	63	1.25V_SR
1.25V_SR_MB	64	64	1.25V_SR
x	65	65	PG0
x	66	66	PG1
x	67	67	PG2
x	68	68	PG3
x	69	69	PG4
CNRXC	70	70	PG5
x	71	71	PG6
CNTXC	72	72	PG7
x	73	73	PG8
x	74	74	PG9
x	75	75	PG10
x	76	76	PG11
x	77	77	PG12
x	78	78	PG13

**Board Interface Connector**

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
CNRXD	79	79	PG14
EMIOS0	80	80	PG15
5.0V_SR_MB	81	81	5.0V_SR
5.0V_SR_MB	82	82	5.0V_SR
5.0V_SR_MB	83	83	5.0V_SR
5.0V_SR_MB	84	84	5.0V_SR
EMIOS1	85	85	PI0
EMIOS2	86	86	PI1
EMIOS3	87	87	PI2
EMIOS4	88	88	PI3
EMIOS5	89	89	PI4
EMIOS6	90	90	PI5
EMIOS7	91	91	PI6
EMIOS8	92	92	PI7
EMIOS9	93	93	PI8
EMIOS10	94	94	PI9
EMIOS11	95	95	PI10
EMIOS12	96	96	PI11
EMIOS13	97	97	PI12
EMIOS14	98	98	PI13
EMIOS15	99	99	PI14
EMIOS16	100	100	PI15
x	101	101	x
x	102	102	x
x	103	103	x
x	104	104	x
EMIOS17	105	105	PK0
EMIOS18	106	106	PK1
EMIOS19	107	107	PK2
EMIOS20	108	108	PK3
EMIOS21	109	109	PK4
EMIOS22	110	110	PK5
EMIOS23	111	111	PK6
EMIOS24	112	112	PK7
EMIOS25	113	113	PK8
EMIOS26	114	114	PK9
EMIOS27	115	115	PK10
EMIOS28	116	116	PK11
EMIOS29	117	117	PK12
EMIOS30	118	118	PK13
PK_14	119	119	PK14

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
PCSB2	120	120	PK15
<b>connector IDs ==&gt;</b>	<b>J501B</b>	<b>J56B</b>	
5.0V_LR	121	121	5.0V_LR
5.0V_LR	122	122	5.0V_LR
5.0V_LR	123	123	5.0V_LR
5.0V_LR	124	124	5.0V_LR
FEC_RX_DV	125	125	PM0
PCSB5	126	126	PM1
PCSA1	127	127	PM2
PM3	128	128	PM3
PM4	129	129	PM4
PCSA5	130	130	PM5
SCKA	131	131	PM6
SINA	132	132	PM7
SOUTA	133	133	PM8
PCSB1	134	134	PM9
PCSB0	135	135	PM10
PCSB3	136	136	PM11
EMIOS31	137	137	PM12
PCSA0	138	138	PM13
PLLCFG0	139	139	PM14
SINB	140	140	PM15
RST-SW_B	141	141	RST-SW
x	142	142	VDD_HV_IO_FLEX
x	143	143	VDD_HV_IO_FLEX
x	144	144	VDD_HV_IO_FLEX
SCKB	145	145	PO0
PCSC0	146	146	PO1
SOUTB	147	147	PO2
PCSC2	148	148	PO3
PCSC1	149	149	PO4
PCSC4	150	150	PO5
PCSC3	151	151	PO6
SCKC	152	152	PO7
PCSC5	153	153	PO8
SOUTC	154	154	PO9
SINC	155	155	PO10
x	156	156	PO11
x	157	157	PO12
x	158	158	PO13

**Board Interface Connector**

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
x	159	159	PO14
ANA0_SDA0	160	160	PO15
1.25_SR_MB	161	161	1.25V_SR
1.25_SR_MB	162	162	1.25V_SR
1.25_SR_MB	163	163	1.25V_SR
1.25_SR_MB	164	164	1.25V_SR
ANA1_SDA1	165	165	PQ0
ANA2_SDA2	166	166	PQ1
ANA3_SDA3	167	167	PQ2
ANA4	168	168	PQ3
ANA5	169	169	PQ4
ANA6	170	170	PQ5
ANA7	171	171	PQ6
ANA8	172	172	PQ7
ANA9	173	173	PQ8
ANA10	174	174	PQ9
ANA11	175	175	PQ10
ANA12	176	176	PQ11
ANA13	177	177	PQ12
ANA14	178	178	PQ13
ANA15	179	179	PQ14
ANA16_SDB0	180	180	PQ15
5.0_SR_MB	181	181	5.0V_SR
5.0_SR_MB	182	182	5.0V_SR
5.0_SR_MB	183	183	5.0V_SR
5.0_SR_MB	184	184	5.0V_SR
ANA17_SDB1	185	185	PS0
ANA18_SDB2	186	186	PS1
ANA19_SDB3	187	187	PS2
ANA20_SDC0	188	188	PS3
ANA21_SDC1	189	189	PS4
ANA22_SDC2	190	190	PS5
ANA23_SDC3	191	191	PS6
AN24	192	192	PS7
AN25	193	193	PS8
AN26	194	194	PS9
AN27	195	195	PS10
AN28	196	196	PS11
AN29	197	197	PS12
AN30	198	198	PS13
AN31	199	199	PS14

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
AN32	200	200	PS15
3.3V_SR_MB	201	201	3.3V_SR
3.3V_SR_MB	202	202	3.3V_SR
3.3V_SR_MB	203	203	3.3V_SR
3.3V_SR_MB	204	204	3.3V_SR
AN33	205	205	PU0
AN34	206	206	PU1
AN35	207	207	PU2
AN36	208	208	PU3
AN37	209	209	PU4
AN38	210	210	PU5
AN39	211	211	PU6
ANB0_SDD0	212	212	PU7
ANB1_SDD1	213	213	PU8
ANB2_SDD2	214	214	PU9
ANB3_SDD3	215	215	PU10
ANB4_SDD4	216	216	PU11
ANB5_SDD5	217	217	PU12
ANB6_SDD6	218	218	PU13
ANB7_SDD7	219	219	PU14
ANB8	220	220	PU15
VDD_HV_IO_MAIN	221	221	VDD_HV_IO_MAIN
VDD_HV_IO_MAIN	222	222	VDD_HV_IO_MAIN
VDD_HV_IO_MAIN	223	223	VDD_HV_IO_MAIN
VDD_HV_IO_MAIN	224	224	VDD_HV_IO_MAIN
ANB9	225	225	PW0
ANB10	226	226	PW1
ANB11	227	227	PW2
ANB12	228	228	PW3
ANB13	229	229	PW4
ANB14	230	230	PW5
ANB15	231	231	PW6
ANB16	232	232	PW7
ANB17	233	233	PW8
ANB18	234	234	PW9
ANB19	235	235	PW10
ANB20	236	236	PW11
ANB21	237	237	PW12
ANB22	238	238	PW13
ANB23	239	239	PW14
SENT2_A	240	240	PW15

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
Connector IDs ==>	J500A	J43A	
5.0V_LR	120	120	5.0V_LR
5.0V_LR	119	119	5.0V_LR
5.0V_LR	118	118	5.0V_LR
5.0V_LR	117	117	5.0V_LR
ETPUA1	116	116	PN0
ETPUA0	115	115	PN1
ETPUA3	114	114	PN2
ETPUA2	113	113	PN3
ETPUA5	112	112	PN4
ETPUA4	111	111	PN5
ETPUA7	110	110	PN6
ETPUA6	109	109	PN7
ETPUA9	108	108	PN8
ETPUA8	107	107	PN9
ETPUA11	106	106	PN10
ETPUA10	105	105	PN11
ETPUA13	104	104	PN12
ETPUA12	103	103	PN13
ETPUA15	102	102	PN14
ETPUA14	101	101	PN15
x	100	100	x
x	99	99	x
x	98	98	x
x	97	97	x
ETPUA17	96	96	PP0
ETPUA16	95	95	PP1
ETPUA19	94	94	PP2
ETPUA18	93	93	PP3
ETPUA21	92	92	PP4
ETPUA20	91	91	PP5
ETPUA23	90	90	PP6
ETPUA22	89	89	PP7
ETPUA25	88	88	PP8
ETPUA24	87	87	PP9
ETPUA27	86	86	PP10
ETPUA26	85	85	PP11
ETPUA29	84	84	PP12
ETPUA28	83	83	PP13
ETPUA31	82	82	PP14



Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
ETPUA30	81	81	PP15
1.25_SR_MB	80	80	1.25V_SR
1.25_SR_MB	79	79	1.25V_SR
1.25_SR_MB	78	78	1.25V_SR
1.25_SR_MB	77	77	1.25V_SR
ETPUB1	76	76	PR0
ETPUB0	75	75	PR1
ETPUB3	74	74	PR2
ETPUB2	73	73	PR3
ETPUB5	72	72	PR4
ETPUB4	71	71	PR5
ETPUB7	70	70	PR6
ETPUB6	69	69	PR7
ETPUB9	68	68	PR8
ETPUB8	67	67	PR9
ETPUB11	66	66	PR10
ETPUB10	65	65	PR11
ETPUB13	64	64	PR12
ETPUB12	63	63	PR13
ETPUB15	62	62	PR14
ETPUB14	61	61	PR15
5.0V_SR_MB	60	60	5.0V_SR
5.0V_SR_MB	59	59	5.0V_SR
5.0V_SR_MB	58	58	5.0V_SR
5.0V_SR_MB	57	57	5.0V_SR
ETPUB17	56	56	PT0
ETPUB16	55	55	PT1
ETPUB19	54	54	PT2
ETPUB18	53	53	PT3
ETPUB21	52	52	PT4
ETPUB20	51	51	PT5
ETPUB23	50	50	PT6
ETPUB22	49	49	PT7
ETPUB25	48	48	PT8
ETPUB24	47	47	PT9
ETPUB27	46	46	PT10
ETPUB26	45	45	PT11
ETPUB29	44	44	PT12
ETPUB28	43	43	PT13
ETPUB31	42	42	PT14
ETPUB30	41	41	PT15

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
3.3V_SR_MB	40	40	3.3V_SR
3.3V_SR_MB	39	39	3.3V_SR
3.3V_SR_MB	38	38	3.3V_SR
3.3V_SR_MB	37	37	3.3V_SR
ETPUC1	36	36	PV0
ETPUC0	35	35	PV1
ETPUC3	34	34	PV2
ETPUC2	33	33	PV3
ETPUC5	32	32	PV4
ETPUC4	31	31	PV5
ETPUC7	30	30	PV6
ETPUC6	29	29	PV7
ETPUC9	28	28	PV8
ETPUC8	27	27	PV9
ETPUC11	26	26	PV10
ETPUC10	25	25	PV11
ETPUC13	24	24	PV12
ETPUC12	23	23	PV13
ETPUC15	22	22	PV14
ETPUC14	21	21	PV15
VDD_HV_IO_MAIN	20	20	VDD_HV_IO_MAIN
VDD_HV_IO_MAIN	19	19	VDD_HV_IO_MAIN
VDD_HV_IO_MAIN	18	18	VDD_HV_IO_MAIN
VDD_HV_IO_MAIN	17	17	VDD_HV_IO_MAIN
ETPUC17	16	16	PX0
ETPUC16	15	15	PX1
ETPUC19	14	14	PX2
ETPUC18	13	13	PX3
ETPUC21	12	12	PX4
ETPUC20	11	11	PX5
ETPUC23	10	10	PX6
ETPUC22	9	9	PX7
ETPUC25	8	8	PX8
ETPUC24	7	7	PX9
ETPUC27	6	6	PX10
ETPUC26	5	5	PX11
ETPUC29	4	4	PX12
ETPUC28	3	3	PX13
ETPUC31	2	2	PX14
ETPUC30	1	1	PX15

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
Connector IDs ==>	J500B	J43B	
1.25V_SR_MB	240	240	1.25_SR
1.25V_SR_MB	239	239	1.25_SR
1.25V_SR_MB	238	238	1.25_SR
1.25V_SR_MB	237	237	1.25_SR
x	236	236	PB0
x	235	235	PB1
x	234	234	PB2
x	233	233	PB3
x	232	232	PB4
x	231	231	PB5
x	230	230	PB6
x	229	229	PB7
x	228	228	PB8
x	227	227	PB9
x	226	226	PB10
x	225	225	PB11
x	224	224	PB12
x	223	223	PB13
x	222	222	PB14
x	221	221	PB15
5.0V_SR_MB	220	220	5.0V_SR
5.0V_SR_MB	219	219	5.0V_SR
5.0V_SR_MB	218	218	5.0V_SR
5.0V_SR_MB	217	217	5.0V_SR
x	216	216	PD0
x	215	215	PD1
x	214	214	PD2
D_CS3	213	213	PD3
x	212	212	PD4
x	211	211	PD5
TP11	210	210	PD6
TP10/TP9	209	209	PD7
x	208	208	PD8
x	207	207	PD9
D_TA	206	206	PD10
x	205	205	PD11
x	204	204	PD12
x	203	203	PD13
TXDC	202	202	PD14

**Board Interface Connector**

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
RXDC	201	201	PD15
3.3V_SR_MB	200	200	3.3V_SR
3.3V_SR_MB	199	199	3.3V_SR
3.3V_SR_MB	198	198	3.3V_SR
3.3V_SR_MB	197	197	3.3V_SR
x	196	196	PF0
x	195	195	PF1
x	194	194	PF2
x	193	193	PF3
x	192	192	PF4
x	191	191	PF5
x	190	190	PF6
x	189	189	PF7
x	188	188	PF8
x	187	187	PF9
x	186	186	PF10
x	185	185	PF11
x	184	184	PF12
TP8/TP10	183	183	PF13
x	182	182	PF14
x	181	181	PF15
1.25V_SR_MB	180	180	1.25V_SR
1.25V_SR_MB	179	179	1.25V_SR
1.25V_SR_MB	178	178	1.25V_SR
1.25V_SR_MB	177	177	1.25V_SR
x	176	176	PH0
x	175	175	PH1
x	174	174	PH2
x	173	173	PH3
x	172	172	PH4
x	171	171	PH5
x	170	170	PH6
x	169	169	PH7
x	168	168	PH8
x	167	167	PH9
x	166	166	PH10
x	165	165	PH11
x	164	164	PH12
x	163	163	PH13
x	162	162	PH14
x	161	161	PH15

Daughter Card		Mother Board	
mP Pin Name(516/416)	Connector Pin #	Connector Pin #	Evaluation Board Port
3.3V_SR_MB	160	160	3.3V_SR
3.3V_SR_MB	159	159	3.3V_SR
3.3V_SR_MB	158	158	3.3V_SR
3.3V_SR_MB	157	157	3.3V_SR
x	156	156	PJ0
x	155	155	PJ1
x	154	154	PJ2
x	153	153	PJ3
x	152	152	PJ4
TP6	151	151	PJ5
x	150	150	PJ6
TP9/TP8	149	149	PJ7
x	148	148	PJ8
x	147	147	PJ9
x	146	146	PJ10
x	145	145	PJ11
x	144	144	PJ12
x	143	143	PJ13
x	142	142	PJ14
x	141	141	PJ15
x	140	140	x
x	139	139	x
x	138	138	x
x	137	137	x
x	136	136	PL0
x	135	135	PL1
x	134	134	PI2
x	133	133	PL3
x	132	132	PL4
x	131	131	PL5
x	130	130	PL6
x	129	129	PL7
x	128	128	PL8
TP7	127	127	PL9
x	126	126	PL10
TP3	125	125	PL11
x	124	124	PL12
TP4	123	123	PL13
x	122	122	PL14
TP5	121	121	PL15

Some of the port pins on the mother board share functionality with other peripherals like communication interfaces. [Table](#) shows what port pins are used for peripherals on the motherboard.

**Table 30: Port pins alternate function - on motherboard**

Port Pin	Function	Port Pin	Function
PC2	FEC MDIO	PE9	Unused
PC3	FEC MDC	PE10	Unused
PC8	RX MCAN2	PE11	Unused
PC9	TX MCAN2	PE12	Unused
PC10	FEC RXCLK	PF14	DRCLK (SIPI)
PC11	FEC CRS_LEDG	PF15	EVTI/EVTO (JTAG)
PC12	FEC RXD0	PG14	RX TTCAN
PC13	FEC RXD1	PH3	Unused
PC14	FEC TXEN	PH4	Unused
PC15	FEC TXD0	PH7	Unused
PD14	TXD eSCI/LINFlex_2	PH8	Unused
PD15	RXD eSCI/LINFlex_2	PH9	Unused
PE5	TX TTCAN	PH10	Unused
PE6	RX LINFlexD_1	PL3	TX MCAN1
PE7	TX LINFlexD_1	PL4	RX MCAN1

Some of the port pins of the MCU share functionality with a peripheral that is used on the daughter card and these pins might not be routed to the motherboard. [Table 25](#) lists port pins that are not routed to the motherboard and shows what they are used for on the daughter card.

**Table 251: Port pins alternate function — not on motherboard**

Port Pin	Function	Port Pin	Function
PA5	JCOMP	PK14	Nexus EVT11
PA6	TCK	PL9	Nexus TX1N
PA7	TMS	PL11	Nexus TX1P
PA8	TDI	PL13	Nexus TX0N
PA9	TDO	PL15	Nexus TX0P
PA14	SIPI_TXP	PM4	Nexus EVT10
PD6	SIPI_TXN	PM5	Nexus EVTO0
PD7	SIPI_RXP	PM6	Nexus EVTO1
PF13	SIPI_RXN	—	Nexus TX2N
PJ6	Nexus CLKP	—	Nexus TX2P
PJ7	Nexus CLKN	—	Nexus TX3N
		—	Nexus TX3P

## 7. Default Jumper Summary Table

The following table details the DEFAULT jumper configuration of the EVB as set up on delivery.

### 7.1 Default Jumper Table - Motherboard

On delivery the motherboard comes with a default jumper configuration. [Table 26](#) lists and describes briefly the jumpers on the MPC57xx motherboard and indicates which jumpers are on/off on delivery of the board.

**Table 262: Default Jumper Table-Motherboard**

Jumper	Default	PCB Legend	Description
J8	On	MASTER	LIN Master/Slave select
J9	On	CAP A DIS	Disable capacitor circuitry for FlexRAY_A signals
J10	On	CAP A DIS	Disable capacitor circuitry for FlexRAY_A signals
J11	On	CAP B DIS	Disable capacitor circuitry for FlexRAY_B signals
J12	On	CAP B DIS	Disable capacitor circuitry for FlexRAY_B signals
J13	On	SCI TX	1-2: Connect SCI TX signal
J14	On	SCI RX	1-2: Connect SCI RX signal
J15	On	LIN_EN	1-2: Enable LIN PHY U50
J16	On	LIN_RX	1-2: Connect LIN RX signal
J17	On	LIN_TX	1-2: Connect LIN TX signal
J18	On	—	1-2: Ethernet signal: RXCLK
J20	On	—	Ethernet signal: CRS_LEDCFG
J21	On	CAN2_EN	PHY U2 configuration:
			1-2: WAKE to GND
			3-4: STB to 5V
			5-6: EN to 5V
J22	On	—	Ethernet PHY power-on
J23	On	CAN-EN	PHY U1 configuration:
			1-2: WAKE to GND
			3-4: STB to 5V
			5-6: EN to 5V
J24	On	—	1-2: Ethernet signal: RXER_MDIXEN
J25	On	SCI-PWR	1-2: SCI PHY power-on
J26	On	—	1-2: Ethernet signal: RXDV_MIIMODE
J27	On	FR-A	1-2: PHY U4 TX to MCU
			3-4: PHY U4 TXEN to MCU
			5-6: PHY U4 RX to MCU

## Default Jumper Table – Mother Board

Jumper	Default	PCB Legend	Description
J28	On	FR-A	PHY U4 configuration:
			1-2: 3.3V (VIO) to BGE
			3-4: 3.3V (VIO) to EN
			5-6: 3.3V (VIO) to STBY
			7-8: GND to WAKE
J29	On	FR_PWR	Unused
			1-2: 12V to VBAT
			3-4: 5V_SR to VCC and VBUF
			5-6 : VDD_HV_IO_FLEX to FR-VIO
J30	On	FR_B	1-2: PHY U5 TX to MCU
			3-4: PHY U5 TXEN to MCU
			5-6: PHY U5 RX to MCU
J31	On	FR_B	PHY U5 configuration:
			1-2: 3.3V (VIO) to BGE
			3-4: 3.3V (VIO) to EN
			5-6: 3.3V (VIO) to STBY
			7-8: GND to WAKE
J32	On	CAN2	1-2: PHY TX to MCU
			3-4: WAKE to GND
J33	On	CAN-PWR	1-2: 5V_SR to PHY U2 VCC
			3-4: 12V to PHY U2 VBAT
J34	Off	—	MCAN2 signal out:
			1: ERR
			2: INH
J35	On	CAN	1-2: 5V_SR to PHY U1 VCC
			3-4: 12V to PHY U1 VBAT
J36	Off	—	CAN PHY U1 signal out
J37	On	—	1-2: CAN TX connect
J38	On	—	1-2: CAN RX connect
J39	On	—	Ethernet signal: RXD0_PHYAD1
J40	On	—	Ethernet signal: RXD1_PHYAD1
J41	On	—	Ethernet signal: RXD2_PHYAD2
J42	On	—	Ethernet signal: RXD3_PHYAD3
J44	On	—	Ethernet signal: COL_PHYAD0
J45	On	—	Ethernet signal: TXEN
J46	On	—	Ethernet signal: TXCLK
J47	On	—	Ethernet signal: TXD0
J48	On	—	Ethernet signal: TXD1



## Default Jumper Table – Mother Board

Jumper	Default	PCB Legend	Description
J49	On	—	Ethernet signal: TXD2
J50	On	—	Ethernet signal: TXD3_SNIMODE
J51	On	—	Ethernet signal: MDC
J52	On	—	Ethernet signal: MDIO
J53	Off	RV1	Connect RV1 to analog input AN0
J54	Off	ADC_VSUP	Connect EVB supply voltages to analog inputs
J55	Off	12V (4.3V)	Connect 12V (scaled to 4.3V) EVB power to analog input
J57	On	ENABLE	Enable 5V linear regulator
J58	Off	DISABLE	Disable 1.25V switching regulator
J59	Off	DISABLE	Disable 3.3V switching regulator
J60	Off	DISABLE	Disable 5.0V switching regulator
J61	On	—	1-2: PM0 to GND
J62	On	—	1-2: RST-SW
J63	On	—	1-2 : QZ1-X1 connect
J64	On	—	1-2: QZ1-X2 connect

## 8. List of Acronyms

**Table 273: List of Acronyms**

<b>Acronym</b>	<b>Description</b>
1.25V_SR	Supply voltage from the 1.25V switching regulator
3.3V_SR	Supply voltage from the 3.3V switching regulator
5V_LR	Supply voltage from the 5.0V linear regulator
5V_SR	Supply voltage from the 5.0V switching regulator
ADC	Analog-to-Digital converter
CAN	Controller Area Network
EBI	External Bus Interface
ESR0	External signal reset
EVB	Evaluation Board
FEC	Fast Ethernet controller module
GND	Ground
HV	High voltage (3.3V and/or 5V)
LED	Light emitting diode
LIN	Local Interconnect Network
LV	Low voltage (1.25V)
MB	Mother Board
MCU	Microcontroller
MII	Media Independent Interface
OSC	Oscillator
P12V	12 V EVB supply power domain
PCB	Printed Circuit Board
PORST	Power-on reset
PWR	Power
RMII	Reduced Media-Independent Interface
RX	Receive
SBC	System Basis Chip
TBD	To be defined
TP	Test Point
TX	Transmit
USB	Universal Serial Bus
VSS	Ground

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