NXP Semiconductors
Data Sheet: Technical Data

Document Number: MPC5777M
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MPC5777M

416 TEPBGA
27mm x 27 mm

512 TEPBGA
25 mm x 25 mm

MPC5777M Microcontroller Data Sheet

- Three main CPUs, single issue, 32-bit CPU core complexes (e200z7), one of which is a dedicated lockstep core.
  - Power Architecture® embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - 16 KB Local instruction RAM and 64 KB local data RAM
  - 16 KB I-Cache and 4 KB D-Cache
- I/O Processor, dual issue, 32-bit CPU core complex (e200z4), with
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
  - Lightweight Signal Processing Auxiliary Processing Unit (LSP APU) instruction support for digital signal processing (DSP)
  - 16 KB Local instruction RAM and 64 KB local data RAM
  - 8 KB I-Cache
- 8640 KB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 404 KB on-chip general-purpose SRAM including 64 KB standby RAM (+ 192 KB data RAM included in the CPUs). Of this 404 KB, 64 KB can be powered by a separate supply so the contents of this portion can be preserved when the main MCU is powered down.
- Multichannel direct memory access controllers (eDMA): 2 x 64 channels per eDMA (128 channels total)
- Triple Interrupt controller (INTC)
  - Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Dual crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters with end-to-end ECC
- Hardware Security Module (HSM) to provide robust integrity checking of flash memory
- System Integration Unit Lite (SIUL)
- Boot Assist Module (BAM) supports factory programming using serial bootload through ‘UART Serial Boot Mode Protocol’. Physical interface (PHY) can be:
  - UART/LIN
  - CAN
- GTM104 — generic timer module
- Enhanced analog-to-digital converter system with
  - Twelve separate 12-bit SAR analog converters
  - Ten separate 16-bit Sigma-Delta analog converters
- Eight deserial serial peripheral interface (DSPI) modules
- Two Peripheral Sensor Interface (PSI5) controllers
- Three LIN and three UART communication interface (LINFlexD) modules (6 total)
  - LINFlexD_0 is a Master/Slave
  - LINFlexD_1, LINFlexD_2, LINFlexD_14, LINFlexD_15, and LINFlexD_16 are Masters
- Four modular controller area network (MCAN) modules and one time-triggered controller area network (M-TTCAN)
- External Bus Interface (EBI)
  - Dual routing of accesses to EBI
  - Access path determined by access address
  - Access path downstream of PFLASH controller
    - Allows EBI accesses to share buffer and prefetch capabilities of internal flash
    - Allows internal flash accesses to be remapped to memories connected to EBI

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  - Access path via dedicated AXBS slave port
    - Avoids contention with other memory accesses
- Two Dual-channel FlexRay controllers
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- Self-test capability

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5777M series of microcontroller units (MCUs). For functional characteristics, see the *MPC5777M Microcontroller Reference Manual*.

1.2 Description

This family of MCUs is targeted at automotive powertrain controller and chassis control applications from single cylinder motorcycles at the very bottom end; through 4 to 8 cylinder gasoline and diesel engines; transmission control; steering and breaking applications; to high end hybrid and advanced combustion systems at the top end.

Many of the applications are considered to be functionally safe and the family is designed to achieve ISO26262 ASIL-D compliance.

1.3 Device feature

Table 1. MPC5777M feature

Feature		MPC5777M
Process		55 nm
Main processor	Core	e200z7
	Number of main cores	2
	Number of checker cores	1
	Local RAM (per main core)	16 KB Instruction 64 KB Data
	Single precision floating point	Yes
	LSP	No
	VLE	Yes
	Cache	16 KB Instruction 4 KB Data
I/O processor	Core	e200z4
	Local RAM	16 KB instruction 64 KB Data
	Single precision floating point	Yes
	LSP	Yes
	VLE	Yes
	Cache	8 KB instruction
Main processor frequency		300 MHz[1]
I/O processor frequency		200 MHz
MMU entries		0
MPU		Yes
Semaphores		Yes

Table 1. MPC5777M feature (continued)

Feature	MPC5777M
CRC channels	2
Software watchdog timer (Task SWT/Safety SWT)	4 (3/1)
Core Nexus class	3+
Sequence processing unit (SPU)	Yes
Debug and calibration interface (DCI) / run control module	Yes
System SRAM	404 KB
Flash memory	8640 KB
Flash memory fetch accelerator	4 × 256 bit
Data flash memory (EEPROM)	8 × 64 KB + 2 × 16 KB
Flash memory overlay RAM	16 KB
External bus	32 bit
Calibration interface	64-bit IPS Slave
DMA channels	2 × 64
DMA Nexus Class	3+
LINFlex (UART/MSC)	6 (3/3)
MCAN/TTCAN	4/1
DSPI (SPI/MSC/sync SCI)	8 (4/3/1)
Microsecond bus downlink	Yes
SENT bus	15
I^2C	2
PSI5 bus	5
PSI5-S UART-to-PSI5 interface	Yes
FlexRay	2 × dual channel
Ethernet	MII / RMII
Zipwire® (SIPI / LFAST[2]) Interprocessor Communication Interface	High speed
System timers	8 PIT channels 3 AUTOSAR® (STM) 64-bit PIT
BOSCH® GTM Timer[3]	Yes
GTM RAM	58 KB
Interrupt controller	727 sources
ADC (SAR)	12

Table 1. MPC5777M feature (continued)

Feature	MPC5777M
ADC (SD)	10
Temperature sensor	Yes
Self test controller	Yes
PLL	Dual PLL with FM
Integrated linear voltage regulator	None
External power supplies	5 V 3.3 V[7] 1.2 V
Low-power modes	Stop mode Slow mode
Packages	• 416 TEPBGA[4] • 512 TEPBGA[5]

1 Includes four user-programmable CPU cores and one safety core. The main computational shell consists of dual e200z7 CPUs operating at 300 MHz with a third identical core running as a safety checker core in delayed lockstep mode with one of the dual e200z7 cores. The I/O subsystem includes a CPU targeted at managing the peripherals. This is an e200z4 CPU running at 200 MHz. The fifth CPU is an e200z0 running at 100 MHz and is embedded in the Hardware Security Module. All CPUs are compatible with the Power Architecture.

2 LVDS Fast Asynchronous Serial Transmission

3 BOSCH® is a registered trademark of Robert Bosch GmbH.

4 416 TEPBGA package supports development and production applications with the same package footprint.

5 512 TEPBGA package supports development and production applications with the same package footprint.

1.4 Block diagram

The figures below show the top-level block diagrams.

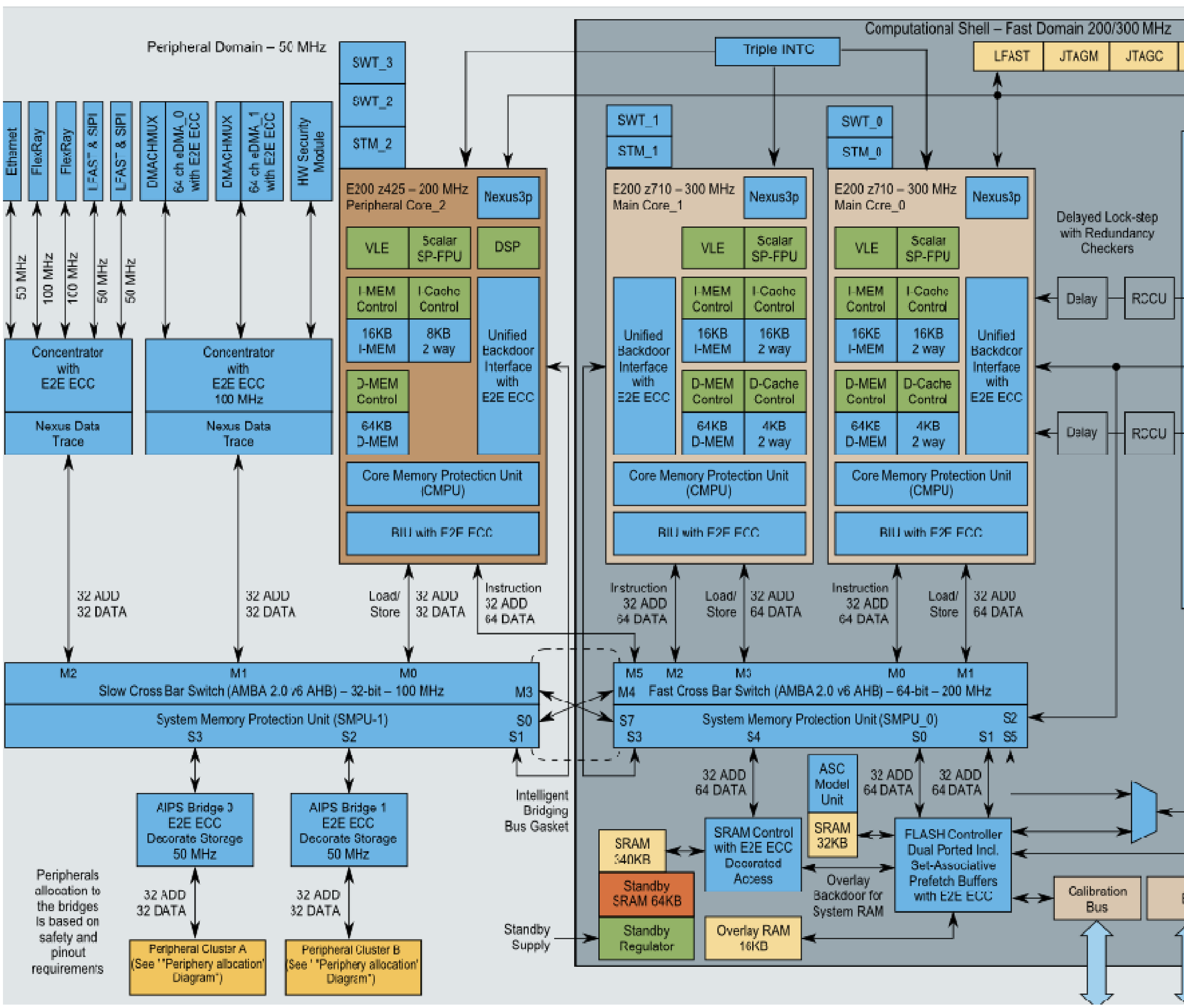


Figure 1. Block diagram

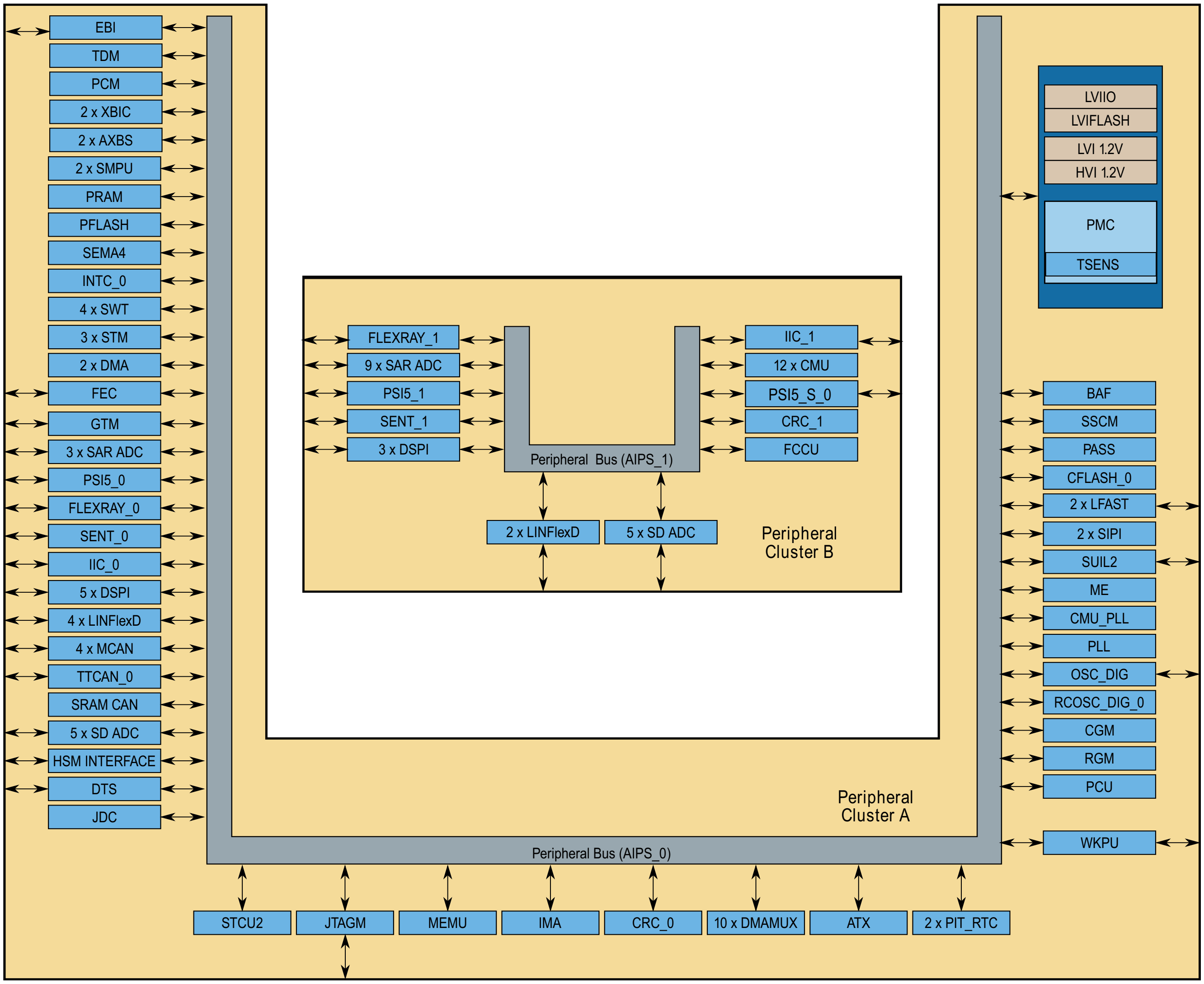


Figure 2. Periphery allocation

2 Package pinouts and signal descriptions

See the *MPC5777M Microcontroller Reference Manual* for signal information.

2.1 Package pinouts

The BGA ballmap package pinouts for the 416 and 512 production and emulation devices are shown in the following figures.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	NC	PX[0]	PN[0]	PH[12]	PC[15]	PF[3]	PF[5]	PH[14]	PH[15]	PK[15]	PM[8]	PX[2]	PQ[14]	PH[9]	PQ[4]	PQ[10]	PQ[9]	VDD_HV_ FLA	PQ[3]	PH[0]	PA[0]	PA[4]
B	PD[15]	PD[14]	PM[15]	PH[13]	PC[13]	PM[11]	PM[10]	PF[4]	PM[3]	PK[14]	PM[7]	PQ[15]	PX[1]	PQ[7]	PQ[6]	PQ[11]	PQ[8]	VDD_HV_ FLA	PQ[5]	PM[9]	PA[12]	PORST
C	PC[7]	PL[2]	PM[14]	PM[12]	PC[10]	PC[14]	PM[2]	PM[0]	PM[1]	PM[6]	PM[4]	PQ[13]	PH[4]	PE[10]	PH[7]	PD[0]	PD[3]	PD[2]	PH[8]	PH[3]	PA[10]	PA[1]
D	PN[2]	PN[4]	PN[1]	PC[6]	PC[12]	PC[11]	VDD_HV_ IO_FLEX	VSS_HV	VDD_LV	PE[12]	PM[5]	PH[10]	PE[11]	VDD_HV_ PMC	VSS_HV	PH[1]	PD[1]	PA[13]	PG[15]	PH[2]	PA[11]	VDD_HV_ IO_MAIN
E	PN[3]	PC[9]	PL[7]	PL[1]																		
F	PN[5]	PC[8]	PL[6]	PL[0]																		
G	PN[7]	PF[2]	PL[3]	PL[5]																		
H	PC[4]	PC[5]	PL[4]	VDD_LV																		
J	PN[9]	PN[6]	PC[3]	VSS_HV																		
K	PN[11]	PN[10]	PN[8]	VDD_HV_ IO_MAIN						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
L	PN[15]	PN[14]	PN[13]	PN[12]						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
M	PE[0]	PC[0]	PC[1]	PC[2]						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
N	PG[0]	PE[4]	PE[2]	PE[1]						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
P	PI[9]	PI[8]	PQ[1]	PQ[2]						NC	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	NC					
R	NC	PQ[0]	PD[12]	NC						NC	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	NC					
T	PK[1]	PE[3]	PD[13]	VSS_HV						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
U	PK[0]	PR[14]	PK[2]	PK[3]						NC	NC	NC	NC	NC	NC	NC	NC					
V	PR[15]	PR[12]	PB[13]	PB[12]																		
W	PR[13]	PR[10]	PI[1]	VDD_HV_ ADR_D																		
Y	PR[11]	PR[8]	PI[0]	VSS_HV_ ADR_D																		
AA	PR[9]	PI[5]	PE[13]	PR[6]																		
AB	PI[3]	PI[4]	PR[7]	PE[14]																		
AC	PI[2]	PD[11]	PG[8]	PE[15]	PB[0]	VSS_HV_ ADR_D2	PG[6]	PB[6]	PL[9]	PL[10]	PI[13]	PF[1]	PL[14]	PA[15]	PD[10]	VDD_HV_ IO_MAIN	PF[7]	VDD_HV_ IO_FLEXE	VSS_HV	VDD_LV	NC	VDD_HV_ IO_FLEXE
AD	PB[4]	PR[0]	PG[7]	PK[10]	PB[1]	VDD_HV_ ADR_D2	PG[5]	PB[7]	VDDSTBY	PL[12]	PI[12]	PF[0]	PL[15]	PJ[6]	PB[11]	VDD_HV_ IO_MAIN	PF[6]	PS[0]	PS[3]	PS[6]	PS[9]	PS[12]
AE	PR[1]	PI[7]	PG[12]	PB[2]	VDD_HV_ ADV_D	PR[2]	PR[4]	VSS_HV_ ADR_S	VDD_HV_ ADV_S	PL[13]	PI[11]	PD[9]	PJ[0]	PB[9]	PD[8]	VDD_HV_ IO_MAIN	PJ[7]	PS[1]	PS[4]	PS[7]	PS[10]	PS[13]
AF	NC	PI[6]	PG[11]	PB[3]	VSS_HV_ ADV_D	PR[3]	PR[5]	VDD_HV_ ADR_S	VSS_HV_ ADV_S	PL[11]	PI[10]	PB[10]	PJ[1]	PB[8]	PA[3]	VDD_HV_ IO_MAIN	PJ[5]	PS[2]	PS[5]	PS[8]	PS[11]	PT[0]
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

Figure 3. 416-ball BGA production device pinout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	NC	PX[0]	PN[0]	PH[12]	PC[15]	PF[3]	PF[5]	PH[14]	PH[15]	PK[15]	PM[8]	PX[2]	PQ[14]	PH[9]	PQ[4]	PQ[10]	PQ[9]	VDD_HV_FLA	PQ[3]	PH[0]	PA[0]	PA[4]
B	PD[15]	PD[14]	PM[15]	PH[13]	PC[13]	PM[11]	PM[10]	PF[4]	PM[3]	PK[14]	PM[7]	PQ[15]	PX[1]	PQ[7]	PQ[6]	PQ[11]	PQ[8]	VDD_HV_FLA	PQ[5]	PM[9]	PA[12]	PORST
C	PC[7]	PL[2]	PM[14]	PM[12]	PC[10]	PC[14]	PM[2]	PM[0]	PM[1]	PM[6]	PM[4]	PQ[13]	PH[4]	PE[10]	PH[7]	PD[0]	PD[3]	PD[2]	PH[8]	PH[3]	PA[10]	PA[1]
D	PN[2]	PN[4]	PN[1]	PC[6]	PC[12]	PC[11]	VDD_HV_IO_FLEX	VSS_HV	VDD_LV	PE[12]	PM[5]	PH[10]	PE[11]	VDD_HV_PMC	VSS_HV	PH[1]	PD[1]	PA[13]	PG[15]	PH[2]	PA[11]	VDD_HV_IO_MAIN
E	PN[3]	PC[9]	PL[7]	PL[1]																		
F	PN[5]	PC[8]	PL[6]	PL[0]																		
G	PN[7]	PF[2]	PL[3]	PL[5]																		
H	PC[4]	PC[5]	PL[4]	VDD_LV																		
J	PN[9]	PN[6]	PC[3]	VSS_HV																		
K	PN[11]	PN[10]	PN[8]	VDD_HV_IO_MAIN						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
L	PN[15]	PN[14]	PN[13]	PN[12]						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
M	PE[0]	PC[0]	PC[1]	PC[2]						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
N	PG[0]	PE[4]	PE[2]	PE[1]						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
P	PI[9]	PI[8]	PQ[1]	PQ[2]						TX3P	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_HV_IO_BD					
R	VDD_LV_BD	PQ[0]	PD[12]	VDD_LV_BD						TX3N	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	NC					
T	PK[1]	PE[3]	PD[13]	VSS_HV						VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV					
U	PK[0]	PR[14]	PK[2]	PK[3]						TX2N	TX2P	TX1N	TX1P	TX0N	TX0P	CLKN	CLKP					
V	PR[15]	PR[12]	PB[13]	PB[12]																		
W	PR[13]	PR[10]	PI[1]	VDD_HV_ADR_D																		
Y	PR[11]	PR[8]	PI[0]	VSS_HV_ADR_D																		
AA	PR[9]	PI[5]	PE[13]	PR[6]																		
AB	PI[3]	PI[4]	PR[7]	PE[14]																		
AC	PI[2]	PD[11]	PG[8]	PE[15]	PB[0]	VSS_HV_ADR_D2	PG[6]	PB[6]	PL[9]	PL[10]	PI[13]	PF[1]	PL[14]	PA[15]	PD[10]	VDD_HV_IO_MAIN	PF[7]	VDD_HV_IO_FLEXE	VSS_HV	VDD_LV	NC	VDD_HV_IO_FLEXE
AD	PB[4]	PR[0]	PG[7]	PK[10]	PB[1]	VDD_HV_ADR_D2	PG[5]	PB[7]	VDDSTBY	PL[12]	PI[12]	PF[0]	PL[15]	PJ[6]	PB[11]	VDD_HV_IO_MAIN	PF[6]	PS[0]	PS[3]	PS[6]	PS[9]	PS[12]
AE	PR[1]	PI[7]	PG[12]	PB[2]	VDD_HV_ADV_D	PR[2]	PR[4]	VSS_HV_ADR_S	VDD_HV_ADV_S	PL[13]	PI[11]	PD[9]	PJ[0]	PB[9]	PD[8]	VDD_HV_IO_MAIN	PJ[7]	PS[1]	PS[4]	PS[7]	PS[10]	PS[13]
AF	NC	PI[6]	PG[11]	PB[3]	VSS_HV_ADV_D	PR[3]	PR[5]	VDD_HV_ADR_S	VSS_HV_ADV_S	PL[11]	PI[10]	PB[10]	PJ[1]	PB[8]	PA[3]	VDD_HV_IO_MAIN	PJ[5]	PS[2]	PS[5]	PS[8]	PS[11]	PT[0]
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

Figure 4. 416-ball BGA emulation device pinout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A		VDD_HV_IO_MAIN	NC	NC	PX[0]	PM[15]	PN[0]	NC	NC	NC	PX[4]	PX[3]	PX[1]	PQ[13]	PQ[11]	PQ[9]	NC	PQ[7]	PQ[5]	PQ[3]	NC	PX[11]	PX[9]	PX[7]	NC
B	NC	VSS_HV	VDD_HV_IO_MAIN	NC	PM[14]	PM[13]	PM[12]	PM[11]	NC	NC	PX[2]	PQ[15]	PQ[14]	PQ[12]	PQ[10]	PQ[8]	NC	PQ[6]	PQ[4]	NC	NC	PX[10]	PX[8]	PX[6]	PX[5]
C	NC	NC																							
D	NC	NC																							
E	NC	NC																							
F	PN[2]	PN[1]				VSS_HV	VDD_HV_IO_MAIN	PH[13]	PF[2]	PF[5]	PM[10]	PH[15]	PC[11]	PC[13]	PE[12]	PD[0]	PD[2]	PH[9]	PH[3]	PA[11]	PM[9]	PA[0]	PA[1]	VDD_HV_IO_MAIN	VSS_HV
G	PN[4]	PN[3]				PD[14]	VSS_HV	VDD_HV_IO_MAIN	PH[12]	PF[3]	PH[14]	PF[4]	PC[10]	PC[12]	PC[15]	PD[1]	PD[3]	PH[4]	PE[10]	PE[11]	PA[10]	PA[13]	VDD_HV_IO_MAIN	VSS_HV	PA[2]
H	NC	NC				PC[9]	PD[15]																	PA[12]	PE[9]
J	NC	PN[5]				PC[7]	PC[8]		VSS_HV	VDD_HV_IO_FLEX	PM[2]	PM[0]	PK[14]	PC[14]	PM[6]	PH[7]	PH[8]	PH[10]	PH[1]	PH[0]	VDD_HV_FLA	VSS_HV		PD[5]	PE[8]
K	PN[6]	PN[7]				PC[5]	PC[6]		PL[1]	VSS_HV	PM[3]	PM[1]	PK[15]	PM[4]	PM[5]	PM[7]	PM[8]	PH[2]	PG[15]	VDD_HV_FLA	VSS_HV	PE[6]		PE[7]	PD[4]
L	PN[8]	PN[9]				PC[3]	PC[4]		PL[2]	PL[0]											ESR0	PG[13]		PG[14]	PE[5]
M	PN[11]	PN[10]				PC[2]	PC[1]		PL[3]	PL[4]			NC	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV			PA[4]	PORST		PH[11]	PF[15]
N	PN[13]	PN[12]				PC[0]	PE[0]		PL[6]	PL[5]		NC		VSS_LV	VSS_LV	VSS_LV	VSS_LV		VDD_LV		PA[9]	PA[8]		TESTMODE	PF[14]
P	PN[15]	PN[14]				PE[1]	PE[2]		PD[12]	PL[7]		VSS_LV	VSS_LV		VSS_LV	VSS_LV		VSS_LV	VSS_LV		PA[6]	PI[15]		PD[7]	PA[14]
R	NC	NC				PD[13]	PE[4]		PE[3]	PG[0]		NC	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	NC		PA[7]	PI[14]		PF[13]	PD[6]
T	PL[8]	PQ[1]				PI[8]	PI[9]		PK[0]	PK[1]		NC	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	NC		PK[13]	PK[12]		PA[5]	VSS_HV_OSC
U	PQ[2]	PQ[0]				PG[2]	PG[1]		PK[2]	PK[3]		VSS_LV	VSS_LV		VSS_LV	VSS_LV		VSS_LV	VSS_LV		PJ[15]	PJ[14]		XTAL	EXTAL
V	NC	NC				PG[4]	PG[3]		PB[12]	PB[14]		VDD_LV		VSS_LV	VSS_LV	VSS_LV	VSS_LV		VDD_LV		PJ[13]	PJ[12]		NC	VDD_HV_IO_JTAG
W	PR[14]	PR[15]				PB[15]	PB[13]		PI[1]	PK[5]			VDD_LV	VSS_LV	NC	NC	VSS_LV	VDD_LV			PJ[10]	PJ[11]		PF[10]	PF[9]
Y	PR[12]	PR[13]				PI[0]	PB[5]		PK[4]	PK[6]											PJ[8]	PJ[9]		PF[12]	PF[11]
AA	PY[3]	PY[2]				VDD_HV_ADR_D	VSS_HV_ADR_D		PK[7]	PK[8]	PK[9]	PG[10]	PB[4]	PD[11]	PB[0]	VDDSTBY	PL[10]	PL[12]	PL[14]	PJ[6]	VSS_HV	PH[6]		PJ[4]	PH[5]
AB	PR[11]	PR[10]				PI[2]	PI[3]		NC	PG[7]	PK[11]	PK[10]	PE[14]	PB[3]	PB[1]	PL[9]	PL[11]	PL[13]	PL[15]	PJ[7]	PJ[5]	VSS_HV		PF[8]	PJ[3]
AC	PY[1]	PY[0]				PI[4]	PI[5]																	VDD_HV_IO_MAIN	PJ[2]
AD	PR[8]	PR[9]				PG[5]	PG[6]	PI[6]	PI[7]	PG[8]	PG[9]	PG[11]	PE[15]	PB[2]	PI[13]	PI[11]	PF[1]	PD[9]	PB[11]	PB[9]	PA[3]	PF[7]	PA[15]	VSS_HV	VDD_HV_IO_MAIN
AE	PX[15]	PX[14]				NC	PB[7]	PB[6]	VSS_HV_ADV_S	VDD_HV_ADV_S	VDD_HV_ADR_S	VSS_HV_ADR_S	PG[12]	PE[13]	PI[12]	PI[10]	PF[0]	PD[10]	PB[10]	PB[8]	PD[8]	PF[6]	PJ[0]	PJ[1]	VSS_HV
AF	PR[6]	PR[7]																							
AG	VDD_HV_ADR_D2	VSS_HV_ADR_D2																							
AH	NC	NC																							
AJ	NC	NC	NC	PR[4]	PR[2]	PX[12]	PR[1]	VSS_HV_ADV_S	VDD_HV_ADV_S	VSS_HV	VDD_HV_IO_FLEXE	PS[0]	PS[2]	PS[4]	PS[6]	PS[8]	PS[10]	PS[12]	PS[14]	NC	PT[0]	PT[2]	PT[4]	PT[6]	PT[8]
AK		NC	NC	PR[5]	PR[3]	PX[13]	PR[0]	VSS_HV_ADV_D	VDD_HV_ADV_D	VSS_HV	VDD_HV_IO_FLEXE	PS[1]	PS[3]	PS[5]	PS[7]	PS[9]	PS[11]	PS[13]	PS[15]	VDD_HV_IO_FLEXE	PT[1]	PT[3]	PT[5]	PT[7]	PT[9]
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

Figure 5. 512-ball BGA production device pinout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	2
A		VDD_HV_IO_MAIN	NC	NC	PX[0]	PM[15]	PN[0]	NC	NC	NC	PX[4]	PX[3]	PX[1]	PQ[13]	PQ[11]	PQ[9]	NC	PQ[7]	PQ[5]	PQ[3]	NC	PX[11]	PX[9]	PX[7]	NC	N
B	NC	VSS_HV	VDD_HV_IO_MAIN	NC	PM[14]	PM[13]	PM[12]	PM[11]	NC	NC	PX[2]	PQ[15]	PQ[14]	PQ[12]	PQ[10]	PQ[8]	NC	PQ[6]	PQ[4]	NC	NC	PX[10]	PX[8]	PX[6]	PX[5]	N
C	NC	NC																								
D	NC	NC																								
E	NC	NC																								
F	PN[2]	PN[1]				VSS_HV	VDD_HV_IO_MAIN	PH[13]	PF[2]	PF[5]	PM[10]	PH[15]	PC[11]	PC[13]	PE[12]	PD[0]	PD[2]	PH[9]	PH[3]	PA[11]	PM[9]	PA[0]	PA[1]	VDD_HV_IO_MAIN	VSS_HV	
G	PN[4]	PN[3]				PD[14]	VSS_HV	VDD_HV_IO_MAIN	PH[12]	PF[3]	PH[14]	PF[4]	PC[10]	PC[12]	PC[15]	PD[1]	PD[3]	PH[4]	PE[10]	PE[11]	PA[10]	PA[13]	VDD_HV_IO_MAIN	VSS_HV	PA[2]	
H	NC	NC				PC[9]	PD[15]																	PA[12]	PE[9]	
J	NC	PN[5]				PC[7]	PC[8]		VSS_HV	VDD_HV_IO_FLEX	PM[2]	PM[0]	PK[14]	PC[14]	PM[6]	PH[7]	PH[8]	PH[10]	PH[1]	PH[0]	VDD_HV_FLA	VSS_HV		PD[5]	PE[8]	
K	PN[6]	PN[7]				PC[5]	PC[6]		PL[1]	VSS_HV	PM[3]	PM[1]	PK[15]	PM[4]	PM[5]	PM[7]	PM[8]	PH[2]	PG[15]	VDD_HV_FLA	VSS_HV	PE[6]		PE[7]	PD[4]	
L	PN[8]	PN[9]				PC[3]	PC[4]		PL[2]	PL[0]											ESR0	PG[13]		PG[14]	PE[5]	
M	PN[11]	PN[10]				PC[2]	PC[1]		PL[3]	PL[4]			VDD_LV_BD	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_LV			PA[4]	PORST		PH[11]	PF[15]	
N	PN[13]	PN[12]				PC[0]	PE[0]		PL[6]	PL[5]		VDD_LV_BD		VSS_LV	VSS_LV	VSS_LV	VSS_LV		VDD_LV		PA[9]	PA[8]		TESTMODE	PF[14]	
P	PN[15]	PN[14]				PE[1]	PE[2]		PD[12]	PL[7]		VSS_LV	VSS_LV		VSS_LV	VSS_LV		VSS_LV	VSS_LV		PA[6]	PI[15]		PD[7]	PA[14]	
R	NC	NC				PD[13]	PE[4]		PE[3]	PG[0]		TX3P	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VDD_HV_IO_BD		PA[7]	PI[14]		PF[13]	PD[6]	
T	PL[8]	PQ[1]				PI[8]	PI[9]		PK[0]	PK[1]		TX3N	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	VSS_LV	NC		PK[13]	PK[12]		PA[5]	VSS_HV_OSC	
U	PQ[2]	PQ[0]				PG[2]	PG[1]		PK[2]	PK[3]		VSS_LV	VSS_LV		VSS_LV	VSS_LV		VSS_LV	VSS_LV		PJ[15]	PJ[14]		XTAL	EXTAL	
V	NC	NC				PG[4]	PG[3]		PB[12]	PB[14]		VDD_LV		VSS_LV	VSS_LV	VSS_LV	VSS_LV		VDD_LV		PJ[13]	PJ[12]		NC	VDD_HV_IO_JTAG	
W	PR[14]	PR[15]				PB[15]	PB[13]		PI[1]	PK[5]			VDD_LV	VSS_LV	TX2N	TX2P	VSS_LV	VDD_LV			PJ[10]	PJ[11]		PF[10]	PF[9]	
Y	PR[12]	PR[13]				PI[0]	PB[5]		PK[4]	PK[6]											PJ[8]	PJ[9]		PF[12]	PF[11]	
AA	PY[3]	PY[2]				VDD_HV_ADR_D	VSS_HV_ADR_D		PK[7]	PK[8]	PK[9]	PG[10]	PB[4]	PD[11]	PB[0]	VDDSTBY	PL[10]	PL[12]	PL[14]	PJ[6]	VSS_HV	PH[6]		PJ[4]	PH[5]	
AB	PR[11]	PR[10]				PI[2]	PI[3]		NC	PG[7]	PK[11]	PK[10]	PE[14]	PB[3]	PB[1]	TX1N	TX1P	TX0N	TX0P	CLKN	CLKP	VSS_HV		PF[8]	PJ[3]	
AC	PY[1]	PY[0]				PI[4]	PI[5]																	VDD_HV_IO_MAIN	PJ[2]	
AD	PR[8]	PR[9]				PG[5]	PG[6]	PI[6]	PI[7]	PG[8]	PG[9]	PG[11]	PE[15]	PB[2]	PI[13]	PI[11]	PF[1]	PD[9]	PB[11]	PB[9]	PA[3]	PF[7]	PA[15]	VSS_HV	VDD_HV_IO_MAIN	
AE	PX[15]	PX[14]				NC	PB[7]	PB[6]	VSS_HV_ADV_S	VDD_HV_ADV_S	VDD_HV_ADR_S	VSS_HV_ADR_S	PG[12]	PE[13]	PI[12]	PI[10]	PF[0]	PD[10]	PB[10]	PB[8]	PD[8]	PF[6]	PJ[0]	PJ[1]	VSS_HV	
AF	PR[6]	PR[7]																								
AG	VDD_HV_ADR_D2	VSS_HV_ADR_D2																								
AH	NC	NC																								
AJ	NC	NC	NC	PR[4]	PR[2]	PX[12]	PR[1]	VSS_HV_ADV_S	VDD_HV_ADV_S	VSS_HV	VDD_HV_IO_FLEXE	PS[0]	PS[2]	PS[4]	PS[6]	PS[8]	PS[10]	PS[12]	PS[14]	NC	PT[0]	PT[2]	PT[4]	PT[6]	PT[8]	PT[
AK		NC	NC	PR[5]	PR[3]	PX[13]	PR[0]	VSS_HV_ADV_D	VDD_HV_ADV_D	VSS_HV	VDD_HV_IO_FLEXE	PS[1]	PS[3]	PS[5]	PS[7]	PS[9]	PS[11]	PS[13]	PS[15]	VDD_HV_IO_FLEXE	PT[1]	PT[3]	PT[5]	PT[7]	PT[9]	PT[

Figure 6. 512-ball BGA emulation device pinout (top view)

2.2 Pin/ball descriptions

The following sections provide signal descriptions and related information about device functionality and configuration.

2.2.1 Power supply and reference voltage pins/balls

Table 2 contains information on power supply and reference pin functions for the devices.

NOTE

All ground supplies must be tied to ground. They can NOT float.

Table 2. Power supply and reference pins

Supply			BGA ball			
Symbol	**Type**	**Description**	**416PD**	**416ED**	**512PD**	**512ED**
V_{SS_HV}	Ground	High voltage ground	A26, B25, C24, D23, D15, D8, J4, L23, R23, T4, W23, AC23, AC19		B2, B29, B30, F6, F25, G7, G24, H29, H30, J9, J22, K10, K21,V29, AA21, AB22, AD24, AE25, AJ10, AJ29, AK10	
V_{SS_LV}	Ground	Low voltage ground	K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15,N 16, N17, P11, P12, P13, P14, P15, P16, R 11, R12, R13, R14, R15, R16, T10, T11, T12, T13, T14, T15, T16, T17		M14, M15, M16, M17, N14, N15, N16, N17, P12, P13, P15, P16, P18, P19, R13, R14, R15, R16, R17, R18, T13,T14, T15, T16, T17, T18, U12, U13, U 15, U16, U18, U19, V14, V15 V16, V17, W14, W17	
V_{DD_LV}	Power	Low voltage power supply for production device (PLL is also powered by this pin.)	B26, C25, D9, D24, E23, H4, P23, V23, AB23, AC20		M18, N19, V12, V19, W13, W18	
$V_{DD\_LV\_BD}$	Power	Low voltage power supply for buddy die	—	R1, R4	—	M13, N12
$V_{DD\_HV\_PMC}$	Power	High voltage power supply for internal power management unit	D14		—	
$V_{DD\_HV\_IO\_MAIN}$	Power	High voltage power supply for I/O	A25, B24, C23, D22, K4, AC16, AD16, AE16, AF16		A2, A29, B3, B28, F7, F24, G8, G23, AC24, AD25, AH29, AJ30	
$V_{DD\_HV\_IO\_BD}$	Power	High voltage power supply for buddy die I/O	—	P17	—	R19
$V_{SS\_HV\_OSC}$	Ground	Oscillator ground supply	F25		T25	
$V_{DD\_HV\_JTAG}$	Power	JTAG/Oscillator power supply	E26		V25	

Table 2. Power supply and reference pins (continued)

Supply			BGA ball			
Symbol	Type	Description	416PD	416ED	512PD	512ED
$V_{DD\_HV\_IO\_FLEX}$	Power	FlexRay/Ethernet 3.3 V I/O supply	D7		J10	
$V_{DD\_HV\_IO\_FLEXE}$	Power	FLexRay/Ethernet/EBI I/O Segment Voltage Supply	AC18, AC22		AJ11, AK11, AK20, AK29	
$V_{DD\_HV\_IO\_EBI}$	Power	EBI Address/Control I/O Segment Voltage Supply	M23,T23,Y23		J29, J30, V30, AH30	
$V_{DD\_HV\_FLA}$	Power	Decoupling supply pin for flash	A18, B18		J21, K20	
$V_{SS\_HV\_ADV\_S}$	Ground	Ground supply for ADC SAR	AF9		AE9, AJ8	
$V_{DD\_HV\_ADV\_S}$	Power	Voltage supply for ADC SAR	AE9		AE10, AJ9	
$V_{SS\_HV\_ADV\_D}$	Ground	Ground supply for ADC SD	AF5		AK8	
$V_{DD\_HV\_ADV\_D}$	Power	Voltage supply for ADC SD	AE5		AK9	
$V_{SS\_HV\_ADR\_S}$	Reference	Ground reference for ADC SAR	AE8		AE12	
$V_{DD\_HV\_ADR\_S}$	Reference	Voltage reference for ADC SAR	AF8		AE11	
$V_{SS\_HV\_ADR\_D}$	Reference	Ground reference for ADC SD	Y4, AC6		AA7	
$V_{DD\_HV\_ADR\_D}$	Reference	Voltage reference for ADC SD	W4, AD6		AA6	
V_{DDSTBY}	Power	Standby RAM supply	AD9		AA16	

2.2.2 System pins/balls

Table 3 contains information on system pin functions for the devices.

Table 3. System pins

Symbol	Description	Direction	BGA ball			
			416PD	416ED	512PD	512ED
PORST	Power on reset with Schmitt trigger characteristics and noise filter. PORST is active low	Bidirectional	B22		M22	
ESR0	External functional reset with Schmitt trigger characteristics and noise filter. ESR0 is active low	Bidirectional	A23		L21	
TESTMODE	Pin for testing purpose only. TESTMODE pull-down is implemented to prevent the device from entering TESTMODE. It is recommended to connect the TESTMODE pin to VSS_HV_IO on the board. The value of the TESTMODE pin is latched at the negation of reset and has no affect afterward. **Note:** The device will not exit reset with the TESTMODE pin asserted during power-up.	Input only	B23		N24	

Table 3. System pins (continued)

Symbol	Description	Direction	BGA ball			
			416PD	416ED	512PD	512ED
XTAL	Analog output of the oscillator amplifier circuit needs to be grounded if oscillator is used in bypass mode.	Output	G25		U24	
EXTAL	Analog input of the oscillator amplifier circuit when oscillator is not in bypass mode Analog input for the clock generator when oscillator is in bypass mode	Input	G26		U25	

2.2.3 LVDS pins/balls

The following table contains information on LVDS pin functions for the devices.

Table 4. LVDS pin descriptions

Functional block	Port pin	Signal	Signal description	Direction	BGA ball (416 PD, 416 ED)	BGA ball (512 PD, 512 ED)
SIPI / LFAST[1]	PA[14]	SIPI_TXP	Interprocessor Bus LFAST, LVDS Transmit Positive Terminal	O	C26	P25
	PD[6]	SIPI_TXN	Interprocessor Bus LFAST, LVDS Transmit Negative Terminal	O	D26	R25
	PD[7]	SIPI_RXP	Interprocessor Bus LFAST, LVDS Receive Positive Terminal	I	G23	P24
	PF[13]	SIPI_RXN	Interprocessor Bus LFAST, LVDS Receive Negative Terminal	I	H23	R24
High-Speed Debug (HSD) / LFAST[1,2]	PA[7]	DEBUG_TXP	Debug LFAST, LVDS Transmit Positive Terminal	O	F24	R21
	PA[8]	DEBUG_TXN	Debug LFAST, LVDS Transmit Negative Terminal	O	E25	N22
	PA[9]	DEBUG_RXP	Debug LFAST, LVDS Receive Positive Terminal	I	D25	N21
	PA[5]	DEBUG_RXN	Debug LFAST, LVDS Receive Negative Terminal	I	F23	T24

Table 4. LVDS pin descriptions (continued)

Functional block	Port pin	Signal	Signal description	Direction	BGA ball (416 PD, 416 ED)	BGA ball (512 PD, 512 ED)
DSPI 4 Microsecond Bus	PD[2]	SCK_P	DSPI 4 Microsecond Bus Serial Clock, LVDS Positive Terminal	O	C18	F17
	PD[3]	SCK_N	DSPI 4 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	C17	G17
	PD[0]	SOUT_P	DSPI 4 Microsecond Bus Serial Data, LVDS Positive Terminal	O	C16	F16
	PD[1]	SOUT_N	DSPI 4 Microsecond Bus Serial Data, LVDS Negative Terminal	O	D17	G16
DSPI 5 Microsecond Bus	PF[10]	SCK_P	DSPI 5 Microsecond Bus Serial Clock, LVDS Positive Terminal	O	J24	W24
	PF[9]	SCK_N	DSPI 5 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	K23	W25
	PF[12]	SOUT_P	DSPI 5 Microsecond Bus Serial Data, LVDS Positive Terminal	O	J26	Y24
	PF[11]	SOUT_N	DSPI 5 Microsecond Bus Serial Data, LVDS Negative Terminal	O	J25	Y25
DSPI 6 Microsecond Bus	PQ[9]	SCK_P	DSPI 6Microsecond Bus Serial Clock, LVDS Positive Terminal	O	A17	A16
	PQ[8]	SCK_N	DSPI 6 Microsecond Bus Serial Clock, LVDS Negative Terminal	O	B17	B16
	PQ[11]	SOUT_P	DSPI 6 Microsecond Bus Serial Data, LVDS Positive Terminal	O	B16	A15
	PQ[10]	SOUT_N	DSPI 6 Microsecond Bus Serial Data, LVDS Negative Terminal	O	A16	B15

Table 4. LVDS pin descriptions (continued)

Functional block	Port pin	Signal	Signal description	Direction	BGA ball (416 PD, 416 ED)	BGA ball (512 PD, 512 ED)
Differential DSPI 2	PD[2]	SCK_P	Differential DSPI 2 Clock, LVDS Positive Terminal	O	C18	F17
	PD[3]	SCK_N	Differential DSPI 2 Clock, LVDS Negative Terminal	O	C17	G17
	PD[0]	SOUT_P	Differential DSPI 2 Serial Output, LVDS Positive Terminal	O	C16	F16
	PD[1]	SOUT_N	Differential DSPI 2 Serial Output, LVDS Negative Terminal	O	D17	G16
	PD[7]	SIN_P	Differential DSPI 2 Serial Input, LVDS Positive Terminal	I	G23	P24
	PF[13]	SIN_N	Differential DSPI 2 Serial Input, LVDS Negative Terminal	I	H23	R24
Differential DSPI 5	PF[10]	SCK_P	Differential DSPI 5 Clock, LVDS Positive Terminal	O	J24	W24
	PF[9]	SCK_N	Differential DSPI 5 Clock, LVDS Negative Terminal	O	K23	W25
	PF[12]	SOUT_P	Differential DSPI 5 Serial Output, LVDS Positive Terminal	O	J26	Y24
	PF[11]	SOUT_N	Differential DSPI 5 Serial Output, LVDS Negative Terminal	O	J25	Y25
	PD[7]	SIN_P	Differential DSPI 5 Serial Input, LVDS Positive Terminal	I	G23	P24
	PF[13]	SIN_N	Differential DSPI 5 Serial Input, LVDS Negative Terminal	I	H23	R24
	PI[15]	SIN_P	Differential DSPI 5 Serial Input, LVDS Positive Terminal	I	G24	P22
	PI[14]	SIN_N	Differential DSPI 5 Serial Input, LVDS Negative Terminal	I	J23	R22

1 DRCLK and TCK/DRCLK usage for SIPI LFAST and Debug LFAST are described in the *MPC5777M Microcontroller Reference Manual* SIPI LFAST and Debug LFAST chapters.

2 Pads use special enable signal form DCI block: DCI driven enable for Debug LFAST pads is transparent to user.

Table 5. Aurora pin descriptions

Functional Block	PAD	Signal	Signal Description	Direction	BGA			
					416PD	416ED	512PD	512ED
Nexus Aurora High Speed Trace	—	TX0P	Nexus Aurora High Speed Trace Lane 0, LVDS Positive Terminal	O	—	U15	—	AB19
	—	TX0N	Nexus Aurora High Speed Trace Lane 0, LVDS Negative Terminal	O	—	U14	—	AB18
	—	TX1P	Nexus Aurora High Speed Trace Lane 1, LVDS Positive Terminal	O	—	U13	—	AB17
	—	TX1N	Nexus Aurora High Speed Trace Lane 1, LVDS Negative Terminal	O	—	U12	—	AB16
	—	TX2P	Nexus Aurora High Speed Trace Lane 2, LVDS Positive Terminal	O	—	U11	—	W16
	—	TX2N	Nexus Aurora High Speed Trace Lane 2, LVDS Negative Terminal	O	—	U10	—	W15
	—	TX3P	Nexus Aurora High Speed Trace Lane 3, LVDS Positive Terminal	O	—	P10	—	R12
	—	TX3N	Nexus Aurora High Speed Trace Lane 3, LVDS Negative Terminal	O	—	R10	—	T12
	—	CLKP (BD-AGB TCLKP)	Nexus Aurora High Speed Trace Clock, LVDS Positive Terminal	I	—	U17	—	AB21
	—	CLKN (BD-AGB TCLKN)	Nexus Aurora High Speed Trace Clock, LVDS Negative Terminal	I	—	U16	—	AB20

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

NOTE

Within this document, $V_{DD\_HV\_IO}$ refers to supply pins $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_FLEXE}$, $V_{DD\_HV\_IO\_EBI}$, and $V_{DD\_HV\_FLA}$. $V_{DD\_HV\_ADV}$ refers to ADC supply pins $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADR}$ refers to ADC reference pins $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$. $V_{SS\_HV\_ADV}$ refers to ADC ground pins $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$. $V_{SS\_HV\_ADR}$ refers to ADC reference pins $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$.

3.2 Absolute maximum ratings

Table 6 describes the maximum ratings of the device.

Table 6. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	SR	Lifetime power cycles	—	—	1000 k	—
V_{DD_LV}	SR	1.2 V core supply voltage[2,3,4]	—	–0.3	1.5	V
$V_{DD\_LV\_BD}$	SR	Emulation module voltage[2,3,4]	—	–0.3	1.5	V
$V_{DD\_HV\_IO}$	SR	I/O supply voltage[5,6]	—	–0.3	6.0	V
$V_{DD\_HV\_PMC}$	SR	Power Management Controller supply voltage[5]	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$	SR	Flash core voltage[7]	—	–0.3	4.5	V
V_{DDSTBY}	SR	RAM standby supply voltage[5]	—	–0.3	6.0	V
$V_{SS\_HV\_ADV}$[8]	SR	SAR and S/D ADC ground voltage	Reference to V_{SS_HV}	–0.3	0.3	V
$V_{DD\_HV\_ADV}$[9]	SR	SAR and S/D ADC supply voltage	Reference to corresponding $V_{SS\_HV\_ADV}$	–0.3	6.0	V
$V_{SS\_HV\_ADR}$[10]	SR	SAR and S/D ADC low reference	Reference to V_{SS_HV}	–0.3	0.3	V
$V_{DD\_HV\_ADR}$[11]	SR	SAR and S/D ADC high reference	Reference to corresponding $V_{SS\_HV\_ADR}$	–0.3	6.0	V
$V_{DD\_HV\_IO\_JTAG}$	SR	Crystal oscillator, FEC MDIO/MDC, LFAST, JTAG[5]	Reference to V_{SS_HV}	–0.3	6.0	V

Table 6. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{DD\_HV\_IO\_EBI}$	SR	External Bus Interface supply voltage	—	–0.3	6.0	V
$V_{DD\_LV\_BD} – V_{DD\_LV}$	SR	Emulation module supply differential to 1.2 V core supply	—	–0.3	1.5	V
V_{IN}	SR	I/O input voltage range[12]	—	–0.3	6.0	V
			Relative to $V_{SS\_HV\_IO}$[13,14]	–0.3	—	
			Relative to $V_{DD\_HV\_IO}$[13,14]	—	0.3	
I_{INJD}	SR	Maximum DC injection current for digital pad	Per pin, applies to all digital pins	–5	5	mA
I_{INJA}	SR	Maximum DC injection current for analog pad	Per pin, applies to all analog pins	–5	5	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	–7	8	mA
			Strong	–10	10	
			Very strong	–11	11	
I_{MAXSEG}	SR	Maximum current per power segment[15]	—	–90	90	mA
T_{STG}	SR	Storage temperature range and non-operating times	—	–55	175	°C
STORAGE	SR	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	20	years
T_{SDR}	SR	Maximum solder temperature[16] Pb-free package	—	—	260	°C
MSL	SR	Moisture sensitivity level[17]	—	—	3	—
t_{XRAY}	SR	X-ray screen time[18]	At 160 KeV at max 5 mm	—	3	min

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in note 3 and note 4

3 Allowed 1.38– 1.45 V– for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in note 4

4 1.32 – 1.38 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.326 V at maximum T_J = 150 °C.

5 Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C, remaining time at or below 5.5 V.

6 $V_{DD\_HV\_IO}$ applies to $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_FLEXE}$, $V_{DD\_HV\_IO\_JTAG}$, and $V_{DD\_HV\_IO\_EBI}$ I/O power supplies.

7 Allowed 3.6–4.5 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C, remaining time at or below 3.6 V.

8 Includes ADC grounds $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$.

9 Includes ADC supplies $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADV\_S}$ is also the supply for the device temperature sensor, RCOSC, and bandgap reference.

10 Includes ADC low references $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$.

11 Includes ADC high references $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$.

12 The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies significantly across process and temperature, but a value of 0.3V can be used for nominal calculations.

13 $V_{DD\_HV\_IO}$/$V_{SS\_HV\_IO}$ refers to supply pins and corresponding grounds: $V_{DD\_HV\_IO\_MAIN}$, $V_{DD\_HV\_IO\_FLEX}$, $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_OSC}$, $V_{DD\_HV\_FLA}$.

14 Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameters I_{INJD} and I_{INJA}).

15 Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

16 Solder profile per IPC/JEDEC J-STD-020D

17 Moisture sensitivity per JEDEC test method A112

18 Three Screen done, 1 minute each. No change in device parameters during characterization of at least 10 devices at 30 minutes exposure of 150 KeV at maximum 5 mm.

3.3 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 7. ESD ratings[1,2]

Parameter	Conditions	Value	Unit
ESD for Human Body Model (HBM)[3]	All pins	2000	V
ESD for field induced Charged Device Model (CDM)[4]	All pins	500	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”

3 This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing

4 This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

3.4 Operating conditions

The following table describes the operating conditions for the device for which all specifications in the data sheet are valid, except where explicitly noted.

The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 8. Device operating conditions[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Frequency							
f_{SYS}	SR	Device operating frequency[2]	T_J = –40 °C to 150 °C	—	—	300	MHz

Table 8. Device operating conditions[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Temperature							
T_J	SR	Operating temperature range - junction	—	–40.0	—	150.0	°C
T_A (T_L to T_H)	SR	Ambient operating temperature range	—	–40.0	—	125.0	°C
Voltage							
V_{DD_LV}	SR	External core supply voltage[3,4]	LVD/HVD enabled	1.24	—	1.38[5]	V
			LVD/HVD disabled[6,7,8,9]	1.19	—	1.38[5]	
$V_{DD\_HV\_IO\_MAIN}$[10,11]	SR	I/O supply voltage	LVD400/HVD600 enabled[18]	4.5	—	5.5[12]	V
			LVD400/HVD600 disabled [6,13,14,15,18]	4.2	—	5.5	
			LVD360/HVD600 disabled [6,13,14,16,17,18]	3.0	—	5.5	
$V_{DD\_HV\_IO\_JTAG}$	SR	JTAG I/O supply voltage[6,19]	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_IO\_FLEX}$	SR	FlexRay I/O supply voltage	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_IO\_FLEXE}$	SR	FlexRay/EBI I/O supply voltage	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_IO\_EBI}$	SR	External Bus Interface supply voltage	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_OSC}$	SR	Oscillator supply voltage[6,20]	5 V range	4.5	—	5.5	V
			3.3 V range	3.0	—	3.6	
$V_{DD\_HV\_PMC}$[21]	SR	Power Management Controller (PMC) supply voltage	Full functionality[22,23]	3.5[24,25]	—	5.5	V
			Reduced internal regulator output capability[26]	3.15	—	3.5	
			Supply monitoring activity only (LVD/HVD)	3.0	—	3.15	
V_{DDSTBY}	SR	RAM standby supply voltage[27,28,29]	—	1.1	—	5.5	V
$V_{DD\_HV\_ADV}$	SR	SARADC, SDADC, Temperature Sensor, and Bandgap Reference supply voltage	LVD400 enabled	4.5	—	5.5	V
			LVD400 disabled[30,31,34]	4.0	—	5.5[32]	
			LVD300 disabled[6,30,31,33,34]	3.7	—	5.5[32]	

Table 8. Device operating conditions[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$V_{DD\_HV\_ADR\_D}$	SR	SD ADC supply reference voltage	Reduced SNR	3.0	$V_{DD\_HV\_ADV\_D}$	4.5	V
			Full SNR	4.5		5.5[32]	
$V_{DD\_HV\_ADR\_D} – V_{DD\_HV\_ADV\_D}$	SR	SD ADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_D}$	SR	SD ADC ground reference voltage	—	$V_{SS\_HV\_ADV\_D}$			V
$V_{SS\_HV\_ADR\_D} – V_{SS\_HV\_ADV\_D}$	SR	$V_{SS\_HV\_ADR\_D}$ differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$[35]	SR	SARADC reference	—	2.0	$V_{DD\_HV\_ADV\_S}$	4.0	V
				4.0		5.5[32]	
$V_{SS\_HV\_ADR\_S}$	SR	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV\_S}$			V
$V_{DD\_HV\_ADR\_S} – V_{DD\_HV\_ADV\_S}$	SR	SARADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_S} – V_{SS\_HV\_ADV\_S}$	SR	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
$V_{SS\_HV\_ADV} – V_{SS}$	SR	$V_{SS\_HV\_ADV}$ differential voltage	—	–25	—	25	mV
V_{RAMP_LV}	SR	Slew rate on core power supply pins	—	—	—	100	V/ms
V_{RAMP_HV}	SR	Slew rate on HV power supply pins	—	—	—	100	V/ms
V_{por_rel}	CC	POR release trip point	-40 °C < Tj < 150 °C	3.10	—	4.26	V
V_{por_hys}	CC	POR hysteresis	-40 °C < Tj < 150 °C	150	—	300	mV
V_{IN}	SR	I/O input voltage range	—	0	—	5.5	V
Injection current							
I_{IC}	SR	DC injection current (per pin)[36,37,38]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	SR	Maximum current per power segment[39]	—	–80	—	80	mA

1 The ranges in this table are design targets and actual data may vary in the given range.

2 Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the *MPC5777M Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.

3 Core voltage as measured on device pin to guarantee published silicon performance.

4 During power ramp, voltage measured on silicon might be lower. maximum performance is not guaranteed, but correct silicon operation is guaranteed. Refer to the Power Management and Reset Generation Module chapters in the *MPC5777M Microcontroller Reference Manual* for further information.

5 Although the maximum V_{DD_LV} operating voltage is 1.38 V, reset is not entered at that voltage. An external voltage monitor is needed or the HVD140_C can be monitored (via an interrupt or by polling the HVD140_C flag bit). Performance above 1.38 V is not guaranteed, and allowed operation above 1.38 V is defined in Absolute maximum ratings.

6 In the LVD/HVD disabled case, it is necessary for the system to be within a higher voltage range during destructive reset events.

7 Maximum core voltage is not permitted for entire product life. *See Absolute maximum rating*.

8 When internal LVD/HVDs are disabled, external monitoring is required to guarantee correct device operation.

9 Vdd_lv should be above 1.24 V during destructive resets or POR events.

10 VDD_HV_IO_MAIN range limited to 4.75–5.25 V when FERS = 1 to enable the fast erase time of the flash memory.

11 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

12 When the LVD/HVDs are enabled, the $V_{DD\_HV\_IO\_MAIN}$ must be less than 5.412 V to exit from a destructive reset.

13 Maximum voltage is not permitted for entire product life. See *Absolute maximum rating*.

14 When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.

15 When these LVD/HVDs are disabled, the $V_{DD\_HV\_IO\_MAIN}$ supply must be between 3.182 V and 5.412 V.

16 Reduced output capabilities below 4.2 V. See performance derating values in *I/O pad electrical characteristics.*

17 When the LVD/HVDs are disabled, the VDD_HV_IO_MAIN must be between 3.024 V and 5.412 V.

18 The PMC supply voltage ($V_{DD\_HV\_PMC}$) must be within the correct range (see the $V_{DD\_HV\_PMC}$ specification).

19 When the LVD/HVDs are disabled, the HV I/O JTAG supply ($V_{DD\_HV\_IO\_JTAG}$) must be above 3.024 V.

20 When the LVD/HVDs are disabled, the HV OSC supply ($V_{DD\_HV\_OSC}$) must be above 3.024 V.

21 Flash read operation is supported for a minimum $V_{DD\_HV\_PMC}$ value of 3.15 V. Flash read, program, and erase operations are supported for a minimum $V_{DD\_HV\_PMC}$ value of 3.5 V.

22 When the LVD/HVDs are disabled, the $V_{DD\_HV\_PMC}$ must be below 5.412 V during destructive reset events.

23 A minimum of 4.5 V is required to guarantee correct user logic BIST operation.

24 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

25 Above Ta = 25°C, the minimum $V_{DD\_HV\_PMC}$ voltage is 3.6 V.

26 With the reduced internal regulator output capability, erases and writes to the device flash cannot be guaranteed for a single event and multiple erases and writes may be necessary. User logic BIST is not supported with reduced capability.

27 RAM data retention is guaranteed at a voltage that is always below the maximum brownout flag trip point voltage (see the DC Electrical Specification table). The minimum V_{DDSTBY} voltage at the pin is larger in order to account for on-chip IR drop and noise. There is no effect on RAM operation when V_{DDSTBY} is below 1.1 V, and V_{DD_LV} is above the minimum operating value.

28 Non-regulated supplies can be used on the VDDSTBY pin if the absolute maximum and operating condition voltage limits are met. There is no static clamp to a supply rail for the VDDSTBY pin, only dynamic protection for ESD events.

29 The VDDSTBY pin should be connected to ground in the application when the standby RAM feature is not used.

30 $V_{DD\_HV\_ADV\_S}$ is required to be between 4.5 V and 5.5 V to read the internal Temperature Sensor and Bandgap Reference.

31 SAR ADC only. SDADC minimum is 4.5 V.

32 The ADC is functional up to 5.9V with no reliability issues, but performance is not guaranteed.

33 When the LVD/HVDs are disabled, the HV ADC supply ($V_{DD\_HV\_ADV}$) must be above 3.182 V.

34 For supply voltages between 3.0 V and 4.0 V there is no guaranteed precision of ADC (accuracy/linearity). ADCs recover to a fully functional state when the voltage rises above 4.0 V.

35 $V_{DD\_HV\_ADR\_S}$ must be between 4.5 V and 5.5 V for accurate reading of the device Temperature Sensor.

36 Full device lifetime without performance degradation

37 I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the *Absolute maximum ratings* table for maximum input current for reliability requirements.

38 The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current is injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.

39 Sum of all controller pins (including both digital and analog) must not exceed 200 mA. A $V_{DD\_HV\_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD\_HV\_IO}$ supply pins.

Table 9. Emulation (buddy) device operating conditions[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Frequency							
—	SR	Standard JTAG 1149.1/1149.7 frequency	—	—	—	50	MHz
—	SR	High-speed debug frequency	—	—	—	320	MHz
—	SR	Data trace frequency	—	—	—	1250	MHz
Temperature							
T_{J_BD}	SR	Device junction operating temperature range	—	–40.0	—	150.0	°C
T_{A_BD}	SR	Ambient operating temperature range	—	–40.0	—	125.0	°C
Voltage							
$V_{DD\_LV\_BD}$	SR	Buddy core supply voltage	—	1.2	—	1.365	V
$V_{DD\_HV\_IO\_BD}$	SR	Buddy I/O supply voltage	—	3.0	—	5.5	V
$V_{RAMP\_LV\_BD}$	SR	Buddy slew rate on core power supply pins	—	—	—	100	V/ms
$V_{RAMP\_HV\_BD}$	SR	Buddy slew rate on HV power supply pins	—	—	—	100	V/ms

1 The ranges in this table are design targets and actual data may vary in the given range.

3.5 DC electrical specifications

The following table describes the DC electrical specifications.

Table 10. DC electrical specifications[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
I_{DD_LV}	CC	Maximum operating current on the V_{DD_LV} supply[2]	T_J = 150 °C V_{DD_LV} = 1.325 V f_{MAX}	—	—	1140	mA
I_{DDAPP_LV}	CC	Application use case operating current on the V_{DD_LV} supply[3]	T_J = 150 °C V_{DD_LV} = 1.325 V f_{MAX}	—	—	950	mA
$I_{DD\_LV\_PE}$	CC	Operating current on the V_{DD_LV} supply for flash program/erase	T_J = 150 °C	—	—	40	mA

Table 10. DC electrical specifications[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$I_{DD\_HV\_PMC}$	CC	Operating current on the $V_{DD\_HV\_PMC}$ supply[4,5]	Flash read	—	—	10	mA
			Flash P/E	—	—	40	
			PMC only	—	—	25[6]	
$I_{DD\_MAIN\_CORE\_AC}$[7]	CC	Main Core 0/1 dynamic operating current	300 MHz	—	—	115	mA
$I_{DD\_CHKR\_CORE\_AC}$	CC	Checker Core 0 dynamic operating current	300 MHz	—	—	80	mA
$I_{DD\_HSM\_AC}$	CC	HSM platform dynamic operating current	100 MHz	—	—	20	mA
I_{DDSTBY_RAM}	CC	64 KB RAM Standby Leakage Current (RAM not operational)[8,9,10,11]	V_{DDSTBY} @1.1 V to 5.5 V, T_J = 150 °C	—	—	350	µA
	CC		V_{DDSTBY} @1.1 V to 5.5 V, T_A = 40 °C	—	—	60	
	CC		V_{DDSTBY} @1.1 V to 5.5 V, T_A = 85 °C	—	—	100	
I_{DDSTBY_REG}	CC	64 KB RAM Standby Leakage Current[12]	V_{DDSTBY} @1.3 V to 5.5 V, T_A = 125 °C	—	—	50	µA
$I_{DD\_LV\_BD}$	CC	BD Debug/Emulation low voltage supply operating current[13]	T_J = 150 °C $V_{DD\_LV\_BD}$ = 1.32 V	—	—	290	mA
$I_{DD\_HV\_IO\_BD}$	CC	Debug/Emulation high voltage supply operating current (Aurora + JTAGM/LFAST)	T_J = 150 °C	—	—	130	mA
$I_{DD\_BD\_STBY}$	CC	BD Debug/Emulation low voltage supply standby current[14,15]	$V_{DD\_LV\_BD}$ = 1.32 V, T_J = 150 °C	—	—	230	mA
	CC		$V_{DD\_LV\_BD}$ = 1.32 V, T_J = 55 °C	—	—	5	
I_{SPIKE}	CC	Maximum short term current spike[16]	< 20 µs observation window	—	—	90	mA
dI	CC	Current difference ratio to average current (dI/avg(I))[17]	20 µs observation window	—	—	20	%

Table 10. DC electrical specifications[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
I_{SR}[18]	CC	Current variation during power up/down	See footnote[19]	—	—	90	mA
I_{BG}	CC	Bandgap reference current consumption		—	—	600	µA
I_{DDOFF}	CC	Power-off current on high voltage supply rails[20]	V_{DD_HV} = 2.5 V	100	—	—	µA
V_{STBY_BO}	CC	Standby RAM brownout flag trip point voltage	—	—	—	0.9[21]	V
$V_{DD\_LV\_STBY\_SW}$	CC	Standby RAM switch VDD_LV voltage threshold	—	0.93	—	—	V
$V_{REF\_BG\_T}$	CC	Bandgap trimmed reference voltage	T_J = –40 °C to 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	1.200	—	1.237	V
$V_{REF\_BG\_TC}$	CC	Bandgap temperature coefficient[22]	T_J = –40 °C to 150 °C $V_{DD\_HV\_ADV}$ = 5 V	—	—	50	ppm/°C
$V_{REF\_BG\_LR}$	CC	Bandgap line regulation[22]	T_J = –40 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	8000	ppm/V
			T_J = 150 °C $V_{DD\_HV\_ADV}$ = 5 V ± 10%	—	—	4000	

1 All parameters in this data sheet are valid for operation within an operating range of -40° C ≤ T_J≤ 150 °C except where otherwise noted

2 f_{MAX} as specified per IP. Excludes flash P/E and HSM dynamic current. Measured on an application specific pattern. Calculation of total current for the device, all rails, is done by adding the applicable dynamic currents to the I_{DD_LV} value for the core supply, and summing the currents based on use case for the 5 V blocks, for which current consumption values are defined in later sections of the DC electrical specification.

3 f_{MAX} as specified per IP. Excludes flash P/E and HSM dynamic current. Measured on an application specific pattern.

4 $V_{DD\_HV\_PMC}$ only available in the 416 BGA package. PMC supply is shorted to $V_{DD\_HV\_IO\_MAIN}$ in the 512 BGA, with an external bypass capacitor connected to the $V_{DD\_HV\_PMC\_BYP}$ ball. The flash read and P/E current, and PMC current apply to $V_{DD\_HV\_IO\_MAIN}$ for the 512 BGA.

5 The flash read and flash P/E currents are mutually exclusive, and are not cumulative.

6 This includes PMC consumption, LFAST PLL regulator current, and Nwell bias regulator current. If the V_{DD_LV} auxiliary regulator is enabled, the PMC supply may see short term (10 µs) spikes of up to 150 mA depending on transient current conditions from use case of the device. The auxiliary regulator can be disabled at power-up in the user DCF clients in the flash memory.

7 There is an additional 25 mA when FERS = 1 to enable the fast erase time of the flash memory.

8 Data is retained for full T_J range of -40 °C to 150 °C. RAM supply switch to the standby regulator occurs when the V_{DD_LV} supply falls below 0.95V.

9 V_{DDSTBY} may be supplied with a non-regulated power supply, but the absolute maximum voltage on VDDSTBY given in the absolute maximum ratings table must be observed.

10 Standby current is reduced by a factor of two from T_J=150 °C, for approximately every ~20 °C drop in operating temperature.

11 The maximum value for I_{DDSTBY_ON} is also valid when switching from the core supply to the standby supply, and when powering up the device and switching the RAM supply back to V_{DD_LV}.

12 The standby RAM regulator current is present on the VDDSTBY pin whenever a voltage is applied to the pin. This also applies to normal operation where the RAM is powered by the VDD_LV supply. Connecting the VDDSTBY pin to ground when not using the standby RAM feature will remove the leakage current on the VDDSTBY pin.

13 If Aurora and JTAGM/LFAST not used, $V_{DD\_LV\_BD}$ current is reduced by ~20mA.

14 Applies to 2MB calibration RAM in the BD.

15 Buddy device leakage dependency on temperature can be estimated by dividing the 150 °C leakage by two for each temperature drop of ~20 °C.

16 Current spike may occur during normal operation that are above average current, valid for I_{DDAPP} and its conditions given in Table 10 (DC electrical specifications). Internal schemes must be used (eg frequency ramping, feature enable) to ensure that incremental demands are made on the external power supply. An internal fast regulator providing ~40mA peak current within 1us to filter any core power supply droops is available on the device. Assumption is minimum 13.3 µF (20 µF typical) capacitance on the core supply.]

17 Moving window, valid for I_{DDAPP} and its conditions given in Table 10 (DC electrical specifications), with a maximum of 90 mA for the worst case application

18 This specification is the maximum value and is a boundary for the dI specification.

19 Condition1: For power on period from 0 V up to normal operation with reset asserted. Condition 2: From reset asserted until PLL running free. Condition 3: Increasing PLL from free frequency to full frequency. Condition 4: reverse order for power down to 0 V.

20 I_{DDOFF} is the minimum guaranteed consumption of the device during power-up. It can be used to correctly size power-off ballast in case of current injection during power-off state.Power up/down current transients can be limited by controlling the clock ramp rates with the Progressive Clock Frequency Switching block on the device.

21 V_{STBY_BO} is the maximum voltage that sets the standby RAM brown-out flag in the device logic. The minimum voltage for RAM data retention is guaranteed to always be less than the V_{STBY_BO} maximum value.

22 The temperature coefficient and line regulation specifications are used to calculate the reference voltage drift at an operating point within the specified voltage and temperature operating conditions.

3.6 I/O pad specification

The following table describes the different pad type configurations.

Table 11. I/O pad specification descriptions

Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission. Pad impedance is centered around 800 Ω.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission. Pad impedance is centered around 200 Ω.
Strong configuration	Provides fast transition speed; used for fast interface. Pad impedance is centered around 50 Ω.
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface including Ethernet, FlexRay, and the EBI data bus interfaces requiring fine control of rising/falling edge jitter. Pad impedance is centered around 40 Ω.
EBI configuration	Provides necessary speed for fast external memory interfaces on the EBI address and control signals. Drive strength is matched to four selectable loads.

Table 11. I/O pad specification descriptions (continued)

Pad type	Description
Differential configuration	A few pads provide differential capability providing very fast interface together with good EMC performances.
Input only pads	These low input leakage pads are associated with the ADC channels.

NOTE

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

The device supports both 3.3 V and 5 V nominal I/O voltages. In order to use 3.3 V on the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment, the HV supply low voltage monitor (V_{LVD400}) must be disabled by DCF client. All other physical I/O segments are unaffected by the LVD400.

3.6.1 I/O input DC characteristics

Table 12 provides input DC electrical characteristics as described in Figure 7.

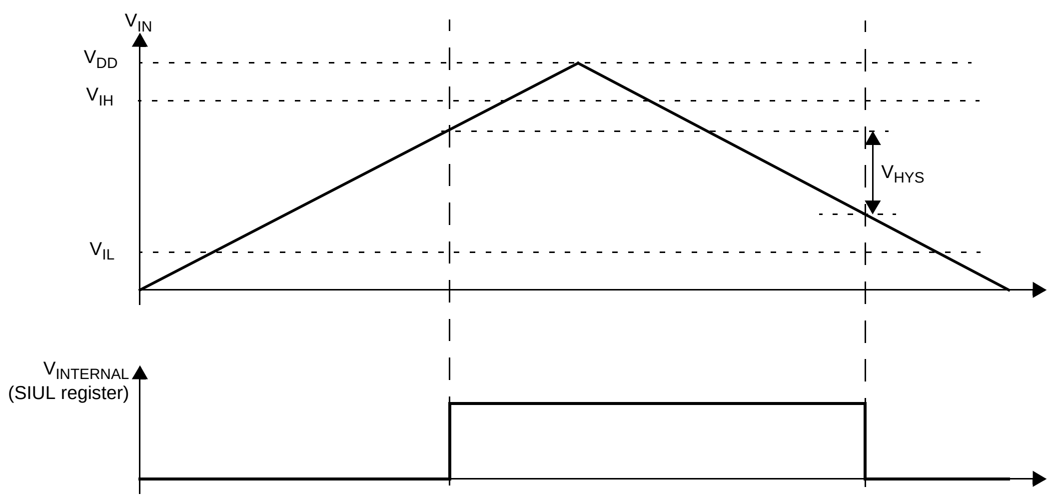


Figure 7. I/O input DC electrical characteristics definition

Table 12. I/O input DC electrical characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
TTL							
V_{IHTTL}	SR	Input high level TTL	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V[6]	2	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILTTL}	SR	Input low level TTL	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V[6]	–0.3	—	0.8	
V_{HYSTTL}	—	Input hysteresis TTL	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V[6]	0.275	—	—	

Table 12. I/O input DC electrical characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
$V_{DRFTTTL}$	—	Input V_{IL}/V_{IH} temperature drift TTL	—	—	—	100	mV
AUTOMOTIVE							
V_{IHAUT}[2]	SR	Input high level AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3.8	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ILAUT}[3]	SR	Input low level AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	–0.3	—	2.2	V
V_{HYSAUT}[4]	—	Input hysteresis AUTOMOTIVE	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	0.4	—	—	V
$V_{DRFTAUT}$	—	Input V_{IL}/V_{IH} temperature drift	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	100[5]	mV
CMOS/EBI							
V_{IHCMOS_H}[6]	SR	Input high level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.70 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{IHCMOS}[6]	SR	Input high level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.6 * $V_{DD\_HV\_IO}$	—	$V_{DD\_HV\_IO}$ + 0.3	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{ILCMOS_H}[6]	SR	Input low level CMOS (with hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	–0.3	—	0.35 * $V_{DD\_HV\_IO}$	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
V_{ILCMOS}[6]	SR	Input low level CMOS (without hysteresis)	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	–0.3	—	0.4 * $V_{DD\_HV\_IO}$	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
$V_{HYSCMOS}$	—	Input hysteresis CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	0.1 * $V_{DD\_HV\_IO}$	—	—	V
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V[7]				
$V_{DRFTCMOS}$	—	Input V_{IL}/V_{IH} temperature drift CMOS	3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	100[5]	mV
			4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V				
INPUT CHARACTERISTICS[8]							
I_{LKG}	CC	Digital input leakage	4.5 V < V_{DD_HV} < 5.5 V V_{SS_HV} < V_{IN} < V_{DD_HV} TJ = 150 °C	—	—	750	nA
I_{LKG_EBI}	CC	Digital input leakage for EBI pad	4.5 V < V_{DD_HV} < 5.5 V V_{SS_HV} < V_{IN} < V_{DD_HV} TJ = 150 °	—	—	750	nA
C_{IN}	CC	Digital input capacitance	GPIO input pins	—	—	7	pF
			EBI input pins	—	—	7	

1 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

2 A good approximation for the variation of the minimum value with supply is given by formula $V_{IHAUT} = 0.69 \times V_{DD\_HV\_IO}$.
3 A good approximation for the variation of the maximum value with supply is given by formula $V_{ILAUT} = 0.49 \times V_{DD\_HV\_IO}$.
4 A good approximation of the variation of the minimum value with supply is given by formula $V_{HYSAUT} = 0.11 \times V_{DD\_HV\_IO}$.
5 In a 1 ms period, assuming stable voltage and a temperature variation of ±30 °C, V_{IL}/V_{IH} shift is within ±50 mV. For SENT requirement refer to NOTE on page 41.
6 Only for $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_FLEX}$ power segment. The TTL threshold are controlled by the VSIO bit. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V.
7 Only for $V_{DD\_HV\_IO\_JTAG}$ and $V_{DD\_HV\_IO\_FLEX}$ power segment.
8 For LFAST, microsecond bus and LVDS input characteristics, refer to dedicated communication module chapters.

Table 13 provides weak pull figures. Both pull-up and pull-down current specifications are provided.

Table 13. I/O pull-up/pull-down DC electrical characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
$\|I_{WPU}\|$	CC	Weak pull-up current absolute value[2]	V_{IN} = 0 V V_{DD_POR}[3] < $V_{DD\_HV\_IO}$ < 3.0 V[4,5]	10.6 * V_{DD_HV} – 10.6	—	—	µA
			$V_{IN} > V_{IL}$ = 1.1 V (TTL) 4.5 V < V_{DD}< 5.5 V	—	—	130	
			V_{IN} = 0.75*$V_{DD\_HV\_IO}$ (AUTO) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	10	—	—	
			V_{IN} = 0.35* $V_{DD\_HV\_IO}$ (AUTO) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	70	
			V_{IN} = 0.35* $V_{DD\_HV\_IO}$ (CMOS) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	25	—	80	
			V_{IN} = 0.69* $V_{DD\_HV\_IO}$ (AUTO) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	23	—	—	
			V_{IN} = 0.49* $V_{DD\_HV\_IO}$ (AUTO) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	82	
			V_{IN} = 0.35* $V_{DD\_HV\_IO}$ (CMOS) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	120	
R_{WPU}	CC	Weak pull-up resistance	—	34	—	62	kΩ

Table 13. I/O pull-up/pull-down DC electrical characteristics (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
$\lvert I_{WPD}\rvert$	CC	Weak pull-down current absolute value	$V_{IN} < V_{IL}$ = 0.9 V (TTL) 4.5 V < V_{DD} < 5.5 V	16	—	—	µA
			V_{IN} = 0.75* $V_{DD\_HV\_IO}$ (AUTO) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	—	—	92	
			V_{IN} = 0.35* $V_{DD\_HV\_IO}$ (AUTO) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	19	—	—	
			V_{IN} = 0.65* $V_{DD\_HV\_IO}$ (CMOS) 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V	25	—	80	
			V_{IN} = 0.69* $V_{DD\_HV\_IO}$ (AUTO) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	—	—	130	
			V_{IN} = 0.49* $V_{DD\_HV\_IO}$ (AUTO) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	—	
			V_{IN} = 0.65* $V_{DD\_HV\_IO}$ (CMOS) 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	120	
R_{WPD}	CC	Weak pull-down resistance	—	30	—	55	kΩ

1 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

2 Weak pull-up/down is enabled within t_{WK_PU} = 1 µs after internal/external reset has been asserted. Output voltage will depend on the amount of capacitance connected to the pin.

3 V_{DD_POR} is the minimum $V_{DD\_HV\_IO}$ supply voltage for the activation of the device pull-up/down, and is given in the *Reset electrical characteristics* table of Section *Reset pad (PORST, ESR0) electrical characteristics* in this Data Sheet.

4 V_{DD_POR} is defined in the *Reset electrical characteristics* table of Section *Reset pad (PORST, ESR0) electrical characteristics* in this Data Sheet.

5 Weak pull-up behavior during power-up. Operational with $V_{DD\_HV\_IO} > V_{DD\_POR}$.

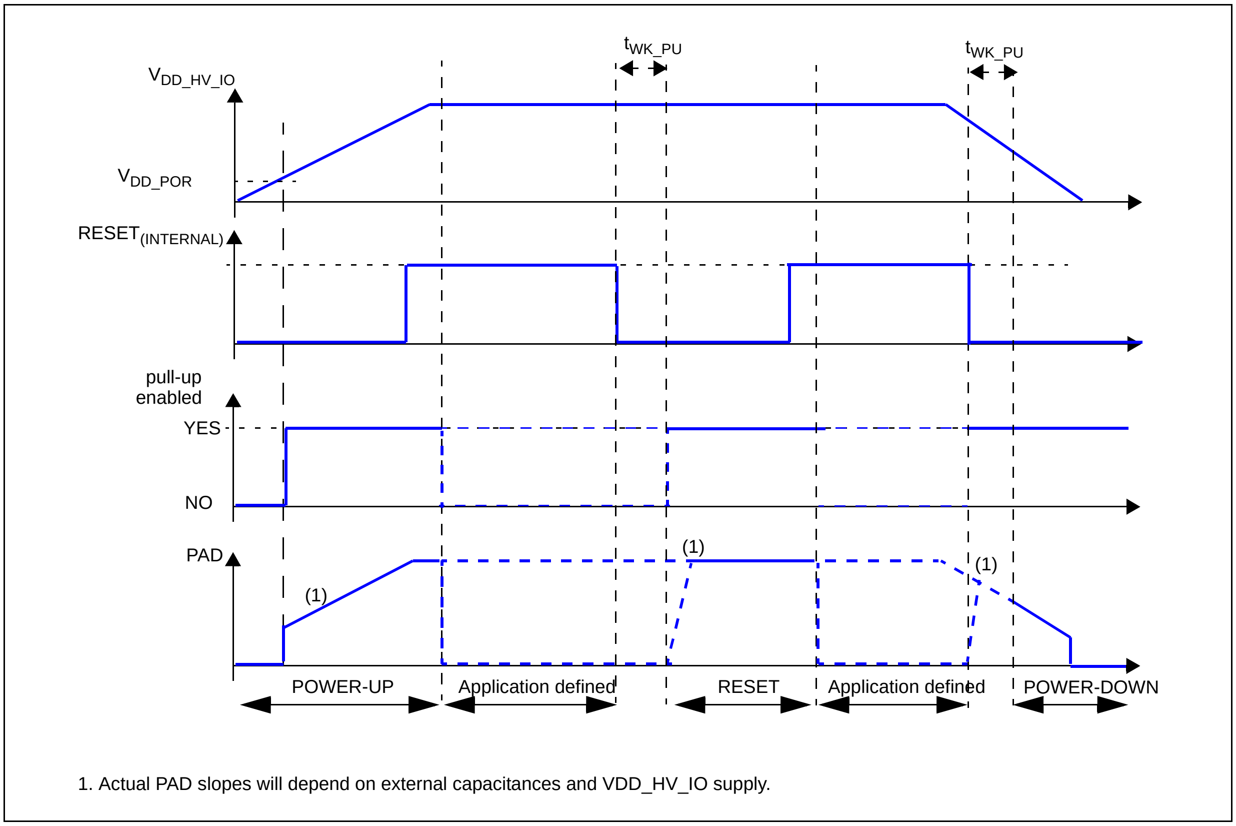


Figure 8. Weak pull-up electrical characteristics definition

3.6.2 I/O output DC characteristics

The figure below provides description of output DC electrical characteristics.

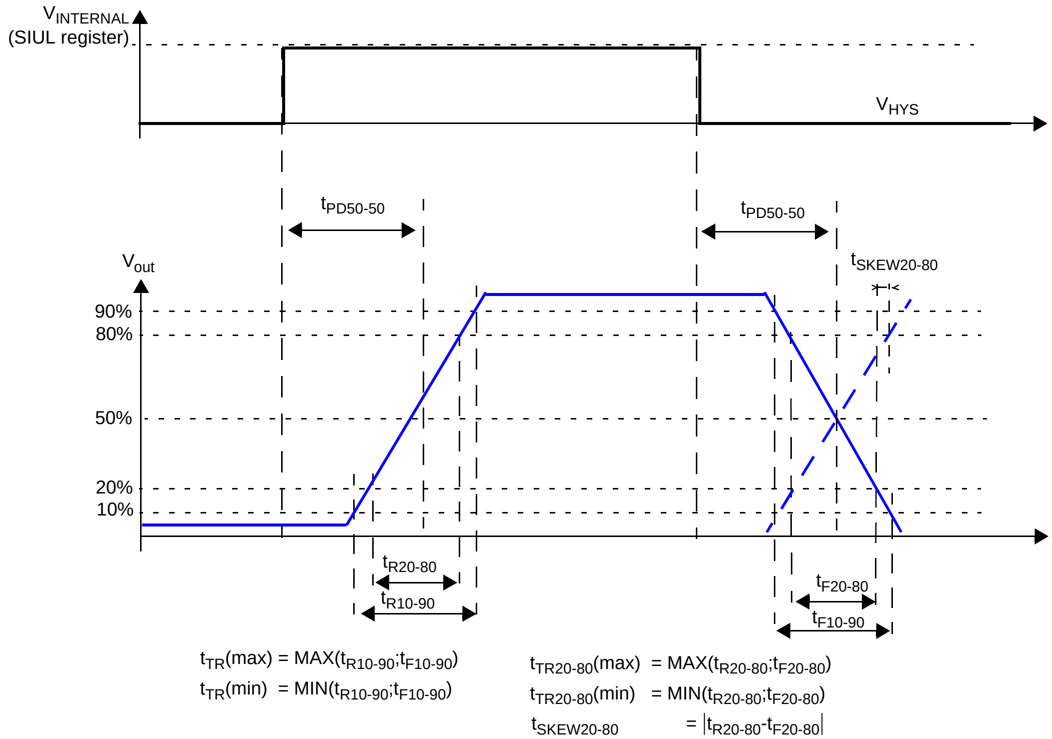


Figure 9. I/O output DC electrical characteristics definition

The following tables provide DC characteristics for bidirectional pads:

- Table 14 provides output driver characteristics for I/O pads when in WEAK configuration.
- Table 15 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 16 provides output driver characteristics for I/O pads when in STRONG configuration.
- Table 17 provides output driver characteristics for I/O pads when in VERY STRONG configuration.
- Table 18 provides output driver characteristics for the EBI pads.

NOTE

Driver configuration is controlled by SIUL2_MSCR*n* registers. It is available within two PBRIDGEA_CLK clock cycles after the associated SIUL2_MSCR*n* bits have been written.

Table 14 shows the WEAK configuration output buffer electrical characteristics.

Table 14. WEAK configuration output buffer electrical characteristics

Symbol		Parameter	Conditions[1,2]	Value			Unit
				Min	Typ	Max	
R_{OH_W}	CC	PMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 0.5 mA	520	800	1052	Ω
R_{OL_W}	CC	NMOS output impedance weak configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 0.5 mA	520	800	1052	Ω

Table 14. WEAK configuration output buffer electrical characteristics (continued)

Symbol		Parameter	Conditions[1,2]	Value			Unit
				Min	Typ	Max	
f_{MAX_W}	CC	Output frequency weak configuration	C_L = 25 pF[3]	—	—	2	MHz
			C_L = 50 pF[3]	—	—	1	
			C_L = 200 pF[3]	—	—	0.25	
t_{TR_W}	CC	Transition time output pin weak configuration[4]	C_L = 25 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	40	—	120	ns
			C_L = 50 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	80	—	240	
			C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	320	—	820	
			C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	50	—	150	
			C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	100	—	300	
			C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[5]	350	—	1050	
$\|t_{SKEW\_W}\|$	CC	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_W}	CC	Maximum DC current	—	—	—	4	mA

1 All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0

2 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

3 C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in Table 12) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).

4 Transition time maximum value is approximated by the following formula:

0 pF < C_L < 50 pF t_{TR_W}(ns) = 22 ns + C_L(pF) × 4.4 ns/pF

50 pF < C_L < 200 pF t_{TR_W}(ns) = 50 ns + C_L(pF) × 3.85 ns/pF

5 Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0.

Table 15 shows the MEDIUM configuration output buffer electrical characteristics.

Table 15. MEDIUM configuration output buffer electrical characteristics

Symbol		Parameter	Conditions[1,2]	Value			Unit
				Min	Typ	Max	
R_{OH_M}	CC	PMOS output impedance MEDIUM configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 2 mA	135	200	260	Ω
R_{OL_M}	CC	NMOS output impedance MEDIUM configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 2 mA	135	200	260	Ω

Table 15. MEDIUM configuration output buffer electrical characteristics (continued)

Symbol		Parameter	Conditions[1,2]	Value			Unit
				Min	Typ	Max	
f_{MAX_M}	CC	Output frequency MEDIUM configuration	C_L = 25 pF[3]	—	—	12	MHz
			C_L = 50 pF[3]	—	—	6	
			C_L = 200 pF[3]	—	—	1.5	
$t_{TPD50-50}$[4]	CC	50-50 % Output pad propagation delay time	$V_{DD\_HV\_IO}$ = 5 V +/- 10 %, C_L = 25 pF	—	—	21/17	ns
			$V_{DD\_HV\_IO}$ = 5.0 V +/- 10 %, C_L = 50 pF	—	—	35/27	ns
t_{TR_M}	CC	Transition time output pin MEDIUM configuration[5]	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	10	—	30	ns
			C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	20	—	60	
			C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	60	—	200	
			C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	12	—	42	
			C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	24	—	86	
			C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	70	—	300	
$\|t_{SKEW\_M}\|$	CC	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_M}	CC	Maximum DC current	—	—	—	4	mA

1 All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0

2 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

3 C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in Table 12) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).

4 If two values are given for propagation delay, the first value is for rising edge signals and the second for falling edge signals.

5 Transition time maximum value is approximated by the following formula:

0 pF < C_L < 50 pF t_{TR_M}(ns) = 5.6 ns + C_L(pF) × 1.11 ns/pF

50 pF < C_L < 200 pF t_{TR_M}(ns) = 13 ns + C_L(pF) × 0.96 ns/pF

6 Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0

Table 16 shows the STRONG configuration output buffer electrical characteristics.

Table 16. STRONG configuration output buffer electrical characteristics

Symbol		Parameter	Conditions[1,2]	Value			Unit
				Min	Typ	Max	
R_{OH_S}	CC	PMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	30	50	77	Ω
R_{OL_S}	CC	NMOS output impedance STRONG configuration	4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	30	50	77	Ω
f_{MAX_S}	CC	Output frequency STRONG configuration	C_L = 25 pF[3]	—	—	40	MHz
			C_L = 50 pF[3]	—	—	20	
			C_L = 200 pF[3]	—	—	5	
$t_{TPD50-50}$[4]	CC	50-50 % Output pad propagation delay time	$V_{DD\_HV\_IO}$ = 5 V +/- 10 %, C_L = 25 pF	—	—	8/7	ns
			$V_{DD\_HV\_IO}$ = 5.0 V +/- 10 %, C_L = 50 pF	—	—	11/9	ns
t_{TR_S}	CC	Transition time output pin STRONG configuration[5]	C_L = 25 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	3	—	10	ns
			C_L = 50 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	5	—	16	
			C_L = 200 pF 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V	17	—	50	
			C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	4	—	15	
			C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	6	—	27	
			C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V[6]	20	—	83	
$\|t_{SKEW\_S}\|$	CC	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_S}	CC	Maximum DC current	—	—	—	10	mA

1 All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0

2 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

3 C_L is the sum of external capacitance. Device and package capacitances (C_{IN}, defined in Table 12) are to be added to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).

4 If two values are given for propagation delay, the first value is for rising edge signals and the second for falling edge signals.

5 Transition time maximum value is approximated by the following formula: t_{TR_S}(ns) = 4.5 ns + C_L(pF) x 0.23 ns/pF.

6 Only for $V_{DD\_HV\_IO\_JTAG}$ segment when VSIO[VSIO_IJ] = 0 or $V_{DD\_HV\_IO\_FLEX}$ segment when VSIO[VSIO_IF] = 0

Table 17 shows the VERY STRONG configuration output buffer electrical characteristics.

Table 17. VERY STRONG configuration output buffer electrical characteristics[1]

Symbol		Parameter	Conditions[2,3]	Value			Unit
				Min	Typ	Max	
R_{OH_V}	CC	PMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1 I_{OH} = 8 mA	20	40	72	Ω
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OH} = 7 mA[4]	30	50	90	
R_{OL_V}	CC	NMOS output impedance VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, VSIO[VSIO_xx] = 1 I_{OL} = 8 mA	20	40	72	Ω
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, VSIO[VSIO_xx] = 0, I_{OL} = 7 mA[4]	30	50	90	
f_{MAX_V}	CC	Output frequency VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	—	—	50	MHz
			VSIO[VSIO_xx] = 1, C_L = 15 pF[4,5]	—	—	50	
$t_{TPD50-50}$[6]	CC	50-50 % Output pad propagation delay time	$V_{DD\_HV\_IO}$ = 5 V +/- 10 %, C_L = 25 pF	—	—	5.5	ns
			$V_{DD\_HV\_IO}$ = 5.0 V +/- 10 %, C_L = 50 pF	—	—	6.5	ns
			$V_{DD\_HV\_IO}$ = 3.3 V +/- 10 %, C_L = 15 pF	—	—	7.3/7.6	ns
t_{TR_V}	CC	10–90% threshold transition time output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	1	—	5.3	ns
			$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 50 pF[5]	3	—	12	
			$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 200 pF[5]	14	—	45	
$t_{TR20-80}$	CC	20–80% threshold transition time[7] output pin VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	0.8	—	4	ns
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF[5]	1	—	5	
t_{TRTTL}	CC	TTL threshold transition time[8] for output pin in VERY STRONG configuration	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 25 pF[5]	1	—	5	ns
$\Sigma t_{TR20-80}$	CC	Sum of transition time 20–80% output pin VERY STRONG configuration[9]	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF	—	—	9	ns
			$V_{DD\_HV\_IO}$ = 3.3 V ± 10%, C_L = 15 pF[5]	—	—	9	
$\lvert t_{SKEW\_V} \rvert$	CC	Difference between rise and fall time at 20–80%	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 25 pF[5]	0	—	1	ns

Table 17. VERY STRONG configuration output buffer electrical characteristics[1] (continued)

Symbol		Parameter	Conditions[2,3]	Value			Unit
				Min	Typ	Max	
I_{DCMAX_VS}	CC	Maximum DC current	—	—	—	10	mA

1 Refer to FlexRay section for parameter dedicated to this interface.

2 All VDD_HV_IO conditions for 4.5V to 5.5V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0.

3 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characteristics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

4 Only available on the $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEXE}$, and $V_{DD\_HV\_IO\_FLEX}$ segments.

5 C_L is the sum of external capacitance. Add device and package capacitances (C_{IN}, defined in the *I/O input DC electrical characteristics* table in this Data Sheet) to calculate total signal capacitance ($C_{TOT} = C_L + C_{IN}$).

6 If two values are given for propagation delay, the first value is for rising edge signals and the second for falling edge signals.

7 20–80% transition time as per FlexRay standard.

8 TTL transition time as for Ethernet standard.

9 For specification per Electrical Physical Layer Specification 3.0.1, see the $dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$ (Sum of Rise and Fall time of TxD signal at the output pin) specification in *TxD output characteristics* table in Section *TxD* of this Data Sheet.

Table 18 shows the EBI pad electrical specification.

Table 18. EBI pad output electrical specification

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
EBI Mode Output Specifications[1]							
C_{DRV}	CC	External Bus Load Capacitance	MSCR[OERC] = b101	—	—	10	pF
			MSCR[OERC] = b110	—	—	20	
			MSCR[OERC] = b111	—	—	30	
f_{MAX_EBI}	CC	External Bus Maximum Operating Frequency	C_{DRV} = 10/20/30 pF	—	—	66.7	MHz
t_{TR_EBI}	CC	10%–90% threshold transition time External Bus output pins	C_{DRV}= 10/20/30 pF	0.9	—	3.0	ns
t_{PD_EBI}	CC	50%–50% threshold propagation delay time External Bus output pins	C_{DRV} = 10/20/30 pF	1.9	—	4.0	ns
$\|t_{SKEW\_EBI}\|$	CC	Difference between rise and fall time	—	—	—	25	%
I_{DCMAX_EBI}	CC	Maximum DC current	—	—	—	12	mA
GPIO Mode Output Specifications - MSCR[OERC] = b100							

Table 18. EBI pad output electrical specification (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$R_{OH\_EBI\_GPIO}$	CC	PMOS output impedance	4.5 V < $V_{DD\_HV\_IO\_EBI}$ < 5.5 V Push pull, I_{OH} < 2 mA	100	225	400	Ω
$R_{OL\_EBI\_GPIO}$	CC	NMOS output impedance	4.5 V < $V_{DD\_HV\_IO\_EBI}$ < 5.5 V Push pull, I_{OH} < 2 mA	100	200	400	Ω
$f_{MAX\_EBI\_GPIO}$	CC	Output frequency	C_L = 25 pF[2]	—	—	12	MHz
			C_L = 50 pF	—	—	6	
			C_L = 200 pF	—	—	1.5	
$I_{DCMAX\_EBI\_GPIO}$	CC	Maximum DC current	—	—	—	4	mA

[1] All EBI mode specifications are valid for $V_{DD\_HV\_IO\_EBI}$ = 3.3V +/- 10%.

[2] C_L is the sum of the capacitance loading external to the device.

3.7 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair.

Table 19 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment remain below the I_{MAXSEG} value given in the Table 6 (Absolute maximum ratings). Use the RMS current consumption values to calculate total segment current.

In order to ensure device functionality, the sum of the dynamic and static currents of the I/O on a single segment should remain below the I_{MAXSEG} value given in the Table 8 (Device operating conditions). Use the dynamic current consumption values to calculate total segment current.

Pad mapping on each segment can be optimized using the pad usage information provided in the I/O Signal Description table. The sum of all pad usage ratios within a segment should remain below 100%.

NOTE

In order to maintain the required input thresholds for the SENT interface, the sum of all I/O pad output percent IR drop as defined in the I/O Signal Description table, must be below 50 %. See the I/O Signal Description attachment.

NOTE

The MPC5777M I/O Signal Description and Input Multiplexing Tables are contained in a Microsoft Excel® workbook file attached to this document. Locate the paperclip symbol on the left side of the PDF window, and click it. Double-click on the Excel file to open it and select the I/O Signal Description Table tab.

Table 19. I/O consumption[1]

Symbol		Parameter	Conditions[2]	Value			Unit
				Min	Typ	Max	
I_{RMS_W}	CC	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	mA
			C_L = 50 pF, 1 MHz V_{DD} = 5.0 V ± 10%	—	—	1.1	
			C_L = 25 pF, 2 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
			C_L = 50 pF, 1 MHz V_{DD} = 3.3 V ± 10%	—	—	0.6	
I_{RMS_M}	CC	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz V_{DD} = 5.0 V ± 10%	—	—	4.7	mA
			C_L = 50 pF, 6 MHz V_{DD} = 5.0 V ± 10%	—	—	4.8	
			C_L = 25 pF, 12 MHz V_{DD} = 3.3 V ± 10%	—	—	2.6	
			C_L = 50 pF, 6 MHz V_{DD} = 3.3 V ± 10%	—	—	2.7	
I_{RMS_S}	CC	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz V_{DD} = 5.0 V ± 10%	—	—	19	mA
			C_L = 50 pF, 25 MHz V_{DD} = 5.0 V ± 10%	—	—	19	
			C_L = 25 pF, 50 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
			C_L = 50 pF, 25 MHz V_{DD} = 3.3 V ± 10%	—	—	10	
I_{RMS_V}	CC	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0V +/- 10%	—	—	22	mA
			C_L = 50 pF, 25 MHz, V_{DD} = 5.0V ± 10%	—	—	22	
			C_L = 25 pF, 50 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
			C_L = 25 pF, 25 MHz, V_{DD} = 3.3V ± 10%	—	—	11	
I_{RMS_EBI}	CC	RMS I/O current for External Bus output pins	C_{DRV} = 6 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	9	mA
			C_{DRV} = 12 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	15	
			C_{DRV} = 18 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	27	
			C_{DRV} = 30 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	42	

Table 19. I/O consumption[1]

Symbol		Parameter	Conditions[2]	Value			Unit
				Min	Typ	Max	
I_{DYN_W}[3]	CC	Dynamic I/O current for WEAK configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	5.0	mA
			C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	5.1	
			C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	2.2	
			C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	2.3	
I_{DYN_M}	CC	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	15	mA
			C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	15.5	
			C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	7.0	
			C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	7.1	
I_{DYN_S}	CC	Dynamic I/O current for STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	50	mA
			C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	55	
			C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	22	
			C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	25	
I_{DYN_V}	CC	Dynamic I/O current for VERY STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	60	mA
			C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	64	
			C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	26	
			C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	29	
I_{DYN_EBI}[4]	CC	Dynamic I/O current for External Bus output pins	C_{DRV} = 10 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	30	mA
			C_{DRV} = 20 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	50	
			C_{DRV} = 30 pF, f_{EBI} = 66.7 MHz, $V_{DD\_HV\_IO\_EBI}$ = 3.3 V ± 10%	—	—	80	

1 I/O current consumption specifications for the 4.5 V <= $V_{DD\_HV\_IO}$ <= 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V <= $V_{DD\_HV\_IO}$ <= 3.6 V.

2 During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characterstics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.

3 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

4 For $I_{DYN\_EBI\_GPIO}$ dynamic current for EBI GPIO mode use the I_{DYN_M} values.

3.8 Reset pad ($\overline{\text{PORST}}$, $\overline{\text{ESR0}}$) electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

NOTE

$\overline{\text{PORST}}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 kΩ.

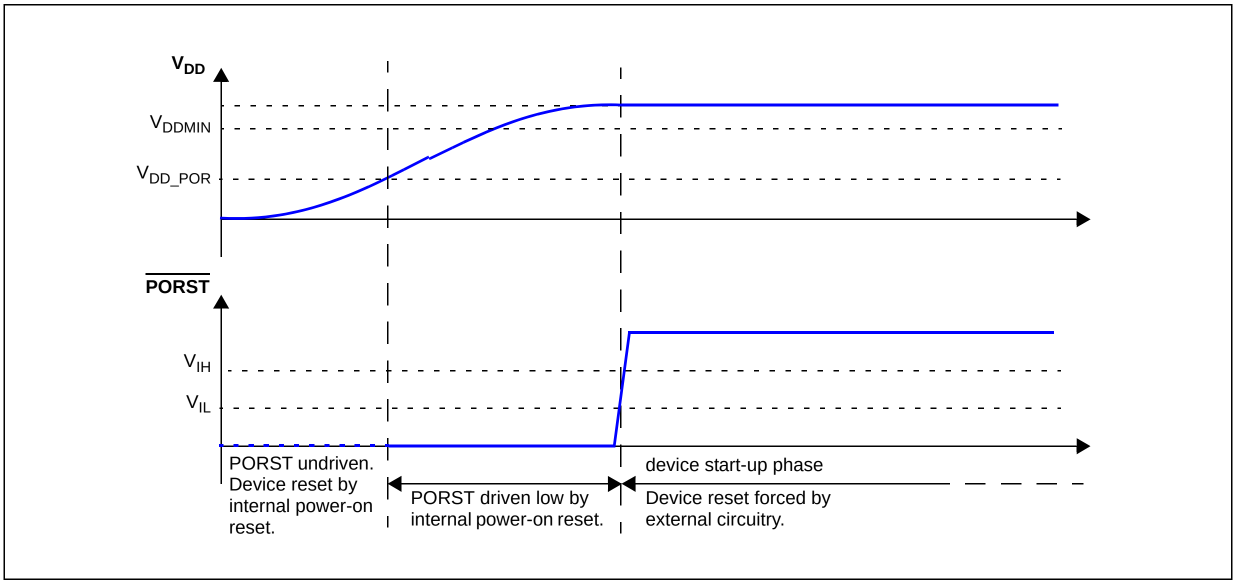


Figure 10. Start-up reset requirements

Figure 11 describes device behavior depending on supply signal on $\overline{\text{PORST}}$:

1. $\overline{\text{PORST}}$ low pulse amplitude is too low—it is filtered by input buffer hysteresis. Device remains in current state.
2. $\overline{\text{PORST}}$ low pulse duration is too short—it is filtered by a low pass filter. Device remains in current state.
3. $\overline{\text{PORST}}$ low pulse generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown: it may either be reset or remains in current state depending on other factors (temperature, voltage, device).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. Device is under reset.

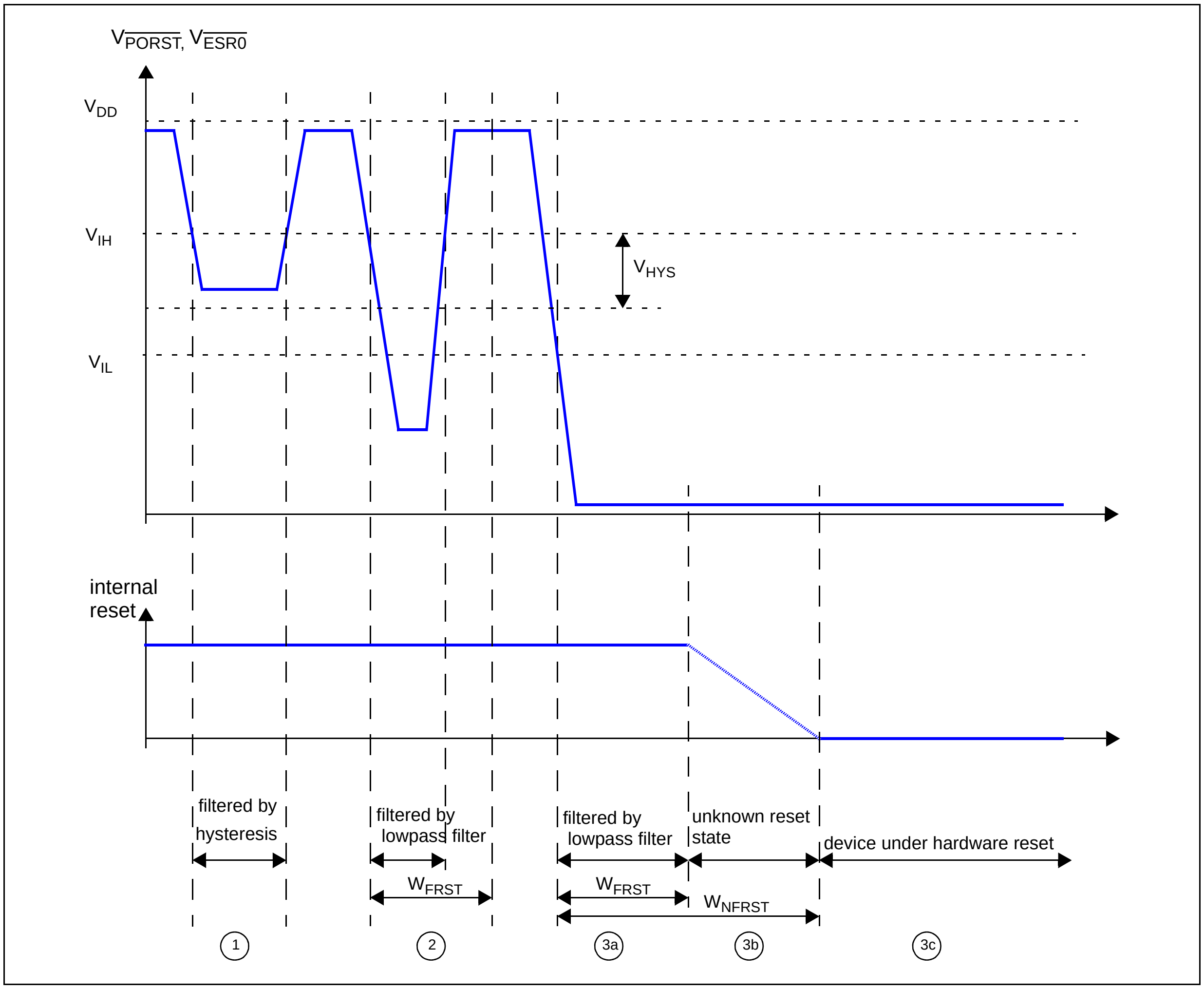


Figure 11. Noise filtering on reset signal

Table 20. Reset electrical characteristics

Symbol		Parameter	Conditions	Value[1]			Unit
				Min	Typ	Max	
V_{IH}	SR	Input high level TTL (Schmitt trigger)	—	2.2	—	$V_{DD\_HV\_IO}$ +0.4	V
V_{IL}	SR	Input low level TTL (Schmitt trigger)	—	–0.4	—	0.8	V
V_{HYS}	CC	Input hysteresis TTL (Schmitt trigger)	—	300	—	—	mV
V_{DD_POR}	CC	Minimum supply for strong pull-down activation	—	—	—	1.2	V

Table 20. Reset electrical characteristics (continued)

Symbol		Parameter	Conditions	Value[1]			Unit
				Min	Typ	Max	
I_{OL_R}	CC	Strong pull-down current[2]	Device under power-on reset $V_{DD\_HV\_IO} = V_{DD\_POR}$, $V_{OL} = 0.35 * V_{DD\_HV\_IO}$	0.2	—	—	mA
			Device under power-on reset 3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V, V_{OL} > 0.9 V	11	—	—	mA
$\|I_{WPU}\|$	CC	Weak pull-up current absolute value	$\overline{ESR0}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	23	—	—	µA
			$\overline{ESR0}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	—	—	82	
$\|I_{WPD}\|$	CC	Weak pull-down current absolute value	$\overline{PORST}$ pin $V_{IN} = 0.69 * V_{DD\_HV\_IO}$	—	—	130	µA
			$\overline{PORST}$ pin $V_{IN} = 0.49 * V_{DD\_HV\_IO}$	40	—	—	
W_{FRST}	SR	$\overline{PORST}$ and $\overline{ESR0}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	SR	$\overline{PORST}$ and $\overline{ESR0}$ input not filtered pulse	—	2000	—	—	ns
W_{FNMI}	SR	ESR1 input filtered pulse	—	—	—	15	ns
W_{NFNMI}	SR	ESR1 input not filtered pulse	—	400	—	—	ns

1 An external 4.7 KOhm pull-up resistor is recommended to be used with the PORST and ESR0 pins for fast negation of the signals.

2 I_{OL_R} applies to both PORST and ESR0: Strong pull-down is active on PHASE0 for PORST. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for ESR0.

NOTE

$\overline{PORST}$ can optionally be connected to an external power-on supply circuitry.

NOTE

No restrictions exist on reset signal slew rate apart from absolute maximum rating compliance.

3.9 Oscillator and FMPLL

The Reference PLL (PLL0) and the System PLL (PLL1) generate the system and auxiliary clocks from the main oscillator driver.

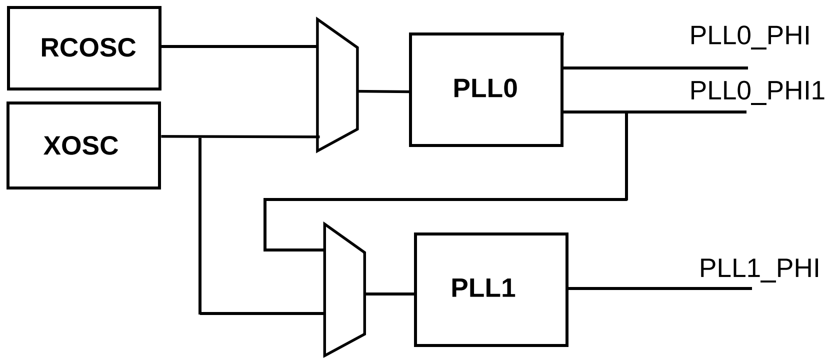


Figure 12. PLL integration

Table 21. PLL0 electrical characteristics

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{PLL0IN}	SR	PLL0 input clock[1,2]	—	8	—	44	MHz
Δ_{PLL0IN}	SR	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	CC	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0VCOFR}$	CC	PLL0 VCO free running frequency	—	35	—	400	MHz
$f_{PLL0PHI}$	CC	PLL0 output frequency	—	4.762	—	400	MHz
$t_{PLL0LOCK}$	CC	PLL0 lock time	—	—	—	110	µs
$\|\Delta_{PLL0PHISPJ}\|$	CC	PLL0_PHI single period jitter[3] f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI}$ = 400 MHz, 6-sigma	—	—	200	ps
$\|\Delta_{PLL0PHI1SPJ}\|$	CC	PLL0_PHI1 single period jitter[3] f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[4]	ps

Table 21. PLL0 electrical characteristics (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$\Delta_{PLL0LTJ}$	CC	PLL0 output long term jitter[3,4] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
			16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
			long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	CC	PLL0 consumption	FINE LOCK state	—	—	5	mA

1 f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure PFD input signal is in the range 8 MHz–20 MHz.

2 PLL0IN clock retrieved directly from either internal RCOSC or external XOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.

3 PLL jitter is guaranteed when transient currents on the V_{DDLV} supply are within the I_{SPIKE} parameter value in Table 10 (DC electrical specifications).

4 Noise on the V_{DD_LV} supply with frequency content below 40 KHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD_LV} supply with frequency content in the range of 40 KHz – 50 MHz must be filtered externally to the device.

Table 22. PLL1 electrical characteristics

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{PLL1IN}	SR	PLL1 input clock[1]	—	38	—	78	MHz
Δ_{PLL1IN}	SR	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	CC	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1VCOFR}$	CC	PLL1 VCO free running frequency	—	35	—	400	MHz
$f_{PLL1PHI}$	CC	PLL1 output clock PHI	—	4.762	—	600	MHz
$t_{PLL1LOCK}$	CC	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	CC	PLL1 modulation frequency	—	—	—	250	kHz
$\|\delta_{PLL1MOD}\|$	CC	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
			Down spread	0.5	—	4	%
I_{PLL1}	CC	PLL1 consumption	FINE LOCK state	—	—	6	mA

1 PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator is used in functional mode.

Table 23. External Oscillator electrical specifications[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
f_{XTAL}	CC	Crystal Frequency Range[2]	—	4	8	MHz
			—	>8	20	
			—	>20	40	
t_{cst}	CC	Crystal start-up time [3,4]	T_J = 150 °C	—	5	ms
t_{rec}	CC	Crystal recovery time[5]	—	—	0.5	ms
V_{IHEXT}	CC	EXTAL input high voltage[6,7] (External Clock Input)	$V_{REF} = 0.28 * V_{DD\_HV\_IO\_JTAG}$	V_{REF} + 0.6	—	V
V_{ILEXT}	CC	EXTAL input low voltage[6,7] (External Clock Input)	$V_{REF} = 0.28 * V_{DD\_HV\_IO\_JTAG}$	—	V_{REF} - 0.6	V
C_{S_xtal}	CC	Total on-chip stray capacitance on XTAL/EXTAL pins[8]	BGA416, BGA512	8	8.6	pF
V_{EXTAL}	CC	Oscillation Amplitude on the EXTAL pin after startup[9]	T_J = –40 °C to 150 °C	0.5	1.6	V
V_{HYS}	CC	Comparator Hysteresis	T_J = –40 °C to 150 °C	0.1	1.0	V
I_{XTAL}	CC	XTAL current[13,10]	T_J = –40 °C to 150 °C	—	14	mA

1 All oscillator specifications are valid for VDD_HV_IO_JTAG = 3.0 V – 5.5 V.

2 The range is selectable by UTEST miscellaneous DCF clients XOSC_LF_EN and XOSC_EN_40MHZ.

3 This value is determined by the crystal manufacturer and board design.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.

6 This parameter is guaranteed by design rather than 100% tested.

7 Applies to an external clock input and not to crystal mode.

8 See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.

9 Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.

10 I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in Figure 13.

Table 24. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Load capacitance[1,2] (pF)
00000	1.032
00001	1.976
00010	2.898
00011	3.823
00100	4.751
00101	5.679
00110	6.605
00111	7.536
01000	8.460
01001	9.390
01010	10.317
01011	11.245
01100	12.173
01101	13.101
01110	14.029
01111	14.957

1 Values are determined from simulation across process corners and voltage and temperature variation. Capacitance values vary ±12% across process, 0.25% across voltage, and no variation across temperature.

2 Values in this table do not include the die and package capacitances given by Cs_xtal/Cs_extal in Table 23 (External Oscillator electrical specifications).

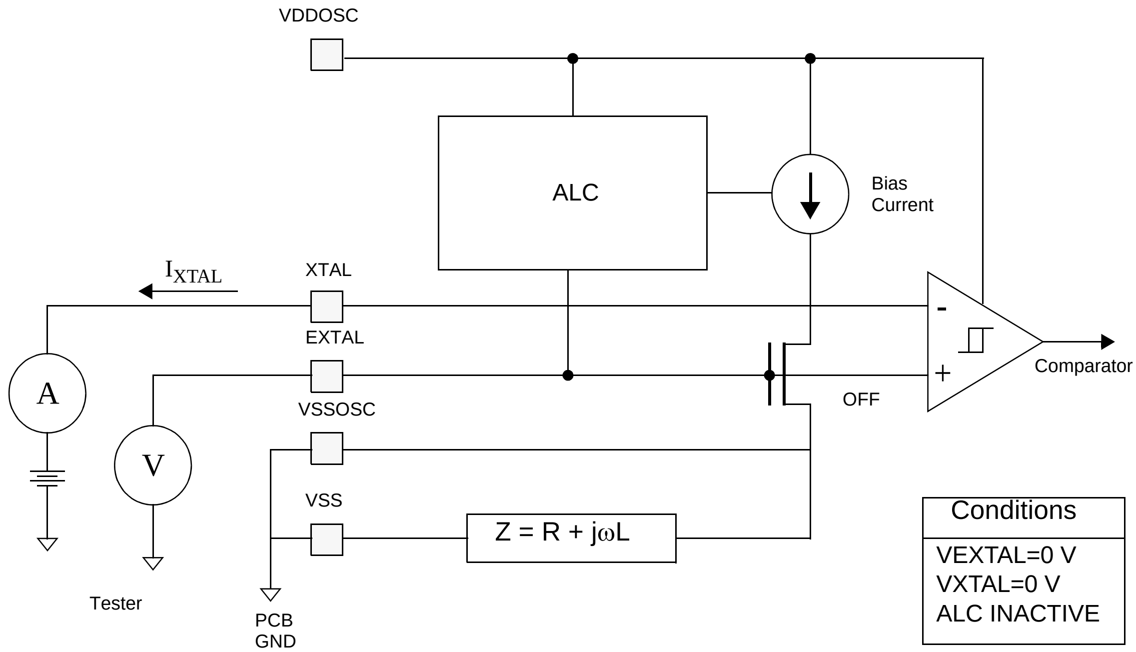


Figure 13. Test circuit

Table 25. Internal RC Oscillator electrical specifications

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{Target}	CC	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	IRC frequency variation without temperature compensation	T < 150 ^{o}C	–8	—	8	%
δf_{var_T}	CC	IRC frequency variation with temperature compensation	T < 150 ^{o}C	–3	—	3	%
δf_{var_SW}[1]	CC	IRC software trimming accuracy	Trimming temperature	–1	—	1	%
δf_{TPIM}		IRC Software trimming step	—	-48	—	+40	kHz
T_{start_noT}	CC	Startup time to reach within f_{var_noT}	No trimming	—	—	5	µs
T_{start_T}	CC	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs
I_{AVDD5}	CC	Current consumption on 5 V power supply	After T_{start_T}	—	—	400	µA
I_{DVDD12}	CC	Current consumption on 1.2 V power supply	After T_{start_T}	—	—	175	µA

1 IRC software trimmed accuracy is performed either with the CMU_0 clock monitor, using the XOSC as a reference or through the CCCU (CAN clock control Unit), extracting reference clock from CAN master clock. Software trim must be repeated as the device operating temperature varies in order to maintain the specified accuracy.

3.10 ADC specifications

3.10.1 ADC input description

Figure 14 shows the input equivalent circuit for fast SARn channels.

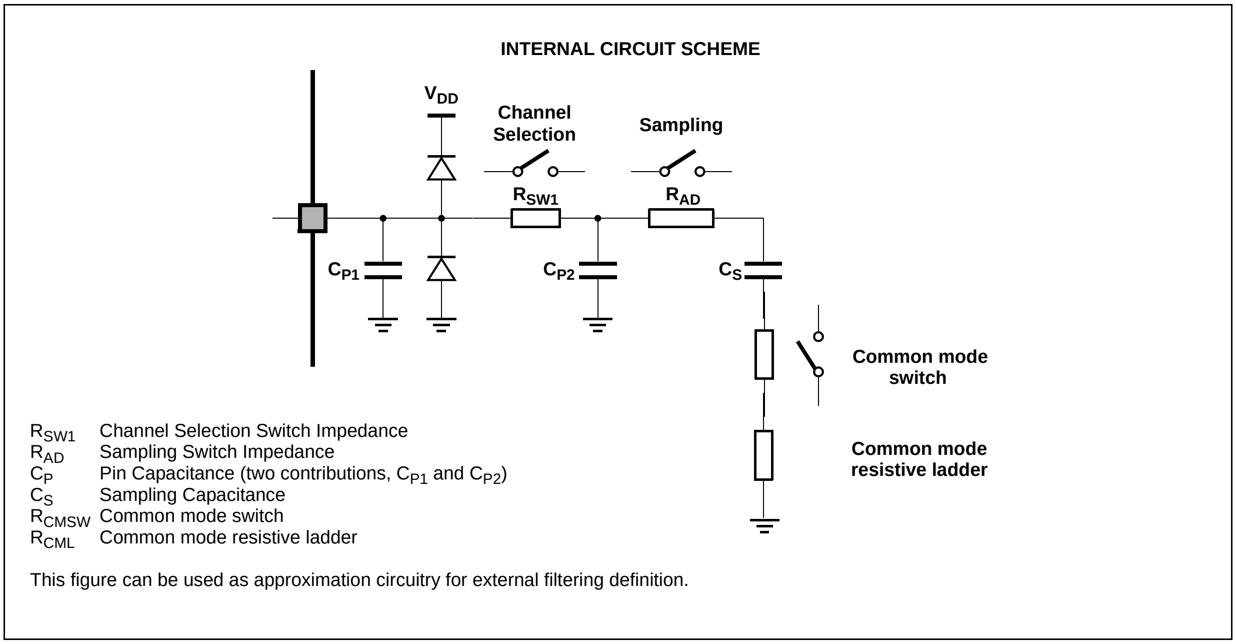


Figure 14. Input equivalent circuit (Fast SARn channels)

Figure 15 shows the input equivalent circuit for SARB channels.

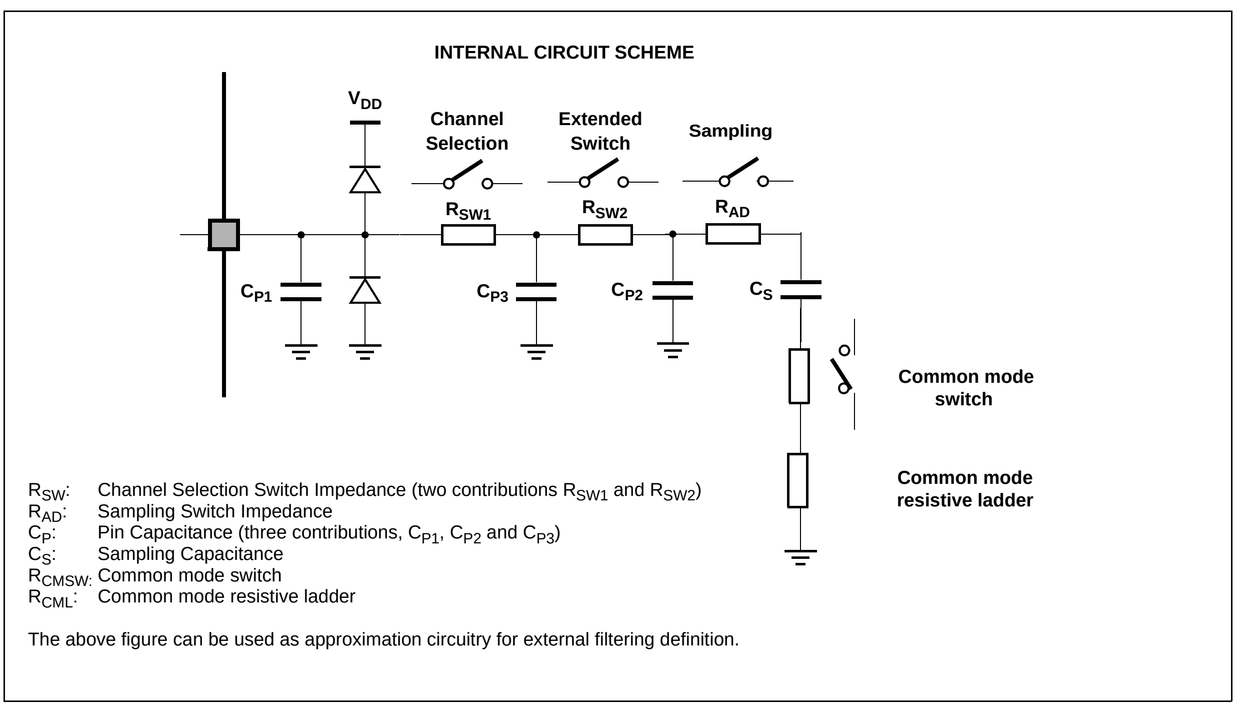


Figure 15. Input equivalent circuit (SARB channels)

Table 26. ADC pin specification[1]

Symbol		Parameter	Conditions	Value Min	Value Max	Unit
I_{LK_INUD}	CC	Input leakage current, two ADC channels input with weak pull-up and weak pull-down	T_J < 40 °C	—	50	nA
			T_J < 150 °C	—	150	
I_{LK_INUSD}	CC	Input leakage current, two ADC channels input with weak pull-up and strong pull-down	T_J < 40 °C	—	80	nA
			T_J < 150 °C	—	250	
I_{LK_INREF}	CC	Input leakage current, two ADC channels input with weak pull-up and weak pull-down and alternate reference	T_J < 40 °C	—	160	nA
			T_J < 150 °C	—	400	
I_{LK_INOUT}	CC	Input leakage current, two ADC channels input, GPIO output buffer with weak pull-up and weak pull-down	T_J < 40 °C	—	140	nA
			T_J < 150 °C	—	380	
I_{INJ}	CC	Injection current on analog input preserving functionality	Applies to any analog pins	–3	3	mA
C_{HV_ADC}	SR	$V_{DD\_HV\_ADV}$ external capacitance[2]		1	2.2	µF
C_{P1}	CC	Pad capacitance	—	0	10	pF
C_{P2}	CC	Internal routing capacitance	SARn channels	0	0.5	pF
			SARB channels	0	1	
C_{P3}	CC	Internal routing capacitance	Only for SARB channels	0	1	pF
C_S	CC	SAR ADC sampling capacitance	—	6	8.5	pF
R_{SWn}	CC	Analog switches resistance	SARn channels	0	1.1	kΩ
			SARB channels	0	1.7	
R_{AD}	CC	ADC input analog switches resistance	—	0	0.6	kΩ
R_{CMSW}	CC	Common mode switch resistance	—	0	2.6	kΩ
R_{CMRL}	CC	Common mode resistive ladder	—	0	3.5	kΩ
R_{SAFEPD}[3]	CC	Discharge resistance for AN7/AN35 channels (strong pull-down for safety)	—	0	300	Ω

1 All specifications in this table valid for the full input voltage range for the analog inputs.

2 For noise filtering, add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.

3 Safety pull-down is available for port pin PB[5] and PE[14].

3.10.2 SAR ADC electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Table 27. SARn ADC electrical specification[1]

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{ALTREF}	SR	ADC alternate reference voltage	$V_{ALTREF} < V_{DD\_HV\_IO\_MAIN}$	2.0	$V_{DD\_HV\_ADV\_S}$	V
V_{IN}	SR	ADC input signal	$0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$V_{SS\_HV\_ADR\_S}$	$V_{DD\_HV\_ADR\_S}$	V
f_{ADCK}	SR	Clock frequency	$T_J < 150$ °C	7.5	14.6	MHz
$t_{ADCPRECH}$	SR	ADC precharge time	Fast SAR—fast precharge	135	—	ns
			Fast SAR—full precharge	270	—	
			Slow SAR (SARADC_B)—fast precharge	270	—	
			Slow SAR (SARADC_B)—full precharge	540	—	
ΔV_{PRECH}	SR	Precharge voltage precision	Full precharge $V_{PRECH} = V_{DD\_HV\_ADR\_S}/2$ $T_J < 150$ °C	–0.25	0.25	V
			Fast precharge $V_{PRECH} = V_{DD\_HV\_ADR\_S}/2$ $T_J < 150$ °C	–0.5	0.5	V
ΔV_{INTREF}	CC	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR\_S}$, 1/3 * $V_{DD\_HV\_ADR\_S}$, 2/3 * $V_{DD\_HV\_ADR\_S}$, $V_{DD\_HV\_ADR\_S}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	ADC sample time[2]	Fast SAR – 12-bit configuration	0.750	—	µs
			Slow SAR (SARADC_B) – 12-bit configuration	1.500	—	
$t_{ADCEVAL}$	SR	ADC evaluation time	12-bit configuration (25 clock cycles)	1.712	—	µs
$I_{ADCREFH}$[3,4]	CC	ADC high reference current	Run mode $t_{conv} \geq 5$ µs (average across all codes)	—	7	µA
			Run mode $t_{conv} = 2.5$ µs (average across all codes)	—	7	
			Power Down mode	—	6	
			Bias Current[5]	—	+2	
$I_{ADCREFL}$[4]	CC	ADC low reference current	Run mode $t_{conv} \geq 5$ µs $V_{DD\_HV\_ADR\_S} <= 5.5$ V	—	15	µA
			Run mode $t_{conv} = 2.5$ µs $V_{DD\_HV\_ADR\_S} <= 5.5$ V	—	30	
			Power Down mode $V_{DD\_HV\_ADR\_S} <= 5.5$ V	—	1	

Table 27. SARn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
I_{ADV_S}[4]	CC	$V_{DD\_HV\_ADV\_S}$ power supply current (each ADC)	Run mode $t_{conv} \geq 5$ µs	—	4.0	mA
			Run mode $t_{conv} = 2.5$ µs	—	4.0	
			Power Down mode	—	1.0	
TUE_{12}	CC	Total unadjusted error in 12-bit configuration[6]	$T_J < 150$ °C, $V_{DD\_HV\_ADV\_S} > 4$ V, $V_{DD\_HV\_ADR\_S} > 4$ V	–4	4	LSB (12b)
			$T_J < 150$ °C, $V_{DD\_HV\_ADV\_S} > 4$ V, 4 V > $V_{DD\_HV\_ADR\_S} > 2$ V	–6	6	
			$T_J < 150$ °C, 4 V > $V_{DD\_HV\_ADV\_S} > 3.5$ V	–12	12	

Table 27. SARn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
ΔTUE_{12}	CC	TUE degradation due to $V_{DD\_HV\_ADR\_S}$ offset with respect to $V_{DD\_HV\_ADV\_S}$	$V_{IN} < V_{DD\_HV\_ADV\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in [0:25 mV]$	0	0	LSB (12b)
			$V_{IN} < V_{DD\_HV\_ADV\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in [25:50 mV]$	–2	2	
			$V_{IN} < V_{DD\_HV\_ADV\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in [50:75 mV]$	–4	4	
			$V_{IN} < V_{DD\_HV\_ADV\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in [75:100 mV]$	–6	6	
			$V_{DD\_HV\_ADV\_S} < V_{IN} < V_{DD\_HV\_ADR\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in [0:25 mV]$	–2.5	2.5	
			$V_{DD\_HV\_ADV\_S} < V_{IN} < V_{DD\_HV\_ADR\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in [25:50 mV]$	–4	4	
			$V_{DD\_HV\_ADV\_S} < V_{IN} < V_{DD\_HV\_ADR\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in [50:75 mV]$	–7	7	
			$V_{DD\_HV\_ADV\_S} < V_{IN} < V_{DD\_HV\_ADR\_S}$ $V_{DD\_HV\_ADR\_S} - V_{DD\_HV\_ADV\_S} \in [75:100 mV]$	–12	12	
DNL	CC	Differential non-linearity	$V_{DD\_HV\_ADV\_S} > 4 V$ $V_{DD\_HV\_ADR\_S} > 4 V$	–1	2	LSB (12b)
INL	CC	Integral non-linearity	$4.0 V < V_{DD\_HV\_ADV\_S} < 5.5 V$ $4.0 V < V_{DD\_HV\_ADR\_S} < 5.5 V$	–3	3	LSB (12b)
			$V_{DD\_HV\_ADV\_S} = 2V$ $V_{DD\_HV\_ADR\_S} = 2 V$	–5	5	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Please refer to Figure 14 and Figure 15 for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.

3 $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.

4 Current parameter values are for a single ADC.

5 Extra bias current is present only when BIAS is selected.

6 This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to ± 6 LSB.

3.10.3 S/D ADC electrical specification

The SDn ADCs are Sigma Delta 16-bit analog-to-digital converters with 333 Ksps maximum output rate.

Table 28. SDn ADC electrical specification[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
V_{IN}	SR	ADC input signal	—	0	—	$V_{DD\_HV\_ADV\_D}$	V
V_{IN_PK2PK}[2]	SR	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[3] – V_{INM}[4]	Single ended $V_{INM} = V_{SS\_HV\_ADR\_D}$	$V_{DD\_HV\_ADR\_D}$/GAIN			V
			Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR\_D}$ GAIN = 1	$\pm 0.5*V_{DD\_HV\_ADR\_D}$			
			Single ended $V_{INM} = 0.5*V_{DD\_HV\_ADR\_D}$ GAIN = 2,4,8,16	$\pm V_{DD\_HV\_ADR\_D}$/GAIN			
			Differential, $0 < V_{IN} < V_{DD\_HV\_IO\_MAIN}$	$\pm V_{DD\_HV\_ADR\_D}$/GAIN			
f_{ADCD_M}	SR	S/D modulator Input Clock	—	4	14.4	16	MHz
f_{ADCD_S}	SR	Output conversion rate	—	—	—	333	ksps
—	CC	Oversampling ratio	Internal modulator	24	—	256	—
			External modulator	—	—	256	—
RESOLUTION	CC	S/D register resolution[5]	2's complement notation	16			bit
GAIN	SR	ADC gain	Defined via ADC_SD[PGA] register. Only integer powers of 2 are valid gain values.	1	—	16	—
$\|\delta_{GAIN}\|$	CC	Absolute value of the ADC gain error[6,7]	Before calibration (applies to gain setting = 1)	—	—	1.5	%
			After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 5\%$ $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
			After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 5\%$ $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
			After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 5\%$ $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
V_{OFFSET}	CC	Input Referred Offset Error[6,7,8]	Before calibration (applies to all gain settings – 1, 2, 4, 8, 16)	—	10* (1+1/gain)	20	mV
			After calibration, $\Delta V_{DD\_HV\_ADR\_D} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
			After calibration, $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 100$ °C			7.5	
			After calibration, $\Delta V_{DD\_HV\_ADV\_D} < 10\%$ $\Delta T_J < 150$ °C	0.5		10	
$SNR_{DIFF150}$	CC	Signal to noise ratio in differential mode 150 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 1 $T_J < 150$ °C	80	—	—	dBFS
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 2 $T_J < 150$ °C	77	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 4 $T_J < 150$ °C	74	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 8 $T_J < 150$ °C	71	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 16 $T_J < 150$ °C	68	—	—	

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$SNR_{DIFF333}$	CC	Signal to noise ratio in differential mode 333 ksps output rate	$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 1 $T_J < 150$ °C	74	—	—	dBFS
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 2 $T_J < 150$ °C	71	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 4 $T_J < 150$ °C	68	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 8 $T_J < 150$ °C	65	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 16 $T_J < 150$ °C	62	—	—	
SNR_{SE150}	CC	Signal to noise ratio in single ended mode 150 ksps output rate[11]	$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 1 $T_J < 150$ °C	74	—	—	dBFS
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 2 $T_J < 150$ °C	71	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 4 $T_J < 150$ °C	68	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 8 $T_J < 150$ °C	65	—	—	
			$4.5 < V_{DD\_HV\_ADV\_D} < 5.5$[9,10,17] $V_{DD\_HV\_ADR\_D} = V_{DD\_HV\_ADV\_D}$ GAIN = 16 $T_J < 150$ °C	62	—	—	
SFDR	CC	Spurious free dynamic range	GAIN = 1	60	—	—	dBc
			GAIN = 2	60	—	—	
			GAIN = 4	60	—	—	
			GAIN = 8	60	—	—	
			GAIN = 16	60	—	—	

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Z_{DIFF}	D	Differential Input impedance[12][13]	GAIN=1	1000	1250	1500	kΩ
			GAIN=2	600	800	1000	
			GAIN=4	300	400	500	
			GAIN=8	200	250	300	
			GAIN=16	200	250	300	
Z_{CM}	D	Common Mode Input impedance[14] [15]	GAIN=1	1400	1800	2200	kΩ
			GAIN=2	1000	1300	1600	
			GAIN=4	700	950	1150	
			GAIN=8	500	650	800	
			GAIN=16	500	650	800	
R_{BIAS}	D	Bare Bias resistance	—	110	144	180	kΩ
ΔV_{INTCM}	D	common mode input reference voltage[16]	—	-12	—	+12	%
V_{BIAS}	CC	Bias voltage	—	—	$V_{DD\_HV\_ADR\_D}/2$	—	V
δV_{BIAS}	CC	Bias voltage accuracy	—	–2.5	—	+2.5	%
V_{cmrr}	SR	Common mode rejection ratio	—	54	—	—	dB
R_{Caaf}	SR	Anti-aliasing filter	External series resistance	—	—	20	kΩ
	CC		Filter capacitances	180	—	—	pF
$f_{PASSBAND}$	CC	Pass band[17]	—	0.01	—	0.333 * f_{ADCD_S}	kHz
δ_{RIPPLE}	CC	Pass band ripple[18]	0.333 * f_{ADCD_S}	–1	—	1	%
$F_{rolloff}$	CC	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
			[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
			[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
			[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
			[2.5 * f_{ADCD_S}, f_{ADCD_M}/2]	60	—	—	

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
δ_{GROUP}	CC	Group delay	Within pass band – Tclk is f_{ADCD_M} / 2	—	—	—	—
			OSR = 24	—	—	238.5	Tclk
			OSR = 28	—	—	278	
			OSR = 32	—	—	317.5	
			OSR = 36	—	—	357	
			OSR = 40	—	—	396.5	
			OSR = 44	—	—	436	
			OSR = 48	—	—	475.5	
			OSR = 56	—	—	554.5	
			OSR = 64	—	—	633.5	
			OSR = 72	—	—	712.5	
			OSR = 75	—	—	699	
			OSR = 80	—	—	791.5	
			OSR = 88	—	—	870.5	
			OSR = 96	—	—	949.5	
			OSR = 112	—	—	1107.5	
			OSR = 128	—	—	1265.5	
			OSR = 144	—	—	1423.5	
			OSR = 160	—	—	1581.5	
			OSR = 176	—	—	1739.5	
			OSR = 192	—	—	1897.5	
			OSR = 224	—	—	2213.5	
			OSR = 256	—	—	2529.5	
			Distortion within pass band	–0.5/ f_{ADCD_S}	—	+0.5/ f_{ADCD_S}	—
f_{HIGH}	CC	High pass filter 3dB frequency	Enabled	—	10e-5* f_{ADCD_S}	—	—
$t_{STARTUP}$	CC	Start-up time from power down state	—	—	—	100	µs
$t_{LATENCY}$	CC	Latency between input data and converted data when input mux does not change[19]	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
			HPF = OFF	—	—	δ_{GROUP}	—

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$t_{SETTLING}$	CC	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP}$ + $3*f_{ADCD\_S}$	—
			HPF = OFF	—	—	$2*\delta_{GROUP}$ + $2*f_{ADCD\_S}$	—
$t_{ODRECOVERY}$	CC	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP}$ + f_{ADCD_S}	—
			HPF = OFF	—	—	$2*\delta_{GROUP}$	—
C_{S_D}	CC	S/D ADC sampling capacitance after sampling switch[20]	GAIN = 1, 2, 4, 8	—	—	75*GAIN	fF
			GAIN = 16	—	—	600	fF
I_{BIAS}	CC	Bias consumption	At least 1 ADCD enabled			3.5	mA
I_{ADV_D}	CC	$V_{DD\_HV\_ADV\_D}$ power supply current (each ADC)	ADCD enabled	—	—	3.5	mA
ΣI_{ADR_D}	CC	Sum of all ADC reference consumption	ADCD enabled, f_{ADCD_M} = 14.4 MHz	—	—	30	µA
$SINAD_{DIFF150}$	CC	Signal to Noise and Distortion Ratio, Differential Mode, 150 Ksps output rate	Gain = 1 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	72	—	—	dBFS
			Gain = 2 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	72	—	—	
			Gain = 4 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	69	—	—	
			Gain = 8 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	68.8	—	—	
			Gain = 16 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	64.8	—	—	

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$SINAD_{DIFF333}$	CC	Signal to Noise and Distortion Ratio, Single-ended Mode, 150Ksps output rate	Gain = 1 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	66	—	—	dBFS
			Gain = 2 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	66	—	—	
			Gain = 4 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	63	—	—	
			Gain = 8 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	62	—	—	
			Gain = 16 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	59	—	—	
$SINAD_{SE150}$	CC	Signal to Noise and Distortion Ratio, Single-ended Mode, 150Ksps output rate	Gain = 1 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	66	—	—	dBFS
			Gain = 2 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	66	—	—	
			Gain = 4 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	63	—	—	
			Gain = 8 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	62	—	—	
			Gain = 16 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	59	—	—	

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$THD_{DIFF150}$	CC	Total Harmonic Distortion, Differential Mode, 150Ksps output rate	Gain = 1 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	65	—	—	dBFS
			Gain = 2 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	68	—	—	
			Gain = 4 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	74	—	—	
			Gain = 8 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	80	—	—	
			Gain = 16 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	80	—	—	
$THD_{DIFF333}$	CC	Total Harmonic Distortion, Differential Mode, 333Ksps output rate	Gain = 1 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	65	—	—	dBFS
			Gain = 2 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	68	—	—	
			Gain = 4 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	74	—	—	
			Gain = 8 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	80	—	—	
			Gain = 16 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	80	—	—	

Table 28. SDn ADC electrical specification[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
THD_{SE150}	CC	Total Harmonic Distortion, Single-ended Mode, 150Ksps output rate	Gain = 1 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	68	—	—	dBFS
			Gain = 2 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	68	—	—	
			Gain = 4 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	68	—	—	
			Gain = 8 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	68	—	—	
			Gain = 16 4.5 V < $V_{DD\_HV\_ADV\_D}$ < 5.5 V $V_{DD\_HV\_ADR\_D}$ = $V_{DD\_HV\_ADV\_D}$ Tj < 150 °C	68	—	—	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 For input voltage above the maximum and below the clamp voltage of the input pad, there is no latch-up concern, and the signal will only be ‘clipped’.

3 V_{INP} is the input voltage applied to the positive terminal of the SDADC.

4 V_{INM} is the input voltage applied to the negative terminal of the SDADC.

5 When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. The gives an effective resolution of 15 bits.

6 Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the device.

7 Calibration of gain is possible when gain = 1.
Offset Calibration should be done with respect to 0.5*$V_{DD\_HV\_ADR\_D}$ for *differential mode* and *single ended mode with negative input=0.5*$V_{DD\_HV\_ADR\_D}$*.
Offset Calibration should be done with respect to 0 for "single ended mode with negative input=0".
Both offset and Gain Calibration is guaranteed for ±5% variation of $V_{DD\_HV\_ADR\_D}$, ±10% variation of $V_{DD\_HV\_ADV\_D}$, and ± 50 °C temperature variation.

8 Conversion offset error must be divided by the applied gain factor (1, 2, 4, 8, or 16) to obtain the actual input referred offset error.

9 S/D ADC is functional in the range 3.6 V – 4.5 V, SNR parameter degrades by 3 dB. Degraded SNR value based on simulation.

10 S/D ADC is functional in the range 3.0 V –4.5 V, SNR parameter degrades by 9 dB. Degraded SNR value based on simulation.

11 This parameter is guaranteed by bench validation with a small sample of typical devices, and tested in production to a value of 6 dB less.

12 Input impedance in differential mode Z_{IN}(input impedance) = Z_{DIFF}.

13 Impedance given at F_{ADCD_M}= 16 MHz. Impedance is inversely proportional to SDADC clock frequency. $Z_{DIFF}(F_{ADCD\_M})$ = (16 MHz / F_{ADCD_M}) * Z_{DIFF}, Z_{CM} (F_{ADCD_M}) = (16MHz / F_{ADCD_M}) * Z_{CM}.

14 Input impedance in single-ended mode Z_{IN} = (2 * Z_{DIFF} * Z_{CM}) / (Z_{DIFF} + Z_{CM}).

15 Impedance given at F_{ADCD_M}= 16 MHz. Impedance is inversely proportional to SDADC clock frequency. $Z_{DIFF}(F_{ADCD\_M})$ = (16 MHz / F_{ADCD_M}) * Z_{DIFF}, Z_{CM} (F_{ADCD_M}) = (16MHz / F_{ADCD_M}) * Z_{CM}.

16 Vintcm is the common mode input reference voltage for the SDADC, and has a nominal value of ($V_{DD\_HV\_ADC}$ - $V_{SS\_HV\_ADC}$) / 2.

17 SNR values guaranteed only if external noise on the ADC input pin is attenuated by the required SNR value in the frequency range of f_{ADCD_M} – f_{ADCD_S} to f_{ADCD_M} + f_{ADCD_S}, where f_{ADCD_M} is the input sampling frequency, and f_{ADCD_S} is the output sample frequency. A proper external input filter should be used to remove any interfering signals in this frequency range.

18 The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB.

19 Propagation of the information from the pin to the register CDR[CDATA] and flags SFR[DFEF], SFR[DFFF] is given by the different modules that need to be crossed: delta/sigma filters, high pass filter, fifo module, clock domain synchronizers. The time elapsed between data availability at pin and internal S/D module registers is given by the below formula:

REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)fPBRIDGEx_CLK

where fADCD_S is the frequency of the sampling clock, fADCD_M is the frequency of the modulator, and fPBRIDGEx_CLK is the frequency of the peripheral bridge clock feeds to the ADC S/D module. The (~+1) symbol refers to the number of clock cycles uncertainty (from 0 to 1 clock cycle) to be added due to resynchronization of the signal during clock domain crossing.
Some further latency may be added by the target module (core, DMA, interrupt) controller to process the data received from the ADC S/D module.

20 This capacitance does not include pin capacitance, that can be considered together with external capacitance, before sampling switch.

3.11 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 29. Temperature sensor electrical characteristics

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
—	CC	Temperature monitoring range	—	–40	—	150	°C
T_{SENS}	CC	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	Accuracy	T_J < 150 °C	–3	—	3	°C
I_{TEMP_SENS}	CC	$V_{DD\_HV\_ADV\_S}$ power supply current	—	—	—	700	µA

3.12 LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics

The LFAST pad electrical characteristics apply to both the SIPI and high-speed debug serial interfaces on the device. The same LVDS pad is used for the Microsecond Channel (MSC) and DSPI LVDS interfaces, with different characteristics given in the following tables.

3.12.1 LFAST interface timing diagrams

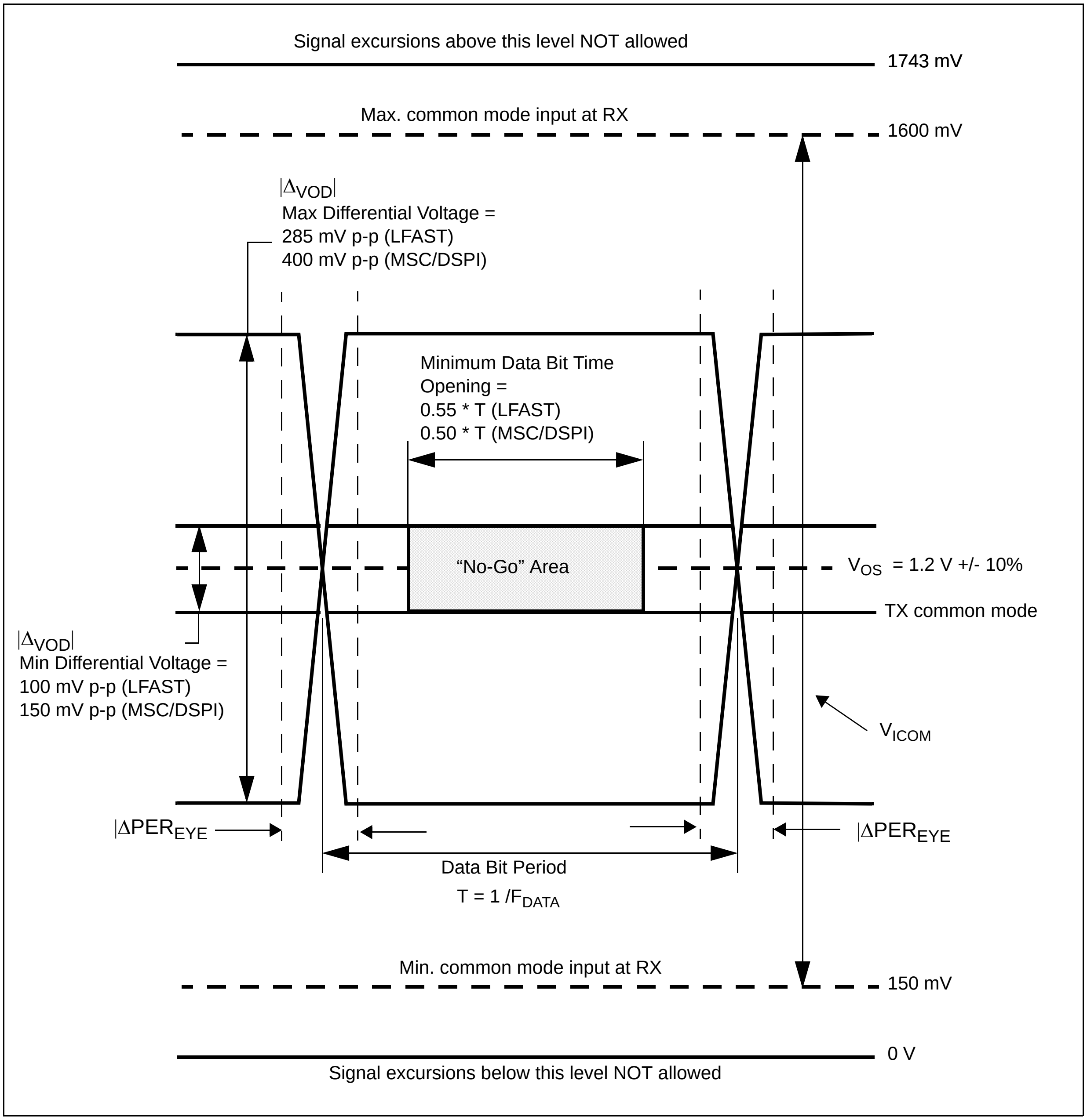


Figure 16. LFAST and MSC/DSPI LVDS timing definition

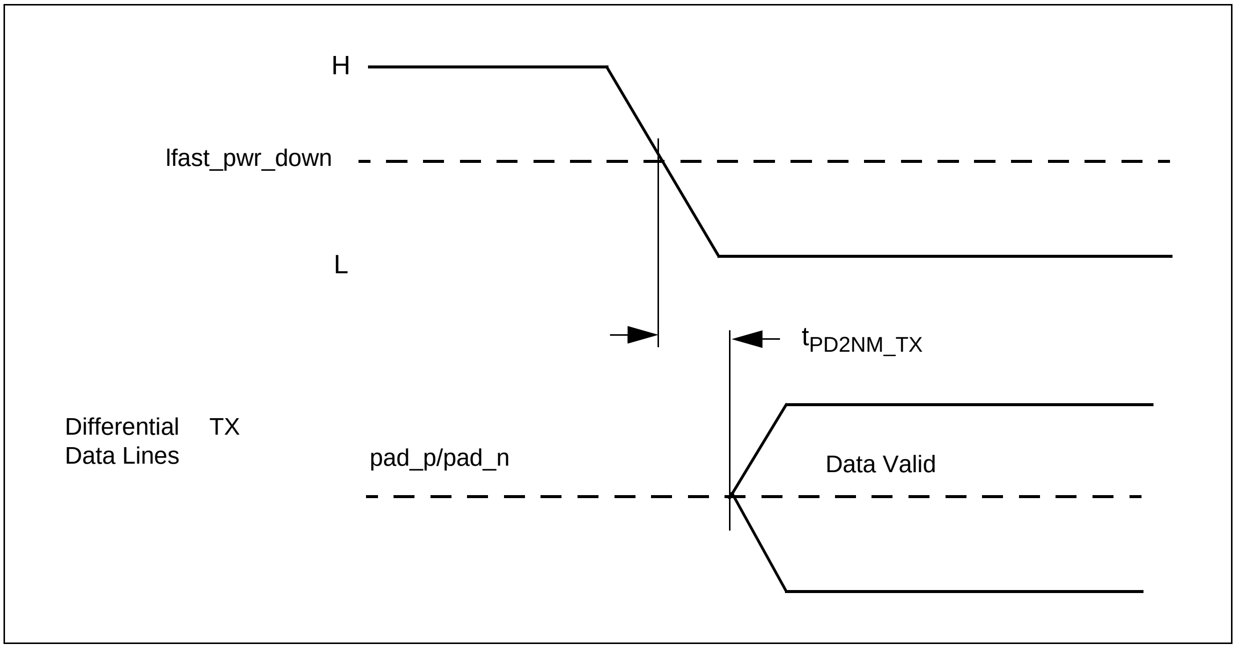


Figure 17. Power-down exit time

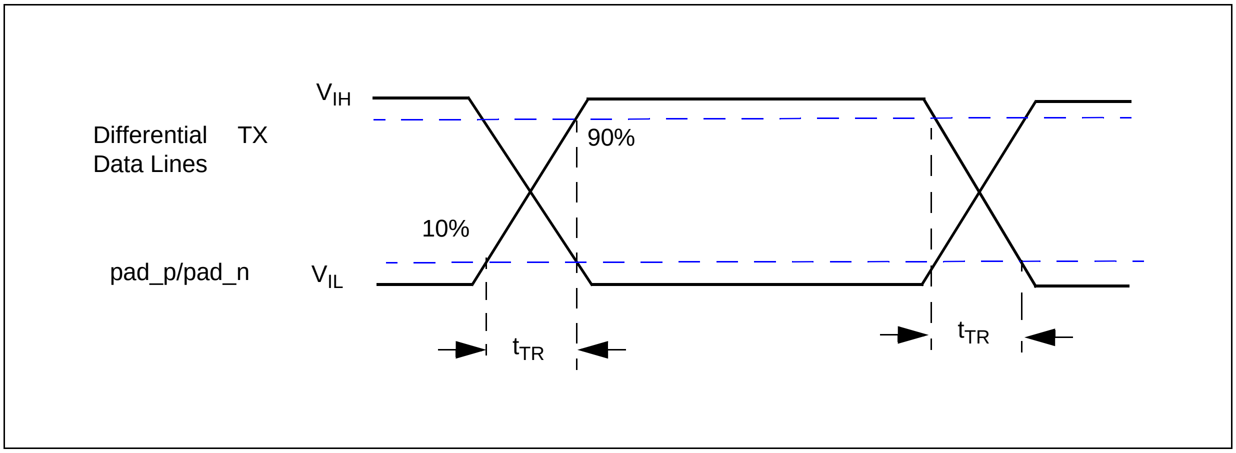


Figure 18. Rise/fall time

3.12.2 LFAST and MSC/DSPI LVDS interface electrical characteristics

The following table contains the electrical characteristics for the LFAST interface.

Table 30. LVDS pad startup and receiver electrical characteristics[1,2]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
STARTUP[3,4]							
t_{STRT_BIAS}	CC	Bias current reference startup time[5]	—	—	0.5	4	µs
t_{PD2NM_TX}	CC	Transmitter startup time (power down to normal mode)[6]	—	—	0.4	2.75	µs

Table 30. LVDS pad startup and receiver electrical characteristics[1,2] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
t_{SM2NM_TX}	CC	Transmitter startup time (sleep mode to normal mode)[7]	Not applicable to the MSC/DSPI LVDS pad	—	0.2	0.5	µs
t_{PD2NM_RX}	CC	Receiver startup time (power down to normal mode)[8]	—	—	20	40	ns
t_{PD2SM_RX}	CC	Receiver startup time (power down to sleep mode)[9]	Not applicable to the MSC/DSPI LVDS pad	—	20	50	ns
I_{LVDS_BIAS}	CC	LVDS bias current consumption	Tx or Rx enabled	—	—	0.95	mA
TRANSMISSION LINE CHARACTERISTICS (PCB Track)							
Z_0	SR	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	SR	Transmission line differential impedance	—	95	100	105	Ω
RECEIVER							
V_{ICOM}	SR	Common mode voltage	—	0.15[10]	—	1.6[11]	V
$\|\Delta_{VI}\|$	SR	Differential input voltage[12]	—	100	—	—	mV
V_{HYS}	CC	Input hysteresis	—	25	—	—	mV
R_{IN}	CC	Terminating resistance	3.0 V–5.5 V	80	125	150	Ω
C_{IN}	CC	Differential input capacitance[13]	—	—	3.5	6.0	pF
I_{LVDS_RX}	CC	Receiver DC current consumption	Enabled	—	—	0.5	mA

1 The LVDS pad startup and receiver electrical characteristics in this table apply to both the LFAST & High-speed Debug (HSD) LVDS pad, and the MSC/DSPI LVDS pad except where noted in the conditions.

2 All LVDS pad electrical characteristics are valid from –40 °C to 150 °C.

3 All startup times are defined after a 2 peripheral bridge clock delay from writing to the corresponding enable bit in the LVDS control registers (LCR) of the LFAST and High-Speed Debug modules. The value of the LCR bits for the LFAST/HSD modules don't take effect until the corresponding SIUL2 MSCR ODC bits are set to LFAST LVDS mode. Startup times for MSC/DSPI LVDS are defined after 2 peripheral bridge clock delay after selecting MSC/DSPI LVDS in the corresponding SIUL2 MSCR ODC field.

4 Startup times are valid for the maximum external loads CL defined in both the LFAST/HSD and MSC/DSPI transmitter electrical characteristic tables.

5 Bias startup time is defined as the time taken by the current reference block to reach the settling bias current after being enabled.

6 Total transmitter startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_TX} + 2 peripheral bridge clock periods.

7 Total transmitter startup time from sleep mode to normal mode is t_{SM2NM_TX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.

8 Total receiver startup time from power down to normal mode is t_{STRT_BIAS} + t_{PD2NM_RX} + 2 peripheral bridge clock periods.

9 Total receiver startup time from power down to sleep mode is t_{PD2SM_RX} + 2 peripheral bridge clock periods. Bias block remains enabled in sleep mode.

10 Absolute min = 0.15 V – (285 mV/2) = 0 V

11 Absolute max = 1.6 V + (285 mV/2) = 1.743 V

[12] The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing.

[13] Total internal capacitance including receiver and termination, co-bonded GPIO pads, and package contributions.

Table 31. LFAST transmitter electrical characteristics[1,2]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{DATA}	SR	Data rate	—	—	—	312/320[3]	Mbps
V_{OS}	CC	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	CC	Differential output voltage swing (terminated)[4,5]	—	110	171	285	mV
t_{TR}	CC	Rise/Fall time (absolute value of the differential output voltage swing)[4,5]	—	0.26	—	1.5	ns
C_L	SR	External lumped differential load capacitance[3]	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	10.0	pF
			$V_{DD\_HV\_IO}$ = 3.0 V	—	—	8.5	
I_{LVDS_TX}	CC	Transmitter DC current consumption	Enabled	—	—	3.2	mA

[1] The LFAST and High-Speed Debug LFAST pad electrical characteristics are based on worst case internal capacitance values shown in Figure 19.

[2] All LFAST and High-Speed Debug LVDS pad electrical characteristics are valid from –40 °C to 150 °C.

[3] The 312 Mbps data rate is achieved with a 26 MHz reference clock, and 320 Mbps is achieved with a 10 or 20 MHz reference clock.

[4] Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 19.

[5] Valid for maximum external load C_L.

Table 32. MSC/DSPI LVDS transmitter electrical characteristics [1,2]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Data Rate							
f_{DATA}	SR	Data rate	—	—	—	80	Mbps
V_{OS}	CC	Common mode voltage	—	1.08	—	1.32	V
$\|V_{OD}\|$	CC	Differential output voltage swing (terminated)[3,4]	—	150	214	400	mV
t_{TR}	CC	Rise/Fall time (absolute value of the differential output voltage swing)[3,4]	—	0.8	—	4.0	ns
C_L	SR	External lumped differential load capacitance[3]	$V_{DD\_HV\_IO}$ = 4.5 V	—	—	50	pF
			$V_{DD\_HV\_IO}$ = 3.0 V	—	—	39	
I_{LVDS_TX}	CC	Transmitter DC current consumption	Enabled	—	—	4.0	mA

[1] The MSC and DSPI LVDS pad electrical characteristics are based on the application circuit and typical worst case internal capacitance values given in Figure 19.

[2] All MSC and DSPI LVDS pad electrical characteristics are valid from –40 °C to 150 °C.

3 Valid for maximum data rate f_{DATA}. Value given is the capacitance on each terminal of the differential pair, as shown in Figure 19.

4 Valid for maximum external load C_L.

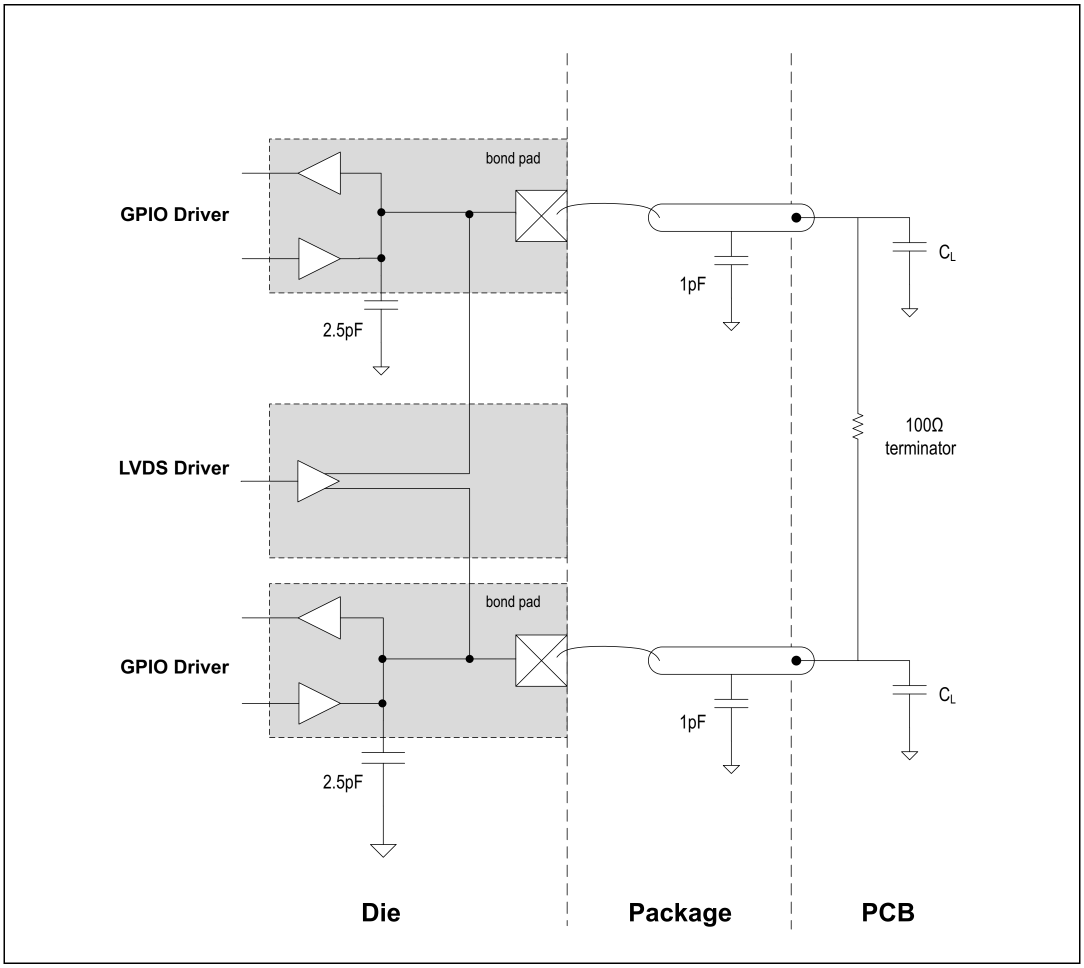


Figure 19. LVDS pad external load diagram

3.12.3 LFAST PLL electrical characteristics

The following table contains the electrical characteristics for the LFAST PLL.

Table 33. LFAST PLL electrical characteristics[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Nominal	Max	
f_{RF_REF}	SR	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	CC	PLL input reference clock frequency error	—	–1	—	1	%
DC_{REF}	CC	PLL input reference clock duty cycle	—	45	—	55	%
PN	CC	Integrated phase noise (single side band)	f_{RF_REF} = 20 MHz	—	—	–58	dBc
			f_{RF_REF} = 10 MHz	—	—	–64	

Table 33. LFAST PLL electrical characteristics[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Nominal	Max	
f_{VCO}	CC	PLL VCO frequency	—	—	640[2]	—	MHz
t_{LOCK}	CC	PLL phase lock[3]	—	—	—	40	µs
ΔPER_{REF}	SR	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 10 MHz	—	—	300	ps
			Long term, f_{RF_REF} = 10 MHz	–500	—	500	ps
ΔPER_{EYE}	CC	Output Eye Jitter (peak to peak)[4]	—	—	—	400	ps

1 The specifications in this table apply to both the interprocessor bus and debug LFAST interfaces.

2 The 640 MHz frequency is achieved with a 10 MHz or 20 MHz reference clock. With a 26 MHz reference, the VCO frequency is 624 MHz.

3 The time from the PLL enable bit register write to the start of phase locks is maximum 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device.

4 Measured at the transmitter output across a 100 Ohm termination resistor on a device evaluation board. See Figure 19.

3.13 Aurora LVDS electrical characteristics

The following table describes the Aurora LVDS electrical characteristics.

NOTE

The Aurora interface is AC coupled, so there is no common-mode voltage specification.

Table 34. Aurora LVDS electrical characteristics[1,2]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Transmitter							
F_{TX}	CC	Transmit Data Rate	—	—	—	1.25	Gbps
$\lvert\Delta V_{OD\_LVDS}\rvert$	CC	Differential output voltage swing (terminated)[3]	—	±400	±600	±800	mV
t_{TR_LVDS}	CC	Rise/Fall time (10%–90% of swing)	—	60	—	—	ps
$R_{V\_L\_Tx}$	SR	Differential Terminating resistance	—	81	100	120	Ω
T_{Loss}	CC	Transmission Line Loss due to loading effects	—	—	—	6[4]	dB
Transmission line characteristics (PCB track)							
L_{LINE}	SR	Transmission line length	—	—	—	20	cm
Z_{LINE}	SR	Transmission line characteristic impedance	—	45	50	55	Ω
C_{ac_clk}	SR	Clock Receive Pin External AC Coupling Capacitance	Values are nominal, valid for +/– 50% tolerance	100	—	270	pF

Table 34. Aurora LVDS electrical characteristics[1,2] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
C_{ac_tx}	SR	Transmit Lane External AC Coupling Capacitance	Values are nominal, valid for +/– 50% tolerance	250	—	2000	pF
Receiver							
F_{RX}	CC	Receive Clock Rate	T_J = 150 °C	—	—	1.25	Gbps
$\|\Delta V_{I\_L}\|$	SR	Differential input voltage (peak to peak)	—	200	—	1000	mV
$R_{V\_L\_Rx}$	CC	Differential Terminating resistance	—	81	100	120	Ω

1 All Aurora electrical characteristics are valid from –40 °C to 150 °C, except where noted.

2 All specifications valid for maximum transmit data rate F_{TX}.

3 The minimum value of 400 mV is only valid for differential terminating resistance (R_{V_L}) = 99 ohm to 101 ohm. The differential output voltage swing tracks with the value of R_{V_L}.

4 Transmission line loss maximum value is specified for the maximum drive level of the Aurora transmit pad.

3.14 Power management: PMC, POR/LVD, sequencing

3.14.1 Power management electrical characteristics

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the $V_{DD\_HV\_PMC}$ supply (see Table 8).

3.14.2 Power management integration

In order to ensure correct functionality of the device, it is recommended to follow below integration scheme.

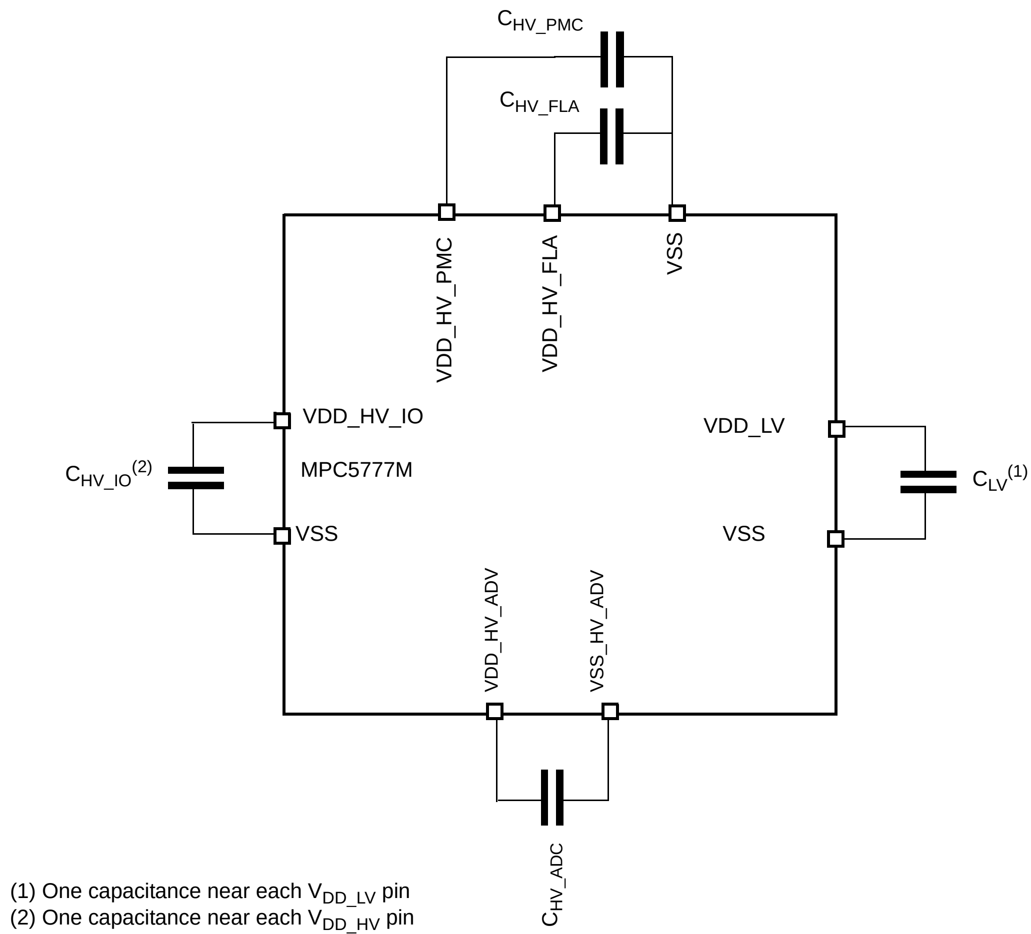


Figure 20. Recommended supply pin circuits

The following table describes the supply stability capacitances required on the device for proper operation.

Table 35. Device power supply integration

Symbol		Parameter		Conditions	Value[1]			Unit
					Min	Typ	Max	
C_{LV}	SR	Minimum VDD_LV external capacitance[2]	Bulk capacitance	External regulator bandwidth > 20 KHz	10	—	—	µF
			Total bypass capacitance at external pin[3]		Note 3	—	—	
C_{HV_IO}	SR	Minimum VDD_HV_IO external capacitance		—	4.7	—	—	µF
C_{HV_FLA}	SR	Minimum VDD_HV_FLA external capacitance[4,5]		—	0.75	1.5	—	µF
C_{HV_PMC}	SR	Minimum $V_{DD\_HV\_PMC}$ External Capacitance[6,7]		512 BGA balls A29, B28, F24, and G23	2.2	4.7	—	µF
C_{HV_ADC}	SR	Minimum $V_{DD\_HV\_ADV}$ external capacitance[8]			1.5	3.3	—	µF

1 See Figure 20 for capacitor integration.

2 Recommended X7R or X5R ceramic low ESR capacitors, ±15% variation over voltage, temperature, and aging.

3 Each VDD_LV pin requires both a 0.1µF and 0.01µF capacitor for high-frequency bypass and EMC requirements.

4 The recommended flash regulator composition capacitor is 1.5 µF typical X7R or X5R, with –50% and +35% as min and max. This puts the min cap at 0.75 µF.

5 Start-up time of the internal flash regulator from release of the LVD360 is worst case 500 us. This is based on the typical CHV_FLA bulk capacitance value.

6 For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_PMC}$ and V_{SS_HV}.

7 In the 512BGA package, $V_{DD\_HV\_PMC}$ is shorted to $V_{DD\_HV\_IO\_MAIN}$. Use a local 200 nF capacitor on 512BGA balls A29, B28, F24, G3, in addition to the normal $V_{DD\_HV\_IO\_MAIN}$ bulk and local external capacitance.

8 For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between $V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$.

3.14.3 3.3 V flash supply

Table 36. Flash power supply

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
$V_{DD\_HV\_FLA}$[1]	CC	Flash regulator DC output voltage	Before trimming	3.1[2]	3.3	3.5	V
			After trimming –40°C ≤ T_J ≤ 25°C	3.15	3.3	3.4	
			After trimming 25°C < T_J ≤ 150°C	3.10	3.3	3.4	

1 Min value accounts for all static and dynamic variations of the regulator (min cap as 0,75uF).

2 Min value of 3.1 V for VDD_HV_REG at 3.15V assumes that the auxiliary regulator on VDD_LV does not actively provide any current to the chip. If the auxiliary regulator actively provides current, the min value may go lower than 3.1 V drop to IR drop caused by auxiliary current demanding on VDD_HV_REG supply.

3.14.4 Device voltage monitoring

The LVD/HVDs and their associated levels for the device are given in the following table. The figure below illustrates the workings of voltage monitoring threshold.

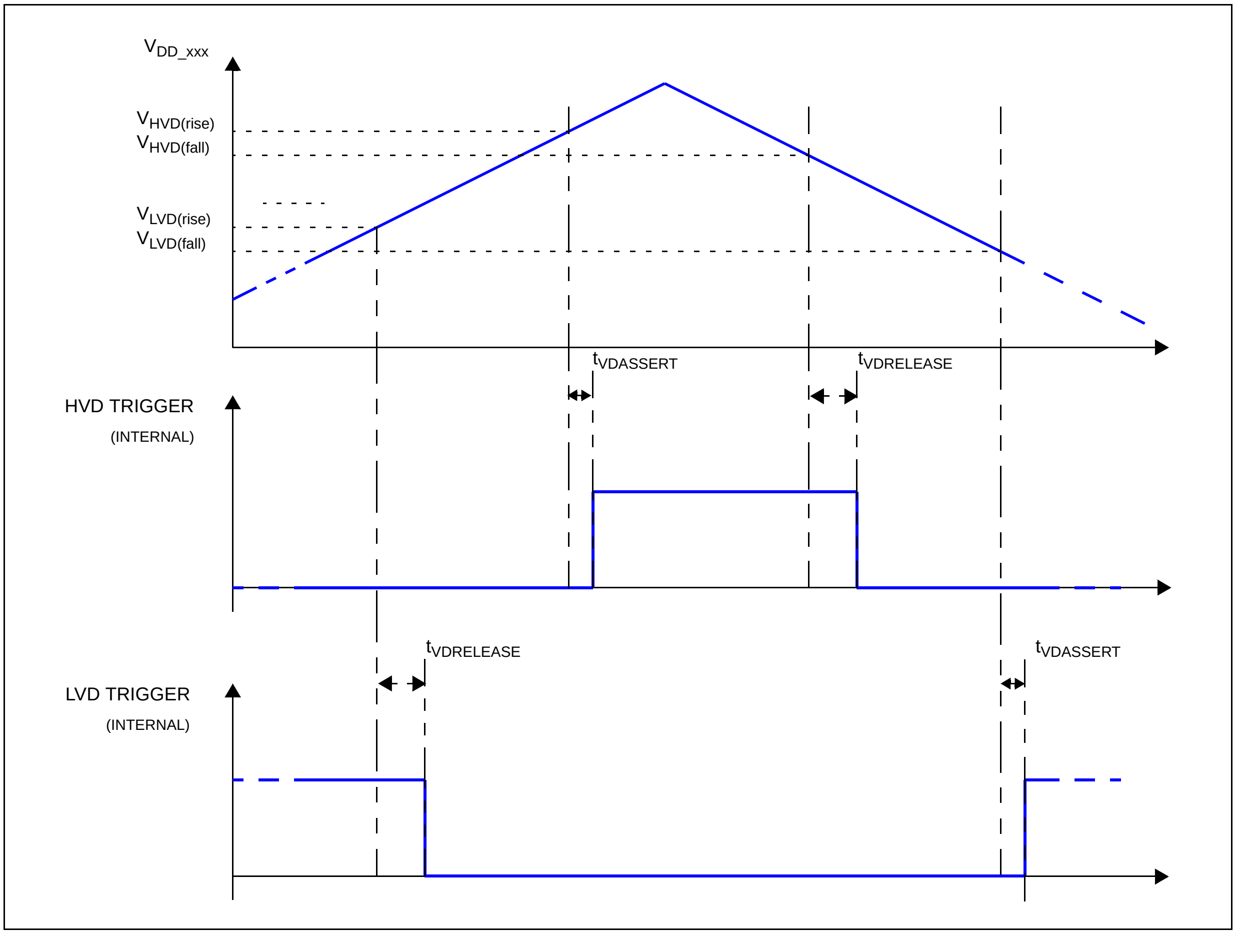


Figure 21. Voltage monitor threshold definition

Table 37. Voltage monitor electrical characteristics[1]

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
V_{PORUP_LV}[2]	CC	LV supply power on reset threshold	Rising voltage (power up)	1111	—	1235	mV
			Falling voltage (power down)[3]	1015	—	1125	
			Hysteresis on power-up	50	—	—	
V_{LVD096}	CC	LV internal[4] supply low voltage monitoring	See note [5]	1015	—	1145	mV
V_{LVD108}	CC	Core LV internal[4] supply low voltage monitoring	See note [6]	1150	—	1220	mV
V_{LVD112}	CC	LV external[7] supply low voltage monitoring	See note [5]	1175	—	1235	mV

Table 37. Voltage monitor electrical characteristics[1] (continued)

Symbol		Parameter	Conditions	Value			Unit
				Min	Typ	Max	
V_{HVD140}	CC	LV external[10] supply high voltage monitoring	See note [8]	1385	—	1475	mV
V_{HVD145}	CC	LV externa[10] supply high voltage reset threshold	—	1430	—	1510	mV
V_{PORUP_HV}[2]	CC	HV supply power on reset threshold[9]	Rising voltage (power up) on PMC/IO Main supply	4040	—	4480[10]	mV
			Rising voltage (power up) on IO JTAG and Osc supply	2730	—	3030	
			Rising voltage (power up) on ADC supply	2870	—	3182	
			Falling voltage (power down)[11]	2850	—	3162	
			Hysteresis on power up[12]	878	—	1630	
V_{POR240}	CC	HV supply power-on reset voltage monitoring	Rising voltage	2420	—	2780	mV
			Falling voltage	2400	—	2760	
V_{LVD270}	CC	HV supply low voltage monitoring	Rising voltage	2750	—	3000	mV
			Falling voltage	2700	—	2950	
V_{LVD295}	CC	Flash supply low voltage monitoring[13]	Rising voltage	—	—	3120	mV
			Falling voltage	2920	—	3100	
V_{HVD360}	CC	Flash supply high voltage monitoring	Rising voltage	3435	—	3650	mV
			Falling voltage	3415	—	—	
V_{LVD360}	CC	HV supply low voltage monitoring	Rising voltage	—	—	4000	mV
			Falling voltage	3600	—	3880	
V_{LVD400}	CC	HV supply low voltage monitoring	Rising voltage	4110	—	4410	mV
			Falling voltage	3970	—	4270	
V_{HVD600}	CC	HV supply high voltage monitoring	Rising voltage	5560	—	5960	mV
			Falling voltage	5500	—	5900	
$t_{VDASSERT}$	CC	Voltage detector threshold crossing assertion	—	0.1	—	2	µs
$t_{VDRELEASE}$	CC	Voltage detector threshold crossing de-assertion	—	5	—	20	µs

1 For V_{DD_LV} levels, a maximum of 30 mV IR drop is incurred from the pin to all sinks on the die. For other LVD, the IR drop is estimated by multiplying the supply current by 0.5 Ω.

2 V_{PORUP_LV} and V_{PORUP_HV} threshold are untrimmed values before completion of the power-up sequence. All other LVD/HVD thresholds are provided after trimming.

3 Assume all of LVDs on LV supplies disabled.

4 LV internal supply levels are measured on device internal supply grid after internal voltage drop.

5 LVD is released after $t_{VDRELEASE}$ temporization when *upper* threshold is crossed, LVD is asserted $t_{VDASSERT}$ after detection when *lower* threshold is crossed.

6 This specification is driven by LVD108_C. There are additional LVDs on PLL and Flash VDD_LV supply nets which will assert at voltage below LVD108_C.

7 LV external supply levels are measured on the die side of the package bond wire after package voltage drop. This is monitoring external regulator supply voltage and board voltage drop. This does not guarantee device is working down to minimum threshold. For minimum supply, refer to operating condition table.

8 HVD is released after $t_{VDRELEASE}$ temporization when *lower* threshold is crossed, HVD is asserted $t_{VDASSERT}$ after detection when *upper* threshold is crossed. HVD140 does not cause reset.

9 This supply also needs to be below 5472 mV (untrimmed HVD600 min)

10 The PMC supply also needs to be below 5472 mV (untrimmed HVD600 mV).

11 Untrimmed LVD300_A will be asserted first on power down.

12 Hysteresis is implemented only between the VDD_HV_IO_MAIN High voltage Supplies and the ADC high voltage supply. When these two supplies are shorted together, the hysteresis is as is shown in Table 37. If the supplies are not shorted (VDD_IO_MAIN and ADC high voltage supply), then there will be no hysteresis on the high voltage supplies.

13 $V_{DD\_HV\_FLA}$ supply range is guaranteed by internal regulator.

3.14.5 Power up/down sequencing

Table 38 shows the constraints and relationships for the different power supplies

Table 38. Device supply relation during power-up/power-down sequence

		Supply 2[1]							
		V_{DD_LV}	$V_{DD\_HV\_PMC}$	$V_{DD\_HV\_IO}$	$V_{DD\_HV\_FLA}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$	ALTREFn[2]	V_{DDSTBY}
Supply 1[1]	V_{DD_LV}								
	$V_{DD\_HV\_PMU}$								
	$V_{DD\_HV\_IO}$								
	$V_{DD\_HV\_FLA}$		2 mA[3]						
	$V_{DD\_HV\_ADV}$								
	$V_{DD\_HV\_ADR}$					5 mA			
	ALTREFn			10 mA[4]		10 mA[4]			
	V_{DDSTBY}								

1 Red cells: supply1 (row) can exceed supply2 (column), granted that external circuitry ensure current flowing from supply1 is less than absolute maximum rating current value provided.

2 ALTREFn are the alternate references for the ADC that can be used in place of the default reference ($V_{DD\_HV\_ADR\_*}$). They are SARB.ALTREF and SAR2.ALTREF.

3 $V_{DD\_HV\_FLA}$ is generated internally in normal mode. Above current constraints is guaranteed.

4 ADC performances is not guaranteed with ALTREFn above $V_{DD\_HV\_IO}$ / $V_{DD\_HV\_ADV}$

During power-up, all functional terminals are maintained into a known state as described within the following table.

Table 39. Functional terminals state during power-up and reset

TERMINAL TYPE[1]	POWERUP[2] pad state	RESET pad state	DEFAULT pad state[3]	Comments
PORST	Strong pull-down[4]	Weak pull-down	Weak pull-down	Power-on reset pad
ESR0[5]	Strong pull-down	Strong pull-down	Weak pull-up	Functional reset pad.
ESR1	High impedance	Weak pull-up	Weak pull-up	—
TESTMODE	Weak pull-down	Weak pull-down[6]	Weak pull-down[6]	—
GPIO	Weak pull-up[4]	Weak pull-up	Weak pull-up	—
ANALOG	High impedance	High impedance	High impedance	—
ERROR0	High impedance	High impedance	High impedance	During functional reset, pad state can be overridden by FCCU
JCOMP	High impedance	Weak pull-down	Weak pull-down	—
TCK	High impedance	Weak pull-down	Weak pull-down	—
TMS	High impedance	Weak pull-up	Weak pull-up	—
TDI	High impedance	Weak pull-up	Weak pull-up	—
TDO	High impedance	Weak pull-up	High impedance	—

1 Refer to pinout information for terminal type

2 POWERUP state is guaranteed from $V_{DD\_HV\_IO}$>1.1 V and maintained until supply cross the power-on reset threshold: V_{PORUP_LV} for LV supply, V_{PORUP_HV} for high voltage supply.

3 Before software configuration

4 Pull-down and pull-up strength are provided as part of Table 13 in Section 3.6.1, I/O input DC characteristics. Pull-up/Pull-down are activated within 2 µs after internal reset has been asserted. Actual pad transition will depend on external capacitance.

5 Unlike ESR0, ESR1 is provided as normal GPIO and implements weak pull-up during power-up.

6 An internal pull-down is implemented on the TESTMODE pin to prevent the device from entering test mode if the package TESTMODE pin is not connected. It is recommended to connect the TESTMODE pin to $V_{SS\_HV\_IO}$ on the board for maximum robustness, but not required. The value of TESTMODE is latched at the negation of reset and has no affect afterward. The device will not exit functional reset with the TESTMODE pin asserted during power-up. The TESTMODE pin can be connected externally directly to ground without any other components.

3.15 Flash memory electrical characteristics

The following sections contain flash memory electrical specifications.

3.15.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 40 shows the estimated Program/Erase times.

Table 40. Flash memory program and erase specifications (pending characterization)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3,4]		Field Update			Units
			Initial Max	Initial Max Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C≤ T_a ≤ 30°C	-40°C≤ T_J ≤ 150°C	-40°C≤ T_J ≤ 150 °C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1.200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1 Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.

2 Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.

3 Conditions: ≤ 150 cycles, nominal voltage.

4 Plant Programming times provide guidance for timeout limits used in the factory.

5 Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.

6 Conditions: -40°C≤ T_J ≤ 150°C; full spec voltage.

3.15.2 Flash memory FERS program and erase specifications

Table 41. Flash memory FERS program and erase specifications (pending characterization)

Symbol	Characteristic[1]	Factory Programming with FERS=1 and Vfers pin is 5V ± 5%[2]			Units
		Typ[3]	Initial Max	Initial Max Full Temp	
			$20°C \leq T_A \leq 30°C$[4]	$-40°C \leq T_J \leq 150°C$[4]	
t_{dwpgm}	Doubleword (64 bits) program time	30	90	135	µs
t_{ppgm}	Page (256 bits) program time	43	145	218	µs
t_{qppgn}	Quad-page (1024 bits) program time	134	530	795	µs
t_{16kers}	16 KB erase time	160	782	782	ms
t_{16kpgn}	16 KB program time	18	24	35	ms
t_{32kers}	32 KB erase time	190	782	782	ms
t_{32kpgm}	32 KB program time	36	47	68	ms
t_{64kers}	64 KB erase time	250	782	782	ms
t_{64kpgm}	64 KB program time	72	94	135	ms
$t_{256kers}$	256 KB erase time	600	1,380	2,070	ms
$t_{256kpgm}$	256 KB program time	288	374	568	ms

1 Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.

2 Conditions: ≤150 cycles, nominal voltage.

3 Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.

4 Plant Programming times provide guidance for timeout limits used in the factory.

3.15.3 Flash memory Array Integrity and Margin Read specifications

Table 42. Flash memory Array Integrity and Margin Read specifications (characterized but not tested)

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 × Tperiod × Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 × Tperiod × Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 × Tperiod × Nread	—
$t_{ai256kseq}$	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 × Tperiod × Nread	—
$t_{aifullseq}$	Array Integrity time for sequential sequence full array.	—	—	3.77e5 × Tperiod × Nread	—
$t_{aifullprop}$	Array Integrity time for proprietary sequence (applies to full array or single block).	—	—	9.96e6 × Tperiod × Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256KB block.	893.01	—	1,339.5	µs
t_{mrfull}	Margin Read time for sequential sequence full array.	45.21	—	60.26	ms

1 Array Integrity times need to be calculated and are dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)

2 The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.15.4 Flash memory module life specifications

Table 43. Flash memory module life spec (pending characterization)

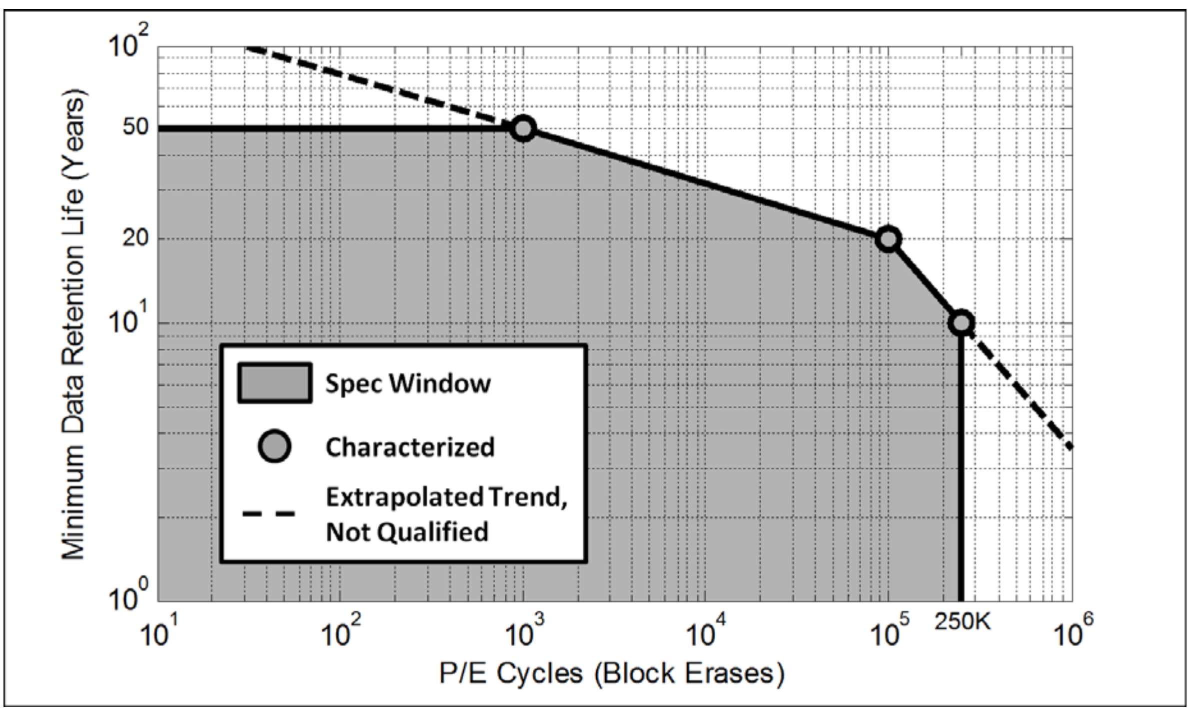
Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 – 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1 Program and erase supported across standard temperature specs.

2 Program and erase supported across standard temperature specs.

3.15.5 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



3.15.6 Flash memory AC timing specifications

Table 44. Flash memory AC timing specifications (characterized but not tested)

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	7 plus four system clock periods	9.1 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UTO-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UTO-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

3.15.7 Flash read wait state and address pipeline control settings

Table 45 describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the C55FMC array at 150 °C.

Table 45. Flash Read Wait State and Address Pipeline Control Combinations

Flash Frequency	RWSC setting	APC setting
0 MHz < fFLASH ≤ 33 MHz	0	0
33 MHz < fFLASH ≤ 100 MHz	2	1
100 MHz < fFLASH ≤ 133 MHz	3	1
133 MHz < fFLASH ≤ 167 MHz	4	1
167 MHz < fFLASH ≤ 200 MHz	5	2

3.16 AC specifications

All AC timing specifications are valid up to 150 °C, except where explicitly noted.

3.16.1 Debug and calibration interface timing

3.16.1.1 JTAG interface timing

Table 46. JTAG pin AC electrical characteristics[1,2]

#	Symbol		Characteristic	Value		Unit
				Min	Max	
1	t_{JCYC}	CC	TCK cycle time	100	—	ns
2	t_{JDC}	CC	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	TCK low to TDO data valid	—	16[3]	ns
7	t_{TDOI}	CC	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	TCK falling edge to output valid	—	600[4]	ns
12	t_{BSDVZ}	CC	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	TCK rising edge to boundary scan input invalid	15	—	ns

1 These specifications apply to JTAG boundary scan only. See Table 47 for functional specifications.

2 JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.

3 Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

4 Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

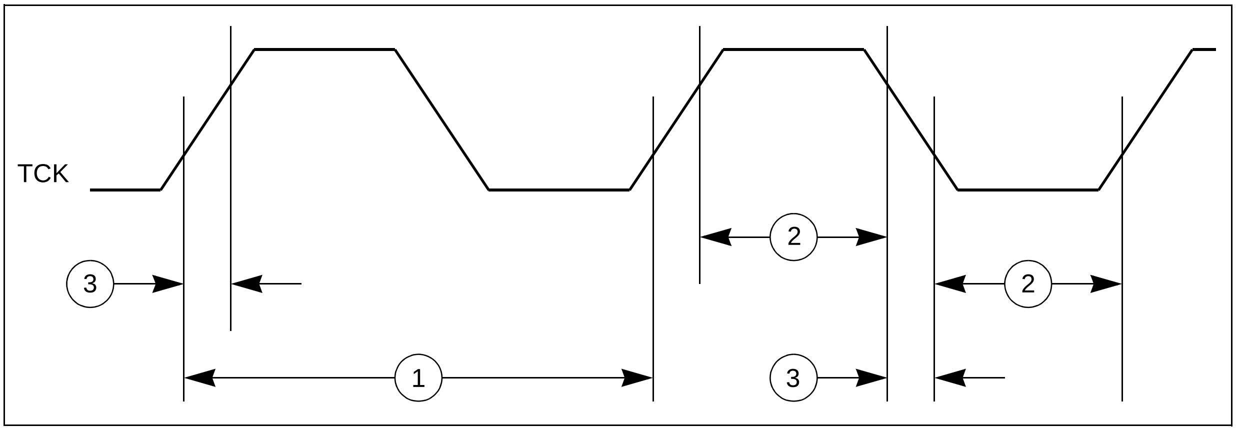


Figure 22. JTAG test clock input timing

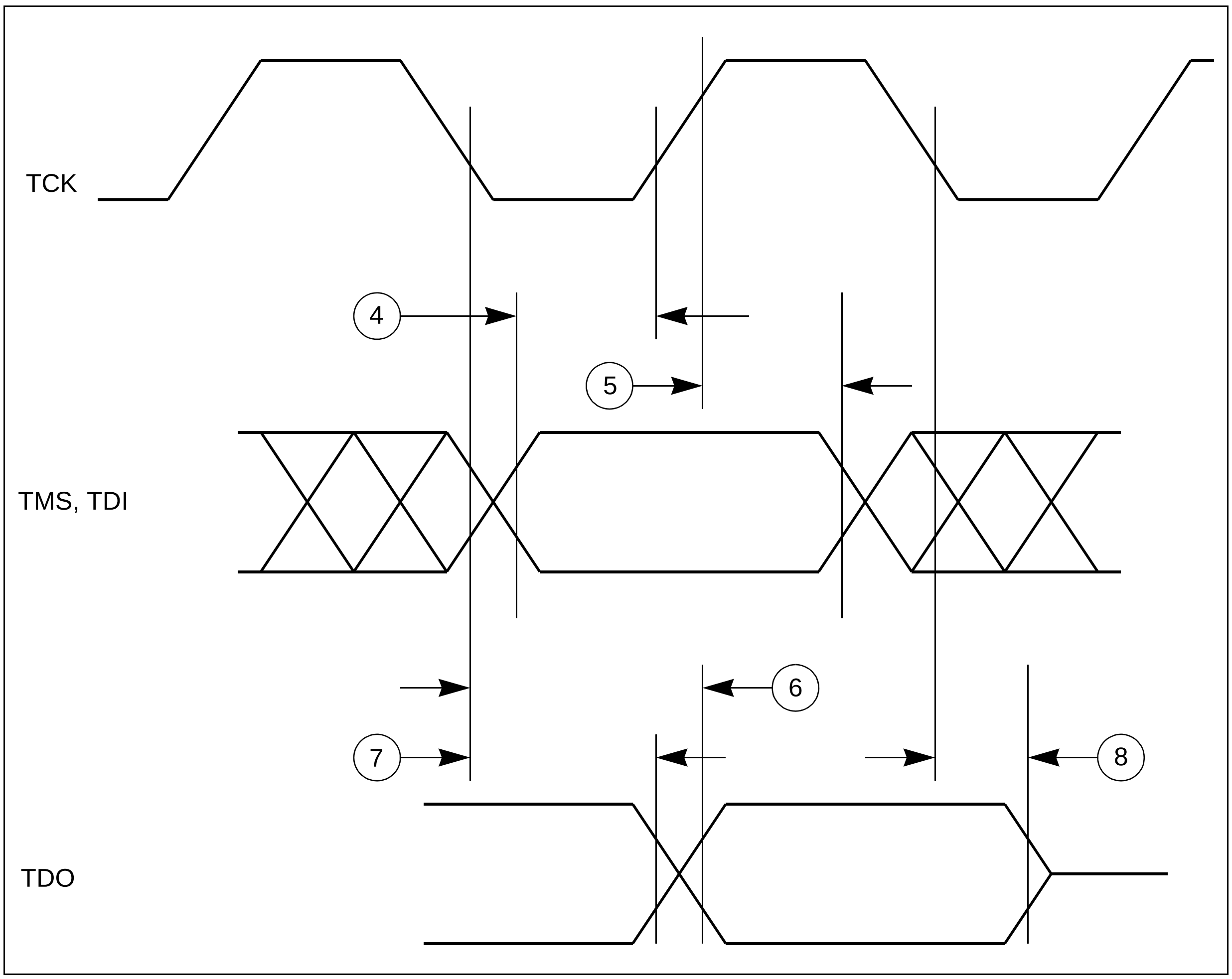


Figure 23. JTAG test access port timing

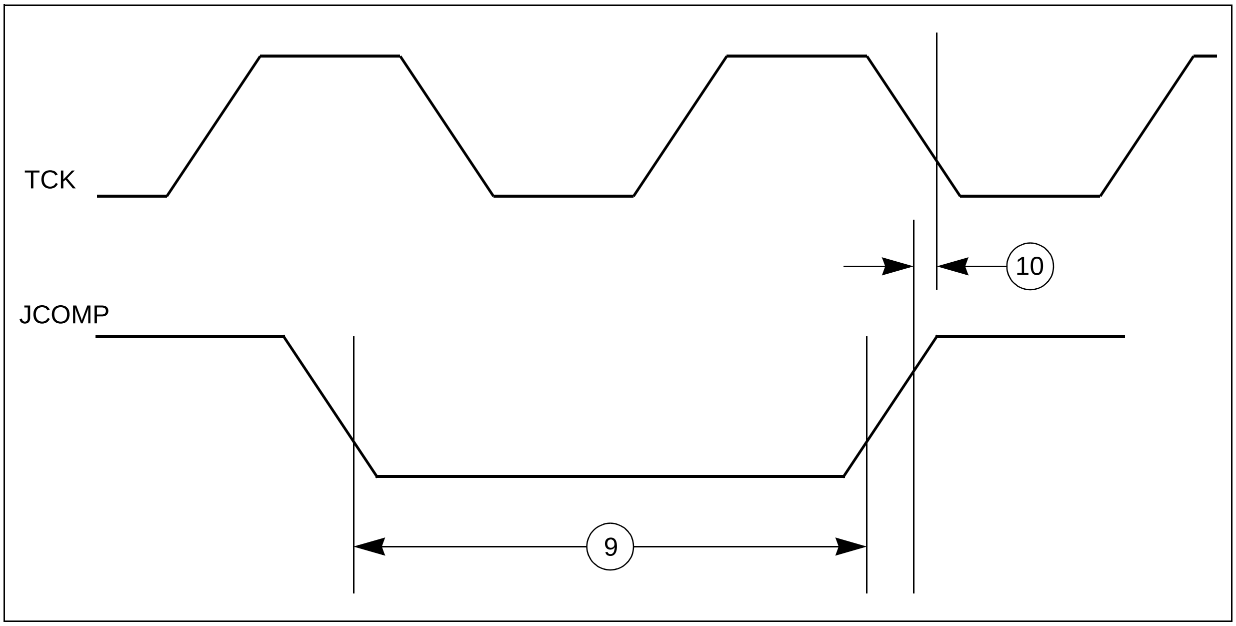


Figure 24. JTAG JCOMP timing

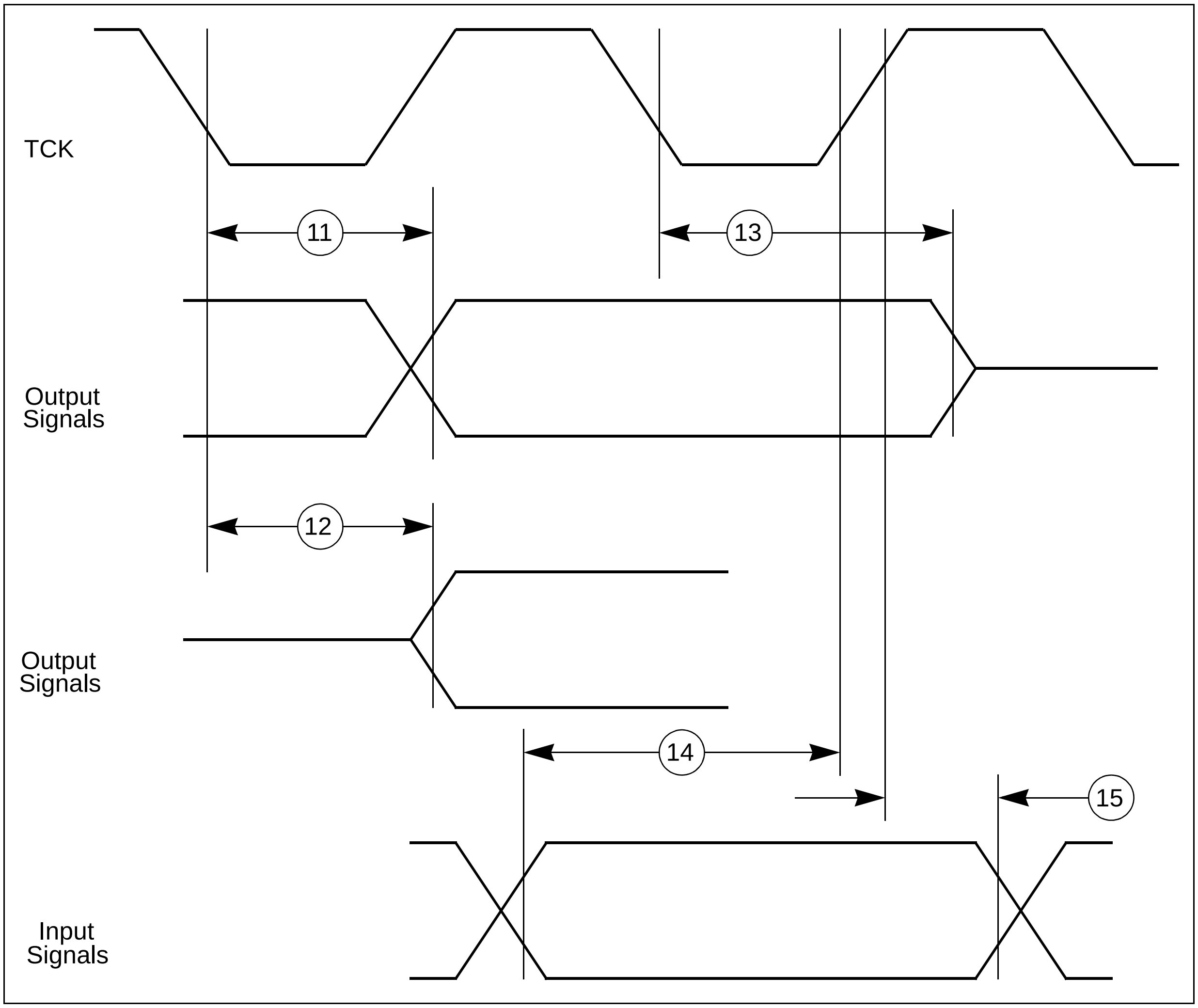


Figure 25. JTAG boundary scan timing

3.16.1.2 Nexus interface timing

Table 47. Nexus debug port timing[1]

#	Symbol		Characteristic	Value		Unit
				Min	Max	
7	t_{EVTIPW}	CC	$\overline{\text{EVTI}}$ pulse width	4	—	t_{CYC}[2]
8	t_{EVTOPW}	CC	$\overline{\text{EVTO}}$ pulse width	40	—	ns
9	t_{TCYC}	CC	TCK cycle time	2[3,4]	—	t_{CYC}[2]
9	t_{TCYC}	CC	Absolute minimum TCK cycle time[5] (TDO/TDOC sampled on posedge of TCK)	40[6]	—	ns
			Absolute minimum TCK cycle time[7] (TDO/TDOC sampled on negedge of TCK)	20[6]	—	
11[8]	t_{NTDIS}	CC	TDI/TDIC data setup time	5	—	ns

Table 47. Nexus debug port timing[1] (continued)

#	Symbol		Characteristic	Value		Unit
				Min	Max	
12	t_{NTDIH}	CC	TDI/TDIC data hold time	5	—	ns
13[9]	t_{NTMSS}	CC	TMS/TMSC data setup time	5	—	ns
14	t_{NTMSH}	CC	TMS/TMSC data hold time	5	—	ns
15[10]	—	CC	TDO/TDOC propagation delay from falling edge of TCK[11]	—	16	ns
16	—	CC	TDO/TDOC hold time with respect to TCK falling edge (minimum TDO/TDOC propagation delay)	2.25	—	ns

1 Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.

2 t_{CYC} is system clock period.

3 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.

4 This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

5 This value is TDO/TDOC propagation time 36ns + 4 ns setup time to sampling edge.

6 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This value is TDO/TDOC propagation time 16ns + 4 ns setup time to sampling edge.

8 TDIC represents the TDI bit frame of the scan packet in compact JTAG 2-wire mode.

9 TMSC represents the TMS bit frame of the scan packet in compact JTAG 2-wire mode.

10 TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.

11 Timing includes TCK pad delay, clock tree delay, logic delay and TDO/TDOC output pad delay.

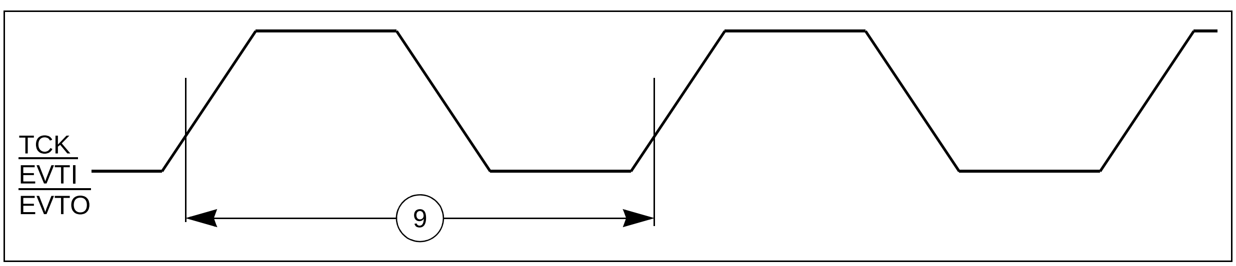


Figure 26. Nexus event trigger and test clock timings

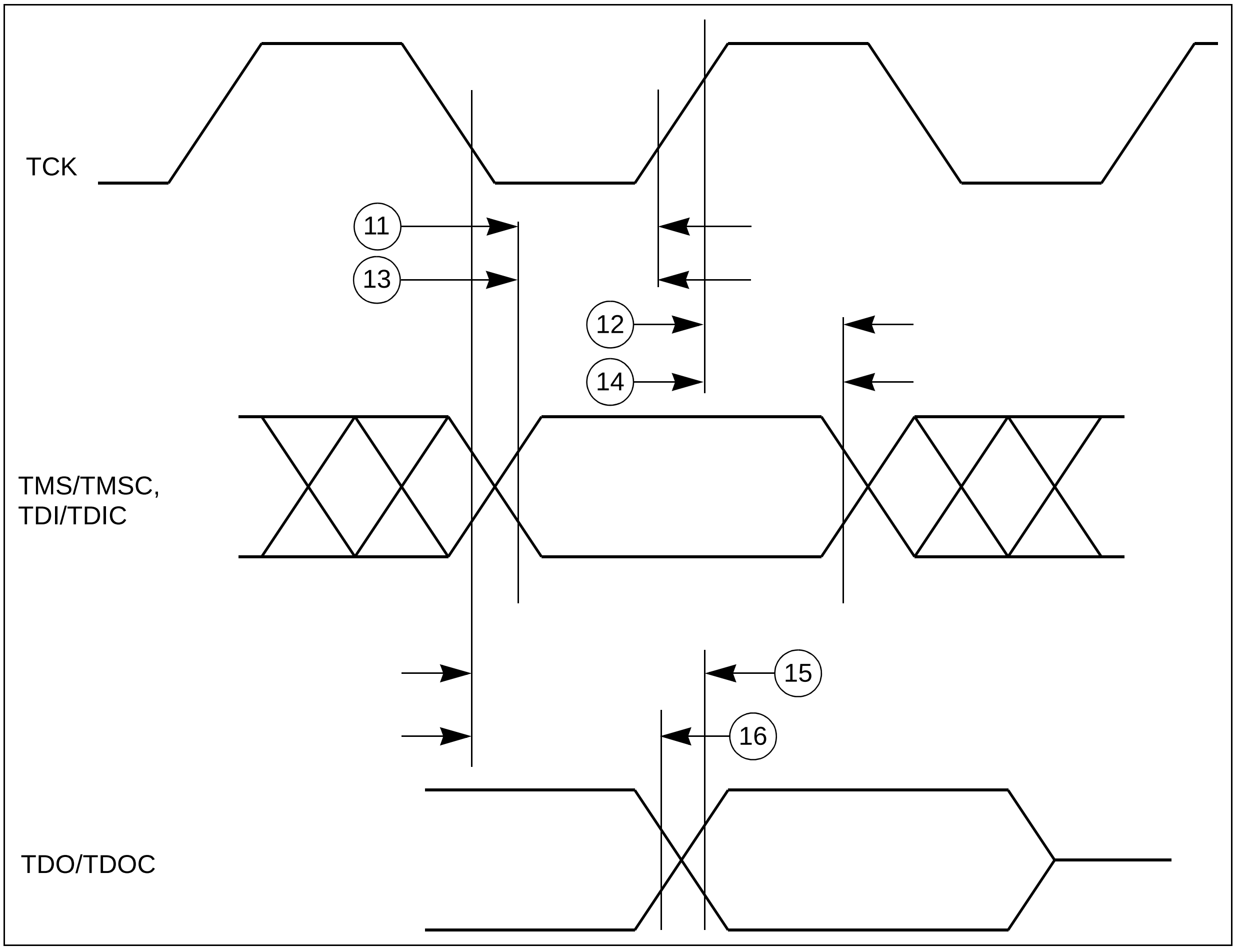


Figure 27. Nexus TDI/TDIC, TMS/TMSC, TDO/TDOC timing

3.16.1.3 Aurora LVDS interface timing

Table 48. Aurora LVDS interface timing specifications

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
Data Rate						
—	SR	Data rate	—	—	1250	Mbps
STARTUP						
t_{STRT_BIAS}	CC	Bias startup time[1]	—	—	5	µs
t_{STRT_TX}	CC	Transmitter startup time[2]	—	—	5	µs
t_{STRT_RX}	CC	Receiver startup time[3]	—	—	4	µs

[1] Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.

[2] Startup time is defined as the time taken by LVDS transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3 Startup time is defined as the time taken by LVDS receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable (see Bias start-up time). LVDS functionality is guaranteed only after the startup time.

3.16.1.4 Aurora debug port timing

Table 49. Aurora debug port timing

#	Symbol		Characteristic		Value		Unit
					Min	Max	
1	t_{REFCLK}	CC	Reference clock frequency		625	1250	MHz
1a	t_{MCYC}	CC	Reference clock rise/fall time		—	400	ps
2	t_{RCDC}	CC	Reference clock duty cycle		45	55	%
3	J_{RC}	CC	Reference clock jitter		—	40	ps
4	$t_{STABILITY}$	CC	Reference clock stability		50	—	PPM
5	BER	CC	Bit error rate		—	10^{-12}	—
6	J_D	SR	Transmit lane deterministic jitter		—	0.17	OUI
7	J_T	SR	Transmit lane total jitter		—	0.35	OUI
8	S_O	CC	Differential output skew		—	20	ps
9	S_{MO}	CC	Lane to lane output skew		—	1000	ps
10	OUI	CC	Aurora lane unit interval[1]	625 Mbps	1600	1600	ps
				1.25 Gbps	800	800	

1 ± 100 PPM

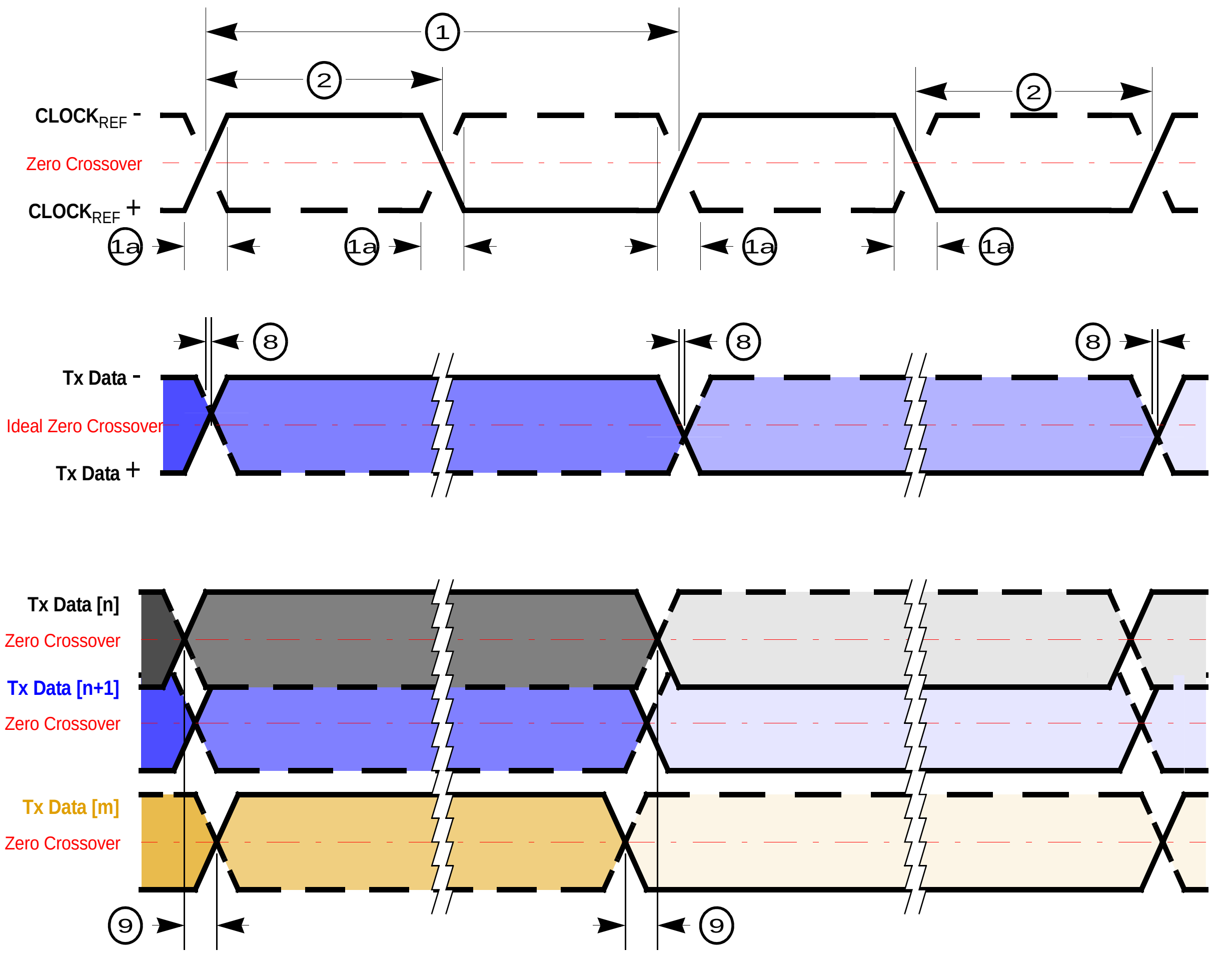


Figure 28. Aurora timings

3.16.2 DSPI timing with CMOS and LVDS[1] pads

DSPI channel frequency support is shown in Table 50. Timing specifications are shown in Table 51, Table 52, Table 54, Table 55 and Table 56.

Table 50. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1,2]
CMOS (Master mode)	Full duplex – Classic timing (Table 51)	17
	Full duplex – Modified timing (Table 52)	30
	Output only mode (SCK/SOUT/PCS) (Table 51 and Table 52)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 56)	30
LVDS (Master mode)[3]	Full duplex – Modified timing (Table 54)	33
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 55)	40

1 Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
2 Maximum usable frequency does not take into account external device propagation delay.
3 µS Channel and LVDS timing is not supported for DSPI12.

3.16.2.1 DSPI master mode full duplex timing with CMOS and LVDS pads

3.16.2.1.1 DSPI CMOS Master Mode – Classic Timing

Table 51. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	SCK cycle time	SCK drive strength				
				Very strong	25 pF	33.0	—	ns
				Strong	50 pF	80.0	—	
				Medium	50 pF	200.0	—	
2	t_{CSC}	CC	PCS to SCK delay	SCK and PCS drive strength				
				Very strong	25 pF	($N^4 \times t_{SYS}{}^5$) – 16	—	ns
				Strong	50 pF	($N^4 \times t_{SYS}{}^5$) – 16	—	
				Medium	50 pF	($N^4 \times t_{SYS}{}^5$) – 16	—	
				PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	($N^4 \times t_{SYS}{}^5$) – 29	—	

1. DSPI in TSB mode with LVDS pads can be used to implement Micro Second Channel bus protocol.

Table 51. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
3	t_{ASC}	CC	After SCK delay	SCK and PCS drive strength				
				Very strong	PCS = 0 pF SCK = 50 pF	($M^6 \times t_{SYS}{}^5$) – 35	—	ns
				Strong	PCS = 0 pF SCK = 50 pF	($M^6 \times t_{SYS}{}^5$) – 35	—	
				Medium	PCS = 0 pF SCK = 50 pF	($M^6 \times t_{SYS}{}^5$) – 35	—	
				PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	($M^6 \times t_{SYS}{}^5$) – 35	—	
4	t_{SDC}	CC	SCK duty cycle[7]	SCK drive strength				
				Very strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
				Strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	
				Medium	0 pF	$^1/_2 t_{SCK} - 5$	$^1/_2 t_{SCK} + 5$	
PCS strobe timing								
5	t_{PCSC}	CC	PCSx to $\overline{PCSS}$ time[8]	PCS and PCSS drive strength				
				Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	$\overline{PCSS}$ to PCSx time[8]	PCS and PCSS drive strength				
				Strong	25 pF	16.0	—	ns
SIN setup time								
7	t_{SUI}	CC	SIN setup time to SCK[9]	SCK drive strength				
				Very strong	25 pF	25.0	—	ns
				Strong	50 pF	32.75	—	
				Medium	50 pF	52.0	—	
SIN hold time								
8	t_{HI}	CC	SIN hold time from SCK[9]	SCK drive strength				
				Very strong	0 pF	–1.0	—	ns
				Strong	0 pF	–1.0	—	
				Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK[10]	SOUT and SCK drive strength				
				Very strong	25 pF	—	7.0	ns
				Strong	50 pF	—	8.0	
				Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)								

Table 51. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
10	t_{HO}	CC	SOUT data hold time after SCK[10]	SOUT and SCK drive strength				
				Very strong	25 pF	–7.7	—	ns
				Strong	50 pF	–11.0	—	
				Medium	50 pF	–15.0	—	

1 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2 All timing values for output signals in this table are measured to 50% of the output voltage.
3 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4 N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
5 t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
6 M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
7 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
8 PCSx and PCSS using same pad configuration.
9 Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
10 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

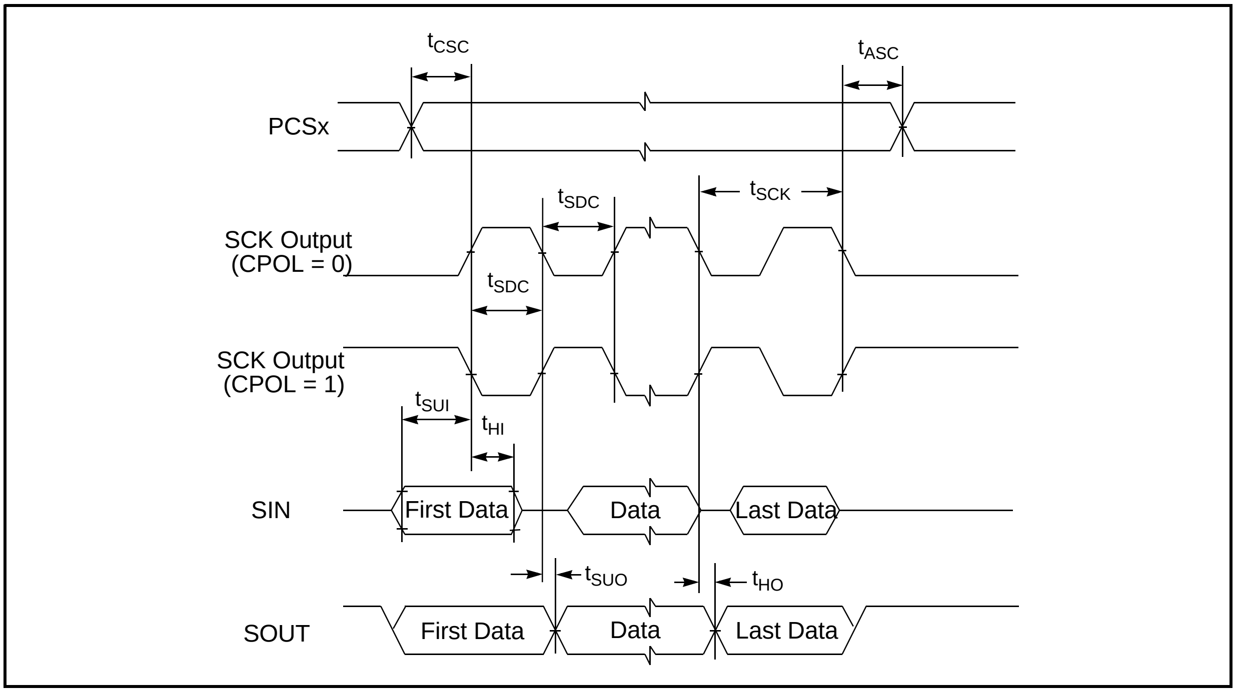


Figure 29. DSPI CMOS master mode – classic timing, CPHA = 0

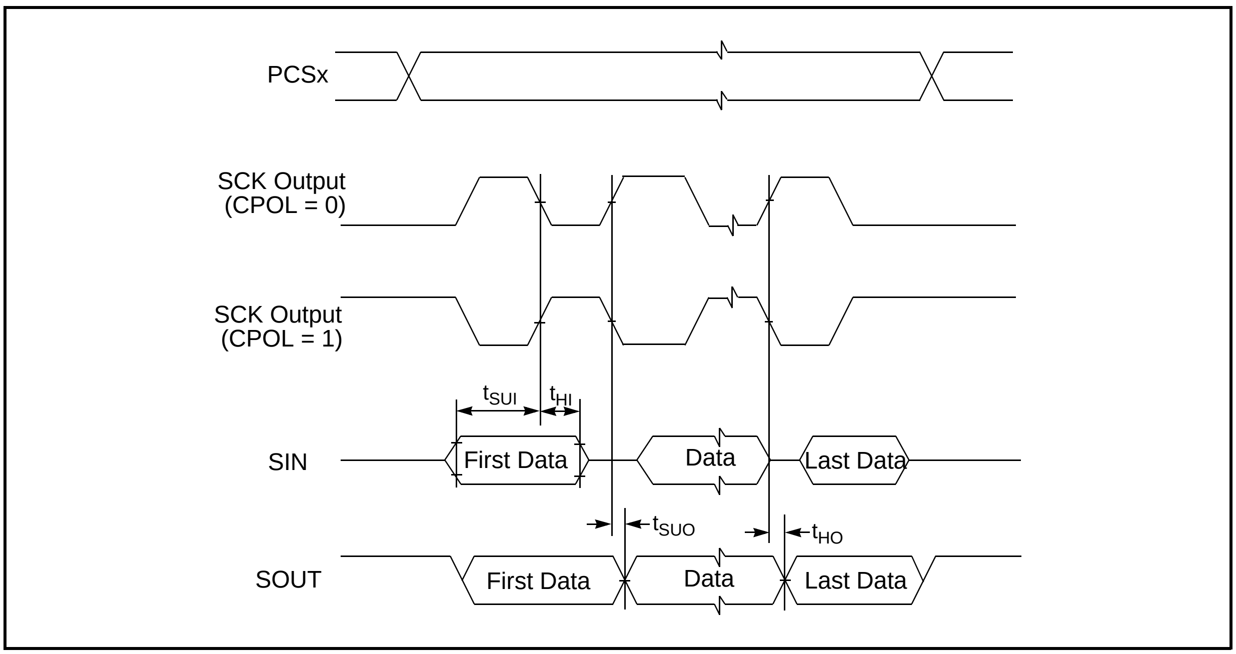


Figure 30. DSPI CMOS master mode – classic timing, CPHA = 1

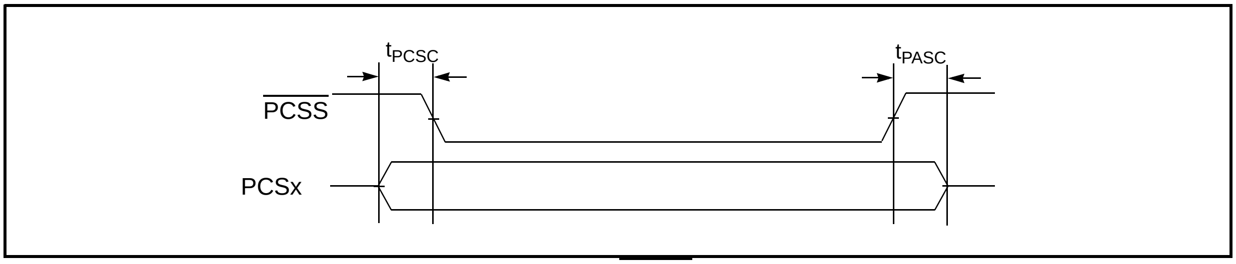


Figure 31. DSPI PCS strobe (PCSS) timing (master mode)

3.16.2.1.2 DSPI CMOS Master Mode – Modified Timing

Table 52. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	SCK cycle time	SCK drive strength				
				Very strong	25 pF	33.0	—	ns
				Strong	50 pF	80.0	—	
				Medium	50 pF	200.0	—	
2	t_{CSC}	CC	PCS to SCK delay	SCK and PCS drive strength				
				Very strong	25 pF	(N[4] × t_{SYS}[5]) – 16	—	ns
				Strong	50 pF	(N[4] × t_{SYS}[5]) – 16	—	
				Medium	50 pF	(N[4] × t_{SYS}[5]) – 16	—	
				PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	(N[4] × t_{SYS}[5]) – 29	—	
3	t_{ASC}	CC	After SCK delay	SCK and PCS drive strength				
				Very strong	PCS = 0 pF SCK = 50 pF	(M[6] × t_{SYS}[5]) – 35	—	ns
				Strong	PCS = 0 pF SCK = 50 pF	(M[6] × t_{SYS}[5]) – 35	—	
				Medium	PCS = 0 pF SCK = 50 pF	(M[6] × t_{SYS}[5]) – 35	—	
				PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	(M[6] × t_{SYS}[5]) – 35	—	
4	t_{SDC}	CC	SCK duty cycle[7]	SCK drive strength				
				Very strong	0 pF	$^1/_2 t_{SCK}$ – 2	$^1/_2 t_{SCK}$ + 2	ns
				Strong	0 pF	$^1/_2 t_{SCK}$ – 2	$^1/_2 t_{SCK}$ + 2	
				Medium	0 pF	$^1/_2 t_{SCK}$ – 5	$^1/_2 t_{SCK}$ + 5	
PCS strobe timing								

Table 52. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
5	t_{PCSC}	CC	PCSx to $\overline{\text{PCSS}}$ time[8]	PCS and PCSS drive strength				
				Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	$\overline{\text{PCSS}}$ to PCSx time[8]	PCS and PCSS drive strength				
				Strong	25 pF	16.0	—	ns
SIN setup time								
7	t_{SUI}	CC	SIN setup time to SCK CPHA = 0[9]	SCK drive strength				
				Very strong	25 pF	25 – (P[10] × t_{SYS}[5])	—	ns
				Strong	50 pF	32.75 – (P[10] × t_{SYS}[5])	—	
				Medium	50 pF	52 – (P[10] × t_{SYS}[5])	—	
			SIN setup time to SCK CPHA = 1[9]	SCK drive strength				
				Very strong	25 pF	25.0	—	ns
				Strong	50 pF	32.75	—	
				Medium	50 pF	52.0	—	
SIN hold time								
8	t_{HI}	CC	SIN hold time from SCK CPHA = 0[9]	SCK drive strength				
				Very strong	0 pF	–1 + (P[9] × t_{SYS}[4])	—	ns
				Strong	0 pF	–1 + (P[9] × t_{SYS}[4])	—	
				Medium	0 pF	–1 + (P[9] × t_{SYS}[4])	—	
			SIN hold time from SCK CPHA = 1[9]	SCK drive strength				
				Very strong	0 pF	–1.0	—	ns
				Strong	0 pF	–1.0	—	
				Medium	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK CPHA = 0[10]	SOUT and SCK drive strength				
				Very strong	25 pF	—	7.0 + t_{SYS}[5]	ns
				Strong	50 pF	—	8.0 + t_{SYS}[5]	
				Medium	50 pF	—	16.0 + t_{SYS}[5]	
			SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
				Very strong	25 pF	—	7.0	ns
				Strong	50 pF	—	8.0	
				Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)								

Table 52. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1]

#	Symbol		Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
10	t_{HO}	CC	SOUT data hold time after SCK CPHA = 0[11]	SOUT and SCK drive strength				
				Very strong	25 pF	$-7.7 + t_{SYS}$[5]	—	ns
				Strong	50 pF	$-11.0 + t_{SYS}$[5]	—	
				Medium	50 pF	$-15.0 + t_{SYS}$[5]	—	
			SOUT data hold time after SCK CPHA = 1[11]	SOUT and SCK drive strength				
				Very strong	25 pF	–7.7	—	ns
				Strong	50 pF	–11.0	—	
				Medium	50 pF	–15.0	—	

1 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

2 All timing values for output signals in this table are measured to 50% of the output voltage.

3 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

4 N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

5 t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

6 M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

7 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

8 PCSx and PCSS using same pad configuration.

9 Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.

10 P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

11 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

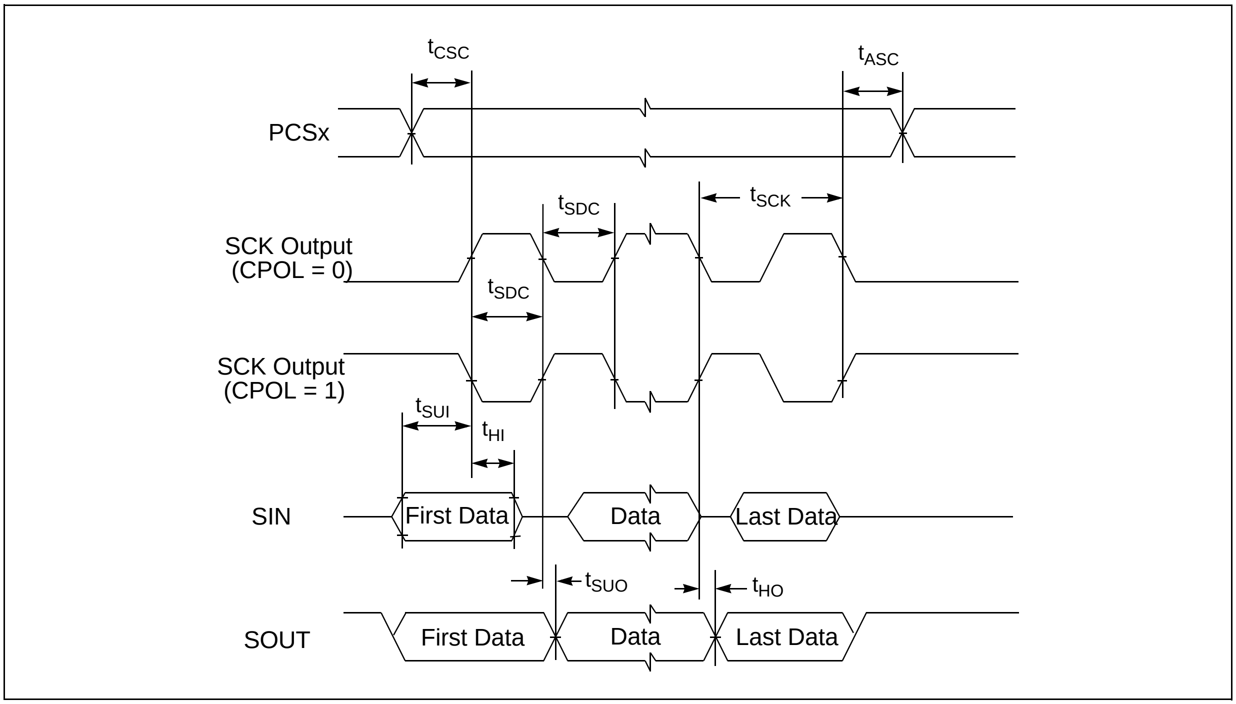


Figure 32. DSPI CMOS master mode – modified timing, CPHA = 0

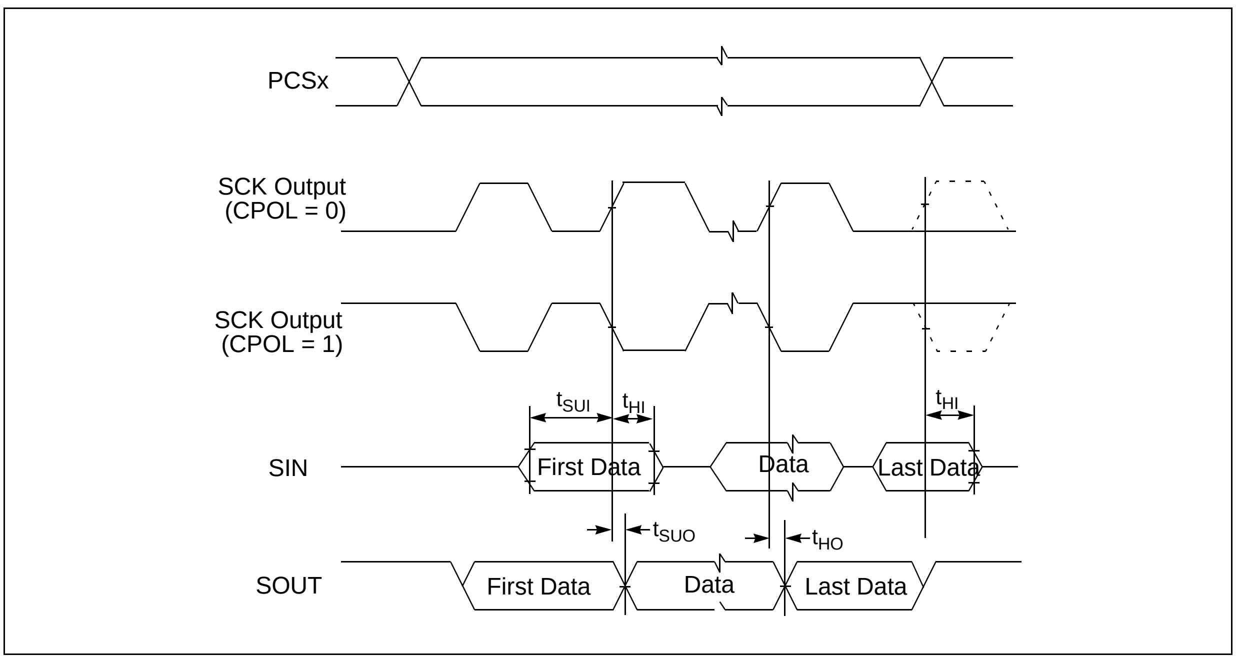


Figure 33. DSPI CMOS master mode – modified timing, CPHA = 1

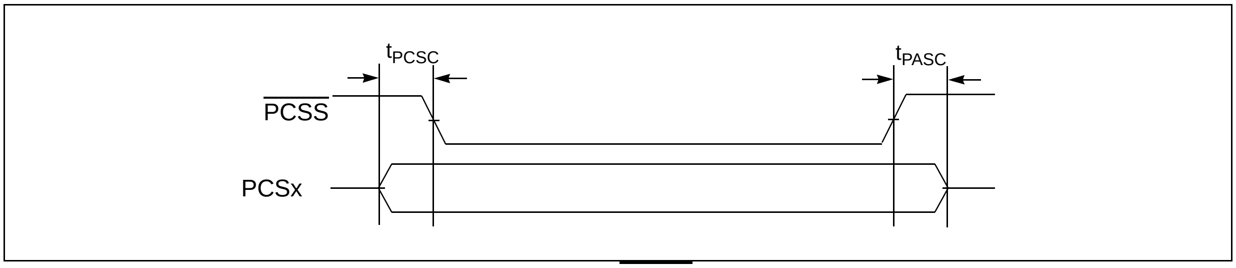


Figure 34. DSPI PCS strobe (PCSS) timing (master mode)

3.16.2.1.3 DSPI LVDS Master Mode – Modified Timing

Table 53. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol		Characteristic	Condition		Value[1]		Unit
				Pad drive	Load	Min	Max	
1	t_{SCK}	CC	SCK cycle time	LVDS	15 pF to 25 pF differential	30.0	—	ns
2	t_{CSC}	CC	PCS to SCK delay (LVDS SCK)	PCS drive strength				
				Very strong	25 pF	$(N^{2} \times t_{SYS}^{3}) - 10$	—	ns
				Strong	50 pF	$(N^{2} \times t_{SYS}^{3}) - 10$	—	ns
				Medium	50 pF	$(N^{2} \times t_{SYS}^{3}) - 32$	—	ns
3	t_{ASC}	CC	After SCK delay (LVDS SCK)	Very strong	PCS = 0 pF SCK = 25 pF	$(M^{4} \times t_{SYS}^{3}) - 8$	—	ns
				Strong	PCS = 0 pF SCK = 25 pF	$(M^{4} \times t_{SYS}^{3}) - 8$	—	ns
				Medium	PCS = 0 pF SCK = 25 pF	$(M^{4} \times t_{SYS}^{3}) - 8$	—	ns
4	t_{SDC}	CC	SCK duty cycle[5]	LVDS	15 pF to 25 pF differential	$^{1}/_{2}t_{SCK} - 2$	$^{1}/_{2}t_{SCK} + 2$	ns
7	t_{SUI}	CC	SIN setup time					
			SIN setup time to SCK CPHA = 0[6]	SCK drive strength				
				LVDS	15 pF to 25 pF differential	$23 - (P^{7} \times t_{SYS}^{3})$	—	ns
			SIN setup time to SCK CPHA = 1[6]	SCK drive strength				
				LVDS	15 pF to 25 pF differential	23	—	ns

Table 53. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol		Characteristic	Condition		Value[1]		Unit
				Pad drive	Load	Min	Max	
8	t_{HI}	CC	SIN Hold Time					
			SIN hold time from SCK CPHA = 0[6]	SCK drive strength				
				LVDS	0 pF differential	$-1 + (P^{7} \times t_{SYS}^{3})$	—	ns
			SIN hold time from SCK CPHA = 1[6]	SCK drive strength				
				LVDS	0 pF differential	–1	—	ns
9	t_{SUO}	CC	SOUT data valid time (after SCK edge)					
			SOUT data valid time from SCK CPHA = 0[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	—	$7.0 + t_{SYS}^{3}$	ns
			SOUT data valid time from SCK CPHA = 1[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	—	7.0	ns
10	t_{HO}	CC	SOUT data hold time (after SCK edge)					
			SOUT data hold time after SCK CPHA = 0[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	$-7.5 + t_{SYS}^{3}$	—	ns
			SOUT data hold time after SCK CPHA = 1[8]	SOUT and SCK drive strength				
				LVDS	15 pF to 25 pF differential	–7.5	—	ns

1 All timing values for output signals in this table are measured to 50% of the output voltage.

2 N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

3 t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).

4 M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).

5 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

6 Input timing assumes an input slew rate of 1 ns (10% – 90%) and LVDS differential voltage = ±100 mV.

7 P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

8 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 54. DSPI LVDS slave timing – full duplex – modified transfer format (MTFE = 0/1)[1]

#	Symbol		Characteristic	Condition		Value		Unit
				Pad drive	Load	Min	Max	
1	t_{SCK}	CC	SCK cycle time[2]	—	—	62	—	ns
2	t_{CSC}	SR	$\overline{SS}$ to SCK delay[2]	—	—	16	—	ns
3	t_{ASC}	SR	SCK to $\overline{SS}$ delay[2]	—	—	16	—	ns
4	t_{SDC}	CC	SCK duty cycle[2]	—	—	30	—	ns
5	t_A	CC	Slave Access Time[2, 3, 4] ($\overline{SS}$ active to SOUT driven)	Very strong	25 pF	—	50	ns
				Strong	50 pF	—	50	ns
				Medium	50 pF	—	60	ns
6	t_{DIS}	CC	Slave SOUT Disable Time [2, 3, 4]($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very strong	25 pF	—	5	ns
				Strong	50 pF	—	5	ns
				Medium	50 pF	—	10	ns
7	t_{SUI}	CC	Data setup time for inputs[2]	—	—	10	—	ns
8	t_{HI}	CC	Data hold time for inputs[2]	—	—	10	—	ns
9	t_{SUO}	CC	SOUT Valid Time[2, 3, 4] (after SCK edge)	Very strong	25 pF	—	30	ns
				Strong	50 pF	—	30	ns
				Medium	50 pF	—	50	ns
10	t_{HO}	CC	SOUT Hold Time[2, 3, 4] (after SCK edge)	Very strong	25 pF	2.5	—	ns
				Strong	50 pF	2.5	—	ns
				Medium	50 pF	2.5	—	ns

1 DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.

2 Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.

3 All timing values for output signals in this table, are measured to 50% of the output voltage.

4 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

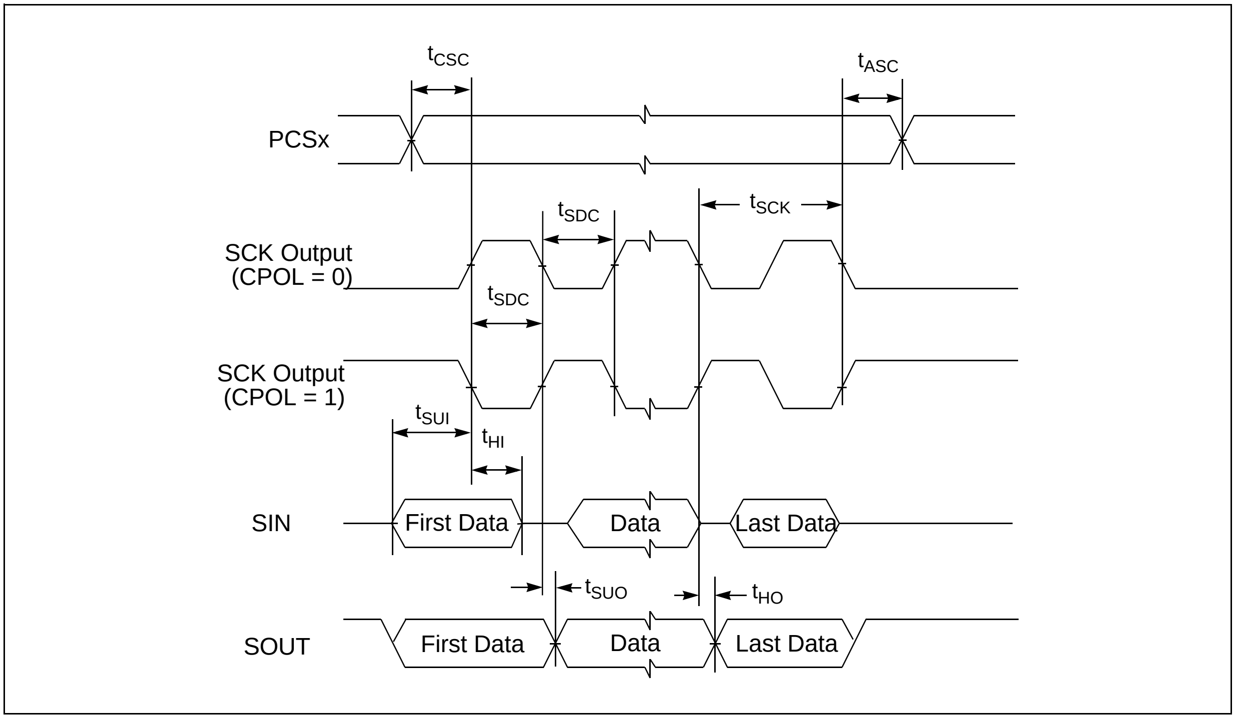


Figure 35. DSPI LVDS master mode – modified timing, CPHA = 0

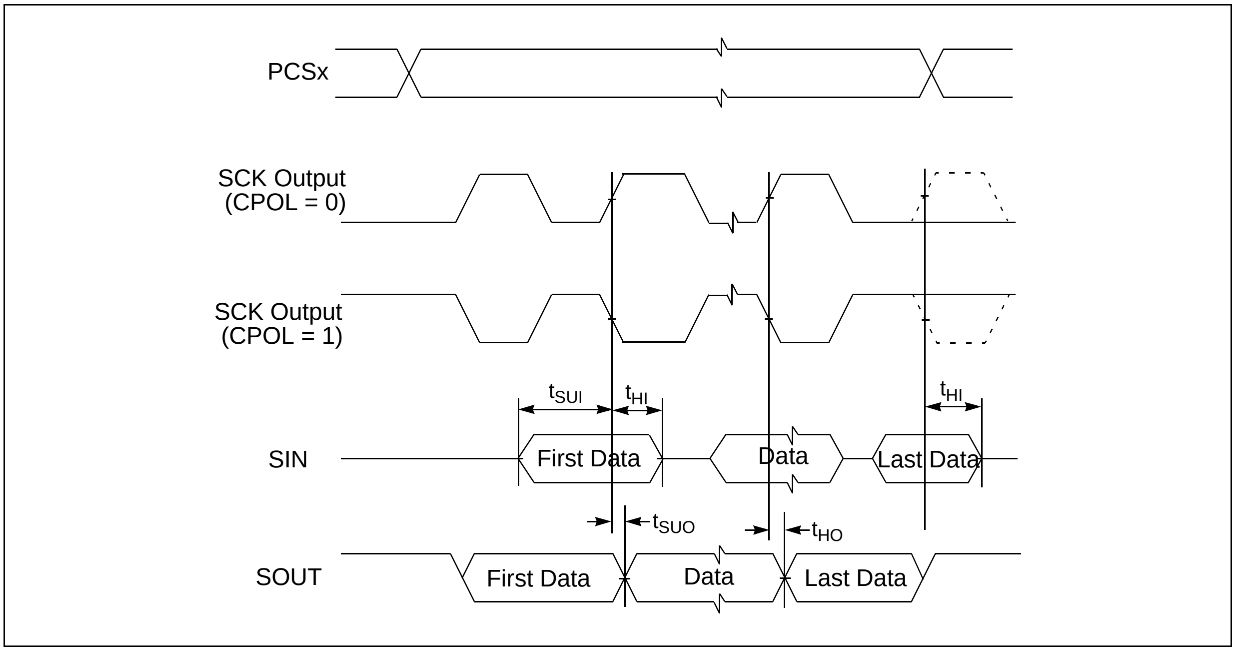


Figure 36. DSPI LVDS master mode – modified timing, CPHA = 1

3.16.2.1.4 DSPI Master Mode – Output Only

Table 55. DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2]

#	Symbol		Characteristic	Condition		Value		Unit
				Pad drive	Load	Min	Max	
1	t_{SCK}	CC	SCK cycle time	LVDS	15 pF to 50 pF differential	25.0	—	ns
2	t_{CSV}	CC	PCS valid after SCK[3] (SCK with 50 pF differential load cap.)	Very strong	25 pF	—	6.0	ns
				Strong	50 pF	—	10.5	ns
3	t_{CSH}	CC	PCS hold after SCK[3] (SCK with 50 pF differential load cap.)	Very strong	0 pF	–4.0	—	ns
				Strong	0 pF	–4.0	—	ns
4	t_{SDC}	CC	SCK duty cycle (SCK with 50 pF differential load cap.)	LVDS	15 pF to 50 pF differential	$^1/_2 t_{SCK} – 2$	$^1/_2 t_{SCK} + 2$	ns
SOUT data valid time (after SCK edge)								
5	t_{SUO}	CC	SOUT data valid time from SCK[4]	SOUT and SCK drive strength				
				LVDS	15 pF to 50 pF differential	—	3.5	ns
SOUT data hold time (after SCK edge)								
6	t_{HO}	CC	SOUT data hold time after SCK[4]	SOUT and SCK drive strength				
				LVDS	15 pF to 50 pF differential	–3.5	—	ns

1 All DSPI timing specifications apply to pins when using LVDS pads for SCK and SOUT and CMOS pad for PCS with pad driver strength as defined. Timing may degrade for weaker output drivers.

2 TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.

3 With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.

4 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 56. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2]

#	Symbol		Characteristic	Condition		Value[3]		Unit
				Pad drive[4]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	SCK cycle time	SCK drive strength				
				Very strong	25 pF	33.0	—	ns
				Strong	50 pF	80.0	—	ns
				Medium	50 pF	200.0	—	ns

Table 56. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock[1,2] (continued)

#	Symbol		Characteristic	Condition		Value[3]		Unit
				Pad drive[4]	Load (C_L)	Min	Max	
2	t_{CSV}	CC	PCS valid after SCK[5]	SCK and PCS drive strength				
				Very strong	25 pF	7	—	ns
				Strong	50 pF	8	—	ns
				Medium	50 pF	16	—	ns
				PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	29	—	ns
3	t_{CSH}	CC	PCS hold after SCK[5]	SCK and PCS drive strength				
				Very strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
				Strong	PCS = 0 pF SCK = 50 pF	–14	—	ns
				Medium	PCS = 0 pF SCK = 50 pF	–33	—	ns
				PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	–35	—	ns
4	t_{SDC}	CC	SCK duty cycle[6]	SCK drive strength				
				Very strong	0 pF	$^1/_2t_{SCK} – 2$	$^1/_2t_{SCK} + 2$	ns
				Strong	0 pF	$^1/_2t_{SCK} – 2$	$^1/_2t_{SCK} + 2$	ns
				Medium	0 pF	$^1/_2t_{SCK} – 5$	$^1/_2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)								
9	t_{SUO}	CC	SOUT data valid time from SCK CPHA = 1[7]	SOUT and SCK drive strength				
				Very strong	25 pF	—	7.0	ns
				Strong	50 pF	—	8.0	ns
				Medium	50 pF	—	16.0	ns
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	SOUT data hold time after SCK CPHA = 1[7]	SOUT and SCK drive strength				
				Very strong	25 pF	–7.7	—	ns
				Strong	50 pF	–11.0	—	ns
				Medium	50 pF	–15.0	—	ns

1 TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.

2 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

3 All timing values for output signals in this table are measured to 50% of the output voltage.

4 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

5 With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.

6 t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.

7 SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

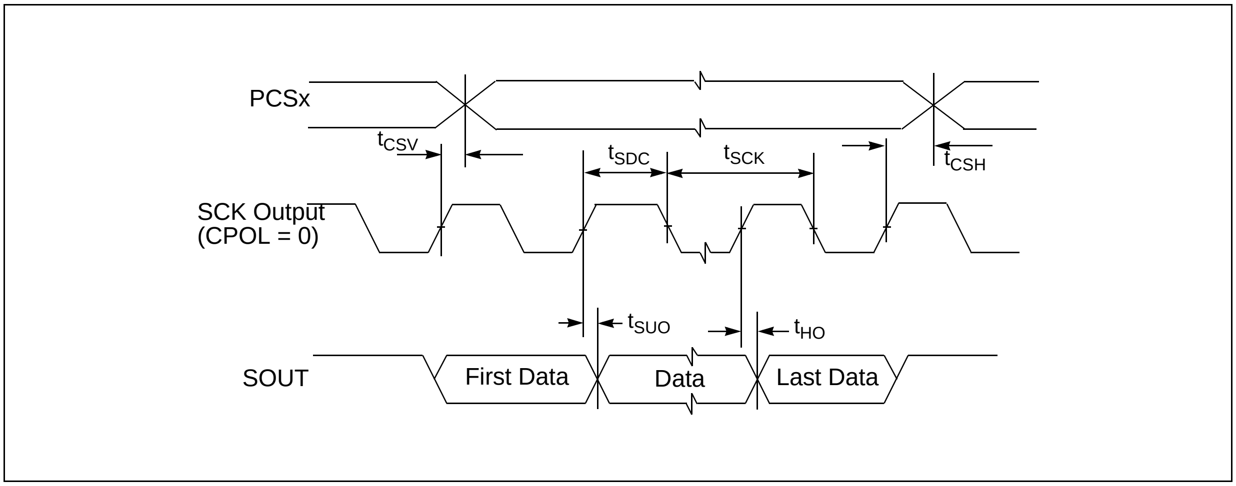


Figure 37. DSPI LVDS and CMOS master timing – output only – modified transfer format MTFE = 1, CHPA = 1

3.16.2.2 Slave Mode timing

Table 57. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)[1]

#	Symbol		Characteristic	Condition		Min	Max	Unit
				Pad Drive	Load			
1	t_{SCK}	CC	SCK Cycle Time[2]	-	-	62	—	ns
2	t_{CSC}	SR	$\overline{SS}$ to SCK Delay[2]	-	-	16	—	ns
3	t_{ASC}	SR	SCK to $\overline{SS}$ Delay[2]	-	-	16	—	ns
4	t_{SDC}	CC	SCK Duty Cycle[2]	-	-	30	—	ns
5	t_A	CC	Slave Access Time[2,3,4] ($\overline{SS}$ active to SOUT driven)	Very Strong	25 pF	—	50	ns
				Strong	50 pF	—	50	ns
				Medium	50 pF	—	60	ns
6	t_{DIS}	CC	Slave SOUT Disable Time[2,3,4] ($\overline{SS}$ inactive to SOUT High-Z or invalid)	Very Strong	25 pF	—	5	ns
				Strong	50 pF	—	5	ns
				Medium	50 pF	—	10	ns
9	t_{SUI}	CC	Data Setup Time for Inputs[2]	—	—	10	—	ns
10	t_{HI}	CC	Data Hold Time for Inputs[2]	—	—	10	—	ns

Table 57. DSPI CMOS Slave timing - Modified Transfer Format (MTFE = 0/1)[1]

#	Symbol		Characteristic	Condition: Pad Drive	Condition: Load	Min	Max	Unit
11	t_{SUO}	CC	SOUT Valid Time[2,3,4] (after SCK edge)	Very Strong	25 pF	—	30	ns
				Strong	50 pF	—	30	ns
				Medium	50 pF	—	50	ns
12	t_{HO}	CC	SOUT Hold Time[2,3,4] (after SCK edge)	Very Strong	25 pF	2.5	—	ns
				Strong	50 pF	2.5	—	ns
				Medium	50 pF	2.5	—	ns

1 DSPI slave operation is only supported for a single master and single slave on the device. Timing is valid for that case only.

2 Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL / Automotive voltage thresholds.

3 All timing values for output signals in this table, are measured to 50% of the output voltage.

4 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

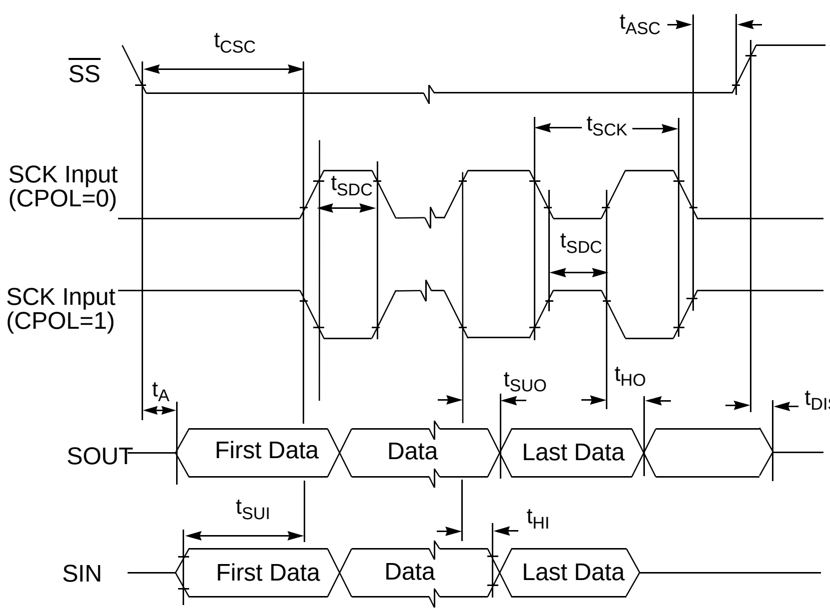


Figure 38. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 0

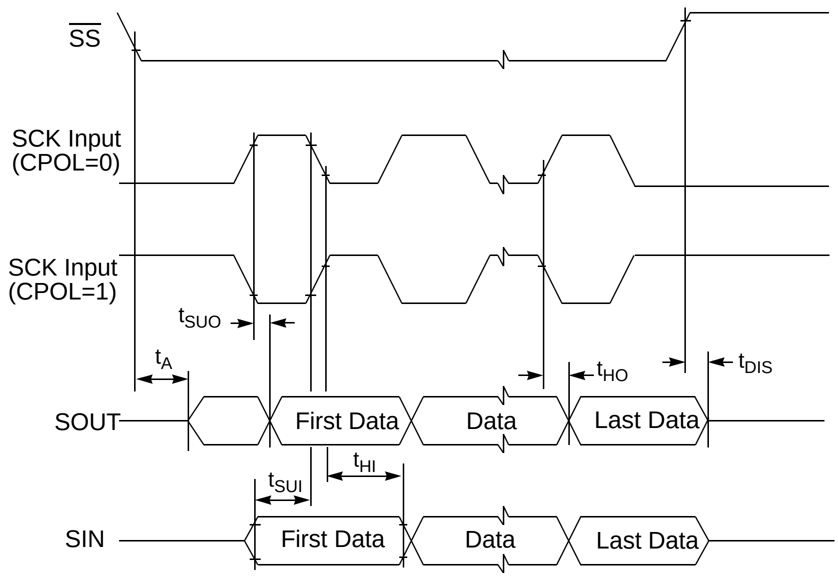


Figure 39. DSPI Slave Mode - Modified transfer format timing (MFTE = 0/1) — CPHA = 1

3.16.3 FEC timing

The FEC provides both MII and RMII interfaces in the 416 TEPBGA and 512 TEPBGA packages, and the MII and RMII signals can be configured for either CMOS or TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

3.16.3.1 MII receive signal timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency.

Table 58. MII receive signal timing[1]

Symbol		Characteristic	Value		Unit
			Min	Max	
M1	CC	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	CC	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	CC	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	CC	RX_CLK pulse width low	35%	65%	RX_CLK period

1 All timing specifications are referenced from RX_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

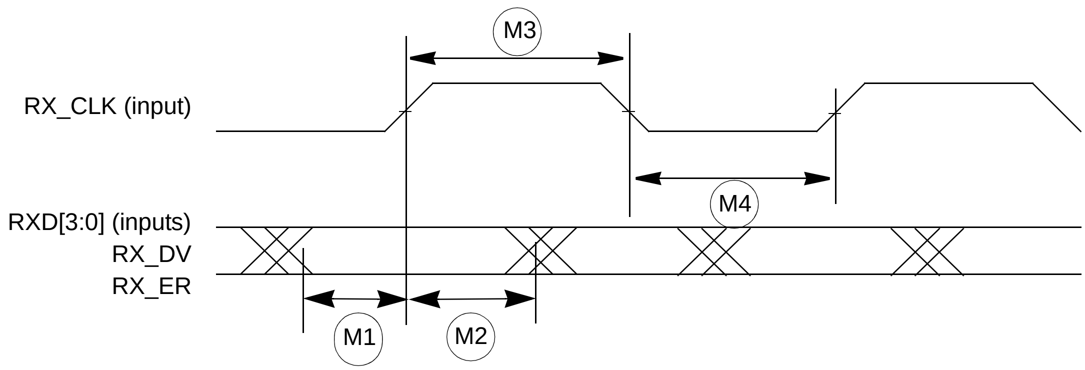


Figure 40. MII receive signal timing diagram

3.16.3.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the *MPC5777M Microcontroller Reference Manual's* Fast Ethernet Controller (FEC) chapter for details of this option and how to enable it.

Table 59. MII transmit signal timing[1]

Symbol		Characteristic	Value[2]		Unit
			Min	Max	
M5	CC	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
M6	CC	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
M7	CC	TX_CLK pulse width high	35%	65%	TX_CLK period
M8	CC	TX_CLK pulse width low	35%	65%	TX_CLK period

[1] All timing specifications are referenced from TX_CLK = 1.4 V to the valid output levels, 0.8 V and 2.0 V.

[2] Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

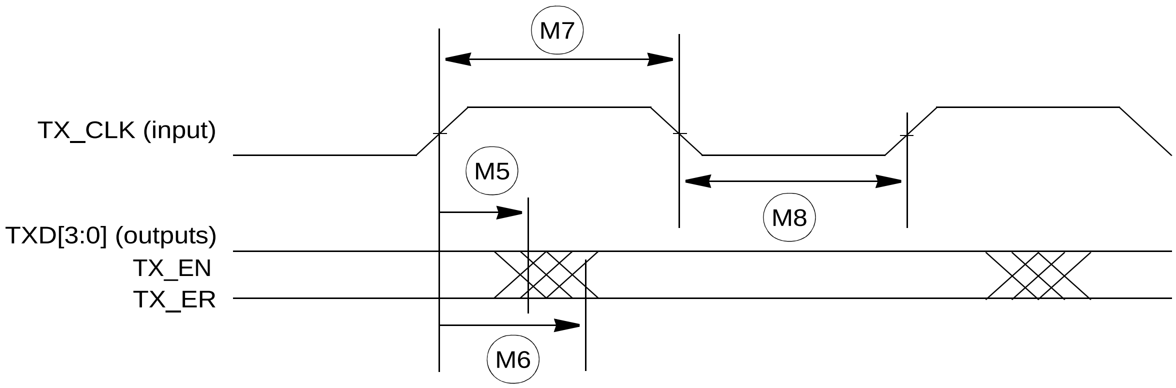


Figure 41. MII transmit signal timing diagram

3.16.3.3 MII async inputs signal timing (CRS and COL)

Table 60. MII async inputs signal timing

Symbol		Characteristic	Value		Unit
			Min	Max	
M9	CC	CRS, COL minimum pulse width	1.5	—	TX_CLK period

Figure 42. MII async inputs timing diagram

3.16.3.4 MII and RMII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 61. MII serial management channel timing[1]

Symbol		Characteristic	Value[2]		Unit
			Min	Max	
M10	CC	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
M11	CC	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
M12	CC	MDIO (input) to MDC rising edge setup	10	—	ns
M13	CC	MDIO (input) to MDC rising edge hold	0	—	ns
M14	CC	MDC pulse width high	40%	60%	MDC period
M15	CC	MDC pulse width low	40%	60%	MDC period

1 All timing specifications are referenced from MDC = 1.4 V (TTL levels) to the valid input and output levels, 0.8 V and 2.0 V (TTL levels). For 5 V operation, timing is referenced from MDC = 50% to 2.2 V/3.5 V input and output levels.

2 Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

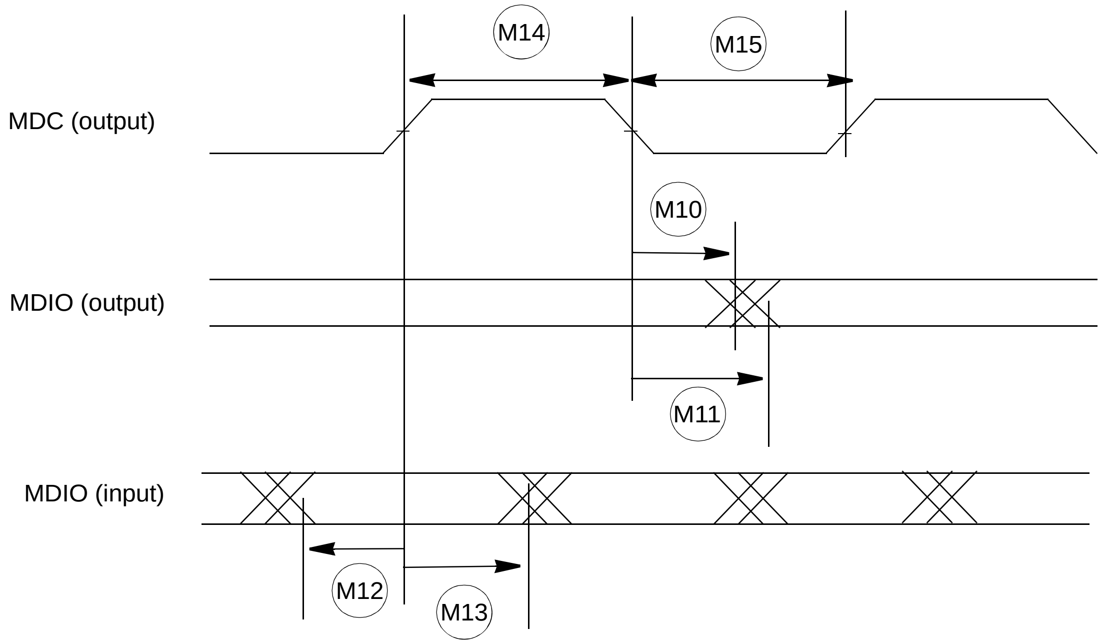


Figure 43. MII serial management channel timing diagram

3.16.3.5 RMII receive signal timing (RXD[1:0], CRS_DV)

The receiver functions correctly up to a REF_CLK maximum frequency of 50 MHz +1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the RX_CLK frequency, which is half that of the REF_CLK frequency.

Table 62. RMII receive signal timing[1]

Symbol		Characteristic	Value		Unit
			Min	Max	
R1	CC	RXD[1:0], CRS_DV to REF_CLK setup	4	—	ns
R2	CC	REF_CLK to RXD[1:0], CRS_DV hold	2	—	ns
R3	CC	REF_CLK pulse width high	35%	65%	REF_CLK period
R4	CC	REF_CLK pulse width low	35%	65%	REF_CLK period

1 All timing specifications are referenced from REF_CLK = 1.4 V to the valid input levels, 0.8 V and 2.0 V.

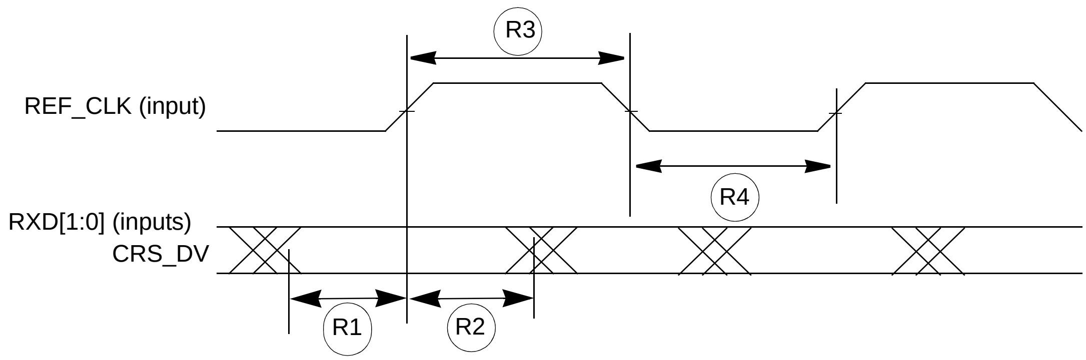


Figure 44. RMII receive signal timing diagram

3.16.3.6 RMII transmit signal timing (TXD[1:0], TX_EN)

The transmitter functions correctly up to a REF_CLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. The system clock frequency must be at least equal to or greater than the TX_CLK frequency, which is half that of the REF_CLK frequency.

The transmit outputs (TXD[1:0], TX_EN) can be programmed to transition from either the rising or falling edge of REF_CLK, and the timing is the same in either case. These options allows the use of non-compliant RMII PHYs.

Table 63. RMII transmit signal timing[1, 2]

Symbol		Characteristic	Value[3]		Unit
			Min	Max	
R5	CC	REF_CLK to TXD[1:0], TX_EN invalid	2	—	ns
R6	CC	REF_CLK to TXD[1:0], TX_EN valid	—	16	ns
R7	CC	REF_CLK pulse width high	35%	65%	REF_CLK period
R8	CC	REF_CLK pulse width low	35%	65%	REF_CLK period

1 RMII timing is valid only up to a maximum of 150 ^{o}C junction temperature.

2 All timing specifications are referenced for TTL or CMOS input levels for REF_CLK to the valid output levels, 0.8 V and 2.0 V.

3 Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

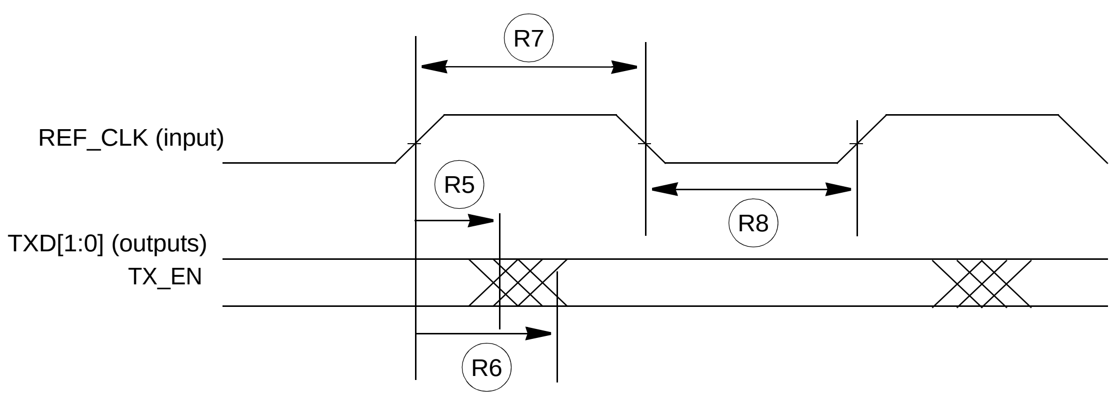


Figure 45. RMII transmit signal timing diagram

3.16.4 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals.

These are recommended numbers as per the FlexRay EPL v3.0 specification.

3.16.4.1 TxEN

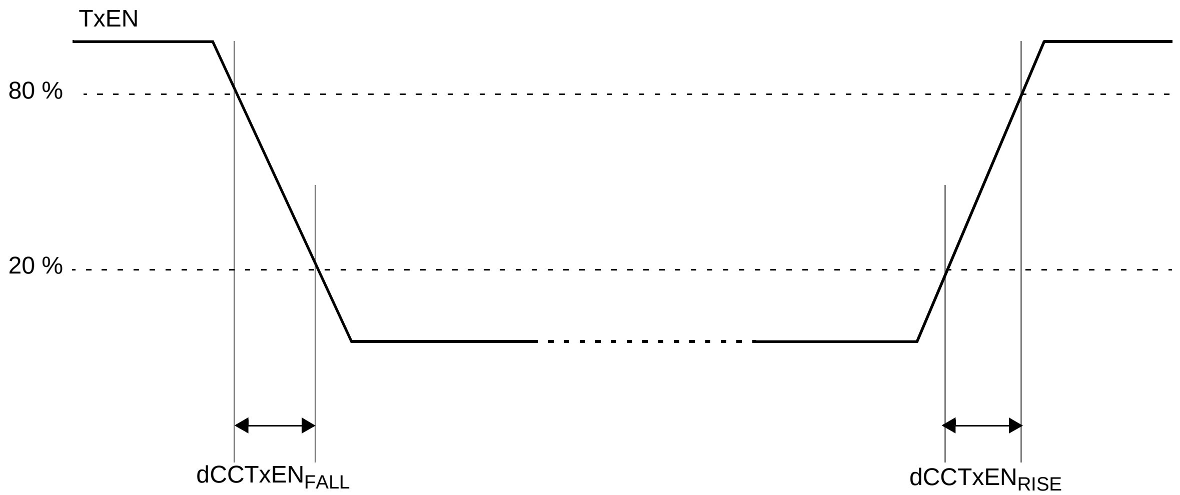


Figure 46. TxEN signal

Table 64. TxEN output characteristics[1]

Symbol		Characteristic	Value		Unit
			Min	Max	
$dCCTxEN_{RISE25}$	CC	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	CC	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1 TxEN pin load maximum 25 pF

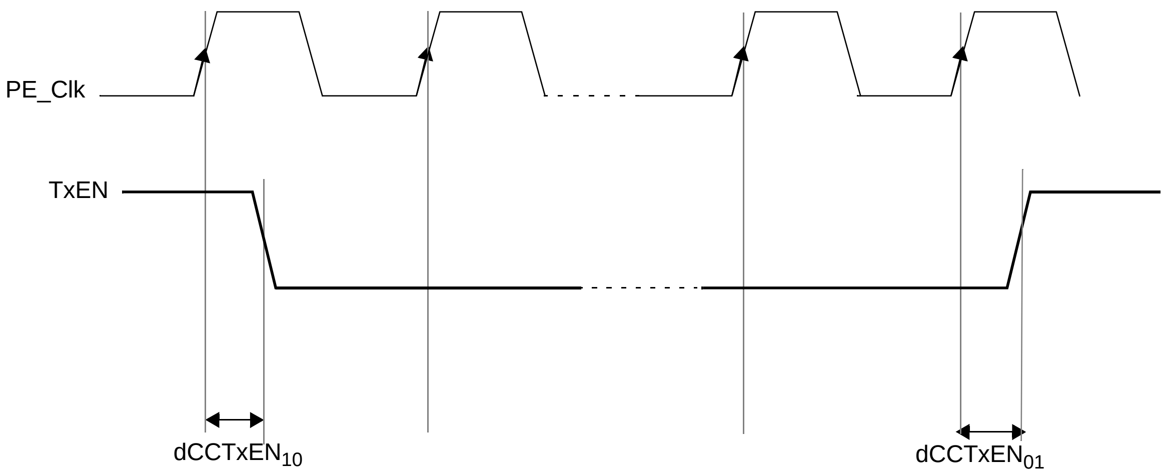


Figure 47. TxEN signal propagation delays

3.16.4.2 TxD

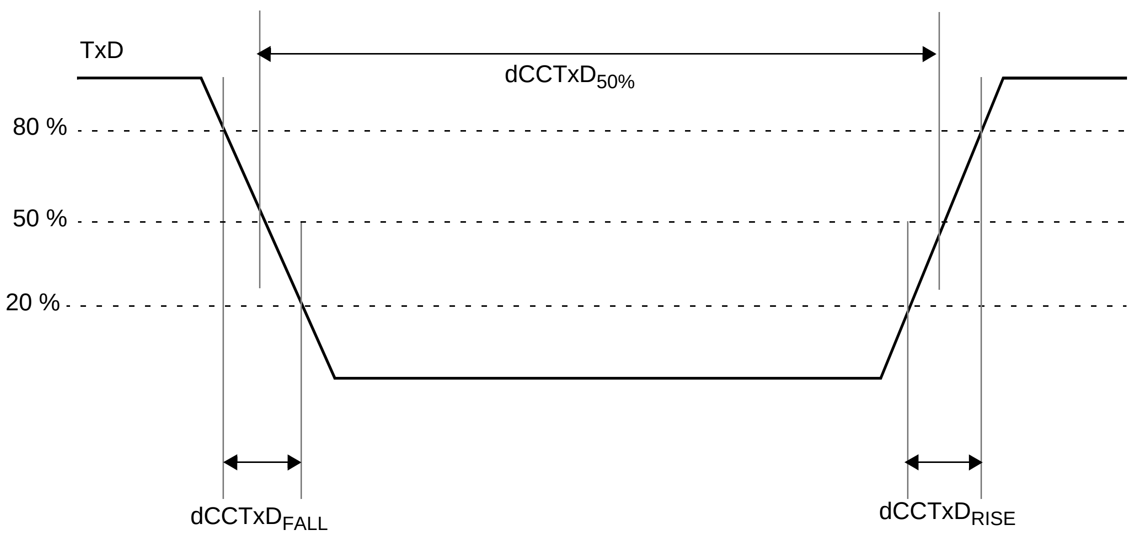


Figure 48. TxD signal

Table 65. TxD output characteristics[1,2]

Symbol		Characteristic	Value		Unit
			Min	Max	
dCCTxAsym	CC	Asymmetry of sending CC at 25 pF load (= $dCCTxD_{50\%}$ – 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	CC	Sum of Rise and Fall time of TxD signal at the output pin[3,4]	—	9[5]	ns
			—	9[6]	
$dCCTxD_{01}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	CC	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1 TxD pin load maximum 25 pF

2 Specifications valid according to FlexRay EPL 3.0.1 standard with 20%–80% levels and a 10pF load at the end of a 50 Ohm, 1 ns stripline. Please refer to the Very Strong I/O pad specifications.

3 Pad configured as VERY STRONG

4 Sum of transition time simulation is performed according to Electrical Physical Layer Specification 3.0.1 and the entire temperature range of the device has been taken into account.

5 $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF

6 $V_{DD\_HV\_IO}$ = 3.3 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 0.6 ns, C_L = 10 pF

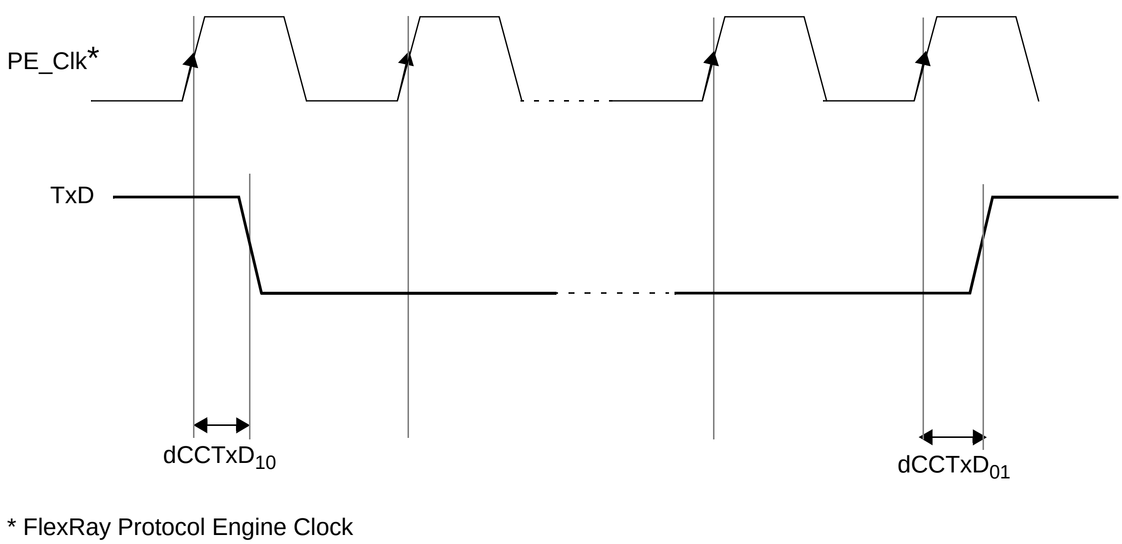


Figure 49. TxD Signal propagation delays

3.16.4.3 RxD

Table 66. RxD input characteristics[1]

Symbol		Characteristic	Value		Unit
			Min	Max	
C_CCRxD	CC	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	CC	Threshold for detecting logic high	35	70	%
uCCLogic_0	CC	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	CC	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	CC	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns
dCCRxAsymAccept15	CC	Acceptance of asymmetry at receiving CC with 15 pF load	–31.5	44	ns
dCCRxAsymAccept25	CC	Acceptance of asymmetry at receiving CC with 25 pF load	–30.5	43	ns

1 FlexRay RxD timing is valid for Automotive input levels with hysteresis enabled (hysteresis permanently enabled in Automotive input levels) and CMOS input levels with hysteresis disabled, 4.5 V ≤ $V_{DD\_HV\_IO}$ ≤ 5.5 V for both cases.

3.16.5 PSI5 timing

The following table describes the PSI5 timing.

Table 67. PSI5 timing

Symbol		Parameter	Value		Unit
			Min	Max	
t_{MSG_DLY}	CC	Delay from last bit of frame (CRC0) to assertion of new message received interrupt	—	3	µs
t_{SYNC_DLY}	CC	Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	2	µs
t_{MSG_JIT}	CC	Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt	—	1	cycles[1]
t_{SYNC_JIT}	CC	Delay jitter from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin	—	±(1 PSI5_1µs_CLK + 1 PBRIDGEn_CLK)	cycles

1 Measured in PSI5 clock cycles (PBRIDGEn_CLK on the device). Minimum PSI5 clock period is 20 ns.

3.16.6 UART timing

UART channel frequency support is shown in the following table.

Table 68. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

3.16.7 External Bus Interface (EBI) Timing

Table 69. Bus Operation Timing[1]

Spec	Characteristic	Symbol	66.7 MHz (Ext. Bus Freq)[2 3]		Unit
			Min	Max	
1	CLKOUT Period[4]	t_C	15.15	—	ns
2	CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C
3	CLKOUT Rise Time	t_{CRT}	—	—[5]	ns
4	CLKOUT Fall Time	t_{CFT}	—	—[5]	ns
5	CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time)[6] ADDR[12:31] ADDR[8:11]/WE[0:3]/BE[0:3] BDIP CS[0:3] DATA[0:31] OE RD_WR TS	t_{COH}	1.0	—	ns
6	CLKOUT Posedge to Output Signal Valid (Output Delay)[7,8] ADDR[12:31] ADDR[8:11]/WE[0:3]/BE[0:3] BDIP CS[0:3] DATA[0:31] OE RD_WR TS	t_{COV}	—	8.0	ns

Table 69. Bus Operation Timing[1] (continued)

Spec	Characteristic	Symbol	66.7 MHz (Ext. Bus Freq)[2 3]		Unit
			Min	Max	
7	Input Signal Valid to CLKOUT Posedge (Setup Time) DATA[0:31]	t_{CIS}	7.0	—	ns
8	CLKOUT Posedge to Input Signal Invalid (Hold Time) DATA[0:31]	t_{CIH}	1.0	—	ns

1 EBI timing specified at $V_{DD\_HV\_IO\_EBI}$ and $V_{DD\_HV\_IO\_FLEXE}$ = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10 for ADDR/CTRL and DSC = 0b11 for CLKOUT/DATA.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including PLL jitter.

3 Depending on the internal bus speed, set the CGM_SC_DC4 register bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66.7 MHz.

4 Signals are measured at 50% $V_{DD\_HV\_IO\_EBI}$ or $V_{DD\_HV\_IO\_FLEXE}$.

5 Refer to Fast pad timing in Table 18.

6 CLKOUT may be required at the highest drive strength in order to meet the hold time specification.

7 One wait state must be added for all write accesses to external memories at the maximum external bus frequency.

8 One wait state must be added to the outut signal valid delay for external writes.

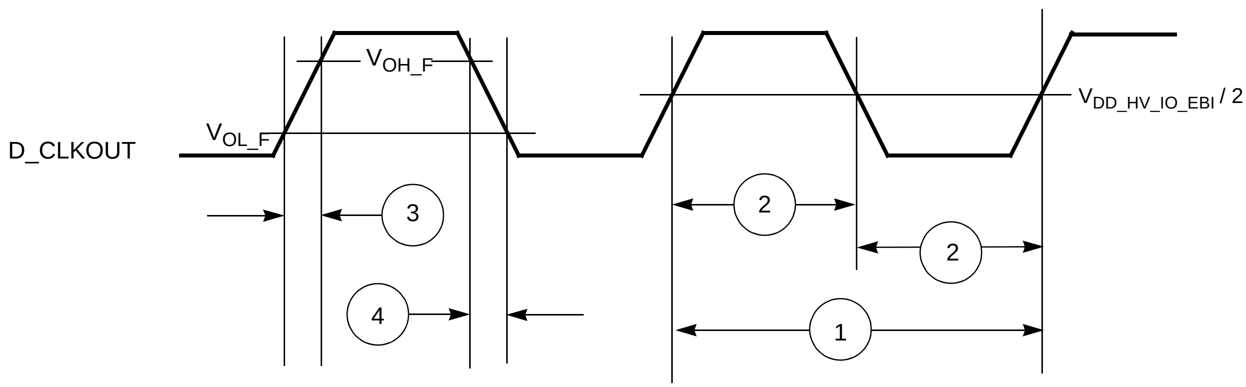


Figure 50. D_CLKOUT Timing

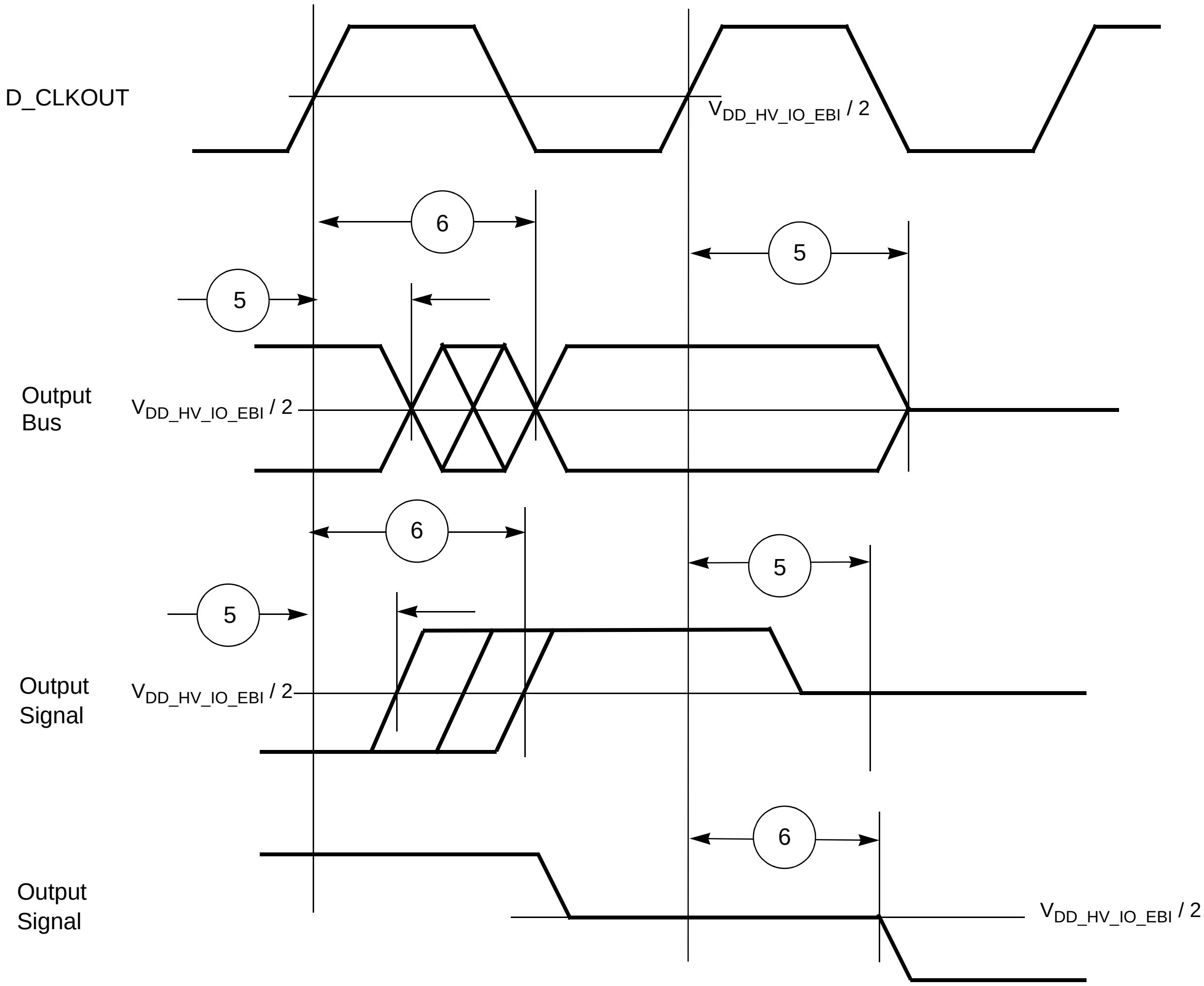


Figure 51. Synchronous Output Timing

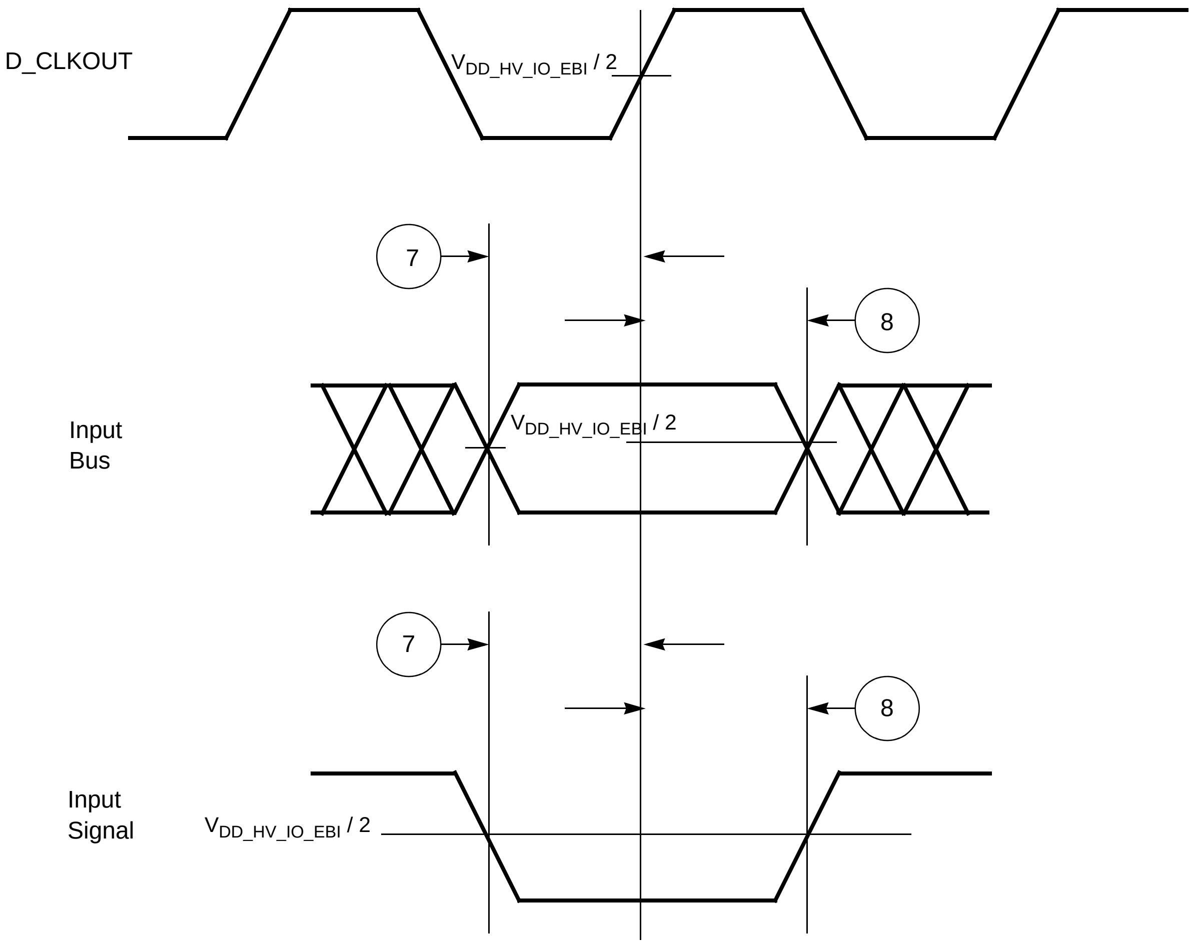


Figure 52. Synchronous Input Timing

3.16.8 I²C timing

The I²C AC timing specifications are provided in the following tables.

Table 70. I²C input timing specifications — SCL and SDA[1]

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1	—	CC	Start condition hold time	2	—	PER_CLK Cycle[2]
2	—	CC	Clock low time	8	—	PER_CLK Cycle
3	—	CC	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	Data hold time	0.0	—	ns

Table 70. I²C input timing specifications — SCL and SDA[1] (continued)

No.	Symbol		Parameter	Value		Unit
				Min	Max	
5	—	CC	Clock high time	4	—	PER_CLK Cycle
6	—	CC	Data setup time	0.0	—	ns
7	—	CC	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	—	CC	Stop condition setup time	2	—	PER_CLK Cycle

1 I²C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).

2 PER_CLK is the SoC peripheral clock, which drives the I²C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Table 71. I²C output timing specifications — SCL and SDA[1,2,3,4]

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1	—	CC	Start condition hold time	6	—	PER_CLK Cycle[5]
2	—	CC	Clock low time	10	—	PER_CLK Cycle
3	—	CC	Bus free time between Start and Stop condition	4.7	—	μs
4	—	CC	Data hold time	7	—	PER_CLK Cycle
5	—	CC	Clock high time	10	—	PER_CLK Cycle
6	—	CC	Data setup time	2	—	PER_CLK Cycle
7	—	CC	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	—	CC	Stop condition setup time	10	—	PER_CLK Cycle

1 All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

2 Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.

3 Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.

4 Programming the IBFD register (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.

5 PER_CLK is the SoC peripheral clock, which drives the I²C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

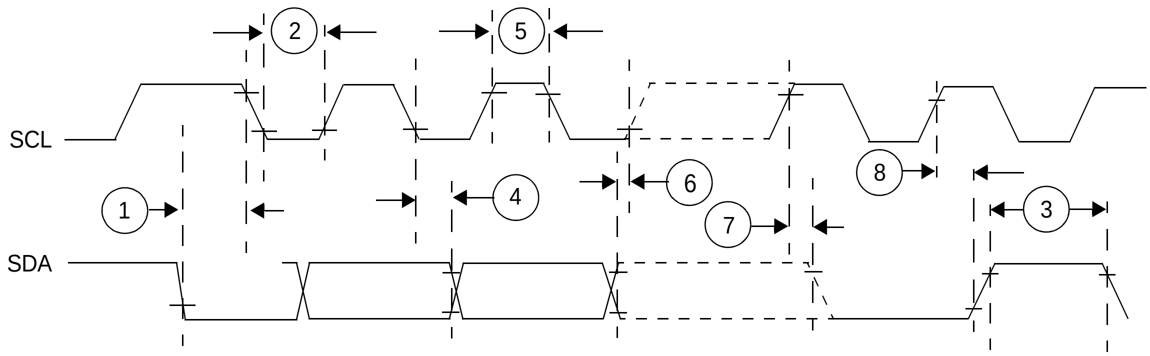


Figure 53. I²C input/output timing

3.16.9 GPIO delay timing

The GPIO delay timing specification is provided in the following table.

Table 72. GPIO delay timing

Symbol		Parameter	Value		Unit
			Min	Max	
IO_delay	CC	Delay from SIUL2 MSCR register bit update to pad function enable at the input of the I/O pad	5	25	ns

3.16.10 Package characteristics

The following table lists the case numbers for each available package for the device.

Table 73. Package case numbers

Package Type	Device Type	Case Outline Number
416TEPBGA	Production	98ARE10523D
416TEPBGA	Emulation	98ASA00493D
512TEPBGA	Production or Emulation	98ASA00262D

3.17 416 TEPBGA (production) case drawing

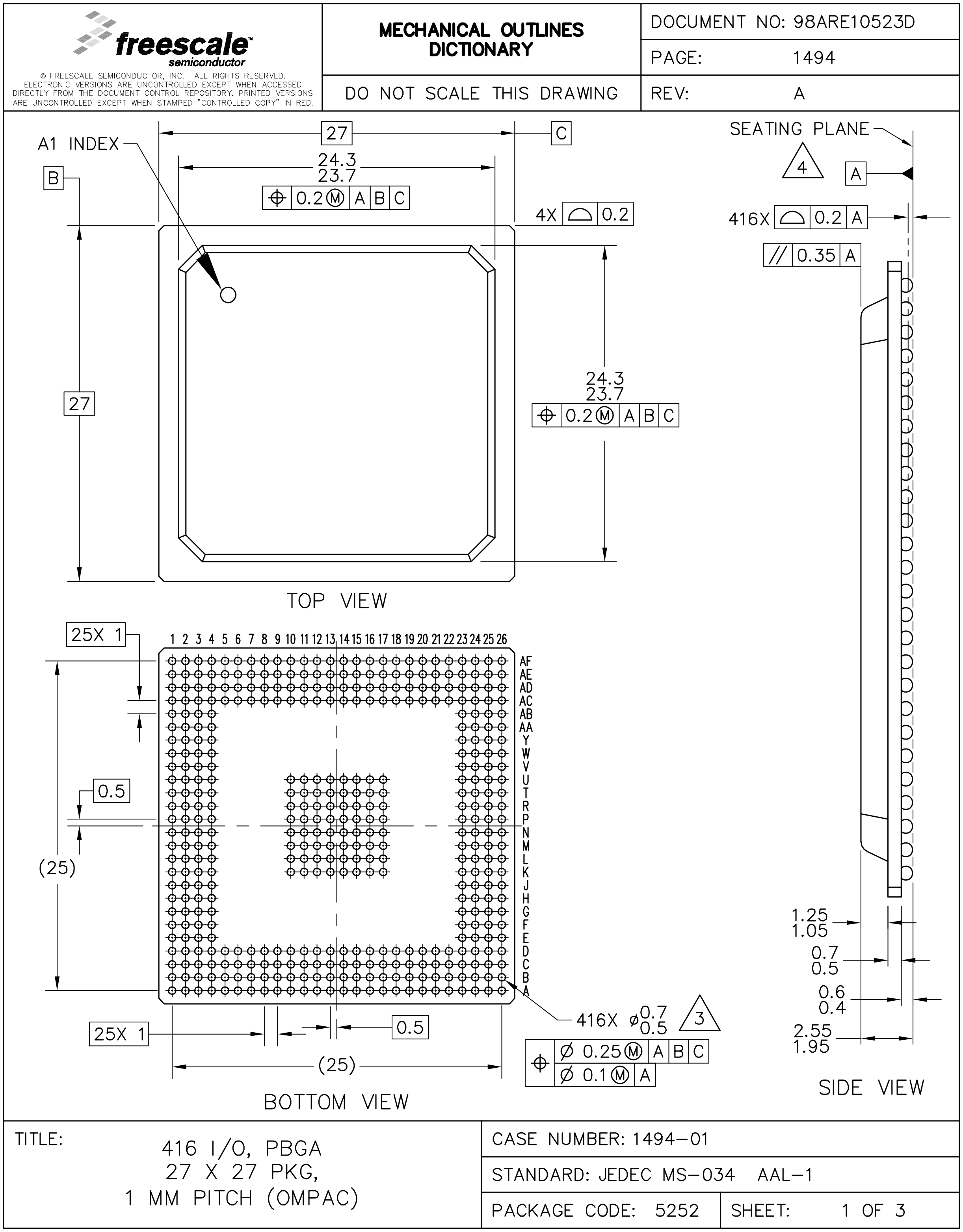


Figure 54. 416 TEPBGA (production) package mechanical drawing (Sheet 1 of 2)

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		PAGE: 1494
	DO NOT SCALE THIS DRAWING	REV: A

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

TITLE: 416 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	CASE NUMBER: 1494—01	
	STANDARD: JEDEC MS—034 AAL—1	
	PACKAGE CODE: 5252	SHEET: 2 OF 3

Figure 55. 416 TEPBGA (production) package mechanical drawing (Sheet 2 of 2)

3.18 416 TEPBGA (emulation) case drawing

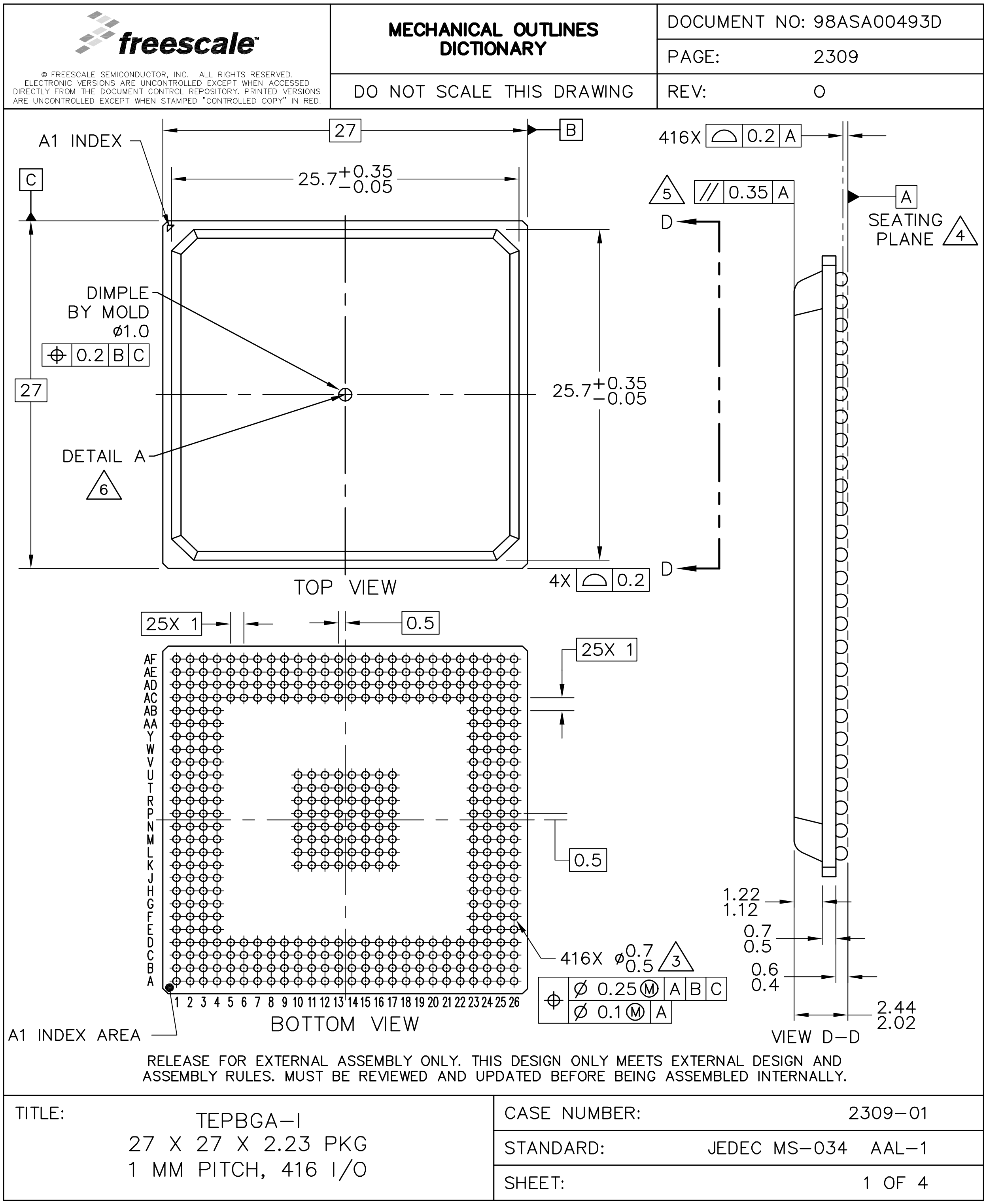

Figure 56. 416 TEPBGA (emulation) package mechanical drawing (Sheet 1 of 3)

freescale	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00493D
		PAGE: 2309
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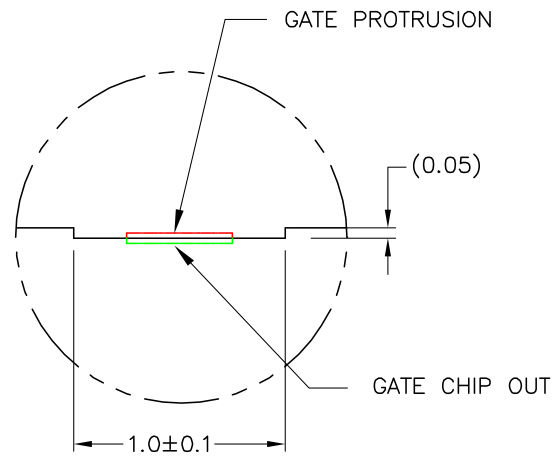

DETAIL A

TITLE: TEPBGA-I 27 X 27 X 2.23 PKG 1 MM PITCH, 416 I/O	CASE NUMBER: 2309-01
	STANDARD: JEDEC MS-034 AAL-1
	SHEET: 2

Figure 57. 416 TEPBGA (emulation) package mechanical drawing (Sheet 2 of 3)

freescale	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00493D
		PAGE: 2309
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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

6. GATE PROTRUSION HEIGHT OR CHIP OUT DEPTH: MAXIMUM 0.049MM.

TITLE: TEPBGA−I 27 X 27 X 2.23 PKG 1 MM PITCH, 416 I/O	CASE NUMBER:	2309−01
	STANDARD:	JEDEC MS−034 AAL−1
	SHEET:	3

Figure 58. 416 TEPBGA (emulation) package mechanical drawing (Sheet 3 of 3)

3.19 512 TEPBGA case drawing

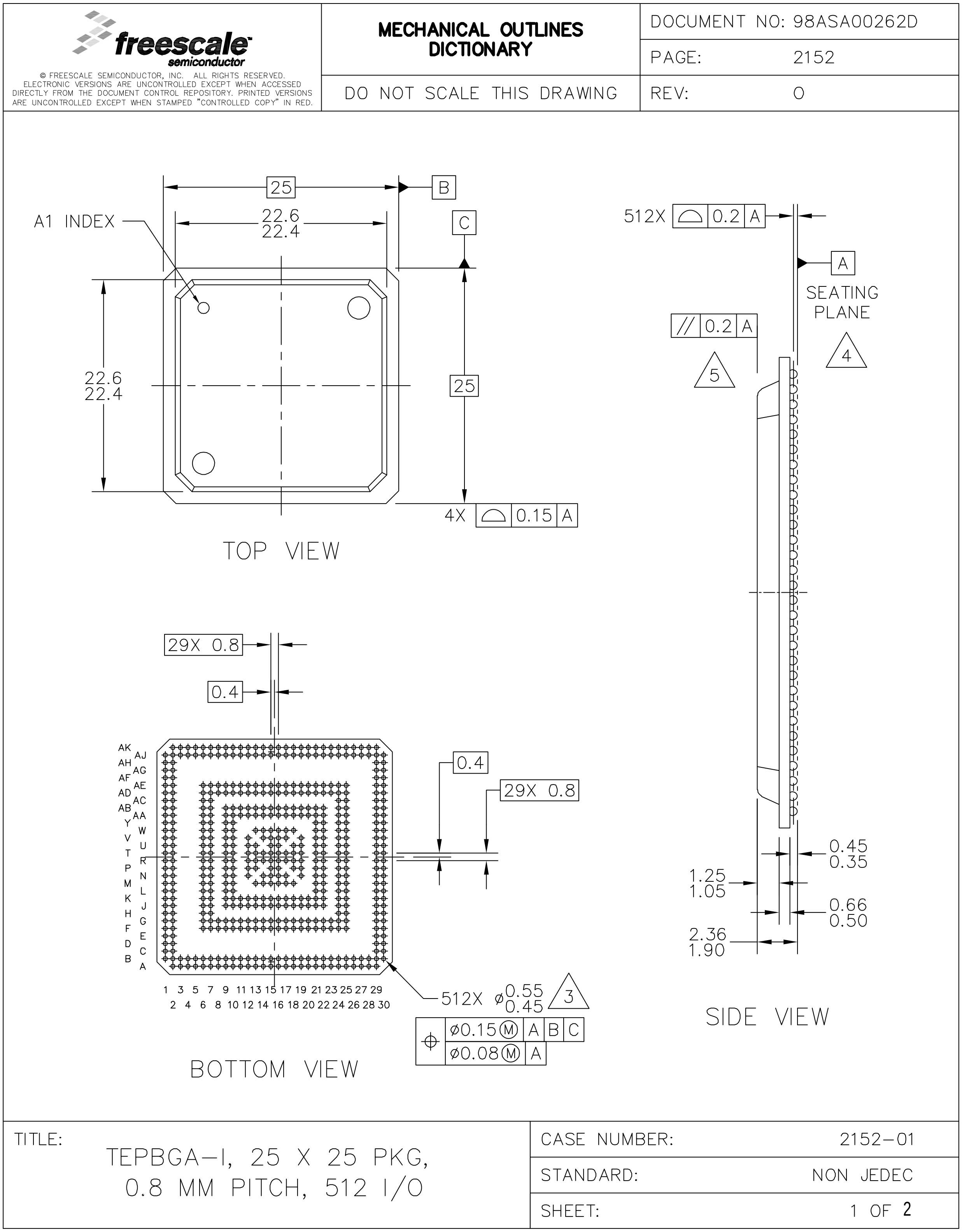


Figure 59. 512 TEPBGA package mechanical drawing (Sheet 1 of 2)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASA00262D
		PAGE: 2152
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: TEPBGA—I, 25 X 25 PKG, 0.8 MM PITCH, 512 I/O	CASE NUMBER: 2152—01
	STANDARD: NON JEDEC
	SHEET: 2

Figure 60. 512 TEPBGA package mechanical drawing (Sheet 2 of 2)

3.20 Thermal characteristics

The following tables describe the thermal characteristics of the device.

Table 74. Thermal characteristics

Symbol	Parameter	Conditions	416 Value	512 Value	Unit	Notes
$R_{\theta JA}$	Junction-to-Ambient, Natural Convection	Single Layer board (1s)	25	24.1	°C/W	1,2
		Four layer board (2s2p)	17.2	16.8		1,2,3
$R_{\theta JMA}$	Junction-to-Moving-Air, Ambient	@200 ft/min., single layer board (1s)	18.1	16.6	°C/W	1,3
		@200 ft/min., four layer board (2s2p)	13.4	12.4		1,3
$R_{\theta JB}$	Junction-to-board	—	8.6	8.8	°C/W	4
$R_{\theta JC}$	Junction-to-case	—	5.0	5.0	°C/W	5
Ψ_{JT}	Junction-to-package top	Natural convection	0.2	0.2	°C/W	6
Ψ_{JB}	Junction-to-package bottom/solder balls	Natural convection	3.5	3.0	°C/W	7

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[2] Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

[3] Per JEDEC JESD51-6 with the board horizontal.

[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

[7] Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

3.20.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \qquad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)
$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D) \quad \textit{Eqn. 2}$$

where:

T_B = board temperature for the package perimeter (^oC)
$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)
$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)
Ψ_{JT} = thermal characterization parameter ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

$$T_J = T_B + (\Psi_{JPB} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_T = thermocouple temperature on bottom of the package (^oC)
Ψ_{JT} = thermal characterization parameter ($^oC/W$)
P_D = power dissipation in the package (W)

4 Ordering information

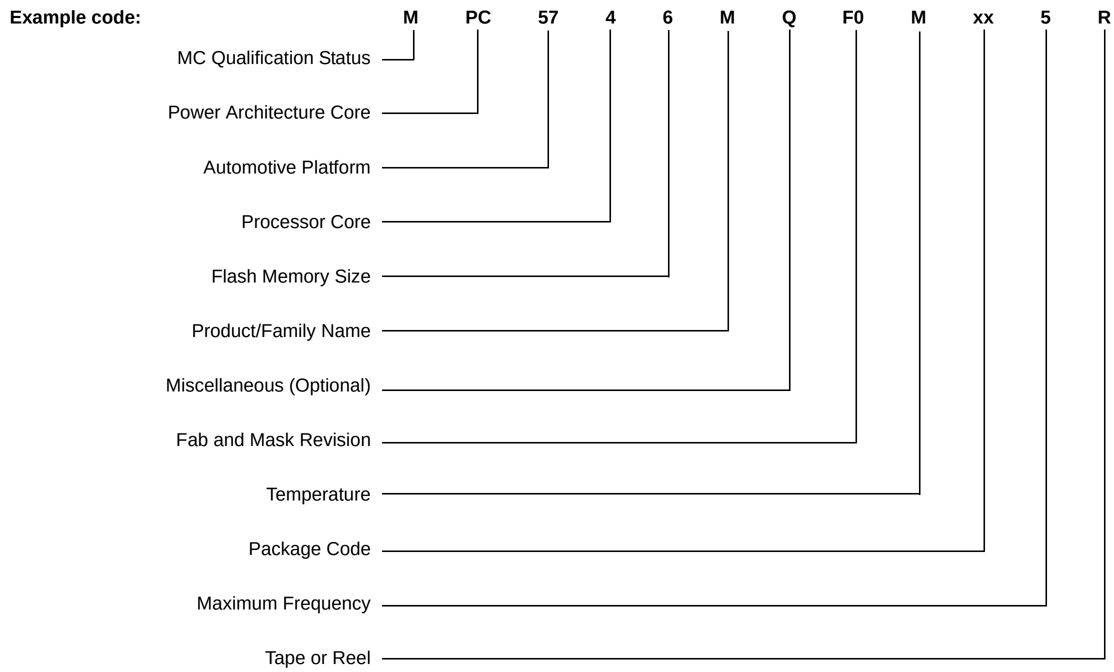
Table 75 shows the orderable part numbers for the MPC5777M series.

Table 75. Orderable part number summary

Part Number	Device Type[1,2]	Package
PPC5777MK0MVU8B	Sample	416 TEPBGA
PPC5777MK0MVA8B	Sample	512 TEPBGA
PPC5777M2K0MVU8B	Sample ED	416 TEPBGA
PPC5777M2K0MVA8B	Sample ED	512 TEPBGA
SPC5777MK0MVU8	Production PD	416 TEPBGA
SPC5777MK0MVU8R	Production PD	416 TEPBGA w/Tape and Reel
SPC5777MK0MVA8	Production PD	512 TEPBGA
SPC5777MK0MVA8R	Production PD	512 TEPBGA w/Tape and Reel

[1] “PD” refers to a production device, orderable in quantity

[2] “ED" refers to an emulation device, orderable in limited quantities. An emulation device (ED) is for use during system development only and is not to be used in production. An ED is a Production PD chip combined with a companion chip to form an Emulation and Debug Device (ED) and includes additional RAM memory and debug features. EDs are provided “as is" without warranty of any kind. In the event of a suspected ED failure, NXP agrees to exchange the suspected failing ED from the customer at no additional charge; however, NXP will not analyze ED returns.



Qualification Status
MPC = Full specification qualified
SPC = Mask specification qualified
PPC = Engineering samples

Automotive Platform
55 = PPC in 130 nm
56 = PPC in 90 nm
57 = PPC in 55 nm

Processor Core
0 = e200z0
1 = e200z1
2 = e200z2
3 = e200z3
4 = e200z4
5 = e200z6 without VLE
6 = e200z6
7 = e200z7

Miscellaneous
D = Dual Core
T = Triple Core
Q = Quad Core
S = Single Core
2 = Emulation Device

Fab and Mask Revision
F = ATMC
K = TSMC
0 = Revision

Flash Memory Size

	z0, z2	z4	z7
1	256 KB	1 MB	1 MB
2	384 KB	1.5 MB	1.5 MB
3	512 KB	2 MB	2 MB
4	768 KB	2.5 MB	3 MB
5	1 MB	3 MB	4 MB
6	1.5 MB	4 MB	6 MB
7	2 MB	5 MB	8 MB
8	2.5 MB	6 MB	12 MB
9	3 MB	8 MB	16 MB

Temperature Specification
C = –40 °C to 85 °C
V = –40 °C to 105 °C
M = –40 °C to 125 °C
K = –40 °C to 135 °C

Package Code
ZP = 416 PBGA SnPb
VA = 416 PBGA Pb-free
VA = 512 TEPBGA Pb-free
VU = 416 TEPBGA Pb-free
VF = 208 MAPBGA SnPb
VM = 208 MAPBGA Pb-free
ZQ = 324 PBGA SnPb
VZ = 324 PBGA Pb-free
LQ = 144 LQFP Pb-free
LU = 176 LQFP Pb-free
KU = 176 LQFP ep Pb-free
MP = 292 MAPBGA Pb-free
OU = 216 FQ (176 leads)

Maximum Frequency
0 = 64 MHz
1 = 80 MHz
2 = 120 MHz
3 = 150 MHz
4 = 160 MHz
5 = 200 MHz
8 = 300 MHz

Suffix
A = cut2.0 revision
T = Tape
R = Reel

Figure 61. Product code structure

5 Document revision history

Table 76 summarizes revisions to this document.

Table 76. Revision history

Revision	Date	Description of changes
1	12/2011	Initial release
2	4/2013	**Throughout**
		• Data sheet now includes both KGD (T_J≤165 °C) and non-KGD (T_J≤150 °C) specifications • The interfaces and components formerly including the name “DigRF” have been renamed to “LFAST.”
		Introduction
		• Changed on-chip general-purpose SRAM to 404 KB (was 384 KB) • Changed item describing Boot Assist Flash support to “Boot Assist Module (BAM) supports factory programming using serial bootload through ’UART Serial Boot Mode Protocol’. Physical interface (PHY) can be: UART/LIN, CAN, FlexRay” Table 1 (Family comparison): • Changed feature from “Zipwire/LFAST[7] bus” to “Zipwire (SIPI / LFAST[7]) Interprocessor Communication Interface” Figure 1 (Block diagram): • Changed SRAM from 320 to 340 KB • Changed figure to include “Triple INTC” • Added “LFAST Switch” block to Computational Shell • Added “Debug SIPI” block to the Peripheral Domain 50 MHz Concentrator Figure 2 (Periphery allocation): • Added PSI5_S_0 module • Changed “Peripheral Cluster A” to “Peripheral Cluster B” and “Peripheral Cluster B” to “Peripheral Cluster A” • Added PSI5_S_0 module
		Package pinouts and signal descriptions
		Figure 3 (292-ball BGA production device pinout (top view)) Figure 4 (292-ball BGA emulation device pinout (top view)) Figure 5 (512-ball BGA production device pinout (top view)) Figure 8 (512-ball BGA emulation device pinout (top view)): • Changed “VDD_HV_PMC_BYP” to “VDD_HV_IO_MAIN” Table 2 (Power supply and reference pins): • Removed $V_{DD\_HV\_PMC\_BYP}$ (PMC Voltage Supply Bypass Capacitor) row. Table 3 (System pins): • Clarification of TESTMODE pin definition: “TESTMODE pull-down is implemented to prevent the device from entering TESTMODE. It is recommended to connect the TESTMODE pin to VSS_HV_IO on the board. The value of the TESTMODE pin is latched at the negation of reset and has no affect afterward. The device will not exit reset with the TESTMODE pin asserted during power-up.” (Added detail regarding when TESTMODE pin value is latched and that device will not exit reset when pin is asserted during power-up)

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Package pinouts and signal descriptions (con't)**
		Table 4 (LVDS pin descriptions): • In SIPI/LFAST, Differential DSPI2, and Differential DSPI 5 groups, changed port pin "PF[7]" to "PD[7]" • Changed the polarity of the signal assigned to several port pins. For example, the signal for port pin PD[7] has been changed to "SIPI_RXP" (was SIPI_RXN) and "Interprocessor Bus LFAST, LVDS Receive Positive Terminal" (was "Interprocessor Bus LFAST, LVDS Receive Negative Terminal"). This change affects port pins PD[7], PF[13], PA[14], PD[6], PA[7], PA[8], PD[2], PD[3], PD[0], PD[1], PF[10], PF[9], PF[11], PF[12], PQ[8], PQ[9], PQ[10], PQ[11], PI[14], and PI[15]. • Added package ball locations
		Electrical characteristics—Miscellaneous
		Section 3, Electrical characteristics: • Thermal characteristics section has been moved to Package characteristics section. • Following note removed: "All parameter values in this document are tested with nominal supply voltage values (VDD_LV = 1.25 V, VDD_HV = 5.0 V ± 10%, VDD_HV_IO = 5.0 V ± 10% or 3.3 V ± 10%) and TA = –40 to 125 °C unless otherwise specified.". Operating conditions will appear elsewhere in the data sheet. • Added VDD_HV_IO_FLEX before VDD_HV_FLA in the second note on the page
		Electrical characteristics—Absolute maximum ratings
		Table 6 (Absolute maximum ratings): • I_{MAXD} specification now given by pad type (Medium, Strong, and Very Strong) • I_{MAXA} specification deleted. • New specification: I_{INJD} (Maximum DC injection current for digital pad) • New specification: I_{INJA} (Maximum DC injection current for analog pad) • New specification: I_{MAXSEG} (Maximum current per power segment) • New specification: V_{FERS} (Flash erase acceleration supply) • New specification: $V_{DD\_HV\_IO\_EBI}$ (External Bus Interface supply) • Changed "Emulation module supply" to "BD supply" in the VDD_LV_BD – BDD_LV row • Maximum junction temperature changed from 125 °C to 165 °C in cumulative time limits on voltage levels for V_{DD_LV} and $V_{DD\_LV\_BD}$ • Footnote added to V_{FERS}: V_{FERS} is a factory test supply pin that is used to reduce the erase time of the flash. It is only available in bare die devices. There is no V_{FERS} pin in the packaged devices. The V_{FERS} supply pad can be bonded to ground (V_{SS_HV}) to disable, or connected to 5.0 V ± 5% to use the flash erase acceleration feature. Pad can be left at 5 V ± 5% in normal operation. • Footnote added to V_{IN}: "The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations." • Footnote V_{DD_LV} changed: "1.32 – 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.288 V at maximum T_J = 165 °C" (was 1.275)

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—Operating conditions**
		Table 8 (Device operating conditions) • Changed VSTBY_BO minimum from 0.7V to 0.8V.
		Electrical characteristics—DC electrical specifications
		Table 10 (DC electrical specifications) • Replaced table; significant changes throughout, including parameter names, descriptions, and values.

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—I/O pad specification**
		Table 11 (I/O pad specification descriptions) • Revised “Very strong configuration” description to include EBI data bus. • Added “EBI configuration” row. • Changed “Input only pads” description to “These pads, which ensure low input leakage, are associated with the ADC channels” (was “These pads are associated with the ADC channels and 32 kHz low power external crystal oscillator providing low input leakage”) • Changed note following table to “Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin” (was “All pads can be configured in all configurations”) Table 12 (I/O input DC electrical characteristics) • New specification: $V_{DRFTTTL}$ (Input V_{IL}/V_{IH} temperature drift TTL) • New specification: $V_{DRFTAUT}$ (Input V_{IL}/V_{IH} temperature drift) • New specification: $V_{DRFTCMOS}$ (Input V_{IL}/V_{IH} temperature drift CMOS) • Conditions for V_{IHCMOS_H}, V_{IHCMOS}, V_{ILCMOS_H}, V_{ILCMOS}, $V_{HYSCMOS}$, $V_{DRFTCMOS}$ are now 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V (was 2.7 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.0 V < $V_{DD\_HV\_IO}$ < 5.5 V) • New specification: I_{LKG_MED} (Digital input leakage for MEDIUM pad) • Footnotes give formulas for approximation of the variation of the *minimum* value with supply of V_{IHAUT} and V_{HYSAUT} (previously stated formulas approximated *upper* value instead of minimum value). Changed formula for V_{IHAUT} to “0.69 x VDD_HV_IO” (was “0.69 supply”). Changed formula for V_{HYSAUT} to “0.11 x $V_{DD\_HV\_IO}$” (was “0.11 supply”). • Footnote gives formula for approximation of the variation of the *maximum* value with supply of V_{ILAUT} (previously stated formula approximated *upper* value instead of maximum value). Changed formula for V_{ILAUT} to “0.49 x $V_{DD\_HV\_IO}$” (was “0.49 supply”). • Added footnote: “In a 1 ms period, assuming stable voltage and a temperature variation of ±30°C, VIL/VIH shift is within ±50 mV.” • VHYSAUT conditions column: replaced dash with 4.5V < VDD_HV_IO < 5.5V • CIN row, changed GPIO input pins conditions Max value from “10” to 7pF and EBI input pins Max value from “8” to “7pF” Table 13 (I/O pull-up/pull-down DC electrical characteristics) • Significant revisions throughout this table, including new conditions for $\lvert I_{WPU} \rvert$ and $\lvert I_{WPD} \rvert$ • New specification: R_{WPU} (Weak pull-up resistance) • New specification: R_{WPD} (Weak pull-down resistance) • New figure: Figure 8 (Weak pull-up electrical characteristics definition) • New figure: Figure 18 (I/O output DC electrical characteristics definition)

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—I/O pad specification (con't)**
		Table 14 (WEAK configuration output buffer electrical characteristics) • R_{OH_W} (PMOS output impedance weak configuration) condition is now 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull I_{OH} < 0.5 mA (was 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V). Removed 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V condition. • R_{OL_W} (NMOS output impedance WEAK configuration) condition is now 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull I_{OL} < 0.5 mA (was 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V). Removed 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V condition. • t_{TR_W} (Transition time output pin WEAK configuration) conditions changed for C_L = 25 pF, C_L = 50 pF, C_L = 200 pF: 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V (was 4.0 V < VDD_HV_IO < 5.9 V) • Specification change: t_{TR_W}, C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V max value is 820 ns (was 1000) • Specification change: t_{TR_W}, C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 50 ns (was TBD) • Specification change: t_{TR_W}, C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 100 ns (was TBD) • Specification change: t_{TR_W}, C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 350 ns (was TBD) and max value is 1050 ns (was TBD) • Conditions column heading, added footnote: All VDD_HV_IO conditions for 4.5V to 5.9V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0 Table 15 (MEDIUM configuration output buffer electrical characteristics) • R_{OH_M} (PMOS output impedance MEDIUM configuration) condition is now 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull I_{OH} < 2 mA (was 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V). Removed 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V condition. • R_{OL_M} (NMOS output impedance MEDIUM configuration) condition is now 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull I_{OL} < 2 mA (was 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V). Removed 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V condition. • t_{TR_M} (Transition time output pin MEDIUM configuration) conditions changed for C_L = 25 pF, C_L = 50 pF, C_L = 200 pF: 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V (was 4.0 V < VDD_HV_IO < 5.9 V) • Specification change: t_{TR_M}, C_L = 200 pF, 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V max value is 200 ns (was 240) • Specification change: t_{TR_M}, C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 12 ns (was TBD) • Specification change: t_{TR_M}, C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 24 ns (was TBD) • Specification change: t_{TR_M}, C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 70 ns (was TBD) and max value is 300 ns (was TBD) • New specification: I_{DCMAX_M} (Maximum DC current) • New specification: $\|t_{SKEW\_M}\|$ (Difference between rise and fall time) • Formula given for transition time typical value changed to: t_{TR_M}(ns) = 5.6 ns+C_L(pF) x 1.11 ns/pF (when 0 pF < C_L < 50 pF) and t_{TR_M}(ns) = 13 ns+C_L(pF) x 0.96 ns/pF (when 50 pF < C_L < 200 pF) • Footnote added: R_{OX_M}(min) may decrease by 10% at T_J = 165 °C. • Footnote added: R_{OX_M}(max) may increase by 10% at T_J = 165 °C. • Conditions column heading, added footnote: All VDD_HV_IO conditions for 4.5V to 5.9V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—I/O pad specification (con't)**
		Table 16 (STRONG configuration output buffer electrical characteristics) • New specification: I_{DCMAX_S} (Maximum DC current) • Renamed: R_{OH_F} (PMOS output impedance STRONG configuration) is now R_{OH_S} • Renamed: R_{OL_F} (NMOS output impedance STRONG configuration) is now R_{OL_S} • Renamed: f_{MAX_M} (Output frequency STRONG configuration) is now f_{MAX_S} • R_{OH_S} condition is now 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull I_{OH} < 8 mA (was 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V). Removed 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V condition. • R_{OL_S} condition is now 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V, Push pull I_{OH} < 8 mA (was 4.0 V < $V_{DD\_HV\_IO}$ < 5.9 V). Removed 3.0 V < $V_{DD\_HV\_IO}$ < 4.0 V condition. • t_{TR_S} conditions changed for C_L = 25 pF, C_L = 50 pF, C_L = 200 pF: 4.5 V < $V_{DD\_HV\_IO}$ < 5.9 V (was 4.0 V < VDD_HV_IO < 5.9 V) • Specification change: f_{MAX_S}, C_L = 200 pF max value is 5 MHz (was "—") • Specification change: t_{TR_S}, C_L = 25 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 4 ns (was TBD) and max value is 15 ns (was TBD) • Specification change: t_{TR_S}, C_L = 50 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 6 ns (was TBD) and max value is 27 ns (was TBD) • Specification change: t_{TR_S}, C_L = 200 pF, 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V min value is 20 ns (was TBD) and max value is 83 ns (was TBD) • Footnote added: R_{OX_S}(min) may decrease by 10% at T_J = 165 °C. • Footnote added: R_{OX_S}(max) may increase by 10% at T_J = 165 °C. • Conditions column heading, added footnote: All VDD_HV_IO conditions for 4.5V to 5.9V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0 Table 17 (VERY STRONG configuration output buffer electrical characteristics) • New specification: I_{DCMAX_M} (Maximum DC current) • New condition added to $t_{TR\_V:}$ $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, C_L = 200 pF • Footnote added: R_{OX_V}(min) may decrease by 10% at T_J = 165 °C. • Footnote added: R_{OX_V}(max) may increase by 10% at T_J = 165 °C. • Conditions column heading, added footnote: All VDD_HV_IO conditions for 4.5V to 5.9V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0V to 3.6V are valid for VSIO[VSIO_xx] = 0 Table 18 (EBI pad output electrical specification) • Replaced this table "EBI output driver electrical characteristics" with new table "EBI pad electrical specification"
		Electrical characteristics—I/O pad current specification
		New section
		Electrical characteristics—Reset pad (PORST, ESR0) electrical characteristics
		Section 3.8, Reset pad (PORST, ESR0) electrical characteristics: • Added note on $\overline{PORST}$ and active control Figure 11 (Noise filtering on reset signal): • Replaced; significant detail added • Clarification: $V_{\overline{ESR0}}$ is also described by $V_{\overline{PORST}}$ behavior shown in illustration. • Figure prefaced with more detailed $\overline{PORST}$ description.

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—Reset pad (PORST, ESR0) electrical characteristics (con't)**
		Table 20 (Reset electrical characteristics) • New specification: W_{FNMI} (ESR1 input filtered pulse) • New specification: W_{NFNMI} (ESR1 input not filtered pulse) • New specification: V_{DD_POR} (Minimum supply for strong pull-down activation) • I_{OL_R} condition changed ($V_{DD\_HV\_IO}$ = 1.0 V is now $V_{DD\_HV\_IO} = V_{DD\_POR}$, $V_{DD\_HV\_IO}$ = 4.0 V is now 3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V, and V_{OL} = 0.35*$V_{DD\_HV\_IO}$ is now V_{OL} > 0.9 V) • Specification change: I_{OL_R} (3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V, V_{OL} > 0.9 V) min value is 11 mA (was 15) • Added footnote: An external 4.7 KΩ pull-up resistor is recommended to be used with the PORST and ESR0 pins for fast negation of the signals. • Added footnote: I_{OL_R} applies to both PORST and ESR0: Strong pull-down is active on PHASE0 for PORST. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for ESR0. • Added note on reset signal slew rate restrictions
		Electrical characteristics—Oscillator and FMPLL
		Section 3.12, Oscillator and FMPLL Table 21 (PLL0 electrical characteristics) • New specification: $f_{PLL0PHI0}$ (PLL0 output frequency) • Specification change: $t_{PLL0LOCK}$ (PLL0 lock time) maximum is 100 µs (was 100–110 µs) • $\Delta_{PLL0LTJ}$ specification parameter and conditions change: "PLL0 output long term jitter, f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz" (was "PLL0 output long term jitter, f_{PLL0IN} = 20 MHz (resonator)"). Conditions significantly revised. • Revised footnote: "VDD_LV noise due to application in the range V_{DD_LV} = 1.25 V ±5% with frequency below PLL bandwidth (40 KHz) will be filtered" (was "1.25 V ±5% application noise below 40kHz at VDD_LV pin") • Removed "F" from "FXOSC" in footnote 1 Table 22 (PLL1 electrical characteristics) • Specification change: $f_{PLL1PHI}$ (PLL1 output clock PHI) is now $f_{PLL1PHI0}$ (PLL1 output clock PHI0) • Specification change: $f_{PLL1PHI0}$ (PLL1 output clock PHI0) max is 200 MHz (was 625 MHz) • fPLL1PHI parameter, Max column, changed 200MHz to 300MHz. • Removed "F" from "FXOSC" in footnote 1

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—Oscillator and FMPLL (con't)**
		Table 23 (External Oscillator electrical specifications): • New specification: V_{HYS} (Comparator Hysteresis) • New specification: V_{EXTAL} (Oscillation Amplitude on the EXTAL pin after startup) • Specification change: f_{XTAL} range values changed: f_{XTAL} ranges are 4–8 MHz, >8–20 MHz, and >20–40 MHz (previously stated as 4–8 MHz, 8–16 MHz, and 20–40 MHz • Specification change t_{cst} (Crystal start-up time) is now specified by temperature range • Specification change: V_{IHEXT} specified at V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$ (previously specified at V_{DDOSC} = 3.0 V and V_{DDOSC} = 5.5 V) • Specification change: V_{ILEXT} specified at V_{REF} = 0.28 * $V_{DD\_HV\_IO\_JTAG}$ (previously specified at V_{DDOSC} = 3.0 V and V_{DDOSC} = 5.5 V) • Specification change: C_{S_EXTAL} values specified by package (was previously based on selected load capacitance value) • Specification change: C_{S_XTAL} values specified by package (was previously based on selected load capacitance value) • Specification change: g_m (Oscillator Transconductance) is now specified by temperature and frequency range conditions (was previously specified without conditions) • Footnote added: "All oscillator specifications are valid for $V_{DD\_HV\_IO\_JTAG}$ = 3.0 V – 5.5 V." • Footnote added to C_{S_EXTAL}, C_{S_XTAL} to refer to crystal manufacturer's specifications for load capacitance values. • Footnote added: "Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions." • Footnote added: "I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2–3 mA range and is dependent on the load and series resistance of the crystal." • V_{ILEXT} parameter, changed "External Reference" to "External Clock Input" • V_{ILEXT} parameter, added footnote: This parameter is guaranteed by design rather than 100% tested. Table 24 (Selectable load capacitance): • Changed footnote 2 from "Values in this table do not include 8 pF routing and ESD structure on die and package trace capacitance." to "Values in this table do not include the die and package capacitances given by Cs_xtal/Cs_extal in Table 23 (External Oscillator electrical specifications)."
		Electrical characteristics—ADC specifications
		Section 3.10.1, ADC input description Table 26 (ADC pin specification) • I_{LK_IN} specification change: removed T_A = 125 °C row from (T_A = 125 °C) • I_{LK_INUD}, I_{LK_INUSD}, I_{LK_INREF}, and I_{LK_INOUT} specification changes to parameters, conditions, and values. • Specification change: I_{INJ} min value is –3 mA (was –1) • Specification change: C_S max value is 8.5 pF (was 7) • Specification change: R_{SWn} max value for SARn channels is 1.1 kΩ (was 0.6)

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—ADC specifications (con't)**
		Section 3.10.1, ADC input description Table 26 (ADC pin specification): • Specification change: R_{SWn} max value for SARB channels is 1.7 kΩ (was 1.2) • Specification change: R_{CMSW} max value is 2.6 kΩ (was 2) • Removed V_{REF_BG} specification • Added $V_{REF\_BG\_LR}$ and $V_{REF\_BG\_TC}$ specifications • Added footnote: Specifications in this table apply to both packaged parts and Known Good Die (KGD) parts, except where noted. • Added footnote: The temperature coefficient and line regulation specifications are used to calculate the reference voltage drift at an operating point within the specified voltage and temperature operating conditions. • Parameter I_{LK_INOUT} description column, changed MEDIUM output buffer with GPIO output buffer. Table 27 (SARn ADC electrical specification) • Replaced table Section 3.13.3, S/D ADC electrical specification • Revised sentence to indicate that the ADCs are 14-bit (was 16-bit) Table 28 (SDn ADC electrical specification) • New specification: $f_{PASSBAND}$ (Pass band) • Removed V_{DD} and V_{SS} specifications • Removed f_{IN} specification • Throughout table, appended _D to change to $V_{DD\_HV\_ADV\_D}$ (was $V_{DD\_HV\_ADV}$), $V_{SS\_HV\_ADV\_D}$ (was $V_{SS\_HV\_ADV}$), $V_{DD\_HV\_ADR\_D}$ (was $V_{DD\_HV\_ADR}$), and $V_{SS\_HV\_ADR\_D}$ (was $V_{SS\_HV\_ADR}$). • V_{IN_PK2PK} (Input range peak to peak $V_{IN\_PK2PK}= V_{INP} – V_{INM}$): single ended specification extended to include multiple conditions • Multiple condition changes for the $\|\delta_{GAIN}\|$ and $SNR_{DIFF150}$ parameters • $\delta_{GAIN:}$ changed maximum value for Before calibration condition to "1.5 %" (was 1 %). • SFDR conditions revised to include different GAIN settings • Specification change: δV_{BIAS} min value is –2.5% (was –10) and the max value is +2.5% (was +10) • Significant revisions to footnotes, including one added to voltage range conditions in all SNR specs: "In the range 3.6 V< $V_{DD\_HV\_ADV}$<4.0 V and <3.0 V<$V_{DD\_HV\_ADR\_D}$<4.0 V, SNR parameter degrades by 9 dB" • fADCD_M, changed "S/D clock 3(4)" to "S/D Modulator Input Clock" and replaced "—" with "4" in Min column • fADCD_S changed "conversion rate'" to "output conversion rate" • Changed SNR specifications Unit column from "dB" to "dBFS" • Changed SFDR specification Unit column from "dB" to "dBc" • Add to footnote: Input impedance is calculated in megaohms by the formula 25.6/(Gain Fadcd_m) • Changed Group delay, OSR = 75, Max value from "546" to "596" • Added new specifications: $SINAD_{DIFF150}$, $SINAD_{DIFF333}$, $SINAD_{SE150}$, $THD_{DIFF150}$, $THD_{DIFF333}$, THD_{SE150}
		Electrical characteristics—Temperature sensor specifications
		Table 29 (Temperature sensor electrical characteristics) • T_{SENS}, T_{ACC}, and I_{TEMP_SENS} added to Symbol column. • Condition change for T_{ACC} (Accuracy): added 150 °C and 165 °C conditions • Specification change: T_{ACC} min value for T_J < 165°C is 7 °C (was –3) and max value is 7 °C (was 3) • Specification change: I_{TEMP_SENS} max value is 700 µA (was 600).

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—LFAST electrical specifications**
		Formerly named “DigRF interface electrical characteristics”; renamed to “LVDS Fast Asynchronous Serial Transmission (LFAST) pad electrical characteristics. The change from “DigRF” to “LFAST” applies throughout. Figure 16 (LFAST and MSC/DSPI LVDS timing definition). Figure updated. Section Table 30., LVDS pad startup and receiver electrical characteristics, • Specification change: added I_{LVDS_BIAS} • TRANSMITTER parameters moved to separate table: V_{OS_DRF} (Common mode voltage), $\|D_{VOD\_DRF}\|$ (Differential output voltage swing (terminated)), t_{TR_DRF} (Rise/Fall time (10%–90% of swing)), R_{OUT_DRF} (Terminating resistance), C_{OUT_DRF} (Capacitance) • Receiver requirement V_{ICOM_DRF} renamed to V_{ICOM} • Receiver requirement $\|\Delta_{VI\_DRF\|}$ renamed to $\|\Delta_{VI}\|$ • Receiver specification V_{HYS_DRF} renamed to V_{HYS} • Receiver specification R_{IN_DRF} renamed to R_{IN} • Receiver specification C_{IN_DRF} renamed to C_{IN} • Receiver specification L_{IN_DRF} deleted • Extensive changes throughout table footnotes. Table 31 (LFAST transmitter electrical characteristics,): Differential output voltage swing parameter: • Removed the delta symbol from |VOD| • Changed Min = 100, Typ = 171, Max = 285. removed the “+/-” from each value. Rise/Fall time parameter: • Changed “(10%–90% of swing)” to (absolute value of the differential output voltage swing Table 32 (MSC/DSPI LVDS transmitter electrical characteristics ,): Differential output voltage swing parameter: • Removed the delta symbol from |VOD| • Changed Min +/- 150 to 150 • Changed Typ +/- 200 to 214 • Changed Max +/- 400 to 400 Rise/Fall time parameter: • Changed “(10%–90% of swing)” to (absolute value of the differential output voltage swing) Table 33 (LFAST PLL electrical characteristics) • Changed footnote 2, from “320” to “640” MHz frequency Table 34 (Aurora LVDS electrical characteristics,) • Extensive changes throughout table

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—Power management: PMC, POR/LVD, sequencing**
		Table 40 (PMC operating conditions and external regulators supply voltage) • Specification change: $V_{DD\_HV\_PMC,}$ Reduced internal regulator output capacity max value is 3.5 V (was 5.5) • Specification change: $V_{DD\_HV\_PMC}$, Monitoring activity only min value is 2.7 V (was 3.0) and max value is 3.15 V (was 5.5) Section 3.14.2, Power management integration • Entire section replaced Table 36 (Flash power supply): • New Section 3.14.4, Device voltage monitoring • Added Figure 24 (Voltage monitor threshold definition) Table 37 (Voltage monitor electrical characteristics) • VPORUP_LV Added footnote2, "Hysteresis is only true with the High voltage Supplies for the I/O Main and the ADC are connected together. (There is actually around 1V of Hysteresis using these two supplies.)" • New specification: V_{POR240} (HV supply power-on reset voltage monitoring) • New specification: $t_{VDASSERT}$ (Voltage detector threshold crossing assertion) • New specification: $t_{VDRELEASE}$ (Voltage detector threshold crossing deassertion) • Specification change: V_{PORUP_LV}, Rising voltage max value is 1180 mV (was 1170) • Specification change: V_{PORUP_LV} Falling voltage max value is 1100 mV • Significant changes to footnotes for this table. • V_{LVD096} (LV internal supply low voltage monitoring). Footnote added: "LV internal supply levels are measured on device internal supply grid after internal voltage drop." • V_{LVD108} (LV internal supply low voltage monitoring). Footnote added: "LV internal supply levels are measured on device internal supply grid after internal voltage drop." • Specification change: V_{LVD112} max value is 1180 mV (was 1190) • Specification change: VHVD140 is 1440 mV (was 1420) • Specification change: V_{PORUP_HV} Rising voltage max value is 4480 mV (was 4200); min value is 4040. in addition, the Falling voltage min value is 2830 mV (was 2700) and the max value of 3210 mV was added • Specification change: V_{LVD270} max value is 2950 mV (was 2980) • Specification change: V_{LVD400} max value is 4410 mV (was 4400); min value added for Rising voltage. Also, changed min value for Falling voltage is 3970 mV (was 3980) Specification change: V_{HVD600} min value is 5560 mV (was 5520) and max value is 6000 mV (was 5960) Table 39 (Functional terminals state during power-up and reset) • Corrected ESR1 RESET pad state to "Weak pull-up" (was "pull-down") and DEFAULT pad state to "Weak pull-up" (was "pull-down") • Corrected TMS RESET pad state to "Weak pull-up" (was "pull-down") and DEFAULT pad state to "Weak pull-up" (was "pull-down") • Changed TDO RESET pad state to "High impedance" (was "Weak pull-up") • Revised TESTMODE footnote: "An internal pull-down is implemented on the TESTMODE pin to prevent the device from entering test mode if the package TESTMODE pin is not connected. It is recommended to connect the TESTMODE pin to VSS_HV_IO on the board for maximum robustness, but not required. The value of TESTMODE is latched at the negation of reset and has no affect afterward. The device will not exit functional reset with the TESTMODE pin asserted during power-up. The TESTMODE pin can be connected externally directly to ground without any other components."

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—Flash memory electrical characteristics**
		Section 3.15, Flash memory electrical characteristics • This section completely revised.
		Electrical characteristics—AC specifications—Debug and Calibration
		Table 46 (JTAG pin AC electrical characteristics,): • Specification change: t_{JCYC} (TCK cycle time) now consists of a single specification—minimum value is 100 ns. Footnotes from previous entries have been removed. • Specification change: t_{TDOHZ} (TCK low to TDO high impedance) is now 15 ns (was 16) • Classification change: All specifications are “D” (were “P” and “C”) Table 47 (Nexus debug port timing) • New specification: t_{EVTIPW} (EVTI pulse width) • New specification: t_{EVTOPW} (EVTO pulse width) • Clarification: footnote added to T_{CYC}, defining it as the system clock period • Specification change: TDO propagation delay from falling edge of TCK max is 16 ns (was 12.5 ns) • Specification change: TCK cycle time is min value is 2 t_{CYC} (was 4) • Specification change: Absolute minimum TCK cycle time min value is 40 ns (was 25) • Specification change: TDI Data Hold Time min value is 5 ns (was 17.5) • Specification change: TMS Data Hold Time min value is 5 ns (was 17.5) • TDO propagation delay from falling edge of TCK max value is 16 ns (was 12.5) • Specification change: t_{TCYC} (absolute minimum TCK cycle time) now consists of two specifications—one with TDO sampled on posedge of TCK and one sampled with TDO sampled on negedge of TCK. Table 48 (Aurora LVDS interface timing specifications) • Specification change: Data rate typ. value is undefined (was 1200 Mbps) • Specification change: Data rate max. value is 1250 Mbps (was “Typ+1%”) Table 49 (Aurora debug port timing) • Specification change: t_{REFCLK} (Reference clock frequency) max value is 1250 MHz (was 1200) • Specification change: OUI (Aurora lane unit interval) is now specified by data rate • Characteristic vs. Requirement change: J_D (Transmit lane deterministic jitter) is “SR” (was “CC”) • Characteristic vs. Requirement change: J_T (Transmit lane total jitter) is “SR” (was “CC”)
		Electrical characteristics—AC specifications—DSPI
		Section 3.19.2, DSPI timing with CMOS and LVDS pads: Substantive changes to entire section, including reclassification of content as: • Table 51 (DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0, CPHA = 0 or 1) • Table 52 (DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1) • Table 54 (DSPI LVDS slave timing – full duplex – modified transfer format (MTFE = 0/1)) • Table 55 (DSPI LVDS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock,) • Table 56 (DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock,)

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—AC specifications—Fast Ethernet Controller (FEC)**
		Section 3.16.3, “FEC timing Table 58 (MII receive signal timing) • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 59 (MII transmit signal timing) • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) • Footnote added to max and min values columns: “Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.” Table 60 (MII async inputs signal timing) • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 61 (MII serial management channel timing): • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 62 (RMII receive signal timing): • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 63 (RMII transmit signal timing,): • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) • Specification change: REF_CLK to TXD[1:0], TX_EN valid max value is 16 ns (was 14) • Added footnote 2 to value column “Output parameters are valid for CL = 25 pF, where CL is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.”
		Electrical characteristics—AC specifications—FlexRay
		Section 3.16.4, FlexRay timing Table 64 (TxEN output characteristics): • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design) Table 65 (TxD output characteristics’): • $\Sigma t_{TR20-80}$ specification for $V_{DD\_HV\_IO}$ = 5.0 V ± 10%, Transmission line Z = 50 ohms, t_{delay} = 1 ns, C_L = 10 pF, moved from Table 17 (VERY STRONG configuration output buffer electrical characteristics) • $\Sigma t_{TR20-80}$ specification combined with $dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$ specification. Footnotes added for conditions. 3.3V specification added. • Footnote added: “Specifications valid according to FlexRay EPL 3.0.1 standard with 20%-80% levels and a 10pF load at the end of a 50ohm, 1ns stripline. Please refer to the Very Strong I/O pad specifications.“ • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design)

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Electrical characteristics—AC specifications—FlexRay (con't)**
		Table 66 (RxD input characteristics): • New specification: dCCRxAsymAccept15 (Acceptance of asymmetry at receiving CC with 15 pF load) • New specification: dCCRxAsymAccept25 (Acceptance of asymmetry at receiving CC with 25 pF load) • Column added: SR/CC (system requirement or controller characteristic) • Column added: Classification (parameters are guaranteed by design)
		Electrical characteristics—AC specifications—PSI5
		Section 3.19.6, PSI5 timing Table 67 (PSI5 timing): • Specification description for t_{MSG_DLY} changed to, "Delay from last bit of frame (CRC0) to assertion of new message received interrupt" (was, "Delay from last bit of frame (end of idle time) ...") • Specification description for t_{MSG_JIT} changed to, "Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt" (was, "Delay from last bit of frame (end of idle time) ...") • Maximum value for t_{SYNC_JIT} changed to ±(1 PSI5_1µs_CLK + 1 PBRIDGEn_CLK); was 1 cycle • Footnote 2 ("Measured in PSI5 1 MHz clock cycles (PSI5_1us_CLK on the device).") on the unit for t_{SYNC_JIT} deleted • Classification change: t_{MSG_DLY} (Delay from last bit of frame (CRC0) to assertion of new message received interrupt) is "D" (was "C") • Classification change: t_{SYNC_DLY} (Delay from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin) is "D" (was "C") • Classification change: t_{MSG_JIT} (Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt) is "D" (was "C") • Classification change: t_{SYNC_JIT} (Delay jitter from internal sync pulse to sync pulse trigger at the SDOUT_PSI5_n pin) is "D" (was "C")
		Electrical characteristics—AC specifications—UART
		Section 3.18.7, UART timing • New
		Electrical characteristics—AC specifications—EBI
		Section 3.16.7, External Bus Interface (EBI) Timing: • New
		Package characteristics
		• 292 MAPBGA case drawing Rev. A included. • 416 TEPBGA case drawing Rev. 0 included.
		Electrical characteristics—Thermal Characteristics
		Table 74 (Thermal characteristics) • This table consolidates what were formerly separate thermal specifications tables for each package. All values have been updated.

Table 76. Revision history (continued)

Revision	Date	Description of changes
2	4/2013	**Ordering Information**
		Section 4, Ordering information: • New
3	3/2014	**Throughout**
		• Changed document ID to “MPC5777M.” • Updated the “e200_z720n3” cores to “e200_z710n3” and the “e200_z719” core to “e200_z709.” • Removed references to the 292 MAPBGA and LFBGA292 packages. • Editorial (non-technical) changes and improvements. • Removed references to KGD and 165^{o}C ratings.
		Introduction
		Table 1 (Family comparison): • SPC5744K column, ADC (SD) feature, changed “3” to “2”. • MPC5777M column, removed 292 MAPBGA. • Changed feature from “SIPI/LFAST[7] bus” to “Zipwire® (SIPI / LFAST[7]) Interprocessor Communication Interface”. • Removed “To be confirmed for final silicon” footnote from Local RAM row for SPC5744K. • Removed “Only on the I/O processor core” footnote from LSP row for all devices. • Changed System SRAM for MPC5777M to “404 KB” (was 384 KB). • Changed Flash memory for MPC5777M to “8640 KB” (was 7.9 MB). • Changed DMA Nexus Class for SPC5744K, MPC5746M, and MPC5777M to “3+” (was 3). • Changed GTM RAM for MPC5777M to “58 KB” (was 52 KB). • Changed Interrupt Controller entry for MPC5777M to “727 sources” (was 930 sources). • Removed “Integrated switch mode voltage regulator” row. • Removed “Degraded performance below 4.0 V” footnote from 5 V value in External power supplies row. Figure 1 (Block diagram): • Updated the “e200_z720n3” cores to “e200_z710n3” and the “e200_z719” core to “e200_z709”. Section 1.5, Feature overview • Changed item describing main CPUs to “single issue” (was “dual issue). • Changed item describing on-chip flash memory to “8640 KB” (was “8528 KB”). • Removed FlexRay as an option for BAM serial port.

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Package pinouts and signal descriptions**
		Section 2.1, Package pinouts: • Removed “292” from the first sentence. • Removed figure “292-ball BGA production device pinout (top view)” and figure “292-ball BGA production device pinout (bottom view)”. Table 2 (Power supply and reference pins) and Table 3 (System pins): • Removed the “292PD” and 292ED” BGA ball columns. • V_{SS_LV}: Added K13 and K14 for 416PD/416ED. Added M15 and M16 for 512PD/512ED. • $V_{DD\_LV\_BD}$: R1/R4 now applies only to 416ED (416PD changed to “—”). M13/N12 now applies only to 512ED (512PD changed to “—”). • Removed $V_{DD\_HV\_OSC}$ row. • Changed $V_{DD\_HV\_JTAG}$ Description to "JTAG/Oscillator power supply." • V_{DDSTBY}: removed "Input" from description. • Significantly revised $V_{SS\_HV\_ADV\_S}$, $V_{DD\_HV\_ADV\_S}$, $V_{SS\_HV\_ADV\_D}$, and $V_{DD\_HV\_ADV\_D}$ rows. Added rows for $V_{SS\_HV\_ADR\_S}$, $V_{DD\_HV\_ADR\_S}$, $V_{SS\_HV\_ADR\_D}$, $V_{DD\_HV\_ADR\_D}$. Table 4 (LVDS pin descriptions): • Changed title to “LVDS pin descriptions” (was “LVDSM”). • Removed the “292 PD, 292 ED” BGA ball column. • In the BGA ball (416 PD,416 ED) column, added ball locations. • In the BGA ball (512 PD, 512 ED) column, added ball locations. • Changed SIPI_TXP to P25 for 512BGA (was T25). • DSPI 4: Changed SCK_N to G17 for 512BGA (was G18). • DSPI 2: Changed SIN_P to G23 for 416BGA (was D17). • DSPI 5: For SCK_P, changed PI[15] to PF[10], G26 to J24, and P22 to W24. • DSPI 5: For SCK_N, changed PI[15] to PF[9], J23 to K23, and R22 to W25. • Added another pair of SIN_P/SIN_N rows for DSPI_5.
		Electrical characteristics—Absolute maximum ratings
		Section 3.1, Introduction: • Added $V_{DD\_HV\_IO\_FLEXE}$ and $V_{DD\_HV\_IO\_EBI}$ to list in supply pins note. Table 7 (Parameter classifications): • Changed Tag description for C classification to “Parameters are guaranteed. . .” (was “Those parameters are achieved. . .” • Changed Tag description for T classification to “Parameters are guaranteed. . .” (was “Those parameters are achieved. . .” Table 6 (Absolute maximum ratings): • Changed V_{SS} to V_{SS_HV}. • Removed “$V_{SS} – V_{SS\_HV\_ADV}$” parameter row. • Removed V_{FERS} row. • Removed “VFERS is a factory test supply pin . . .” footnote. • $V_{SS\_HV\_ADR}$: Added "Reference to V_{SS_HV}" to Conditions field. • Removed V_{SS}–$V_{SS\_HV\_ADR\_D}$ and V_{SS}–$V_{SS\_HV\_ADR\_S}$ rows. • In $V_{DD\_HV\_IO}$ footnote, added $V_{DD\_HV\_IO\_JTAG}$ to list of power supplies to which $V_{DD\_HV\_IO}$ applies. • In ADC grounds footnote, removed $V_{SS\_HV\_ADV\_D2}$. • In ADC supplies footnote, changed $V_{DD\_HV\_ADV}$ to $V_{DD\_HV\_ADV\_S}$. • In ADC low and high references footnote, removed $V_{SS\_HV\_ADR\_D2}$ and $V_{DD\_HV\_ADR\_D2}$. • In ADC supplies footnote, removed $V_{DD\_HV\_ADV\_D2}$. Table 7 (ESD ratings,): • Changed ESD for Human Body Model (HBM) parameter classification to “T” (was SR)

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—Electromagnetic Compatibility (EMC)**
		• Removed section.
		Electrical characteristics—Operating conditions
		Table 8 (Device operating conditions): • V_{DDSTBY} added new footnote: The VDDSTBY pin should be connected to ground in the application when the standby RAM feature is not used.' • Added “Vin” specification, Min = 0V, Max = 5.5 V. • $V_{DD\_HV\_ADV}$ changed Min value from 3.6 V to 3.7 V. • $V_{DD\_HV\_IO\_MAIN}$, LVD400/HVD 600 disabled and LVD360/HVD600 disabled conditions: changed max to “5.5 V” (was “5.9 V”). • $V_{DD\_HV\_IO\_MAIN}$: Added footnote "VDD_HV_IO_MAIN range limited to 4.75–5.25 V when FERS = 1 to enable the fast erase time of the flash memory." • $V_{DD\_HV\_ADR\_D}$: Changed Typ value from $V_{DD\_HV\_ADV}$ to $V_{DD\_HV\_ADV\_D}$. • Changed "$V_{DD\_HV\_ADR\_D}$–$V_{DD\_HV\_ADV}$" parameter to "$V_{DD\_HV\_ADR\_D}$–$V_{DD\_HV\_ADV\_D}$." • $V_{SS\_HV\_ADR\_D}$: Changed $V_{SS\_HV\_ADV}$ to $V_{SS\_HV\_ADV\_D}$. • Changed "$V_{SS\_HV\_ADR\_D}$–$V_{SS\_HV\_ADV}$" parameter to "$V_{SS\_HV\_ADR\_D}$–$V_{SS\_HV\_ADV\_D}$." • $V_{DD\_HV\_ADR\_S}$: Added typ value of $V_{DD\_HV\_ADV\_S}$ • Added $V_{SS\_HV\_ADR\_S}$ parameter. • Changed "$V_{DD\_HV\_ADR\_S}$–$V_{DD\_HV\_ADV}$" parameter to "$V_{DD\_HV\_ADR\_S}$–$V_{DD\_HV\_ADV\_S}$" • Changed "$V_{SS\_HV\_ADR\_S}$–$V_{SS\_HV\_ADV}$" parameter to "$V_{SS\_HV\_ADR\_S}$–$V_{SS\_HV\_ADV\_S}$" • For $V_{DD\_HV\_ADV}$ specification, changed parameter to “SARADC, SDADC, Temperature Sensor, and Bandgap Reference supply voltage” (was SARADC and SDADC). For LVD400 disabled and LVD360 disabled conditions, referenced new footnote: “$V_{DD\_HV\_ADV\_S}$ is required to be between 4.5V and 5.5V to read to read the internal Temp Sensor and Bandgap Reference.” • Changed V_{RAMP} to V_{RAMP_LV}, and changed parameter to “slew rate on core power supply pins”. • Added V_{RAMP_HV} specification, parameter “Slew rate on HV power supply pins”, max value 500 V/ms. • Changed $V_{DD\_HV\_IO\_JTAG}$, $V_{DD\_HV\_IO\_FLEX}$, and $V_{DD\_HV\_IO\_EBI}$ values from 4.0 V Min to 4.5 V Min, and changed “5.9 V” Max to “5.5 V” Max. • Moved $V_{REF\_BG\_T}$, $V_{REF\_BG\_TC}$ and $V_{REF\_BG\_LR}$ specifications from ADC pin specification table to Device operating conditions table. • Removed footnote “Maximum frequency for the 292BGA is TBD, and may be lower due to package thermal considerations.” from f_{SYS} specification, Max value “300” MHz. • $V_{DD\_HV\_ADV}$ changed “LVD400 disabled” condition to “LVD360 disabled” for the 3.7V-5.9 V case. • $V_{DD\_HV\_IO\_FLEXE}$ added specification. • V_{STBY_BO} and $V_{DD\_LV\_STBY\_SW}$ removed from the Device operating conditions table and added to the DC electrical specifications table. • V_{por_rel} and V_{por_hys} specifications added. • Removed V_{FERS} row and associated footnote. Table 9 (Emulation (buddy) device operating conditions): • Changed $V_{DD\_LV\_BD}$ minimum value from blank to “1.2” V. • $V_{DD\_LV\_BD}$: Maximum changed to 1.365 V (was 1.32 V). • Changed V_{RAMP_BD} to $V_{RAMP\_LV\_BD}$ and added specification $V_{RAMP\_HV\_BD}$.

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—DC electrical specification**
		Table 10 (DC electrical specifications): • Changed footnote 11, to "The standby RAM regulator current is present on the VDDSTBY pin whenever a voltage is applied to the pin. This also applies to normal operation where the RAM is powered by the VDD_LV supply. Connecting the VDDSTBY pin to ground when not using the standby RAM feature will remove the leakage current on the VDDSTBY pin." • Moved $V_{REF\_BG\_T}$, $V_{REF\_BG\_TC}$ and $V_{REF\_BG\_LR}$ specifications from ADC pin specification table to DC electrical specifications table. • Removed I_{FERS} row. • V_{STBY_BO} and $V_{DD\_LV\_STBY\_SW}$ removed from the Device operating conditions table and added to the DC electrical specifications table. • Changed I_{DD_LV} maximum value to 850 mA (was 910).
		Electrical characteristics—DC electrical specification (con't)
		Table 10 (DC electrical specifications): • Changed I_{DD_LV} maximum value to 850 mA (was 910).\ • $I_{DD\_LV\_BD,}$ changed "250" to "290" mA. • $I_{DD\_BD\_STBY}$, 150 °C condition, changed "120" to "230" mA. • $I_{DD\_MAIN\_CORE\_AC}$: Added footnote "There is an additional 25mA when FERS=1 to enable the fast erase time of the flash memory." • In VDD_HV_PMC availability footnote, changed "QFP" to "416 BGA" and "BGA" to "512 BGA." • Revised footnote "If Aurora and JTAGM/LFAST not used, $V_{DD\_LV\_BD}$ current is reduced by ~20mA." • Removed silicon characterization footnote. Table 12 (I/O input DC electrical characteristics): • $V_{DRFTAUT}$ specification, conditions column, added "4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V". • $V_{DRFTCMOS}$ specification, added 3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V and 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V conditions. • I_{LKG} specification, entire row revised. • Changed footnote 6 "n the range 4.5 V < $VD_{D\_HV\_IO}$ < 5.9 V." to "in the range 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. • V_{HYSAUT} conditions column: replaced dash with 4.5 V < $V_{DD\_HV\_IO}$ < 5.5 V. • C_{IN} row, changed GPIO input pins conditions Max value from "10" to "7" pF and EBI input pins Max value from "8" to "7" pF. • I_{LKG_EBI} removed "Vin = 10%/90%" from parameter column. Figure 18 (I/O output DC electrical characteristics definition): Replaced figure.

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—I/O pad specification**
		Table 13 (I/O pull-up/pull-down DC electrical characteristics): • I_{WPU}, I_{WPD}: substantially revised these specifications. Table 14,Table 15,Table 16,Table 17: • Added footnote to “C” classification header: "Once device characterization is correlated to production I/O testing, the test classification of output resistance parameters may be subject to change in future revisions of this document." • R_{OH_W}, R_{OL_W}, R_{OH_M}, R_{OL_M}, R_{OH_S}, R_{OL_S}, R_{OH_V}, R_{OL_V}: Changed classification to C (was P). • Removed all VSIO conditions (VSIO[VSIO_xx] = 1 and VSIO[VSIO_xx] = 0) from conditions column and added footnote: “All $V_{DD\_HV\_IO}$ conditions for 4.5 V to 5.9 V are valid for VSIO[VSIO_xx] = 1, and all specifications for 3.0 V to 3.6 V are valid for VSIO[VSIO_xx] = 0.” • Removed $T_{PHL/PLH}$ specification from WEAK, MEDIUM, and STRONG configuration output buffer electrical characteristics. • Removed characterization and validation footnotes (total 2) for each table. Table 14, Table 15, Table 16: • $R_{OH\_}$, $R_{OL\_}$, $t_{TR\_}$: Changed 5.9 V conditions to 5.5 V. Table 15,Table 16,Table 17: • Added $t_{TPD10\text{-}90}$ specification. Table 16, Table 17: • In footnotes, changed 5.9 V to 5.5 V. Table 18 (EBI pad output electrical specification): • Replaced this table “EBI output driver electrical characteristics” with new table “EBI pad electrical specification”. Table 19 (I/O consumption) • I_{RMS_EBI}: In Conditions column, changed 66MHz references to 66.7MHz. Removed C_{DRV} = 6 pF condition row. • I_{DYN_EBI}: revised specification.
		Electrical characteristics—I/O pad current specification
		Section 3.7, I/O pad current specification: Changed the first note: from “In order to ensure correct functionality for SENT, the sum of all pad usage ratio within the SENT segment should remain below 50%.” to “In order to maintain the required input thresholds for the SENT interface, the sum of all I/O pad output percent IR drop as defined in the I/O Signal Description table, must be below 50 %. See the I/O Signal Description attachment.”
		Electrical characteristics—Reset pad (PORST, ESR0) electrical characteristics
		Table 20 (Reset electrical characteristics): • |IWPU| parameter, changed Min value from “25” to “23” and Max value from “100” to “82” uA. • |IWPD| parameter, changed Min value from “25” to “40” and Max value from “100” to “130” uA.

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—Oscillator and FMPLL**
		Section 3.12, Oscillator and FMPLL • Updated text to reflect that there is one FMPLL on the chip. Table 22 (PLL1 electrical characteristics) • $f_{PLL1PHI}$ parameter, changed Max freq from “200” MHz to “600” MHz. • First footnote, changed “FXOSC” to “XOSC”. Table 23 (External Oscillator electrical specifications): • Added footnote to both V_{IHEXT} and V_{ILEXT} parameter column “Applies to an external clock input and not to crystal mode”. • Added footnote to V_{ILEXT} parameter column “This parameter is guaranteed by design rather than 100% tested.” • V_{ILEXT} parameter, changed “External Reference” to “External Clock Input”. • Combined C_{S_XTAL} and C_{S_EXTAL} parameters into one specification C_{S_xtal}, updated Min and Max values and removed the “BG292” condition. Table 24 (Selectable load capacitance): • Removed last 16 rows “10000” to “11111”. • Changed footnote 2 from “Values in this table do not include 8 pF routing and ESD structure on die and package trace capacitance.” to “Values in this table do not include the die and package capacitances given by Cs_xtal/Cs_extal in Table 23 (External Oscillator electrical specifications).” • Table 25 (Internal RC Oscillator electrical specifications): δf_{var_SW} parameter added footnote “IRC software trimmed accuracy is performed either with the CMU_0 clock monitor, using the XOSC as a reference or through the CCCU (CAN clock control Unit), extracting reference clock from CAN master clock. Software trim must be repeated as the device operating temperature varies in order to maintain the specified accuracy.”
		Electrical characteristics—ADC specifications
		Table 36 (ADC pin specification·): • I_{LK_INUD}, I_{LK_INUSD}, I_{LK_INREF}, I_{LK_INOUT}: Removed footnote “Leakage current is a parameter potentially showing variation with process maturity. This table is based on current process model, and will be validated when preliminary silicon data of ADC modules and I/O module is available.” • Parameter I_{LK_INOUT} description column, changed “MEDIUM” output buffer with “GPIO” output buffer. Table 27 (SARn ADC electrical specification): • Added new condition for “ΔV_{PRECH}” - “$V_{PRECH} = V_{DD\_HV\_ADR}/2$ $T_J < 150$ °C CTRn[PRECHG] > 2” • $I_{ADCREFL}$ specification: added $V_{DD\_HV\_ADR\_S}$ <= 5.5 V to all modes in condition column. • D_{NL}, “Differential non-linearity” parameter, conditions column, replaced “—” with “$V_{DD\_HV\_ADV} > 4V$, $V_{DD\_HV\_ADR\_S} > 4V$”. • I_{NL}: Conditions column, first row, removed $T_J < 150C$ and added $4.0V < V_{DD\_HV\_ADV\_S} < 5.5V$. Conditions column, second row, removed $T_J < 150C$ and added $V_{DD\_HV\_ADV\_S} = 2V$.

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—ADC specifications (con't)**
		Table 28 (SDn ADC electrical specification): • Removed the I_{LK_IN} specification from table. • For $SNR_{DIFF150}$, $SNR_{DIFF333}$, and SNR_{SE150} specifications, added reference to "S/D ADC is functional in the range 3.0 V < VDD_HV_ADR_D , 4.0 V. . ." footnote. • Moved $V_{REF\_BG\_T}$, $V_{REF\_BG\_TC}$ and $V_{REF\_BG\_LR}$ specifications from ADC pin specification table to Device operating table. • Removed I_{BG} specification as it is already provided in the DC electrical table. • Maximum value of parameter "GAIN" changed from "16" to "15"
		Table 28 (SDn ADC electrical specification): • Changed footnote from "The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.87 dB." to "The ±1% passband ripple specification is equivalent to 20 * $\log_{10}$ (0.99) = 0.087 dB." • Max value of δ_{GROUP} modified for all values of OSR. • $t_{LATENCY}$, $t_{SETTLING}$ and $t_{ODRECOVERY}$: "HPF = ON" and "HPF = OFF" conditions added. New max values. • Added SINAD and THD specifications. • RESOLUTION specification, added footnote "When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. The gives an effective resolution of 15 bits." • $\|\delta_{GAIN}\|$ specification, changed Max value from "1" % to "1.5" %, "0.1" % to "5" mV, "0.25" % to "7.5" mV, and "0.5 %" to 10" mV". • VOFFSET specification, added 3 "After calibration" conditions, $\Delta_{VDD\_HV\_ADR\_D}$ < 5% $\Delta_{VDD\_HV\_ADV\_D}$ < 10% ΔT_J < 50 °C, Max value of "5" mV, $\Delta_{VDD\_HV\_ADR\_D}$ < 5% $\Delta_{VDD\_HV\_ADV\_D}$ < 10% ΔT_J < 100 °C, Max value of "7.5" mV and "After calibration" conditions, $\Delta_{VDD\_HV\_ADR\_D}$ < 5% $\Delta_{VDD\_HV\_ADV\_D}$ < 10% ΔT_J < 150 °C, Max value of "10" mV. • Changed all SNR specification "Unit"s from "dB" to "dBFS". • Changed SFDR specification "Unit" from "dB" to "dBc". • Z_{IN} specification, changed footnote to "Input impedance is valid over the full input frequency range.Input impedance is calculated in megaohms by the formula 25.6/(Gain * f_{ADCD_M}). • Common mode rejection ratio parameter changed symbol from "—" to "V_{cmrr}". • Anti-aliasing filter parameter, changed symbol "—" to "R_{Caaf}". • Stop band attenuation parameter, changed symbol "—" to "$F_{rolloff}$". • Changed footnote in 13 "full input range (specified by Vin)" to "full input frequency range." • Changed in footnote 15 "0.873" dB to "0.087" dB. • f_{ADCD_M}, changed "S/D clock 3(4)" to "S/D Modulator Input Clock" and replaced "—" with "4" in Min column. • f_{ADCD_S} changed "conversion rate'" to "output conversion rate".

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—LFAST electrical specifications**
		Table 30 (LVDS pad startup and receiver electrical characteristics,): • $\lvert\Delta_{VI}\rvert$ specification, Differential input voltage parameter, added footnote 12 "The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing." Table 31 (LFAST transmitter electrical characteristics,): • $\lvert_{VOD}\rvert$: removed the delta from symbol. Changed values to Min = 110, Typ = 171, Max = 285 and removed the "+/-" from each value. • t_{TR}: changed "(10%–90% of swing)" to "(absolute value of the differential output voltage swing)." Table 32 (MSC/DSPI LVDS transmitter electrical characteristics ,): • $\lvert_{VOD}\rvert$: removed the delta from symbol. Changed values to Min = 150, Typ = 214, Max = 400 and removed the "+/-" from each value. • t_{TR}: Changed "(10%–90% of swing)" to "(absolute value of the differential output voltage swing)." Table 33 (LFAST PLL electrical characteristics): • $\lvert\Delta_{VI}\rvert$ specification, Differential input voltage parameter, added footnote 12 "The LXRXOP[0] bit in the LFAST LVDS Control Register (LCR) must be set to one to ensure proper LFAST receive timing."
		Table 32 (MSC/DSPI LVDS transmitter electrical characteristics ,), Rise/Fall time parameter: • Changed "(10%–90% of swing)" to (absolute value of the differential output voltage swing). Table 33 (LFAST PLL electrical characteristics): • Changed footnote 2, from "320" to "640" MHz frequency.
		Electrical characteristics—Aurora LVDS electrical characteristics
		Table 34 (Aurora LVDS electrical characteristics,): • Removed $V_{DD\_HV\_IO\_BD}$ and V_{DD_LV} specifications as they are supplied in the device operating conditions table. • Changed "C_{AC}" specification name to "C_{ac_clk}". • Added specification "C_{ac_tx}".

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—Power management: PMC, POR/LVD, sequencing**
		Figure 20 (Recommended supply pin circuits): • For VDD_LV supply: Changed "nxClv" to "Clv." Table 35 (Device power supply integration): • C_{HV_IO} removed footnote. • C_{HV_FLA} parameter, added footnote "Start-up time of the internal flash regulator from release of the LVD360 is worst case 500 us. This is based on the typical CHV_FLA bulk capacitance value." • C_{LV}: Changed the 3 for Bypass capacitance at pin to "Note3." Changed parameter "Bypass capacitance at pin" to "Total bypass capacitance at external pin." • Significantly revised $C_{HV\_PMC\_BYP}$, including changing spec name to C_{HV_PMC}, min value to 2.2 µF (was 200 nF), and typ value to 4.7 µF (was "—"). Added footnote "For noise filtering it is recommended to add a high frequency bypass capacitance of 0.1 µF between VDD_HV_PMC and VSS_HV." Table 36 (Flash power supply): • $V_{DD\_HV\_FLA}$, after trimming, Min value "3.2" changed to "3.15". Added two notes. • Removed I_{REG_FLA} specification. Table 39 (Functional terminals state during power-up and reset): • Changed "TRST" to "JCOMP."

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—Device voltage monitoring electrical characteristics**
		Table 37 (Voltage monitor electrical characteristics): • V_{PORUP_LV} Rising voltage (power up) condition, changed Min value "1040" to "1111" and Max value "1180" to "1235". • V_{PORUP_LV} Falling voltage (power down) condition, changed Min value "960" to "1015" and Max value "1100" to "1125". Added footnote. • V_{LVD096} "960" to "1015" and Max value "1100" to "1145". • V_{LVD108} changed Min value "1080" to "1125" and Max value "1140" to "1235". • V_{LVD112} changed Min value "1110" to "1175 and Max value "1180" to "1235". • V_{HVD140} changed Min value "1320" to "1385" and Max value "1440" to "1475". • Added new specification V_{HVD145}. • Added "HVD140 does not cause reset" at end of footnote "HVD is released after $t_{VDRELEASE}$ temporization when lower threshold is crossed, HVD is asserted $t_{VDASSERT}$ after detection when upper threshold is crossed." •]V_{PORUP_HV}, added footnote "the PMC supply also needs to be below 5472 mV (untrimmed HVD600)". Added new conditions: Rising voltage (power up) on IO JTAG, and Osc supply, Rising voltage (power up) on ADC supply, and Hysteresis on Power-up. • V_{PORUP_HV}: Changed Falling voltage (power down) minimum value to "2850" (was "2680") and maximum value to 3162 (was "2980"). • Revised Falling voltage footnote to read "Untrimmed LVD300_A will be asserted first on power down" (was "Assume all LVDs except LVD270 on HV supplies disabled"). • V_{LVD295} Rising voltage condition changed Max value "3100" to "3120". • V_{LVD295} Falling voltage condition changed Min value "2950" to "2920" and Max value "3080" to "3100". • V_{HVD360} Rising voltage condition changed Min value "3420" to "3435" and Max value "3610" to "3650". • V_{HVD360} Falling voltage condition changed Min value "3400" to "3415".
		Electrical characteristics—Flash memory electrical characteristics
		Section 3.15, Flash memory electrical characteristics: • This section completely revised.
		Electrical characteristics—AC specifications—Debug and Calibration
		Table 46 (JTAG pin AC electrical characteristics,): • Added footnote "JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet." Table 47 (Nexus debug port timing) • Footnote 1 changed to "Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet." • Changed "TDI" to "TDI/TDIC," "TMS" to "TMS/TMSC," and "TDO" to "TDO/TDOC." Figure 27 (Nexus TDI/TDIC, TMS/TMSC, TDO/TDOC timing): • Changed "TDI" to "TDI/TDIC," "TMS" to "TMS/TMSC," and "TDO" to "TDO/TDOC."

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Electrical characteristics—AC specifications—Fast Ethernet Controller (FEC)**
		Table 61 (MII serial management channel timing): • Added footnote to "Value" column: **"**Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value." Table 63 (RMII transmit signal timing,): • Added footnote to "Value" column **"**Output parameters are valid for C_L = 25 pF, where C_L is the external load to the device. The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value." • Added footnote to table title: "RMII timing is valid only up to a maximum of 150 ^{o}C junction temperature."
		Electrical characteristics—AC specifications—FlexRay
		Section 3.16.4, FlexRay timing: • Removed reference to "292 MAPBGA". • Removed " . . . and subject to change per the final timing analysis of the device" from FlexRay specification sentence. Table 66 (RxD input characteristics): • Added footnote: "FlexRay RxD timing is valid for all input levels and hysteresis disabled."
		Electrical characteristics—AC specifications—EBI
		Table 69 (Bus Operation Timing): • Changed bus frequency in table heading to "66.7 MHz" (was "66 MHz"). • Footnote 1, added "with DSC = 0b10 for ADDR/CTRL and DSC = 0b11 for CLKOUT/DATA." • Footnote 3, changed "[Clock Register TBD]" TO "CGM_SC_DC4 register". • Footnote 4, changed "VDDE" to "VDD_HV_IO_EBI or VDD_HV_IO_FLEXE." • Spec 5, Characteristic column, added "ADDR[8:11]/WE[0:3]/BE[0:3]," "BDIP," and overbar on CS, OE, and TS. Changed "ADDR[8:31]" to "ADDR[12:31]." • Spec 6, Characteristic column, added "ADDR[8:11]/WE[0:3]/BE[0:3]", "BDIP," overbar on CS, OE, TS, and footnote "One wait state must be added to the output signal valid delay for external writes." Changed "ADD[8:31]" to "ADDR[12:31]." • Spec 7, change Min value from "6.0" to "7.0" ns. • Spec 8, Characteristic column, changed to "DATA[0:31]". • Removed cut 1 footnotes associated with output delay and setup time (total 2). Figure 50 (D_CLKOUT Timing) Figure 51 (Synchronous Output Timing) Figure 52 (Synchronous Input Timing): • Changed "VDDE" to "VDD_HV_IO_EBI" throughout.
		Electrical characteristics—AC specifications—I2C
		Section 3.16.8, "I2C timing: New section.
		Electrical characteristics—AC specifications—GPIO delay
		Section 3.19.10, GPIO delay timing • New section

Table 76. Revision history (continued)

Revision	Date	Description of changes
3	3/2014	**Package characteristics**
		Section 4, Package characteristics: • Removed the "292 MAPBGAcase drawing" figures. • Table 73 (Package case numbers): Removed the 292MAPBGA row.
		Electrical characteristics—Thermal Characteristics
		Table 74 (Thermal characteristics): • Removed "292 Value" column.
		Ordering Information
		Table 75 (Orderable part number summary) • Changed Freescale part numbers: 416 MAPBGA PD to TEPBGA "PPC5777MK0MVU8A" (was PPC5777MQK0MVU8), 512 TEPBGA PD to "PPC5777MK0MVA8A" (was PPC5777MQK0MVA8), 416 MAPBGA ED to TEPBGA "PPC5777M2K0MVU8A" (was PPC5777M2K0MVU8), and 512 TEPBGA ED to "PPC5777M2K0MVA8A" (was PPC5777M2K0MVA8) • Removed KGD and Production PD rows. • Removed "Flash/SRAM," "Emulation RAM," and "Frequency" columns. Figure 61 (Product code structure): • Package Code, added "VA = 512 TEPBGA Pb-Free". • Package Code, added "VU = 416 TEPBGA Pb-Free". • Miscellaneous, added "2 = Emulation Device". • Changed "Tape and Reel" to "Suffix" and added "A = cut2.0 revision". • In "Fab and Mask Revision" codes, changed "K = TBD" to "K = TSMC."
4	9/2014	**Throughout**
		• Removed parameter classifications from specification tables. • Editorial changes and improvements.
		Introduction
		• In Figure 1 (Block diagram), added "LFAST & SIPI" block to 50 MHz concentrator. • In Figure 2 (Periphery allocation), changed block to "2 x SIPI" (was "SIPI_0") and removed double arrow on its right side.
		Electrical characteristics—Operating conditions
		• Extensive revisions to Table 8 (Device operating conditions).

Table 76. Revision history (continued)

Revision	Date	Description of changes
4	9/2014	**Electrical characteristics—DC electrical specification**
		• In Section 3.1, Introduction, added the following to note text: "$V_{DD\_HV\_ADV}$ refers to ADC supply pins $V_{DD\_HV\_ADV\_S}$ and $V_{DD\_HV\_ADV\_D}$. $V_{DD\_HV\_ADR}$ refers to ADC reference pins $V_{DD\_HV\_ADR\_S}$ and $V_{DD\_HV\_ADR\_D}$. $V_{SS\_HV\_ADV}$ refers to ADC ground pins $V_{SS\_HV\_ADV\_S}$ and $V_{SS\_HV\_ADV\_D}$. $V_{SS\_HV\_ADR}$ refers to ADC reference pins $V_{SS\_HV\_ADR\_S}$ and $V_{SS\_HV\_ADR\_D}$." • In Table 10 (DC electrical specifications), changed $I_{DD\_HV\_PMC}$ maximum for PMC only condition (was 5 mA, is 25 mA). Added “This includes PMC consumption, LFAST PLL regulator current, and Nwell bias regulator current” to footnote associated with this value. • In Table 10 (DC electrical specifications), changed I_{DD_LV} maximum to 1140 mA (was 600 mA) and added “V_{DD_LV} = 1.325 V” to conditions. • In Table 10 (DC electrical specifications), added I_{DDAPP_LV} specification. • In Table 10 (DC electrical specifications), changed the conditions for I_{DDSTBY_RAM} and I_{DDSTBY_REG} (were “...to 6 V...”, are “...to 5.5 V...”). • In Table 10 (DC electrical specifications), I_{DDSTBY_RAM} specification: changed max value for 40°C condition to 60 µA (was 40). Changed max value for 85°C condition to 100 µA (was 60). • In Table 10 (DC electrical specifications), V_{STBY_BO} specification: changed min value to 0.9 V (was 0.8).
		Electrical characteristics—I/O pad current specification
		• Table 12 (I/O input DC electrical characteristics), Table 13 (I/O pull-up/pull-down DC electrical characteristics), Table 14 (WEAK configuration output buffer electrical characteristics), Table 15 (MEDIUM configuration output buffer electrical characteristics), Table 16 (STRONG configuration output buffer electrical characteristics), Table 17 (VERY STRONG configuration output buffer electrical characteristics), Table 19 (I/O consumption) added the following footnote to Conditions heading: “During power up operation, the minimum required voltage to come out of reset state is determined by the V_{PORUP_HV} monitor, which is defined in the voltage monitor electrical characterstics table. Note that the V_{PORUP_HV} monitor is connected to the $V_{DD\_HV\_IO\_MAIN0}$ physical I/O segment.” • Table 12 (I/O input DC electrical characteristics): V_{HYSTTL} specification: changed min value to 0.275 (was 0.3). V_{HYSAUT} specification: changed min value to 0.4 (was 0.5). • Table 12 (I/O input DC electrical characteristics), changed V_{IHCMOS_H} min value to “0.70 * $V_{DD\_HV\_IO}$” (was 0.65 * $V_{DD\_HV\_IO}$). • In Table 12 (I/O input DC electrical characteristics), changed V_{IHAUT} min value to 3.9 V (was 3.8). • Table 12 (I/O input DC electrical characteristics), revised I_{LKG} and I_{LKG_EBI} rows.

Table 76. Revision history (continued)

Revision	Date	Description of changes
4	9/2014	**Electrical characteristics—I/O pad current specification**
		• Table 14 (WEAK configuration output buffer electrical characteristics), R_{OH_W} and R_{OL_W}: changed min value to 517 (was 560) and max value to 1052 (was 1040). • Table 15 (MEDIUM configuration output buffer electrical characteristics), R_{OH_M} and R_{OL_M}: changed min value to 135 (was 140). • Table 16 (STRONG configuration output buffer electrical characteristics), R_{OH_S} and R_{OL_S}: changed min value to 30 (was 35) and max value to 77 (was 65). • Table 17 (VERY STRONG configuration output buffer electrical characteristics), revised R_{OH_V} and R_{OL_V} conditions. • Table 17 (VERY STRONG configuration output buffer electrical characteristics), R_{OH_V} and R_{OL_V}: changed max values to 72 (was 60) and 90 (was 75). • Table 18 (EBI pad output electrical specification), $R_{OH\_EBI\_GPIO}$ and $R_{OL\_EBI\_GPIO}$: changed max value to 400 (was 260). • In Table 18 (EBI pad output electrical specification): $V_{IHCMOS\_H\_EBI}$ specification: changed max value to "$V_{DD\_HV\_IO\_EBI}$ + 0.3" (was "$V_{DD\_HV\_IO}$ + 0.3"). $R_{OH\_EBI\_GPIO}$ specification: changed condition to "4.5 V < $V_{DD\_HV\_IO\_EBI}$ < 5.5 V" (was "3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V"). $R_{OL\_EBI\_GPIO}$ specification: changed condition to "4.5 V < $V_{DD\_HV\_IO\_EBI}$ < 5.5 V" (was "3.0 V < $V_{DD\_HV\_IO}$ < 3.6 V").
		Electrical characteristics—Oscillator and FMPLL
		• In Table 23 (External Oscillator electrical specifications), deleted the transconductance specification (g_m).
		Electrical characteristics—ADC specifications
		• Table 26 (ADC pin specification), I_{LK_INUD} specification: changed T_J < 40 °C condition max value to 50 nA (was 70). Changed T_J< 150 °C condition max value to 150 nA (was 220). • In Table 27 (SARn ADC electrical specification): added condition rows for full and fast precharge to $t_{ADCPRECH}$, revised condition entries for ΔV_{PRECH}. • In Table 28 (SDn ADC electrical specification), changed the max value for $t_{LATENCY}$ at HPF = OFF (was 2*δ_{GROUP}, is δ_{GROUP}). • In Table 28 (SDn ADC electrical specification), changed the max value for GAIN (was 15, is 16). • Table 28 (SDn ADC electrical specification), SNR_{SE150}: changed GAIN=1 min value to 72 (was 74), GAIN=2 min value to 69 (was 71), GAIN=4 min value to 66 (was 68), GAIN=8 min value to 63 (was 65), and GAIN=16 min value to 60 (was 62). • Table 28 (SDn ADC electrical specification), δ_{GROUP} specification: changed OSR = 75 max value to 696 Tclk (was 746), changed OSR = 96 max value to 946.5 Tclk (was 946.4). • In Table 28 (SDn ADC electrical specification), added footnote to parameter column for $t_{LATENCY}$.
		Electrical characteristics—Power management: PMC, POR/LVD, sequencing
		• In Section 3.16, Power management: PMC, POR/LVD, sequencing, replaced PMC operating conditions and external regulators supply voltage table with a cross reference to Table 8 (Device operating conditions). • In Table 35 (Device power supply integration), changed minimum VDD_LV external capacitance footnote to "variation over voltage, temperature, and aging" (was "variation over process, voltage, temperature, and aging.") • In Table 36 (Flash power supply), revised table footnotes and added new "After trimming; 25°C < TJ ≤ 150°C" condition to $V_{DD\_HV\_FLA}$.

Table 76. Revision history (continued)

Revision	Date	Description of changes
4	9/2014	**Electrical characteristics—Device voltage monitoring electrical characteristics**
		• In Table 37 (Voltage monitor electrical characteristics), revised the entries for V_{LVD108} and V_{LVD145}.
		Electrical characteristics—Flash memory electrical characteristics
		• Multiple changes throughout Section 3.15, Flash memory electrical characteristics.
		Electrical characteristics—AC specifications—GPIO delay
		• In Table 72, changed parameter to “Delay from SIUL2 MSCR register bit update to pad function enable at the input of the I/O pad” (was “Delay from MSCR bit update to pad function enable”).
		Electrical characteristics—Thermal Characteristics
		• Updated Table 74 (Thermal characteristics).
		Ordering Information
		• Revised Table 75 (Orderable part number summary).
5	6/2015	**Electrical characteristics—Absolute maximum ratings**
		Table 6 (Absolute maximum ratings) • $V_{DD\_LV\_BD}$: corrected footnote numbering. • Revised footnote (“Allowed 1.38– 1.45 V...”) text to 1.38 (was 1.375). Revised footnote (“1.32 – 1.38 V range...”) text to 1.38 (was 1.375) and “1.326 V at maximum” (was “1.288 V at maximum”).
		Electrical characteristics—Operating conditions
		Table 8 (Device operating conditions) • Consolidated duplicate footnotes throughout table. • $V_{DD\_HV\_ADV}$: added footnote (“SAR ADC only...”) to LVD disabled conditions. • Revised $V_{DD\_HV\_ADR\_D}$ row. • Changed V_{RAMP_LV} max value to 100 V/mx (was 500). • Revised footnote (“RAM data retention is guaranteed at a voltage...”) (was “RAM data retention is not guaranteed below...”). Table 9 (Emulation (buddy) device operating conditions) • Changed $V_{RAMP\_LV\_BD}$ max value to 100 V/ms (was 500).
		Electrical characteristics—DC electrical specification
		Table 10 (DC electrical specifications) • $I_{DD\_MAIN\_CORE\_AC}$: changed max value to 115 mA (was 105). • $I_{DD\_CHKR\_CORE\_AC}$: changed max value to 80 mA (was 45). • I_{DDSTBY_REG}: changed max value to 50 µA (was 30). • V_{STBY_BO} specification: changed minimum to no value (was 0.9 V) and maximum to 0.9 V (was no value) with footnote (“V_{STBY_BO} is the maximum voltage...”). • $V_{DD\_LV\_STBY\_SW}$: changed min value to 0.93 V (was 0.95).
		Electrical characteristics—Reset pad (PORST, ESR0) electrical characteristics
		Table 20 (Reset electrical characteristics) • Changed V_{IH} min value to 2.2 V (was 2.0). • Changed W_{FNMI} max value to 15 ns (was 20).

Table 76. Revision history (continued)

Revision	Date	Description of changes
5	6/2015	**Electrical characteristics—I/O pad current specification**
		Replaced Figure 18 (I/O output DC electrical characteristics definition). Table 12 (I/O input DC electrical characteristics) • V_{IHAUT} specification: changed min value to 3.8 V. • V_{HYSTTL}: Changed min value to 0.250 V (was 0.275). Removed footnote ("Minimum hysteresis...") from min value. Table 13 (I/O pull-up/pull-down DC electrical characteristics) • Added "AUTO" and "CMOS" designations to conditions for $\|I_{WPU}\|$ and $\|I_{WPD}\|$. • $\|I_{WPU}\|$ specification: changed final condition row to "V_{IN} = 0.35*$V_{DD\_HV\_IO}$" (was "V_{IN} = 0.65*$V_{DD\_HV\_IO}$"). Table 14 (WEAK configuration output buffer electrical characteristics) • R_{OH_W} specification: changed min value to 520 Ω (was 517). • R_{OL_W} specification: changed min value to 520 Ω (was 517). Table 15 (MEDIUM configuration output buffer electrical characteristics), Table 16 (STRONG configuration output buffer electrical characteristics), and Table 17 (VERY STRONG configuration output buffer electrical characteristics) • Changed specification to $t_{TPD50-50}$ and revised row. Table 16 (STRONG configuration output buffer electrical characteristics) • Added $\|t_{SKEW\_S}\|$ specification. Table 17 (VERY STRONG configuration output buffer electrical characteristics) • Added I_{DCMAX_VS} specification. Table 18 (EBI pad output electrical specification) • Removed all specifications in Input Specifications section and changed table title to "EBI Pad Output Electrical Specifications." • t_{PD_EBI}: changed parameter to "50% – 50% threshold..." (was "50% - 10% 90% threshold...") and changed max value to 4.0 ns (was 5.5). • $R_{OH\_EBI\_GPIO}$ specification: change min value to 100 Ω (was 150).
		Electrical characteristics—Oscillator and FMPLL
		Table 21 (PLL0 electrical characteristics) • Added footnote ("f_{PLL0IN} frequency must be...") to f_{PLL0IN} parameter. • Changed footnote text to "Noise on the V_{DD_LV} supply..." (was "VDD_LV noise due..."). • Added footnote ("PLL jitter is guaranteed when...") to $\|\Delta_{PLL0PHISPJ}\|$, $\|\Delta_{PLL0PHI1SPJ}\|$, and $\Delta_{PLL0LTJ}$ specifications. • Added $f_{PLL0VCOFR}$ specification. Table 22 (PLL1 electrical characteristics), • Added $f_{PLL1VCOFR}$ specification. Table 24 (Selectable load capacitance) • Significant changes throughout table.

Table 76. Revision history (continued)

Revision	Date	Description of changes
5	6/2015	**Electrical characteristics—ADC specifications**
		In Table 27 (SARn ADC electrical specification) • $I_{ADCREFH}$ specification: changed min value for Run mode $t_{conv} \geq 5$ µs condition to 7 µA (was 3.5). Changed max value for Power Down mode condition to 6 µA (was 1). • I_{ADV_S} specification, Power Down mode: changed max value to 1.0 mA (was 0.04). • INL and DNL rows: removed injection current footnote. • TUE_{12} row: changed footnote text to "This parameter is guaranteed..." (was "TUE, INL, and DNL are granted..."). Removed T_J < 150 °C, $V_{DD\_HV\_ADV\_S}$ > 4 V, $V_{DD\_HV\_ADR\_S}$ > 4 V condition row. In Table 28 (SDn ADC electrical specification) • V_{OFFSET}: Changed parameter name to "Input Referred Offset Error" (was "Conversion Offset") and added footnote ("Conversion offset error must be..."). • $SNR_{DIFF150}$, $SNR_{DIFF333}$, SNR_{SE150}: removed footnote ("SNR degraded by 3dB...") and changed conditions range to 4.5 (was 4.0). • SNR_{SE150} specification: revised min values for each condition. Added footnote ("This parameter is guaranteed..."). • For first footnote "S/D ADC is functional in the range..." changed voltage range to 3.6 V–4.5 V (was 3.6 V < $V_{DD\_HV\_ADV\_D}$ < 4.0 V) and added "Degraded SNR value based on simulation." • For second footnote "S/D ADC is functional in the range..." changed voltage range to 3.0 V–4.5 V and added "Degraded SNR value based on simulation." • V_{cmrr} specification: changed min value to 54 dB (was 20 dB). • δ_{GROUP} specification: increased the max value for each condition by 3 Tclk. • ΣI_{ADR_D} specification: changed max value to 30 µA (was 20). Added "f_{ADCD_M} = 14.4 MHz" to condition.
		Electrical characteristics—LFAST electrical specifications
		Table 30 (LVDS pad startup and receiver electrical characteristics,) • Revised entire R_{IN} specification row. Table 31 (LFAST transmitter electrical characteristics,) • f_{DATA}: Changed max value to "312/320" (was 320) and added footnote. Table 33 (LFAST PLL electrical characteristics) • Changed ERR_{REF} and DC_{REF} parameter descriptions to "PLL input reference clock" (was "PLL reference clock").
		Electrical characteristics—Power management: PMC, POR/LVD, sequencing
		Table 36 (Flash power supply) • Removed $V_{DD\_HV\_PMC}$ row (this specification documented in Table 8 (Device operating conditions).
		Electrical characteristics—Flash memory electrical characteristics
		• Added Section 3.15.7, Flash read wait state and address pipeline control settings.
		Electrical characteristics—AC specifications—DSPI
		• Substantial revisions to Section 3.16.2, DSPI timing with CMOS and LVDS pads.
		Electrical characteristics—AC specifications—FlexRay
		Table 66 (RxD input characteristics) • Revised footnote ("FlexRay RxD timing is valid . . .").

Table 76. Revision history (continued)

Revision	Date	Description of changes
5	6/2015	**Ordering Information**
		Table 75 (Orderable part number summary) • Revised ED footnote ("'ED' refers to . . .").
6	6/2016	**Introduction**
		Section 1.3, Device feature • Changed the name of the section to Device feature. • Table 1 (MPC5777M feature) Changed the name of the table to MPC5777M feature. Figure 1 • Removed the 50 MHz from the concentrator box and added 50 MHz and 100 Mhz to the connection arrows.
		Electrical characteristics—I/O pad specification
		Section 3.7, I/O pad current specification • Added paragraph (In order to ensure device reliability....., and In order to ensure device functionality....). • Removed the entries I_{RMS_SEG} and I_{DYN_SEG} in Table 19 (I/O consumption). Table 12 (I/O input DC electrical characteristics) • V_{HYSTTL} specification: Changed min value to 0.275 V (was 0.250 V)
		Electrical characteristics—Oscillator and FMPLL
		Table 25 (Internal RC Oscillator electrical specifications) • Added δf_{TRIM} specification.
		Electrical characteristics—ADC Specifications
		Table 28 (SDn ADC electrical specification), • Z_{DIFF}, Z_{CM} and ΔV_{INTCM} specifications added. R_{BIAS} specification has been updated.
		Electrical characteristics—AC specifications—FlexRay
		Table 66 (RxD input characteristics) • Changed footnote ("FlexRay RxD timing is valid . . .").

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