

# MPC7410 RISC Microprocessor Hardware Specifications Addendum for the MPC7410TxxnnnNE Series

This document describes part-number-specific changes to the *MPC7410 RISC Microprocessor Hardware Specifications* (Document No. MPC7410EC).

Specifications provided in this document supersede those in the *MPC7410 RISC Microprocessor Hardware Specifications*, Rev. 6.1 or later, for the part numbers listed in [Table A](#). only. Specifications not addressed herein are unchanged.

Because this document is frequently updated, see the website listed on the back page of this document or contact your Freescale sales office for the latest version.

*Freescale Part Numbers Affected:*

*MPC7410TRX400NE*

*MPC7410TRX450NE*

*MPC7410THX450NE*

**Table A. Part-Number-Specific Changes**

| Freescale Part Number | Operating Conditions |            |                     |               | Significant Differences from Hardware Specification  |
|-----------------------|----------------------|------------|---------------------|---------------|--|
|                       | CPU Frequency        | Vdd        | T <sub>J</sub> (°C) | OVdd          |  |
| MPC7410TRX400NE       | 400 MHz              | 1.5V±50mV  | -40 to 105          | 1.8/2.5 V     | Extended temperature range. Reduced core voltage to achieve lower power consumption. Removes 3.3 V OVdd support. For all AC/DC specifications not mentioned in this document, see the MPC7410RX400LE specifications in the general <i>MPC7410 Hardware Specifications</i> .            |
|                       | 450 MHz              | 1.8V±100mV | -40 to 105          | 1.8/2.5/3.3 V | Extended temperature range. The MPC7410TRX400NE also fully conforms to the MPC7410TRX450LE specification. See the general <i>MPC7410 Hardware Specifications</i> .   |
| MPC7410TRX450NE       | 450 MHz              | 1.5V±50mV  | -40 to 105          | 1.8/2.5 V     | Extended temperature range. Reduced core voltage to achieve lower power consumption. Removes 3.3V OVdd support. For all AC/DC specifications not mentioned in this document, please refer to the MPC7410RX450LE specifications in the general <i>MPC7410 Hardware Specifications</i> . |
|                       | 500 MHz              | 1.8V±100mV | -40 to 105          | 1.8/2.5/3.3 V | Extended temperature range. The MPC7410TRX450NE also fully conforms to the MPC7410TRX500LE specification. See the general <i>MPC7410 Hardware Specifications</i> .   |
| MPC7410THX450NE       | 450 MHz              | 1.5V±50mV  | -40 to 105          | 1.8/2.5 V     | Extended temperature range. Reduced core voltage to achieve lower power consumption. Removes 3.3V OVdd support. For all AC/DC specifications not mentioned in this document, see to the MPC7410HX450LE specifications in the general <i>MPC7410 Hardware Specifications</i> .          |
|                       | 500 MHz              | 1.8V±100mV | -40 to 105          | 1.8/2.5/3.3 V | Extended temperature range. The MPC7410THX450NE also fully conforms to the MPC7410THX500LE specification. See the general <i>MPC7410 Hardware Specifications</i> .   |

## Features

The MPC7410TxxnnnNE feature set is identical to that of the MPC7410, with the following exceptions:

- Bus interface
  - Selectable interface voltages of 1.8 V, 2.5 V (3.3 V is not supported)

## DC Electrical Characteristics

The MPC7410TxxnnnNE DC electrical characteristics are identical to that of the MPC7410, with the exceptions shown in [Table B](#), [Table C](#), and [Table D](#).

Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in [Table B](#).

**Table B. Input Threshold Voltage Setting**

| BVSEL Signal <sup>3</sup>  | Processor Bus Input Threshold is Relative to: | L2VSEL Signal <sup>3</sup> | L2 Bus Input Threshold is Relative to: | Note    |
|----------------------------|---|----------------------------|--|---------|
| 0                          | 1.8 V   | 0                          | 1.8 V                                  | 1       |
| $\overline{\text{HRESET}}$ | 2.5 V   | $\overline{\text{HRESET}}$ | 2.5 V                                  | 1, 2    |
| 1                          | Not Supported                                 | 1                          | 2.5 V                                  | 1, 4, 5 |
| HRESET                     | Not Supported                                 | HRESET                     | Not Supported                          | —       |

Notes:

- Caution:** The input threshold selection must agree with the OVdd/L2OVdd voltages supplied.
- To select the 2.5-V threshold option, BVSEL and/or L2VSEL should be tied to  $\overline{\text{HRESET}}$  so that the two signals change state together. This is the preferred method for selecting this mode of operation.
- To overcome the internal pull-up resistance, a pull-down resistance less than 250 ohms should be used.
- Default voltage setting if left unconnected (internal pulled-up).
- Caution:** The MPC7410TRXnnnNE does not support the default OVdd setting of 3.3 V. The BVSEL input must be tie either low or to  $\overline{\text{HRESET}}$ .

**Table C. Recommended Operating Conditions**

| Characteristic               | Symbol  | Recommended Value  | Unit                      |   |
|------------------------------|---|--------------------|---------------------------|---|
| Core supply voltage          | V <sub>dd</sub>                                   | 1.5V ± 50mV        | V                         |   |
| PLL supply voltage           | AV <sub>dd</sub>                                  | 1.5V ± 50mV        | V                         |   |
| L2 DLL supply voltage        | L2AV <sub>dd</sub>                                | 1.5V ± 50mV        | V                         |   |
| Processor bus supply voltage | BVSEL = 0   | OV <sub>dd</sub>   | 1.8V ± 100mV              | V |
|                              | BVSEL = $\overline{\text{HRESET}}$                | OV <sub>dd</sub>   | 2.5V ± 100mV              | V |
|                              | BVSEL = HRESET or BVSEL = 1                       | OV <sub>dd</sub>   | Not Supported             | V |
| L2 bus supply voltage        | L2VSEL = 0  | L2OV <sub>dd</sub> | 1.8V ± 100mV              | V |
|                              | L2VSEL = $\overline{\text{HRESET}}$ or L2VSEL = 1 | L2OV <sub>dd</sub> | 2.5V ± 100mV              | V |
| Input voltage                | Processor bus and JTAG Signals                    | V <sub>in</sub>    | GND to OV <sub>dd</sub>   | V |
|                              | L2 Bus  | V <sub>in</sub>    | GND to L2OV <sub>dd</sub> | V |
| Die-junction temperature     | T <sub>j</sub>                                    | -40 to 105         | °C                        |   |

**Table D. Power Consumption for MPC7410**

|                                 | Processor (CPU) Frequency | Processor (CPU) Frequency | Unit | Notes |
|---------------------------------|---------------------------|---------------------------|------|-------|
|                                 | 400 MHz                   | 450 MHz                   |      |       |
| Full-On Mode                    |                           |                           |      |       |
| Typical                         | 2.92                      | 3.29                      | W    | 1, 3  |
| Maximum                         | 6.6                       | 7.43                      | W    | 1, 2, |
| Doze Mode                       |                           |                           |      |       |
| Maximum                         | 3.6                       | 4.1                       | W    | 1, 2  |
| Nap Mode                        |                           |                           |      |       |
| Maximum                         | 1.35                      | 1.5                       | W    | 1, 2  |
| Sleep Mode                      |                           |                           |      |       |
| Maximum                         | 1.3                       | 1.45                      | W    | 1, 2  |
| Sleep Mode—PLL and DLL Disabled |                           |                           |      |       |
| Typical                         | 0.6                       | 0.6                       | W    | 1, 3  |
| Maximum                         | 1.1                       | 1.1                       | W    | 1, 2  |

**Notes:**

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mw and L2AVdd = 15 mW.
2. Maximum power is measured at 105 °C and Vdd = 1.5V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at 65 °C and Vdd = 1.5V in a system while running typical benchmarks.

## Part Numbers Addressed by this Specification

Table E provides the ordering information for the MPC7410TxxnnnNE series.

**Table E. Part Marking Nomenclature**

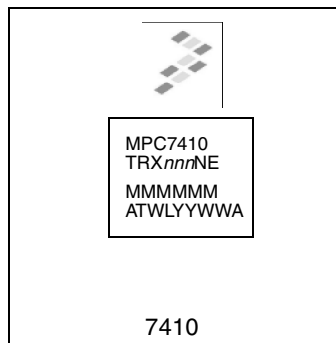
| MPC          | 7410            | x                  | xx             | nnn                              | x                    | x                       |
|--------------|-----------------|--------------------|----------------|----------------------------------|----------------------|-------------------------|
| Product Code | Part Identifier | Process Descriptor | Package        | Processor Frequency <sup>1</sup> | Application Modifier | Revision Level          |
| MPC          | 7410            | T: -40° to 105°C   | RX = CBGA      | 400<br>450                       | N: 1.5 V ±50 mV      | E: 1.4; PVR = 800C 1104 |
|              |                 |                    | HX = HCTE_CBGA | 450                              |                      |                         |

**Note:**

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.

# Part Marking

Parts are marked as the example shown in [Figure A](#).



**Notes:**

- nnn* is the speed grade of the part
- MMMMMM is the 6-digit mask number
- ATWLYYWWA is the traceability code
- CCCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

BGA

**Figure A. Freescale Part Marking for BGA Device**

# Document Revision History

[Table F](#) provides a revision history for this document.

**Table F. Document Revision History**

| Rev. Number | Date    | Substantive Changes  |
|-------------|---------|--|
| 2           | 11/2010 | <ul style="list-style-type: none"> <li>• Removed “RX” from document title.</li> <li>• Added MPC7410THX450NE to list of devices covered by this document.</li> <li>• In <a href="#">Table B</a>, “Input Threshold Voltage Setting,” changed “XPC7410TRXnnnNE” to “MPC7410TRXnnnNE” in note 5.</li> <li>• Updated <a href="#">Table E</a>, “Part Marking Nomenclature,” to include MPC7410THX450NE.</li> </ul> |
| 1.2         | 4/2005  | <ul style="list-style-type: none"> <li>• Document template update</li> <li>• Document ID change from MPC7410TRXNEPNS/D for Part Number Specification to MPC7410ECS07AD for Hardware Specification Addendum.</li> </ul>   |
| 1.1         | 5/2003  | Rather than readers of this spec referring to the MPC7410RXnnnNE part number spec and then to the MPC7410RXnnnLE general hardware spec, this spec now includes the spec differences outlined in the MPC7410RXnnnNE part number spec. Any specifications not called out in this spec for the part numbers listed in <a href="#">Table A</a> default back to the general hardware spec.                        |
| 1           | —       | Minor formatting   |
| 0           | —       | Initial Release  |

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Freescale Semiconductor China Ltd.  
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