Freescale Semiconductor
Technical Data

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MPC8544E PowerQUICC III Integrated Processor Hardware Specifications

1 MPC8544E Overview

This section provides a high-level overview of MPC8544E features. Figure 1 shows the major functional units within the device.

1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance, 32-bit core enhanced by resources for embedded cores defined by the Power ISA, and built on Power Architecture® technology:
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
  - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.

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- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte–4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 256-Kbyte L2 cache/SRAM
  - Flexible configuration
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both.
  - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    - 1, 2, or 4 ways can be configured for stashing only.
  - Eight-way set-associative cache organization (32-byte cache lines)
  - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - Global locking and flash clearing done through writes to L2 configuration registers
  - Instruction and data locks can be flash cleared separately.
  - SRAM features include the following:
    - I/O devices access SRAM regions by marking transactions as snoopable (global).
    - Regions can reside at any aligned location in the memory map.
    - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  - Eight local access windows define mapping within local 36-bit address space.
  - Inbound and outbound ATMUs map to larger external address spaces.
    - Three inbound windows plus a configuration window on PCI and PCI Express
    - Four outbound windows plus default translation for PCI and PCI Express
- DDR/DDR2 memory controller
  - Programmable timing supporting DDR and DDR2 SDRAM
  - 64-bit data interface

  - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
  - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
  - Full ECC support
  - Page mode support
    - Up to 16 simultaneous open pages for DDR
    - Up to 32 simultaneous open pages for DDR2
  - Contiguous or discontiguous memory mapping
  - Sleep mode support for self-refresh SDRAM
  - On-die termination support when using DDR2
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5-V SSTL_2 compatible I/O (1.8-V SSTL_1.8 for DDR2)
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high resolution timers/counters that can generate interrupts
  - Supports a variety of other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing.
  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
  - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 2048 bits
    - Elliptic curve cryptography with F_2m and F(p) modes and programmable field size up to 511 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES

  - Two key (K1, K2, K1) or three key (K1, K2, K3)
  - ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU—message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU—Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications

- Dual I^2C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data bus operating at up to 133 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
  - Two protocol engines available on a per chip select basis:

  - General-purpose chip select machine (GPCM)
  - Three user programmable machines (UPMs)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)

- Two enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Two IEEE Std 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, and IEEE 802.3ab-compliant controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, SGMII, and RGMII.
    - 10/100 Mbps full- and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII.
  - Flexible configuration for multiple PHY interface configurations.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
    - Up to 16 exact-match MAC addresses supported

  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- PCI controller
  - PCI 2.2 compatible
  - One 32-bit PCI port with support for speeds from 16 to 66 MHz
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible
  - Selectable hardware-enforced coherency

- Three PCI Express interfaces
  - Two ×4 link width interfaces and one ×1 link width interface
  - PCI Express 1.0a compatible
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing
  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Traffic class 0 only
  - Full 64-bit decode with 32-bit wide windows
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compliant, JTAG boundary scan
- 783 FC-PBGA package

Figure 1 shows the MPC8544E block diagram.

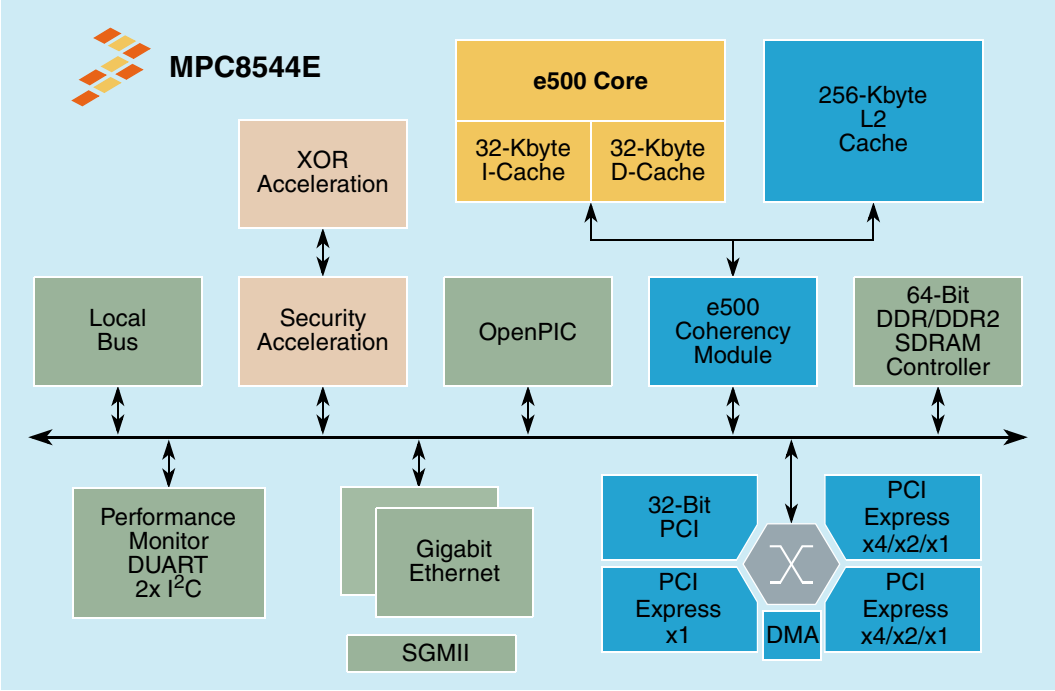


Figure 1. MPC8544E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8544E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage	AV_{DD}	–0.3 to 1.1	V	—
Core power supply for SerDes transceivers	SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers	XV_{DD}	–0.3 to 1.1	V	—

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD} (eTSEC1)	–0.3 to 3.63 –0.3 to 2.75	V	—
		TV_{DD} (eTSEC3)	–0.3 to 3.63 –0.3 to 2.75	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	2
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	2
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause.
2. (M,L,O)V_{IN}, and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for this device. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 ± 50 mV	V	—
PLL supply voltage	AV_{DD}	1.0 ± 50 mV	V	1
Core power supply for SerDes transceivers	SV_{DD}	1.0 ± 50 mV	V	—
Pad power supply for SerDes transceivers	XV_{DD}	1.0 ± 50 mV	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	2

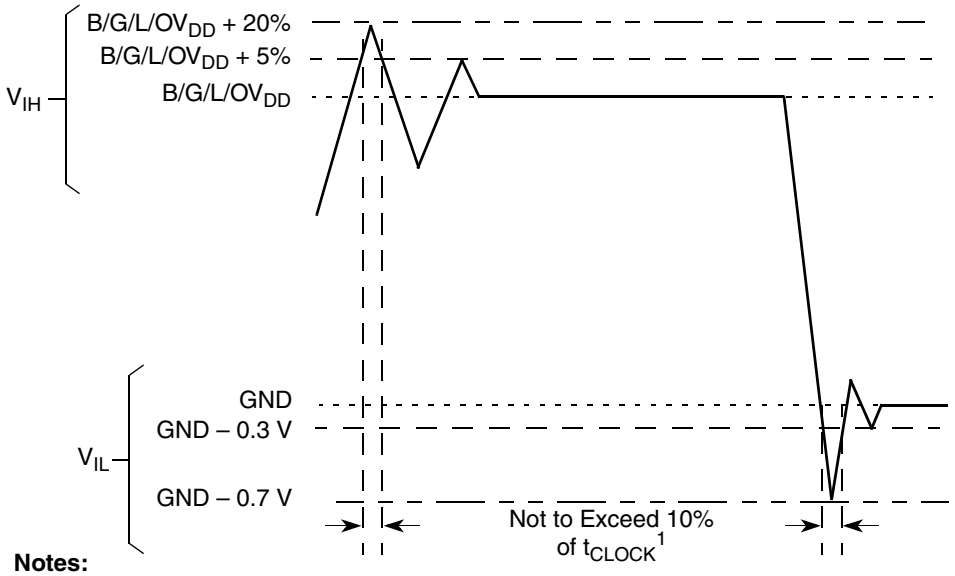
Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV_{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV_{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, PCI Express, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	3
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	5
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	2
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	2
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	5
	PCI, Local bus, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	3
Junction temperature range		T_j	0 to 105	°C	—

Notes:

1. This voltage is the input to the filter discussed in Section 21.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** T/LV_{IN} must not exceed T/ LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8544E.



Notes:
1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
2. Please note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in Section 4.2.2.3 of the *PCI 2.2 Local Bus Specifications*.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$

The core voltage must always be provided at nominal 1.0 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45 (default) 45 (default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	42 (default)		
DDR signal	20	GV_{DD} = 2.5 V	—
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V	—
TSEC signals	42	LV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV_{DD} = 3.3 V	—
I^2C	150	OV_{DD} = 3.3 V	—

Notes:
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI_GNT1}}$ signal at reset.

2.2 Power Sequencing

The device requires its power rails to be applied in specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, LV_{DD}, SV_{DD}, OV_{DD}, TV_{DD}, XV_{DD}
2. GV_{DD}

Note that all supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, then the sequencing for GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

3 Power Characteristics

The estimated typical core power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in Table 4.

Table 4. MPC8544ECore Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD} (V)	Junction Temperature (°C)	Power (W)	Notes
Typical	667	333	1.0	65	2.6	1, 2
Thermal				105	4.5	1, 3
Maximum					7.15	1, 4
Typical	800	400	1.0	65	2.9	1, 2
Thermal				105	4.8	1, 3
Maximum					7.35	1, 4
Typical	1000	400	1.0	65	3.6	1, 2
Thermal				105	5.3	1, 3
Maximum					7.5	1, 4
Typical	1067	533	1.0	65	3.9	1, 2
Thermal				105	6.0	1, 3
Maximum					7.7	1, 4

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.

4 Input Clocks

This section contains the following subsections:

- Section 4.1, “System Clock Timing”
- Section 4.2, “Real-Time Clock Timing”
- Section 4.3, “eTSEC Gigabit Reference Clock Timing”
- Section 4.4, “Platform to FIFO Restrictions”
- Section 4.5, “Other Input Clocks”

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8544E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	—
SYSCLK jitter	—	—	—	±150	ps	3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. This represents the total input jitter—short- and long-term.
4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8544E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8544E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:
1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

4.2 Real-Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2 × the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8544E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD}, TV_{DD} = 2.5 V LV_{DD}, TV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TV_{DD} = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.7.4, “RGMII and RTBI AC Timing Specifications,” for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency ≤ platform clock frequency ÷ 4.2

For example, if the platform frequency is 533 MHz, the FIFO Tx/Rx clock frequency should be no more than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency ≤ platform clock frequency ÷ 3.2

For example, if the platform frequency is 533 MHz, the FIFO Tx/Rx clock frequency should be no more than 167 MHz.

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8544E. Table 8 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications[1]

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:
1. SYSCLK is the primary clock input for the MPC8544E.

Table 9 provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
Core and platform PLL lock times	—	100	μs	—
Local bus PLL	—	50	μs	—
PCI bus lock time	—	50	μs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8544E. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 10 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8544E when GV_{DD}(typ) = 1.8 V.

Table 10. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.26	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.24	V	—
Output high current (V_{OUT} = 1.26 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.33 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

Table 11 provides the DDR2 I/O capacitance when GV_{DD}(typ) = 1.8 V.

Table 11. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 12 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 12. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.3	V	—
Output high current (V_{OUT} = 1.8 V)	I_{OH}	–16.2	—	mA	—

Table 12. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current (V_{OUT} = 0.42 V)	I_{OL}	16.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

Table 13 provides the DDR I/O capacitance when GV_{DD}(typ) = 2.5 V.

Table 13. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the current draw characteristics for MV_{REF}.

Table 14. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 15 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 1.8 V.

Table 15. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 16 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5$ V.

Table 16. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

Table 17 provides the input AC timing specifications for the DDR SDRAM interface.

Table 17. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		3
400 MHz		–365	365		—
333 MHz		–390	390		—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}. See Figure 3.
3. Maximum DDR1 frequency is 400 MHz.

Figure 3 shows the DDR SDRAM input timing diagram.

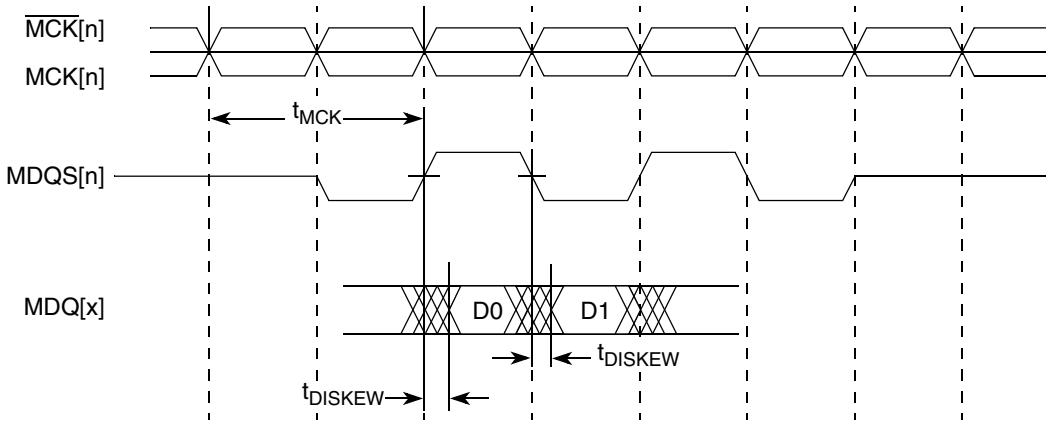


Figure 3. DDR SDRAM Input Timing Diagram (t_{DISKEW})

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 18 provides the output AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		538	—		7
400 MHz		700	—		—
333 MHz		900	—		—
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		538	—		7
400 MHz		700	—		—
333 MHz		900	—		—
MDQS preamble	t_{DDKHMP}	0.75 x tMCK	—	ns	6

Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQS postamble	t_{DDKHME}	0.4 x tMCK	0.6 x tMCK	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MPC8544E PowerQUICC III Integrated Communications Processor Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

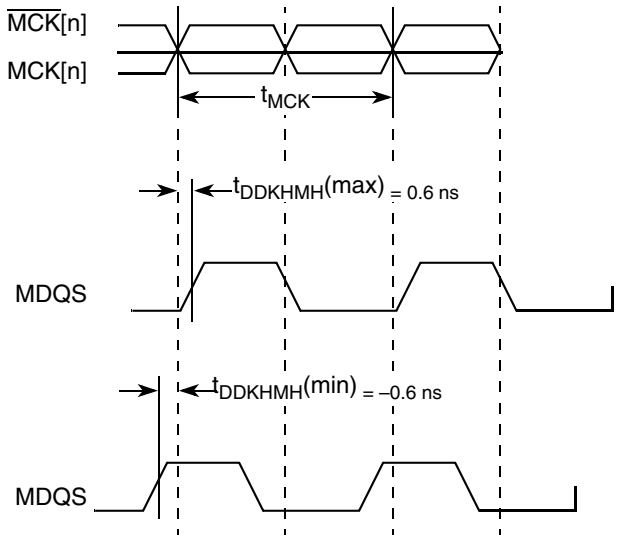


Figure 4. Timing Diagram for t_{DDKHMH}

Figure 5 shows the DDR SDRAM output timing diagram.

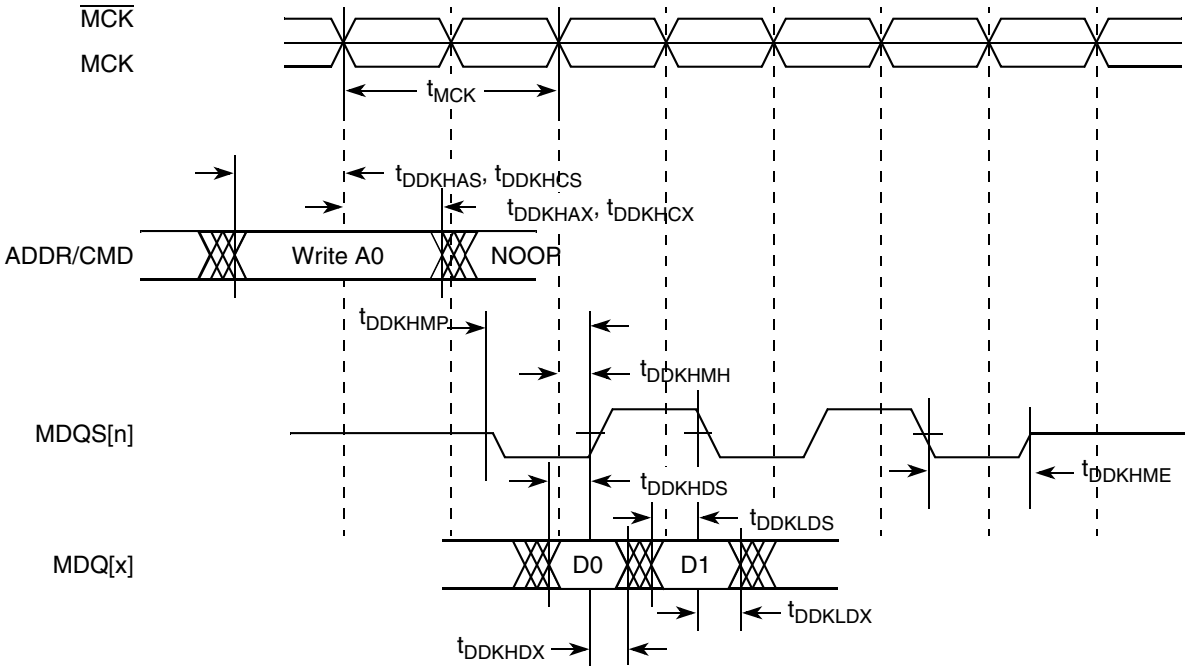


Figure 5. DDR and DDR2 SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

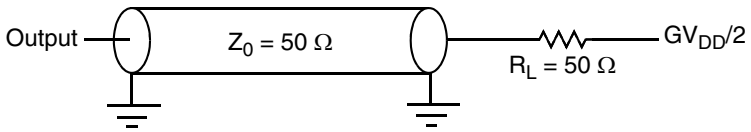


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8544E.

7.1 DUART DC Electrical Characteristics

Table 19 provides the DC electrical characteristics for the DUART interface.

Table 19. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 19. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 20 provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Notes:
1. CCB clock refers to the platform clock.
2. Actual attainable baud rate will be limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—SGMII/GMII/MII/TBI/RGMII/RTBI/RMII/FIFO Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), 8-bit FIFO interface (FIFO), serial gigabit media independent interface (SGMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The 8-bit FIFO interface can operate at 3.3 or 2.5 V. The RGMII and RTBI interfaces are defined for 2.5 V, while the MII, GMII, TBI, and RMII interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The SGMII interfaces follow the *Serial Gigabit Media-Independent Interface (SGMII) Specification Version 1.8*. The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical

Characteristics.”

8.2 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RTBI, RMII, and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The potential applied to the input of a GMII, MII, TBI, RTBI, RMII, and FIFO receiver may exceed the potential of the receiver’s power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 21. GMII, MII, TBI, RMII and FIFO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.5	V	—
Input high voltage	V_{IH}	1.95	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 22. GMII, MII, RMII, RGMII, RTBI, TBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.7	V	—
Input current (V_{IN} = 0, V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IN}	—	±15	μA	1, 2, 3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes 2 interface of MPC8544E as shown in Figure 7, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SGND_SRDS2 (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 7.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 21.5, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and SD2_REF_CLK pins.

8.3.1 AC Requirements for SGMII SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$

Table 23 lists the SGMII SerDes reference clock AC requirements. Please note that SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 23. SD2_REF_CLK and $\overline{\text{SD2_REF_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10 (8)	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Note:
1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected via cfg_srds_sgmii_refclk during POR.

8.3.2 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 24 and Table 25 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2_TX}}$[n]) as depicted in Figure 8.

Table 24. DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD_SRDS2}	0.95	1.0	1.05	V	—
Output high voltage	V_{OH}	—	—	V_{OS}-max + $\lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	V_{OL}	V_{OS}-min –$\lvert V_{OD}\rvert_{-max}/2$	—	—	mV	
Output ringing	V_{RING}	—	—	10	%	—

Table 24. DC Transmitter Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage[2,3,5]	$\|V_{OD}\|$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	577.5	mV	1, 4
Output impedance (single ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between 0 and 1	$\Delta\|V_{OD}\|$	—	—	25	mV	—
Change in V_{OS} between 0 and 1	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Notes:

1. This will not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD2_TXn} - V_{\overline{SD2_TXn}}|$. $|V_{OD}|$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{OD}|$.
3. The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**CD** (for SerDes 2 lane 2 and 3) bit field of MPC8544E SerDes 2 control register 1:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude—power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in this table.
4. V_{OS} is also referred to as output common mode voltage.
5. The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD_SRDS2\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} = 500 mV), SerDes2 transmitter is terminated with 100-Ω differential load between SD2_TX[n] and SD2_TX[n].

Figure 7 shows an example of a 4-wire AC-coupled SGMII serial link connection.

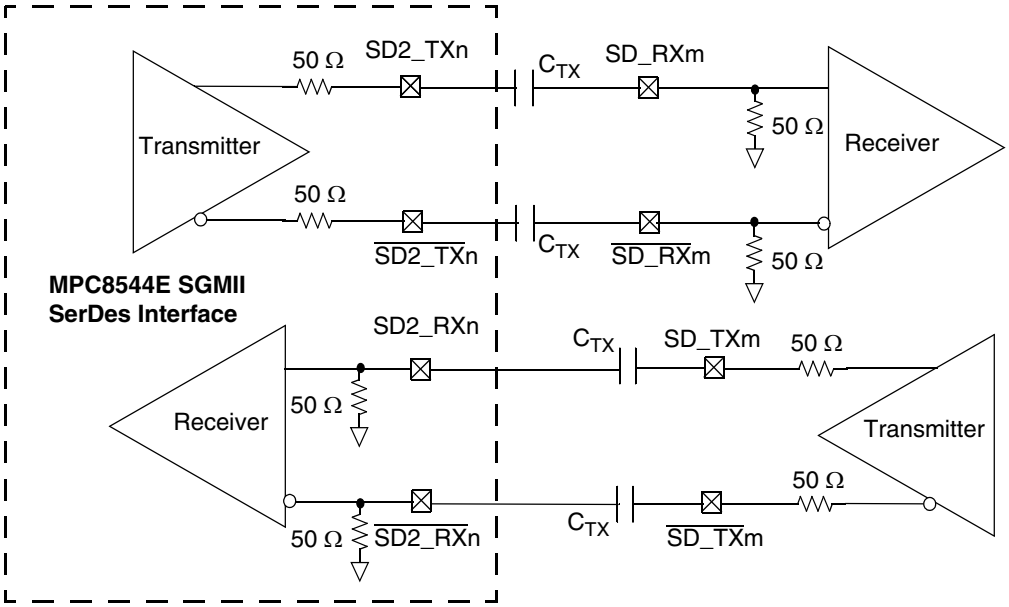


Figure 7. 4-Wire AC-Coupled SGMII Serial Link Connection Example

Figure 8 shows an SGMII transmitter DC measurement circuit.

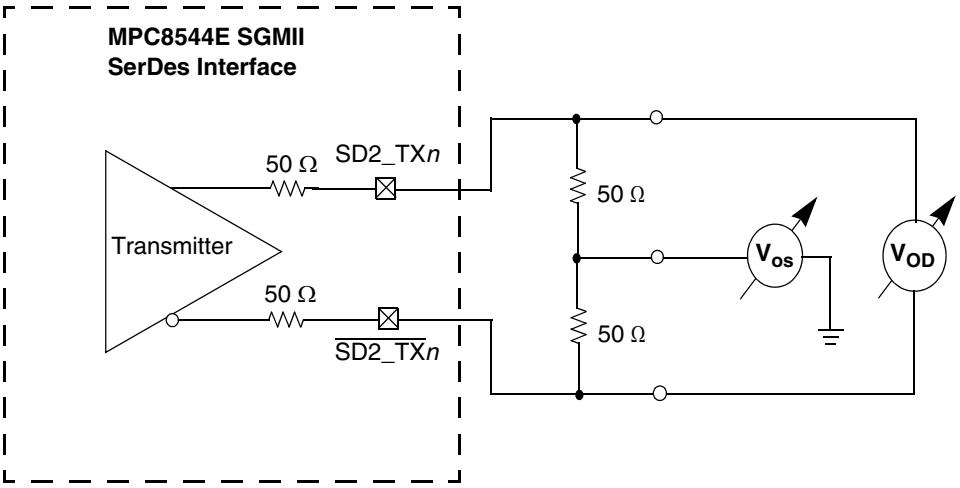


Figure 8. SGMII Transmitter DC Measurement Circuit

Table 25 shows the DC receiver electrical characteristics.

Table 25. DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD_SRDS2}	0.9	1.0	1.05	V	—
DC input voltage range	—	—	—	—	—	1

Table 25. DC Receiver Electrical Characteristics (continued)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Input differential voltage	LSTS = 0	V_{rx_diffpp}	100	—	1200	mV	2, 4
	LSTS = 1		175	—			
Loss of signal threshold	LSTS = 0	VI_{os}	30	—	100	mV	3, 4
	LSTS = 1		65	—	175		
Input AC common mode voltage		V_{cm_acpp}	—	—	100	mV	5.
Receiver differential input impedance		Zrx_diff	80	—	120	Ω	—
Receiver common mode input impedance		Zrx_cm	20	—	35	Ω	—
Common mode input voltage		Vcm	xcorevss	—	xcorevss	V	6

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 17.4.3, "Differential Receiver (RX) Input Specifications," for further explanation.
4. The LSTS shown in this table refers to the LSTS**CD** bit field of MPC8544E SerDes 2 control register 1.
5. $V_{CM_ACp\text{-}p}$ is also referred to as peak-to-peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

8.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2_RX}}$[n]) as depicted in Figure 10, respectively.

8.4.1 SGMII Transmit AC Timing Specifications

Table 26 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 26. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit interval	U_I	799.92	800	800.08	ps	2
V_{OD} fall time (80%–20%)	t_{fall}	50	—	120	ps	—
V_{OD} rise time (20%–80%)	t_{rise}	50	—	120	ps	—

Notes;
1. Source synchronous clock is not supported.
2. Each UI value is 800 ps ± 100 ppm.

8.4.2 SGMII Receive AC Timing Specifications

Table 27 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 9 shows the SGMII receiver input compliance mask eye diagram.

Table 27. SGMII Receiver AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Sinusoidal jitter tolerance	Jsin	0.1	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	5	—	200	nF	3

Notes:
1. Measured at receiver.
2. Each UI value is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.

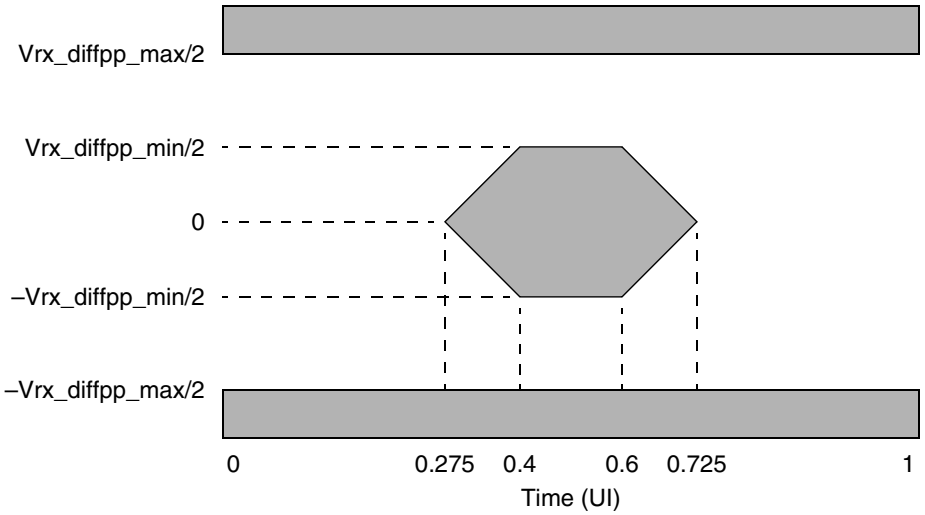


Figure 9. Receive Input Compliance Mask

Figure 10 provides the AC test load for SGMII.

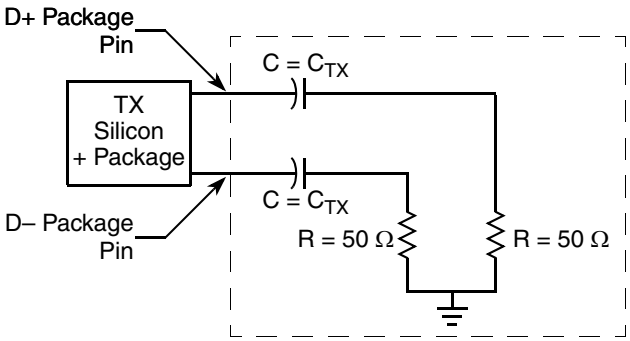


Figure 10. SGMII AC Test/Measurement Load

8.5 FIFO, GMII,MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.5.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n* TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver.

A summary of the FIFO AC specifications appears in Table 28 and Table 29.

Table 28. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TX_CLK, GTX_CLK clock period	t_{FIT}	—	8.0	—	ns	—
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%	—
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps	—
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns	—

Table 28. FIFO Mode Transmit AC Timing Specification (continued)

(continued)At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns	—
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns	1

Note:

1. Data valid t_{FITDV} to GTX_CLK Min setup time is a function of clock period and max hold time. (Min setup = Cycle time – Max hold).

Table 29. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{FIR}	—	8.0	—	ns	—
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%	—
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns	—
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t_{FIRDX}	0.5	—	—	ns	—

Timing diagrams for FIFO appear in Figure 11 and Figure 12.

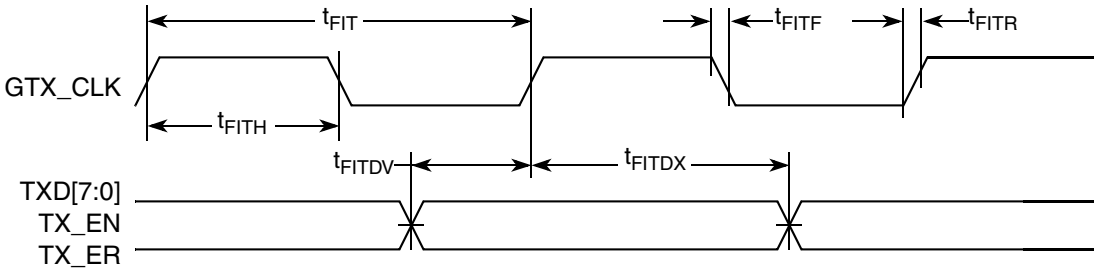


Figure 11. FIFO Transmit AC Timing Diagram

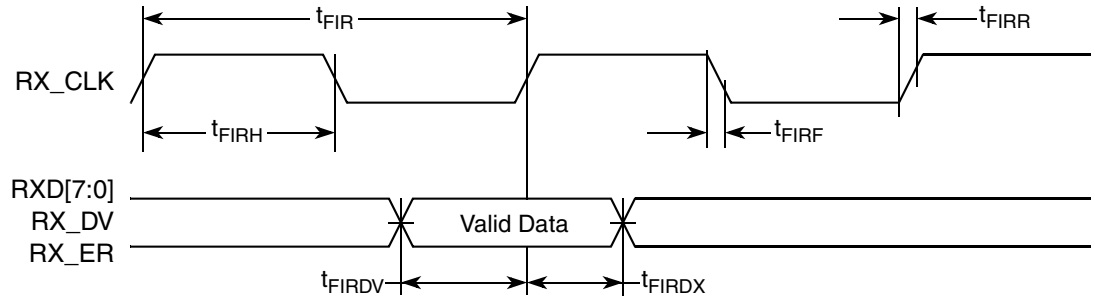


Figure 12. FIFO Receive AC Timing Diagram

8.5.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.5.2.1 GMII Transmit AC Timing Specifications

Table 30 provides the GMII transmit AC timing specifications.

Table 30. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.2	—	5.0	ns	2
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid t_{GTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).

Figure 13 shows the GMII transmit AC timing diagram.

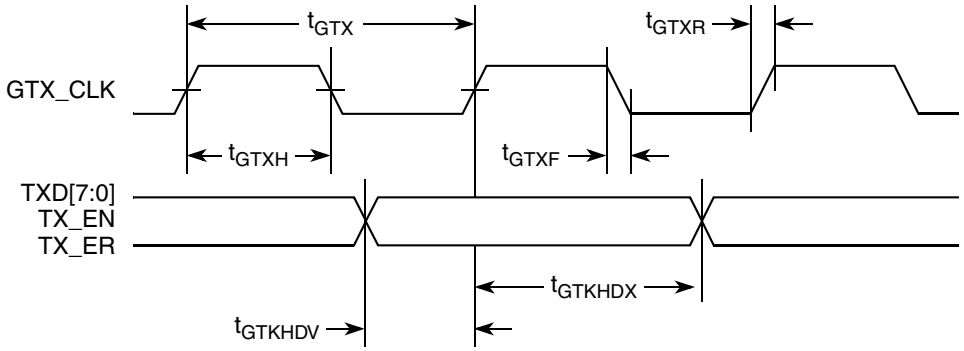


Figure 13. GMII Transmit AC Timing Diagram

8.5.2.2 GMII Receive AC Timing Specifications

Table 31 provides the GMII receive AC timing specifications.

Table 31. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{GRX}	—	8.0	—	ns	—
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	65	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t_{GRDXKH}	0.5	—	—	ns	—
RX_CLK clock rise (20%–80%)	t_{GRXR}	—	—	1.0	ns	—
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 provides the AC test load for eTSEC.

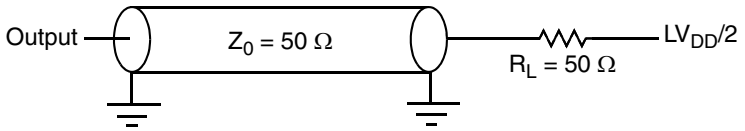


Figure 14. eTSEC AC Test Load

Figure 15 shows the GMII receive AC timing diagram.

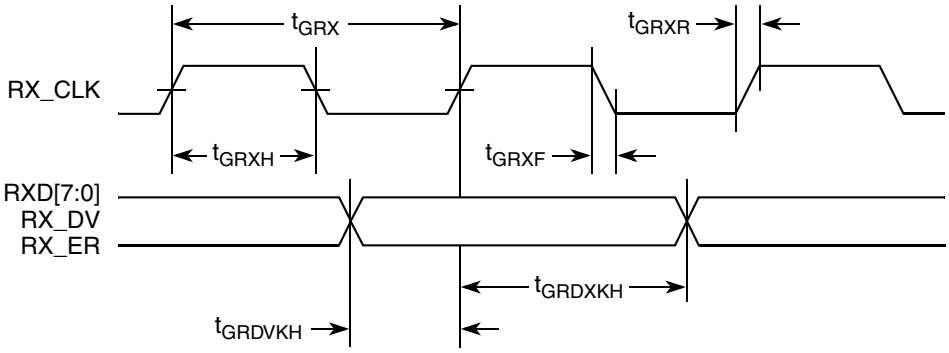


Figure 15. GMII Receive AC Timing Diagram

8.6 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.6.1 MII Transmit AC Timing Specifications

Table 32 provides the MII transmit AC timing specifications.

Table 32. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 16 shows the MII transmit AC timing diagram.

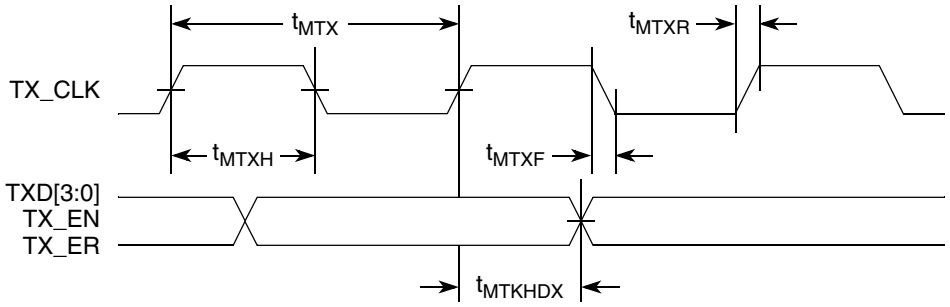


Figure 16. MII Transmit AC Timing Diagram

8.6.2 MII Receive AC Timing Specifications

Table 33 provides the MII receive AC timing specifications.

Table 33. MII Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns	—
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns	—
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	—

Table 33. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 17 provides the AC test load for eTSEC.

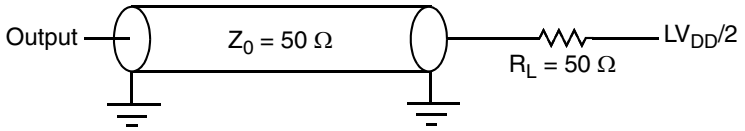


Figure 17. eTSEC AC Test Load

Figure 18 shows the MII receive AC timing diagram.

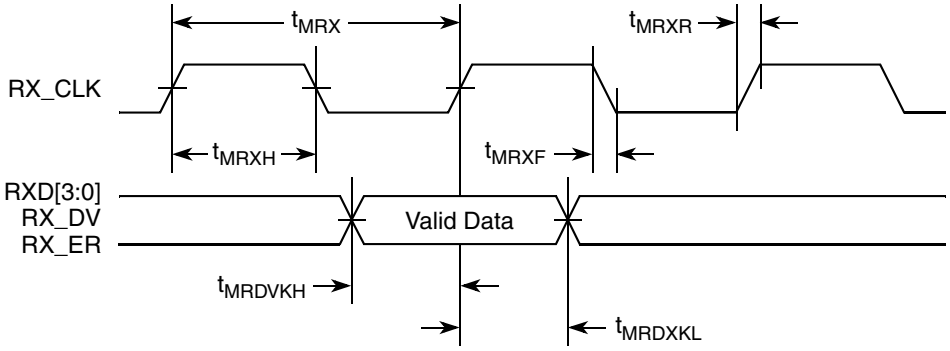


Figure 18. MII Receive AC Timing Diagram

8.7 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.7.1 TBI Transmit AC Timing Specifications

Table 34 provides the TBI transmit AC timing specifications.

Table 34. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK to TCG[9:0] delay time	t_{TTKHDX}	0.2	—	5.0	ns	2
GTX_CLK rise (20%–80%)	t_{TTXR}	—	—	1.0	ns	—
GTX_CLK fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid t_{TTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).

Figure 19 shows the TBI transmit AC timing diagram.

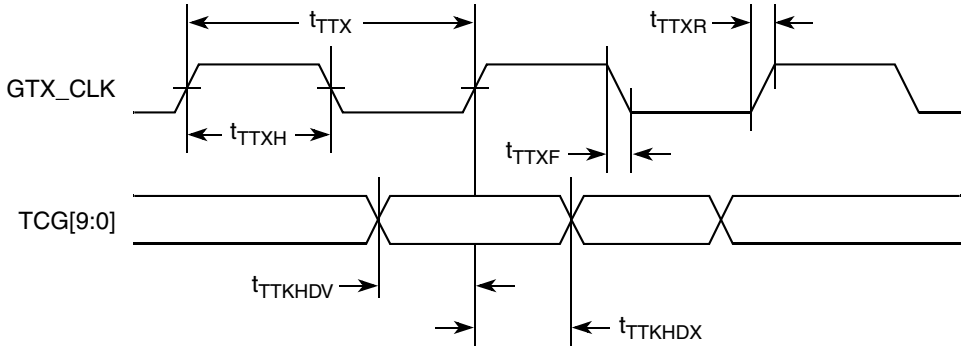


Figure 19. TBI Transmit AC Timing Diagram

8.7.2 TBI Receive AC Timing Specifications

Table 35 provides the TBI receive AC timing specifications.

Table 35. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
PMA_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns	—

Table 35. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	—
PMA_RX_CLK to RCG[9:0] hold time	t_{TRDXKH}	1.5	—	—	ns	—
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR}	0.7	—	2.4	ns	—
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF}	0.7	—	2.4	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).

Figure 20 shows the TBI receive AC timing diagram.

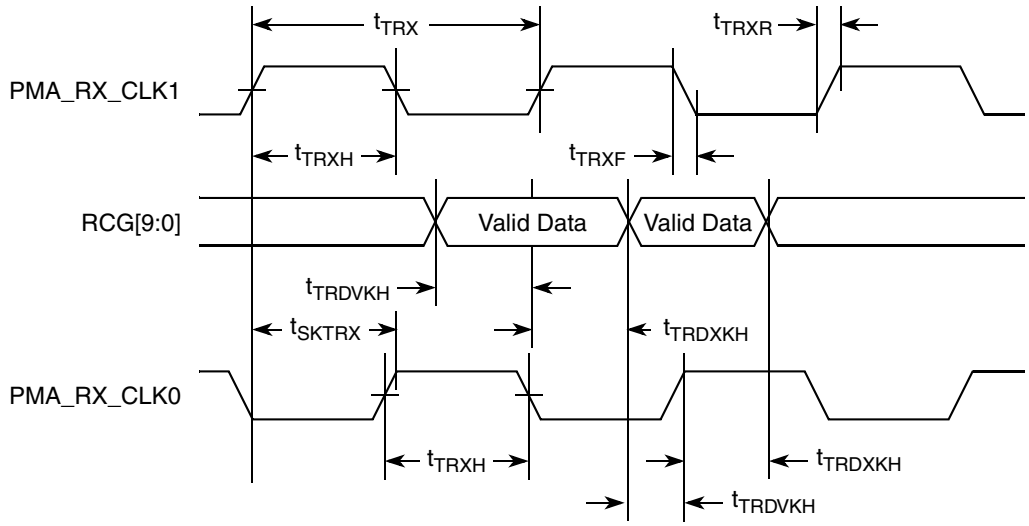


Figure 20. TBI Receive AC Timing Diagram

8.7.3 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC*n*_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 36.

Table 36. TBI Single-Clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns	—
RX_CLK duty cycle	t_{TRRH}	40	50	60	%	—
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns	—
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns	—
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns	—
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns	—

A timing diagram for TBI receive appears in Figure 21.

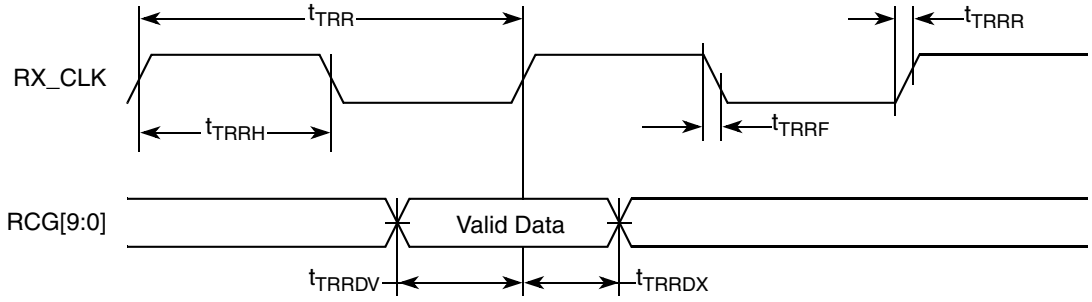


Figure 21. TBI Single-Clock Mode Receive AC Timing Diagram

8.7.4 RGMII and RTBI AC Timing Specifications

Table 37 presents the RGMII and RTBI AC timing specifications.

Table 37. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.8	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—

Table 37. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by design.

Figure 22 shows the RGMII and RTBI AC timing and multiplexing diagrams.

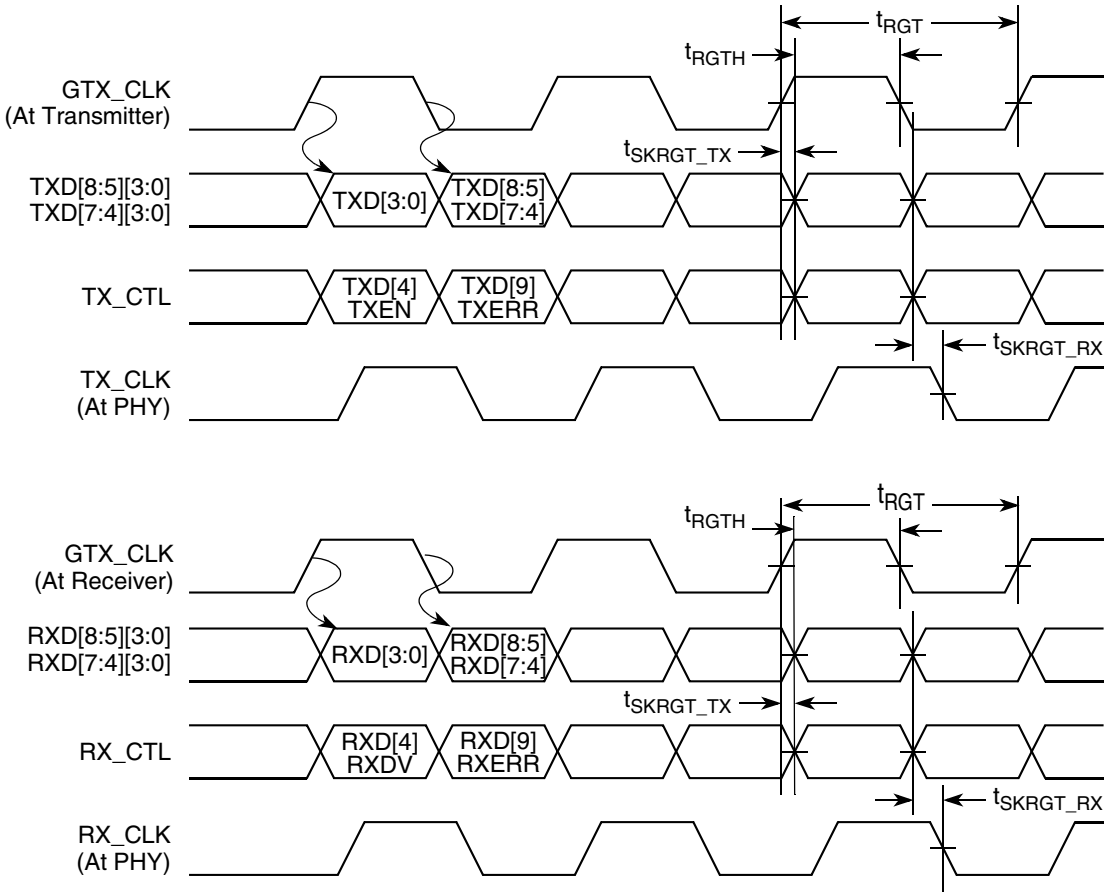


Figure 22. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.7.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.7.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 38.

Table 38. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t_{RMTH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 23 shows the RMII transmit AC timing diagram.

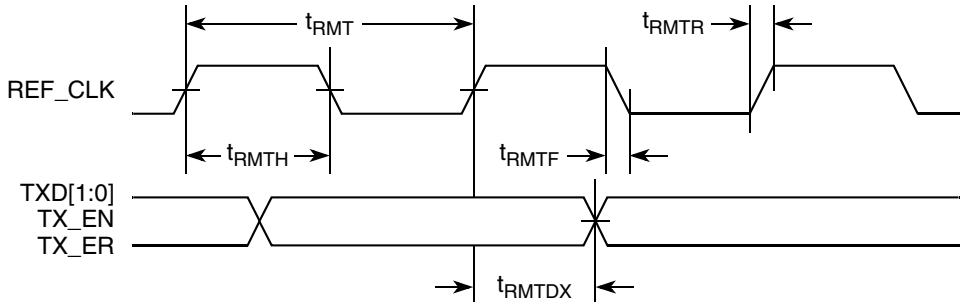


Figure 23. RMII Transmit AC Timing Diagram

8.7.5.2 RMII Receive AC Timing Specifications

Table 39 shows the RMII receive AC timing specifications.

Table 39. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t_{RMRH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns	—
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns	—
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 24 provides the AC test load for eTSEC.

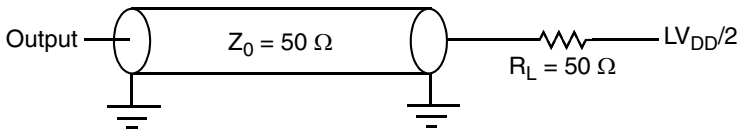


Figure 24. eTSEC AC Test Load

Figure 25 shows the RMII receive AC timing diagram.

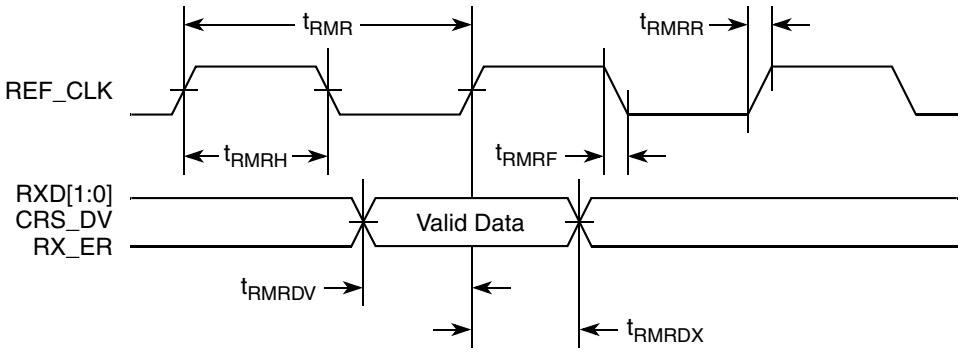


Figure 25. RMII Receive AC Timing Diagram

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC), MII Management."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 40.

Table 40. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage (3.3 V)	OV_{DD}	3.135	3.465	V	—
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	3.60	V	—
Output low voltage (OV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	1.95	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (OV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	—

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

Table 41 provides the MII management AC timing specifications.

Table 41. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb_clk}) - 3$	—	$(16 \times t_{plb_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

Table 41. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
4. t_{plb_clk} is the platform (CCB) clock.

Figure 26 shows the MII management AC timing diagram.

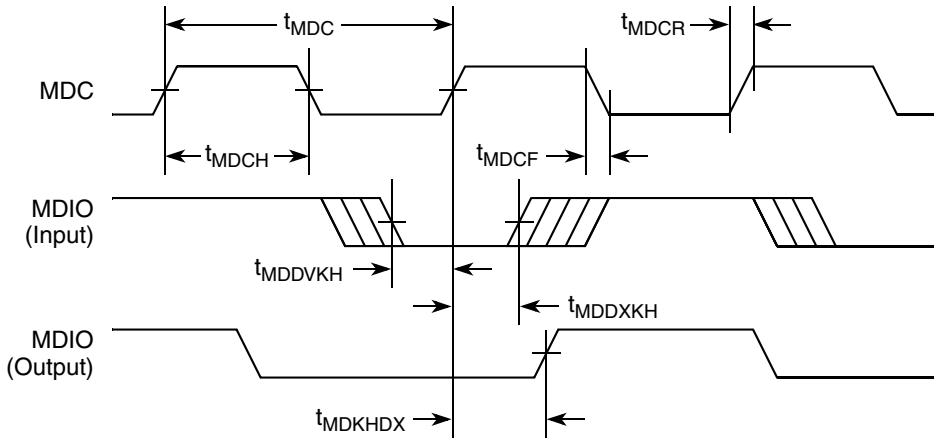


Figure 26. MII Management Interface Timing Diagram

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8544E.

10.1 Local Bus DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 42. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BOV_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 43 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 43. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.7	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±15	μA	1
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 44 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 1.8 V DC.

Table 44. Local Bus DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	1.3	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.6	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±15	μA	1

Table 44. Local Bus DC Electrical Characteristics (1.8 V DC) (continued)

Parameter	Symbol	Min	Max	Unit	Notes
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.45	V	—

10.2 Local Bus AC Electrical Specifications

Table 45 describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V. For information about the frequency range of local bus see Section 19.1, "Clock Ranges."

Table 45. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	2.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.85	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.9	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.8	ns	—
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.7	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.7	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5

Table 45. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

Table 46 describes the general timing parameters of the local bus interface at BV_{DD} = 2.5 V.

Table 46. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.8	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.8	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.8	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.8	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5

Table 46. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 2.5-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

Table 47 describes the general timing parameters of the local bus interface at BV_{DD} = 1.8 V DC.

Table 47. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	2.6	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.9	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5

Table 47. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC) (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 1.8-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

Figure 27 provides the AC test load for the local bus.

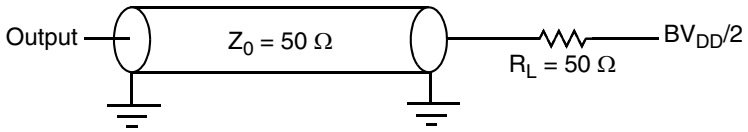


Figure 27. Local Bus AC Test Load

Figure 28 through Figure 33 show the local bus signals.

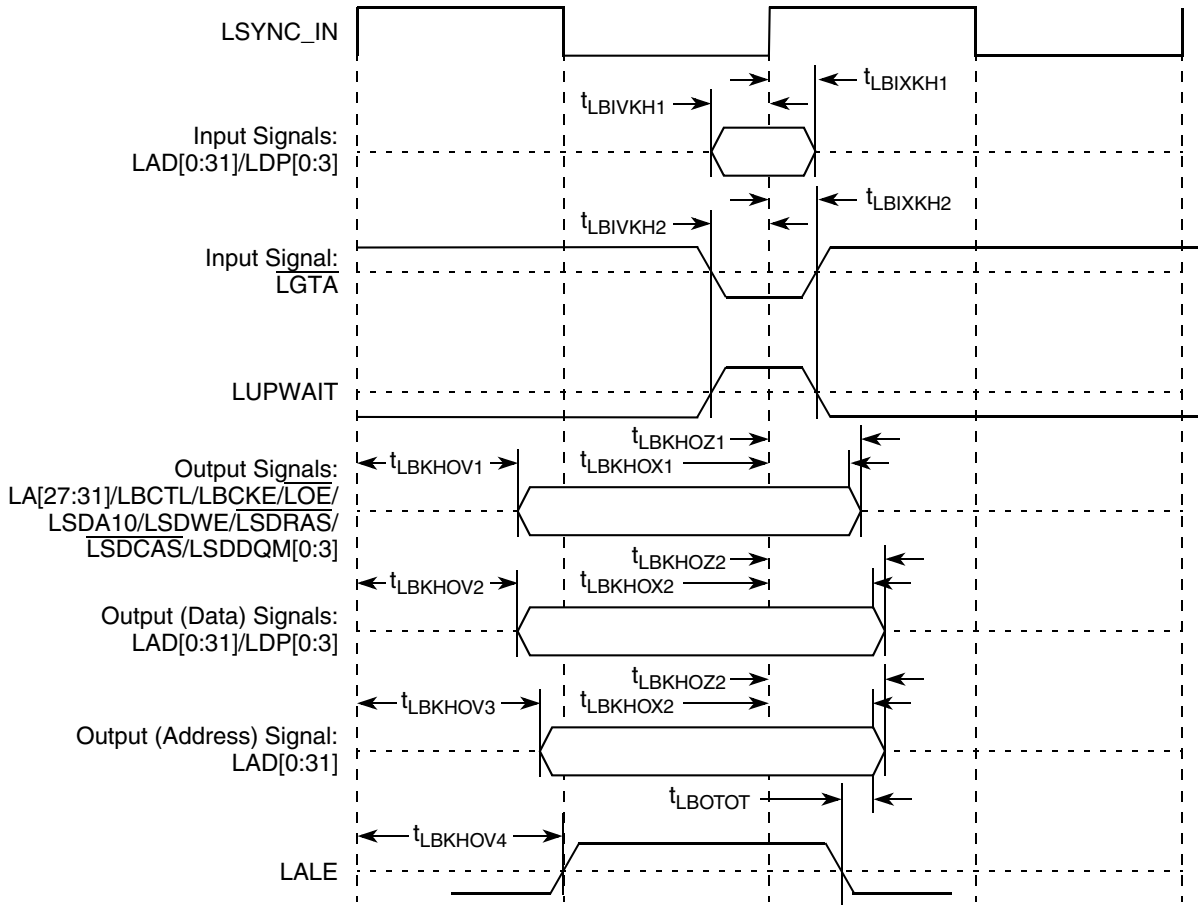


Figure 28. Local Bus Signals (PLL Enabled)

Table 48 describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Table 48. Local Bus General Timing Parameters—PLL Bypassed

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	1.2	4.9	ns	—
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	7.4	—	ns	4, 5
LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.75	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	–0.2	—	ns	4, 5
LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–0.2	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	1.6	ns	—

Table 48. Local Bus General Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	1.6	ns	4
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	1.6	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	–4.1	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	–4.1	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	1.4	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	1.4	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which proceeds LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

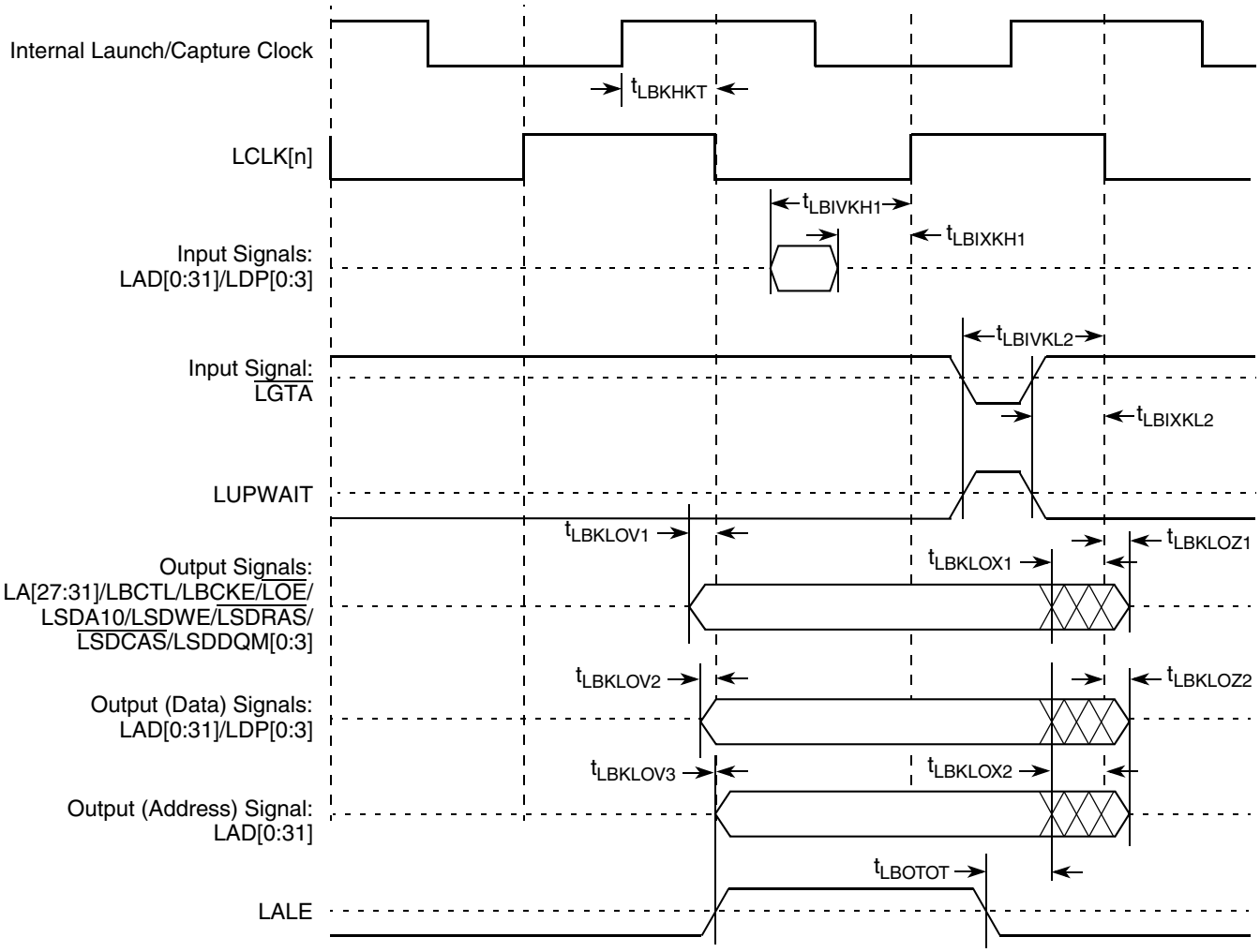


Figure 29. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT}. In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock withe the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

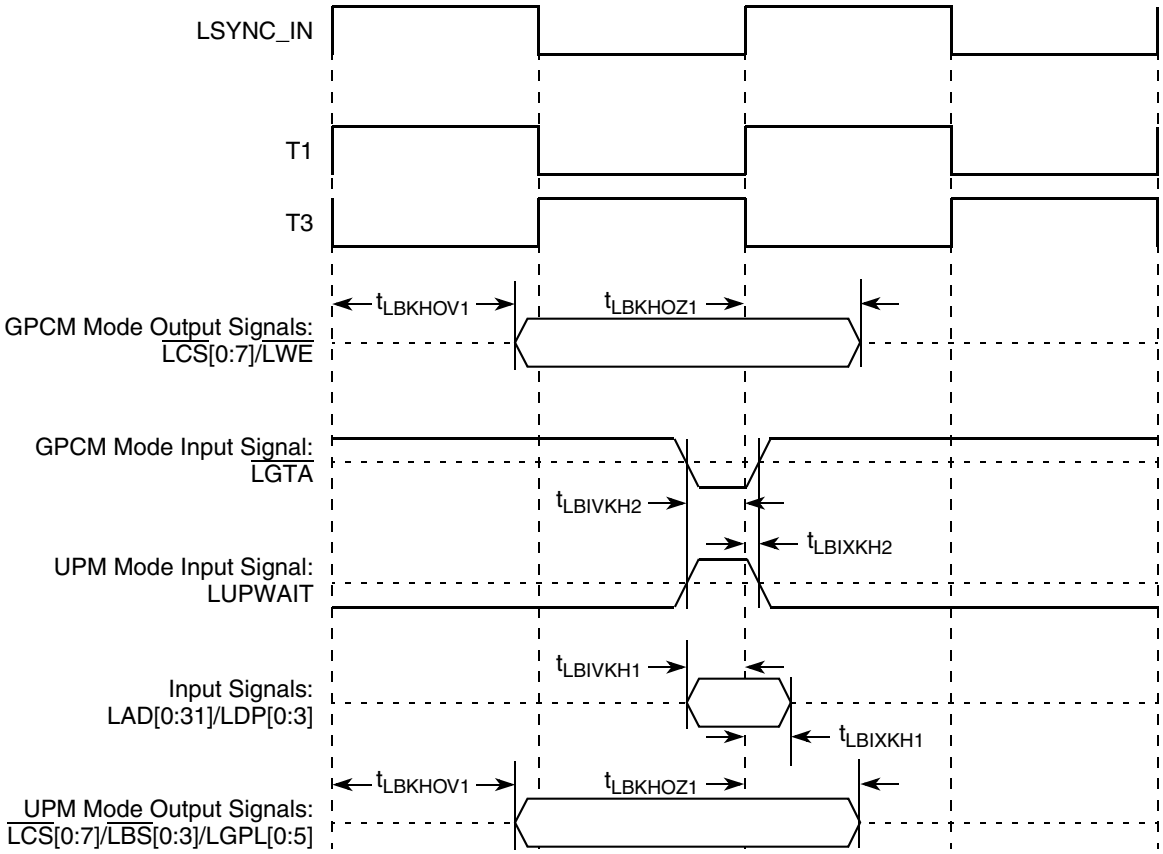


Figure 30. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

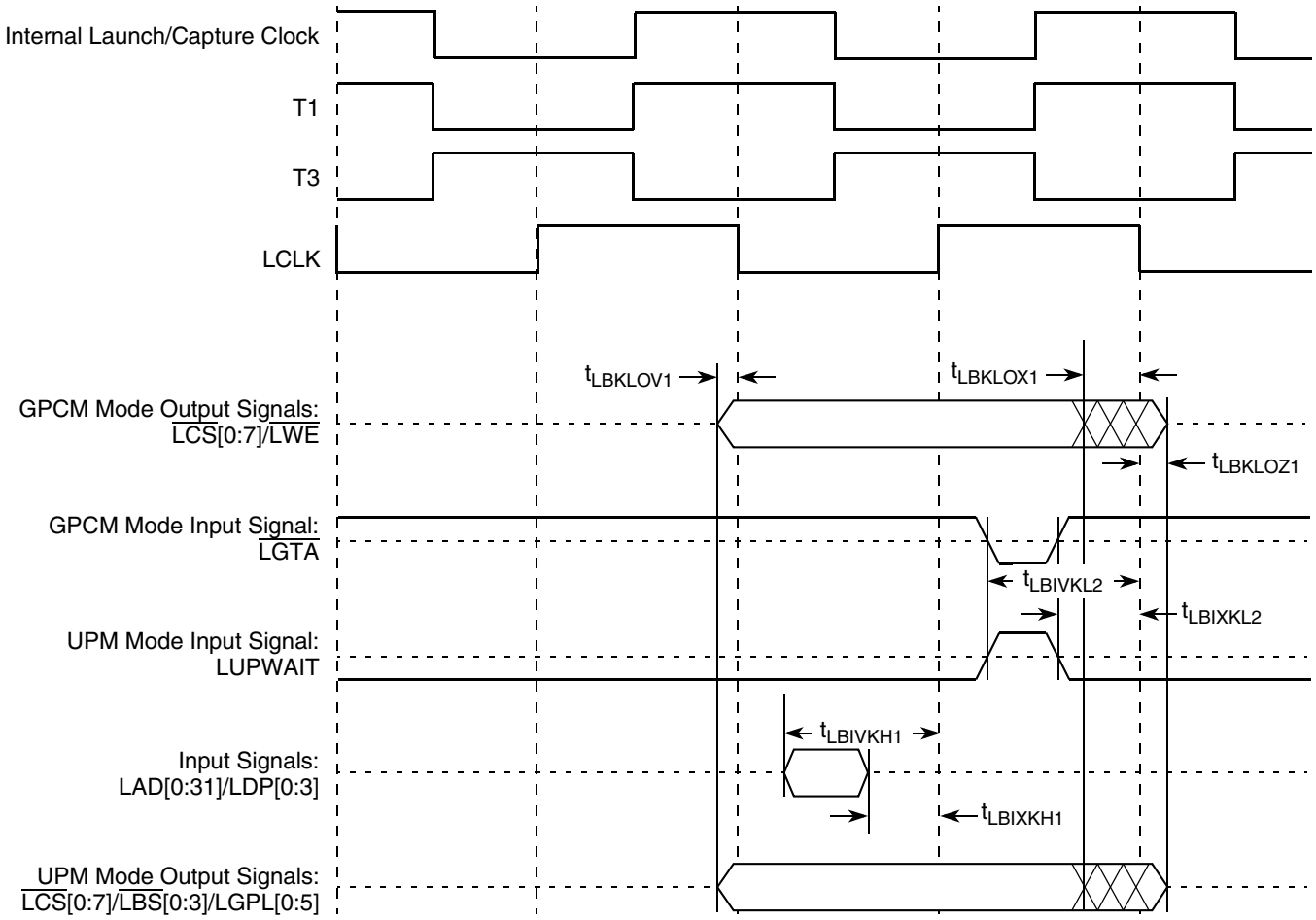


Figure 31. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

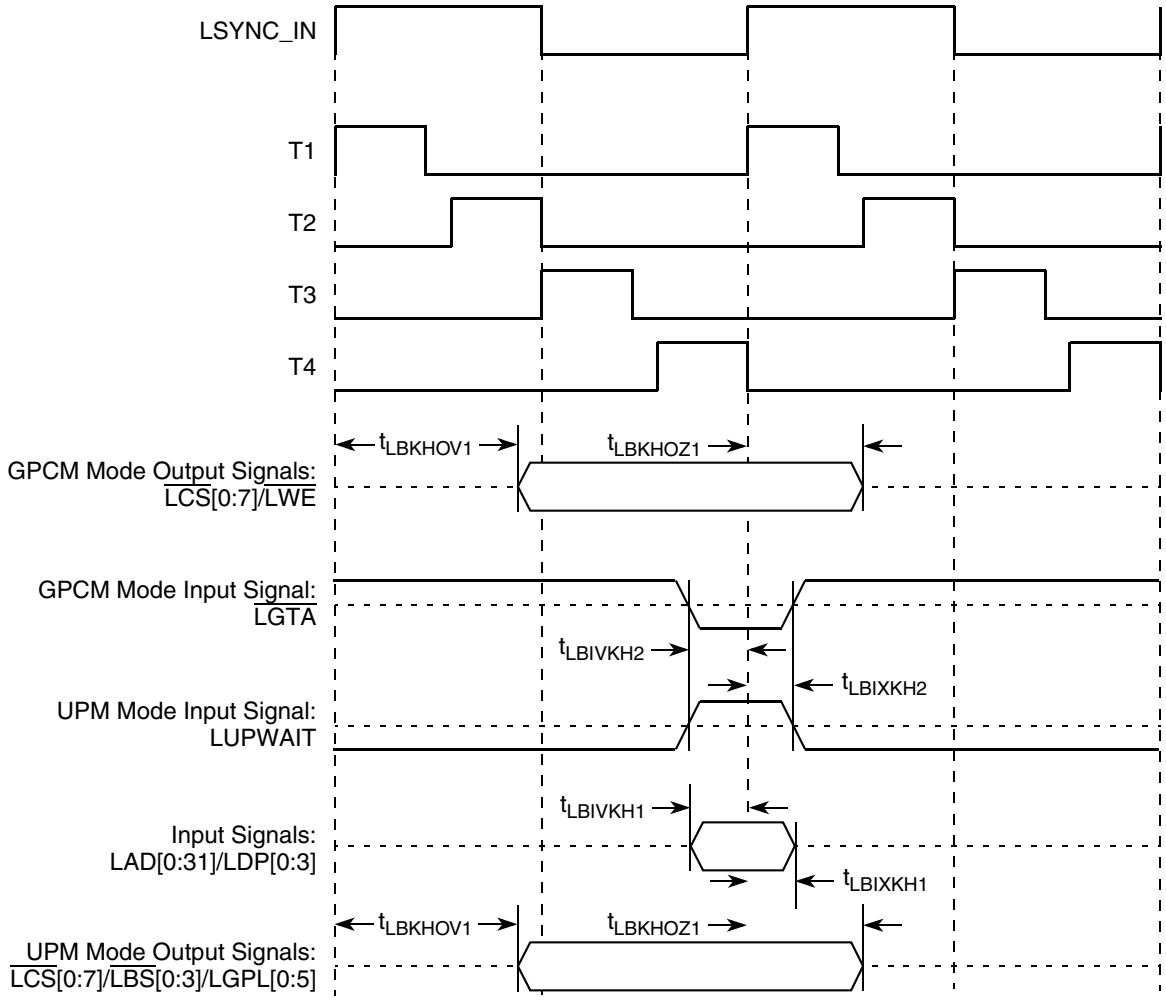


Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

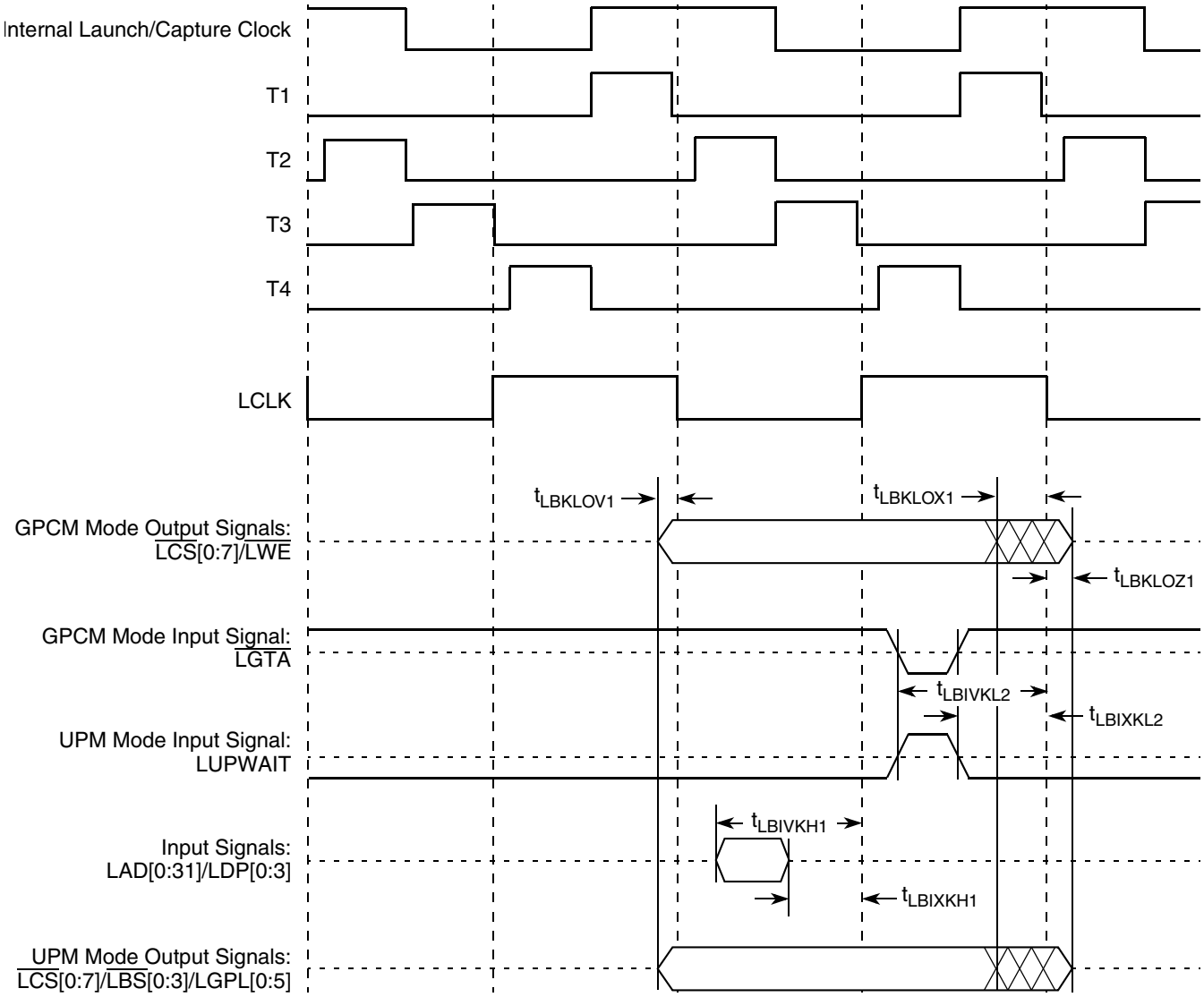


Figure 33. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8544E.

12.1 JTAG DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the JTAG interface.

Table 49. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN}.

12.2 JTAG AC Electrical Specifications

Table 50 provides the JTAG AC timing specifications as defined in Figure 34 through Figure 37.

Table 50. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions (see Table 3).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2.5 4	 — —	ns	5

Table 50. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.

Figure 34 provides the AC test load for TDO and the boundary-scan outputs.

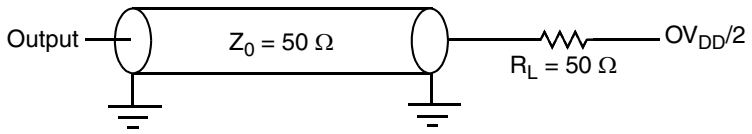


Figure 34. AC Test Load for the JTAG Interface

Figure 35 provides the JTAG clock input timing diagram.

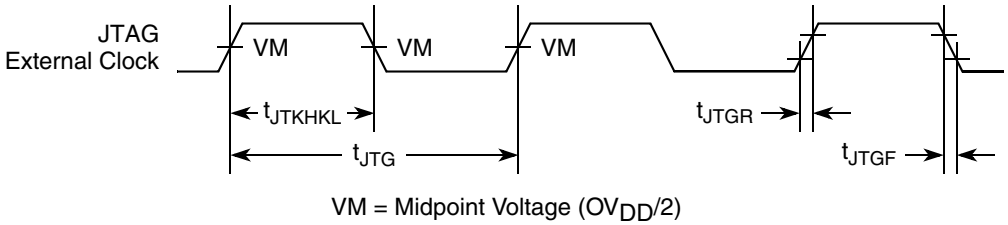


Figure 35. JTAG Clock Input Timing Diagram

Figure 36 provides the $\overline{\text{TRST}}$ timing diagram.

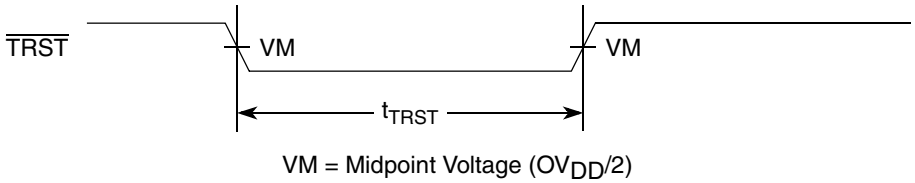


Figure 36. $\overline{\text{TRST}}$ Timing Diagram

Figure 37 provides the boundary-scan timing diagram.

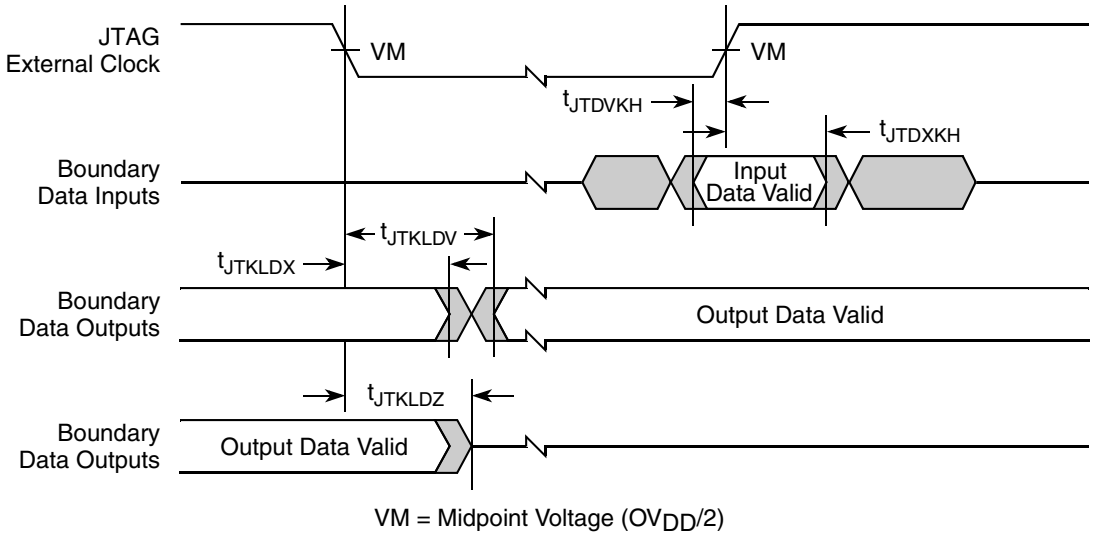


Figure 37. Boundary-Scan Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8544E.

13.1 I²C DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the I²C interfaces.

Table 51. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	3
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8544EPowerQUICC III Integrated Communications Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

13.2 I²C AC Electrical Specifications

Table 52 provides the AC timing parameters for the I²C interfaces.

Table 52. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 51).

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	—
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	2
Data output delay time	t_{I2OVKL}	—	0.9		3
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_b$	300	ns	4
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1\ C_b$	300	ns	4
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8544E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 38 provides the AC test load for the I^2C.

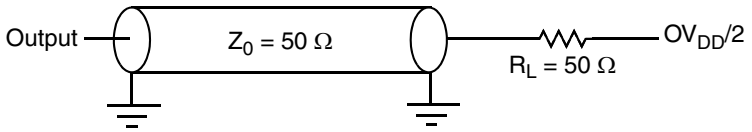


Figure 38. I^2C AC Test Load

Figure 39 shows the AC timing diagram for the I^2C bus.

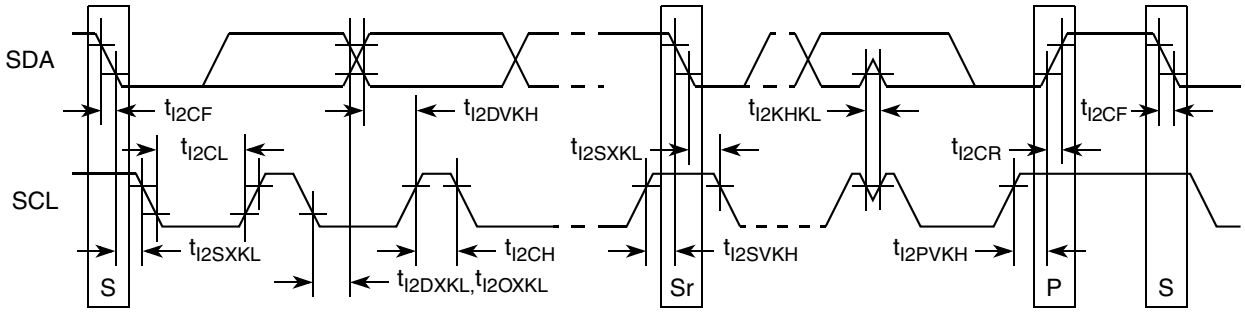


Figure 39. I^2C Bus AC Timing Diagram

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8544E.

14.1 GPIO DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the GPIO interface.

Table 53. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

14.2 GPIO AC Electrical Specifications

Table 54 provides the GPIO input and output AC timing specifications.

Table 54. GPIO Input AC Timing Specifications

Parameter	Symbol	Typ	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 40 provides the AC test load for the GPIO.

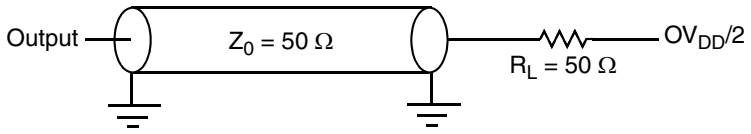


Figure 40. GPIO AC Test Load

15 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8544E.

15.1 PCI DC Electrical Characteristics

Table 55 provides the DC electrical characteristics for the PCI interface.

Table 55. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	2
High-level output voltage (OV_{DD} = min, I_{OH} = –2mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

15.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 56 provides the PCI AC timing specifications at 66 MHz.

Table 56. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	7.4	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.7	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0.5	—	ns	2, 5
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$[9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Fall time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 19, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs.

Figure 41 provides the AC test load for PCI.

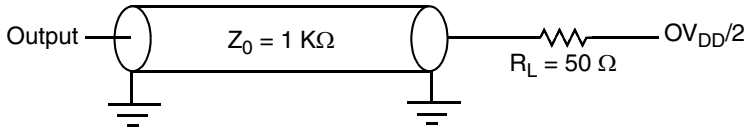


Figure 41. PCI AC Test Load

Figure 42 shows the PCI input AC timing conditions.

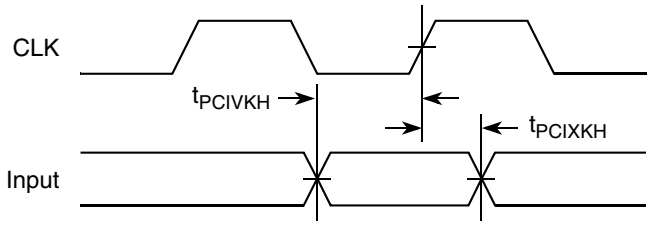


Figure 42. PCI Input AC Timing Measurement Conditions

Figure 43 shows the PCI output AC timing conditions.

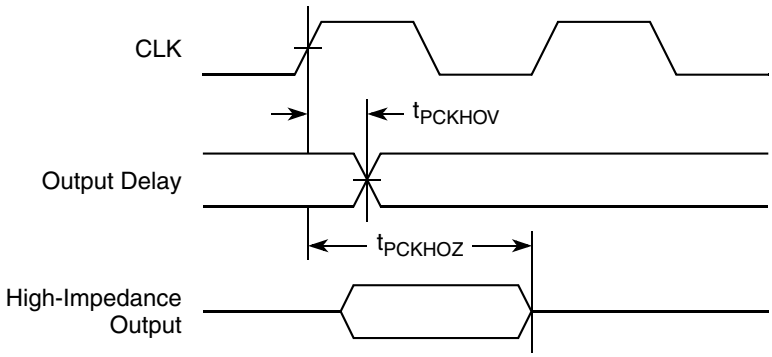


Figure 43. PCI Output AC Timing Measurement Condition

16 High-Speed Serial Interfaces (HSSI)

The MPC8544E features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications.The SerDes1 dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or SGMII application. This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 44 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{_RX}}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. **Differential Waveform**

   The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{_TX}}$, for example) from the non-inverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 44 as an example for differential waveform.

7. **Common Mode Voltage, V_{cm}**

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SDn_TX} + V_{\overline{SDn_TX}} = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasions.

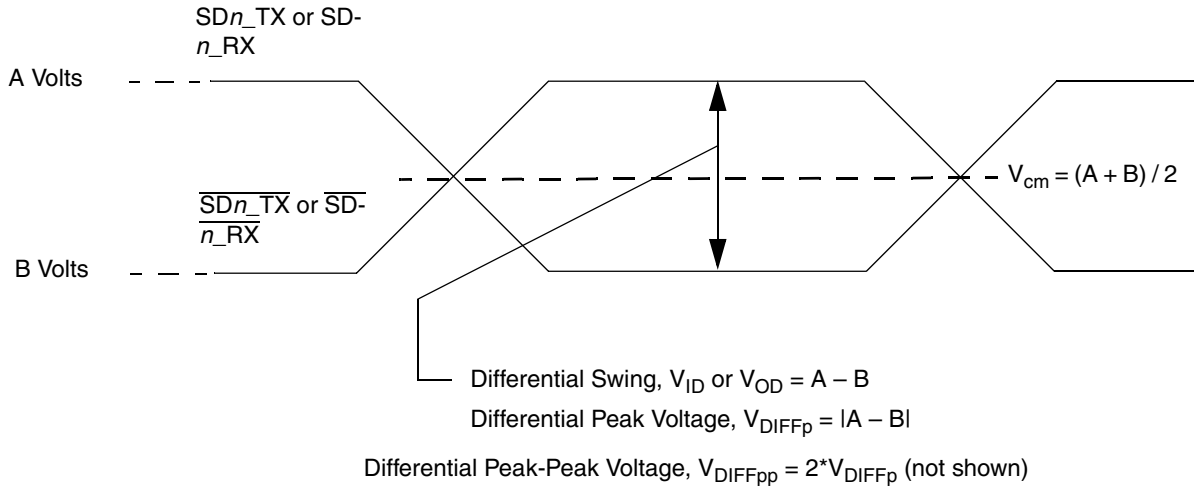


Figure 44. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and $\overline{\text{SD1_REF_CLK}}$ for PCI Express1, PCI Express2. SD2_REF_CLK, and $\overline{\text{SD2_REF_CLK}}$ for the PCI Express3 or SGMII interface, respectively. The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 45 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 45. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{_REF_CLK}}$) has a 50-Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

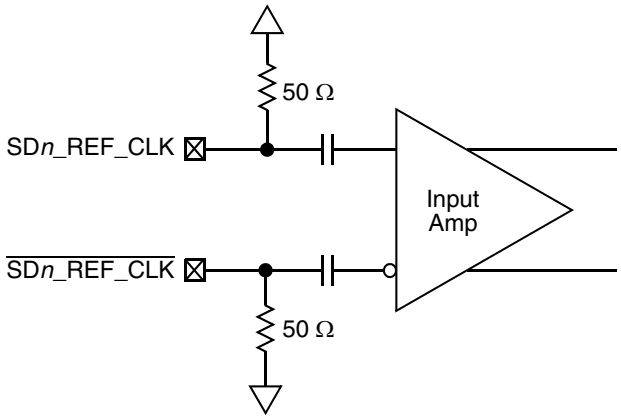


Figure 45. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8544E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 46 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 47 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**
  — The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD}n\text{_REF_CLK}}$ either left unconnected or tied to ground.
  — The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 48 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{_REF_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

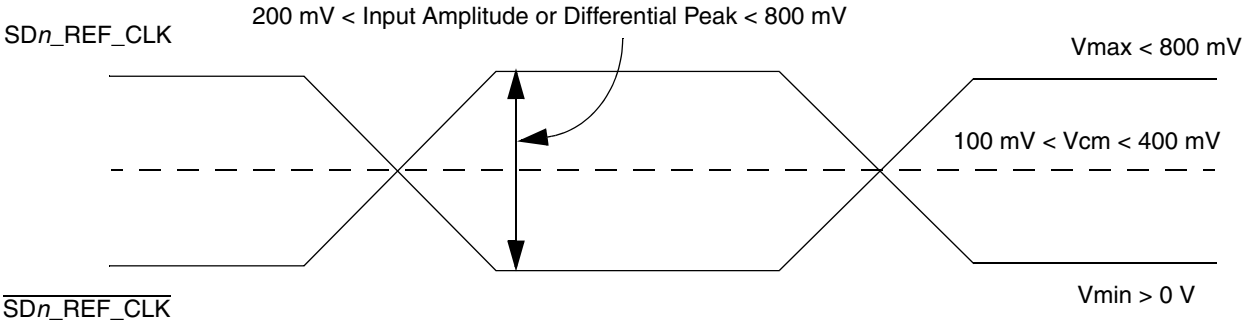


Figure 46. Differential Reference Clock Input DC Requirements (External DC-Coupled)

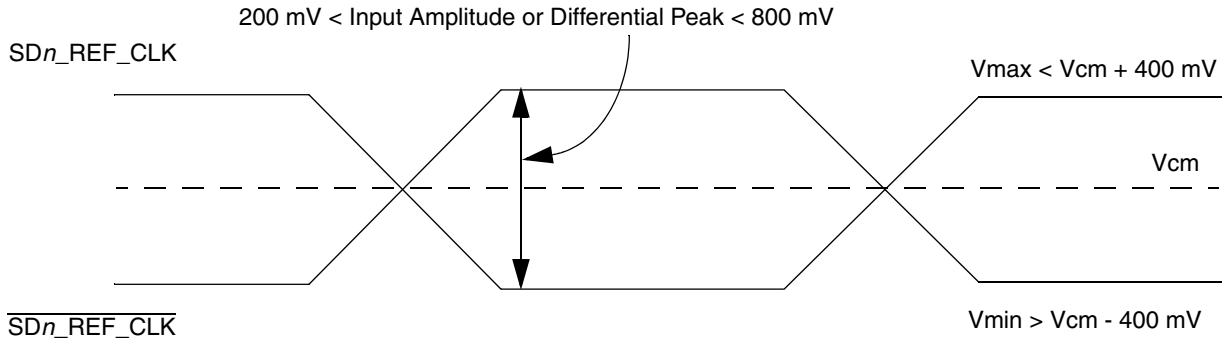


Figure 47. Differential Reference Clock Input DC Requirements (External AC-Coupled)

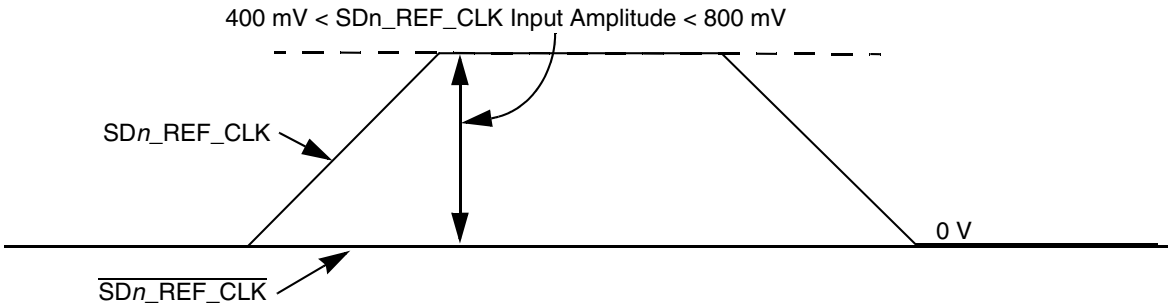


Figure 48. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 49 through Figure 52 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8544E SerDes reference clock receiver requirement provided in this document.

Figure 49 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8544E SerDes reference clock input's DC requirement.

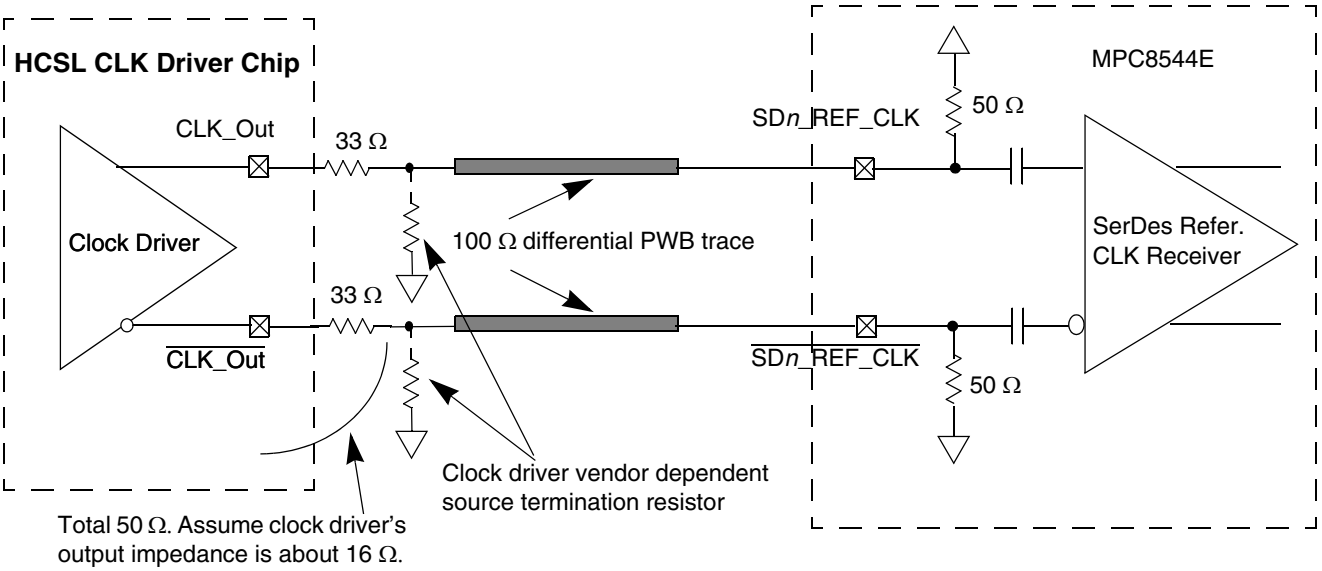


Figure 49. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 50 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8544E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

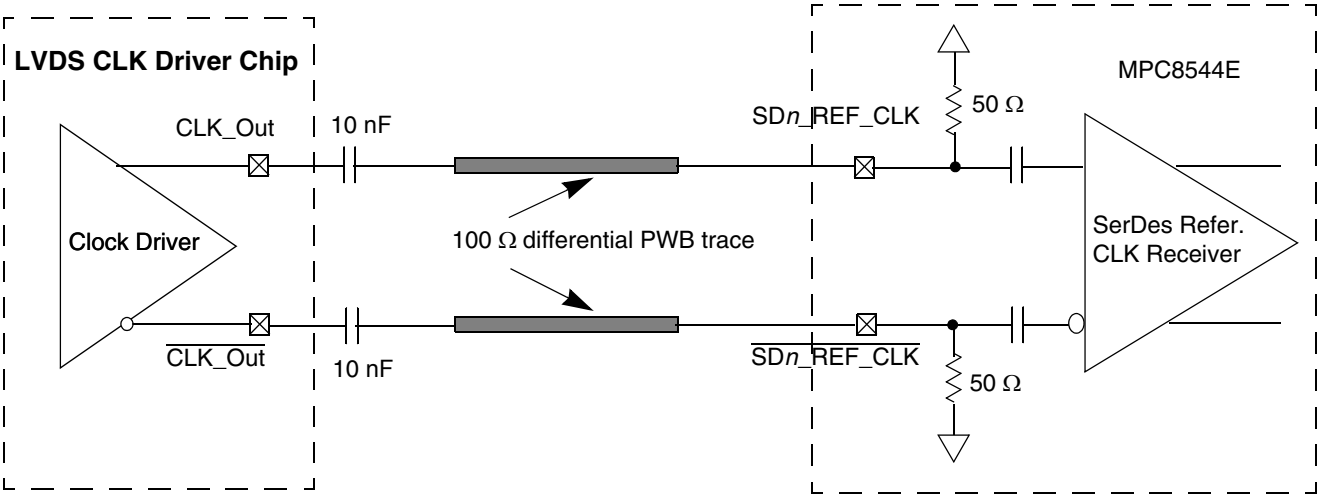


Figure 50. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 51 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8544E SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 51

assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8544E SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

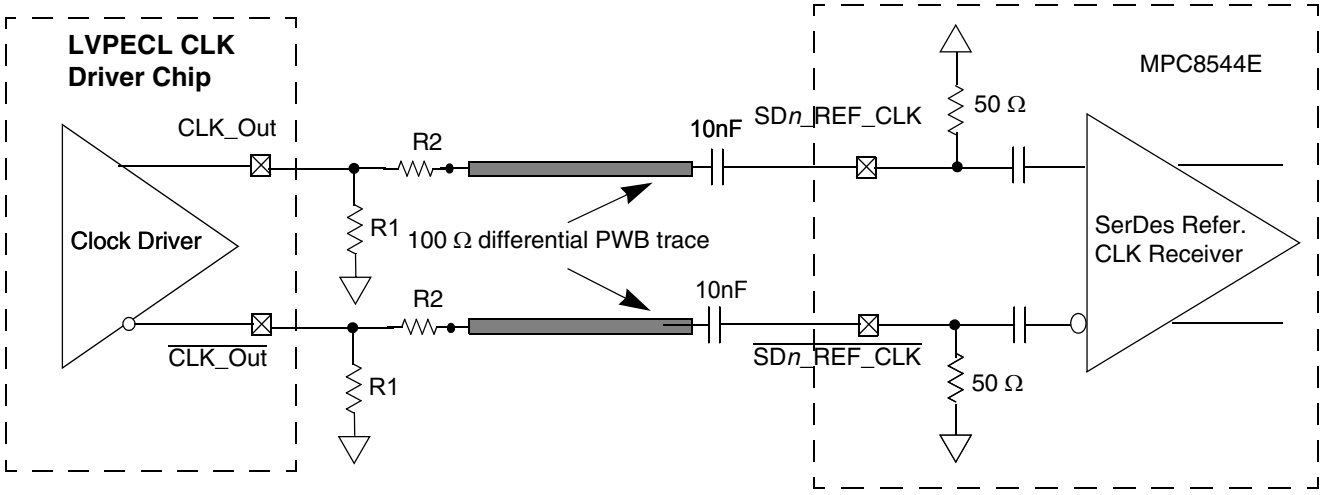


Figure 51. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 52 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8544E SerDes reference clock input's DC requirement.

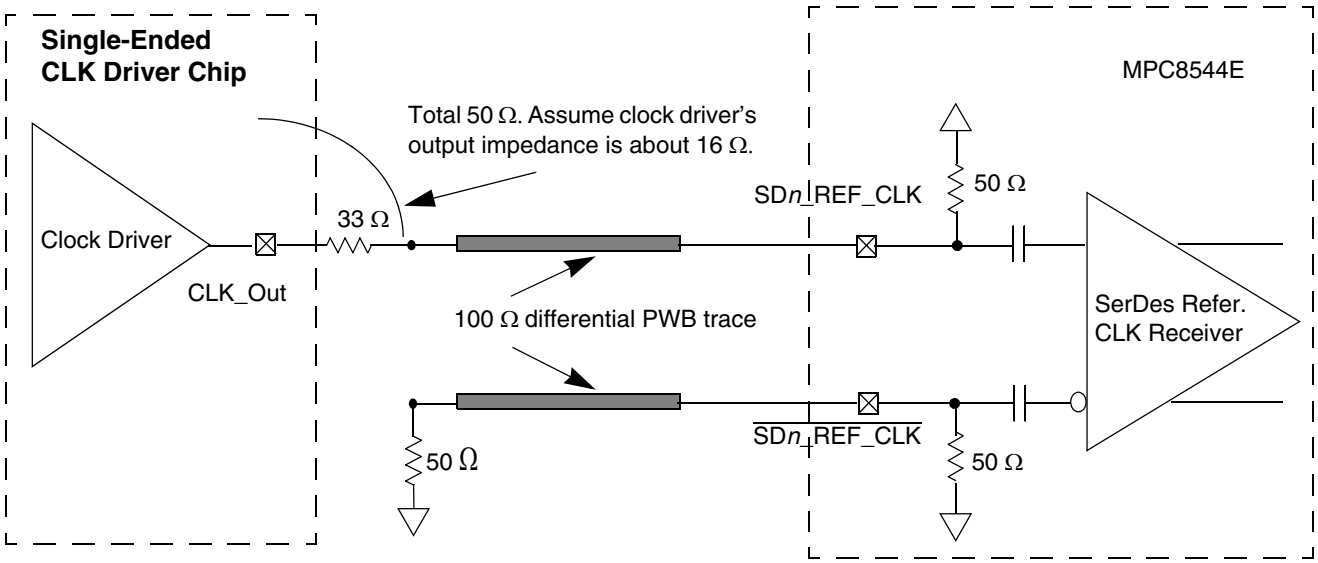


Figure 52. Single-Ended Connection (Reference Only)

16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 57 describes some AC parameters common to SGMII, and PCI Express protocols.

Table 57. SerDes Reference Clock Common AC Parameters

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{_REF_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:
1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{_REF_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 53.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{_REF_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{_REF_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{_REF_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 54.

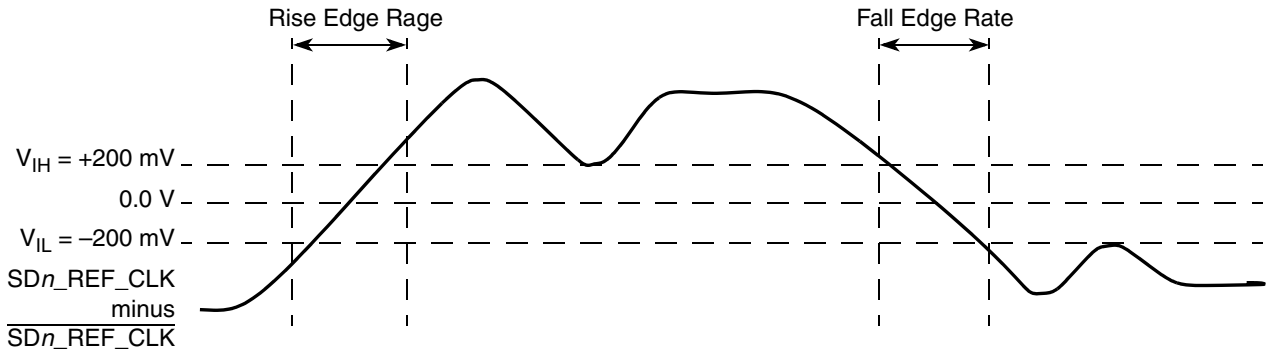


Figure 53. Differential Measurement Points for Rise and Fall Time

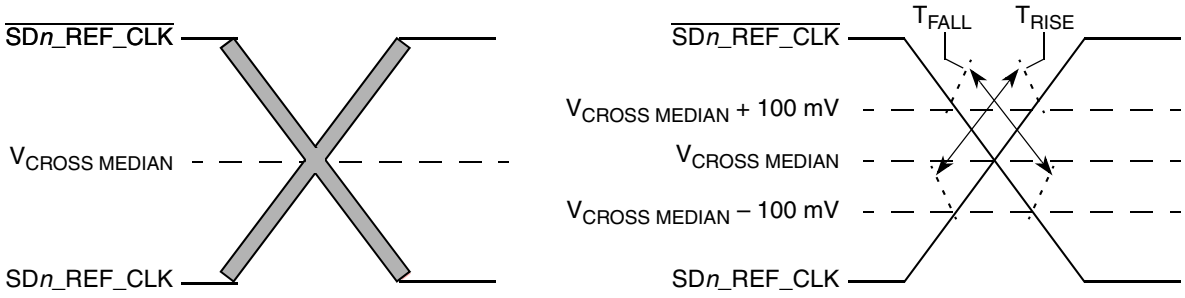


Figure 54. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 8.3.1, "The $\overline{\text{DBWO}}$ Signal"
- Section 17.2, "AC Requirements for PCI Express SerDes Clocks"

16.2.4.1 Spread Spectrum Clock

SD1_REF_CLK/$\overline{\text{SD1_REF_CLK}}$ were designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD2_REF_CLK/$\overline{\text{SD2_REF_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 55 shows the reference circuits for SerDes data lane's transmitter and receiver.

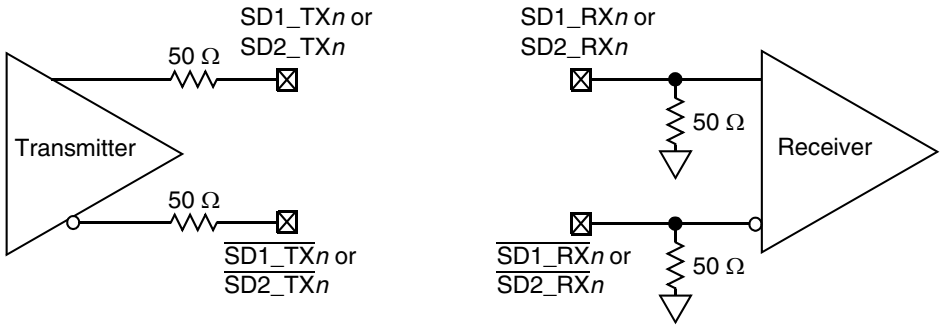


Figure 55. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in the section below (PCI Express or SGMII) in this document based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"
- Section 17, "PCI Express"

Please note that external AC Coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in specification of each protocol section.

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8544.

17.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 58 provides the AC requirements for the PCI Express SerDes clocks.

Table 58. SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ AC Requirements

Symbol[2]	Parameter Description	Min	Typ	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Notes:
1. Typical based on *PCI Express Specification 2.0*.
2. Guaranteed by characterization.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer please refer to the *PCI Express Base Specification*. *Rev. 1.0a*.

17.4.1 Differential Transmitter (TX) Output

Table 59 defines the specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 59. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$. See Note 2.
$V_{TX-DE-RATIO}$	De- emphasized differential output voltage (ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX eye width	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D– TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	—	—	20	mV	$V_{TX-CM-ACp} = RMS(\|V_{TXD+} - V_{TXD-}\|/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ See Note 2.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during LO and electrical idle	0	—	100	mV	$\|V_{TX-CM-DC\ (during\ LO)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\| <= 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [LO] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D–	0	—	25	mV	$\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\| <= 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\|V_{TX-D-}\|$ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = \|V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\| <= 20$ mV See Note 2.

Table 59. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}RCV\text{-}DETECT}$	Amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.
$V_{TX\text{-}DC\text{-}CM}$	TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
$I_{TX\text{-}SHORT}$	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground.
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in electrical idle	50	—	—	UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical Idle ordered set	—	—	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
$RL_{TX\text{-}DIFF}$	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$RL_{TX\text{-}CM}$	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance.
$Z_{TX\text{-}DC}$	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC Impedance during all states.
$L_{TX\text{-}SKEW}$	Lane-to-lane output skew	—	—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single link.
C_{TX}	AC coupling capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Table 59. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$T_{crosslink}$	Crosslink random timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 58 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 56.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 58.) Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 58 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications, Rev 1.0a.*
7. See Section 4.2.6.3 of the *PCI Express Base Specifications, Rev 1.0a.*

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 56 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

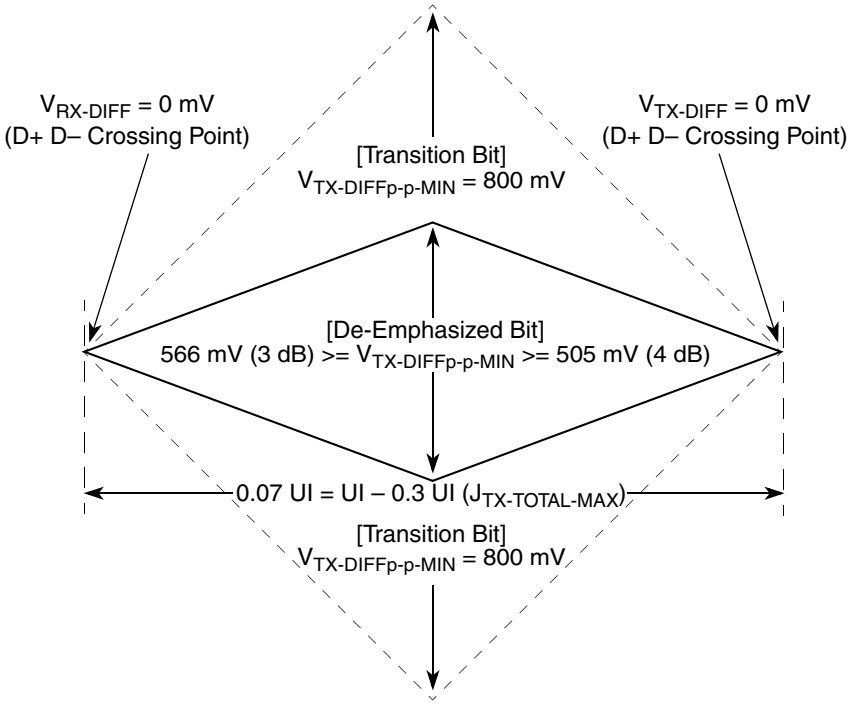


Figure 56. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 60 defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

Table 60. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 2.
T_{RX-EYE}	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.

Table 60. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.
$V_{RX-CM-ACp}$	AC peak common mode input voltage	—	—	150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert \div 2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$ See Note 2.
$RL_{RX-DIFF}$	Differential return loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4.
RL_{RX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
Z_{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	—	—	10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 60. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total skew	—	—	20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 57). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 58). Note that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 57 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express RX component.

In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 58) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 57) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 57). Note that the series capacitors, CTX, are optional for the return loss measurement.

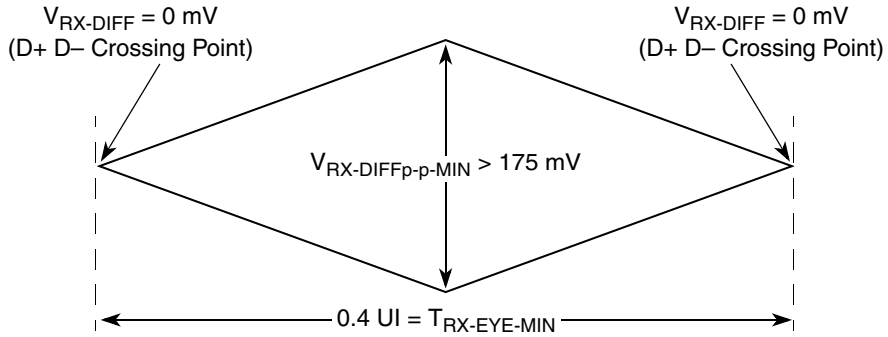


Figure 57. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 58.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

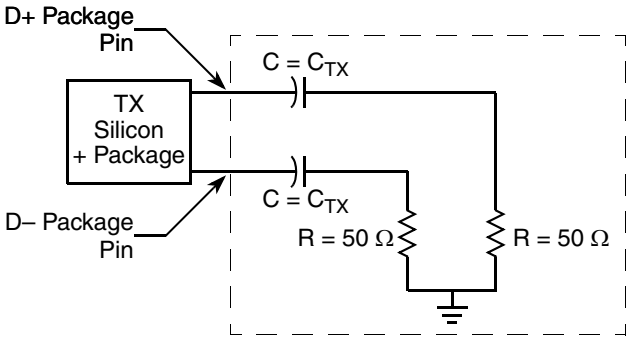


Figure 58. Compliance Test/Measurement Load

18 Package Description

This section details package parameters, pin assignments, and dimensions.

18.1 Package Parameters for the MPC8544E FC-PBGA

The package parameters for flip chip plastic ball grid array (FC-PBGA) are provided in Table 61.

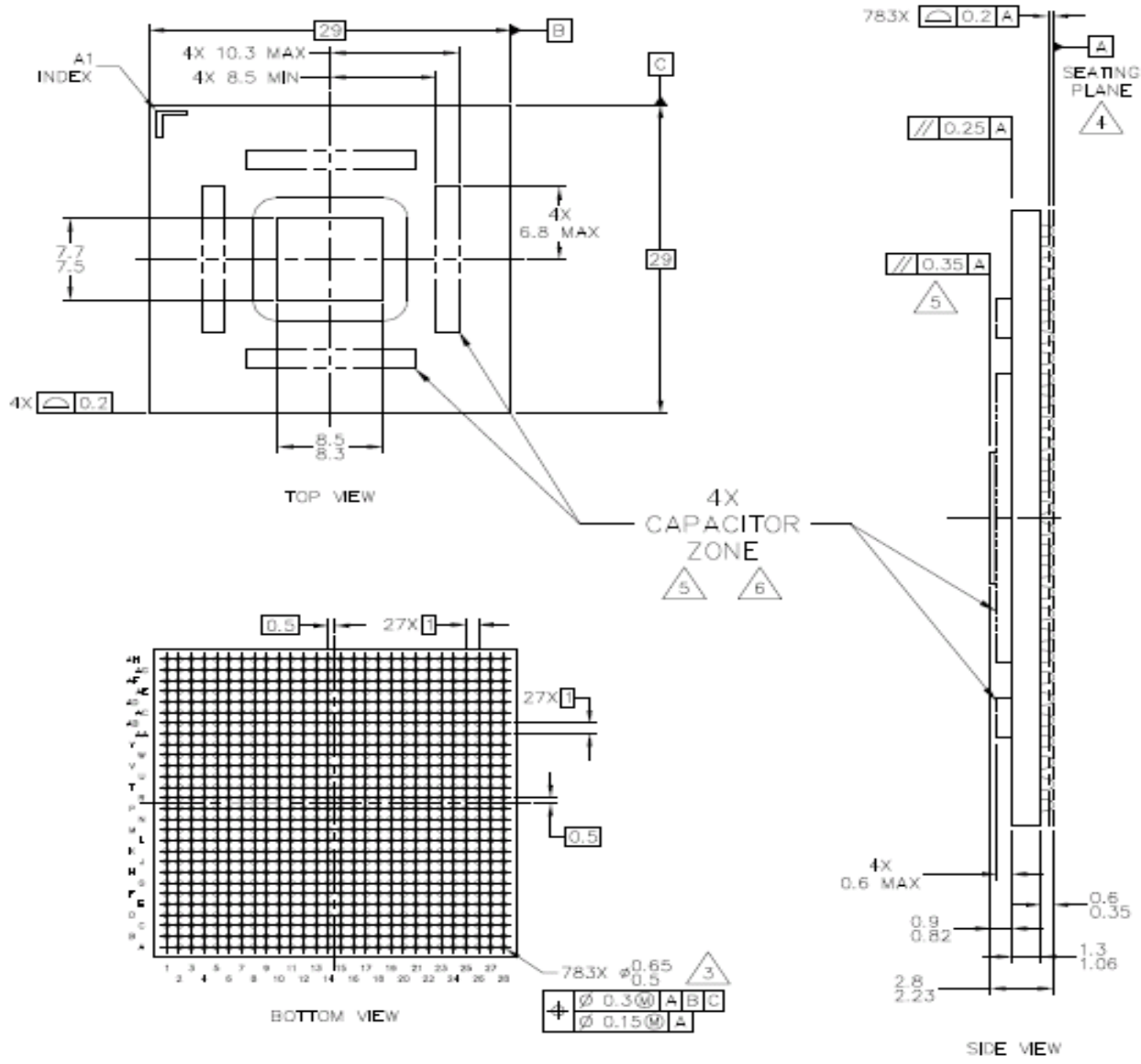
Table 61. Package Parameters

Parameter	PBGA[1]
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (Pb-free)	96.5% Sn 3.5% Ag

Note:
1. (FC-PBGA) without a lid.

18.2 Mechanical Dimensions of the MPC8544E FC-PBGA

Figure 59 shows the mechanical dimensions and bottom surface nomenclature of the MPC8544E, 783 FC-PBGA package without a lid.



Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. Capacitors may not be present on all parts. Care must be taken not to short exposed metal capacitor pads.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

Figure 59. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8544E FC-PBGA without a Lid

18.3 Pinout Listings

Table 62 provides the pinout listing for the MPC8544E 783 FC-PBGA package.

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software.

NOTE

The $\overline{\text{DMA_DACK}}$[0:1] and $\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. Please refer to Table 62 for more details.

Table 62. MPC8544E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI1_AD[31:0]	AE8, AD8, AF8, AH12, AG12, AB9, AC9, AE9, AD10, AE10, AC11, AB11, AB12, AC12, AF12, AE11, Y14, AE15, AC15, AB15, AA15, AD16, Y15, AB16, AF18, AE18, AC17, AE19, AD19, AB17, AB18, AA16	I/O	OV_{DD}	—
PCI1_C_$\overline{\text{BE}}$[3:0]	AC10, AE12, AA14, AD17	I/O	OV_{DD}	—
$\overline{\text{PCI1_GNT}}$[4:1]	AE7, AG11,AH11, AC8	O	OV_{DD}	4, 8, 24
$\overline{\text{PCI1_GNT0}}$	AE6	I/O	OV_{DD}	—
$\overline{\text{PCI1_IRDY}}$	AF13	I/O	OV_{DD}	2
PCI1_PAR	AB14	I/O	OV_{DD}	—
$\overline{\text{PCI1_PERR}}$	AE14	I/O	OV_{DD}	2
$\overline{\text{PCI1_SERR}}$	AC14	I/O	OV_{DD}	2
$\overline{\text{PCI1_STOP}}$	AA13	I/O	OV_{DD}	2
$\overline{\text{PCI1_TRDY}}$	AD13	I/O	OV_{DD}	2
$\overline{\text{PCI1_REQ}}$[4:1]	AF9, AG10, AH10, AD6	I	OV_{DD}	—
$\overline{\text{PCI1_REQ0}}$	AB8	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	—
$\overline{\text{PCI1_DEVSEL}}$	AC13	I/O	OV_{DD}	2
$\overline{\text{PCI1_FRAME}}$	AD12	I/O	OV_{DD}	2
PCI1_IDSEL	AG6	I	OV_{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	A26, B26, C22, D21, D25, B25, D22, E21, A24, A23, B20, A20, A25, B24, B21, A21, E19, D19, E16, C16, F19, F18, F17, D16, B18, A18, A15, B14, B19, A19, A16, B15, D1, F3, G1, H2, E4, G5, H3, J4, B2, C3, F2, G2, A2, B3, E1, F1, L5, L4,N3, P3, J3, K4, N4, P4, J1, K1, P1, R1, J2, K2, N1, R2	I/O	GV_{DD}	—
MECC[0:7]	G12, D14, F11, C11, G14, F14,C13, D12	I/O	GV_{DD}	—
MDM[0:8]	C25, B23, D18, B17, G4, C2, L3, L2, F13	O	GV_{DD}	21
$\overline{\text{MDQS}}$[0:8]	D24, B22, C18, A17, J5, C1, M4, M2, E13	I/O	GV_{DD}	—
MDQS[0:8]	C23, A22, E17, B16, K5, D2, M3, P2, D13	I/O	GV_{DD}	—
MA[0:15]	B7, G8, C8, A10, D9, C10, A11, F9, E9, B12, A5, A12, D11, F7, E10, F10	O	GV_{DD}	—
MBA[0:2]	A4, B5, B13	O	GV_{DD}	—
$\overline{\text{MWE}}$	B4	O	GV_{DD}	—
$\overline{\text{MCAS}}$	E7	O	GV_{DD}	—
$\overline{\text{MRAS}}$	C5	O	GV_{DD}	—
MCKE[0:3]	H10, K10, G10, H9	O	GV_{DD}	10
$\overline{\text{MCS}}$[0:3]	D3, H6, C4, G6	O	GV_{DD}	—
MCK[0:5]	A9, J11, J6, A8, J13, H8	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	B9, H11, K6, B8, H13, J8	O	GV_{DD}	—
MODT[0:3]	E5, H7, E6, F6	O	GV_{DD}	—
MDIC[0:1]	H15, K15	I/O	GV_{DD}	25
TEST_IN	A13	I	—	27
TEST_OUT	A6	O	—	17
Local Bus Controller Interface				
LAD[0:31]	K22, L21, L22, K23, K24, L24, L25, K25, L28, L27, K28, K27, J28, H28, H27, G27, G26, F28, F26, F25, E28, E27, E26, F24, E24, C26, G24, E23, G23, F22, G22, G21	I/O	BV_{DD}	23
LDP[0:3]	K26, G28, B27, E25	I/O	BV_{DD}	
LA[27]	L19	O	BV_{DD}	4, 8
LA[28:31]	K16, K17, H17,G17	O	BV_{DD}	4, 6, 8
$\overline{\text{LCS}}$[0:4]	K18, G19, H19, H20, G16	O	BV_{DD}	—
$\overline{\text{LCS5}}$/$\overline{\text{DMA_DREQ2}}$	H16	I/O	BV_{DD}	1

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCS6/DMA_DACK2	J16	O	BV_{DD}	1
LCS7/DMA_DDONE2	L18	O	BV_{DD}	1
LWE0/LBS0/LSDDQM[0]	J22	O	BV_{DD}	4, 8
LWE1/LBS1/LSDDQM[1]	H22	O	BV_{DD}	4, 8
LWE2/LBS2/LSDDQM[2]	H23	O	BV_{DD}	4, 8
LWE3/LBS3/LSDDQM[3]	H21	O	BV_{DD}	4, 8
LALE	J26	O	BV_{DD}	4, 7, 8
LBCTL	J25	O	BV_{DD}	4, 7, 8
LGPL0/LSDA10	J20	O	BV_{DD}	4, 8
LGPL1/LSDWE	K20	O	BV_{DD}	4, 8
LGPL2/LOE/LSDRAS	G20	O	BV_{DD}	4, 7, 8
LGPL3/LSDCAS	H18	O	BV_{DD}	4, 8
LGPL4/LGTA/LUPWAIT/ LPBSE	L20	I/O	BV_{DD}	28
LGPL5	K19	O	BV_{DD}	4, 8
LCKE	L17	O	BV_{DD}	—
LCLK[0:2]	H24, J24, H25	O	BV_{DD}	—
LSYNC_IN	D27	I	BV_{DD}	—
LSYNC_OUT	D28	O	BV_{DD}	—
DMA				
DMA_DACK[0:1]	Y13, Y12	O	OV_{DD}	4, 8, 9
DMA_DREQ[0:1]	AA10, AA11	I	OV_{DD}	—
DMA_DDONE[0:1]	AA7, Y11	O	OV_{DD}	—
Programmable Interrupt Controller				
UDE	AH15	I	OV_{DD}	—
MCP	AG18	I	OV_{DD}	—
IRQ[0:7]	AG22, AF17, AD21, AF19, AG17, AF16, AC23, AC22	I	OV_{DD}	—
IRQ[8]	AC19	I	OV_{DD}	—
IRQ[9]/DMA_DREQ3	AG20	I	OV_{DD}	1
IRQ[10]/DMA_DACK3	AE27	I/O	OV_{DD}	1
IRQ[11]/DMA_DDONE3	AE24	I/O	OV_{DD}	1
IRQ_OUT	AD14	O	OV_{DD}	2

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Ethernet Management Interface				
EC_MDC	AC7	O	OV_{DD}	4, 8, 14
EC_MDIO	Y9	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	T2	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	U10, U9, T10, T9, U8, T8, T7, T6	I	LV_{DD}	—
TSEC1_TXD[7:0]	T5, U5, V5, V3, V2, V1, U2, U1	O	LV_{DD}	4, 8, 14
TSEC1_COL	R5	I	LV_{DD}	—
TSEC1_CRS	T4	I/O	LV_{DD}	16
TSEC1_GTX_CLK	T1	O	LV_{DD}	—
TSEC1_RX_CLK	V7	I	LV_{DD}	—
TSEC1_RX_DV	U7	I	LV_{DD}	—
TSEC1_RX_ER	R9	I	LV_{DD}	4, 8
TSEC1_TX_CLK	V6	I	LV_{DD}	—
TSEC1_TX_EN	U4	O	LV_{DD}	22
TSEC1_TX_ER	T3	O	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_RXD[7:0]	P11, N11, M11, L11, R8, N10, N9, P10	I	LV_{DD}	—
TSEC3_TXD[7:0]	M7, N7, P7, M8, L7, R6, P6, M6	O	LV_{DD}	4, 8, 14
TSEC3_COL	M9	I	LV_{DD}	—
TSEC3_CRS	L9	I/O	LV_{DD}	16
TSEC3_GTX_CLK	R7	O	LV_{DD}	—
TSEC3_RX_CLK	P9	I	LV_{DD}	—
TSEC3_RX_DV	P8	I	LV_{DD}	—
TSEC3_RX_ER	R11	I	LV_{DD}	—
TSEC3_TX_CLK	L10	I	LV_{DD}	—
TSEC3_TX_EN	N6	O	LV_{DD}	22
TSEC3_TX_ER	L8	O	LV_{DD}	4, 8
DUART				
$\overline{\text{UART_CTS}}$[0:1]	AH8, AF6	I	OV_{DD}	—
$\overline{\text{UART_RTS}}$[0:1]	AG8, AG9	O	OV_{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UART_SIN[0:1]	AG7, AH6	I	OV_{DD}	—
UART_SOUT[0:1]	AH7, AF7	O	OV_{DD}	—
I^2C interface				
IIC1_SCL	AG21	I/O	OV_{DD}	20
IIC1_SDA	AH21	I/O	OV_{DD}	20
IIC2_SCL	AG13	I/O	OV_{DD}	20
IIC2_SDA	AG14	I/O	OV_{DD}	20
SerDes 1				
SD1_RX[0:7]	N28, P26, R28, T26, Y26, AA28, AB26, AC28	I	XV_{DD}	—
$\overline{\text{SD1_RX}}$[0:7]	N27, P25, R27, T25, Y25, AA27, AB25, AC27	I	XV_{DD}	—
SD1_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV_{DD}	—
$\overline{\text{SD1_TX}}$[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV_{DD}	—
SD1_PLL_TPD	V28	O	XV_{DD}	17
SD1_REF_CLK	U28	I	XV_{DD}	—
$\overline{\text{SD1_REF_CLK}}$	U27	I	XV_{DD}	—
SD1_TST_CLK	T22		—	—
$\overline{\text{SD1_TST_CLK}}$	T23		—	—
SerDes 2				
SD2_RX[0]	AD25	I	XV_{DD}	—
SD2_RX[2]	AD1	I	XV_{DD}	26
SD2_RX[3]	AB2	I	XV_{DD}	26
$\overline{\text{SD2_RX}}$[0]	AD26	I	XV_{DD}	—
$\overline{\text{SD2_RX}}$[2]	AC1	I	XV_{DD}	26
$\overline{\text{SD2_RX}}$[3]	AA2	I	XV_{DD}	26
SD2_TX[0]	AA21	O	XV_{DD}	—
SD2_TX[2]	AC4	O	XV_{DD}	26
SD2_TX[3]	AA5	O	XV_{DD}	26
$\overline{\text{SD2_TX}}$[0]	AA20	O	XV_{DD}	—
$\overline{\text{SD2_TX}}$[2]	AB4	O	XV_{DD}	26
$\overline{\text{SD2_TX}}$[3]	Y5	O	XV_{DD}	26
SD2_PLL_TPD	AG3	O	XV_{DD}	17
SD2_REF_CLK	AE2	I	XV_{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD2_REF_CLK}}$	AF2	I	XV_{DD}	—
SD2_TST_CLK	AG4	—	—	—
$\overline{\text{SD2_TST_CLK}}$	AF4	—	—	—
General-Purpose Output				
GPOUT[0:7]	AF22, AH23, AG27, AH25, AF21, AF25, AG26, AF26	O	OV_{DD}	—
General-Purpose Input				
GPIN[0:7]	AH24, AG24, AD23, AE21, AD22, AF23, AG25, AE20	I	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG16	I	OV_{DD}	—
$\overline{\text{HRESET_REQ}}$	AG15	O	OV_{DD}	21
$\overline{\text{SRESET}}$	AG19	I	OV_{DD}	—
$\overline{\text{CKSTP_IN}}$	AH5	I	OV_{DD}	—
$\overline{\text{CKSTP_OUT}}$	AA12	O	OV_{DD}	2, 4
Debug				
TRIG_IN	AC5	I	OV_{DD}	—
TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$	AB5	O	OV_{DD}	5, 8, 15, 21
MSRCID[0:1]	Y7, W9	O	OV_{DD}	4, 5, 8
MSRCID[2:4]	AA9, AB6, AD5	O	OV_{DD}	5, 15, 21
MDVAL	Y8	O	OV_{DD}	5
CLK_OUT	AE16	O	OV_{DD}	10
Clock				
RTC	AF15	I	OV_{DD}	—
SYSCLK	AH16	I	OV_{DD}	—
JTAG				
TCK	AG28	I	OV_{DD}	—
TDI	AH28	I	OV_{DD}	11
TDO	AF28	O	OV_{DD}	10
TMS	AH27	I	OV_{DD}	11
$\overline{\text{TRST}}$	AH22	I	OV_{DD}	11

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DFT				
L1_TSTCLK	AC20	I	OV_{DD}	18
L2_TSTCLK	AE17	I	OV_{DD}	18
$\overline{\text{LSSD_MODE}}$	AH19	I	OV_{DD}	18
$\overline{\text{TEST_SEL}}$	AH13	I	OV_{DD}	3
Thermal Management				
TEMP_ANODE	Y3	—	—	13
TEMP_CATHODE	AA3	—	—	13
Power Management				
ASLEEP	AH17	O	OV_{DD}	8, 15, 21
Power and Ground Signals				
GND	D5, M10, F4, D26, D23, C12, C15, E20, D8, B10, E3, J14, K21, F8, A3, F16, E12, E15, D17, L1, F21, H1, G13, G15, G18, C6, A14, A7, G25, H4, C20, J12, J15, J17, F27, M5, J27, K11, L26, K7, K8, L12, L15, M14, M16, M18, N13, N15, N17, N2, P5, P14, P16, P18, R13, R15, R17, T14, T16, T18, U13, U15, U17, AA8, U6, Y10, AC21, AA17, AC16, V4, AD7, AD18, AE23, AF11, AF14, AG23, AH9, A27, B28, C27	—	—	—
OV_{DD}[1:17]	Y16, AB7, AB10, AB13, AC6, AC18, AD9, AD11, AE13, AD15, AD20, AE5, AE22, AF10, AF20, AF24, AF27	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}[1:2]	R4, U3	Power for TSEC1 interfaces (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}[1:2]	N8, R10	Power for TSEC3 interfaces (2.5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B1, B11, C7, C9, C14, C17, D4, D6, R3, D15, E2, E8,C24, E18, F5, E14, C21, G3, G7, G9, G11, H5, H12, E22, F15, J10, K3, K12, K14, H14, D20, E11, M1, N5	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV_{DD}	—
BV_{DD}	L23, J18, J19, F20, F23, H26, J21, J23	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	L16, L14, M13, M15, M17, N12, N14, N16, N18, P13, P15, P17, R12, R14, R16, R18, T13, T15, T17, U12, U14, U16, U18,	Power for core (1.0 V)	V_{DD}	—
SVDD_SRDS	M27, N25, P28, R24, R26, T24, T27, U25, W24, W26, Y24, Y27, AA25, AB28, AD27	Core power for SerDes 1 transceivers (1.0 V)	SV_{DD}	—
SVDD_SRDS2	AB1, AC26, AD2, AE26, AG2	Core power for SerDes 2 transceivers (1.0 V)	SV_{DD}	—
XVDD_SRDS	M21, N23, P20, R22, T20, U23, V21, W22, Y20	Pad power for SerDes 1 transceivers (1.0 V)	XV_{DD}	—
XVDD_SRDS2	Y6, AA6, AA23, AF5, AG5	Pad power for SerDes 2 transceivers (1.0 V)	XV_{DD}	—
XGND_SRDS	M20, M24, N22, P21, R23, T21, U22, V20, W23, Y21	—	—	—
XGND_SRDS2	Y4, AA4, AA22, AD4, AE4, AH4	—	—	—
SGND_SRDS	M28, N26, P24, P27, R25, T28, U24, U26, V24, W25, Y28, AA24, AA26, AB24, AB27, AC24, AD28	—	—	—
AGND_SRDS	V27	SerDes PLL GND	—	—
SGND_SRDS2	Y2, AA1, AB3, AC2, AC3, AC25, AD3, AD24, AE3, AE1, AE25, AF3, AH2	—	—	—
AGND_SRDS2	AF1	SerDes PLL GND	—	—
AVDD_LBIU	C28	Power for local bus PLL (1.0 V)	—	19
AVDD_PCI1	AH20	Power for PCI PLL (1.0 V)	—	19
AVDD_CORE	AH14	Power for e500 PLL (1.0 V)	—	19
AVDD_PLAT	AH18	Power for CCB PLL (1.0 V)	—	19

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
AVDD_SRDS	W28	Power for SRDSPLL (1.0 V)	—	19
AVDD_SRDS2	AG1	Power for SRDSPLL (1.0 V)	—	19
SENSEVDD	W11	O	V_{DD}	12
SENSEVSS	W10	—	—	12
Analog Signals				
MVREF	A28	Reference voltage signal for DDR	MVREF	—
SD1_IMP_CAL_RX	M26	—	200Ω to GND	—
SD1_IMP_CAL_TX	AE28	—	100Ω to GND	—
SD1_PLL_TPA	V26	—	AVDD_SRDS ANALOG	17
SD2_IMP_CAL_RX	AH3	I	200 Ω to GND	—
SD2_IMP_CAL_TX	Y1	I	100 Ω to GND	—
SD2_PLL_TPA	AH1	O	AVDD_SRDS2 ANALOG	17
No Connect Pins				
NC	C19, D7, D10, K13, L6, K9, B6, F12, J7, M19, M25, N19, N24, P19, R19, AB19, T12, W3, M12, W5, P12, T19, W1, W7, L13, U19, W4, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, W2, W6, W8, T11, U11, W12, W13, W14, W15, W16, W17, W18, W19, W27, V25, Y17, Y18, Y19, AA18, AA19, AB20, AB21, AB22, AB23, J9	—	—	—

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}/\overline{\text{DMA_REQ2}}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
3. This pin must always be pulled high.
4. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed. TSEC3_TXD[3] (cfg_srds_sgmii_refclk) is an exception, because the default value of this configuration signal is low (0). Thus, no external pull-down resistor is needed for selecting the default configuration value.
5. Treat these pins as no connects (NC) unless using debug address functionality.

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

6.The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.2, "CCB/SYSCLK PLL Ratio."

7.The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.3, "e500 Core PLL Ratio."

8.Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. Therefore, this pin will be described as an I/O for boundary scan.

9.For proper state of these signals during reset, $\overline{\text{DMA_DACK}}$[1] must be pulled down to GND through a resistor. $\overline{\text{DMA_DACK}}$[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on $\overline{\text{DMA_DACK}}$[0].

10.This output is actively driven during reset rather than being three-stated during reset.

11.These JTAG pins have weak internal pull-up P-FETs that are always enabled.

12.These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.

13.Anode and cathode of internal thermal diode.

14.Treat pins AC7, T5, V2, and M7 as spare configuration pins cfg_spare[0:3]. The spare pins are unused POR config pins. It is highly recommended that the customer provide the capability of setting these pins low (that is, pull-down resistor which is not currently stuffed) in order to support new config options should they arise between revisions.

15.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

16.This pin is only an output in FIFO mode when used as Rx flow control.

17.Do not connect.

18.These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to OV_{DD} for normal machine operation.

19.Independent supplies derived from board V_{DD}.

20.Recommend a pull-up resistor (1 K~) be placed on this pin to OV_{DD}.

21.The following pins must not be pulled down during power-on reset: $\overline{\text{HRESET_REQ}}$, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], and ASLEEP.

22.This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.

23.General-purpose POR configuration of user system.

24.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as No Connect or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.

25.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.

26.For SGMII mode.

27.Connect to GND.

28.For systems that boot from a local bus (GPCM)-controlled flash, a pull-up on LGPL4 is required.

19 Clocking

This section describes the PLL configuration of the MPC8544E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

Table 63 provides the clocking specifications for the processor cores and Table 64 provides the clocking specifications for the memory bus.

Table 63. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	667 MHz		800 MHz		1000 MHz		1067 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	667	667	667	800	667	1000	667	1067	MHz	1, 2

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” and Section 19.3, “e500 Core PLL Ratio,” for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 64. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	667, 800, 1000, 1067 MHz			
	Min	Max		
Memory bus clock speed	166	266	MHz	1, 2

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, “CCB/SYSCLK PLL Ratio,” and Section 19.3, “e500 Core PLL Ratio,” for ratio settings.
2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals (see Table 65):

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

Table 65. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	Reserved	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

19.3 e500 Core PLL Ratio

Table 66 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in Table 66.

Table 66. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	Reserved	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

19.4 PCI Clocks

For specifications on the PCI_CLK, refer to the *PCI 2.2 Local Bus Specifications*.

The use of PCI_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

19.5 Security Controller PLL Ratio

Table 67 shows the SEC frequency ratio.

Table 67. SEC Frequency Ratio

Signal Name	Value (Binary)	CCB CLK:SEC CLK
LWE_B	0	2:1[1]
	1	3:1[2]

Notes:
1. In 2:1 mode the CCB frequency must be operating ≤ 400 MHz.
2. In 3:1 mode any valid CCB can be used. The 3:1 mode is the default ratio for security block.

19.6 Frequency Options

19.6.1 SYSCLK to Platform Frequency Options

Table 68 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 68. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)						
	33.33	41.66	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)						
2							—
3					—	333	400
4			—	333	400	445	533
5			333	415	500		
6			400	500			
8		333	533				
9		375					
10	333	417					
12	400	500					
16	533						

19.6.2 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed. Refer to Section 4.4, "Platform to FIFO Restrictions," for additional information.

Table 69. FIFO Maximum Speed Restrictions

Platform Speed (MHz)	Maximum FIFO Speed for Reference Clocks TSEC*n*_TX_CLK, TSEC*n*_RX_CLK (MHz)[1]
533	126
400	94

Note:
1. FIFO speed should be less than 24% of the platform speed.

20 Thermal

This section describes the thermal specifications of the MPC8544E.

20.1 Thermal Characteristics

Table 70 provides the package thermal characteristics.

Table 70. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	26	°C/W	1, 2
Junction-to-ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	17	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	12	°C/W	3
Junction-to-case thermal	—	$R_{\theta JC}$	<0.1	°C/W	4

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1°C/W.

Table 71 provides the thermal resistance with heat sink in open flow.

Table 71. Thermal Resistance with Heat Sink in Open Flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 25 mm pin fin	Natural convection	6.1
Wakefield 53 × 53 × 25 mm pin fin	1 m/s	3.0
Aavid 35 × 31 × 23 mm pin fin	Natural convection	8.1
Aavid 35 × 31 × 23 mm pin fin	1 m/s	4.3
Aavid 30 × 30 × 9.4 mm pin fin	Natural convection	11.6
Aavid 30 × 30 × 9.4 mm pin fin	1 m/s	6.7
Aavid 43 × 41 × 16.5 mm pin fin	Natural convection	8.3
Aavid 43 × 41 × 16.5 mm pin fin	1 m/s	4.3

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8544E thermal model without a lid is shown in Figure 60. The substrate is modeled as a block 29 × 29 × 1.18 mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block 29 × 29 × 0.58 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6 × 8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 59 for actual dimensions.

20.2 Recommended Thermal Model

Table 72 shows the MPC8544E thermal model.

Table 72. MPC8544EThermal Model

Conductivity	Value	Units
Die (7.6 × 8.4 × 0.75mm)		
Silicon	Temperature dependent	—
Bump/Underfill (7.6 × 8.4 × 0.070 mm) Collapsed Thermal Resistance		
Kz	6.5	W/m•K
Substrate (29 × 29 × 1.18 mm)		
Kx	18	W/m•K
Ky	18	
Kz	1.0	

Table 72. MPC8544EThermal Model (continued)

Conductivity	Value	Units
Solder and Air (29 × 29 × 0.58 mm)		
Kx	0.034	W/m•K
Ky	0.034	
Kz	12.1	

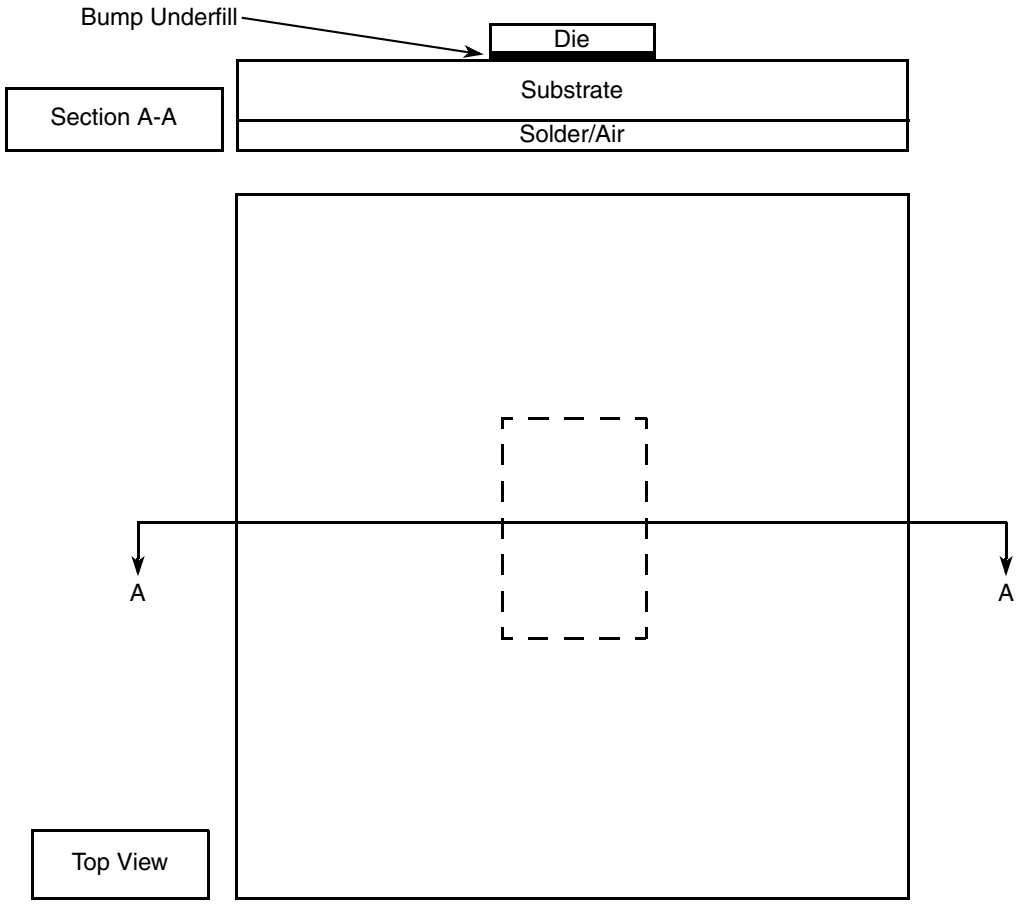


Figure 60. System Level Thermal Model for MPC8544E (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

20.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8544E implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 20.3.4, "Temperature Diode," for more information.

The recommended attachment method to the heat sink is illustrated in Figure 61. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

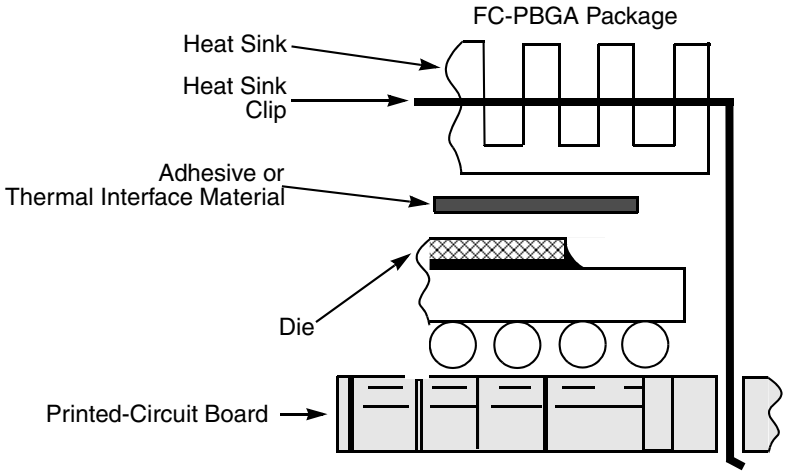


Figure 61. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Advanced Thermal Solutions781-769-2800
89 Access Road #27.
Norwood, MA02062
Internet: www.qats.com

Alpha Novatech408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC)818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI)408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering603-635-2800
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

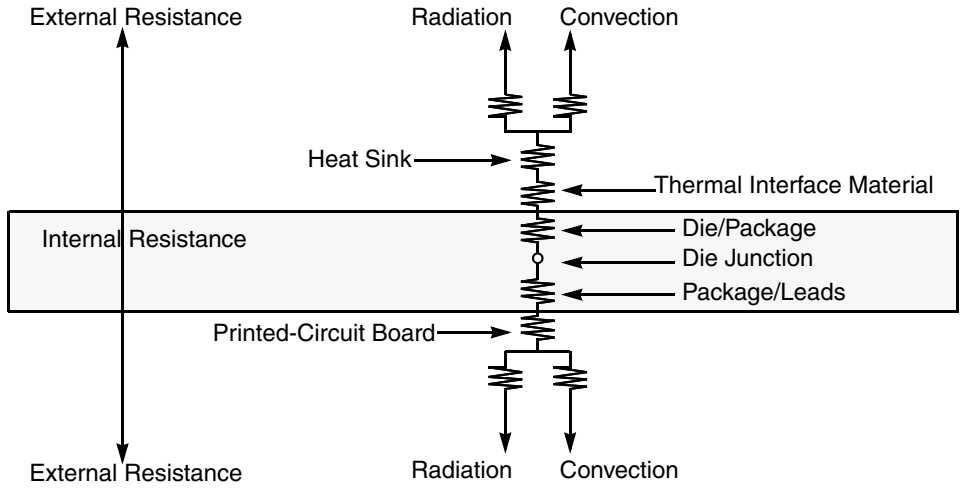
Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8544E to function in various environments.

20.3.1 Internal Package Conduction Resistance

For the packaging technology, shown in Table 70, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 62 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance.)

Figure 62. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

20.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 63 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 61). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

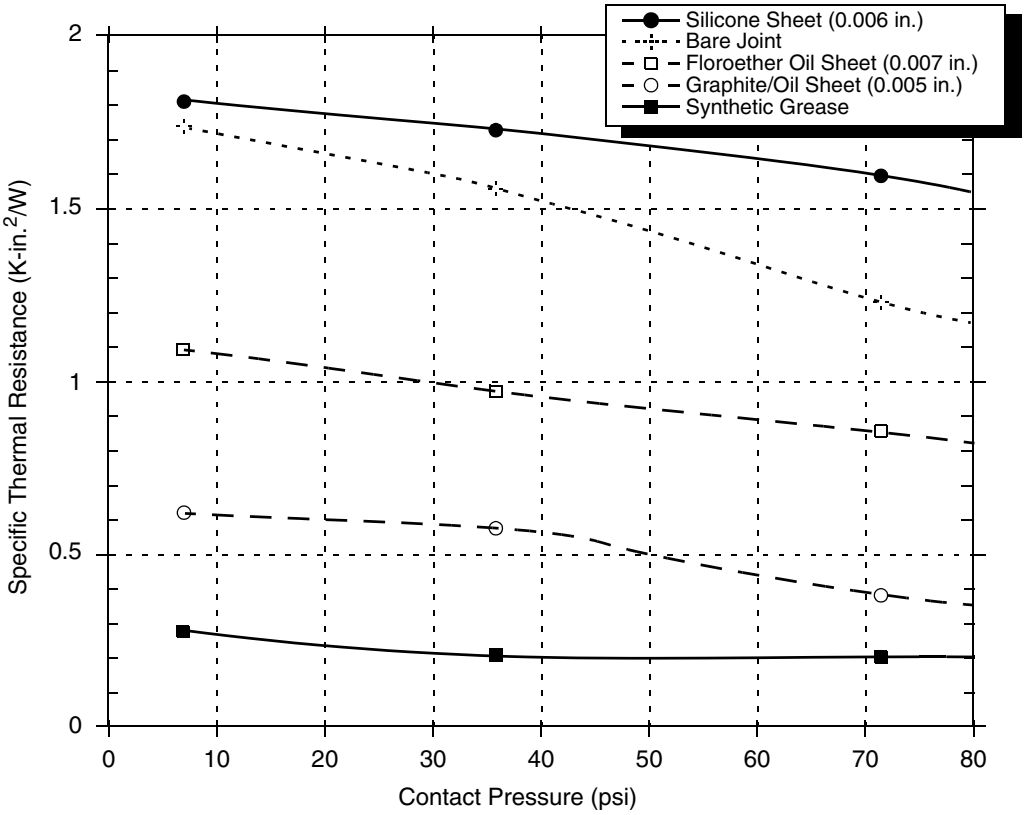


Figure 63. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation800-248-2481
Corporate Center
P.O.Box 999
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc.888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company800-347-4572
18930 West 78th St.

Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

20.3.3 Heat Sink Selection Examples

The following section provides a heat sink selection example using one of the commercially available heat sinks.

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_I + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where

T_J is the die-junction temperature
T_I is the inlet cabinet ambient temperature
T_R is the air temperature rise within the computer cabinet
θ_{JC} is the junction-to-case thermal resistance
θ_{INT} is the adhesive or interface material thermal resistance
θ_{SA} is the heat sink base-to-ambient thermal resistance
P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained within the range specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_I) may range from 30° to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{INT}) may be about 1°C/W. Assuming a T_I of 30°C, a T_R of 5°C, a FC-PBGA package θ_{JC} = 0.1, and a power consumption (P_D) of 5, the following expression for T_J is obtained:

$$\text{Die-junction temperature: } T_J = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{SA}) \times P_D$$

The heat sink-to-ambient thermal resistance (θ_{SA}) versus airflow velocity for a Thermalloy heat sink #2328B is shown in Figure 64.

Assuming an air velocity of 1 m/s, we have an effective θ_{SA+} of about 5°C/W, thus

$$T_J = 30° + 5°C + (0.1°C/W + 1.0°C/W + 5°C/W) \times 5$$

resulting in a die-junction temperature of approximately 66, which is well within the maximum operating temperature of the component.

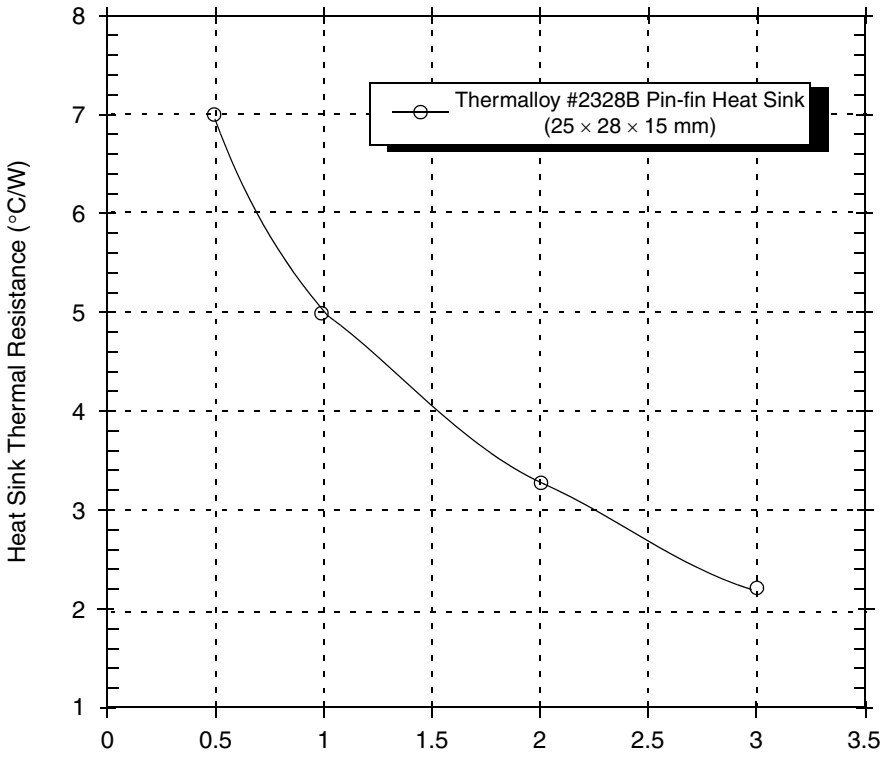


Figure 64. Approach Air Velocity (m/s)

20.3.4 Temperature Diode

The MPC8544E has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are voltage forward biased range of the on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature. The ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = \mathbf{I_s}\left[e^{\frac{qV_f}{nKT}} - \mathbf{1}\right]$$

Another useful equation is:

$$\mathbf{V_H - V_L = n}\frac{KT}{q}\left[\boldsymbol{ln}\ \frac{I_H}{I_L}\right]$$

where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$\mathbf{V_H - V_L = 1.986 \times 10^{-4} \times nT}$$

Solving for T, the equation becomes:

$$\mathbf{nT} = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8544E.

21.1 System Clocking

This device includes six PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 19.2, "CCB/SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 19.3, "e500 Core PLL Ratio."
- The PCI PLL generates the clocking for the PCI bus.
- The local bus PLL generates the clock for the local bus.
- There are two PLLs for the SerDes block.

21.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 65, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

Figure 65 shows the PLL power supply filter circuit.

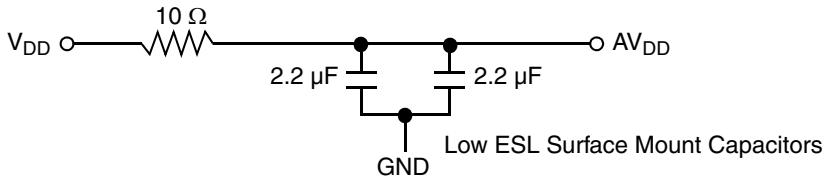
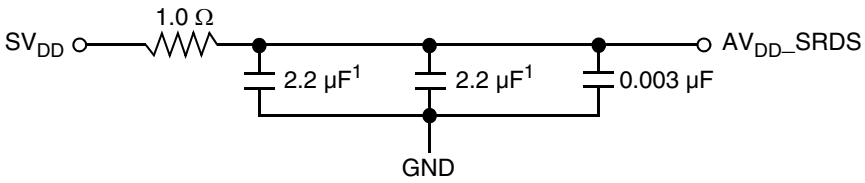


Figure 65. MPC8544E PLL Power Supply Filter Circuit

The AV_{DD}_SRDS*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 66. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.



Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 66. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD}_SRDS should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8544E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}; and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types and quantity of bulk capacitors.

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND pins of the device.

21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8544E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 69. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], $\overline{\text{HRESET_REQ}}$, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP. The $\overline{\text{DMA_DACK}}$[0:1] and $\overline{\text{TEST_SEL}}$ pins must be set to a proper state during POR configuration. Refer to the pinout listing table (Table 62) for more details. Refer to the *PCI 2.2 Local Bus Specifications,* for all pullups required for PCI.

21.7 Output Buffer DC Impedance

The MPC8544E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C). To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 67). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the

resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

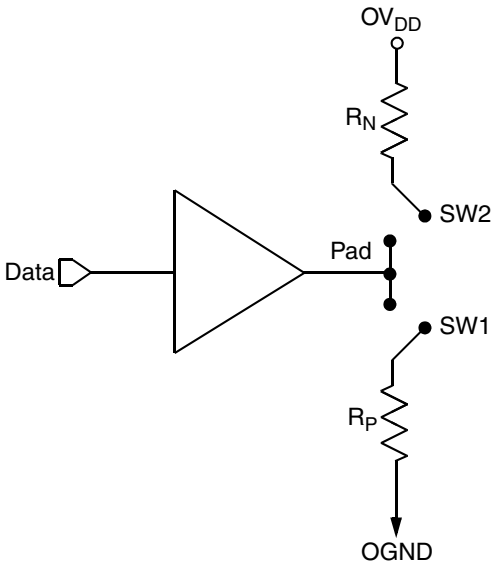


Figure 67. Driver Impedance Measurement

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 90°C.

Table 73. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 1.

21.8 Configuration Pin Muxing

The MPC8544E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has

been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 69. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors built on Power Architecture™ technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic. The arrangement shown in Figure 69 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 68, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 68 is common to all known emulators.

21.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 69. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

Figure 68 shows the COP connector physical pinout.

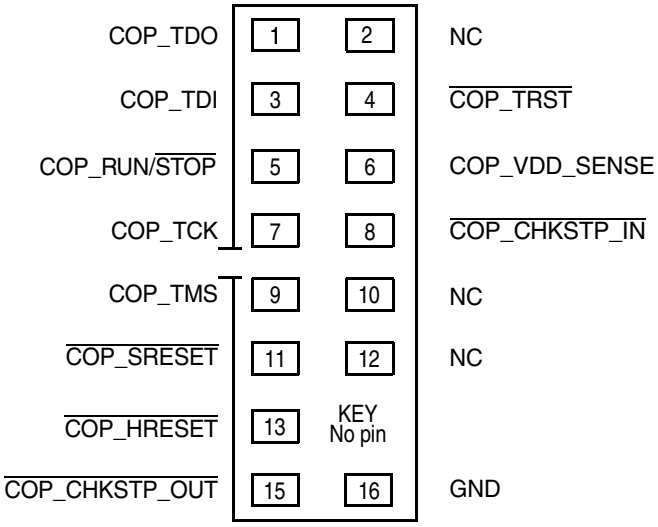
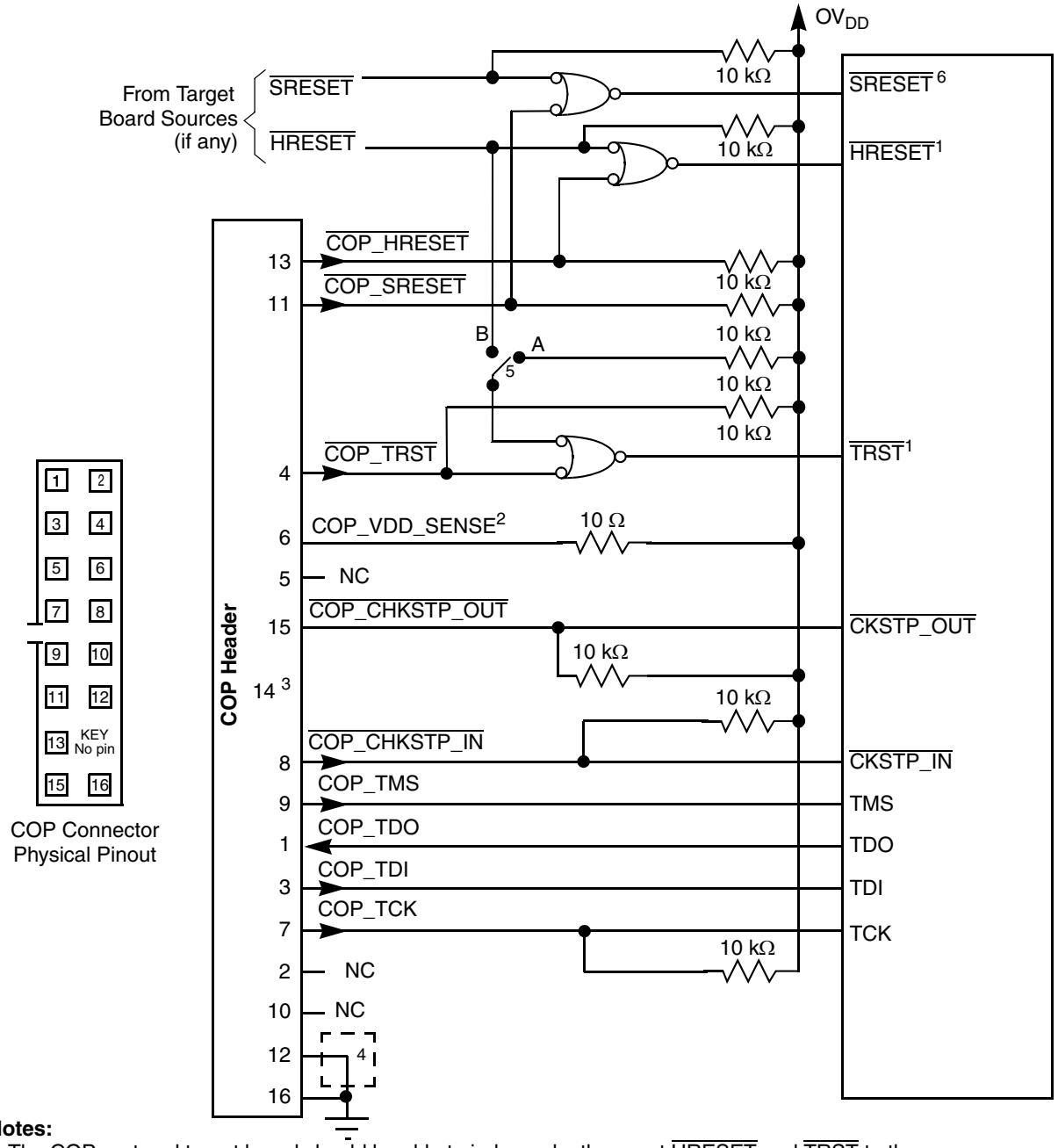


Figure 68. COP Connector Physical Pinout

Figure 69 shows the JTAG interface connection.



Notes:

1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting SRESET causes a machine check interrupt to the e500 core.

Figure 69. JTAG Interface Connection

21.10 Guidelines for High-Speed Interface Termination

This section provides guidelines for when the SerDes interface is either not used at all or only partly used.

21.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[0:7]
- $\overline{\text{SD_TX}}$[0:7]

The following pins must be connected to GND:

- SD_RX[0:7]
- $\overline{\text{SD_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD_REF_CLK}}$

21.10.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[0:7]
- $\overline{\text{SD_TX}}$[0:7]

The following pins must be connected to GND if not used:

- SD_RX[0:7]
- $\overline{\text{SD_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD_REF_CLK}}$

21.11 Guideline for PCI Interface Termination

PCI termination, if not used at all, is done as follows.

Option 1

- If PCI arbiter is enabled during POR,
- All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-kΩ resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-kΩ resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-kΩ resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. Table 74 provides a description for commercial and industrial qualifications.

Table 74. Commercial and Industrial Description

Tier[1]	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Note:
1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.

22.2 Nomenclature of Parts Fully Addressed by this Document

Table 75 provides the Freescale part numbering nomenclature for the MPC8544E.

Table 75. Device Nomenclature

MPC	*nnnn*	*E*	*C*	*HX*	*AA*	*X*	*B*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range**	**Package[1]**	**Processor Frequency[2]**	**Platform Frequency**	**Revision Level**
MPC	8544	Blank = not included E = included	B or Blank = Industrial Tier standard temp range(0° to 105°C) C = Industrial Tier Extended temp range(–40° to 105°C)	VT = FC-PBGA (lead-free) VJ = lead-free FC-PBGA	AL = 667 MHz AN = 800 MHz AQ = 1000 MHz AR = 1067 MHz	F = 333 MHz G = 400 MHz J = 533 MHz	Blank = Rev. 1.1 1.1.1 A = Rev. 2.1

Notes:
1. See Section 18, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
4. The VJ part number is entirely lead-free. This includes the C4 die bumps.

22.3 Part Marking

Parts are marked as in the example shown in Figure 70.

FC-PBGA

Notes:
MMMMM is the 5-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 70. Part Marking for FC-PBGA Device

23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

Table 76. MPC8544E Document Revision History

Revision	Date	Substantive Change(s)
8	09/2015	• In Table 10 and Table 12, removed the output leakage current rows and removed table note 4.
7	06/2014	• In Table 75, “Device Nomenclature,” added full Pb-free part code. • In Table 75, “Device Nomenclature,” added footnotes 3 and 4.
6	05/2011	• Updated the value of t_{JTKLDX} to 2.5 ns from 4ns in Table 50.
5	01/2011	• Updated Table 75.
4	09/2010	• Modified local bus information in Section 1.1, “Key Features,” to show max local bus frequency as 133 MHz. • Added footnote 28 to Table 62. • Updated solder-ball parameter in Table 61.
3	11/2009	• Update Section 20.3.4, “Temperature Diode,” • Update Table 61 Package Parameters from 95.5%sn to 96.5%sn
2	01/2009	• Update power number table to include 1067 MHz/533 MHz power numbers. • Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. • Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note. • Update t_{DDKHMP}, t_{DDKHME} in Table 18. • Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle. • Update paragraph Section 21.3, “Decoupling Recommendations.” • Update Figure 5 DDR Output Timing Diagram. • In Table 40, removed note 1 and renumbered remaining note. • Update Section 22, “Device Nomenclature,” with regards to Commercial Tier.
1	06/2008	Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value Improvement to Section 16, “High-Speed Serial Interfaces (HSSI) Update Figure 59 Mechanical Dimensions Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed
0	04/2008	Initial release.

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