

MPC885/MPC880 PowerQUICC Hardware Specifications

This hardware specification contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC885/MPC880. The MPC885 is the superset device of the MPC885/MPC880 family. The CPU on the MPC885/MPC880 is a 32-bit core built on Power Architecture™ technology that incorporates memory management units (MMUs) and instruction and data caches. For functional characteristics of the MPC885/MPC880, refer to the *MPC885 PowerQUICC Family Reference Manual*.

To locate published errata or updates for this document, refer to the MPC875/MPC870 product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

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1 Overview

The MPC885/MPC880 is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC885/MPC880 provides enhanced ATM functionality, an additional fast Ethernet controller, a USB, and an encryption block.

Table 1 shows the functionality supported by MPC885/MPC880.

Table 1. MPC885 Family

| Part | Cache (Kbytes) | | Ethernet | | SCC | SMC | USB | ATM Support | Security Engine |
|--------|----------------|---------|----------|--------|-----|-----|-----|---------------------------------|-----------------|
| | I Cache | D Cache | 10BaseT | 10/100 | | | | | |
| MPC885 | 8 | 8 | Up to 3 | 2 | 3 | 2 | 1 | Serial ATM and UTOPIA interface | Yes |
| MPC880 | 8 | 8 | Up to 2 | 2 | 2 | 2 | 1 | Serial ATM and UTOPIA interface | No |

2 Features

The MPC885/MPC880 is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communications processor module (CPM).

The following list summarizes the key MPC885/MPC880 features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
 - The 133-MHz core frequency supports 2:1 mode only.
 - The 66-/80-MHz core frequencies support both the 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the Power Architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
 - The core performs branch prediction with conditional prefetch and without conditional execution.
 - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
 - Instruction cache is two-way, set-associative with 256 sets in 2 blocks
 - Data cache is two-way, set-associative with 256 sets
 - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
 - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
 - MMUs with 32-entry TLB, fully associative instruction and data TLBs
 - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
 - Advanced on-chip emulation debug mode

- Provides enhanced ATM functionality found on the MPC862 and MPC866 families and includes the following:
 - Improved operation, administration and maintenance (OAM) support
 - OAM performance monitoring (PM) support
 - Multiple APC priority levels available to support a range of traffic pace requirements
 - Port-to-port switching capability without the need for RAM-based microcode
 - Simultaneous MII (100BaseT) and UTOPIA (half- or full -duplex) capability
 - Optional statistical cell counters per PHY
 - UTOPIA L2-compliant interface with added FIFO buffering to reduce the total cell transmission time and multi-PHY support. (The earlier UTOPIA L1 specification is also supported.)
 - Parameter RAM for both SPI and I²C can be relocated without RAM-based microcode
 - Supports full-duplex UTOPIA master (ATM side) and slave (PHY side) operations using a split bus
 - AAL2/VBR functionality is ROM-resident
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- Thirty-two address lines
- Memory controller (eight banks)
 - Contains complete dynamic RAM (DRAM) controller
 - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
 - Up to 30 wait states programmable per memory bank
 - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
 - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes (32 Kbytes–256 Mbytes)
 - Selectable write protection
 - On-chip bus arbitration logic
- General-purpose timers
 - Four 16-bit timers or two 32-bit timers
 - Gate mode can enable/disable counting.
 - Interrupt can be masked on reference match and event capture
- Two fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS that interface through MII and/or RMI interfaces
- System integration unit (SIU)
 - Bus monitor
 - Software watchdog

- Periodic interrupt timer (PIT)
- Clock synthesizer
- Decrementer and time base
- Reset controller
- IEEE Std 1149.1™ test access port (JTAG)
- Security engine is optimized to handle all the algorithms associated with IPsec, SSL/TLS, SRTP, IEEE Std 802.11i™, and iSCSI processing. Available on the MPC885, the security engine contains a crypto-channel, a controller, and a set of crypto hardware accelerators (CHAs). The CHAs are:
 - Data encryption standard execution unit (DEU)
 - DES, 3DES
 - Two key (K1, K2, K1) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, and counter modes
 - 128-, 192-, and 256- bit key lengths
 - Message digest execution unit (MDEU)
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Crypto-channel supporting multi-command descriptor chains
 - Integrated controller managing internal resources and bus mastering
 - Buffer size of 256 bytes for the DEU, AESU, and MDEU, with flow control for large data sizes
- Interrupts
 - Six external interrupt request (IRQ) lines
 - 12 port pins with interrupt capability
 - 23 internal interrupt sources
 - Programmable priority between SCCs
 - Programmable highest priority request
- Communications processor module (CPM)
 - RISC controller
 - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
 - Supports continuous mode transmission and reception on all serial channels
 - 8-Kbytes of dual-port RAM
 - Several serial DMA (SDMA) channels to support the CPM
 - Three parallel I/O registers with open-drain capability

- On-chip 16 × 16 multiply accumulate controller (MAC)
 - One operation per clock (two-clock latency, one-clock blockage)
 - MAC operates concurrently with other instructions
 - FIR loop—Four clocks per four multiplies
- Four baud rate generators
 - Independent (can be connected to any SCC or SMC)
 - Allow changes during operation
 - Autobaud support option
- Up to three serial communication controllers (SCCs) supporting the following protocols:
 - Serial ATM capability on SCCs
 - Optional UTOPIA port on SCC4
 - Ethernet/IEEE Std 802.3™ optional on the SCC(s) supporting full 10-Mbps operation
 - HDLC/SDLC
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC to support point-to-point protocol (PPP)
 - AppleTalk
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Binary synchronous communication (BISYNC)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- Up to two serial management channels (SMCs) supporting the following protocols:
 - UART (low-speed operation)
 - Transparent
 - General circuit interface (GCI) controller
 - Provide management for BRI devices as GCI controller in time-division multiplexed (TDM) channels
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loop-back diagnostics)
 - USB 2.0 full-/low-speed compatible
 - The USB function mode has the following features:
 - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers.
 - CRC16 generation and checking
 - CRC5 checking
 - NRZI encoding/decoding with bit stuffing
 - 12- or 1.5-Mbps data rate

- Flexible data buffers with multiple buffers per frame
 - Automatic retransmission upon transmit error
- The USB host controller has the following features:
 - Supports control, bulk, interrupt, and isochronous data transfers
 - CRC16 generation and checking
 - NRZI encoding/decoding with bit stuffing
 - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
 - Flexible data buffers with multiple buffers per frame
 - Supports local loop back mode for diagnostics (12 Mbps only)
- Serial peripheral interface (SPI)
 - Supports master and slave modes
 - Supports multiple-master operation on the same bus
- Inter-integrated circuit (I²C) port
 - Supports master and slave modes
 - Supports a multiple-master environment
- Time-slot assigner (TSA)
 - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame synchronization, and clocking
 - Allows dynamic changes
 - Can be internally connected to four serial channels (two SCCs and two SMCs)
- Parallel interface port (PIP)
 - Centronics interface support
 - Supports fast connection between compatible ports on MPC885/MPC880 and other MPC8xx devices
- PCMCIA interface
 - Master (socket) interface, release 2.1-compliant
 - Supports two independent PCMCIA sockets
 - 8 memory or I/O windows supported
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
 - Supports conditions: = ≠ < >
 - Each watchpoint can generate a break point internally.
- Normal high and normal low power modes to conserve power

- 1.8-V core and 3.3-V I/O operation
- The MPC885/MPC880 comes in a 357-pin ball grid array (PBGA) package

The MPC885 block diagram is shown in [Figure 1](#).

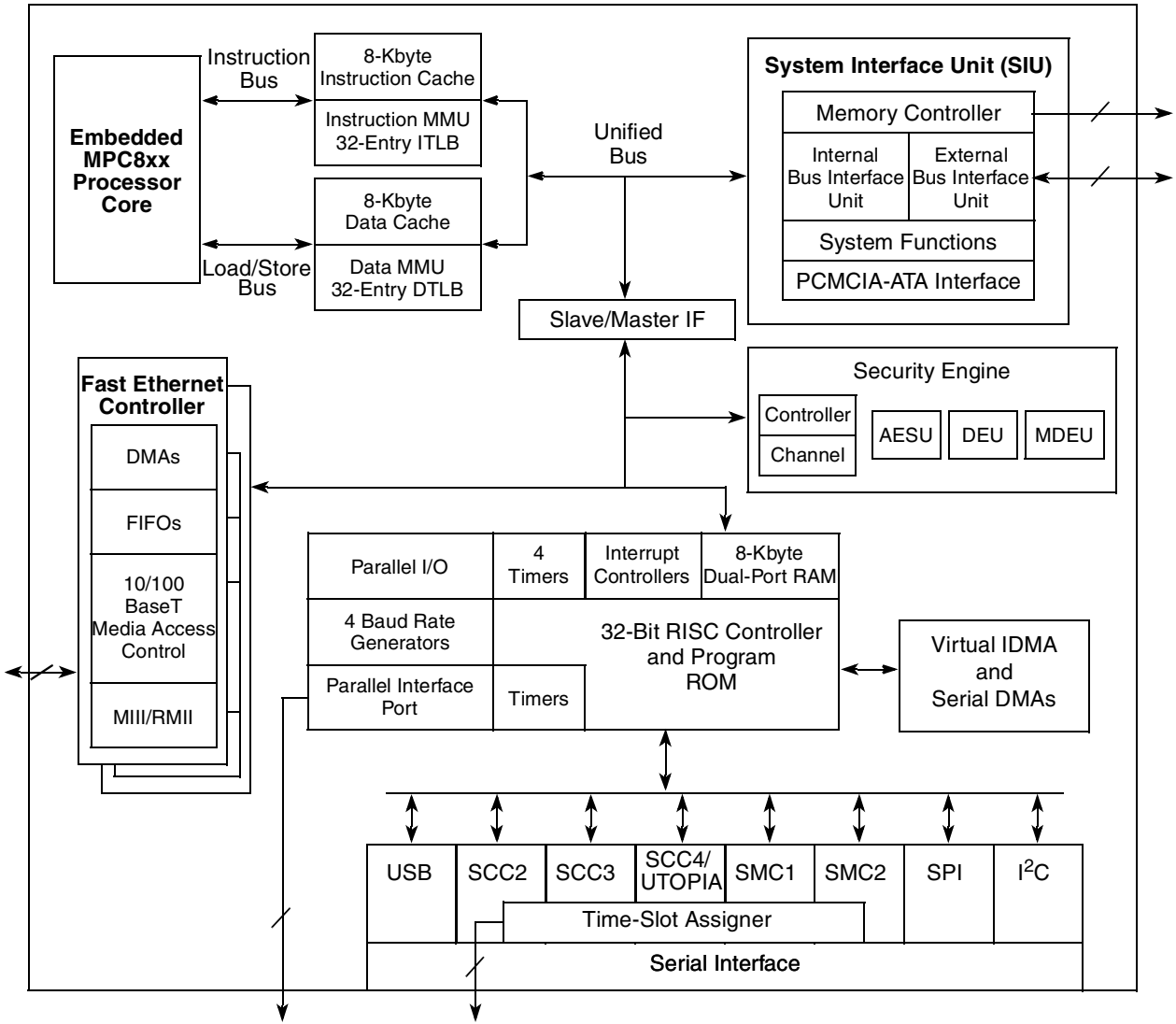


Figure 1. MPC885 Block Diagram

The MPC880 block diagram is shown in [Figure 2](#).

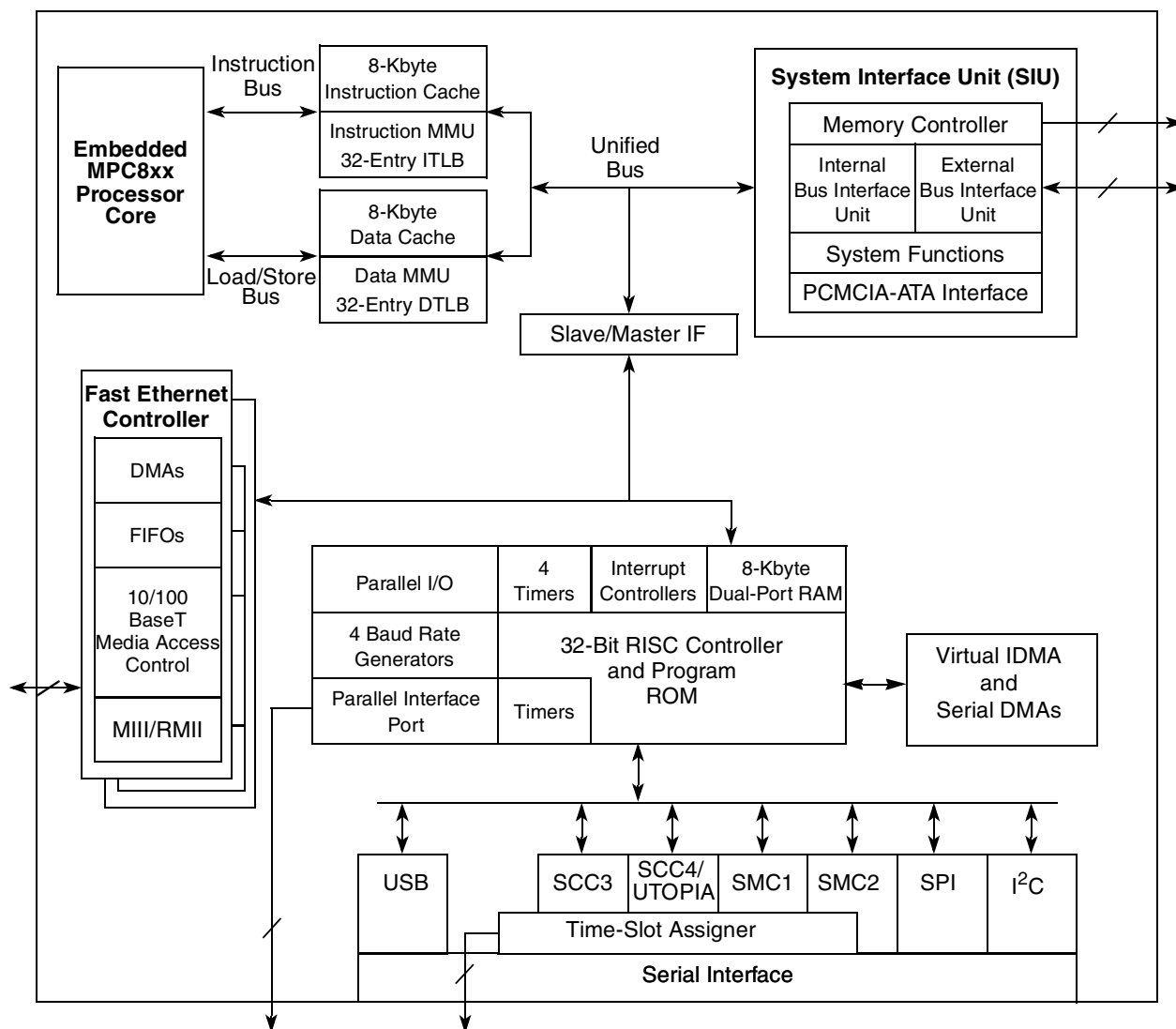


Figure 2. MPC880 Block Diagram

3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC885/MPC880. Table 2 displays the maximum tolerated ratings, and Table 3 displays the operating temperatures.

Table 2. Maximum Tolerated Ratings

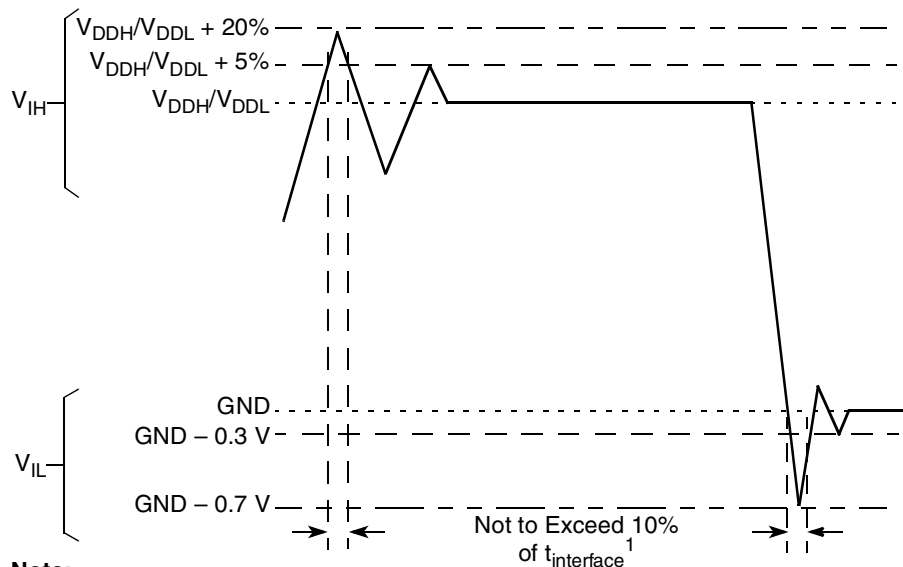
| Rating | Symbol | Value | Unit |
|-----------------------------|--|------------------------|------|
| Supply voltage ¹ | V_{DDH} | -0.3 to 4.0 | V |
| | V_{DDL} | -0.3 to 2.0 | V |
| | V_{DDSYN} | -0.3 to 2.0 | V |
| | Difference between V_{DDL} and V_{DDSYN} | <100 | mV |
| Input voltage ² | V_{in} | GND - 0.3 to V_{DDH} | V |
| Storage temperature range | T_{stg} | -55 to +150 | °C |

¹ The power supply of the device must start its ramp from 0.0 V.

² Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. See Section 8, "Power Supply and Power Sequencing."

Caution: All inputs that tolerate 5 V cannot be more than 2.5 V greater than V_{DDH} . This restriction applies to power up and normal operation (that is, if the MPC885/MPC880 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

Figure 3 shows the undershoot and overshoot voltages at the interfaces of the MPC885/MPC880.



Note:

1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 3. Undershoot/Overshoot Voltage for V_{DDH} and V_{DDL}

Table 3. Operating Temperatures

| Rating | Symbol | Value | Unit |
|-------------------------------------|---------------|-------|------|
| Temperature ¹ (standard) | $T_{A(\min)}$ | 0 | °C |
| | $T_{J(\max)}$ | 95 | °C |
| Temperature (extended) | $T_{A(\min)}$ | -40 | °C |
| | $T_{J(\max)}$ | 100 | °C |

¹ Minimum temperatures are guaranteed as ambient temperature, T_A . Maximum temperatures are guaranteed as junction temperature, T_J .

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC885/MPC880.

Table 4. MPC885/MPC880 Thermal Resistance Data

| Rating | Environment | | Symbol | Value | Unit |
|--------------------------------------|----------------------|-------------------------|-------------------------------|-------|------|
| Junction-to-ambient ¹ | Natural convection | Single-layer board (1s) | $R_{\theta JA}$ ² | 37 | °C/W |
| | | Four-layer board (2s2p) | $R_{\theta JMA}$ ³ | 25 | |
| | Airflow (200 ft/min) | Single-layer board (1s) | $R_{\theta JMA}$ ³ | 30 | |
| | | Four-layer board (2s2p) | $R_{\theta JMA}$ ³ | 22 | |
| Junction-to-board ⁴ | — | — | $R_{\theta JB}$ | 17 | |
| Junction-to-case ⁵ | — | — | $R_{\theta JC}$ | 10 | |
| Junction-to-package top ⁶ | Natural convection | — | Ψ_{JT} | 2 | |
| | Airflow (200 ft/min) | — | Ψ_{JT} | 2 | |

¹ Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5 Power Dissipation

Table 5 provides information on power dissipation. The modes are 1:1, where CPU and bus speeds are equal, and 2:1, where CPU frequency is twice bus speed.

Table 5. Power Dissipation (P_D)

| Die Revision | Bus Mode | CPU Frequency | Typical ¹ | Maximum ² | Unit |
|--------------|----------|---------------|----------------------|----------------------|------|
| 0 | 1:1 | 66 MHz | 310 | 390 | mW |
| | | 80 MHz | 350 | 430 | mW |
| | 2:1 | 133 MHz | 430 | 495 | mW |

¹ Typical power dissipation at $V_{DDL} = V_{DDSYN} = 1.8$ V, and V_{DDH} is at 3.3 V.

² Maximum power dissipation at $V_{DDL} = V_{DDSYN} = 1.9$ V, and V_{DDH} is at 3.5 V.

NOTE

The values in Table 5 represent V_{DDL} -based power dissipation and do not include I/O power dissipation over V_{DDH} . I/O power dissipation varies widely by application due to buffer current, depending on external circuitry.

The V_{DDSYN} power dissipation is negligible.

6 DC Characteristics

Table 6 provides the DC electrical characteristics for the MPC885/MPC880.

Table 6. DC Electrical Specifications

| Characteristic | Symbol | Min | Max | Unit |
|---|--|-----------------------|-----------|---------|
| Operating voltage | V_{DDL} (core) | 1.7 | 1.9 | V |
| | V_{DDH} (I/O) | 3.135 | 3.465 | V |
| | V_{DDSYN} ¹ | 1.7 | 1.9 | V |
| | Difference between V_{DDL} and V_{DDSYN} | — | 100 | mV |
| Input high voltage (all inputs except EXTAL and EXTCLK) ² | V_{IH} | 2.0 | 3.465 | V |
| Input low voltage ³ | V_{IL} | GND | 0.8 | V |
| EXTAL, EXTCLK input high voltage | V_{IHC} | $0.7 \cdot (V_{DDH})$ | V_{DDH} | V |
| Input leakage current, $V_{in} = 5.5$ V (except TMS, \overline{TRST} , DSCK and DSDI pins) for 5-V tolerant pins ² | I_{in} | — | 100 | μ A |
| Input leakage current, $V_{in} = V_{DDH}$ (except TMS, \overline{TRST} , DSCK, and DSDI) | I_{in} | — | 10 | μ A |
| Input leakage current, $V_{in} = 0$ V (except TMS, \overline{TRST} , DSCK and DSDI pins) | I_{in} | — | 10 | μ A |
| Input capacitance ⁴ | C_{in} | — | 20 | pF |

Table 6. DC Electrical Specifications (continued)

| Characteristic | Symbol | Min | Max | Unit |
|--|----------|-----|-----|------|
| Output high voltage, $I_{OH} = -2.0$ mA, except XTAL and open-drain pins | V_{OH} | 2.4 | — | V |
| Output low voltage $I_{OL} = 2.0$ mA (CLKOUT) $I_{OL} = 3.2$ mA ⁵ $I_{OL} = 5.3$ mA ⁶ $I_{OL} = 7.0$ mA (TXD1/PA14, TXD2/PA12) $I_{OL} = 8.9$ mA (\overline{TS} , \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{HRESET} , \overline{SRESET}) | V_{OL} | — | 0.5 | V |

¹ The difference between V_{DDL} and V_{DDSYN} cannot be more than 100 mV.

² The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], PE(14:31), TDI, TDO, TCK, \overline{TRST} , TMS, MII1_TXEN, MII_MDIO are 5-V tolerant. The minimum voltage is still 2.0 V.

³ V_{IL} (max) for the I²C interface is 0.8 V rather than the 1.5 V as specified in the I²C standard.

⁴ Input capacitance is periodically sampled.

⁵ A(0:31), TSIZ0/REG, TSIZ1, D(0:31), $\overline{IRQ6}$, RD \overline{WR} , \overline{BURST} , IP_B(3:7), PA(0:11), PA13, PA15, PB(14:31), PC(4:15), PD(3:15), PE(14:31), MII1_CRS, MII_MDIO, MII1_TXEN, and MII1_COL.

⁶ $\overline{BDIP}/\overline{GPL_B}(5)$, \overline{BR} , \overline{BG} , $\overline{FRZ}/\overline{IRQ6}$, $\overline{CS}(0:7)$, $\overline{WE}(0:3)$, $\overline{BS_A}(0:3)$, $\overline{GPL_A0}/\overline{GPL_B0}$, $\overline{OE}/\overline{GPL_A1}/\overline{GPL_B1}$, $\overline{GPL_A}(2:3)/\overline{GPL_B}(2:3)/\overline{CS}(2:3)$, UPWAITA/ $\overline{GPL_A4}$, UPWAITB/ $\overline{GPL_B4}$, $\overline{GPL_A5}$, $\overline{ALE_A}$, $\overline{CE1_A}$, $\overline{CE2_A}$, OP(0:3), and BADDR(28:30).

7 Thermal Calculation and Measurement

For the following discussions, $P_D = (V_{DDL} \times I_{DDL}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

NOTE

The V_{DDSYN} power dissipation is negligible.

7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see [Figure 4](#).

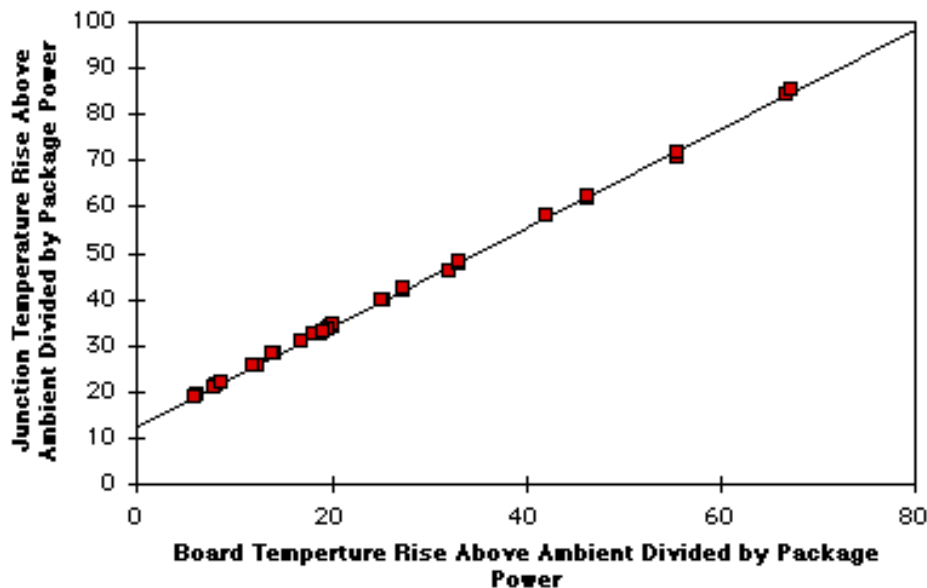


Figure 4. Effect of Board Temperature Rise on Thermal Behavior

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance ($^{\circ}\text{C}/\text{W}$)

T_B = board temperature ($^{\circ}\text{C}$)

P_D = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

Ψ_{JT} = thermal characterization parameter

T_T = thermocouple temperature on top of package

P_D = power dissipation in package

The thermal characterization parameter is measured per the JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
 805 East Middlefield Rd
 Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
 (Available from Global Engineering Documents)303-397-7956

JEDEC Specifications <http://www.jedec.org>

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

8 Power Supply and Power Sequencing

This section provides design considerations for the MPC885/MPC880 power supply. The MPC885/MPC880 has a core voltage (V_{DDL}) and PLL voltage (V_{DDSYN}), which both operate at a lower voltage than the I/O voltage V_{DDH} . The I/O section of the MPC885/MPC880 is supplied with 3.3 V across V_{DDH} and V_{SS} (GND).

The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5 V tolerant. All inputs cannot be more than 2.5 V greater than V_{DDH} . In addition, 5-V tolerant pins cannot exceed 5.5 V and remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- V_{DDL} must not exceed V_{DDH} during power up and power down.
- V_{DDL} must not exceed 1.9 V, and V_{DDH} must not exceed 3.465 V.

These cautions are necessary for the long-term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased, and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown [Figure 5](#) can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power up, and the 1N5820 diodes regulate the maximum potential difference on power down.

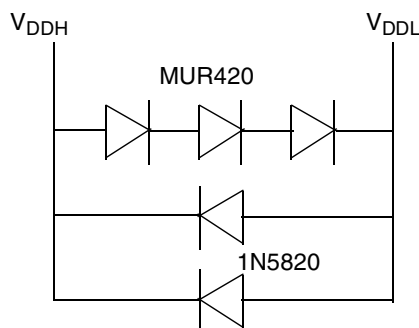


Figure 5. Example Voltage Sequencing Circuit

9 Layout Practices

Each V_{DD} pin on the MPC885/MPC880 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{DD} power supply should be bypassed to ground using at least four 0.1 μF by-pass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and GND should be kept to less than half an inch per capacitor lead. At a minimum, a four-layer board employing two inner layers as V_{DD} and GND planes should be used.

All output pins on the MPC885/MPC880 have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{DD} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to the *MPC885 PowerQUICC™ Family Reference Manual*, Section 14.4.3, "Clock Synthesizer Power (V_{DDSYN} , V_{SSSYN} , V_{SSSYN1})."

10 Bus Signal Timing

The maximum bus speed supported by the MPC885/MPC880 is 80 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC885/MPC880 used at 133 MHz must be configured for a 66 MHz bus). [Table 7](#) shows the frequency ranges for standard part frequencies in 1:1 bus mode, and [Table 8](#) shows the frequency ranges for standard part frequencies in 2:1 bus mode.

Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)

| Part Frequency | 66 MHz | | 80 MHz | |
|----------------|--------|-------|--------|-----|
| | Min | Max | Min | Max |
| Core frequency | 40 | 66.67 | 40 | 80 |
| Bus frequency | 40 | 66.67 | 40 | 80 |

Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)

| Part Frequency | 66 MHz | | 80 MHz | | 133 MHz | |
|----------------|--------|-------|--------|-----|---------|-----|
| | Min | Max | Min | Max | Min | Max |
| Core frequency | 40 | 66.67 | 40 | 80 | 40 | 133 |
| Bus frequency | 20 | 33.33 | 20 | 40 | 20 | 66 |

Table 9 provides the timings for the MPC885/MPC880 at 33-, 40-, 66-, and 80-MHz bus operation.

The timing for the MPC885/MPC880 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load for maximum delays and a 50-pF load for minimum delays.

Table 9. Bus Operation Timings

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|-----|---|--------|------|--------|------|--------|------|--------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B1 | Bus period (CLKOUT), see Table 7 | — | — | — | — | — | — | — | — | ns |
| B1a | EXTCLK to CLKOUT phase skew - If CLKOUT is an integer multiple of EXTCLK, then the rising edge of EXTCLK is aligned with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew. | -2 | +2 | -2 | +2 | -2 | +2 | -2 | +2 | ns |
| B1b | CLKOUT frequency jitter peak-to-peak | — | 1 | — | 1 | — | 1 | — | 1 | ns |
| B1c | Frequency jitter on EXTCLK | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |
| B1d | CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz | — | 4 | — | 4 | — | 4 | — | 4 | ns |
| | CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz | — | 5 | — | 5 | — | 5 | — | 5 | ns |
| B2 | CLKOUT pulse width low (MIN = 0.4 × B1, MAX = 0.6 × B1) | 12.1 | 18.2 | 10.0 | 15.0 | 6.1 | 9.1 | 5.0 | 7.5 | ns |
| B3 | CLKOUT pulse width high (MIN = 0.4 × B1, MAX = 0.6 × B1) | 12.1 | 18.2 | 10.0 | 15.0 | 6.1 | 9.1 | 5.0 | 7.5 | ns |
| B4 | CLKOUT rise time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |

Table 9. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|------|--|--------|-------|--------|-------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B5 | CLKOUT fall time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B7 | CLKOUT to A(0:31), BADDR(28:30), RD \overline{WR} , \overline{BURST} , D(0:31) output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B7a | CLKOUT to TSIZ(0:1), \overline{REG} , \overline{RSV} , \overline{BDIP} , PTR output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B7b | CLKOUT to \overline{BR} , \overline{BG} , FRZ, VFLS(0:1), VF(0:2) IWP(0:2), LWP(0:1), \overline{STS} output hold (MIN = 0.25 × B1) | 7.60 | — | 6.30 | — | 3.80 | — | 3.13 | — | ns |
| B8 | CLKOUT to A(0:31), BADDR(28:30) RD \overline{WR} , \overline{BURST} , D(0:31) valid (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B8a | CLKOUT to TSIZ(0:1), \overline{REG} , \overline{RSV} , AT(0:3) \overline{BDIP} , PTR valid (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B8b | CLKOUT to \overline{BR} , \overline{BG} , VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), \overline{STS} valid ⁴ (MAX = 0.25 × B1 + 6.3) | — | 13.80 | — | 12.50 | — | 10.00 | — | 9.43 | ns |
| B9 | CLKOUT to A(0:31), BADDR(28:30), RD \overline{WR} , \overline{BURST} , D(0:31), TSIZ(0:1), \overline{REG} , \overline{RSV} , AT(0:3), PTR High-Z (MAX = 0.25 × B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.43 | ns |
| B11 | CLKOUT to \overline{TS} , \overline{BB} assertion (MAX = 0.25 × B1 + 6.0) | 7.60 | 13.60 | 6.30 | 12.30 | 3.80 | 9.80 | 3.13 | 9.13 | ns |
| B11a | CLKOUT to \overline{TA} , \overline{BI} assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.30 ¹) | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.30 | ns |
| B12 | CLKOUT to \overline{TS} , \overline{BB} negation (MAX = 0.25 × B1 + 4.8) | 7.60 | 12.30 | 6.30 | 11.00 | 3.80 | 8.50 | 3.13 | 7.92 | ns |
| B12a | CLKOUT to \overline{TA} , \overline{BI} negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 × B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.5 | 9.00 | ns |
| B13 | CLKOUT to \overline{TS} , \overline{BB} High-Z (MIN = 0.25 × B1) | 7.60 | 21.60 | 6.30 | 20.30 | 3.80 | 14.00 | 3.13 | 12.93 | ns |
| B13a | CLKOUT to \overline{TA} , \overline{BI} High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 × B1 + 2.5) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.5 | 15.00 | ns |
| B14 | CLKOUT to \overline{TEA} assertion (MAX = 0.00 × B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | ns |
| B15 | CLKOUT to \overline{TEA} High-Z (MIN = 0.00 × B1 + 2.50) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B16 | \overline{TA} , \overline{BI} valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6 | — | ns |
| B16a | \overline{TEA} , \overline{KR} , \overline{RETRY} , \overline{CR} valid to CLKOUT (setup time) (MIN = 0.00 × B1 + 4.5) | 4.50 | — | 4.50 | — | 4.50 | — | 4.50 | — | ns |

Table 9. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|------|---|--------|-------|--------|-------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B16b | \overline{BB} , \overline{BG} , \overline{BR} , valid to CLKOUT (setup time) ² (4MIN = 0.00 × B1 + 0.00) | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B17 | CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (hold time) (MIN = 0.00 × B1 + 1.00 ³) | 1.00 | — | 1.00 | — | 2.00 | — | 2.00 | — | ns |
| B17a | CLKOUT to \overline{KR} , \overline{RETRY} , \overline{CR} valid (hold time) (MIN = 0.00 × B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B18 | D(0:31) valid to CLKOUT rising edge (setup time) ⁴ (MIN = 0.00 × B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B19 | CLKOUT rising edge to D(0:31) valid (hold time) ⁴ (MIN = 0.00 × B1 + 1.00 ⁵) | 1.00 | — | 1.00 | — | 2.00 | — | 2.00 | — | ns |
| B20 | D(0:31) valid to CLKOUT falling edge (setup time) ⁶ (MIN = 0.00 × B1 + 4.00) | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B21 | CLKOUT falling edge to D(0:31) valid (hold time) ⁶ (MIN = 0.00 × B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B22 | CLKOUT rising edge to \overline{CS} asserted GPCM ACS = 00 (MAX = 0.25 × B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.43 | ns |
| B22a | CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 10, TRLX = [0 or 1] (MAX = 0.00 × B1 + 8.00) | — | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | ns |
| B22b | CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = [0 or 1], EBDF = 0 (MAX = 0.25 × B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.43 | ns |
| B22c | CLKOUT falling edge to \overline{CS} asserted GPCM ACS = 11, TRLX = [0 or 1], EBDF = 1 (MAX = 0.375 × B1 + 6.6) | 10.90 | 18.00 | 10.90 | 16.00 | 5.20 | 12.30 | 4.69 | 10.93 | ns |
| B23 | CLKOUT rising edge to \overline{CS} negated GPCM read access, GPCM write access ACS = 00 and CSNT = 0 (MAX = 0.00 × B1 + 8.00) | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | ns |
| B24 | A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 × B1 – 2.00) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B24a | A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11 TRLX = 0 (MIN = 0.50 × B1 – 2.00) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B25 | CLKOUT rising edge to \overline{OE} , \overline{WE} (0:3) asserted (MAX = 0.00 × B1 + 9.00) | — | 9.00 | — | 9.00 | — | 9.00 | — | 9.00 | ns |
| B26 | CLKOUT rising edge to \overline{OE} negated (MAX = 0.00 × B1 + 9.00) | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | ns |
| B27 | A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 × B1 – 2.00) | 35.90 | — | 29.30 | — | 16.90 | — | 13.60 | — | ns |

Table 9. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|------|--|--------|-------|--------|-------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B27a | A(0:31) and BADDR(28:30) to \overline{CS} asserted GPCM ACS = 11, TRLX = 1 (MIN = $1.50 \times B1 - 2.00$) | 43.50 | — | 35.50 | — | 20.70 | — | 16.75 | — | ns |
| B28 | CLKOUT rising edge to $\overline{WE}(0:3)$ negated GPCM write access CSNT = 0 (MAX = $0.00 \times B1 + 9.00$) | — | 9.00 | — | 9.00 | — | 9.00 | — | 9.00 | ns |
| B28a | CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, CSNT = 1, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 9.93 | ns |
| B28b | CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$) | — | 14.30 | — | 13.00 | — | 10.50 | — | 9.93 | ns |
| B28c | CLKOUT falling edge to $\overline{WE}(0:3)$ negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0, CSNT = 1, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$) | 10.90 | 18.00 | 10.90 | 18.00 | 5.20 | 12.30 | 4.69 | 11.29 | ns |
| B28d | CLKOUT falling edge to \overline{CS} negated GPCM write access TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = $0.375 \times B1 + 6.6$) | — | 18.00 | — | 18.00 | — | 12.30 | — | 11.30 | ns |
| B29 | $\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = $0.25 \times B1 - 2.00$) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B29a | $\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = $0.50 \times B1 - 2.00$) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B29b | \overline{CS} negated to D(0:31) High-Z GPCM write access, ACS = 00, TRLX = 0 & CSNT = 0 (MIN = $0.25 \times B1 - 2.00$) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B29c | \overline{CS} negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = $0.50 \times B1 - 2.00$) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B29d | $\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = $1.50 \times B1 - 2.00$) | 43.50 | — | 35.50 | — | 20.70 | — | 16.75 | — | ns |
| B29e | \overline{CS} negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0 (MIN = $1.50 \times B1 - 2.00$) | 43.50 | — | 35.50 | — | 20.70 | — | 16.75 | — | ns |
| B29f | $\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = $0.375 \times B1 - 6.30$) ⁷ | 5.00 | — | 3.00 | — | 0.00 | — | 0.00 | — | ns |
| B29g | \overline{CS} negated to D(0:31) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = $0.375 \times B1 - 6.30$) ⁷ | 5.00 | — | 3.00 | — | 0.00 | — | 0.00 | — | ns |

Table 9. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|------|--|--------|-------|--------|-------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B29h | $\overline{WE}(0:3)$ negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = $0.375 \times B1 - 3.30$) | 38.40 | — | 31.10 | — | 17.50 | — | 13.85 | — | ns |
| B29i | \overline{CS} negated to D(0:31) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = $0.375 \times B1 - 3.30$) | 38.40 | — | 31.10 | — | 17.50 | — | 13.85 | — | ns |
| B30 | \overline{CS} , $\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) Invalid GPCM read/write access ⁸ (MIN = $0.25 \times B1 - 2.00$) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B30a | $\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) Invalid GPCM, write access, TRLX = 0, CSNT = 1, \overline{CS} negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT = 1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = $0.50 \times B1 - 2.00$) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B30b | $\overline{WE}(0:3)$ negated to A(0:31) invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. \overline{CS} negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = $1.50 \times B1 - 2.00$) | 43.50 | — | 35.50 | — | 20.70 | — | 16.75 | — | ns |
| B30c | $\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. \overline{CS} negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = $0.375 \times B1 - 3.00$) | 8.40 | — | 6.40 | — | 2.70 | — | 1.70 | — | ns |
| B30d | $\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT = 1, \overline{CS} negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1 | 38.67 | — | 31.38 | — | 17.83 | — | 14.19 | — | ns |
| B31 | CLKOUT falling edge to \overline{CS} valid, as requested by control bit CST4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B31a | CLKOUT falling edge to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 10.00 | ns |
| B31b | CLKOUT rising edge to \overline{CS} valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 8.00$) | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B31c | CLKOUT rising edge to \overline{CS} valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.30$) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.40 | ns |
| B31d | CLKOUT falling edge to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = $0.375 \times B1 + 6.6$) | 13.30 | 18.00 | 11.30 | 16.00 | 7.60 | 12.30 | 4.69 | 11.30 | ns |

Table 9. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|------|---|--------|-------|--------|-------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B32 | CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B32a | CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = $0.25 \times B1 + 6.80$) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 10.00 | ns |
| B32b | CLKOUT rising edge to \overline{BS} valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 8.00$) | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B32c | CLKOUT rising edge to \overline{BS} valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 10.00 | ns |
| B32d | CLKOUT falling edge to \overline{BS} valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = $0.375 \times B1 + 6.60$) | 13.30 | 18.00 | 11.30 | 16.00 | 7.60 | 12.30 | 4.49 | 11.30 | ns |
| B33 | CLKOUT falling edge to \overline{GPL} valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = $0.00 \times B1 + 6.00$) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B33a | CLKOUT rising edge to \overline{GPL} valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = $0.25 \times B1 + 6.80$) | 7.60 | 14.30 | 6.30 | 13.00 | 3.80 | 10.50 | 3.13 | 10.00 | ns |
| B34 | A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B34a | A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = $0.50 \times B1 - 2.00$) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B34b | A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid, as requested by CST2 in the corresponding word in UPM (MIN = $0.75 \times B1 - 2.00$) | 20.70 | — | 16.70 | — | 9.40 | — | 6.80 | — | ns |
| B35 | A(0:31), BADDR(28:30) to \overline{CS} valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B35a | A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid, as requested by BST1 in the corresponding word in the UPM (MIN = $0.50 \times B1 - 2.00$) | 13.20 | — | 10.50 | — | 5.60 | — | 4.25 | — | ns |
| B35b | A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = $0.75 \times B1 - 2.00$) | 20.70 | — | 16.70 | — | 9.40 | — | 7.40 | — | ns |

Table 9. Bus Operation Timings (continued)

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|-----|--|--------|-----|--------|-----|--------|-----|--------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B36 | A(0:31), BADDR(28:30), and D(0:31) to \overline{GPL} valid, as requested by control bit GxT4 in the corresponding word in the UPM (MIN = $0.25 \times B1 - 2.00$) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| B37 | UPWAIT valid to CLKOUT falling edge ⁹ (MIN = $0.00 \times B1 + 6.00$) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B38 | CLKOUT falling edge to UPWAIT valid ⁹ (MIN = $0.00 \times B1 + 1.00$) | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| B39 | \overline{AS} valid to CLKOUT rising edge ¹⁰ (MIN = $0.00 \times B1 + 7.00$) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B40 | A(0:31), TSIZ(0:1), RD/ \overline{WR} , \overline{BURST} , valid to CLKOUT rising edge (MIN = $0.00 \times B1 + 7.00$) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B41 | \overline{TS} valid to CLKOUT rising edge (setup time) (MIN = $0.00 \times B1 + 7.00$) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B42 | CLKOUT rising edge to \overline{TS} valid (hold time) (MIN = $0.00 \times B1 + 2.00$) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B43 | \overline{AS} negation to memory controller signals negation (MAX = TBD) | — | TBD | — | TBD | — | TBD | — | TBD | ns |

¹ For part speeds above 50 MHz, use 9.80 ns for B11a.

² The timing required for \overline{BR} input is relevant when the MPC885/MPC880 is selected to work with the internal bus arbiter. The timing for \overline{BG} input is relevant when the MPC885/MPC880 is selected to work with the external bus arbiter.

³ For part speeds above 50 MHz, use 2 ns for B17.

⁴ The D(0:31) input timings B18 and B19 refer to the rising edge of the CLKOUT in which the \overline{TA} input signal is asserted.

⁵ For part speeds above 50 MHz, use 2 ns for B19.

⁶ The D(0:31) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the user-programmable machine (UPM) in the memory controller, for data beats where DLT3 = 1 in the RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

⁷ This formula applies to bus operation up to 50 MHz.

⁸ The timing B30 refers to \overline{CS} when ACS = 00 and to \overline{CS} and $\overline{WE}(0:3)$ when CSNT = 0.

⁹ The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in [Figure 21](#).

¹⁰ The \overline{AS} signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in [Figure 24](#).

Figure 6 provides the control timing diagram.

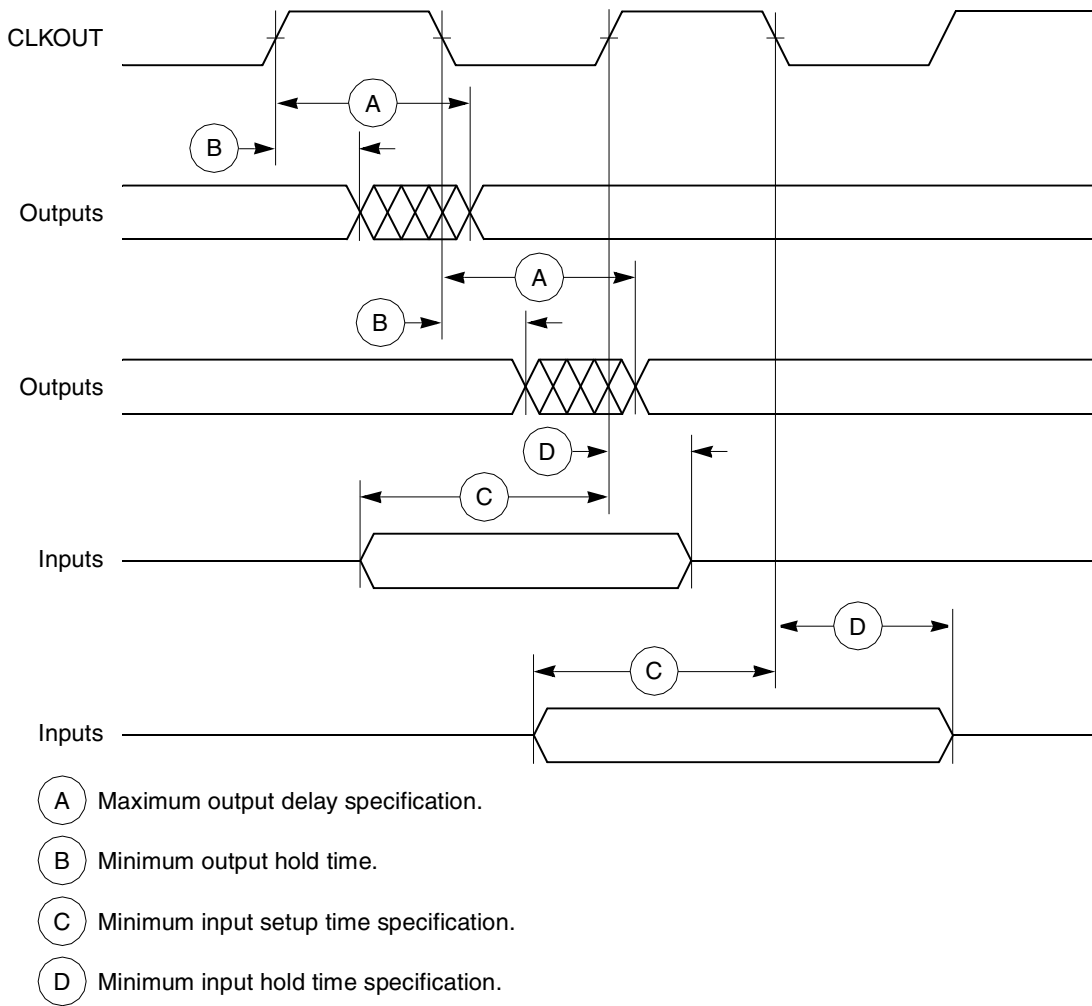


Figure 6. Control Timing

Figure 7 provides the timing for the external clock.

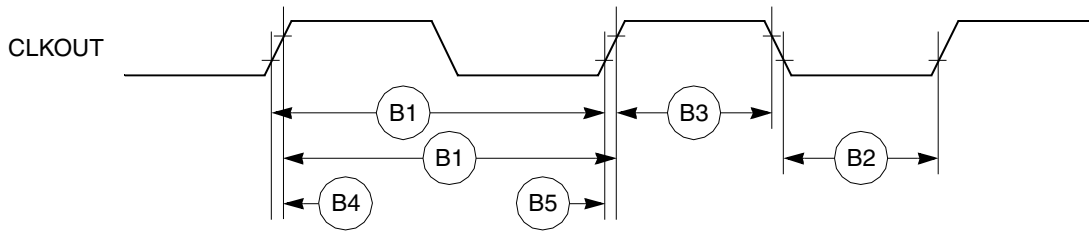


Figure 7. External Clock Timing

Figure 8 provides the timing for the synchronous output signals.

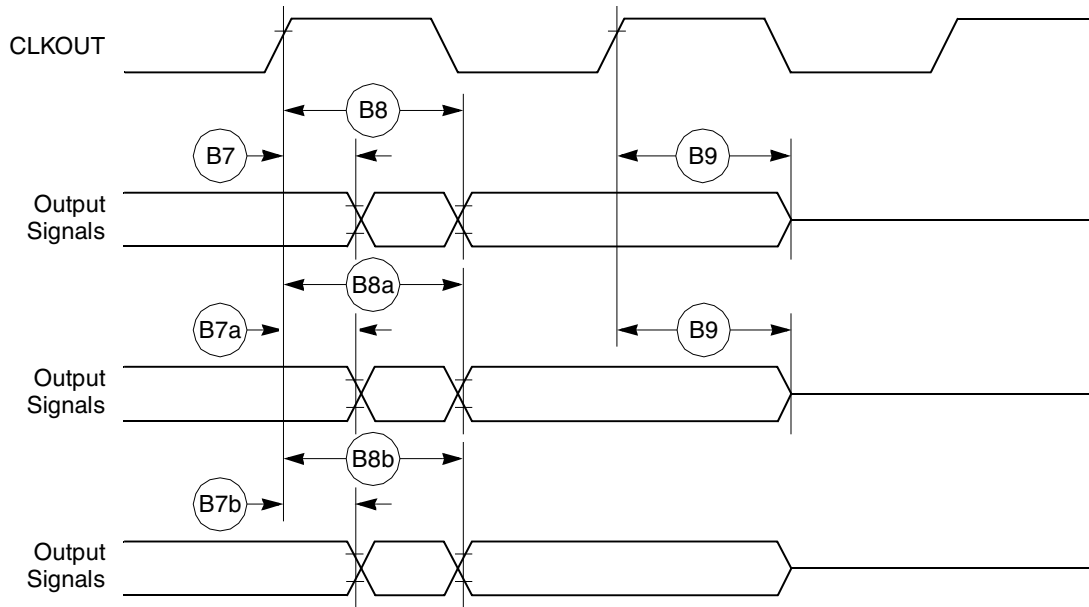


Figure 8. Synchronous Output Signals Timing

Figure 9 provides the timing for the synchronous active pull-up and open-drain output signals.

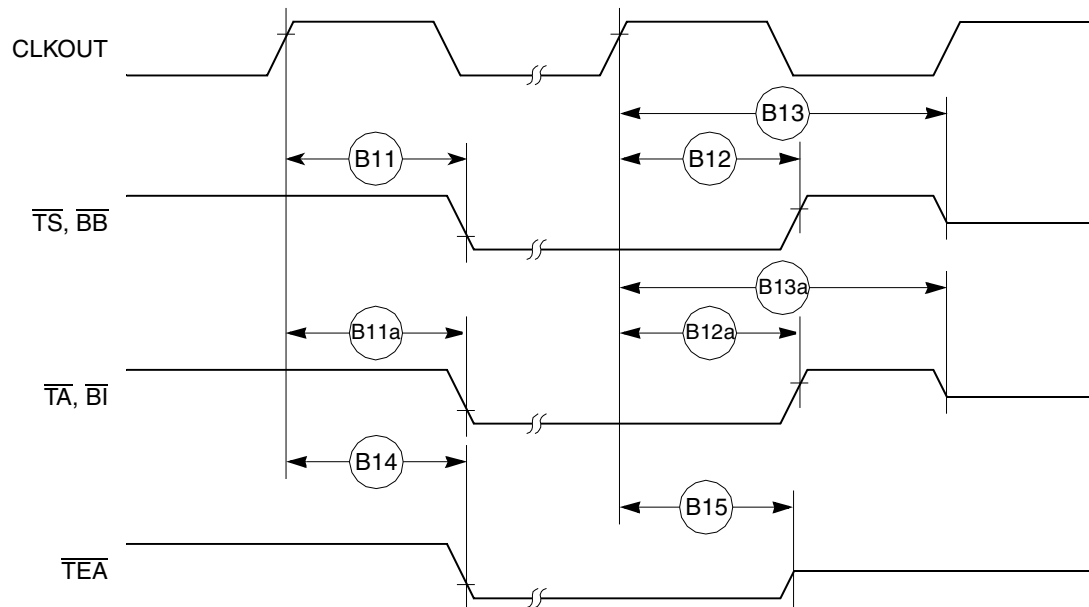


Figure 9. Synchronous Active Pull-Up Resistor and Open-Drain Outputs Signals Timing

Figure 10 provides the timing for the synchronous input signals.

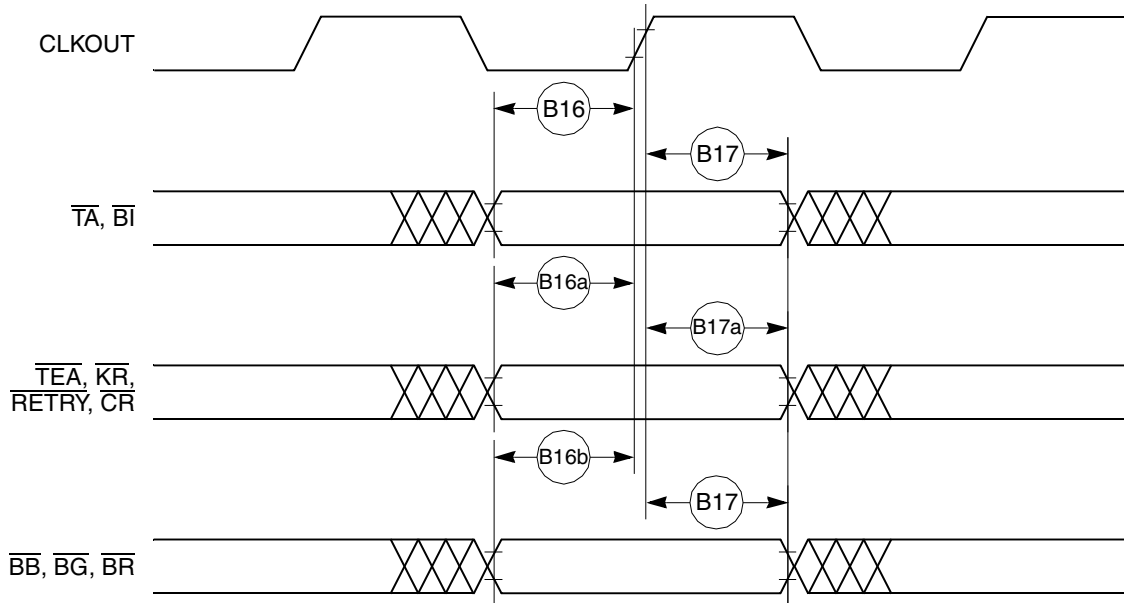


Figure 10. Synchronous Input Signals Timing

Figure 11 provides normal case timing for input data. It also applies to normal read accesses under the control of the user-programmable machine (UPM) in the memory controller.

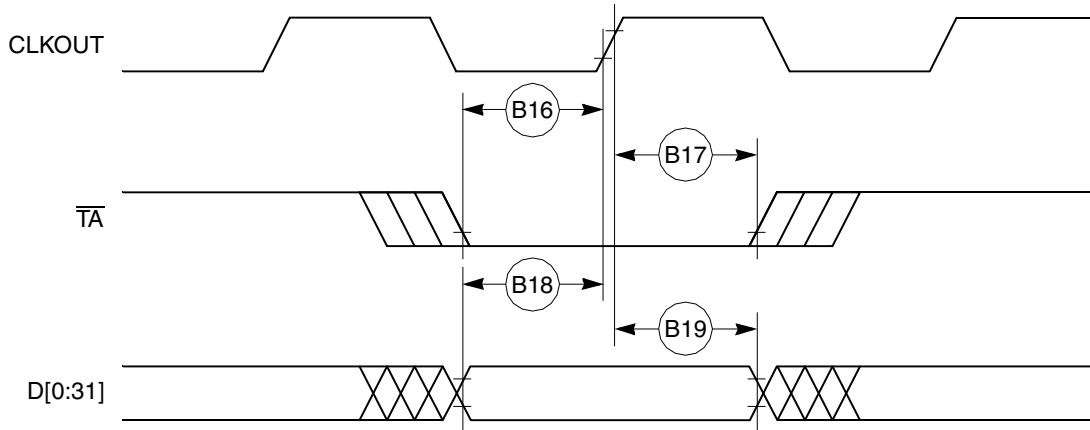


Figure 11. Input Data Timing in Normal Case

Figure 12 provides the timing for the input data controlled by the UPM for data beats where $DLT3 = 1$ in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

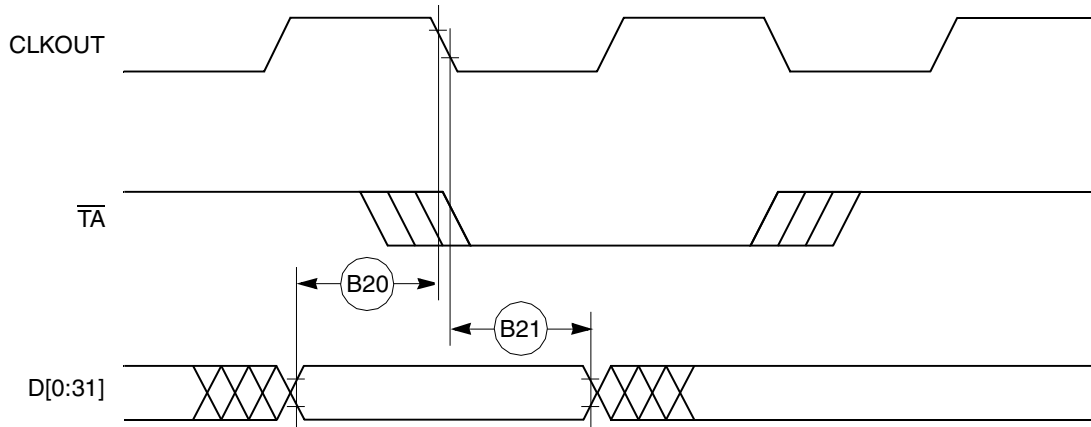


Figure 12. Input Data Timing when Controlled by UPM in the Memory Controller and $DLT3 = 1$

Figure 13 through Figure 16 provide the timing for the external bus read controlled by various GPCM factors.

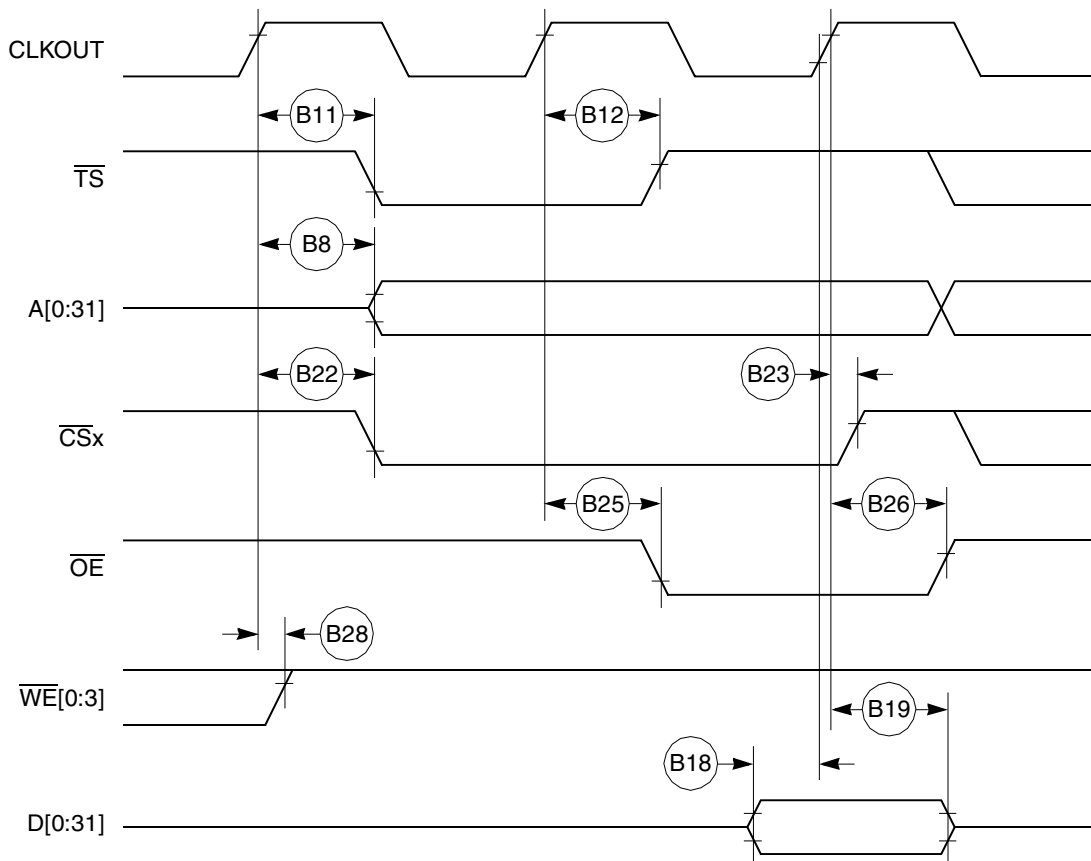


Figure 13. External Bus Read Timing (GPCM Controlled— $ACS = 00$)

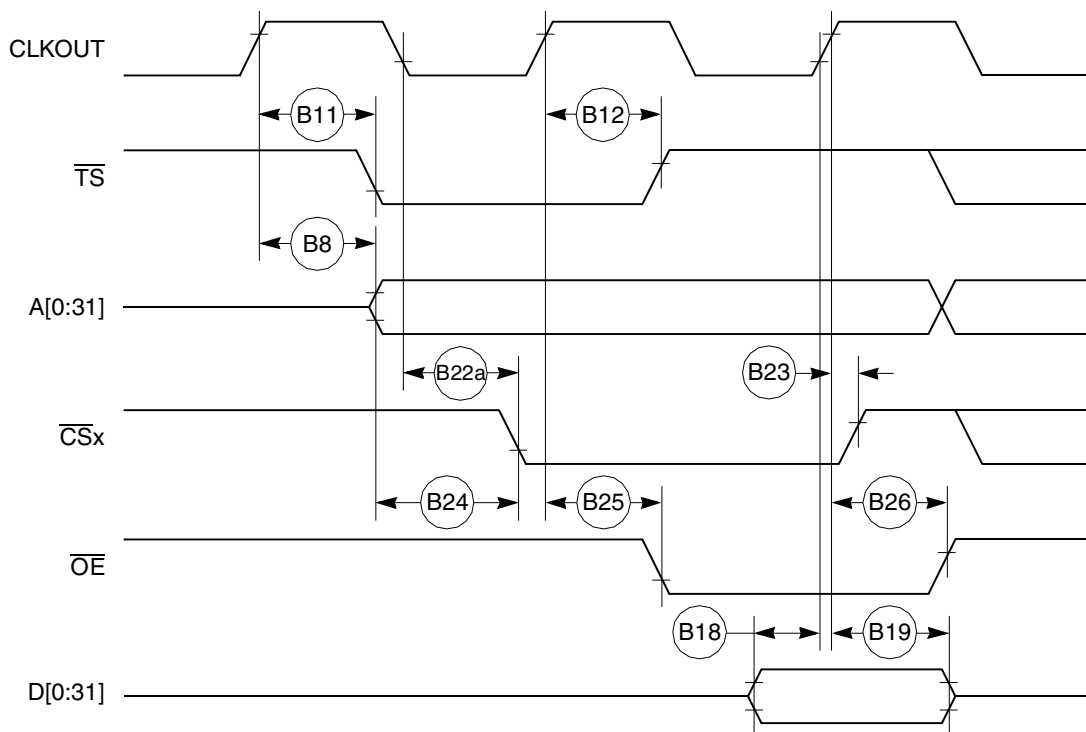


Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 10)

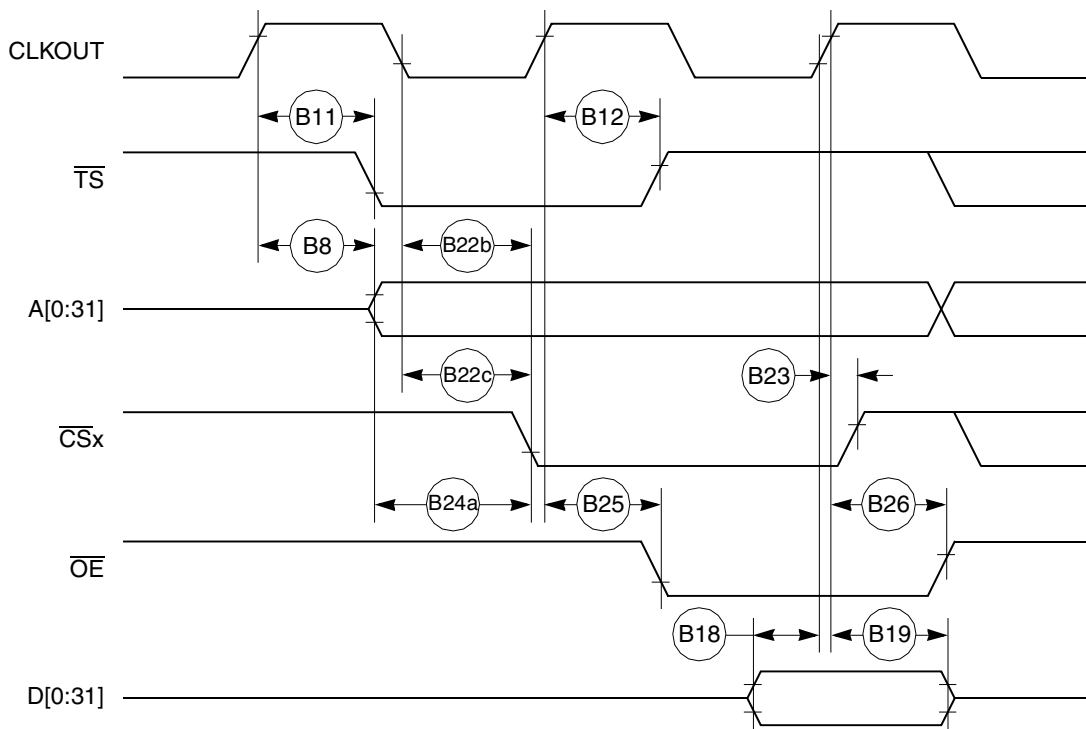


Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 0, ACS = 11)

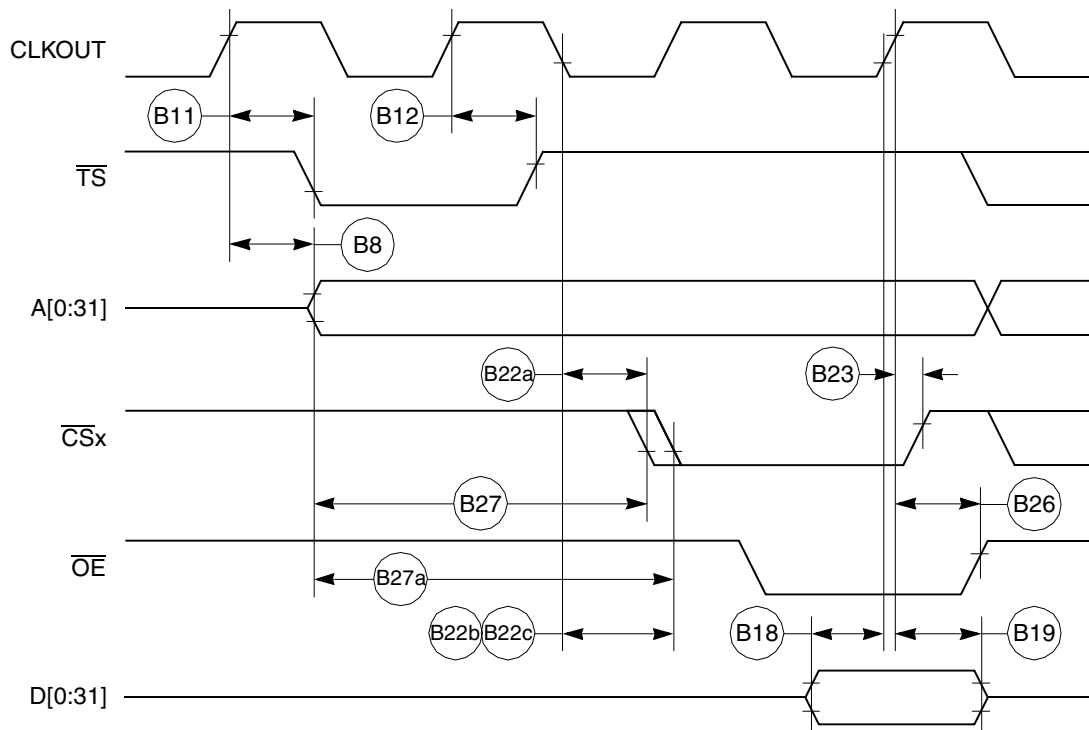


Figure 16. External Bus Read Timing (GPCM Controlled—TRLX = 1, ACS = 10, ACS = 11)

Figure 17 through Figure 19 provide the timing for the external bus write controlled by various GPCM factors.

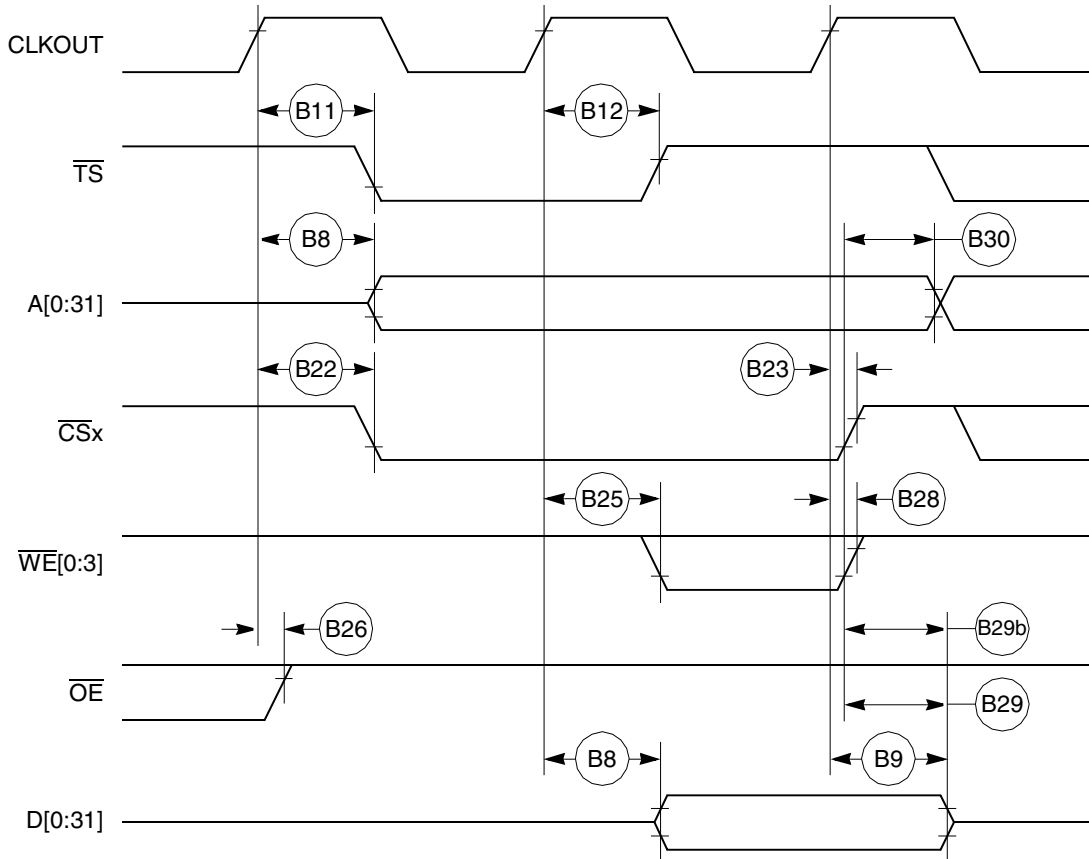


Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 0)

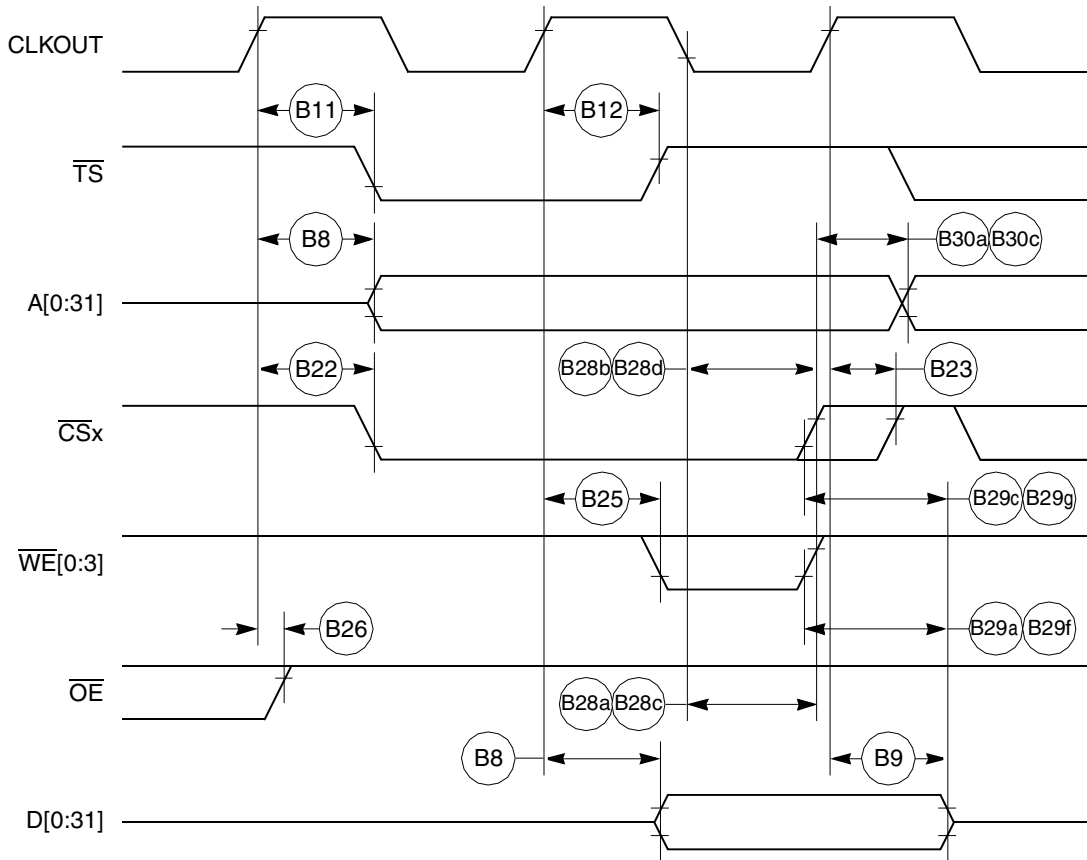


Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)

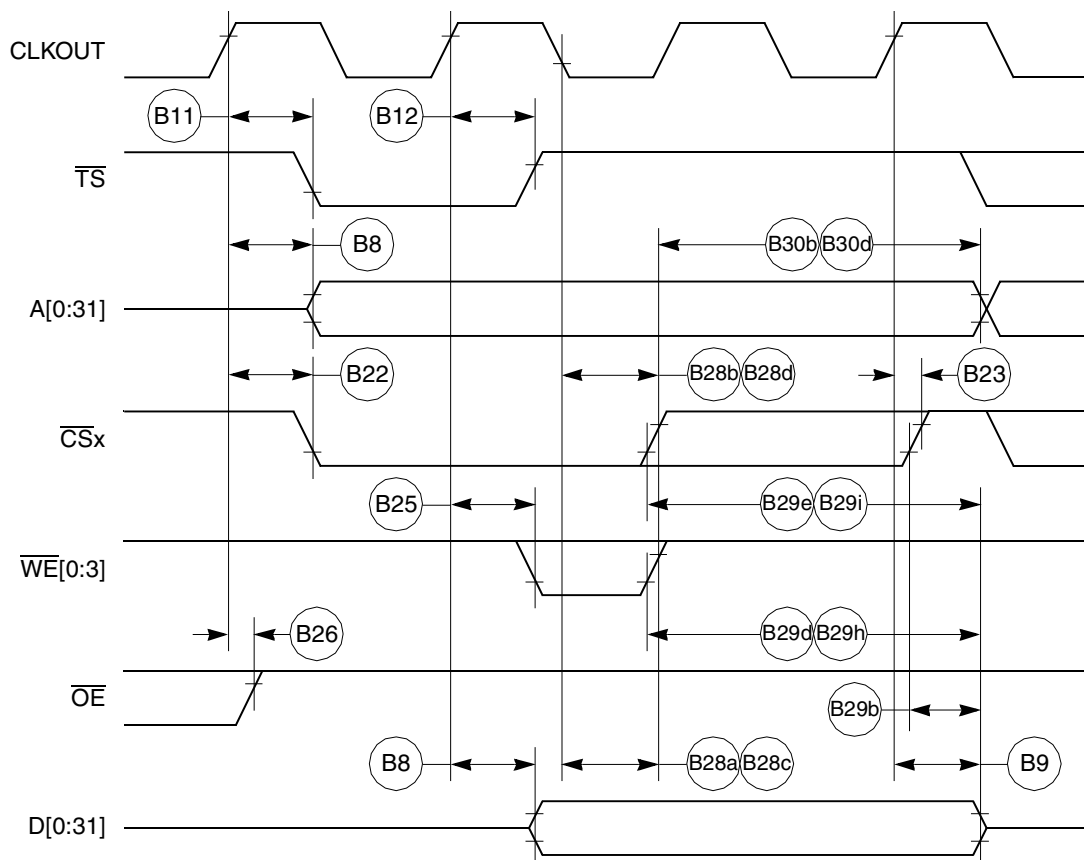


Figure 19. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)

Figure 20 provides the timing for the external bus controlled by the UPM.

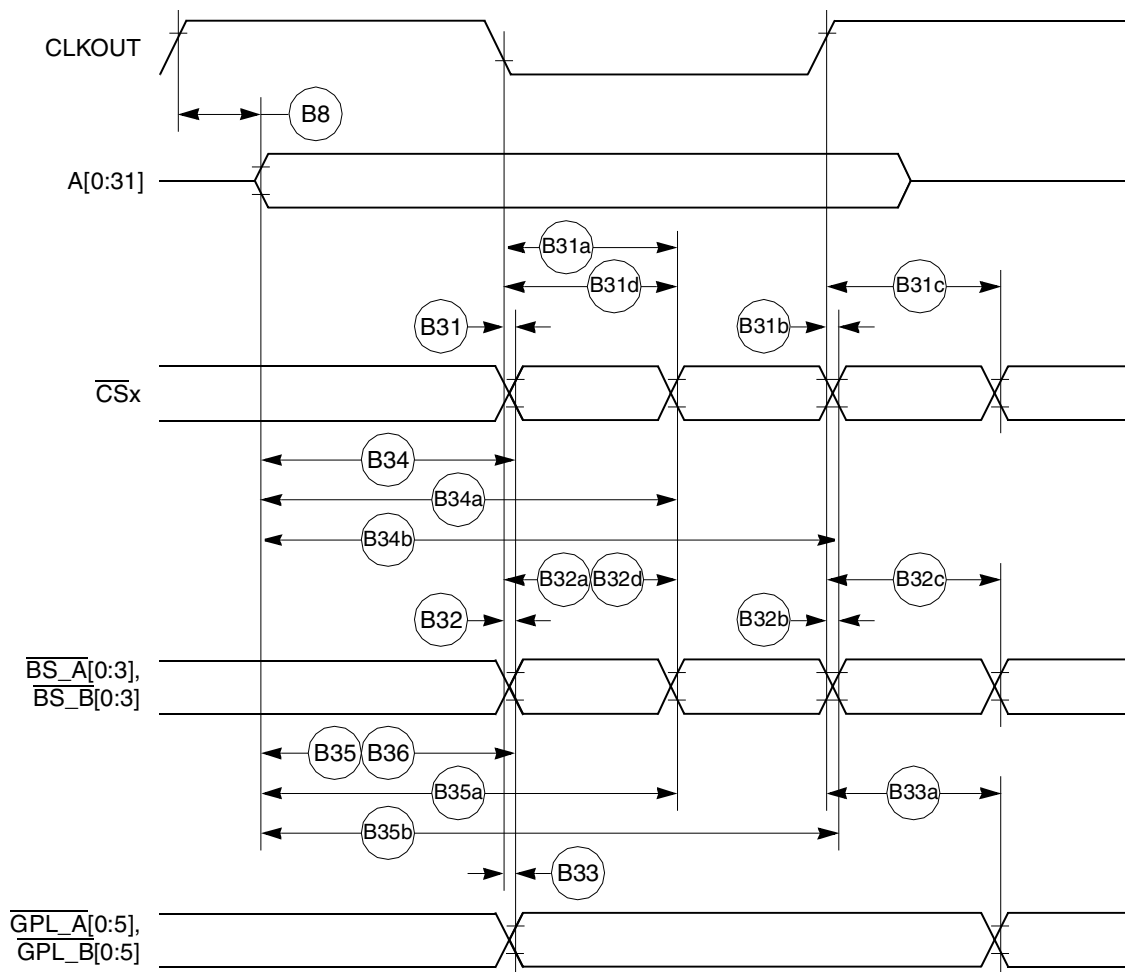


Figure 20. External Bus Timing (UPM-Controlled Signals)

Figure 21 provides the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

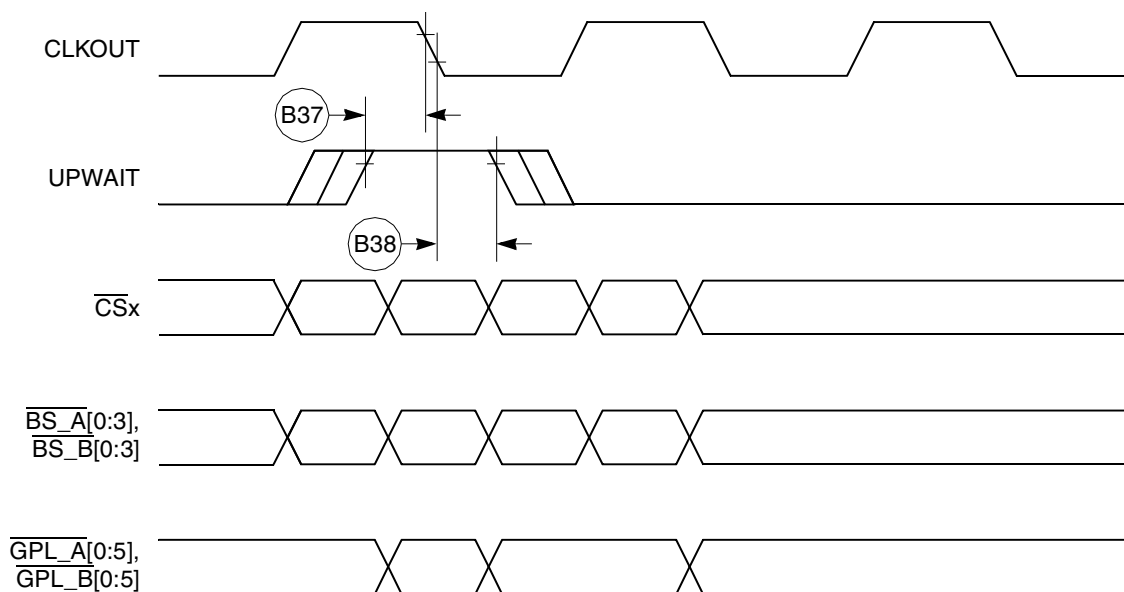


Figure 21. Asynchronous UPWAIT Asserted Detection in UPM-Handled Cycles Timing

Figure 22 provides the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

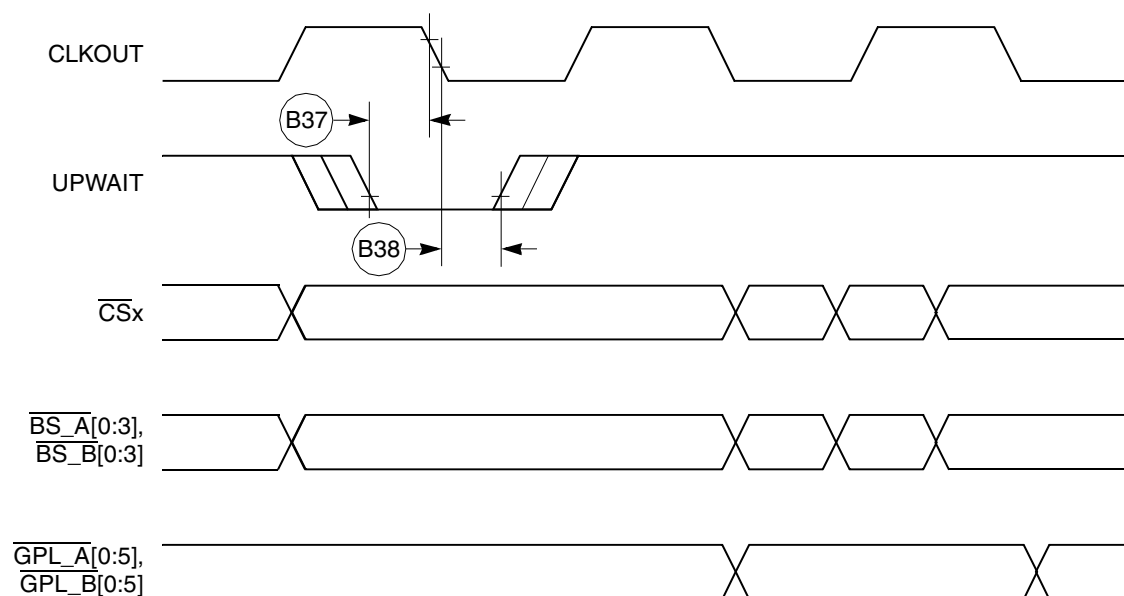


Figure 22. Asynchronous UPWAIT Negated Detection in UPM-Handled Cycles Timing

Figure 23 provides the timing for the synchronous external master access controlled by the GPCM.

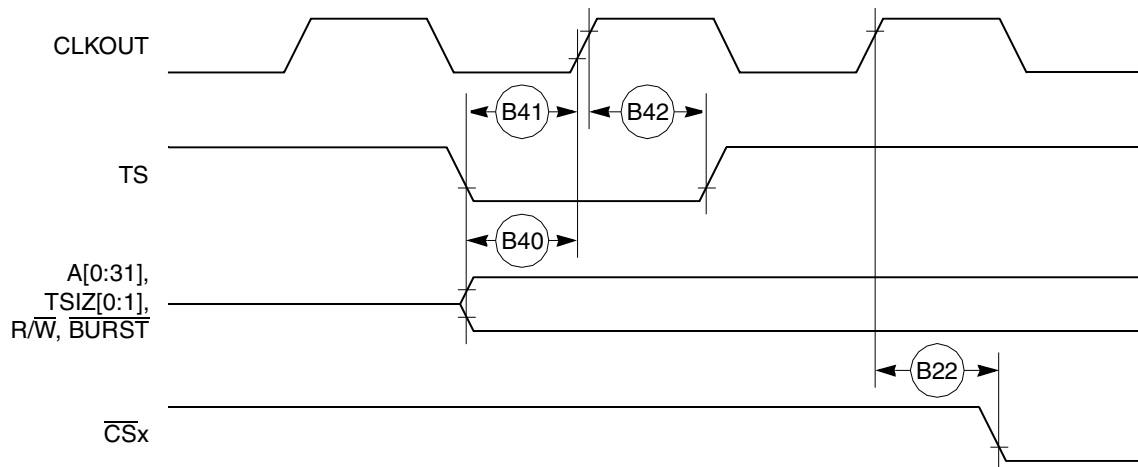


Figure 23. Synchronous External Master Access Timing (GPCM Handled—ACS = 00)

Figure 24 provides the timing for the asynchronous external master memory access controlled by the GPCM.

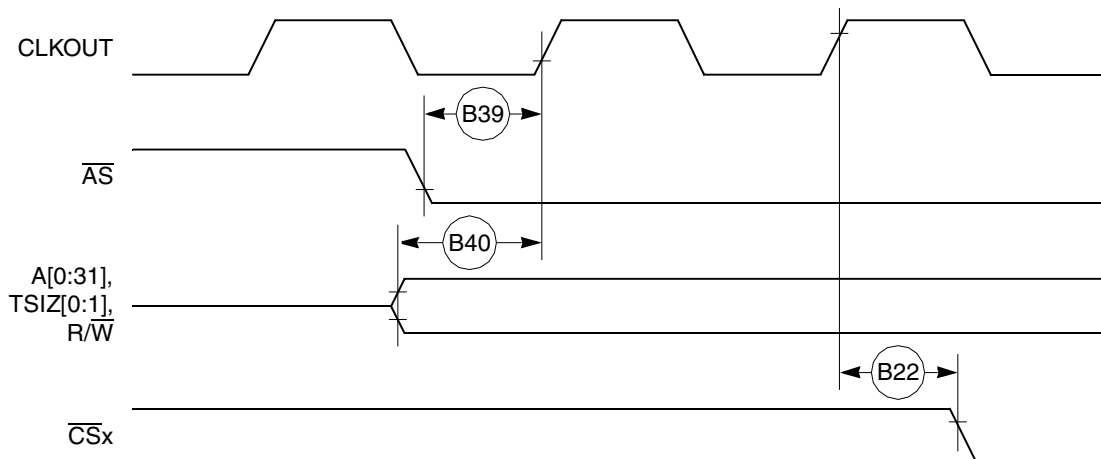


Figure 24. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)

Figure 25 provides the timing for the asynchronous external master control signals negation.

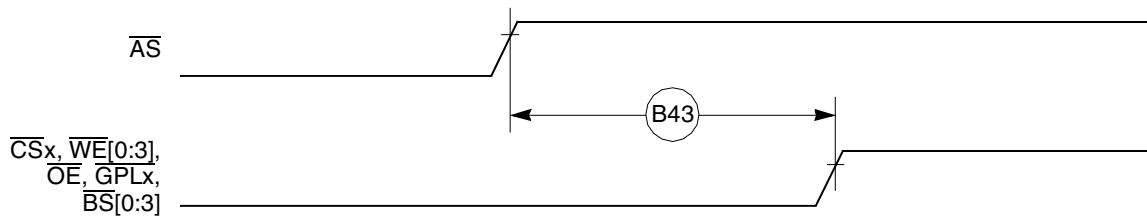


Figure 25. Asynchronous External Master—Control Signals Negation Timing

Table 10 provides the interrupt timing for the MPC885/MPC880.

Table 10. Interrupt Timing

| Num | Characteristic ¹ | All Frequencies | | Unit |
|-----|--|------------------------------|-----|------|
| | | Min | Max | |
| I39 | $\overline{\text{IRQ}}_x$ valid to CLKOUT rising edge (setup time) | 6.00 | | ns |
| I40 | $\overline{\text{IRQ}}_x$ hold time after CLKOUT | 2.00 | | ns |
| I41 | $\overline{\text{IRQ}}_x$ pulse width low | 3.00 | | ns |
| I42 | $\overline{\text{IRQ}}_x$ pulse width high | 3.00 | | ns |
| I43 | $\overline{\text{IRQ}}_x$ edge-to-edge time | $4 \times T_{\text{CLKOUT}}$ | | — |

¹ The I39 and I40 timings describe the testing conditions under which the $\overline{\text{IRQ}}$ lines are tested when being defined as level sensitive. The $\overline{\text{IRQ}}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT. The I41, I42, and I43 timings are specified to allow correct functioning of the $\overline{\text{IRQ}}$ lines detection circuitry and have no direct relation with the total system interrupt latency that the MPC885/MPC880 is able to support.

Figure 26 provides the interrupt detection timing for the external level-sensitive lines.

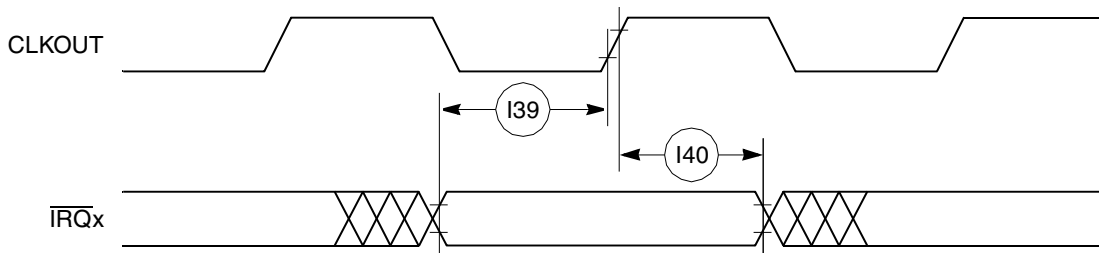


Figure 26. Interrupt Detection Timing for External Level Sensitive Lines

Figure 27 provides the interrupt detection timing for the external edge-sensitive lines.

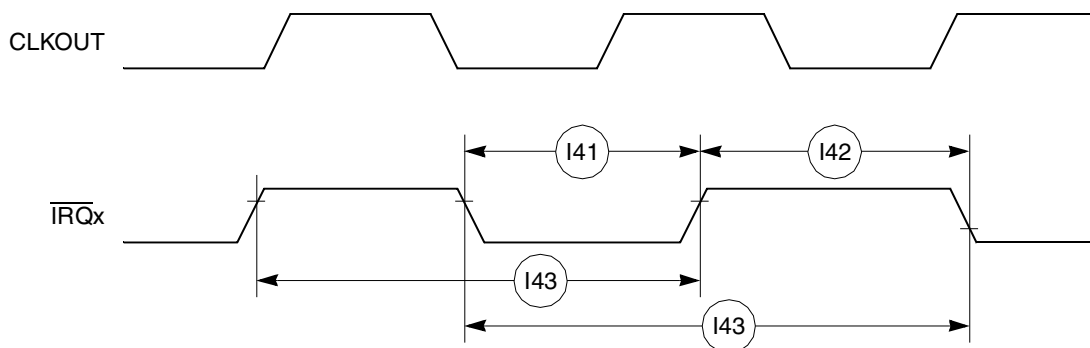


Figure 27. Interrupt Detection Timing for External Edge Sensitive Lines

Table 11 shows the PCMCIA timing for the MPC885/MPC880.

Table 11. PCMCIA Timing

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|-----|---|--------|-------|--------|-------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P44 | A(0:31), $\overline{\text{REG}}$ valid to PCMCIA strobe asserted ¹ (MIN = $0.75 \times B1 - 2.00$) | 20.70 | — | 16.70 | — | 9.40 | — | 7.40 | — | ns |
| P45 | A(0:31), $\overline{\text{REG}}$ valid to ALE negation ¹ (MIN = $1.00 \times B1 - 2.00$) | 28.30 | — | 23.00 | — | 13.20 | — | 10.50 | — | ns |
| P46 | CLKOUT to $\overline{\text{REG}}$ valid (MAX = $0.25 \times B1 + 8.00$) | 7.60 | 15.60 | 6.30 | 14.30 | 3.80 | 11.80 | 3.13 | 11.13 | ns |
| P47 | CLKOUT to $\overline{\text{REG}}$ invalid (MIN = $0.25 - B1 + 1.00$) | 8.60 | — | 7.30 | — | 4.80 | — | 4.13 | — | ns |
| P48 | CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ asserted (MAX = $0.25 \times B1 + 8.00$) | 7.60 | 15.60 | 6.30 | 14.30 | 3.80 | 11.80 | 3.13 | 11.13 | ns |
| P49 | CLKOUT to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ negated (MAX = $0.25 \times B1 + 8.00$) | 7.60 | 15.60 | 6.30 | 14.30 | 3.80 | 11.80 | 3.13 | 11.13 | ns |
| P50 | CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = $0.00 \times B1 + 11.00$) | — | 11.00 | — | 11.00 | — | 11.00 | — | 11.00 | ns |
| P51 | CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = $0.00 \times B1 + 11.00$) | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | ns |
| P52 | CLKOUT to ALE assert time (MAX = $0.25 \times B1 + 6.30$) | 7.60 | 13.80 | 6.30 | 12.50 | 3.80 | 10.00 | 3.13 | 9.40 | ns |
| P53 | CLKOUT to ALE negate time (MAX = $0.25 \times B1 + 8.00$) | — | 15.60 | — | 14.30 | — | 11.80 | — | 11.13 | ns |
| P54 | $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid ¹ (MIN = $0.25 \times B1 - 2.00$) | 5.60 | — | 4.30 | — | 1.80 | — | 1.13 | — | ns |
| P55 | $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge ¹ (MIN = $0.00 \times B1 + 8.00$) | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | — | ns |
| P56 | CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid ¹ (MIN = $0.00 \times B1 + 2.00$) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |

¹ PSST = 1. Otherwise add PSST times cycle time.
PSHT = 0. Otherwise add PSHT times cycle time.

These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See Chapter 16, "PCMCIA Interface," in the *MPC885 PowerQUICC™ Family Reference Manual*.

Figure 28 provides the PCMCIA access cycle timing for the external bus read.

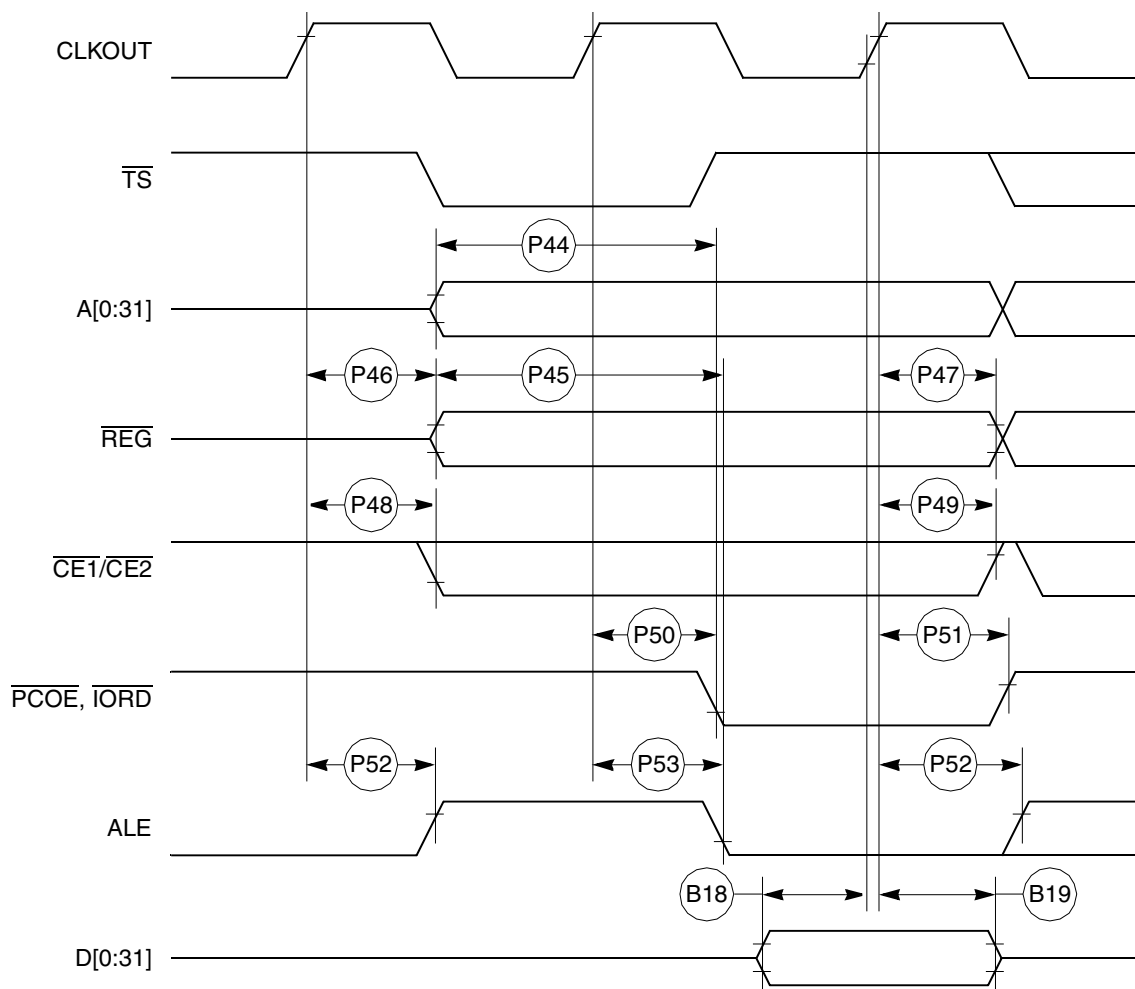


Figure 28. PCMCIA Access Cycles Timing External Bus Read

Figure 29 provides the PCMCIA access cycle timing for the external bus write.

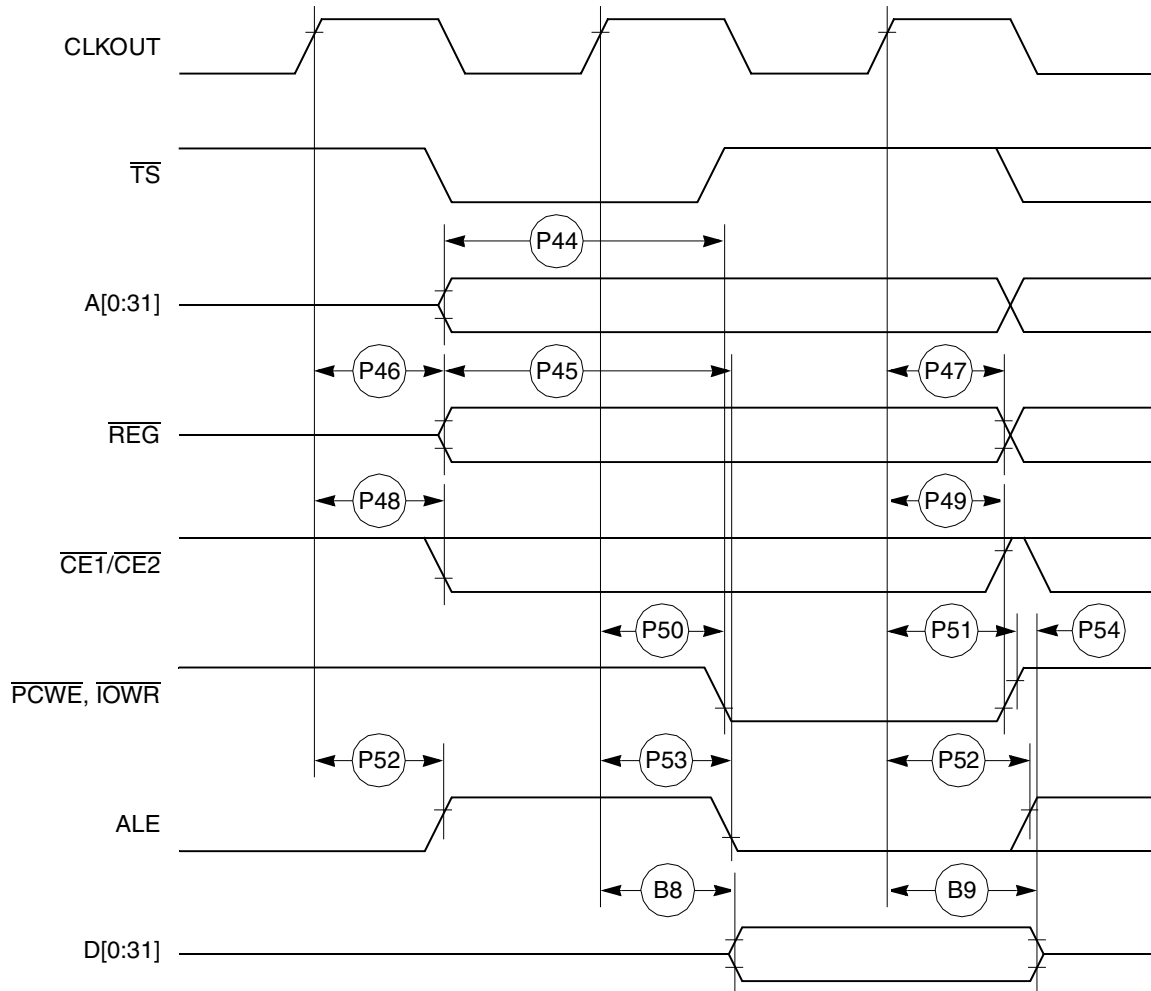


Figure 29. PCMCIA Access Cycles Timing External Bus Write

Figure 30 provides the PCMCIA $\overline{\text{WAIT}}$ signals detection timing.

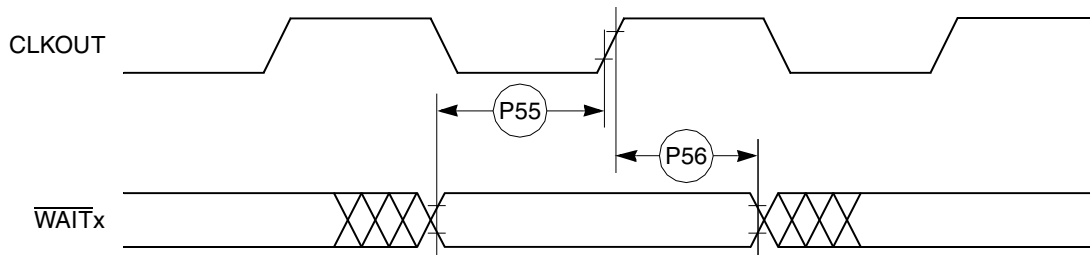


Figure 30. PCMCIA $\overline{\text{WAIT}}$ Signals Detection Timing

Table 12 shows the PCMCIA port timing for the MPC885/MPC880.

Table 12. PCMCIA Port Timing

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|-----|--|--------|-------|--------|-------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P57 | CLKOUT to OPx valid (MAX = $0.00 \times B1 + 19.00$) | — | 19.00 | — | 19.00 | — | 19.00 | — | 19.00 | ns |
| P58 | $\overline{\text{HRESET}}$ negated to OPx drive ¹ (MIN = $0.75 \times B1 + 3.00$) | 25.70 | — | 21.70 | — | 14.40 | — | 12.40 | — | ns |
| P59 | IP_Xx valid to CLKOUT rising edge (MIN = $0.00 \times B1 + 5.00$) | 5.00 | — | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| P60 | CLKOUT rising edge to IP_Xx invalid (MIN = $0.00 \times B1 + 1.00$) | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |

¹ OP2 and OP3 only.

Figure 31 provides the PCMCIA output port timing for the MPC885/MPC880.

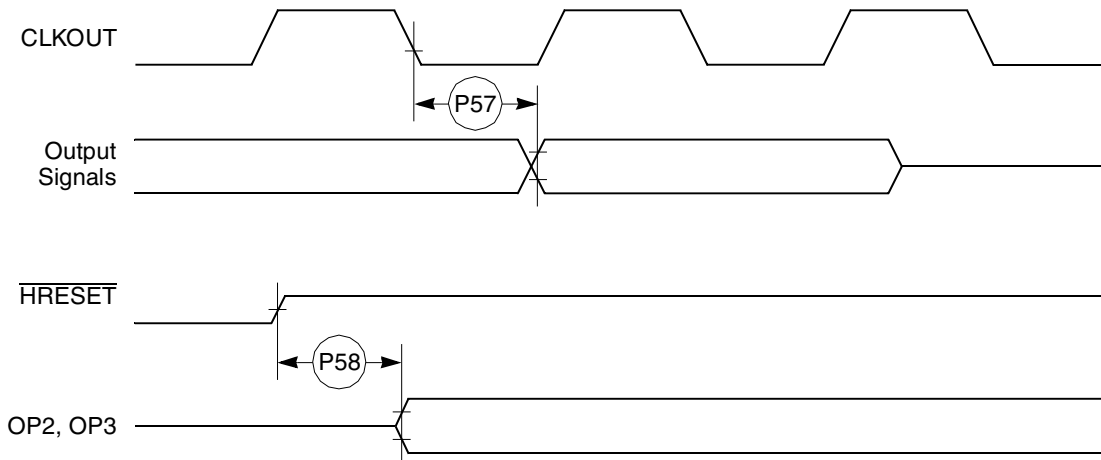


Figure 31. PCMCIA Output Port Timing

Figure 32 provides the PCMCIA input port timing for the MPC885/MPC880.

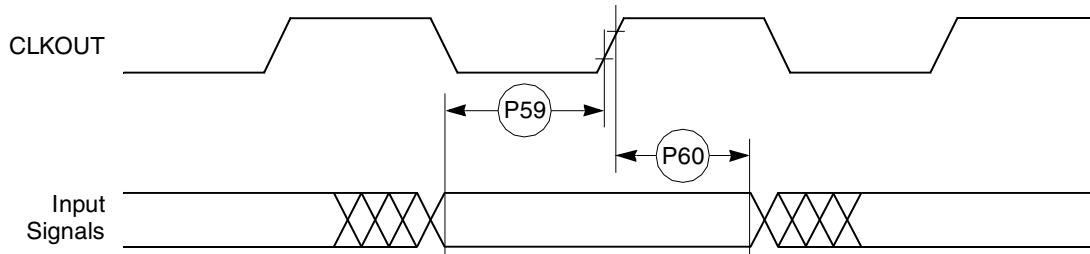


Figure 32. PCMCIA Input Port Timing

Table 13 shows the debug port timing for the MPC885/MPC880.

Table 13. Debug Port Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|-----------------------------|-----------------------------------|-------|------|
| | | Min | Max | |
| D61 | DSCK cycle time | $3 \times T_{\text{CLOCKOUT}}$ | — | — |
| D62 | DSCK clock pulse width | $1.25 \times T_{\text{CLOCKOUT}}$ | — | — |
| D63 | DSCK rise and fall times | 0.00 | 3.00 | ns |
| D64 | DSDI input data setup time | 8.00 | — | ns |
| D65 | DSDI data hold time | 5.00 | — | ns |
| D66 | DSCK low to DSDO data valid | 0.00 | 15.00 | ns |
| D67 | DSCK low to DSDO invalid | 0.00 | 2.00 | ns |

Figure 33 provides the input timing for the debug port clock.

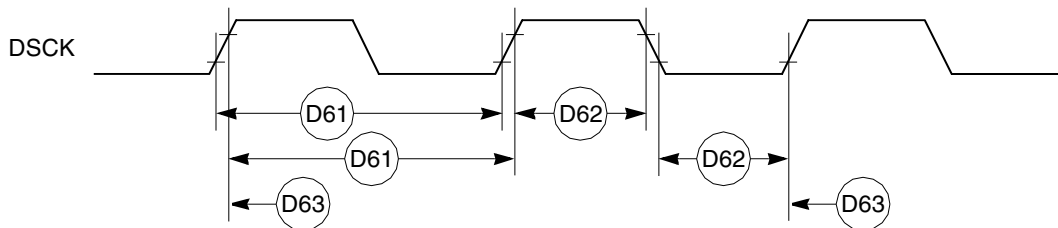


Figure 33. Debug Port Clock Input Timing

Figure 34 provides the timing for the debug port.

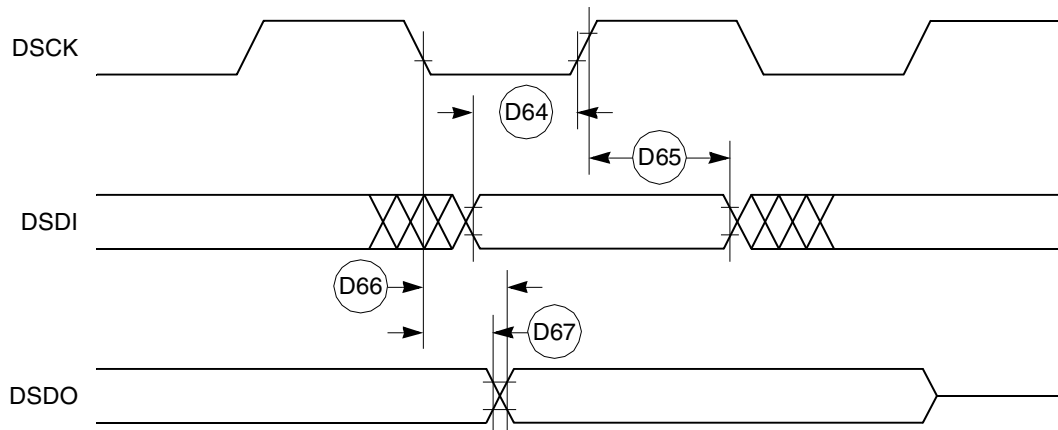


Figure 34. Debug Port Timings

Table 14 shows the reset timing for the MPC885/MPC880.

Table 14. Reset Timing

| Num | Characteristic | 33 MHz | | 40 MHz | | 66 MHz | | 80 MHz | | Unit |
|-----|--|--------|-------|--------|-------|--------|-------|--------|-------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| R69 | CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$) | — | 20.00 | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| R70 | CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = $0.00 \times B1 + 20.00$) | — | 20.00 | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| R71 | $\overline{\text{RSTCONF}}$ pulse width (MIN = $17.00 \times B1$) | 515.20 | — | 425.00 | — | 257.60 | — | 212.50 | — | ns |
| R72 | — | — | — | — | — | — | — | — | — | — |
| R73 | Configuration data to HRESET rising edge setup time (MIN = $15.00 \times B1 + 50.00$) | 504.50 | — | 425.00 | — | 277.30 | — | 237.50 | — | ns |
| R74 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = $0.00 \times B1 + 350.00$) | 350.00 | — | 350.00 | — | 350.00 | — | 350.00 | — | ns |
| R75 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = $0.00 \times B1 + 0.00$) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R76 | Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = $0.00 \times B1 + 0.00$) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R77 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = $0.00 \times B1 + 25.00$) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R78 | $\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = $0.00 \times B1 + 25.00$) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R79 | CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = $0.00 \times B1 + 25.00$) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R80 | DSDI, DSCK setup (MIN = $3.00 \times B1$) | 90.90 | — | 75.00 | — | 45.50 | — | 37.50 | — | ns |
| R81 | DSDI, DSCK hold time (MIN = $0.00 \times B1 + 0.00$) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R82 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = $8.00 \times B1$) | 242.40 | — | 200.00 | — | 121.20 | — | 100.00 | — | ns |

Figure 35 shows the reset timing for the data bus configuration.

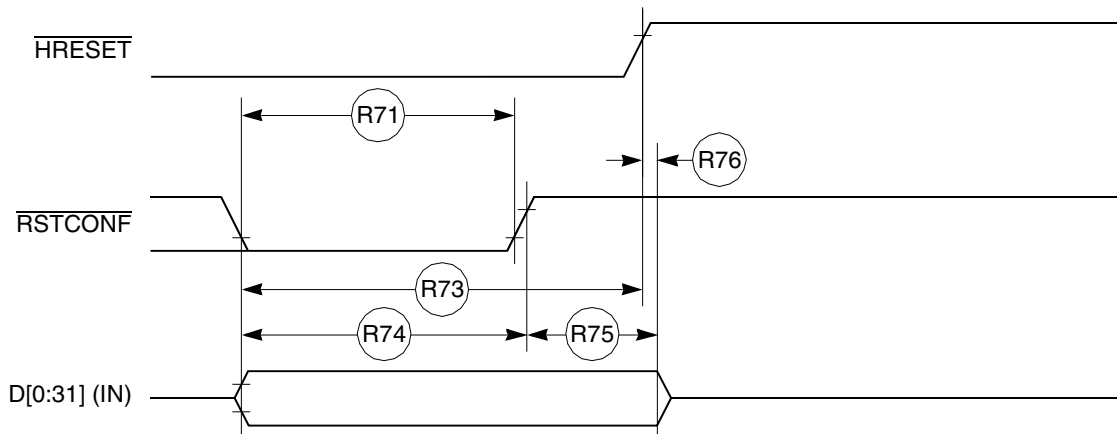


Figure 35. Reset Timing—Configuration from Data Bus

Figure 36 provides the reset timing for the data bus weak drive during configuration.

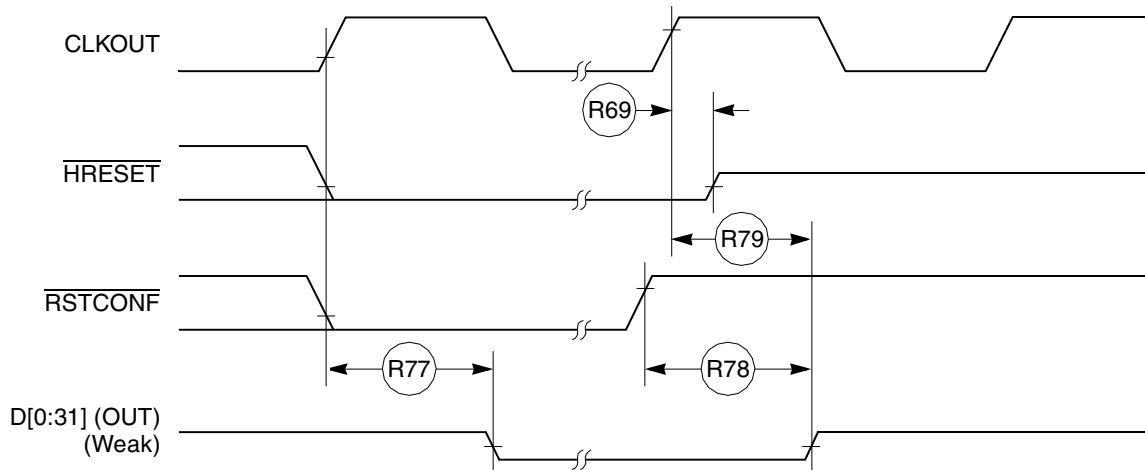


Figure 36. Reset Timing—Data Bus Weak Drive During Configuration

Figure 37 provides the reset timing for the debug port configuration.

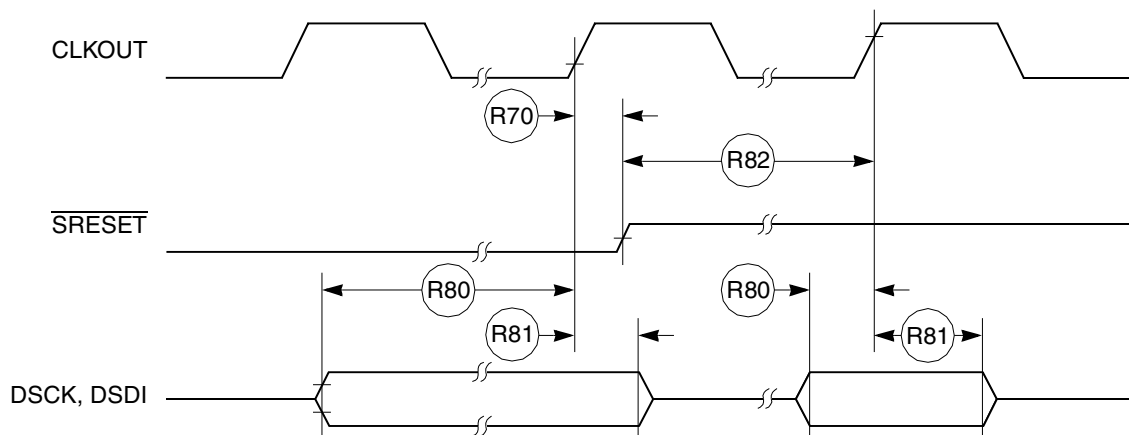


Figure 37. Reset Timing—Debug Port Configuration

11 IEEE 1149.1 Electrical Specifications

Table 15 provides the JTAG timings for the MPC885/MPC880 shown in Figure 38 through Figure 41.

Table 15. JTAG Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|--|-----------------|-------|------|
| | | Min | Max | |
| J82 | TCK cycle time | 100.00 | — | ns |
| J83 | TCK clock pulse width measured at 1.5 V | 40.00 | — | ns |
| J84 | TCK rise and fall times | 0.00 | 10.00 | ns |
| J85 | TMS, TDI data setup time | 5.00 | — | ns |
| J86 | TMS, TDI data hold time | 25.00 | — | ns |
| J87 | TCK low to TDO data valid | — | 27.00 | ns |
| J88 | TCK low to TDO data invalid | 0.00 | — | ns |
| J89 | TCK low to TDO high impedance | — | 20.00 | ns |
| J90 | $\overline{\text{TRST}}$ assert time | 100.00 | — | ns |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low | 40.00 | — | ns |
| J92 | TCK falling edge to output valid | — | 50.00 | ns |
| J93 | TCK falling edge to output valid out of high impedance | — | 50.00 | ns |
| J94 | TCK falling edge to output high impedance | — | 50.00 | ns |
| J95 | Boundary scan input valid to TCK rising edge | 50.00 | — | ns |
| J96 | TCK rising edge to boundary scan input invalid | 50.00 | — | ns |

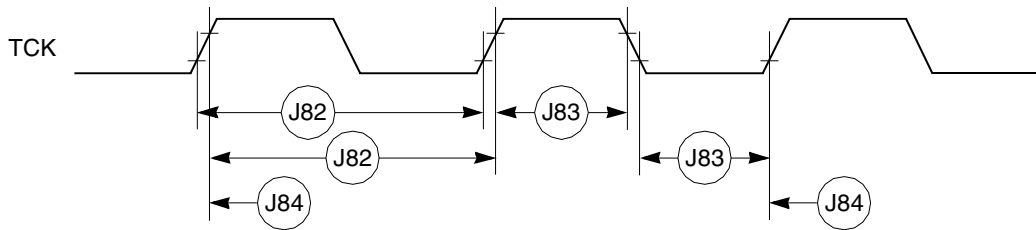


Figure 38. JTAG Test Clock Input Timing

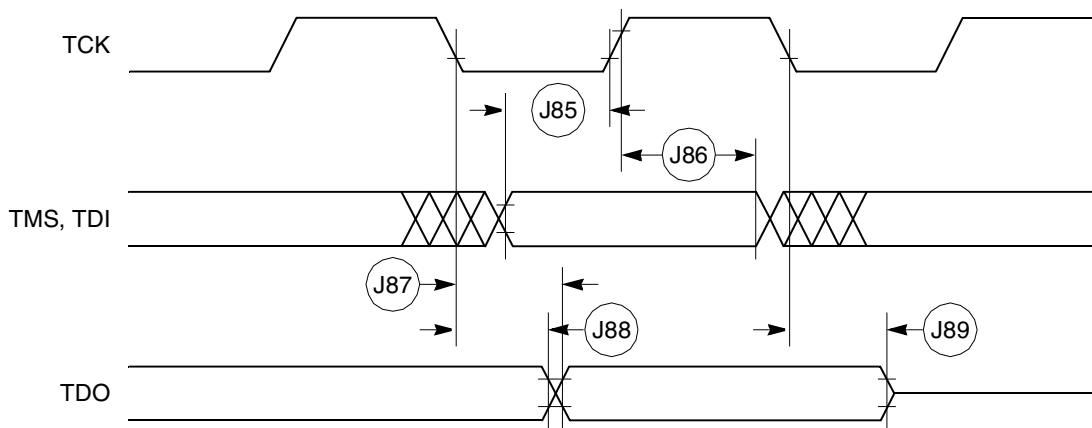


Figure 39. JTAG Test Access Port Timing Diagram

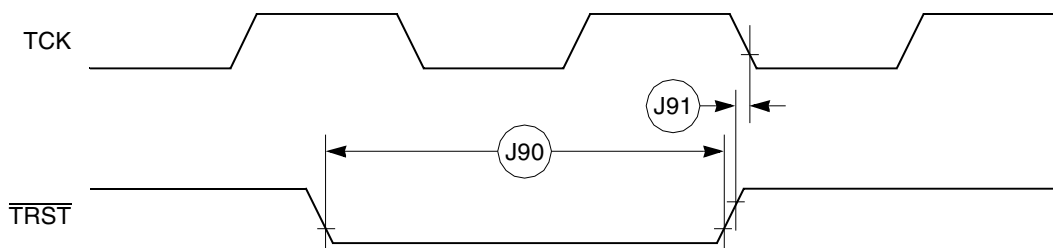


Figure 40. JTAG TRST Timing Diagram

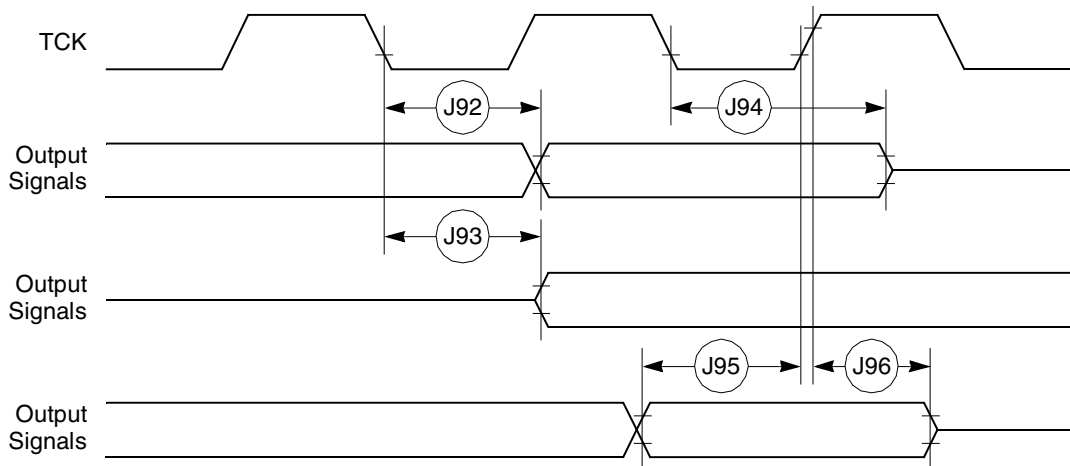


Figure 41. Boundary Scan (JTAG) Timing Diagram

12 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC885/MPC880.

12.1 PIP/PIO AC Electrical Specifications

Table 16 provides the PIP/PIO AC timings as shown in Figure 42 through Figure 46.

Table 16. PIP/PIO Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|--|-----------------|-----|------|
| | | Min | Max | |
| 21 | Data-in setup time to STBI low | 0 | — | ns |
| 22 | Data-In hold time to STBI high | 0 | — | clk |
| 23 | STBI pulse width | 1.5 | — | clk |
| 24 | STBO pulse width | 1 clk – 5 ns | — | ns |
| 25 | Data-out setup time to STBO low | 2 | — | clk |
| 26 | Data-out hold time from STBO high | 5 | — | clk |
| 27 | STBI low to STBO low (Rx interlock) | — | 4.5 | clk |
| 28 | STBI low to STBO high (Tx interlock) | 2 | — | clk |
| 29 | Data-in setup time to clock high | 15 | — | ns |
| 30 | Data-in hold time from clock high | 7.5 | — | ns |
| 31 | Clock low to data-out valid (CPU writes data, control, or direction) | — | 25 | ns |

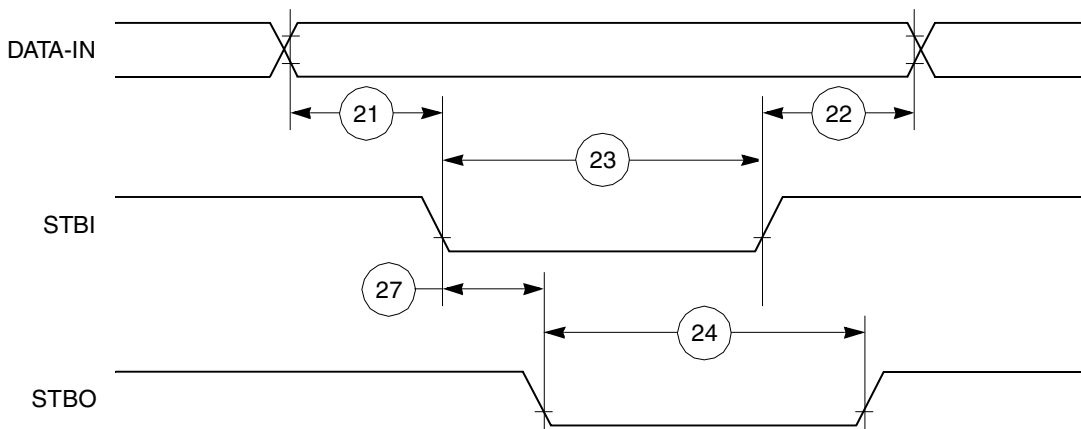


Figure 42. PIP Rx (Interlock Mode) Timing Diagram

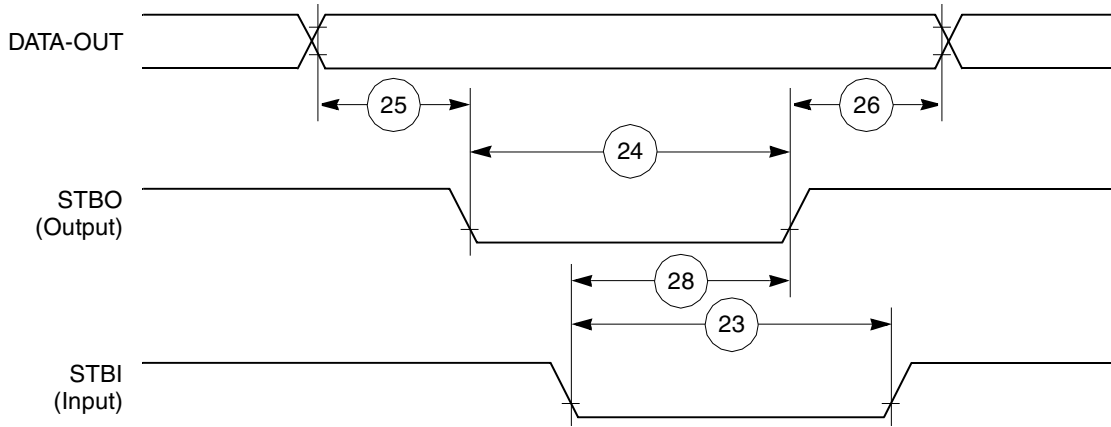


Figure 43. PIP Tx (Interlock Mode) Timing Diagram

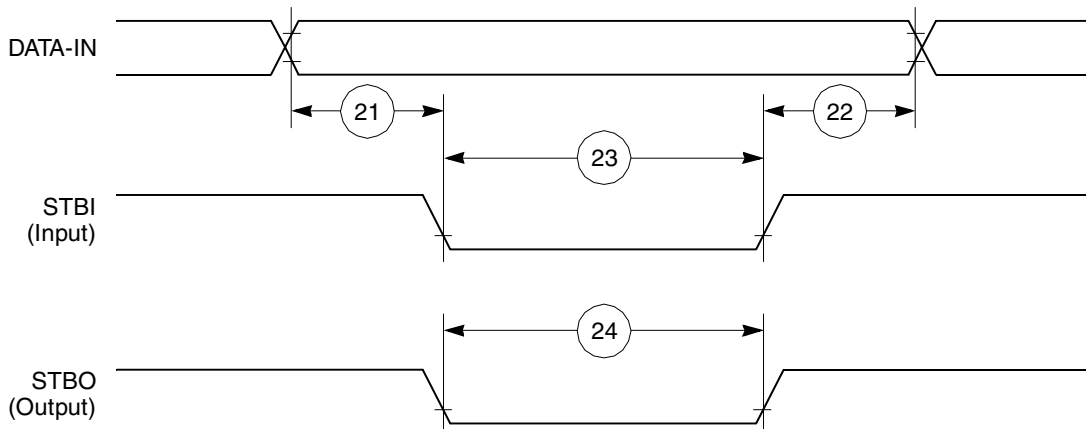


Figure 44. PIP Rx (Pulse Mode) Timing Diagram

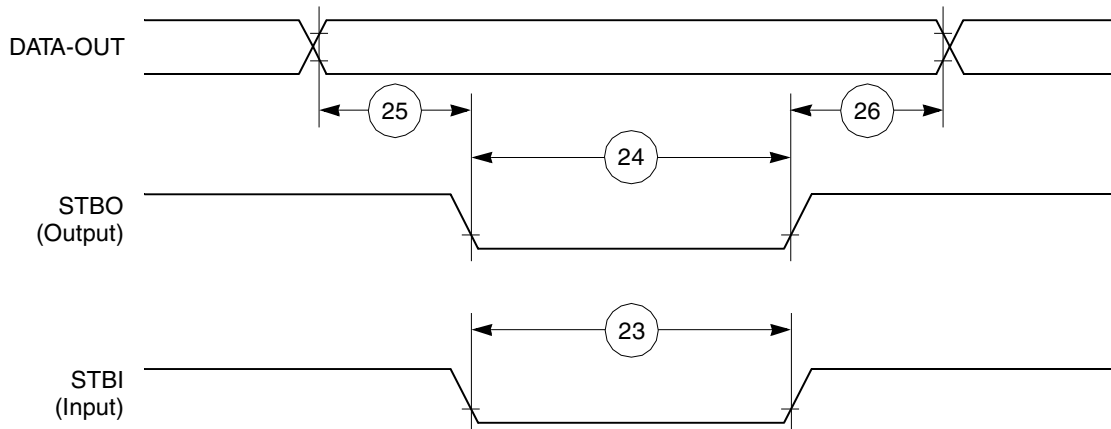


Figure 45. PIP TX (Pulse Mode) Timing Diagram

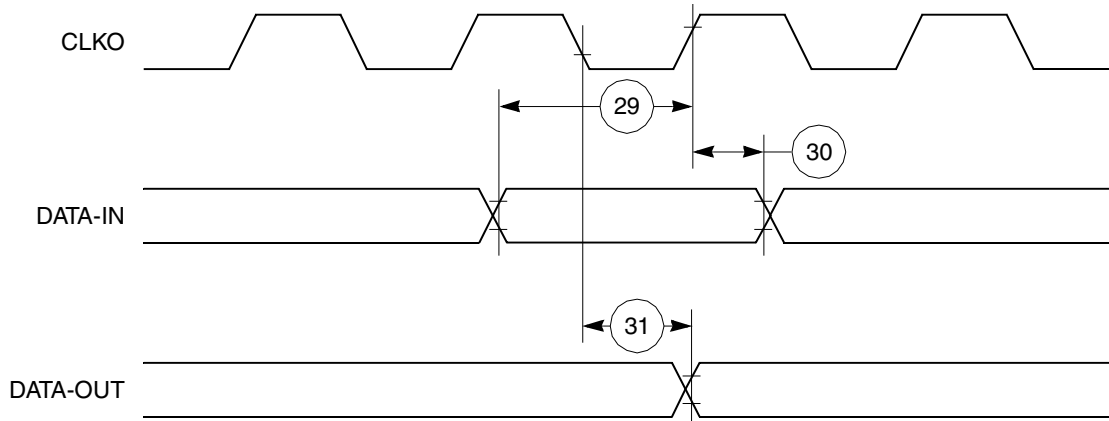


Figure 46. Parallel I/O Data-In/Data-Out Timing Diagram

12.2 Port C Interrupt AC Electrical Specifications

Table 17 provides the timings for port C interrupts.

Table 17. Port C Interrupt Timing

| Num | Characteristic | 33.34 MHz | | Unit |
|-----|--|-----------|-----|------|
| | | Min | Max | |
| 35 | Port C interrupt pulse width low (edge-triggered mode) | 55 | — | ns |
| 36 | Port C interrupt minimum time between active edges | 55 | — | ns |

Figure 47 shows the port C interrupt detection timing.

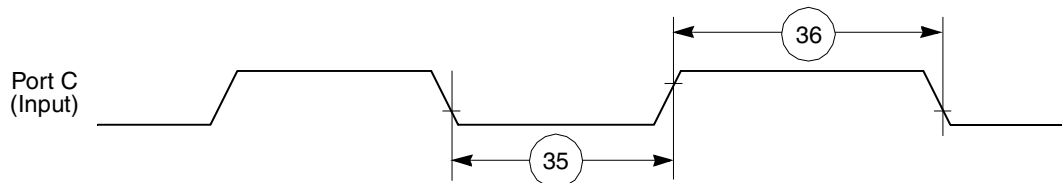


Figure 47. Port C Interrupt Detection Timing

12.3 IDMA Controller AC Electrical Specifications

Table 18 provides the IDMA controller timings as shown in Figure 48 through Figure 51.

Table 18. IDMA Controller Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|---|-----------------|-----|------|
| | | Min | Max | |
| 40 | $\overline{\text{DREQ}}$ setup time to clock high | 7 | — | ns |
| 41 | $\overline{\text{DREQ}}$ hold time from clock high ¹ | TBD | — | ns |
| 42 | $\overline{\text{SDACK}}$ assertion delay from clock high | — | 12 | ns |
| 43 | $\overline{\text{SDACK}}$ negation delay from clock low | — | 12 | ns |
| 44 | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low | — | 20 | ns |
| 45 | $\overline{\text{SDACK}}$ negation delay from clock high | — | 15 | ns |
| 46 | $\overline{\text{TA}}$ assertion to rising edge of the clock setup time (applies to external $\overline{\text{TA}}$) | 7 | — | ns |

¹ Applies to high-to-low mode (EDM = 1).

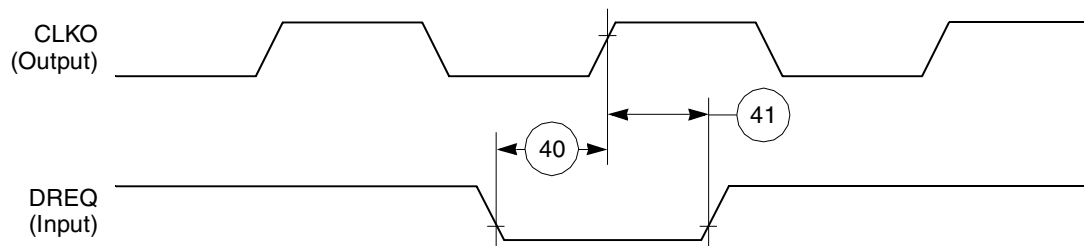


Figure 48. IDMA External Requests Timing Diagram

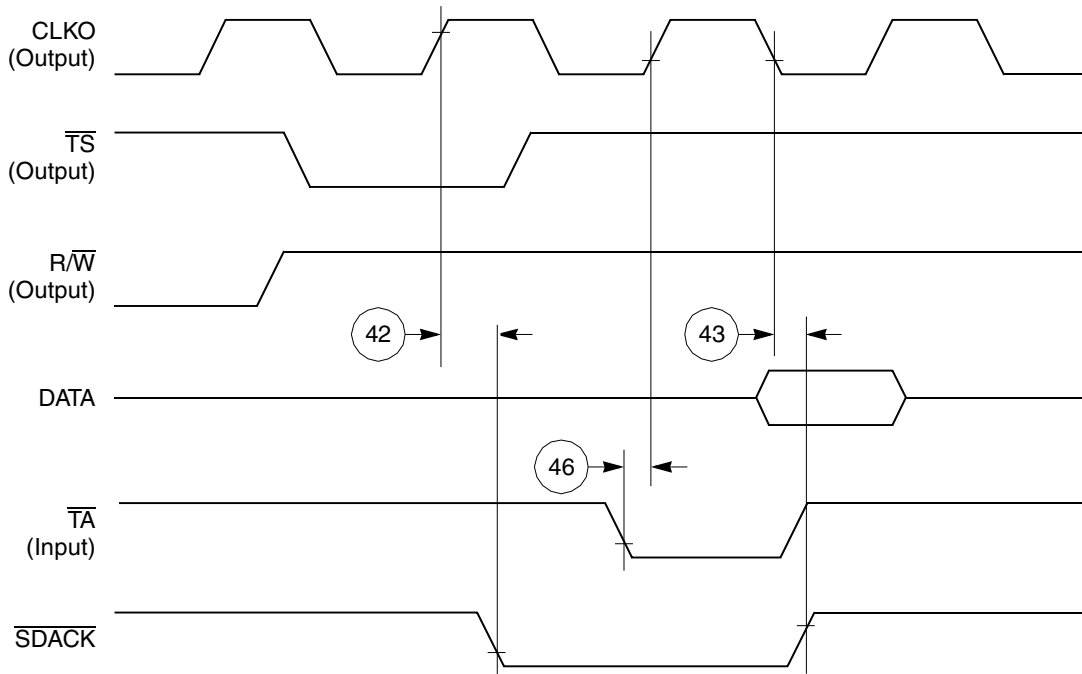


Figure 49. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Externally-Generated $\overline{\text{TA}}$

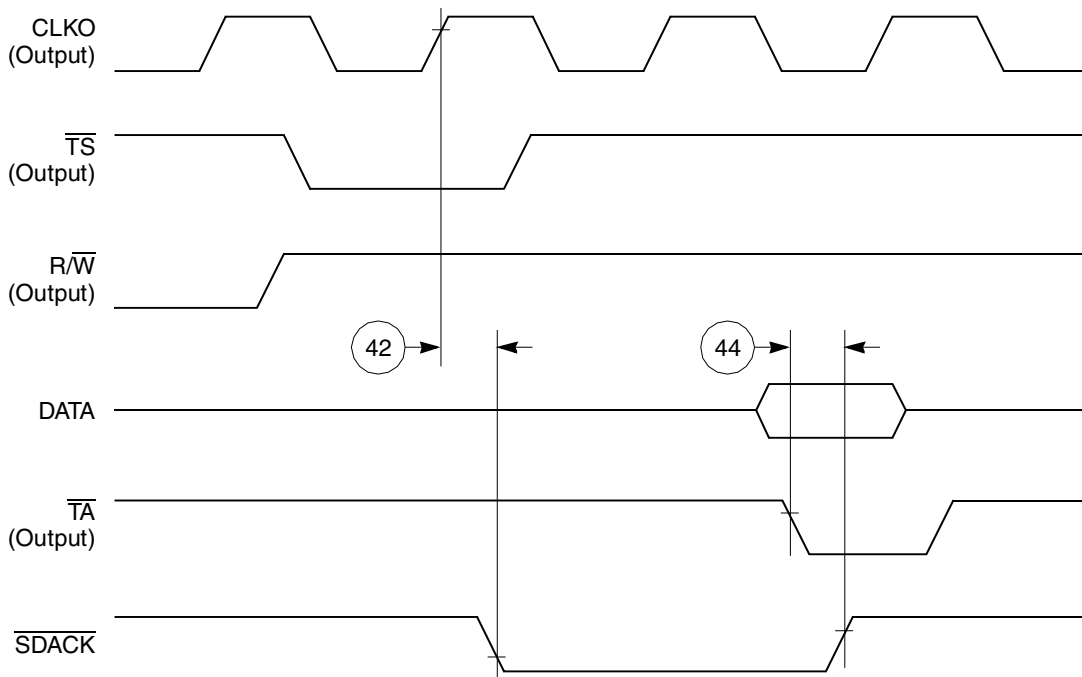


Figure 50. $\overline{\text{SDACK}}$ Timing Diagram—Peripheral Write, Internally-Generated $\overline{\text{TA}}$

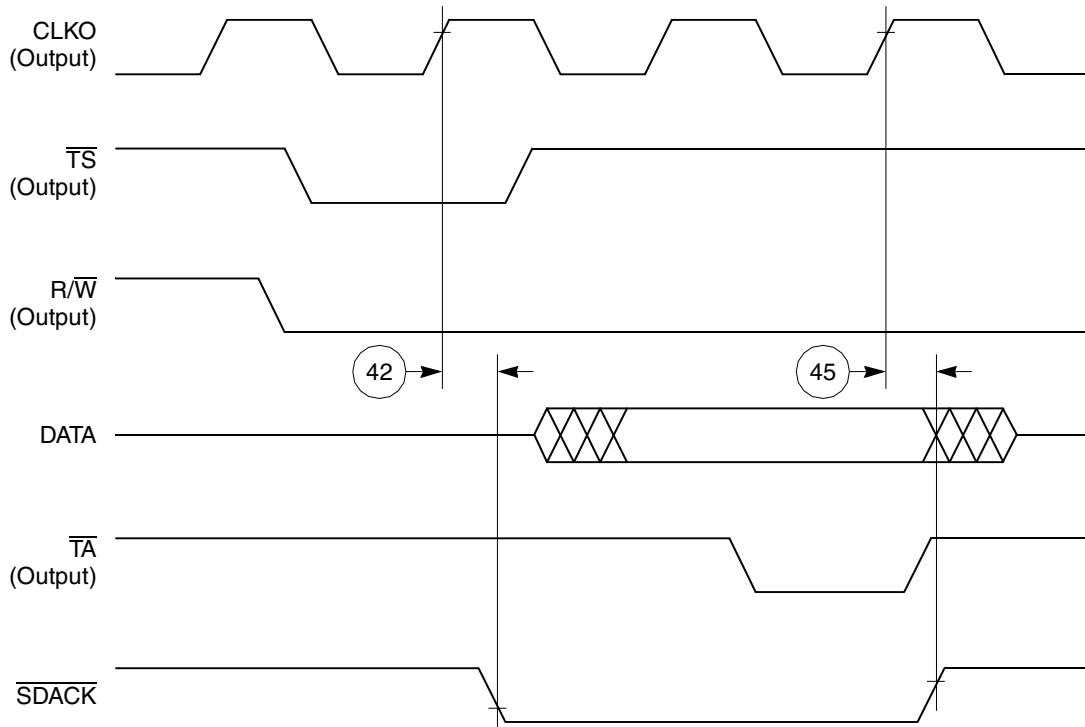


Figure 51. \overline{SDACK} Timing Diagram—Peripheral Read, Internally-Generated \overline{TA}

12.4 Baud Rate Generator AC Electrical Specifications

Table 19 provides the baud rate generator timings as shown in Figure 52.

Table 19. Baud Rate Generator Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|-------------------------|-----------------|-----|------|
| | | Min | Max | |
| 50 | BRGO rise and fall time | — | 10 | ns |
| 51 | BRGO duty cycle | 40 | 60 | % |
| 52 | BRGO cycle | 40 | — | ns |

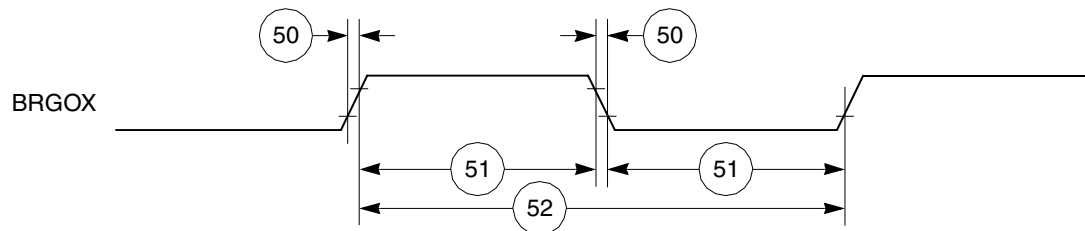


Figure 52. Baud Rate Generator Timing Diagram

12.5 Timer AC Electrical Specifications

Table 20 provides the general-purpose timer timings as shown in Figure 53.

Table 20. Timer Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|------------------------------|-----------------|-----|------|
| | | Min | Max | |
| 61 | TIN/TGATE rise and fall time | 10 | — | ns |
| 62 | TIN/TGATE low time | 1 | — | clk |
| 63 | TIN/TGATE high time | 2 | — | clk |
| 64 | TIN/TGATE cycle time | 3 | — | clk |
| 65 | CLKO low to TOUT valid | 3 | 25 | ns |

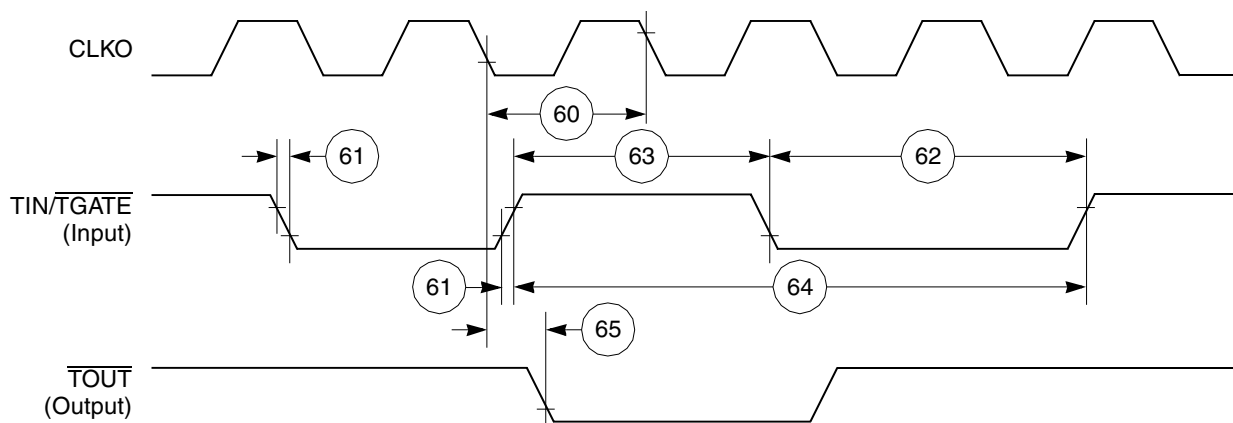


Figure 53. CPM General-Purpose Timers Timing Diagram

12.6 Serial Interface AC Electrical Specifications

Table 21 provides the serial interface timings as shown in Figure 54 through Figure 58.

Table 21. SI Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|--|-----------------|-------------|------|
| | | Min | Max | |
| 70 | L1RCLK, L1TCLK frequency (DSC = 0) ^{1, 2} | — | SYNCCLK/2.5 | MHz |
| 71 | L1RCLK, L1TCLK width low (DSC = 0) ² | P + 10 | — | ns |
| 71a | L1RCLK, L1TCLK width high (DSC = 0) ³ | P + 10 | — | ns |
| 72 | L1TXD, L1ST(1-4), L1RQ, L1CLKO rise/fall time | — | 15.00 | ns |
| 73 | L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time) | 20.00 | — | ns |
| 74 | L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time) | 35.00 | — | ns |
| 75 | L1RSYNC, L1TSYNC rise/fall time | — | 15.00 | ns |

Table 21. SI Timing (continued)

| Num | Characteristic | All Frequencies | | Unit |
|-----|---|-----------------|--------------------|--------|
| | | Min | Max | |
| 76 | L1RXD valid to L1CLK edge (L1RXD setup time) | 17.00 | — | ns |
| 77 | L1CLK edge to L1RXD invalid (L1RXD hold time) | 13.00 | — | ns |
| 78 | L1CLK edge to L1ST(1–4) valid ⁴ | 10.00 | 45.00 | ns |
| 78A | L1SYNC valid to L1ST(1–4) valid | 10.00 | 45.00 | ns |
| 79 | L1CLK edge to L1ST(1–4) invalid | 10.00 | 45.00 | ns |
| 80 | L1CLK edge to L1TXD valid | 10.00 | 55.00 | ns |
| 80A | L1TSYNC valid to L1TXD valid ⁴ | 10.00 | 55.00 | ns |
| 81 | L1CLK edge to L1TXD high impedance | 0.00 | 42.00 | ns |
| 82 | L1RCLK, L1TCLK frequency (DSC = 1) | — | 16.00 or SYNCCLK/2 | MHz |
| 83 | L1RCLK, L1TCLK width low (DSC = 1) | P + 10 | — | ns |
| 83a | L1RCLK, L1TCLK width high (DSC = 1) ³ | P + 10 | — | ns |
| 84 | L1CLK edge to L1CLKO valid (DSC = 1) | — | 30.00 | ns |
| 85 | $\overline{L1RQ}$ valid before falling edge of L1TSYNC ⁴ | 1.00 | — | L1TCLK |
| 86 | L1GR setup time ² | 42.00 | — | ns |
| 87 | L1GR hold time | 42.00 | — | ns |
| 88 | L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0) | — | 0.00 | ns |

¹ The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

² These specs are valid for IDL mode only.

³ Where P = 1/CLKOUT. Thus for a 25-MHz CLKO1 rate, P = 40 ns.

⁴ These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever comes later.

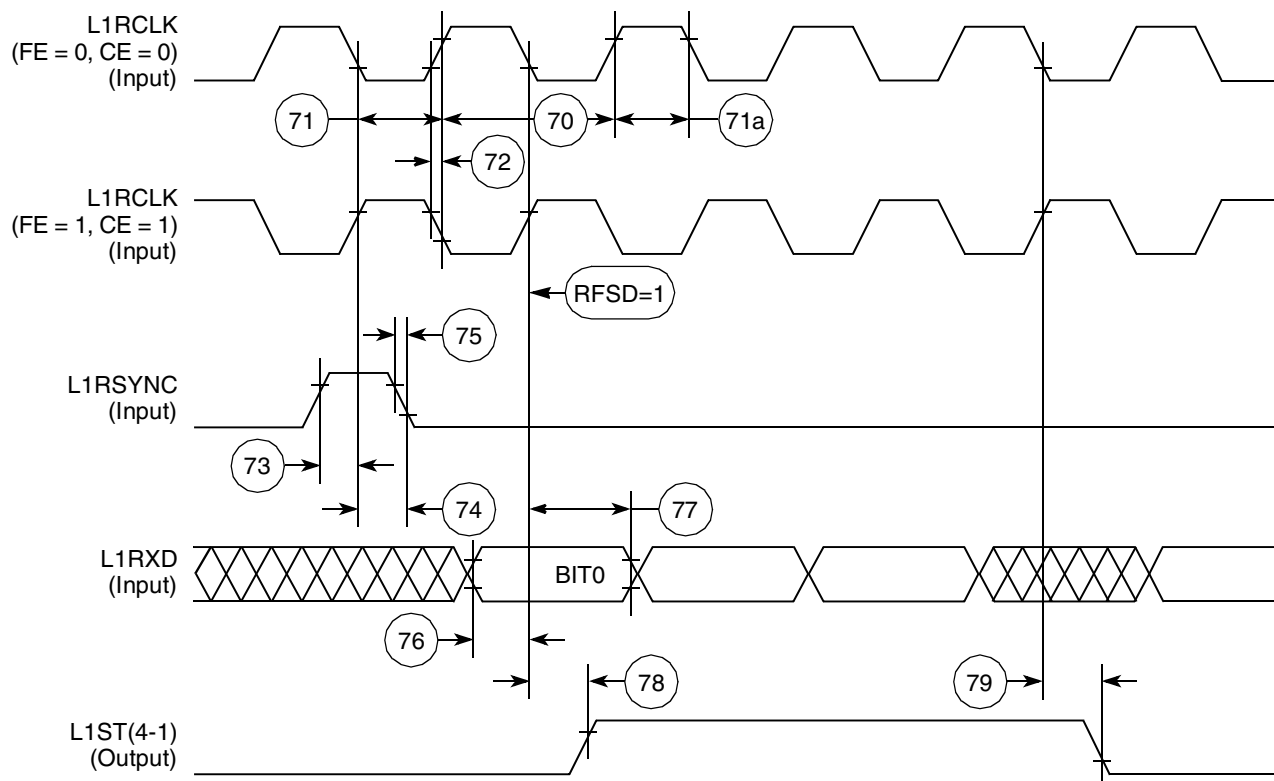


Figure 54. SI Receive Timing Diagram with Normal Clocking (DSC = 0)

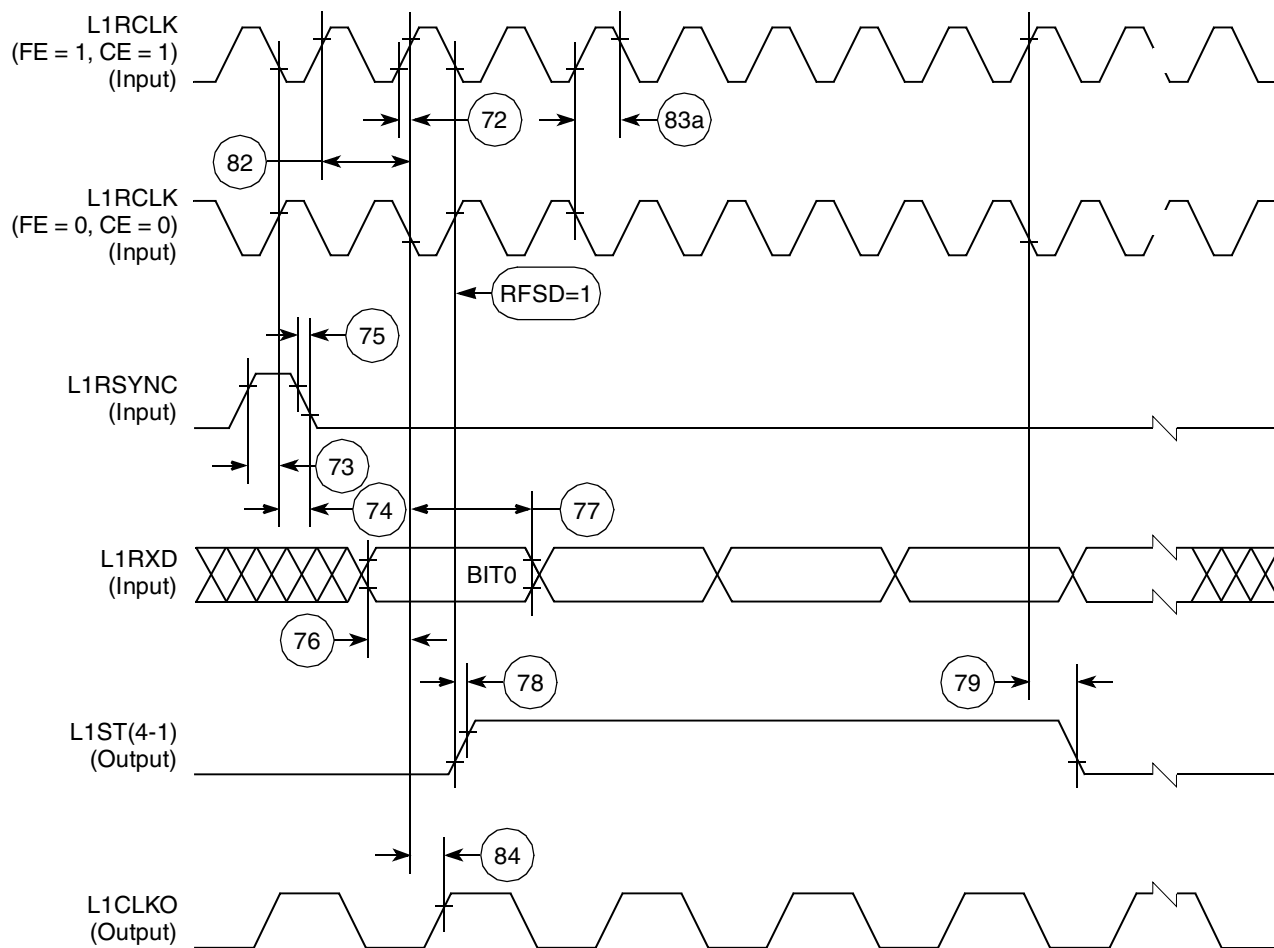


Figure 55. SI Receive Timing with Double-Speed Clocking (DSC = 1)

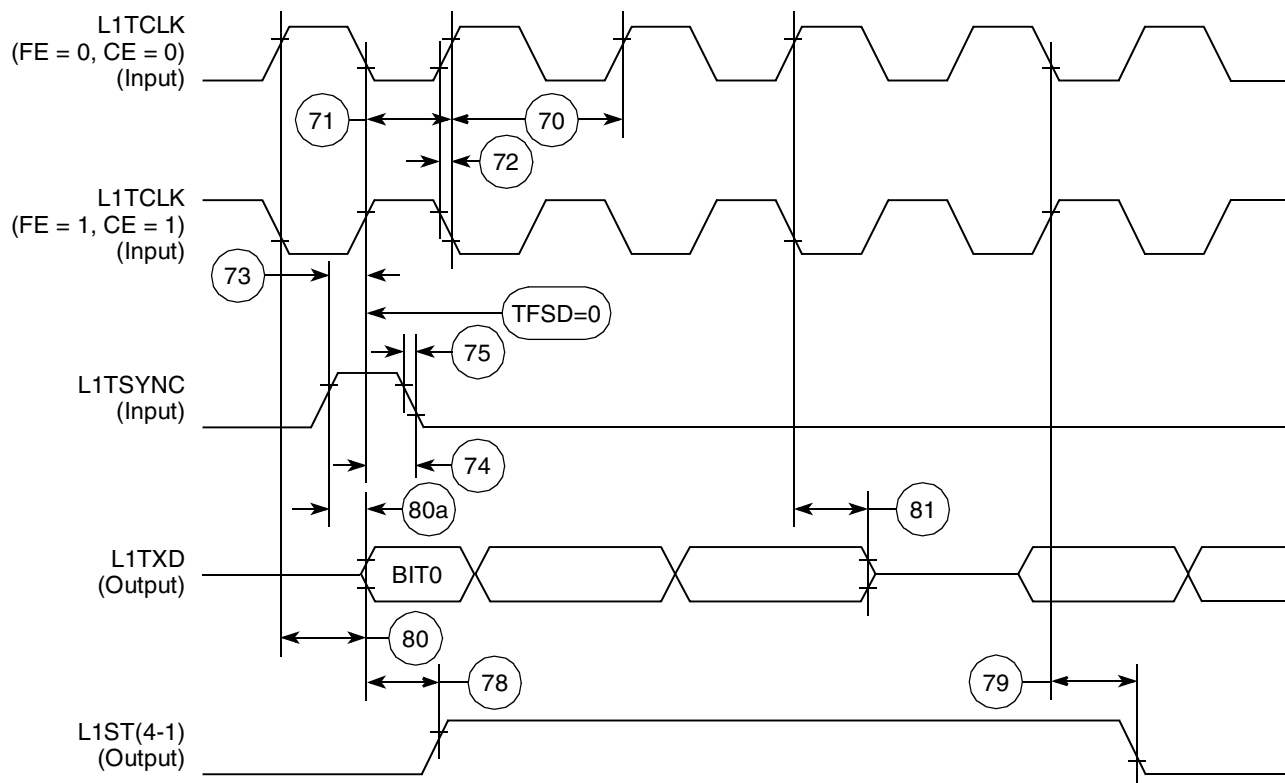


Figure 56. SI Transmit Timing Diagram (DSC = 0)

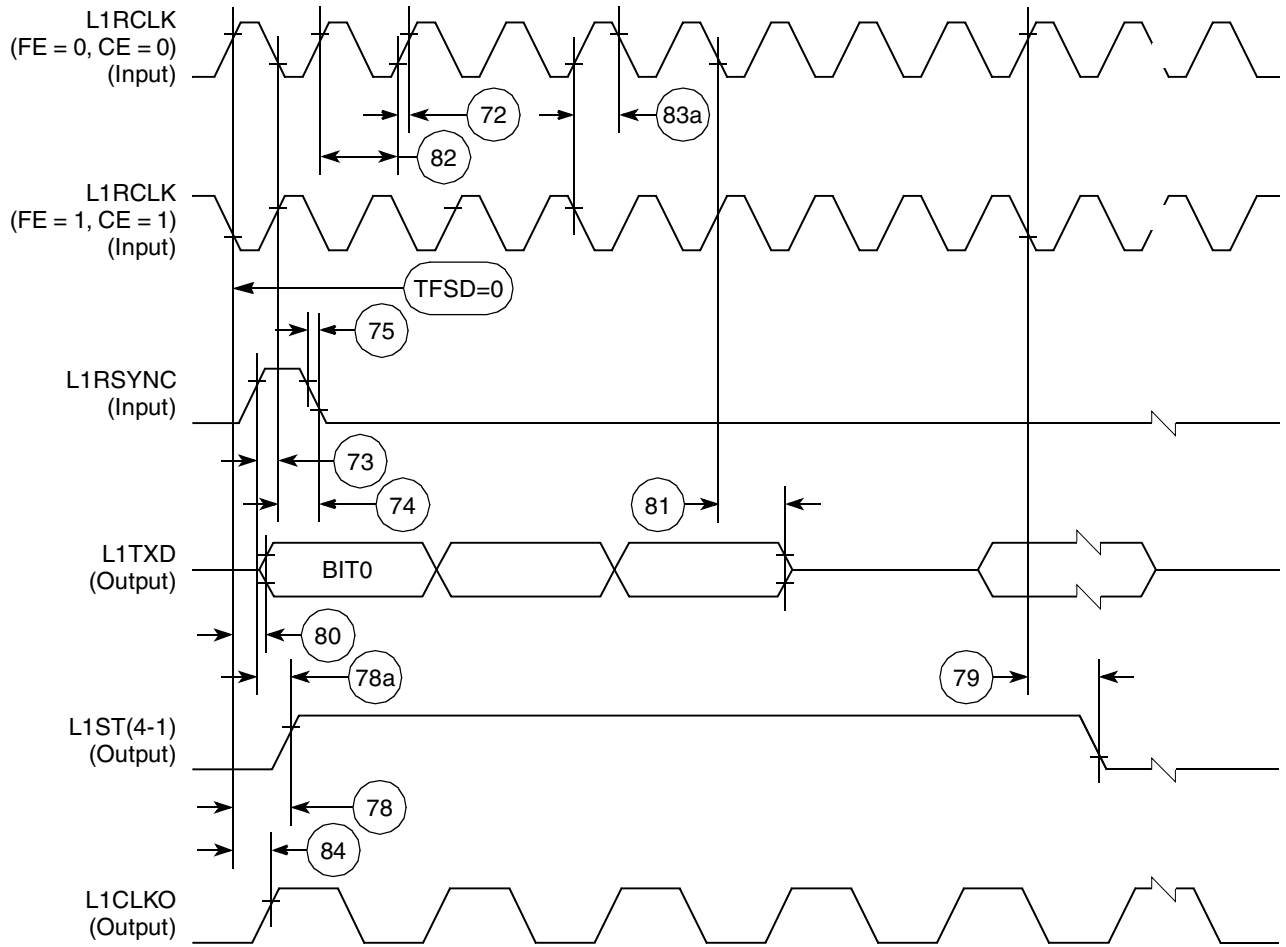


Figure 57. SI Transmit Timing with Double Speed Clocking (DSC = 1)

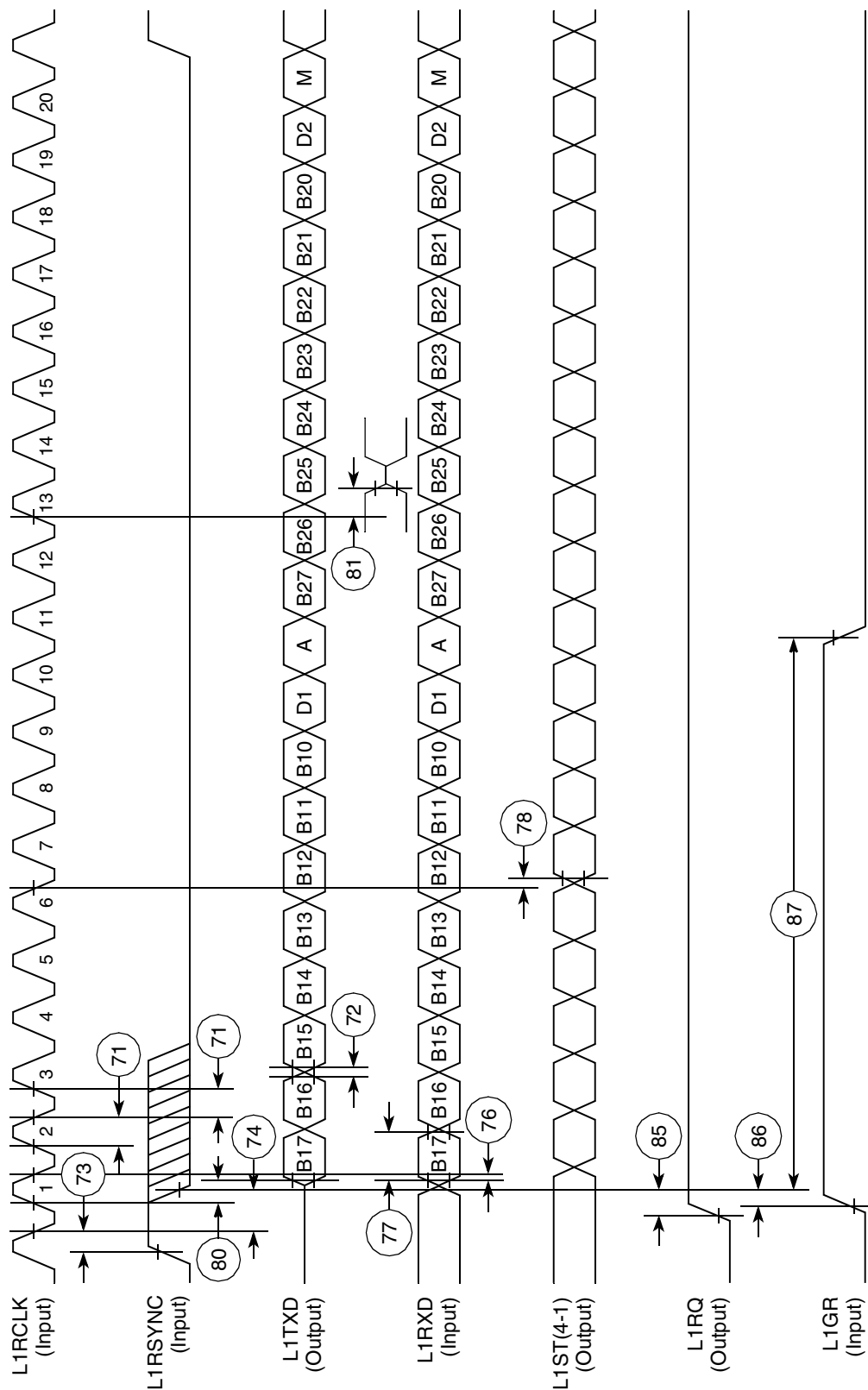


Figure 58. IDL Timing

12.7 SCC in NMSI Mode Electrical Specifications

Table 22 provides the NMSI external clock timing.

Table 22. NMSI External Clock Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|---|-----------------|-------|------|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 width high ¹ | 1/SYNCCLK | — | ns |
| 101 | RCLK1 and TCLK1 width low | 1/SYNCCLK + 5 | — | ns |
| 102 | RCLK1 and TCLK1 rise/fall time | — | 15.00 | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{RTS1}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{CTS1}$ setup time to TCLK1 rising edge | 5.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 5.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge ² | 5.00 | — | ns |
| 108 | $\overline{CD1}$ setup time to RCLK1 rising edge | 5.00 | — | ns |

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

² Also applies to \overline{CD} and \overline{CTS} hold time when they are used as external sync signals.

Table 23 provides the NMSI internal clock timing.

Table 23. NMSI Internal Clock Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|---|-----------------|-----------|------|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 frequency ¹ | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLK1 and TCLK1 rise/fall time | — | — | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{RTS1}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{CTS1}$ setup time to TCLK1 rising edge | 40.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 40.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge ² | 0.00 | — | ns |
| 108 | $\overline{CD1}$ setup time to RCLK1 rising edge | 40.00 | — | ns |

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 3/1.

² Also applies to \overline{CD} and \overline{CTS} hold time when they are used as external sync signals

Figure 59 through Figure 61 show the NMSI timings.

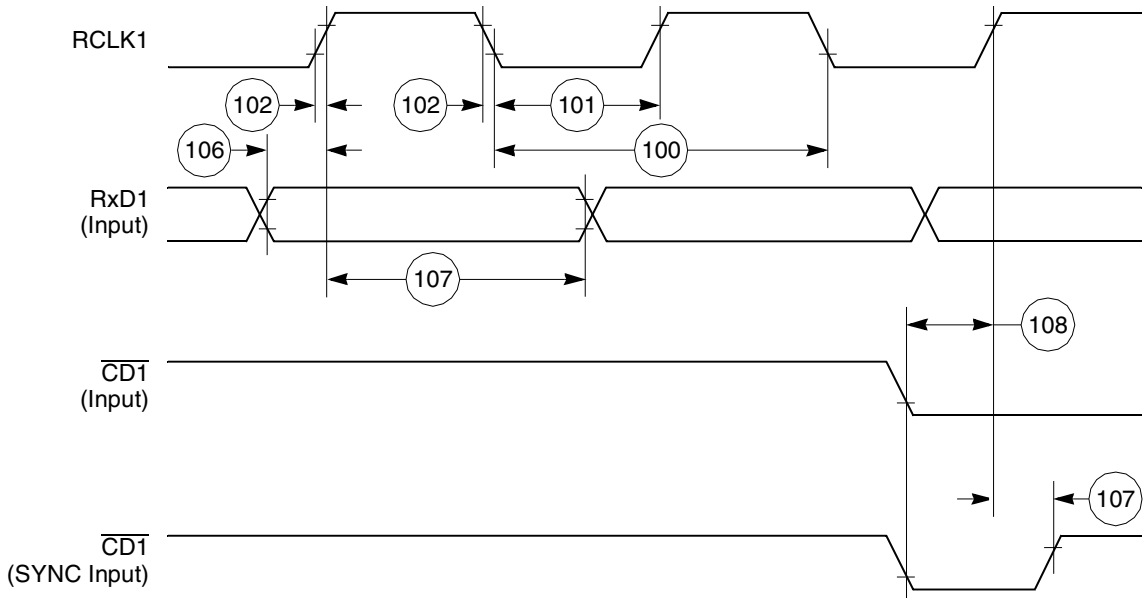


Figure 59. SCC NMSI Receive Timing Diagram

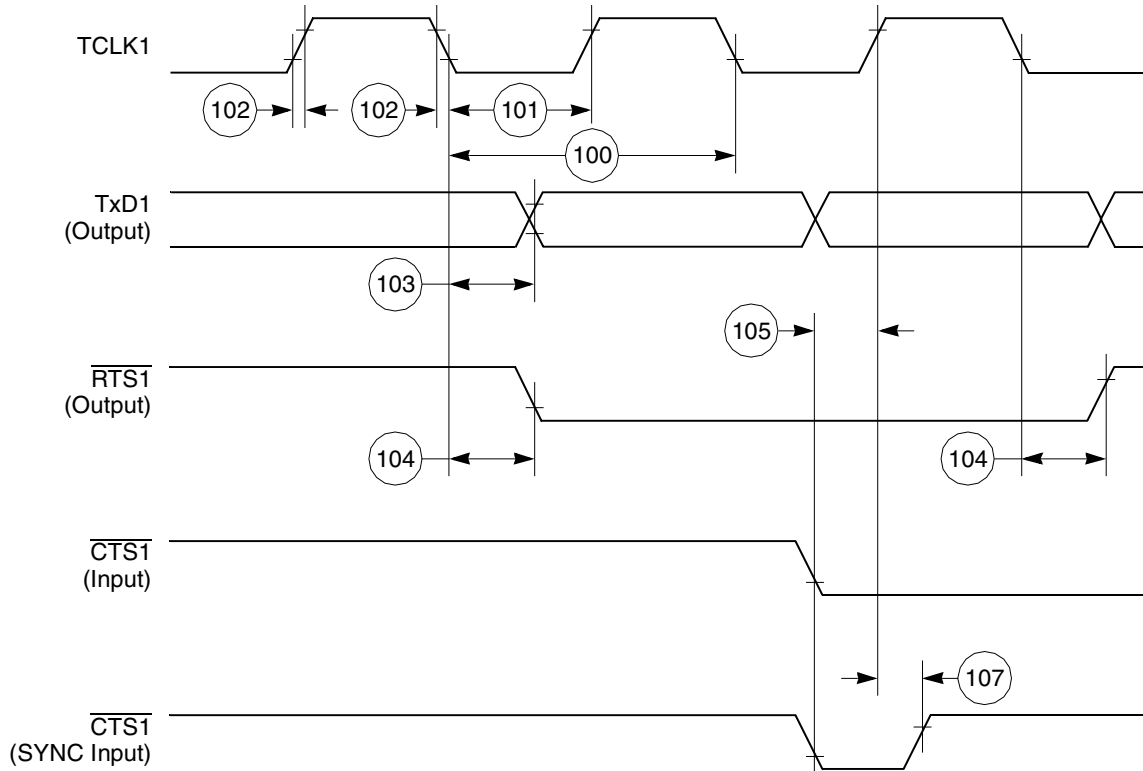


Figure 60. SCC NMSI Transmit Timing Diagram

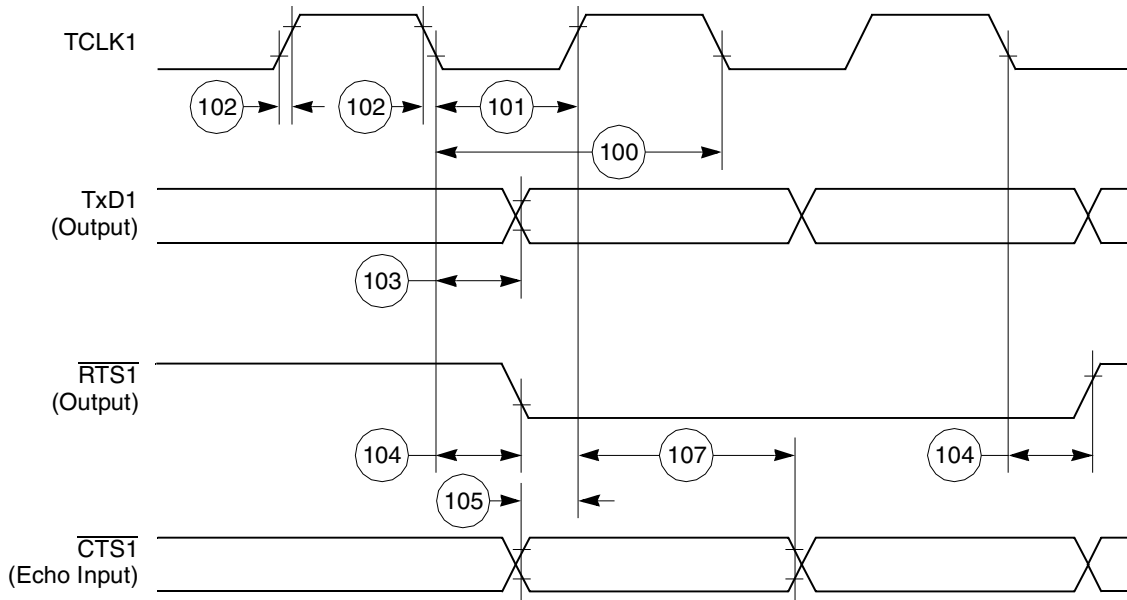


Figure 61. HDLC Bus Timing Diagram

12.8 Ethernet Electrical Specifications

Table 24 provides the Ethernet timings as shown in Figure 62 through Figure 64.

Table 24. Ethernet Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|---|-----------------|-----|------|
| | | Min | Max | |
| 120 | CLSN width high | 40 | — | ns |
| 121 | RCLK1 rise/fall time | — | 15 | ns |
| 122 | RCLK1 width low | 40 | — | ns |
| 123 | RCLK1 clock period ¹ | 80 | 120 | ns |
| 124 | RXD1 setup time | 20 | — | ns |
| 125 | RXD1 hold time | 5 | — | ns |
| 126 | RENA active delay (from RCLK1 rising edge of the last data bit) | 10 | — | ns |
| 127 | RENA width low | 100 | — | ns |
| 128 | TCLK1 rise/fall time | — | 15 | ns |
| 129 | TCLK1 width low | 40 | — | ns |
| 130 | TCLK1 clock period ¹ | 99 | 101 | ns |
| 131 | TXD1 active delay (from TCLK1 rising edge) | — | 50 | ns |
| 132 | TXD1 inactive delay (from TCLK1 rising edge) | 6.5 | 50 | ns |
| 133 | TENA active delay (from TCLK1 rising edge) | 10 | 50 | ns |

Table 24. Ethernet Timing (continued)

| Num | Characteristic | All Frequencies | | Unit |
|-----|--|-----------------|-----|------|
| | | Min | Max | |
| 134 | TENA inactive delay (from TCLK1 rising edge) | 10 | 50 | ns |
| 138 | CLKO1 low to $\overline{\text{SDACK}}$ asserted ² | — | 20 | ns |
| 139 | CLKO1 low to $\overline{\text{SDACK}}$ negated ² | — | 20 | ns |

¹ The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2/1.

² $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

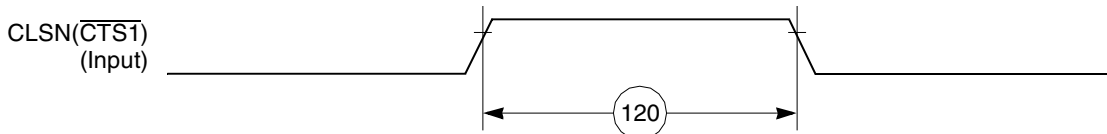


Figure 62. Ethernet Collision Timing Diagram

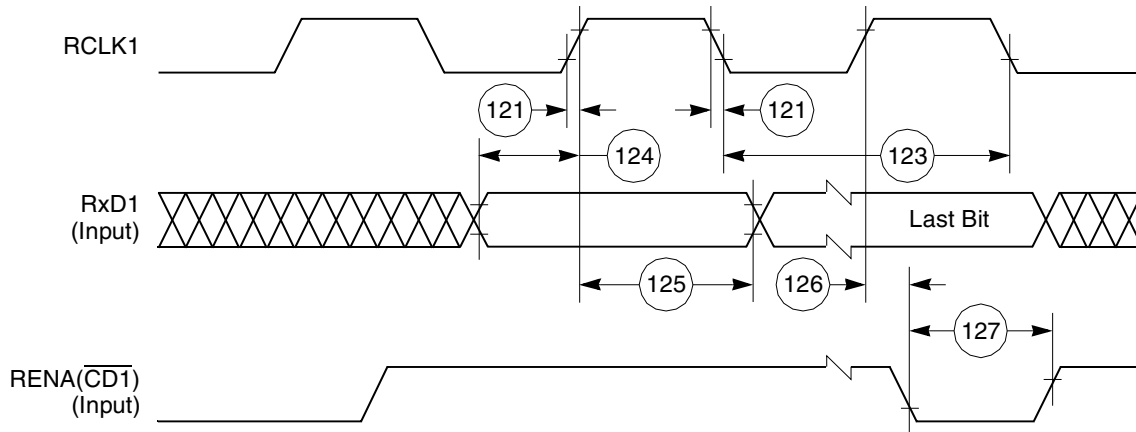
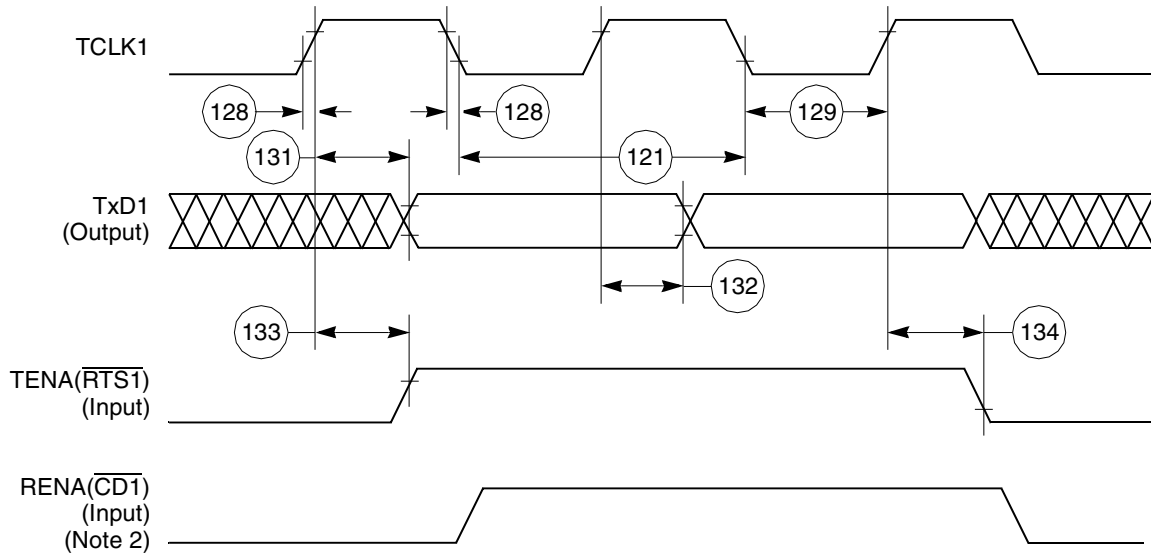


Figure 63. Ethernet Receive Timing Diagram



Notes:

1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is negated before TENA or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 64. Ethernet Transmit Timing Diagram

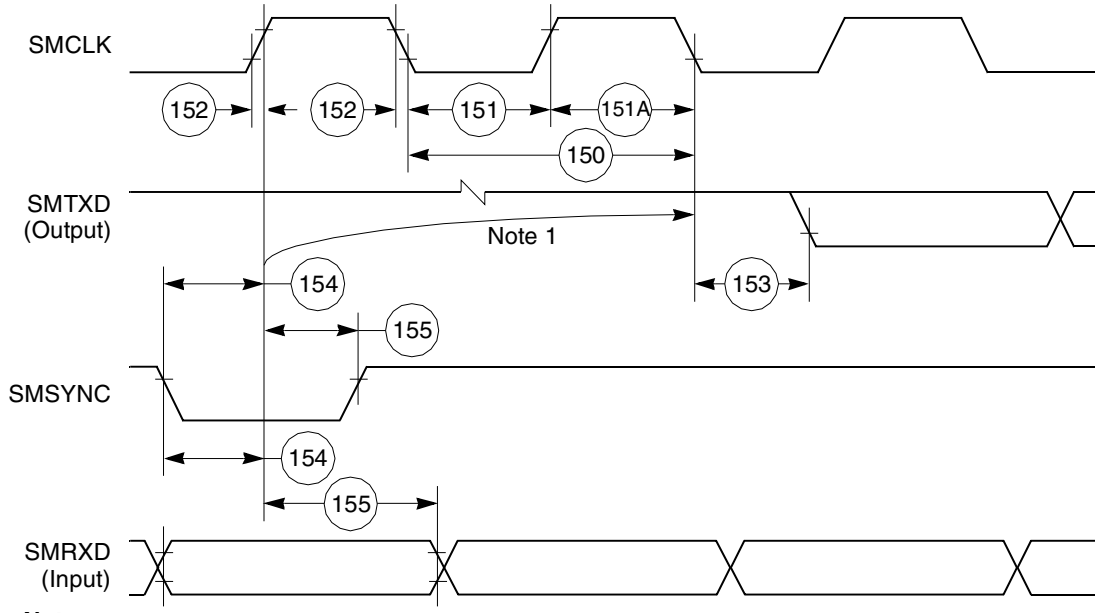
12.9 SMC Transparent AC Electrical Specifications

Table 25 provides the SMC transparent timings as shown in Figure 65.

Table 25. SMC Transparent Timing

| Num | Characteristic | All Frequencies | | Unit |
|------|--|-----------------|-----|------|
| | | Min | Max | |
| 150 | SMCLK clock period ¹ | 100 | — | ns |
| 151 | SMCLK width low | 50 | — | ns |
| 151A | SMCLK width high | 50 | — | ns |
| 152 | SMCLK rise/fall time | — | 15 | ns |
| 153 | SMTXD active delay (from SMCLK falling edge) | 10 | 50 | ns |
| 154 | SMRXD/SMSYNC setup time | 20 | — | ns |
| 155 | RXD1/SMSYNC hold time | 5 | — | ns |

¹ SyncCLK must be at least twice as fast as SMCLK.



Note:
1. This delay is equal to an integer number of character-length clocks.

Figure 65. SMC Transparent Timing Diagram

12.10 SPI Master AC Electrical Specifications

Table 26 provides the SPI master timings as shown in Figure 66 and Figure 67.

Table 26. SPI Master Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|-------------------------------------|-----------------|------|-----------|
| | | Min | Max | |
| 160 | MASTER cycle time | 4 | 1024 | t_{cyc} |
| 161 | MASTER clock (SCK) high or low time | 2 | 512 | t_{cyc} |
| 162 | MASTER data setup time (inputs) | 15 | — | ns |
| 163 | Master data hold time (inputs) | 0 | — | ns |
| 164 | Master data valid (after SCK edge) | — | 10 | ns |
| 165 | Master data hold time (outputs) | 0 | — | ns |
| 166 | Rise time output | — | 15 | ns |
| 167 | Fall time output | — | 15 | ns |

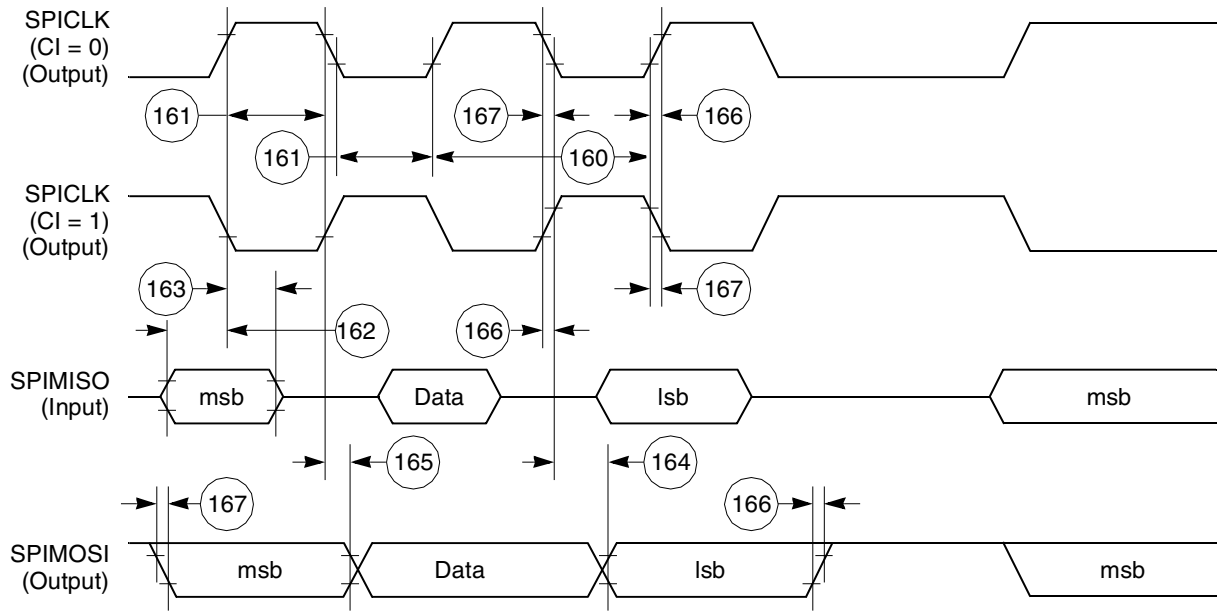


Figure 66. SPI Master (CP = 0) Timing Diagram

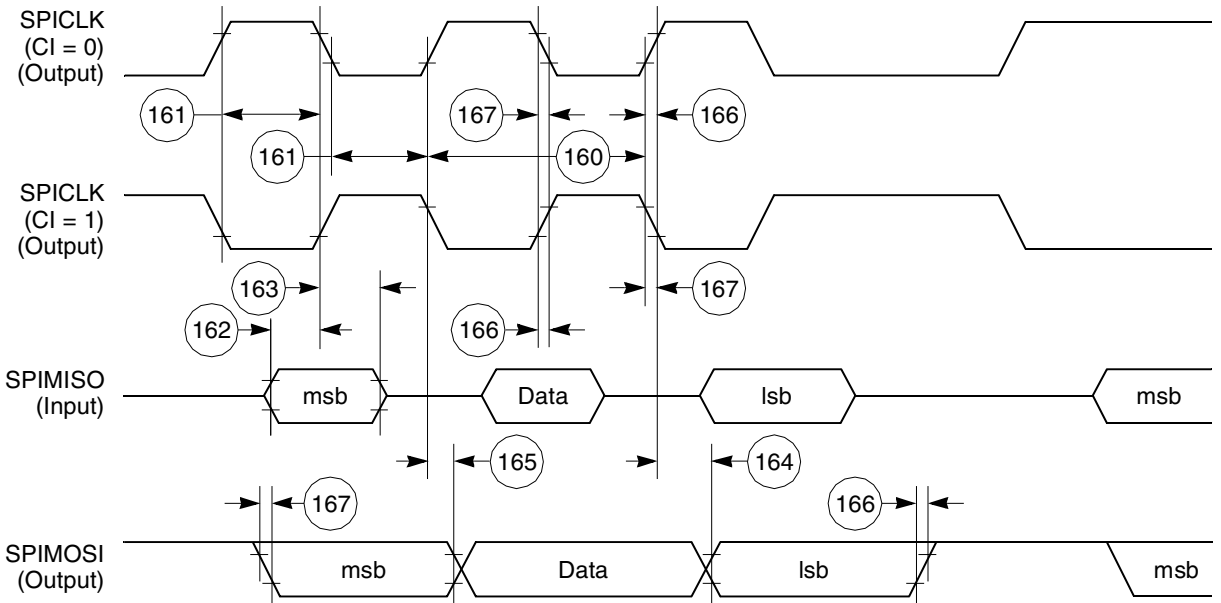


Figure 67. SPI Master (CP = 1) Timing Diagram

12.11 SPI Slave AC Electrical Specifications

Table 27 provides the SPI slave timings as shown in Figure 68 and Figure 69.

Table 27. SPI Slave Timing

| Num | Characteristic | All Frequencies | | Unit |
|-----|---|-----------------|-----|-----------|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | t_{cyc} |
| 171 | Slave enable lead time | 15 | — | ns |
| 172 | Slave enable lag time | 15 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | t_{cyc} |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | t_{cyc} |
| 175 | Slave data setup time (inputs) | 20 | — | ns |
| 176 | Slave data hold time (inputs) | 20 | — | ns |
| 177 | Slave access time | — | 50 | ns |

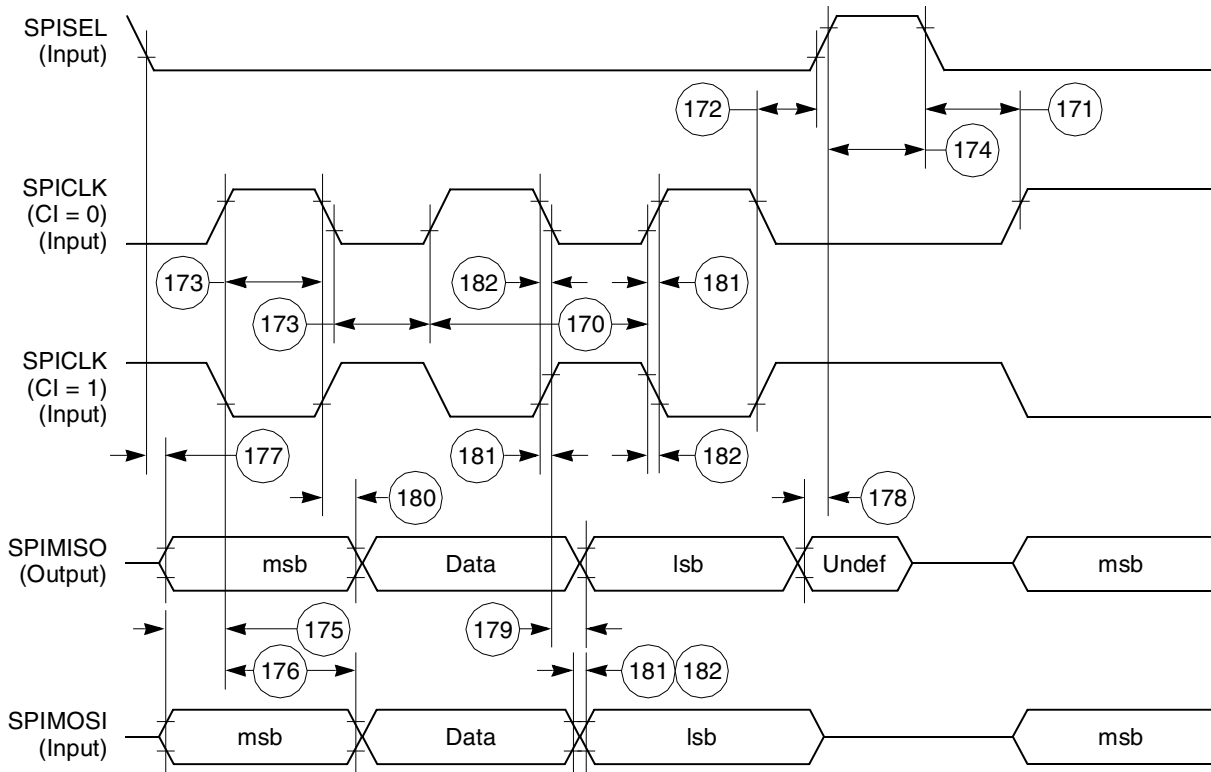


Figure 68. SPI Slave (CP = 0) Timing Diagram

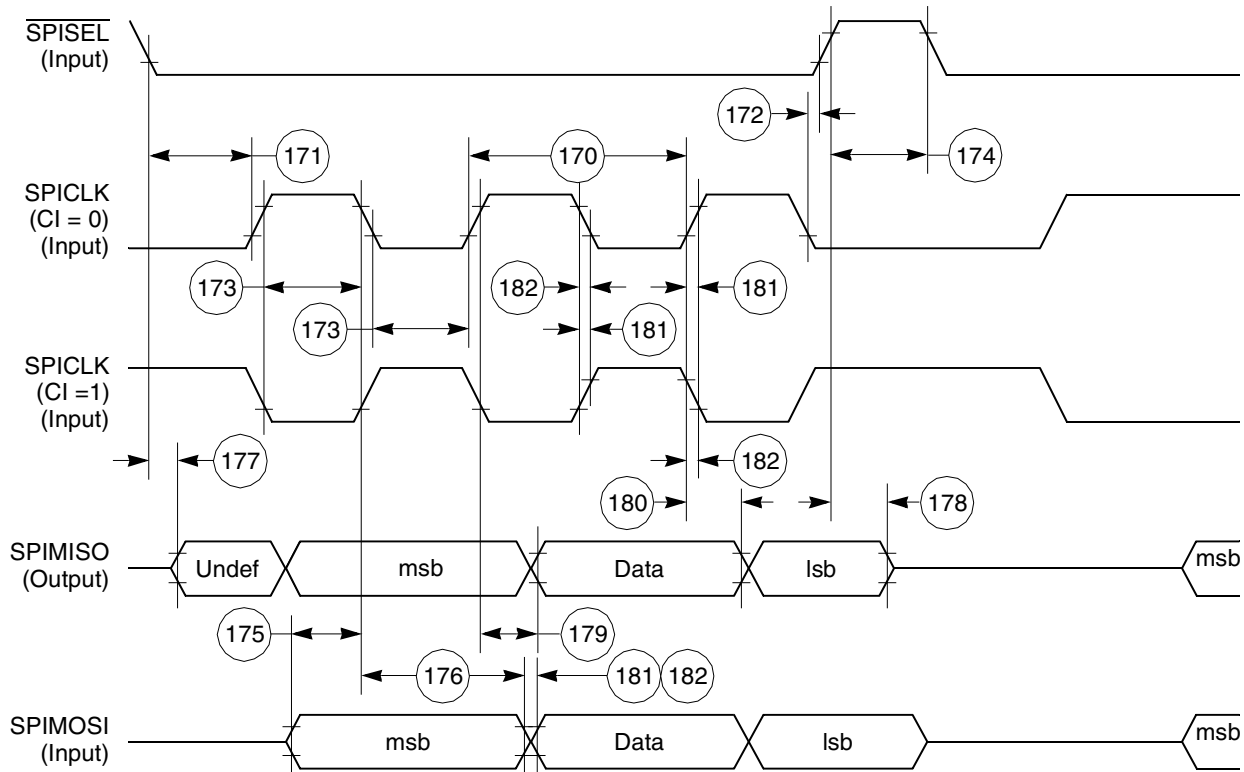


Figure 69. SPI Slave (CP = 1) Timing Diagram

12.12 I²C AC Electrical Specifications

Table 28 provides the I²C (SCL < 100 kHz) timings.

Table 28. I²C Timing (SCL < 100 kHz)

| Num | Characteristic | All Frequencies | | Unit |
|-----|---|-----------------|-----|------|
| | | Min | Max | |
| 200 | SCL clock frequency (slave) | 0 | 100 | kHz |
| 200 | SCL clock frequency (master) ¹ | 1.5 | 100 | kHz |
| 202 | Bus free time between transmissions | 4.7 | — | μs |
| 203 | Low period of SCL | 4.7 | — | μs |
| 204 | High period of SCL | 4.0 | — | μs |
| 205 | Start condition setup time | 4.7 | — | μs |
| 206 | Start condition hold time | 4.0 | — | μs |
| 207 | Data hold time | 0 | — | μs |
| 208 | Data setup time | 250 | — | ns |
| 209 | SDL/SCL rise time | — | 1 | μs |

Table 28. I²C Timing (SCL < 100 kHz) (continued)

| Num | Characteristic | All Frequencies | | Unit |
|-----|---------------------------|-----------------|-----|------|
| | | Min | Max | |
| 210 | SDL/SCL fall time | — | 300 | ns |
| 211 | Stop condition setup time | 4.7 | — | μs |

¹ SCL frequency is given by $SCL = BRGCLK_frequency / ((BRG\ register + 3) \times pre_scaler \times 2)$.
The ratio $SyncClk / (BRGCLK / pre_scaler)$ must be greater or equal to 4/1.

Table 29 provides the I²C (SCL > 100 kHz) timings.

Table 29. I²C Timing (SCL > 100 kHz)

| Num | Characteristic | Expression | All Frequencies | | Unit |
|-----|---|------------|---------------------------|------------------------|------|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master) ¹ | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | — | $1 / (2.2 \times fSCL)$ | — | s |
| 203 | Low period of SCL | — | $1 / (2.2 \times fSCL)$ | — | s |
| 204 | High period of SCL | — | $1 / (2.2 \times fSCL)$ | — | s |
| 205 | Start condition setup time | — | $1 / (2.2 \times fSCL)$ | — | s |
| 206 | Start condition hold time | — | $1 / (2.2 \times fSCL)$ | — | s |
| 207 | Data hold time | — | 0 | — | s |
| 208 | Data setup time | — | $1 / (40 \times fSCL)$ | — | s |
| 209 | SDL/SCL rise time | — | — | $1 / (10 \times fSCL)$ | s |
| 210 | SDL/SCL fall time | — | — | $1 / (33 \times fSCL)$ | s |
| 211 | Stop condition setup time | — | $1 / 2 (2.2 \times fSCL)$ | — | s |

¹ SCL frequency is given by $SCL = BrgClk_frequency / ((BRG\ register + 3) \times pre_scaler \times 2)$.
The ratio $SyncClk / (Brg_Clk / pre_scaler)$ must be greater or equal to 4/1.

Figure 70 shows the I²C bus timing.

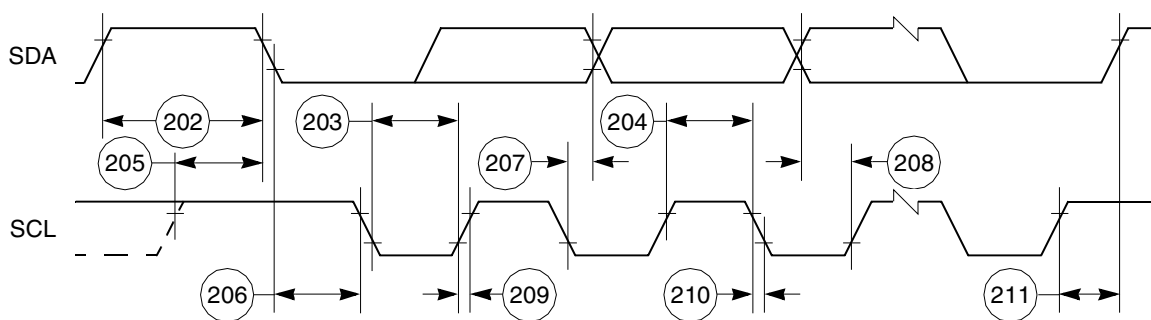


Figure 70. I²C Bus Timing Diagram

13 UTOPIA AC Electrical Specifications

Table 30, Table 31, and Table 32, show the AC electrical specifications for the UTOPIA interface.

Table 30. UTOPIA Master (Muxed Mode) Electrical Specifications

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|-----|---|-----------|-----|-----|------|
| U1 | UtpClk rise/fall time (internal clock option) | Output | | 4 | ns |
| | Duty cycle | | 50 | 50 | % |
| | Frequency | | | 33 | MHz |
| U2 | UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr active delay (PHREQ and PHSEL active delay in multi-PHY mode) | Output | 2 | 16 | ns |
| U3 | UTPB, SOC, Rxclav, and Txclav setup time | Input | 4 | | ns |
| U4 | UTPB, SOC, Rxclav, and Txclav hold time | Input | 1 | | ns |

Table 31. UTOPIA Master (Split Bus Mode) Electrical Specifications

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|-----|---|-----------|-----|-----|------|
| U1 | UtpClk rise/fall time (Internal clock option) | Output | | 4 | ns |
| | Duty cycle | | 50 | 50 | % |
| | Frequency | | | 33 | MHz |
| U2 | UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr active delay (PHREQ and PHSEL active delay in multi-PHY mode) | Output | 2 | 16 | ns |
| U3 | UTPB_Aux, SOC_Aux, Rxclav, and Txclav setup time | Input | 4 | | ns |
| U4 | UTPB_Aux, SOC_Aux, Rxclav, and Txclav hold time | Input | 1 | | ns |

Table 32. UTOPIA Slave (Split Bus Mode) Electrical Specifications

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|-----|--|-----------|-----|-----|------|
| U1 | UtpClk rise/fall time (external clock option) | Input | | 4 | ns |
| | Duty cycle | | 40 | 60 | % |
| | Frequency | | | 33 | MHz |
| U2 | UTPB, SOC, Rxclav, and Txclav active delay | Output | 2 | 16 | ns |
| U3 | UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr setup time | Input | 4 | | ns |
| U4 | UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr hold time | Input | 1 | | ns |

Figure 71 shows signal timings during UTOPIA receive operations.

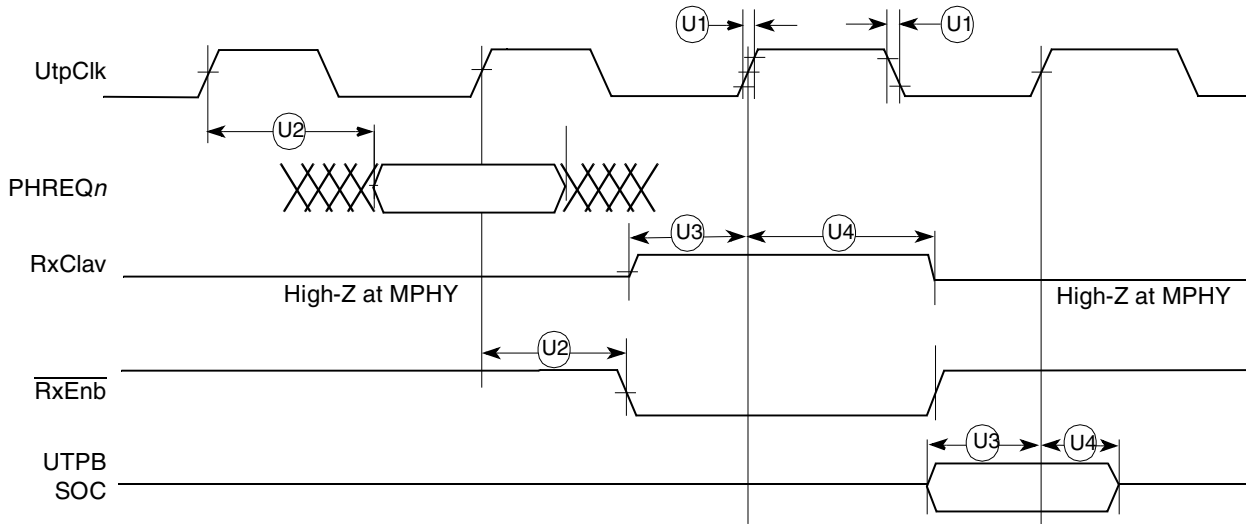


Figure 71. UTOPIA Receive Timing

Figure 72 shows signal timings during UTOPIA transmit operations.

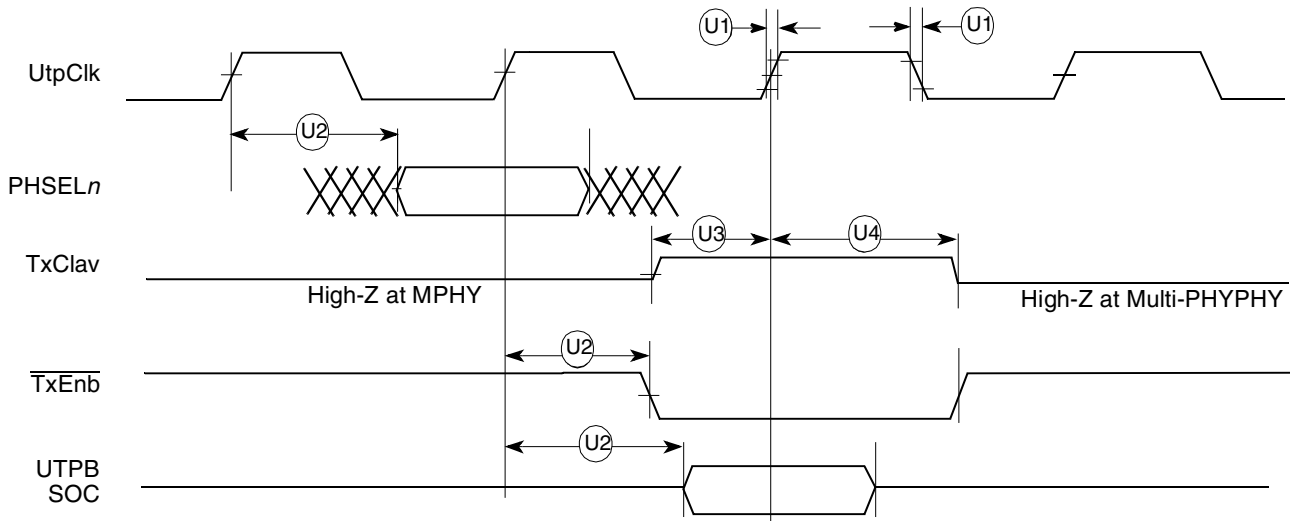


Figure 72. UTOPIA Transmit Timing

14 USB Electrical Characteristics

This section provides the AC timings for the USB interface.

14.1 USB Interface AC Timing Specifications

The USB Port uses the transmit clock on SCC1. [Table 33](#) lists the USB interface timings.

Table 33. USB Interface AC Timing Specifications

| Name | Characteristic | All Frequencies | | Unit |
|------|--|-----------------|-----|------|
| | | Min | Max | |
| US1 | USBCLK frequency of operation ¹ | | | |
| | Low speed | 6 | | MHz |
| | Full speed | 48 | | MHz |
| US4 | USBCLK duty cycle (measured at 1.5 V) | 45 | 55 | % |

¹ USBCLK accuracy should be ± 500 ppm or better. USBCLK may be stopped to conserve power.

15 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

15.1 MII and Reduced MII Receive Signal Timing

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. The reduced MII (RMII) receiver functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency - 1%.

[Table 34](#) provides information on the MII and RMII receive signal timing.

Table 34. MII Receive Signal Timing

| Num | Characteristic | Min | Max | Unit |
|---------|---|-----|-----|-------------------|
| M1 | MII_RXD[3:0], MII_RX_DV, MII_RX_ERR to MII_RX_CLK setup | 5 | — | ns |
| M2 | MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold | 5 | — | ns |
| M3 | MII_RX_CLK pulse width high | 35% | 65% | MII_RX_CLK period |
| M4 | MII_RX_CLK pulse width low | 35% | 65% | MII_RX_CLK period |
| M1_RMII | RMII_RXD[1:0], RMII_CRSDV, RMII_RX_ERR to RMII_REFCLK setup | 4 | — | ns |
| M2_RMII | RMII_REFCLK to RMII_RXD[1:0], RMII_CRSDV, RMII_RX_ERR hold | 2 | — | ns |

Figure 73 shows MII receive signal timing.

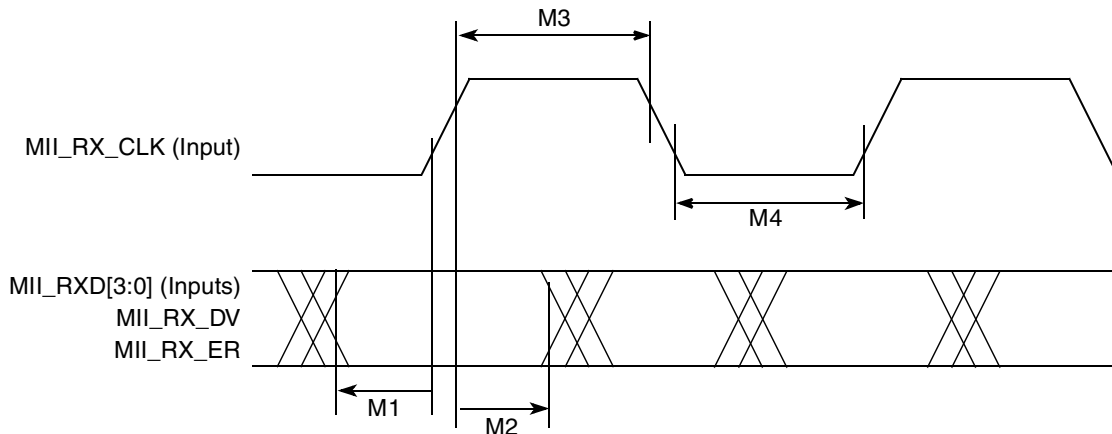


Figure 73. MII Receive Signal Timing Diagram

15.2 MII and Reduced MII Transmit Signal Timing

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz + 1%. The RMII transmitter functions correctly up to a RMII_REFCLK maximum frequency of 50 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 35 provides information on the MII and RMII transmit signal timing.

Table 35. MII Transmit Signal Timing

| Num | Characteristic | Min | Max | Unit |
|----------|--|-----|-----|----------------------------------|
| M5 | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid | 5 | — | ns |
| M6 | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid | — | 25 | ns |
| M20_RMII | RMII_TXD[1:0], RMII_TX_EN to RMII_REFCLK setup | 4 | — | ns |
| M21_RMII | RMII_TXD[1:0], RMII_TX_EN data hold from RMII_REFCLK rising edge | 2 | — | ns |
| M7 | MII_TX_CLK and RMII_REFCLK pulse width high | 35% | 65% | MII_TX_CLK or RMII_REFCLK period |
| M8 | MII_TX_CLK and RMII_REFCLK pulse width low | 35% | 65% | MII_TX_CLK or RMII_REFCLK period |

Figure 74 shows the MII transmit signal timing diagram.

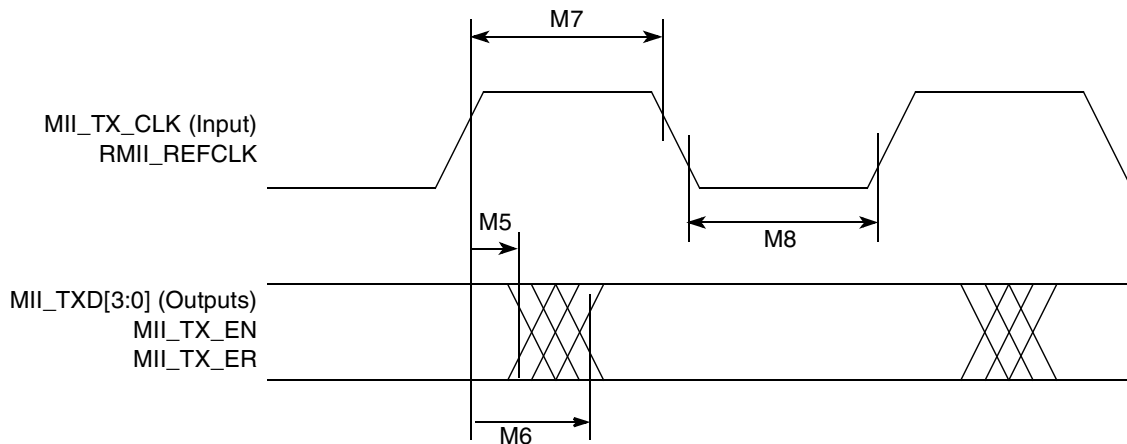


Figure 74. MII Transmit Signal Timing Diagram

15.3 MII Async Inputs Signal Timing (MII_CRSS, MII_COL)

Table 36 provides information on the MII async inputs signal timing.

Table 36. MII Async Inputs Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|---------------------------------------|-----|-----|-------------------|
| M9 | MII_CRSS, MII_COL minimum pulse width | 1.5 | — | MII_TX_CLK period |

Figure 75 shows the MII asynchronous inputs signal timing diagram.

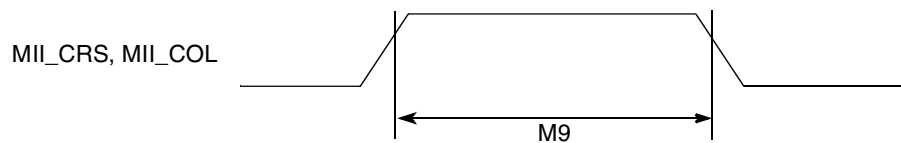


Figure 75. MII Async Inputs Timing Diagram

15.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 37 provides information on the MII serial management channel signal timing. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz.

Table 37. MII Serial Management Channel Timing

| Num | Characteristic | Min | Max | Unit |
|-----|---|-----|-----|------|
| M10 | MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | MII_MDC falling edge to MII_MDIO output valid (max prop delay) | — | 25 | ns |
| M12 | MII_MDIO (input) to MII_MDC rising edge setup | 10 | — | ns |
| M13 | MII_MDIO (input) to MII_MDC rising edge hold | 0 | — | ns |

Table 37. MII Serial Management Channel Timing (continued)

| Num | Characteristic | Min | Max | Unit |
|-----|--------------------------|-----|-----|----------------|
| M14 | MII_MDC pulse width high | 40% | 60% | MII_MDC period |
| M15 | MII_MDC pulse width low | 40% | 60% | MII_MDC period |

Figure 76 shows the MII serial management channel timing diagram.

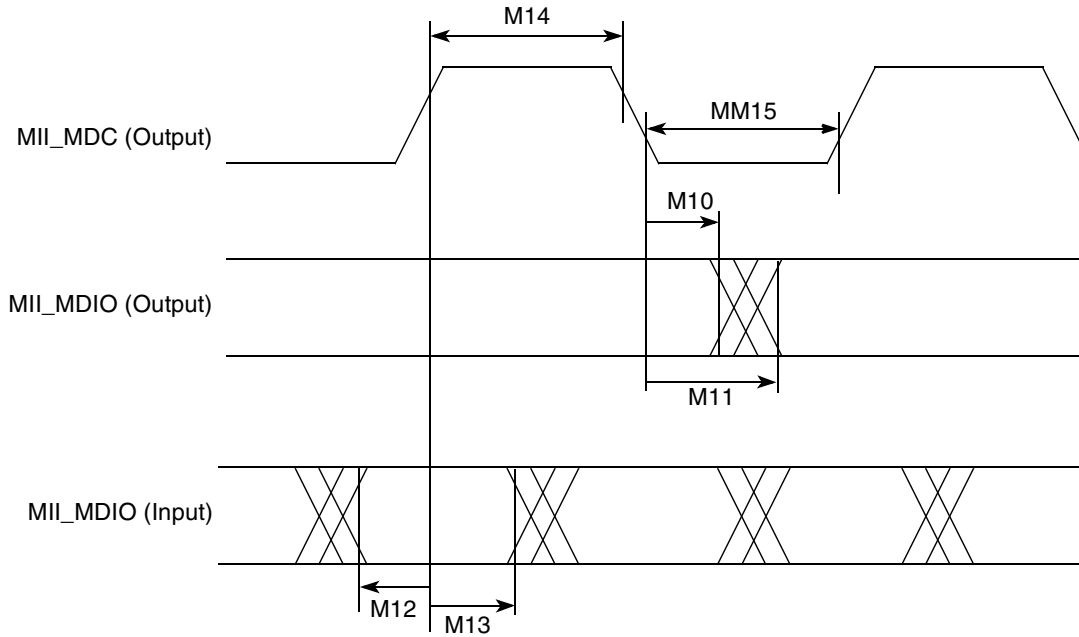


Figure 76. MII Serial Management Channel Timing Diagram

16 Mechanical Data and Ordering Information

Table 38 identifies the available packages and operating frequencies for the MPC885/MPC880 derivative devices.

Table 38. Available MPC885/MPC880 Packages/Frequencies

| Package Type | Temperature (Tj) | Frequency (MHz) | Order Number |
|--|------------------|-----------------|--|
| Plastic ball grid array ZP suffix — Leaded VR suffix — Lead-Free are available as needed | 0°C to 95°C | 66 | KMPC885ZP66 KMPC880ZP66 MPC885ZP66 MPC880ZP66 |
| | | 80 | KMPC885ZP80 KMPC880ZP80 MPC885ZP80 MPC880ZP80 |
| | | 133 | KMPC885ZP133 KMPC880ZP133 MPC885ZP133 MPC880ZP133 |
| Plastic ball grid array CZP suffix — Leaded CVR suffix — Lead-Free are available as needed | -40°C to 100°C | 66 | KMPC885CZP66 KMPC880CZP66 MPC885CZP66 MPC880CZP66 |
| | | 133 | KMPC885CZP133 KMPC880CZP133 MPC885CZP133 MPC880CZP133 |

16.1 Pin Assignments

Figure 77 shows the top-view pinout of the PBGA package. For additional information, see the *MPC885 PowerQUICC™ Family Reference Manual*.

NOTE: This is the top view of the device.

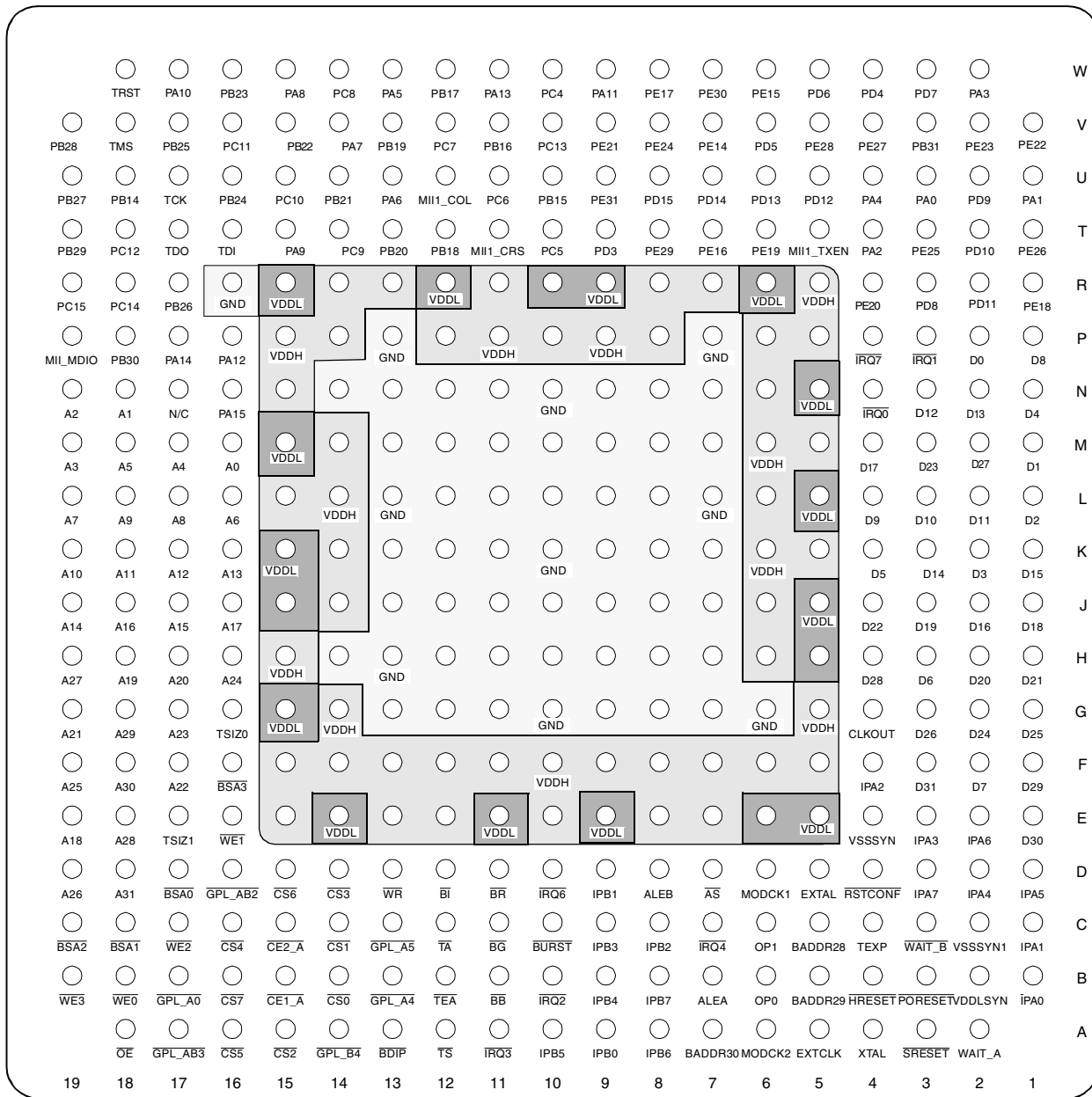


Figure 77. Pinout of the PBGA Package

Table 39 contains a list of the MPC885 input and output signals and shows multiplexing and pin assignments.

Table 39. Pin Assignments

| Name | Pin Number | Type |
|--|--|---------------------------------|
| A[0:31] | M16, N18, N19, M19, M17, M18, L16, L19, L17, L18, K19, K18, K17, K16, J19, J17, J18, J16, E19, H18, H17, G19, F17, G17, H16, F19, D19, H19, E18, G18, F18, D18 | Bidirectional Three-state |
| D[0:31] | P2, M1, L1, K2, N1, K4, H3, F2, P1, L4, L3, L2, N3, N2, K3, K1, J2, M4, J1, J3, H2, H1, J4, M3, G2, G1, G3, M2, H4, F1, E1, F3 | Bidirectional Three-state |
| TSIZ0, $\overline{\text{REG}}$ | G16 | Bidirectional Three-state |
| TSIZ1 | E17 | Bidirectional Three-state |
| $\overline{\text{RD/WR}}$ | D13 | Bidirectional Three-state |
| $\overline{\text{BURST}}$ | C10 | Bidirectional Three-state |
| $\overline{\text{BDIP}}$, $\overline{\text{GPL_B5}}$ | A13 | Output |
| $\overline{\text{TS}}$ | A12 | Bidirectional Active pull-up |
| $\overline{\text{TA}}$ | C12 | Bidirectional Active pull-up |
| $\overline{\text{TEA}}$ | B12 | Open-drain |
| $\overline{\text{BI}}$ | D12 | Bidirectional Active pull-up |
| $\overline{\text{IRQ2}}$, $\overline{\text{RSV}}$ | B10 | Bidirectional Three-state |
| $\overline{\text{IRQ4}}$, $\overline{\text{KR}}$, $\overline{\text{RETRY}}$, SPKROUT | C7 | Bidirectional Three-state |
| $\overline{\text{CR}}$, $\overline{\text{IRQ3}}$ | A11 | Input |
| $\overline{\text{BR}}$ | D11 | Bidirectional |
| $\overline{\text{BG}}$ | C11 | Bidirectional |
| $\overline{\text{BB}}$ | B11 | Bidirectional Active pull-up |
| FRZ, $\overline{\text{IRQ6}}$ | D10 | Bidirectional |
| $\overline{\text{IRQ0}}$ | N4 | Input |
| $\overline{\text{IRQ1}}$ | P3 | Input |
| $\overline{\text{IRQ7}}$ | P4 | Input |
| $\overline{\text{CS}}[0:5]$ | B14, C14, A15, D14, C16, A16 | Output |
| $\overline{\text{CS6}}$, $\overline{\text{CE1_B}}$ | D15 | Output |
| $\overline{\text{CS7}}$, $\overline{\text{CE2_B}}$ | B16 | Output |

Table 39. Pin Assignments (continued)

| Name | Pin Number | Type |
|--|--------------------|---------------------------|
| $\overline{WE0}$, $\overline{BS_B0}$, \overline{IORD} | B18 | Output |
| $\overline{WE1}$, $\overline{BS_B1}$, \overline{IOWR} | E16 | Output |
| $\overline{WE2}$, $\overline{BS_B2}$, \overline{PCOE} | C17 | Output |
| $\overline{WE3}$, $\overline{BS_B3}$, \overline{PCWE} | B19 | Output |
| $\overline{BS_A[0:3]}$ | D17, C18, C19, F16 | Output |
| $\overline{GPL_A0}$, $\overline{GPL_B0}$ | B17 | Output |
| \overline{OE} , $\overline{GPL_A1}$, $\overline{GPL_B1}$ | A18 | Output |
| $\overline{GPL_A[2:3]}$, $\overline{GPL_B[2:3]}$, $\overline{CS[2:3]}$ | D16, A17 | Output |
| UPWAITA, $\overline{GPL_A4}$ | B13 | Bidirectional |
| UPWAITB, $\overline{GPL_B4}$ | A14 | Bidirectional |
| $\overline{GPL_A5}$ | C13 | Output |
| $\overline{PORESET}$ | B3 | Input |
| $\overline{RSTCONF}$ | D4 | Input |
| \overline{HRESET} | B4 | Open-drain |
| \overline{SRESET} | A3 | Open-drain |
| XTAL | A4 | Analog output |
| EXTAL | D5 | Analog input (3.3 V only) |
| CLKOUT | G4 | Output |
| EXTCLK | A5 | Input (3.3 V only) |
| TEXP | C4 | Output |
| ALE_A | B7 | Output |
| $\overline{CE1_A}$ | B15 | Output |
| $\overline{CE2_A}$ | C15 | Output |
| $\overline{WAIT_A}$, SOC_Split ¹ | A2 | Input |
| $\overline{WAIT_B}$ | C3 | Input |
| IP_A0, UTPB_Split0 ¹ | B1 | Input |
| IP_A1, UTPB_Split1 ¹ | C1 | Input |
| IP_A2, $\overline{IOIS16_A}$, UTPB_Split2 ¹ | F4 | Input |
| IP_A3, UTPB_Split3 ¹ | E3 | Input |
| IP_A4, UTPB_Split4 ¹ | D2 | Input |
| IP_A5, UTPB_Split5 ¹ | D1 | Input |
| IP_A6, UTPB_Split6 ¹ | E2 | Input |
| IP_A7, UTPB_Split7 ¹ | D3 | Input |

Table 39. Pin Assignments (continued)

| Name | Pin Number | Type |
|--|------------|---|
| ALE_B, DSCK/AT1 | D8 | Bidirectional Three-state |
| IP_B[0:1], IWP[0:1], VFLS[0:1] | A9, D9 | Bidirectional |
| IP_B2, $\overline{\text{IOIS16_B}}$, AT2 | C8 | Bidirectional Three-state |
| IP_B3, IWP2, VF2 | C9 | Bidirectional |
| IP_B4, LWP0, VF0 | B9 | Bidirectional |
| IP_B5, LWP1, VF1 | A10 | Bidirectional |
| IP_B6, DSDI, AT0 | A8 | Bidirectional Three-state |
| IP_B7, $\overline{\text{PTR}}$, AT3 | B8 | Bidirectional Three-state |
| OP0, UtpClk_Split ¹ | B6 | Bidirectional |
| OP1 | C6 | Output |
| OP2, MODCK1, $\overline{\text{STS}}$ | D6 | Bidirectional |
| OP3, MODCK2, DSDO | A6 | Bidirectional |
| BADDR30, $\overline{\text{REG}}$ | A7 | Output |
| BADDR[28:29] | C5, B5 | Output |
| $\overline{\text{AS}}$ | D7 | Input |
| PA15, USBRXD | N16 | Bidirectional |
| PA14, $\overline{\text{USBOE}}$ | P17 | Bidirectional (Optional: open-drain) |
| PA13, RXD2 | W11 | Bidirectional |
| PA12, TXD2 | P16 | Bidirectional (Optional: open-drain) |
| PA11, RXD4, MII1-TXD0, RMII1-TXD0 | W9 | Bidirectional (Optional: open-drain) |
| PA10, MII1-TXER, TIN4, CLK7 | W17 | Bidirectional (Optional: open-drain) |
| PA9, L1TXDA, RXD3 | T15 | Bidirectional (Optional: open-drain) |
| PA8, L1RXDA, TXD3 | W15 | Bidirectional (Optional: open-drain) |
| PA7, CLK1, L1RCLKA, BRGO1, TIN1 | V14 | Bidirectional |
| PA6, CLK2, $\overline{\text{TOUT1}}$ | U13 | Bidirectional |
| PA5, CLK3, L1TCLKA, BRGO2, TIN2 | W13 | Bidirectional |

Table 39. Pin Assignments (continued)

| Name | Pin Number | Type |
|---|------------|---|
| PA4, $\overline{CTS4}$, MII1-TXD1, RMII1-TXD1 | U4 | Bidirectional |
| PA3, MII1-RXER, RMII1-RXER, BRGO3 | W2 | Bidirectional |
| PA2, MII1-RXDV, RMII1-CRS_DV, TXD4 | T4 | Bidirectional |
| PA1, MII1-RXD0, RMII1-RXD0, BRGO4 | U1 | Bidirectional |
| PA0, MII1-RXD1, RMII1-RXD1, $\overline{TOUT4}$ | U3 | Bidirectional |
| PB31, \overline{SPISEL} , MII1-TXCLK, RMII1-REFCLK | V3 | Bidirectional (Optional: open-drain) |
| PB30, SPICLK | P18 | Bidirectional (Optional: open-drain) |
| PB29, SPIMOSI | T19 | Bidirectional (Optional: open-drain) |
| PB28, SPIMISO, BRGO4 | V19 | Bidirectional (Optional: open-drain) |
| PB27, I2CSDA, BRGO1 | U19 | Bidirectional (Optional: open-drain) |
| PB26, I2CSCL, BRGO2 | R17 | Bidirectional (Optional: open-drain) |
| PB25, RXADDR3 ¹ , TXADDR3, SMTXD1 | V17 | Bidirectional (Optional: open-drain) |
| PB24, TXADDR3 ¹ , RXADDR3, SMRXD1 | U16 | Bidirectional (Optional: open-drain) |
| PB23, TXADDR2 ¹ , RXADDR2, $\overline{SDACK1}$, $\overline{SMSYN1}$ | W16 | Bidirectional (Optional: open-drain) |
| PB22, TXADDR4 ¹ , RXADDR4, $\overline{SDACK2}$, $\overline{SMSYN2}$ | V15 | Bidirectional (Optional: open-drain) |
| PB21, SMTXD2, TXADDR1 ¹ , BRG01, RXADDR1, PHSEL[1] | U14 | Bidirectional (Optional: open-drain) |
| PB20, SMRXD2, L1CLKOA, TXADDR0 ¹ , RXADDR0, PHSEL[0] | T13 | Bidirectional (Optional: open-drain) |
| PB19, MII1-RXD3, $\overline{RTS4}$ | V13 | Bidirectional (Optional: open-drain) |
| PB18, RXADDR4 ¹ , TXADDR4, $\overline{RTS2}$, L1ST2 | T12 | Bidirectional (Optional: open-drain) |

Table 39. Pin Assignments (continued)

| Name | Pin Number | Type |
|--|------------|---|
| PB17, L1ST3, BRG02, RXADDR1 ¹ , TXADDR1, PHREQ[1] | W12 | Bidirectional (Optional: open-drain) |
| PB16, L1RQa, L1ST4, RTS4, RXADDR0 ¹ , TXADDR0, PHREQ[0] | V11 | Bidirectional (Optional: open-drain) |
| PB15, TXCLAV, BRG03, RXCLAV | U10 | Bidirectional |
| PB14RXADDR2 ¹ , TXADDR2 | U18 | Bidirectional |
| PC15, DREQ0, RTS3, L1ST1, TXCLAV, RXCLAV | R19 | Bidirectional |
| PC14, DREQ1, RTS2, L1ST2 | R18 | Bidirectional |
| PC13, MII1-TXD3, SDACK1 | V10 | Bidirectional |
| PC12, MII1-TXD2, TOUT1 | T18 | Bidirectional |
| PC11, USBRXP | V16 | Bidirectional |
| PC10, USBRXN, TGATE1 | U15 | Bidirectional |
| PC9, CTS2 | T14 | Bidirectional |
| PC8, CD2, TGATE2 | W14 | Bidirectional |
| PC7, CTS4, L1TSYNCB, USBTXP | V12 | Bidirectional |
| PC6, CD4, L1RSYNCB, USBTXN | U11 | Bidirectional |
| PC5, CTS3, L1TSYNCA, SDACK2 | T10 | Bidirectional |
| PC4, CD3, L1RSYNCA | W10 | Bidirectional |
| PD15, L1TSYNCA, UTPB0 | U8 | Bidirectional |
| PD14, L1RSYNCA, UTPB1 | U7 | Bidirectional |
| PD13, L1TSYNCB, UTPB2 | U6 | Bidirectional |
| PD12, L1RSYNCB, UTPB3 | U5 | Bidirectional |
| PD11, RXD3, RXENB | R2 | Bidirectional |
| PD10, TXD3, TXENB | T2 | Bidirectional |
| PD9, TXD4, UTPCLK | U2 | Bidirectional |
| PD8, RXD4, MII-MDC, RMII-MDC | R3 | Bidirectional |
| PD7, RTS3, UTPB4 | W3 | Bidirectional |
| PD6, RTS4, UTPB5 | W5 | Bidirectional |

Table 39. Pin Assignments (continued)

| Name | Pin Number | Type |
|---|------------|---|
| PD5, CLK8, L1TCLKB, UTPB6 | V6 | Bidirectional |
| PD4, CLK4, UTPB7 | W4 | Bidirectional |
| PD3, CLK7, TIN4, SOC | T9 | Bidirectional |
| PE31, CLK8, L1TCLKB, MII1-RXCLK | U9 | Bidirectional (Optional: open-drain) |
| PE30, L1RXDB, MII1-RXD2 | W7 | Bidirectional (Optional: open-drain) |
| PE29, MII2-CRS | T8 | Bidirectional (Optional: open-drain) |
| PE28, $\overline{\text{TOUT3}}$, MII2-COL | V5 | Bidirectional (Optional: open-drain) |
| PE27, $\overline{\text{RTS3}}$, L1RQB, MII2-RXER, RMII2-RXER | V4 | Bidirectional (Optional: open-drain) |
| PE26, L1CLKOB, MII2-RXDV, RMII2-CRS_DV | T1 | Bidirectional (Optional: open-drain) |
| PE25, RXD4, MII2-RXD3, L1ST2 | T3 | Bidirectional (Optional: open-drain) |
| PE24, SMRXD1, BRGO1, MII2-RXD2 | V8 | Bidirectional (Optional: open-drain) |
| PE23, $\overline{\text{SMSYN2}}$, TXD4, MII2-RXCLK, L1ST1 | V2 | Bidirectional (Optional: open-drain) |
| PE22, $\overline{\text{TOUT2}}$, MII2-RXD1, RMII2-RXD1, SDACK1 | V1 | Bidirectional (Optional: open-drain) |
| PE21, SMRXD2, $\overline{\text{TOUT1}}$, MII2-RXD0, RMII2-RXD0, $\overline{\text{RTS3}}$ | V9 | Bidirectional (Optional: open-drain) |
| PE20, L1RSYNCA, SMTXD2, $\overline{\text{CTS3}}$, MII2-TXER | R4 | Bidirectional (Optional: open-drain) |
| PE19, L1TXDB, MII2-TXEN, RMII2-TXEN | T6 | Bidirectional (Optional: open-drain) |
| PE18, L1TSYNCA, SMTXD1, MII2-TXD3 | R1 | Bidirectional (Optional: open-drain) |
| PE17, TIN3, CLK5, BRGO3, $\overline{\text{SMSYN1}}$, MII2-TXD2 | W8 | Bidirectional (Optional: open-drain) |
| PE16, L1RCLKB, CLK6, TXD3, MII2-TXCLK, RMII2-REFCLK | T7 | Bidirectional (Optional: open-drain) |
| PE15, $\overline{\text{TGATE1}}$, MII2-TXD1, RMII2-TXD1 | W6 | Bidirectional |

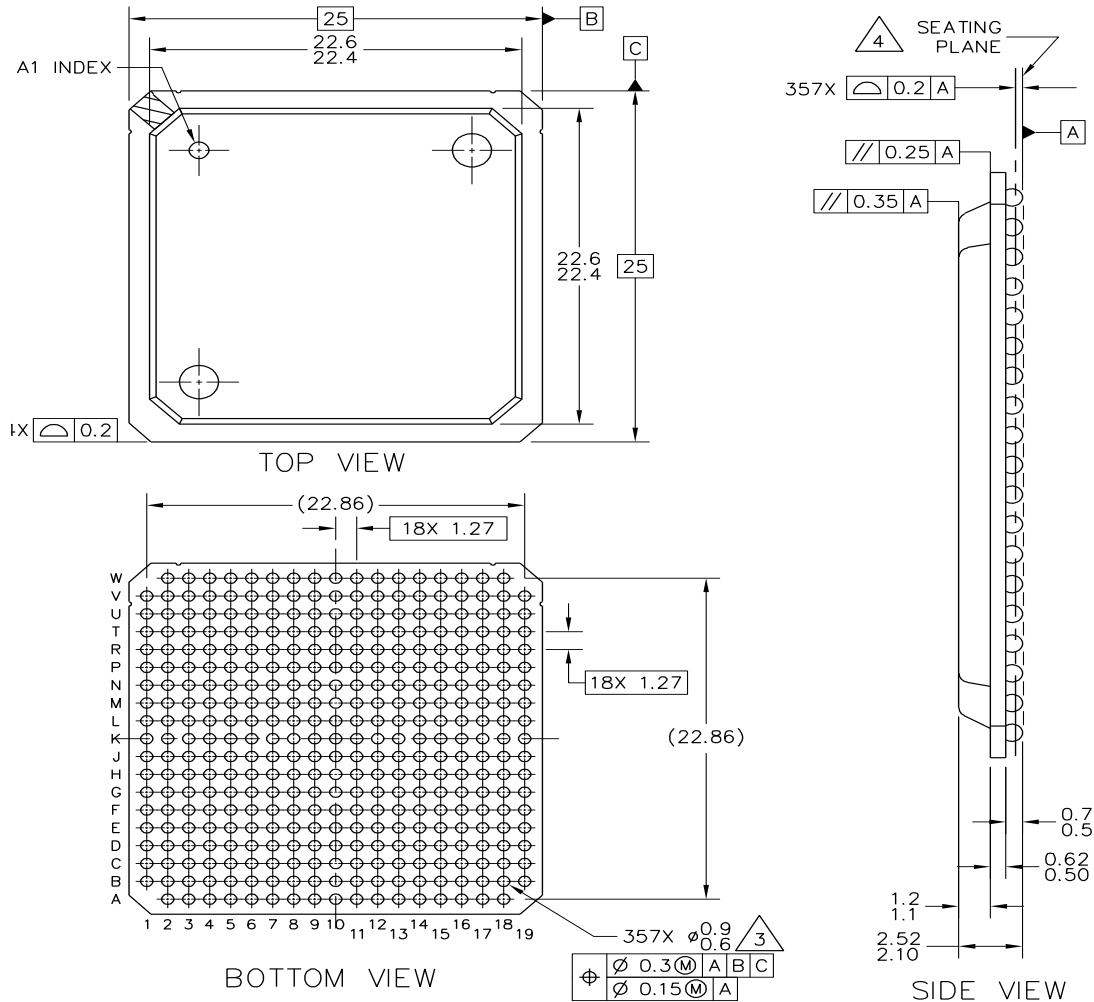
Table 39. Pin Assignments (continued)

| Name | Pin Number | Type |
|-----------------------------------|--|------------------------------------|
| PE14, RXD3, MII2-TXD0, RMII2-TXD0 | V7 | Bidirectional |
| TMS | V18 | Input |
| TDI, DSDI | T16 | Input |
| TCK, DSCK | U17 | Input |
| $\overline{\text{TRST}}$ | W18 | Input |
| TDO, DSDO | T17 | Output |
| MII1_CRS | T11 | Input |
| MII_MDIO | P19 | Bidirectional |
| MII1_TXEN, RMII1_TXEN | T5 | Output |
| MII1_COL | U12 | Input |
| V _{SSSYN1} | C2 | PLL analog V _{DD} and GND |
| V _{SSSYN} | E4 | Power |
| V _{DDL SYN} | B2 | Power |
| GND | G6, G7, G8, G9, G10, G11, G12, G13, H7, H8, H9, H10, H11, H12, H13, H14, J7, J8, J9, J10, J11, J12, J13, K7, K8, K9, K10, K11, K12, K13, L7, L8, L9, L10, L11, L12, L13, M7, M8, M9, M10, M11, M12, M13, N7, N8, N9, N10, N11, N12, N13, N14, P7, P13, R16 | Power |
| V _{DDL} | E5, E6, E9, E11, E14, G15, H5, J5, J15, K15, L5, M15, N5, R6, R9, R10, R12, R15 | Power |
| V _{DDH} | E7, E8, E10, E12, E13, E15, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, G5, G14, H6, H15, J6, J14, K5, K6, K14, L6, L14, L15, M5, M6, M14, N6, N15, P5, P6, P8, P9, P10, P11, P12, P14, P15, R5, R7, R8, R11, R13, R14 | Power |
| N/C | N17 | No connect |

¹ ESAR mode only.

16.2 Mechanical Dimensions of the PBGA Package

Figure 78 shows the mechanical dimensions of the PBGA package.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Figure 78. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package

17 Document Revision History

Table 40 lists significant changes between revisions of this hardware specification.

Table 40. Document Revision History

| Revision Number | Date | Changes |
|-----------------|-----------|---|
| 7 | 07/2010 | In Table 9, "Bus Operation Timings," changed the following: <ul style="list-style-type: none"> Updated TRLX condition value for B22a/b/c to "TRLX = [0 or 1]" Removed TRLX condition for B23 Updated condition and equation for B30 to "Invalid GPCM read/write access (MIN = 0.25 × B1 – 2.00)" Updated note 8 to "The timing B30 refers to \overline{CS} when ACS = 00 and to \overline{CS} and $\overline{WE}(0:3)$ when CSNT = 0." |
| 6 | 05/2010 | Added minimum load for CLKOUT in Section 10, "Bus Signal Timing." |
| 5 | 03/2009 | Updated formatting of Table 12, "PCMCIA Port Timing," Table 13, "Debug Port Timing," Table 14, "Reset Timing," and Table 15, "JTAG Timing." |
| 4 | 08/2007 | <ul style="list-style-type: none"> On page 1, updated first paragraph and added a second paragraph. After Table 2, inserted a new figure showing the undershoot/overshoot voltage (Figure 3) and renumbered the rest of the figures. In Table 9, for reset timings B29f and B29g added footnote indicating that the formula only applies to bus operation up to 50 MHz. In Figure 6, changed all reference voltage measurement points from 0.2 and 0.8 V to 50% level. In Table 18, changed num 46 description to read, "\overline{TA} assertion to rising edge ..." In Figure 49, changed \overline{TA} to reflect the rising edge of the clock. |
| 3.0 | 7/22/2004 | <ul style="list-style-type: none"> Added sentence to Spec B1A about EXTCLK and CLKOUT being in Alignment for Integer Values Added a footnote to Spec 41 specifying that EDM = 1 Added RMII1_EN under M1II_EN in Table 36 Pin Assignments Added a tablefootnote to Table 6 DC Electrical Specifications about meeting the VIL Max of the I2C Standard Put the new part numbers in the Ordering Information Section |
| 2.0 | 12/2003 | <ul style="list-style-type: none"> Changed the maximum operating frequency to 133 MHz. Put in the orderable part numbers that are orderable. Put the timing in the 80 MHz column. Rounded the timings to hundredths in the 80 MHz column. Put the pin numbers in footnotes by the maximum currents in Table 6. Changed 22 and 41 in the Timing. Put in the Thermal numbers. |
| 1.0 | 9/2003 | <ul style="list-style-type: none"> Added the DSP information in the Features list Fixed table formatting. Nontechnical edits. Released to the external web. |
| 0.9 | 8/2003 | Changed the USB description to full-/low-speed compatible. |
| 0.8 | 8/2003 | Added the Reference to USB 2.0 to the Features list and removed 1.1 from USB on the block diagrams. |
| 0.7 | 7/2003 | Added the RxClav and TxClav signals to PC15. |
| 0.6 | 6/2003 | Changed the pin descriptions per the June 22 spec. |
| 0.5 | 5/2003 | Changed some more typos, put in the phsel and phreq pins. Corrected the USB timing. |

Table 40. Document Revision History (continued)

| Revision Number | Date | Changes |
|-----------------|---------|--|
| 0.4 | 5/2003 | Changed the pin descriptions for PD8 and PD9. |
| 0.3 | 05/2003 | Corrected the signals that had overlines on them. |
| 0.2 | 05/2003 | Made the changes to the RMII Timing, Made sure all the V_{DDL} , V_{DDH} , and GND show up on the pinout diagram. Changed the SPI Master Timing Specs. 162 and 164. |
| 0.1 | 04/2003 | Added pinout and pinout assignments table. Added the USB timing to Section 14. Added the Reduced MII to Section 15. Removed the Data Parity. Made some changes to the Features list. |
| 0 | 02/2003 | Initial revision. |

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