

DATA SHEET

74F573

Octal transparent latch (3-State)

74F574

Octal transparent latch (3-State)

Product specification

1989 Oct 16

IC15 Data Handbook

Latch/flip-flop

74F573/74F574

74F573 Octal Transparent Latch (3-State) 74F574 Octal D Flip-Flop (3-State)

FEATURES

- 74F573 is broadside pinout version of 74F373
- 74F574 is broadside pinout version of 74F374
- Inputs and Outputs on opposite side of package allow easy interface to Microprocessors
- Useful as an Input or Output port for Microprocessors
- 3-State Outputs for Bus interfacing
- Common Output Enable
- 74F563 and 74F564 are inverting version of 74F573 and 74F574 respectively
- 3-State Outputs glitch free during power-up and power-down
- These are High-Speed replacements for N8TS805 and N8TS806

DESCRIPTION

The 74F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable (\overline{OE}) control gates.

The 74F573 is functionally identical to the 74F373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable (\overline{OE}) controls all eight 3-State buffers independent to the latch operation. When \overline{OE} is Low, the latched or transparent data appears at the outputs. When \overline{OE} is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F574 is functionally identical to the 74F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable (\overline{OE}) controls all eight 3-State buffers independently of the latch operation. When \overline{OE} is Low, the latched or transparent data appears at the outputs. When \overline{OE} is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|---------------------------|--------------------------------|
| 74F573 | 5.0ns | 35mA |

| TYPE | TYPICAL f_{MAX} | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|-------------------|--------------------------------|
| 74F574 | 180MHz | 50mA |

ORDERING INFORMATION

| DESCRIPTION | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ | PKG DWG # |
|---------------------|--|-----------|
| 20-Pin Plastic DIP | N74F573N, N74F574N | SOT146-1 |
| 20-Pin Plastic SOL | N74F573D, N74F574D | SOT163-1 |
| 20-Pin Plastic SSOP | N74F573DB | SOT339-1 |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

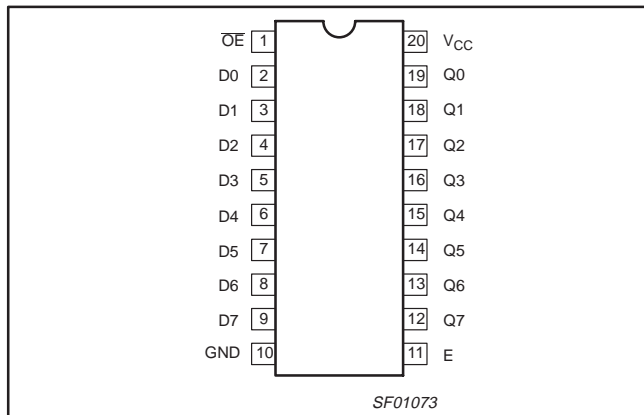
| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-----------------|--|---------------------|---------------------|
| D0 - D7 | Data inputs | 1.0/1.0 | 20 μ A/0.6mA |
| E (74F573) | Latch Enable input (active falling edge) | 1.0/1.0 | 20 μ A/0.6mA |
| \overline{OE} | Output Enable input (active Low) | 1.0/1.0 | 20 μ A/0.6mA |
| CP (74F574) | Clock Pulse input (active rising edge) | 1.0/1.0 | 20 μ A/0.6mA |
| Q0 - Q7 | 3-State outputs | 150/40 | 3.0mA/24mA |

NOTE: One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

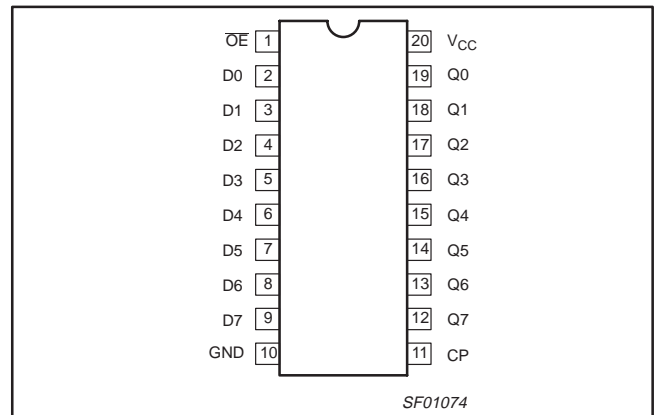
Latch/flip-flop

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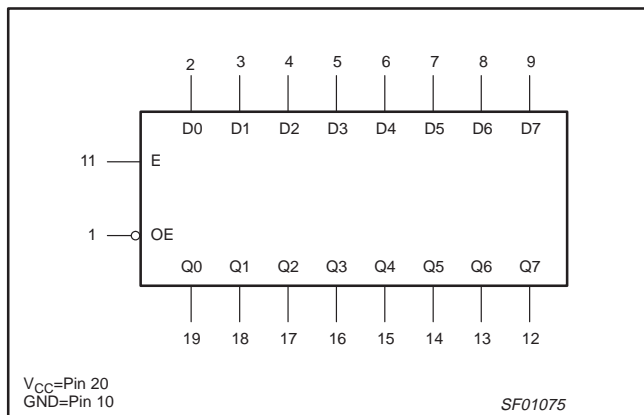
PIN CONFIGURATION – 74F573



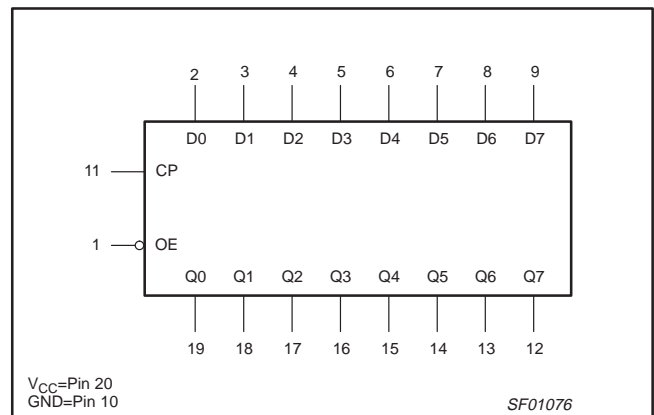
PIN CONFIGURATION – 74F574



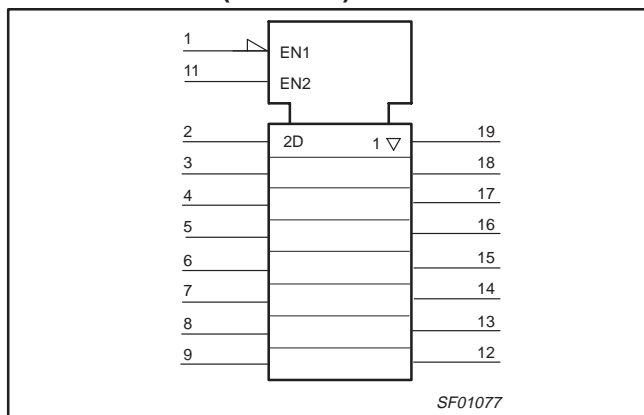
LOGIC SYMBOL – 74F573



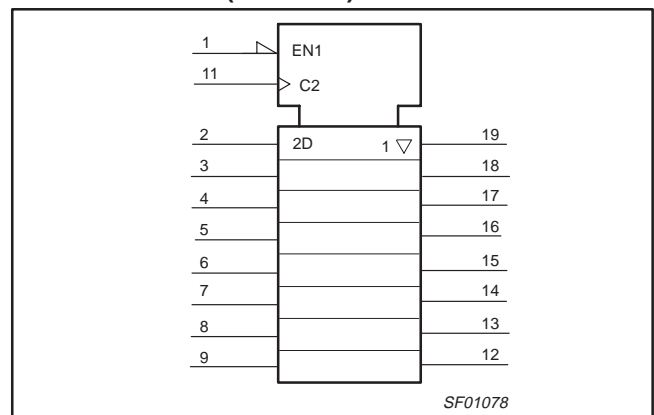
LOGIC SYMBOL – 74F574



LOGIC SYMBOL (IEEE/IEC) – 74F573



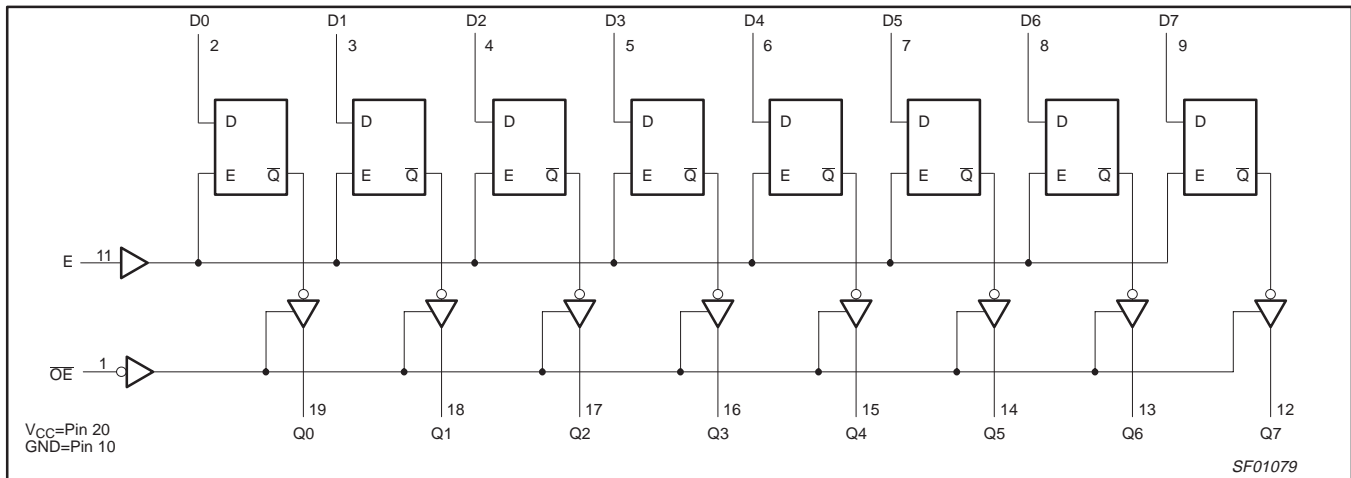
LOGIC SYMBOL (IEEE/IEC) – 74F574



Latch/flip-flop

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LOGIC DIAGRAM – 74F573

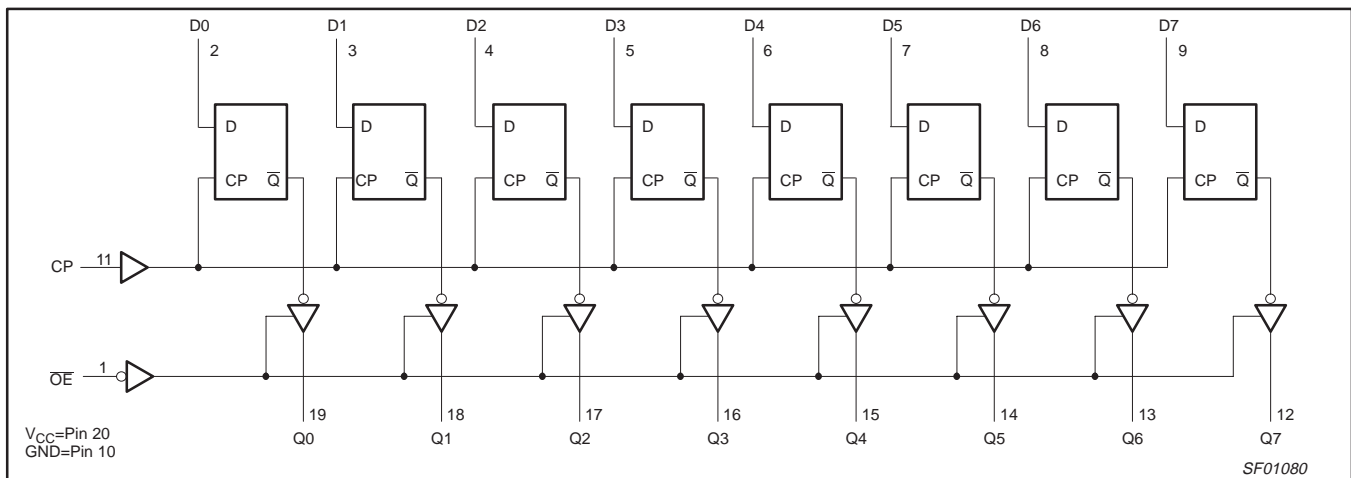


FUNCTION TABLE – 74F573

| INPUTS | | | INTERNAL REGISTER | OUTPUTS | OPERATING MODES |
|--------|---|----|-------------------|---------|-------------------------|
| OE | E | Dn | | Q0 – Q7 | |
| L | H | L | L | L | Load and read register |
| L | H | H | H | H | |
| L | ↓ | l | L | L | Latch and read register |
| L | ↓ | h | H | H | |
| L | L | X | NC | NC | Hold |
| H | L | X | NC | Z | Disable outputs |
| H | H | Dn | Dn | Z | |

- H = High voltage level
- h = High voltage level one setup time prior to the High-to-Low E transition
- L = Low voltage level
- l = Low voltage level one setup time prior to the High-to-Low E transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↓ = High-to-Low E transition

LOGIC DIAGRAM – 74F574



Latch/flip-flop

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FUNCTION TABLE – 74F574

| INPUTS | | | INTERNAL REGISTER | OUTPUTS | OPERATING MODES |
|--------|----|----|-------------------|---------|------------------------|
| OE | CP | Dn | | Q0 – Q7 | |
| L | ↑ | l | L | L | Load and read register |
| L | ↑ | h | H | H | |
| L | ↑̂ | X | NC | NC | Hold |
| H | ↑ | Dn | Dn | Z | Disable outputs |

H = High voltage level

h = High voltage level one setup time prior to the Low-to-High clock transition

L = Low voltage level

l = Low voltage level one setup time prior to the Low-to-High clock transition

NC= No change

X = Don't care

Z = High impedance "off" state

↑ = Low-to-High clock transition

↑̂ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.)

Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--|--------------------------|------|
| V _{CC} | Supply voltage | -0.5 to +7.0 | V |
| V _{IN} | Input voltage | -0.5 to +7.0 | V |
| I _{IN} | Input current | -30 to +5.0 | mA |
| V _{OUT} | Voltage applied to output in High output state | -0.5 to +V _{CC} | V |
| I _{OUT} | Current applied to output in Low output state | 48 | mA |
| T _{amb} | Operating free-air temperature range | 0 to +70 | °C |
| T _{stg} | Storage temperature | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|------------------|--------------------------------------|--------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{IK} | Input clamp current | | | -18 | mA |
| I _{OH} | High-level output current | | | -3 | mA |
| I _{OL} | Low-level output current | | | 24 | mA |
| T _{amb} | Operating free-air temperature range | 0 | | 70 | °C |

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS ^{NO TAG} | | LIMITS | | | UNIT |
|------------------|--|-------------------|---|-----------------------|--------|---------------|------|------|
| | | | | | MIN | TYP NO TAG | MAX | |
| V _{OH} | High-level output voltage | | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX | ±10%V _{CC} | 2.4 | | | V |
| | | | | ±5%V _{CC} | 2.7 | 3.4 | | V |
| V _{OL} | Low-level output voltage | | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX | ±10%V _{CC} | | 0.35 | 0.50 | V |
| | | | | ±5%V _{CC} | | 0.35 | 0.50 | V |
| V _{IK} | Input clamp voltage | | V _{CC} = MIN, I _I = I _{IK} | | | -0.73 | -1.2 | V |
| I _I | Input current at maximum input voltage | | V _{CC} = MAX, V _I = 7.0V | | | | 100 | μA |
| I _{IH} | High-level input current | | V _{CC} = MAX, V _I = 2.7V | | | | 20 | μA |
| I _{IL} | Low-level input current | | V _{CC} = MAX, V _I = 0.5V | | | | -0.6 | mA |
| I _{OZH} | Off-state output current, High-level voltage applied | | V _{CC} = MAX, V _O = 2.7V | | | | 50 | μA |
| I _{OZL} | Off-state output current, Low-level voltage applied | | V _{CC} = MAX, V _O = 0.5V | | | | -50 | μA |
| I _{OS} | Short-circuit output current ^{NO TAG} | | V _{CC} = MAX | | -60 | | -150 | mA |
| I _{CC} | Supply current (total) | I _{CCH} | 74F573 | V _{CC} = MAX | | 30 | 40 | mA |
| | | I _{CCCL} | | | | 35 | 50 | mA |
| | | I _{CCZ} | | | | 40 | 60 | mA |
| | | I _{CCH} | 74F574 | | | 45 | 65 | mA |
| | | I _{CCCL} | | | | 50 | 70 | mA |
| | | I _{CCZ} | | | | 55 | 85 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | | TEST CONDITIONS | LIMITS | | | | | UNIT |
|--------------------------------------|---|--------|--|---|------------|-------------|--|-------------|------|
| | | | | T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω | | | T _{amb} = 0°C to +70°C V _{CC} = +5V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t _{PLH} t _{PHL} | Propagation delay Dn to Qn | 74F573 | Waveform NO TAG | 3.0 1.0 | 5.5 3.5 | 8.0 6.0 | 2.5 1.0 | 9.0 7.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay E to Qn | | Waveform NO TAG | 4.5 3.0 | 8.5 5.0 | 11.5 7.0 | 4.0 2.5 | 12.5 8.0 | ns |
| t _{PZH} t _{PZL} | Output Enable time to High or Low level | | Waveform NO TAG Waveform NO TAG | 2.5 2.5 | 5.5 5.5 | 9.5 8.0 | 2.0 2.0 | 10.5 8.5 | ns |
| t _{PHZ} t _{PLZ} | Output Disable time from High or Low level | | Waveform NO TAG Waveform NO TAG | 1.0 1.0 | 3.0 2.5 | 6.0 5.5 | 1.0 1.0 | 6.5 5.5 | ns |
| f _{MAX} | Maximum Clock frequency | 74F574 | Waveform NO TAG | 160 | 180 | | 150 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CP to Qn | | Waveform NO TAG | 3.5 3.5 | 5.0 5.0 | 7.5 7.5 | 3.0 3.0 | 8.0 8.0 | ns |
| t _{PZH} t _{PZL} | Output Enable time to High or Low level | | Waveform NO TAG Waveform NO TAG | 2.5 3.0 | 4.5 5.0 | 7.5 8.0 | 2.0 3.0 | 7.5 8.5 | ns |
| t _{PHZ} t _{PLZ} | Output Disable time from High or Low level | | Waveform NO TAG Waveform NO TAG | 1.0 1.0 | 3.0 2.5 | 5.5 5.5 | 1.0 1.0 | 6.0 6.0 | ns |

AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | | TEST CONDITIONS | LIMITS | | | | | UNIT |
|--|--------------------------------|--------|-----------------|---|-----|-----|--|-----|------|
| | | | | T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω | | | T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t _s (H) t _s (L) | Setup time, Dn to E | 74F573 | Waveform 4 | 0.0 1.5 | | | 0.0 2.0 | | ns |
| t _h (H) t _h (L) | Hold time, Dn to E | | Waveform 4 | 2.5 4.0 | | | 2.5 4.0 | | ns |
| t _w (H) | E pulse width, High | | Waveform NO TAG | 3.0 | | | 3.5 | | ns |
| t _s (H) t _s (L) | Setup time, Dn to CP | 74F574 | Waveform NO TAG | 2.5 2.5 | | | 3.0 3.0 | | ns |
| t _h (H) t _h (L) | Hold time, Dn to CP | | Waveform NO TAG | 0 0 | | | 0 0 | | ns |
| t _w (H) t _w (L) | CP Pulse width, High or Low | | Waveform NO TAG | 3.0 3.5 | | | 3.0 4.0 | | ns |

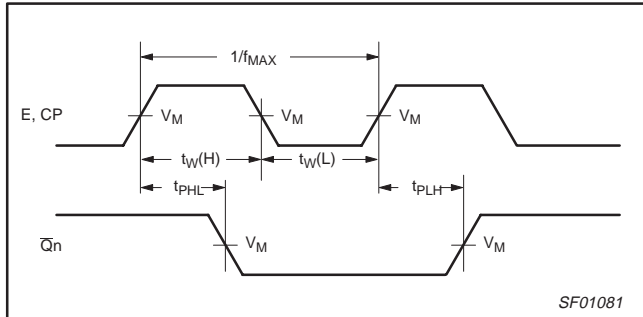
Latch/flip-flop

74F573/74F574

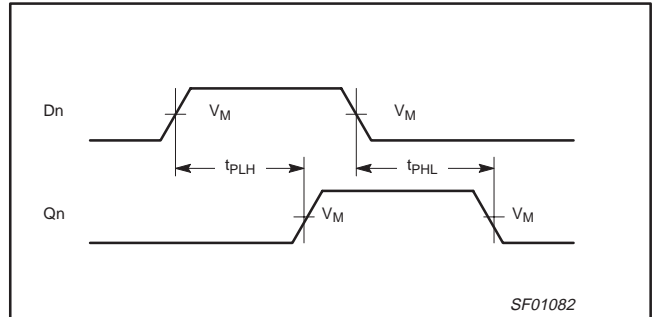
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$

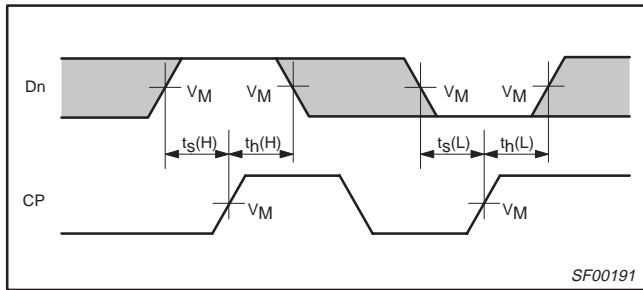
The shaded areas indicate when the input is permitted to change for predictable output performance.



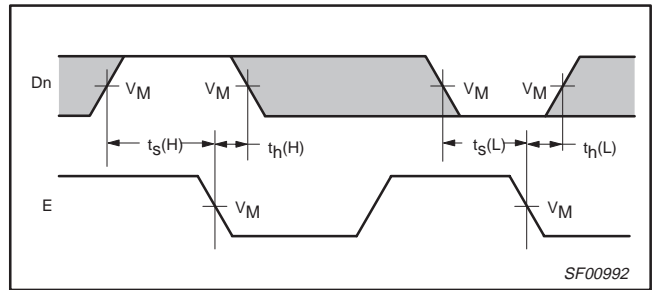
Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency



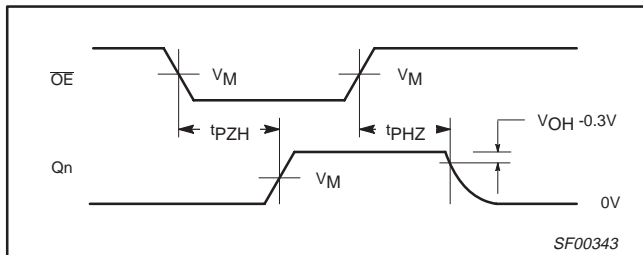
Waveform 2. Propagation Delay for Data to Outputs



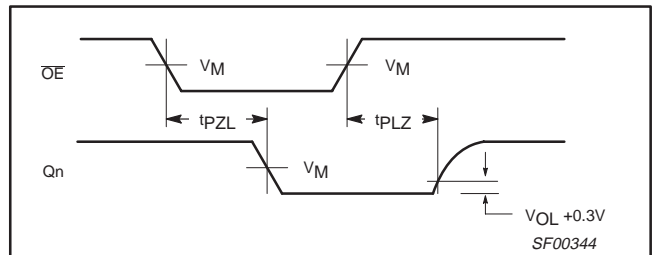
Waveform 3. Data Setup and Hold Times



Waveform 4. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

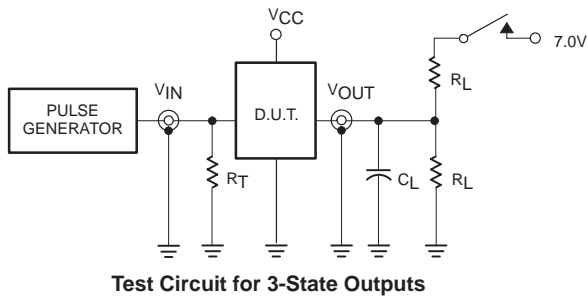


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

Latch/flip-flop

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TEST CIRCUIT AND WAVEFORM



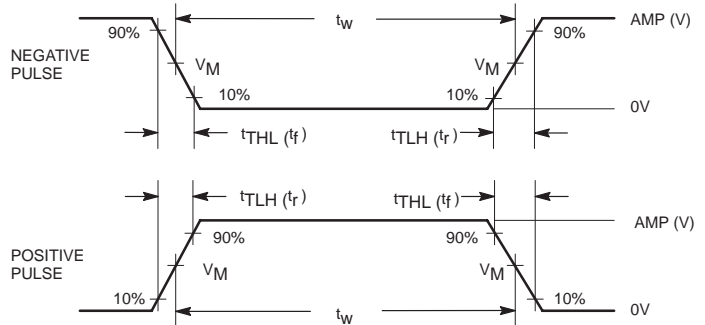
Test Circuit for 3-State Outputs

SWITCH POSITION

| TEST | SWITCH |
|-----------|--------|
| t_{PLZ} | closed |
| t_{PZL} | closed |
| All other | open |

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

| family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
| | amplitude | V_M | rep. rate | t_w | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

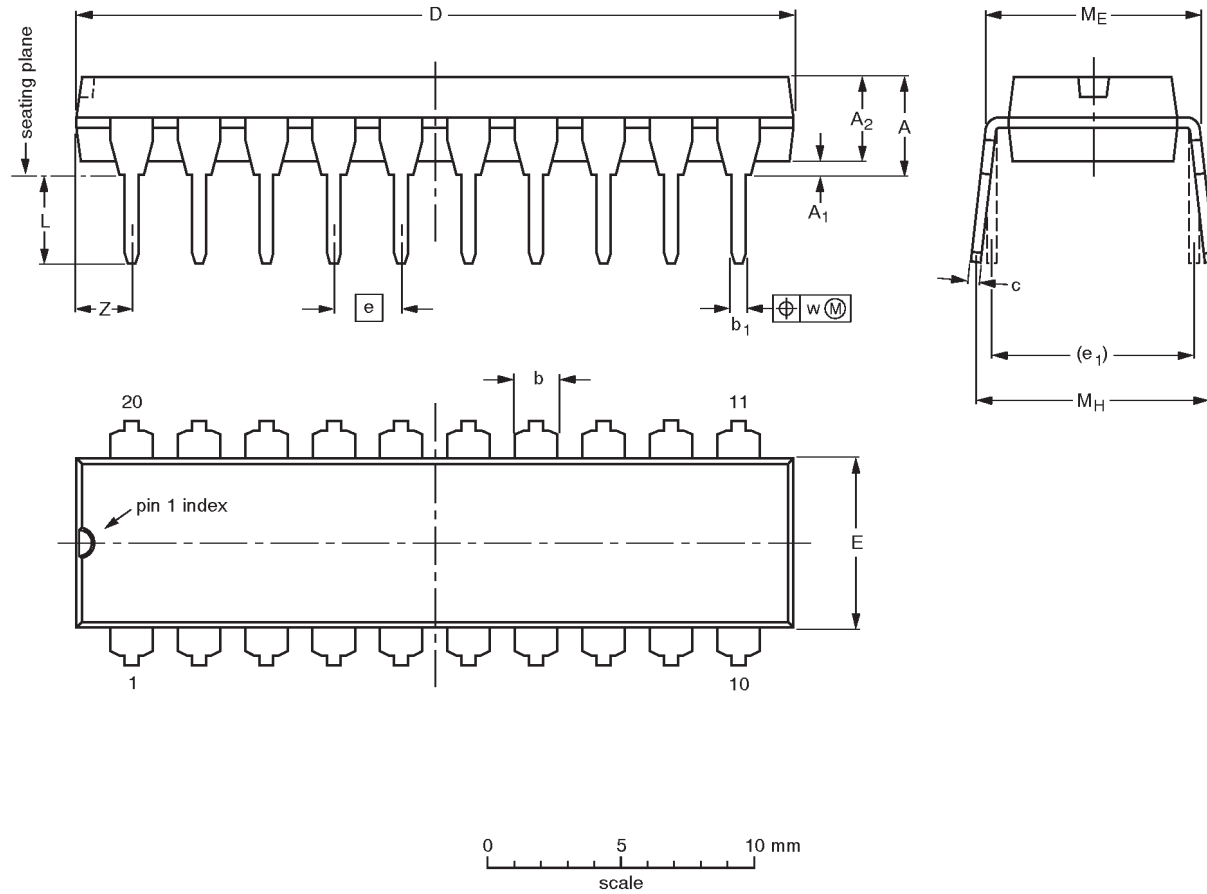
SF00777

Latch/flip-flop

74F573, 74F574

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 0.36 0.23 | 26.92 26.54 | 6.40 6.22 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 2.0 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.014 0.009 | 1.060 1.045 | 0.25 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.078 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

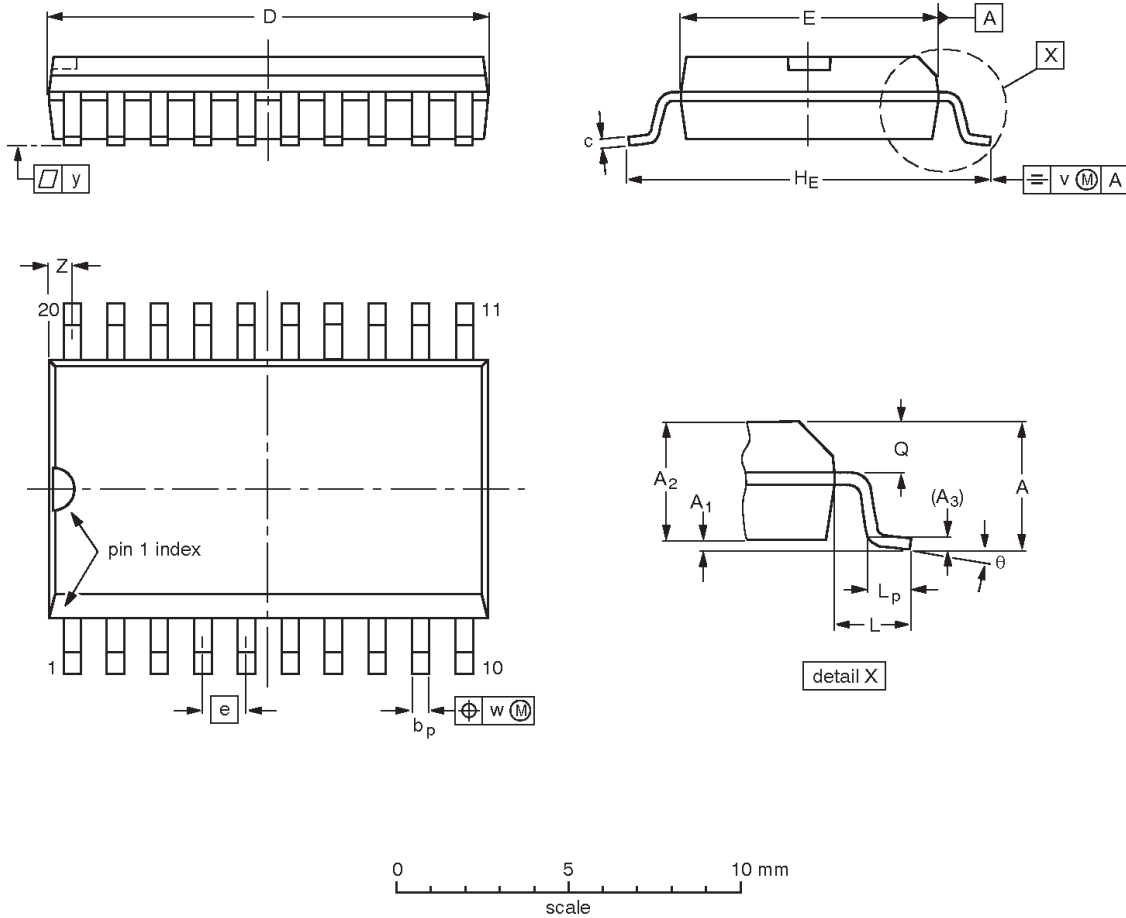
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT146-1 | | | SC603 | | | 92-11-17 95-05-24 |

Latch/flip-flop

74F573, 74F574

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 13.0 12.6 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.51 0.49 | 0.30 0.29 | 0.050 | 0.419 0.394 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

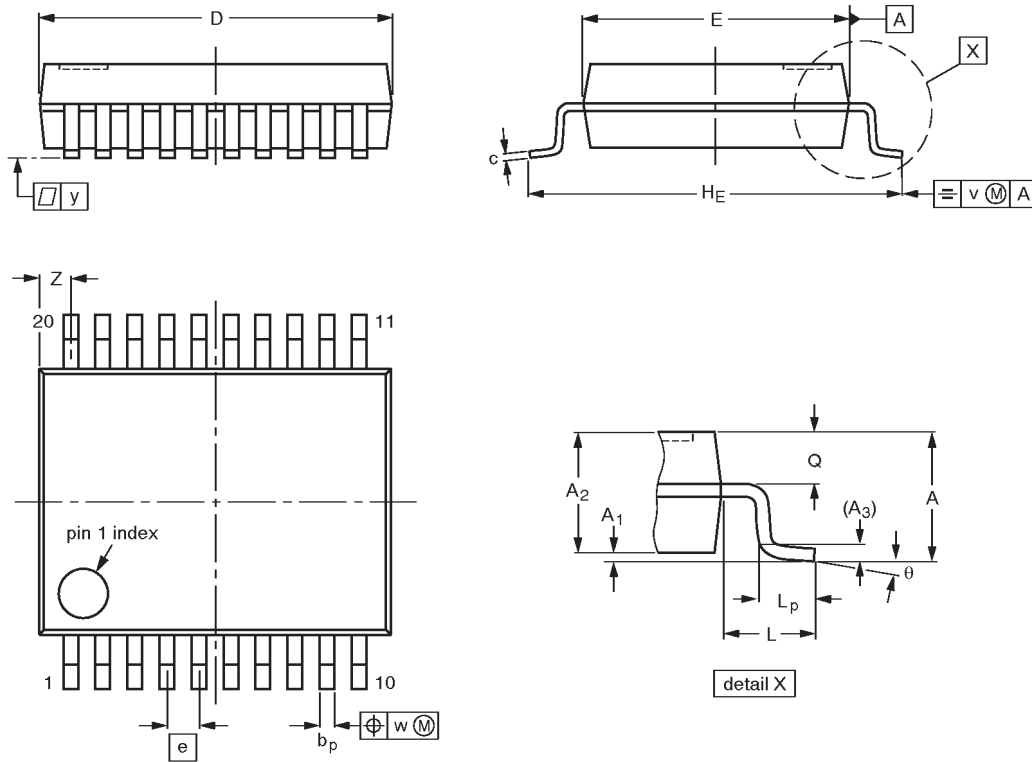
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013AC | | | | 95-01-24 97-05-22 |

Latch/flip-flop

74F573, 74F574

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2.0 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 7.4 7.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 0.9 0.5 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT339-1 | | MO-150AE | | | | 93-09-08 95-02-04 |

Latch/flip-flop

74F573, 74F574

NOTES

Latch/flip-flop

74F573, 74F574

Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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