NX30P6093A

High-voltage I²C controlled OVP load switch with OTG

Rev. 1 — 16 August 2018 Product data sheet

1. General description

The NX30P6093A is a 5.6A I²C controlled overvoltage protection Load switch for USB Type-C and PD applications. It includes undervoltage lockout, overvoltage lockout and overtemperature protection circuits, designed to automatically isolate the power switch terminals when a fault condition occurs. It features input pin impedance detection function, providing USB power supply pin status to system to avoid short circuit damage for the Type-C port power supply pin.

NX30P6093A has a default overvoltage protection threshold, and the OVLO threshold can be adjusted by both external resistor divider on ADJ pin and internal I²C register. A 13ms debounce time is deployed every time before the device is switched ON, followed by a soft start to limit the inrush current.

USB OTG is supported when the plugged accessory is recognized as an OTG device by system and a 5V source is applied on VOUT pin of NX30P6093A. The current capability in USB OTG mode is limited to max 1.5A.

Designed for operation from 2.8V to 20.0V, it can be used in USB Type-C and PD power control applications to offer essential protection and enhance system reliability.

NX30P6093A is offered in a small 20-bump 1.7 x 2.16 mm, 0.4mm pitch WLCSP package.

2. Features and benefits

- Wide supply voltage range for VIN from 2.8V to 20.0V
- System Power supply VDD from 3.0V to 4.5V
- I_{SW} maximum 5.6A continuous current for OVP mode
- Support 1.5A USB OTG
- 29V tolerance on VIN pin
- 16mΩ (typical) ultra-low ON resistance
- Adjustable VIN overvoltage protection by both external resistor and I²C
- Built-in slew rate control for inrush current limit
- Integrated current source for VIN pin impedance detection
- Protection circuitry
  - Overtemperature protection
  - Overvoltage protection
  - Undervoltage lockout

- Surge protection:
  - IEC61000-4-5 exceeds ±100V on VIN
- ESD protection
  - IEC61000-4-2 contact discharge exceeds 8kV on VIN
  - IEC61000-4-2 air discharge exceeds 15kV on VIN
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3kV on all pins
  - MM Class B exceeds 100 V on all the pins
- Specified from -40 °C to +85 °C

3. Applications

- Smart and feature phones
- Tablets, eBooks
- Notebook

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX30P6093AUK	–40 °C to +85 °C	WLCSP20	wafer level chip-scale package; 20 bumps; 1.70 mm x 2.16 mm x 0.525 mm body (backside coating included)	SOT1397-6

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX30P6093AUK	NX30P6093AUKZ	WLCSP20	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	4000	T_{amb} = –40 °C to +85 °C

5. Marking

Table 3. Marking

Line	Marking	Description
1	X30AP2	basic type name

Table 3. Marking *…continued*

Line	Marking	Description
2	mmmmmnn	wafer lot code (mmmmm) and wafer number (nn)
3	ZAYWW	manufacturing code: Z = foundry location A = assembly location Y = assembly year code WW = assembly week code
4	CCC-RRR	Die X-Y Coordinate

6. Functional diagram

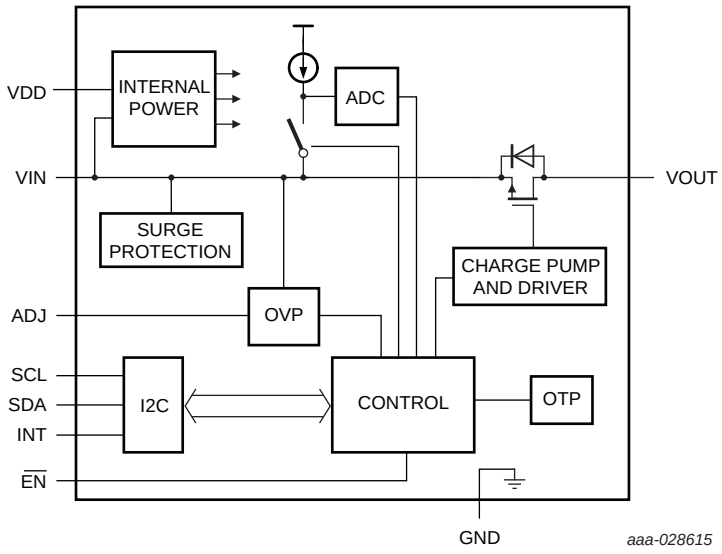


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

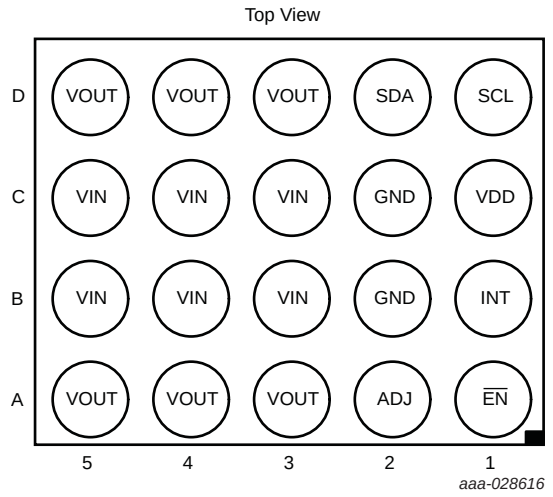


Fig 2. Top view pin map WLCSP20

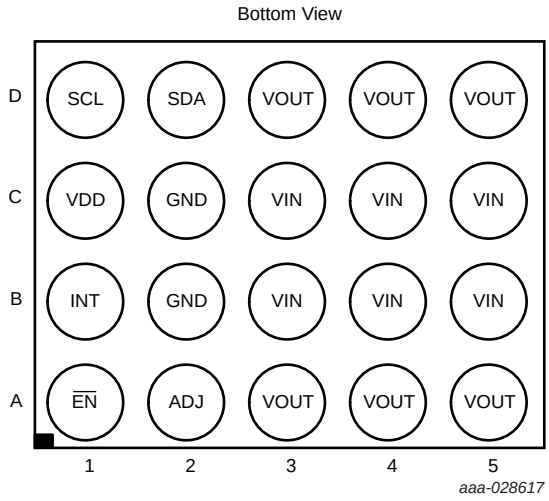


Fig 3. Bottom view pin map WLCSP20

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type	Description
VIN	B3, B4, B5 C3, C4, C5	Power I/O	Power Input pins, these pins should be connected together on PCB
VOUT	A3, A4, A5 D3, D4, D5	Power I/O	Power Input pins, these pins should be connected together on PCB
GND	B2, C2	Ground	Ground pin, these pins should be connected to system ground with good connection for surge protection discharge current
$\overline{EN}$	A1	Input	Enable pin, active low. When it is tied to high, the device enters low power standby mode and VOUT is disconnected from VIN. Internal pull down resistor integrated
INT	B1	Output	I²C-bus interface interrupt to be connected to the I²C-bus master of the host processor
VDD	C1	Power	System Power supply for chip
SDA	D2	I/O	I²C-bus interface serial data to be connected to the I²C-bus master of the host processor
SCL	D1	Input	I²C-bus interface serial clock to be connected to the I²C-bus master of the host processor
ADJ	A2	Input	External OVLO adjust pin. Connect to OVLO resistor divider when select OVLO level by this pin. Connect to ground when it is not used, in this case OVLO determined internally

8. Functional description

NX30P6093A is an integrated device with three major functions: programmable overvoltage protection, VIN pin impedance detection and USB OTG. It protects USB Type-C power supply pin and internal system by isolating high voltage when it is exceeds OVLO threshold. The VIN pin impedance detection provides a status monitoring for system to avoid damage by short circuit of USB Type-C power supply pin.

The impedance detection feature is activated when VIN $<V_{UVLO}$, in this case NX30P6093A supplied by system power VDD. When VIN$>V_{UVLO}$, this feature is disabled automatically.

USB OTG is supported when the plugged accessory is recognized as an OTG device by system and a 5V source is applied on VOUT pin of NX30P6093A.

8.1 $\overline{EN}$ input

A HIGH on $\overline{EN}$ disables the channel MOSFET, all protection circuits, and VIN impedance detection circuits, putting the device into a low power mode. A LOW on $\overline{EN}$ enables the protection circuits and the MOSFET. There is an internal 1 MΩ pull-down resistor on the $\overline{EN}$ pin to ensure the power switch conducting in a dead-battery situation. A 13ms debounce time has been deployed before device turning on.

8.2 OTG Mode

USB OTG is supported when the plugged accessory is recognized as an OTG device by system and a 5V source is applied on VOUT pin of NX30P6093A. The $\overline{EN}$ pin and VOUT_EN bit in register 0x01 must to be set LOW to support USB OTG mode. If $\overline{EN}$ pin or VOUT_EN bit is HIGH, the current is conducted by body diode that will induce much higher power dissipation due to body diode forward voltage and more heating in NX30P6093A. The overtemperature protection will not disable the main switch for the same reason, but only report interrupt to system. In this case, the system should turn off the power source of USB OTG to protect the device and system.

8.3 Slew Rate Tune

The slew rate control is integrated to avoid inrush current when the load switch turns on. It protects the internal circuits or blocks follow NX30P6093A. In order to increase the design flexibility on system level, the slew rate can be tuned through I²C through register 0x0F as follows:

Table 5. Slew rate tune setting by I²C register

Register Value SRT[2:0]	Switch turn on slew rate (TYP)
000	0.42ms
001	0.44ms
010	0.5ms
011	0.65ms
100	0.9ms (Default)
101	1.5ms
110	2.8ms
111	5.6ms

8.4 Undervoltage lockout

When $\overline{EN}$ is LOW and VIN < V_{UVLO}, the Undervoltage Lockout (UVLO) circuit disables the power MOSFET. Once VIN exceeds V_{UVLO}, if no other protection circuit is active and $\overline{EN}$ is LOW, the MOSFET is turned on automatically regardless of the status of VOUT_EN in register 0x01h. If $\overline{EN}$ is HIGH, the MOSFET remains at off and at low power mode.

8.5 Overvoltage lockout

When $\overline{EN}$ is LOW and VIN > V_{OVLO}, the overvoltage lockout (OVLO) circuit disables the power MOSFET. The OV_FLG in register 0x03h is set as “1” and an interrupt is issued to notify the host. Once VIN drops below V_{OVLO} and no other protection circuit is active, the power MOSFET resumes operation.

The OVLO feature can be adjusted by both external resistor divider with ADJ pin and internal I²C register. The sequences are:

- When NX30P6093A is powering up, the initial OVLO threshold is set by ADJ pin. If there is a resistor divider connected to ADJ pin, the OVLO threshold is set by resistor divider value. If ADJ is floating or pull to ground, the OVLO threshold is set by default value in Table 6.
- After power up, the OVLO threshold can be adjusted by system through the I²C register 0x05h according to the flow chart in Figure 4.

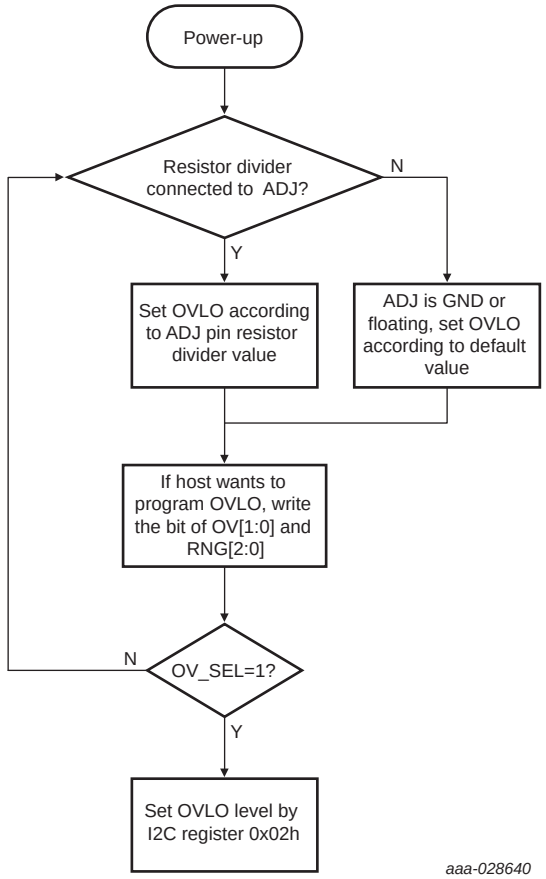


Fig 4. OVLO setting flow chart

When the overvoltage threshold is set by the ADJ pin with the connected resistor divider (see Figure 7), the overvoltage threshold is adjustable from 4V to 23V with below equation

$$Vovlo = Vth(ovlo) \times (R1 + R2)/(R2) \quad (1)$$

If the voltage on ADJ pin is below 0.1V, the device uses internal default OVLO threshold.

When the overvoltage threshold is set by system through I²C-bus, it is set by bit0 and bit1 of register 0x05h. The OVLO thresholds are shown in Table 6.

Table 6. OVLO threshold setting by I²C register

Register Value OV[1:0]	OVLO Threshold
00	6.8V (default)
01	11.5V
10	17V
11	23V

In additional, NX30P6093A provides two additional OVLO thresholds by bit0, bit1 of register 0x0Eh. The additional OVLO thresholds are shown in Table 7.

Table 7. Additional OVLO threshold setting by I²C register

Register Value AOVP[1:0]	OVLO Threshold
00	OVLO set by Table 6.
01	OVLO set by Table 6.
10	10V
11	14V

Furthermore when the OVLO threshold is set by I²C register, it can be fine tuned by bit6-bit4 of register 0x05h. The fine tune values are shown in Table 8.

Table 8. OVLO threshold fine tune setting by I²C register

Register Value RNG[2:0]	OVLO Threshold Fine Tune value
000	-600mV
001	-400mV
010	-200mV
011	0mV (default)
100	+200mV
101	+400mV
110	+600mV
111	+800mV

8.6 Overtemperature protection

When $\overline{EN}$ is LOW and the device temperature exceeds 140 °C the Overtemperature protection (OTP) circuit disables the power MOSFET and an interrupt is issued by setting OT_FLG as “1” in register 0x03h. Once the device temperature decreases below 120 °C and no other protection circuit is active, the state of the N-channel MOSFET is controlled by the $\overline{EN}$ pin again.

8.7 Short circuit protection

NX30P6093A has short circuit protection; after the MOSFET is fully turned on and when the current through it exceeds 10.5A typically, it turns the MOSFET off to protect the device and system. An interrupt is issued when short circuit protection is triggered by setting OC_FLG as “1” in register 0x03h. Once the short circuit condition is removed and no other protection circuit is active, the state of the N-channel MOSFET is controlled by the $\overline{EN}$ pin again.

8.8 VIN impedance detection

An VIN impedance detection function is integrated in NX30P6093A. When $\overline{EN}$ is LOW and VIN $<V_{UVLO}$, NX30P6093A enters VIN detection sleep mode. The host can start the VIN impedance detection according to the following sequences. First, the host can write DETC_EN bit to “1” through I²C, activating NX30P6093A to VIN detection standby mode. In this mode, NX30P6093A turns on internal function circuits and is ready to run detection. After a wake up time t_{WAKEUP}, the host can configure t_{DET}, t_{DUTY} and Tag voltage by writing the register 0x07h and 0x09h through I²C. When I_{source} is changed from default 0μA to any of valid current values in Table 8, NX30P6093A starts the VIN detection according to configured t_{DET} and t_{DUTY} time.

In any of VIN detection modes, while a VIN is plugged and the voltage on VIN pin exceeds V_{UVLO}, NX30P6093A will exit from VIN detection modes to OVP operation modes immediately.

When the VIN detection ADC result is valid after t_{DET} timer out, the TMR_OUT_STS is set to “1” and an interrupt is issued. The host can read the VIN detection voltage at register 0x08h by then. Meanwhile, NX30P6093A can compare the detection result versus the host set VIN TAG voltage in register 0x09h. When the detected voltage is less than the set VIN TAG voltage, the OVER_TAG_STS is set to “1” in register 0x02h and an interrupt is issued.

The VIN pin impedance can be the following two different cases according to the application in system,

- When there is no resistor divider connected to VIN and ADJ pins, the measured impedance (RM) is VIN impedance (RP).
- When an OVLO resistor divider is connected to VIN and ADJ pins, the measured impedance (RM) is VIN impedance (RP) parallels with external OVLO resistor divider R1+R2, (see Figure 7).

Table 9 shows the current source values, which can be programmed by bit3-bit0 of register 0x06h. Please be note there are several internal circuits connected to VIN pin, for example, Surge protection and UVLO resistor ladder. That generates a leakage current according to different VIN voltage specified in Table 28 as $I_{DET\_LEACKAGE}$. This leakage should be excluded in the resistor calculation of VIN impedance detection.

Table 9. Current source set by I²C register

Register Value ISRC[3:0]	Current source value
0000	0μA (default)
0001	1μA
0010	2μA
0011	3μA
0100	4μA
0101	5μA
0110	10μA
0111	20μA
1000	50μA
1001	100μA
1010	200μA
1011	500μA
1100	1000μA
1101	2000μA
1110	5000μA
1111	10000μA

NX30P6093A turns on the I_{source} according to the following system required timing sequence.

Fig 5. VIN Impedance detection timing sequence

The current source turn on pulse width t_{DET} is set by bit7 - bit4 of register 0x07h as follows.

Table 10. Current source turn-on pulse width setting by I²C register

Register Value TDET[3:0]	I_{source} Turn on Pulse Width (t_{DET})
0000	200µs (default)
0001	400µs
0010	1000µs
0011	2000µs
0100	4000µs
0101	10000µs
0110	20000µs
0111	40000µs
1000	100000µs
1001	200000µs
1010	400000µs
1011	1000000µs
1100	2000000µs
1101	4000000µs
1110	10000000µs
1111	Always on

The detection duty cycle is set by bit3 to bit0 of register 0x07h according to the following table.

Table 11. Detection duty cycle setting by I²C register

Register Value DUTY[3:0]	Detection duty cycle (t_{DUTY})
0000	single pulse (default)
0001	10ms
0010	20ms
0011	50ms
0100	100ms
0101	200ms
0110	500ms
0111	1000ms
1000	2000ms
1001	3000ms
1010	6000ms

Table 11. Detection duty cycle setting by I²C register *...continued*

Register Value DUTY[3:0]	Detection duty cycle (t_{DUTY})
1011	12000ms
1100	30000ms
1101	60000ms
1110	120000ms
1111	300000ms

8.9 Interrupt

NX30P6093A has two types of interrupt. One is the interrupt generated by Flag register 0x03h, which includes the alarms of overvoltage, overtemperature and short circuit. The second type of interrupt is generated by Status register 0x02h. The following is a detailed description of the two interrupts.

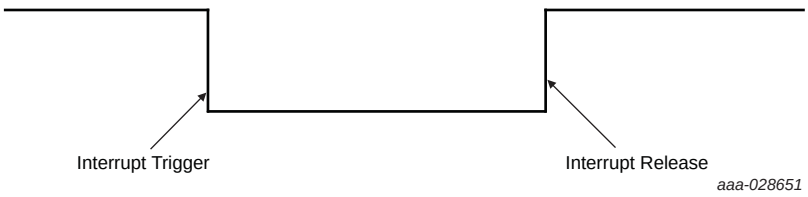


Fig 6. Interrupt triger and release

- The interrupt trigger is by all 3 bits of Flag register (0x03h) and 4 bits of Status register (0x02h) except for OTG_STS. Whenever one of them is changed from “0” to “1”, the interrupt will be triggered. An event will be latched and only the first occurrence triggers an interrupt (if not masked). Reoccurring events will not trigger an additional interrupt.
- The interrupt release of Flag register is by read on clear, t_{DET} timer start, the interrupt status over 1000ms or NX30P6093A disabled by $\overline{EN}$. For OV_FLG and OT_FLG interrupt, if it is not read by host and the fault condition is back to normal in 1000ms, the $\overline{INT}$ will be released. The bit values of the register 0x03h are cleared only by host read or VIN drop below UVLO.
- The interrupt release of Status register is by read on clear, t_{DET} timer start, the interrupt status over 1000ms or NX30P6093A disabled by $\overline{EN}$. The 4 bit values are the real status of the circuit status and will not be cleared when host read them after interrupt.

8.10 I²C-bus interface

NX30P6093A implements I²C-bus slave interface which interfaces with the host system. The host processor can issue commands, monitor status and receive response through this bus. A detailed description of the I²C-bus specification, with applications, is given in *UM10204, “I²C-bus specification and user manual”* . NX30P6093A supports I²C-bus data transfers in both Standard-mode (100 kbit/s), Fast-mode (400 kbit/s) and Fast-mode (2 Mbit/s).

As an exception to the I²C-bus specification, the NX30P6093A does not support the I²C 'General Call' address (and therefore does not issue an Acknowledge), clock stretching, Software Reset command, nor 10-bit address.The various registers, address offsets and bit definitions are shown in Table 12.

The I²C address at Power-On Reset is as follows:

- Write address: 0x6C
- Read address: 0x6D

Table 12. NX30P6093A Register map

Addr	Name	Type	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit
0x00h	Device ID Register	R	-	Vendor ID						Versio
0x01h	Enable Register	R/W	00h	VOUT_EN	DETC_EN	Reserved	Reserved	Reserved	Reserved	Rese
0x02h	Status Register	R	00h	PWRON_STS	OVER_TAG_STS	TMR_OUT_STS	SWON_STS	OTG_STS	Reserved	Rese
0x03h	Flag	C/R	00h	Reserved	Reserved	Reserved	Reserved	Reserved	OV_FLG	OC_I
0x04h	Interrupt Mask	R/W	F7h	PWRON_STS	OVER_TAG_STS	TMR_OUT_STS	SWON_STS	Reserved	OV_FLG	OC_I
0x05h	OVLO Trigger level	R/W	30h	Reserved	RNG2	RNG1	RNG0	OV_SEL	Reserved	OV
0x06h	I_{source} to VIN	R/W	00h	Reserved	Reserved	Reserved	Reserved	ISRC3	ISRC2	ISR
0x07h	I_{source} working time	R/W	00h	TDET3	TDET2	TDET1	TDET0	DUTY3	DUTY2	DUT
0x08h	Voltage to VIN	R	00h	VIN7	VIN6	VIN5	VIN4	VIN3	VIN2	VIN
0x09h	Set Tag on VIN	R/W	00h	TVIN7	TVIN6	TVIN5	TVIN4	TVIN3	TVIN2	TVI
0x0Ah	Reserved	R/W	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Rese
0x0Bh	Reserved	R/W	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Rese
0x0Ch	Reserved	R/W	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Rese
0x0Dh	Reserved	R/W	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Rese
0x0Eh	Additional OVP	R/W	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AOV
0x0Fh	Slew rate Tune	R/W	04h	Reserved	Reserved	Reserved	Reserved	Reserved	SRT2	SR

8.10.1 Device ID Register (Address 0x00h)

Table 13. Device ID Register

Bit	Name	Type	Reset Value	Description
7:3	Vendor ID	R	00001	NXP Vendor ID 00001
2:0	Version ID	R	001	Device revision number 001

8.10.2 Enable Register (Address 0x01h)

Table 14. Enable Register

Bit	Name	Type	Reset Value	Description
7	VOUT_EN	R/W	0h	0h = Main switch MOSFET turned on
				1h = Main switch MOSFET turned off
6	DETC_EN	R/W	0h	0h = ISOURCE VIN impedance detection turn off
				1h = ISOURCE VIN impedance detection turn on
5:0	Reserved	R/W	0h	0h = default

8.10.3 Status Register (Address 0x02h)

Table 15. Status Register

Bit	Name	Type	Reset Value	Description
7	PWRON_STS	R	0h	0h = VIN voltage less than V_{UVLO}
				1h= VIN voltage larger than V_{UVLO}. An interrupt will be issued
6	OVER_TAG_STS	R	0h	0h = VIN detected voltage larger than Tag voltage
				1h = VIN detected voltage less than Tag voltage. An interrupt will be issued, please refer to Section 8.8 for the details
5	TMR_OUT_STS	R	0h	0h = t_{DET} timer is not out
				1h = t_{DET} timer out. An interrupt will be issued, please refer to Section 8.8 for the details
4	SWON_STS	R	0h	0h = The main switch is turn off
				1h= The main switch is turn on. An interrupt will be issued
3	OTG_STS	R	0h	0h = The device is not in OTG mode
				1h = The device is in OTG mode
3:0	Reserved	R	0h	0h = default

8.10.4 Flag Register (Address 0x03h)

This is the interrupt register, when one of the FLAGs is “1”, the $\overline{INT}$ pin will be pulled LOW. Please refer to Section 8.8.

Table 16. FLAG Register

Bit	Name	Type	Reset Value	Description
7:3	Reserved	C/R	0h	0h = Default
2	OV_FLG	C/R	0h	Overvoltage protection flag
				When overvoltage protection triggered, set this bit as “1”
1	OC_FLG	C/R	0h	Short circuit protection flag
				When short circuit protection triggered, set this bit as “1”
0	OT_FLG	C/R	0h	Over temperature protection flag
				When Over temperature protection triggered, set this bit as “1”

8.10.5 Interrupt Mask Register (Address 0x04h)

This is the register to enable masking of the interrupts of both Flag Register and Status Register.

Table 17. Interrupt Mask Register

Bit	Name	Type	Reset Value	Description
7	PWRON_STS	R/W	1h	0h = mask OVER_TAG_STS interrupt
				1h = Do not mask OVER_TAG_STS interrupt
6	OVER_TAG_STS	R/W	1h	0h = mask OVER_TAG_STS interrupt
				1h = Do not mask OVER_TAG_STS interrupt
5	TMR_OUT_STS	R/W	1h	0h = mask TMR_OUT_STS interrupt
				1h = Do not mask TMR_OUT_STS interrupt
4	SWON_STS	R/W	1h	0h = mask OVER_TAG_STS interrupt
				1h = Do not mask OVER_TAG_STS interrupt
3	Reserved	R/W	0h	0h = Default
2	OV_FLG	R/W	1h	0h = mask OV_FLG interrupt
				1h = Do not mask OV_FLG interrupt
1	OC_FLG	R/W	1h	0h = mask OC_FLG interrupt
				1h = Do not mask OC_FLG interrupt
0	OT_FLG	R/W	1h	0h = mask OT_FLG interrupt
				1h = Do not mask OT_FLG interrupt

8.10.6 OVLO trig level Register (Address 0x05h)

This is the register to set OVLO trig level and also another 2 bits for enable signal.

Table 18. OVLO trig level Register

Bit	Name	Type	Reset Value	Description
7	Reserved	R/W	0h	0h = Default
6:4	RNG[2:0]	R/W	03h	OVLO fine tune bits, please refer to Section 8.5
3	OV_SEL	R/W	0h	0h= OVLO level adjusted by ADJ pin
				1h=OVLO level adjusted by I²C register bit
2	Reserved	R/W	0h	0h = Default
1:0	OV[1:0]	R/W	0h	OVLO threshold set bits, please refer to Section 8.5

8.10.7 I_{source} to VIN Register (Address 0x06h)

This is the register to set I_{source} value for VIN impedance detection, please refer to Section 8.8.

Table 19. I_{source} to VIN Register

Bit	Name	Type	Reset Value	Description
7:4	Reserved	R/W	0h	0h = Default
3:0	ISRC[3:0]	R/W	0h	I_{source} current value setting bits

8.10.8 I_{source} timing Register (Address 0x07h)

This is the register to set I_{source} timing for VIN impedance detection, please refer to Section 8.8.

Table 20. I_{source} timing Register

Bit	Name	Type	Reset Value	Description
7:4	TDET[3:0]	R/W	0h	I_{source} current pulse width setting bits
3:0	DUTY[3:0]	R/W	0h	VIN Impedance detection duty cycle setting bits

8.10.9 Voltage on VIN Register (Address 0x08h)

This is the register to store the VIN voltage detection results from ADC, please refer to Section 8.8.

Table 21. Voltage on VIN Register

Bit	Name	Type	Reset Value	Description
7:0	VIN[7:0]	R	0h	VIN voltage detection results. The detected VIN voltage can be calculated as: $V_{DET} = 2.7 \times \frac{VIN[7:0]}{256}$ Where, VIN[7:0] is decimal value of this register.

8.10.10 Set tag on VIN Register (Address 0x09h)

This is the register to set the tag of VIN voltage in VIN impedance detection, please refer to Section 8.8.

Table 22. Set tag on VIN Register

Bit	Name	Type	Reset Value	Description
7:0	TVIN[7:0]	R/W	00h	Set tag of VIN voltage bits. The TVIN [7:0] can be calculated as: $TVIN = \frac{V_{TAG}}{2.7}$ Where, TVIN is decimal data and should be transfer to binary to TVIN[7:0]

8.10.11 Additional OVP Register (Address 0x0Eh)

This is the register to set additional OVLO trip level; please refer to Section 8.5 for more details.

Table 23. Additional OVP Register

Bit	Name	Type	Reset Value	Description
7:2	Reserved	R/W	00h	00h = Default
1:0	AOVP[1:0]	R/W	00h	Set additional OVLO trip level

8.10.12 Slew rate tune Register (Address 0x0Fh)

This is the register to set the load switch slew rate; please refer to Section 8.3 for more details.

Table 24. Additional OVP Register

Bit	Name	Type	Reset Value	Description
7:3	Reserved	R/W	00h	00h = Default
2:0	SRT[2:0]	R/W	02h	Set slew rate tune

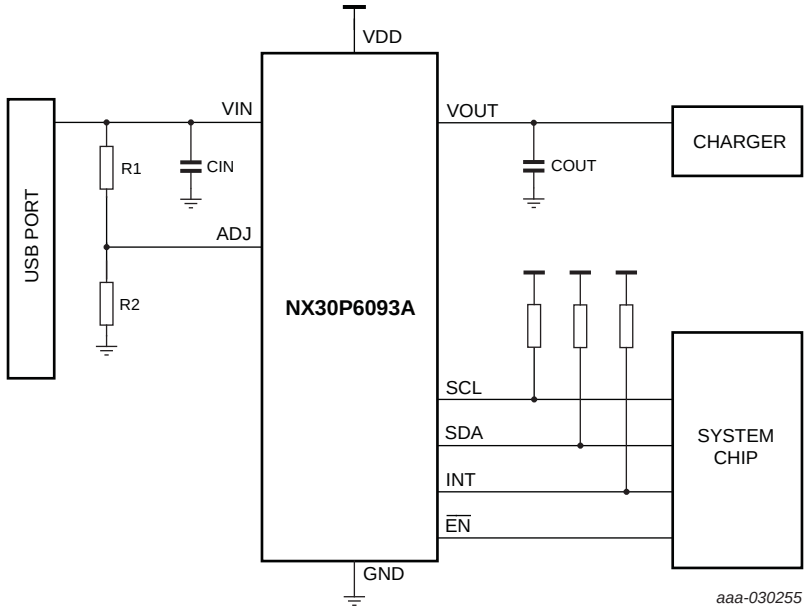
9. Application diagram

The NX30P6093 is typically used on a USB port charging path in a portable, battery operated device. The I²C signals require an external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level that it is connected to.

When the default internal OVLO threshold is used, the ADJ pin shall be shorted to GND. While OVLO threshold is adjusted by ADJ pin, a resister divider shall be connected.

In order to have better VIN pin impedance detection range, it is recommended that the total resistance of R1 and R2 are larger than 1MΩ.

For the best performance, it is recommended to keep input and output trace short and capacitors as close to the device as possible. Regarding the thermal performance, it is recommended to increase the PCB area around VIN and VOUT pins.



R1 and R2 are only needed for adjustable V_{OVLO}; To use default V_{OVLO} threshold, connect OVLO to GND

The recommended resistor value R1+R2 > 1MΩ

C_{IN} and C_{OUT} minimum are recommended to be 1μF

Fig 7. NX30P6093A application diagram

10. Limiting values

Table 25. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VIN	[1]	–2	+29	V
		VDD		–0.3	+7.0	V
		VOUT, as an input pin in OTG mode		–0.3	+7.0	V
		ADJ		–0.3	VIN	V
		$\overline{EN}$	[2]	–0.3	+7.0	V
		SCL, SDA		–0.3	+7.0	V
V_O	output voltage	VOUT, as an output pin in OVP mode		–0.3	+22	V
		$\overline{EN}$		–0.3	+7.0	V
I_{IK}	input clamping current	$\overline{EN}$: V_I < –0.5 V		–50	-	mA
I_{SK}	switch clamping current	VIN; VOUT; V_I < –0.5 V		–50	-	mA
I_{SW}	OVP mode continuous switch current	T_{amb} = 85 °C		-	5.6	A
	OVP mode peak switch current	100μs pulse, 2% duty cycle		-	7	A

Table 25. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
	OTG mode continuous switch current	T_{amb} = 85 °C		-	1.5	A
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation		[3]	-	1.7	W

[1] The -2V limiting value is 200ms non-repetitive pulse

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a 4 layer PCB.

11. Recommended operating conditions

Table 26. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VIN	0	20	V
		VOUT (OTG Mode input voltage)	4.5	5.5	V
		$\overline{EN}$	0	5.5	V
		VDD	3.0	4.5	V
V_O	output voltage	$\overline{INT}$	0	5.5	V
$T_{j(max)}$	maximum junction temperature		–40	+125	°C
T_{amb}	ambient temperature		–40	+85	°C

12. Thermal characteristics

Table 27. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	58.6	K/W

[1] The overall Rth(j-a) can vary depending on the board layout. To minimize the effective Rth(j-a), all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.

[2] Rth(j-a) is calculated based on JEDEX2S2P board. The actual Rth(j-a) value may vary in applications using different layer stacks and layouts.

13. Static characteristics

Table 28. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

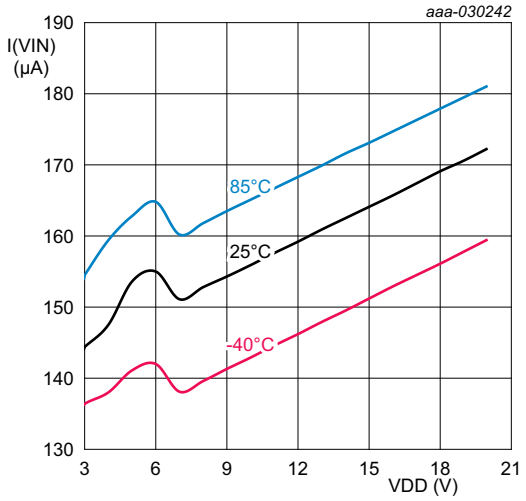
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\overline{EN}$ pin; $V_{I(VIN)}$ = 2.8V to 20V	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	$\overline{EN}$ pin; $V_{I(VIN)}$ = 2.8V to 20V	-	-	0.4	-	0.4	V
I_{EN}	Input leakage current	$\overline{EN}$ pin; $V_{I(\overline{EN})}$=0V	-	0.1	-	-1	1	µA
C_I	input capacitance	$\overline{EN}$ pin; $V_{I(VIN)}$ = 5V	-	5	-	-	-	pF
R_{pd}	pull-down resistance	$\overline{EN}$ pin;	-	1	-	-	-	MΩ
I_q	VIN quiescent current	$\overline{EN}$ = 0 V; $V_{I(VIN)}$ = 5.0 V; I_O = 0 A;	-	150	-	-	200	µA
		$\overline{EN}$ = 5.0 V; $V_{I(VIN)}$ = 5.0 V; I_O = 0 A;	-	1	-	-	3	µA
I_{q_SLEEP}	VDD Sleep mode current	$\overline{EN}$ = 0 V; $V_{I(VIN)}$ <V_{UVLO}; VDD=3.0V; DETC_EN=0	-	12.5	-	-	20.5	µA
I_{q_OTG}	VOUT quiescent current	$\overline{EN}$ = 0 V; $V_{I(VOUT)}$ = 5.0 V; I_O = 0 A;	-	160	-	-	210	µA
$I_{DET\_LEAKAGE}$	VIN Pin leakage in detection mode	$\overline{EN}$ = 0 V; $V_{I(VIN)}$ =1V; DETC_EN=1	-	0.2	-	-	0.5	µA
$I_{S(OFF)}$	VOUT OFF-state leakage current	$\overline{EN}$ = 5.0 V; $V_{I(VIN)}$ = 5.0V; VOUT = 0 V	-	0.5	-	-	2	µA
V_{UVLO}	undervoltage lockout release voltage	VIN Rising; $\overline{EN}$ = 0 V	-	2.65	-	2.5	2.8	V
$V_{hys(UVLO)}$	undervoltage lockout hysteresis voltage	VIN Falling;	-	100	-			mV
I_{OVLO}	ADJ pin input leakage Current	VIN=5V, V_{ADJ}=3V apply after power up	-	3	-	-	6	µA
		VIN=5V, V_{ADJ}=3V apply before power up	-	10	-	-	100	nA
V_{OVLO}	Default overvoltage lockout voltage	VIN Rising; $\overline{EN}$ = 0 V; ADJ short to GND	-	6.8	-	6.6	7.0	V
$V_{hys(OVLO)}$	Overvoltage lockout hysteresis voltage	VIN Falling; $\overline{EN}$ = 0 V; ADJ short to GND	-	2	-	1.3	2.7	%
$V_{th(OVLO)}$	external OVLO set threshold voltage	$V_{I(VIN)}$ = 2.8V to 20V; $\overline{EN}$ = 0 V	-	1.204	-	1.175	1.224	V
I²C-bus Interface Specifications								
V_{IH}	HIGH-level input voltage	SCL, SDA; VDD= 3.0V to 4.5V	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	SCL, SDA; VDD= 3.0V to 4.5V	-	-	0.4	-	0.4	V
V_{OL}	LOW-level output voltage	$\overline{INT}$ pin; VDD= 3.0V to 4.5V; I_{load} = 1mA	-	-	0.3	-	0.3	V

Table 28. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
f_{CLK_I2C}	I²C-bus clock frequency		0	-	1	0	1	MHz
I_{SOURCE} ADC Specifications								
I_{SOURCE}_ACC	Current source accuracy	VDD= 3.0V to 4.5V	-	-	5	-	5	%
V_{ADC}	ADC input voltage range	VDD= 3.0V to 4.5V	0		2.5	0	2.5	V
V_{ADC}	ADC reference voltage	VDD= 3.0V to 4.5V	-	2.7	-	2.64	2.76	V
Resolution	ADC bits	VDD= 3.0V to 4.5V	-	8	-	-	-	bit
Thermal Protection								
$T_{th(otp)}$	over temperature shutdown threshold temperature	VIN=2.8V to 20V	-	140	-	-	-	°C
$T_{th(otp)hys}$	hysteresis of over temperature protection threshold temperature	VIN=2.8V to 20V	-	25	-	-	-	°C

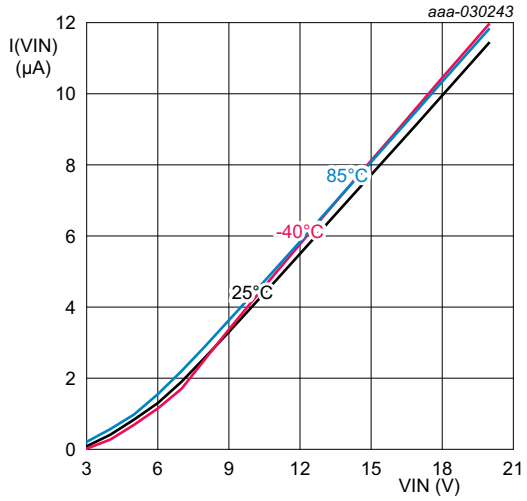
13.1 Graphs



$\overline{EN}$ = 0V; I_O = 0 A

(1) T_{amb} = +25 °C.

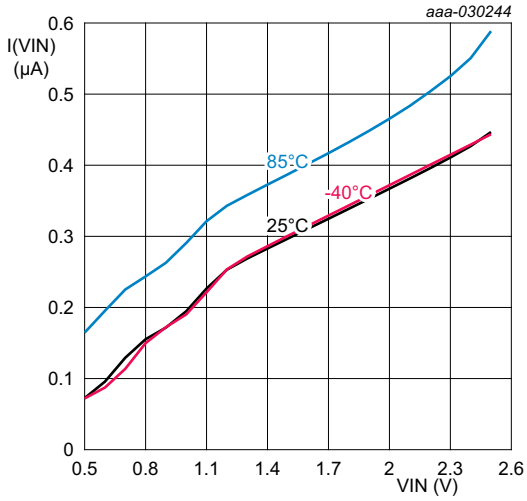
Fig 8. On-state quiescent current versus input voltage



$\overline{EN}$ = 5V; I_O = 0 A

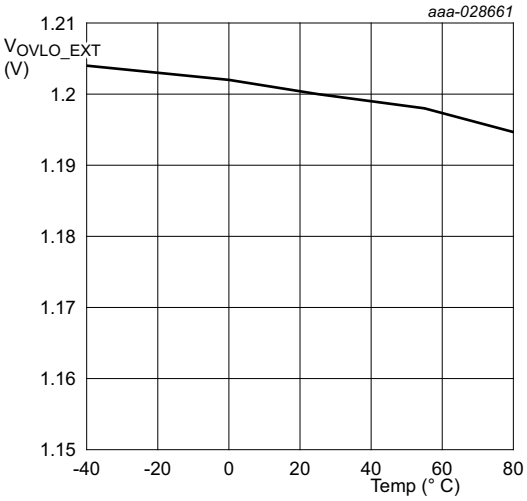
(1) T_{amb} = +25 °C.

Fig 9. OFF-state quiescent current versus input voltage



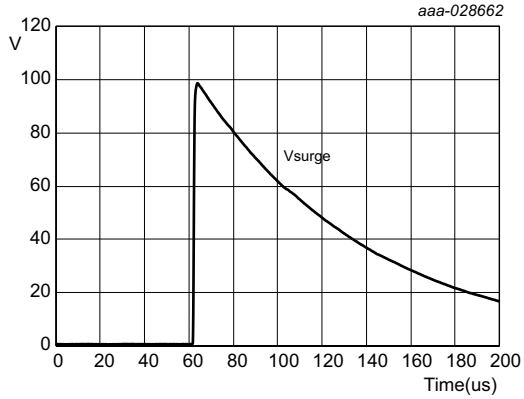
$\overline{EN}$ = 0V; VDD=3.0V; DETC_EN=1

Fig 10. VIN pin leakage current in detection mode versus VIN voltage



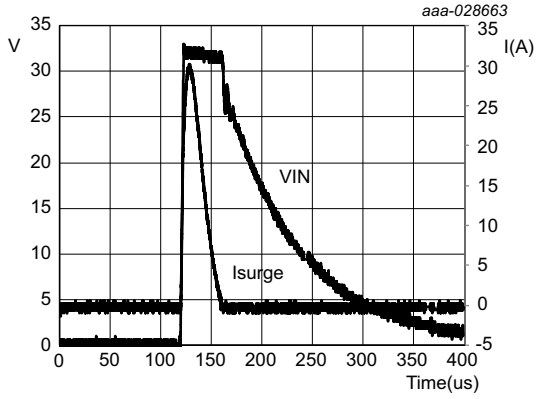
$\overline{EN}$ = 0V; $V_{I(VIN)}$ = 5V;

Fig 11. External OVLO set threshold versus temperature



IEC61000-4-5 100V

Fig 12. 100V surge voltage without device



$\overline{EN}$ = 0V; OVLO short to GND; no capacitor on VIN

(1) $I_{I(VIN)}$

(2) $V_{I(VIN)}$

(3) $V_{O(VOUT)}$

Fig 13. 100V surge with device

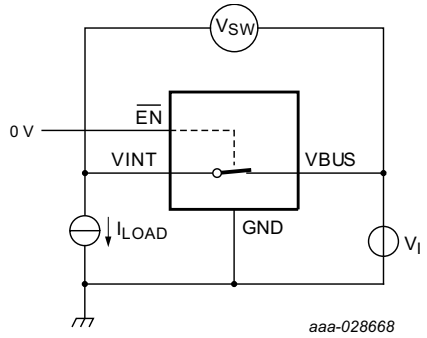
13.2 ON resistance

Table 29. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	I_{LOAD} = 1 A							
		$V_{I(VIN)}$ = 5.0 V		-	15.5	20	-	25	mΩ
		$V_{I(VIN)}$ = 20 V		-	15.5	20	-	25	mΩ

13.3 ON resistance test circuit and graphs



$R_{ON} = V_{SW}/I_{LOAD}$

Fig 14. Test circuit for measuring ON resistance

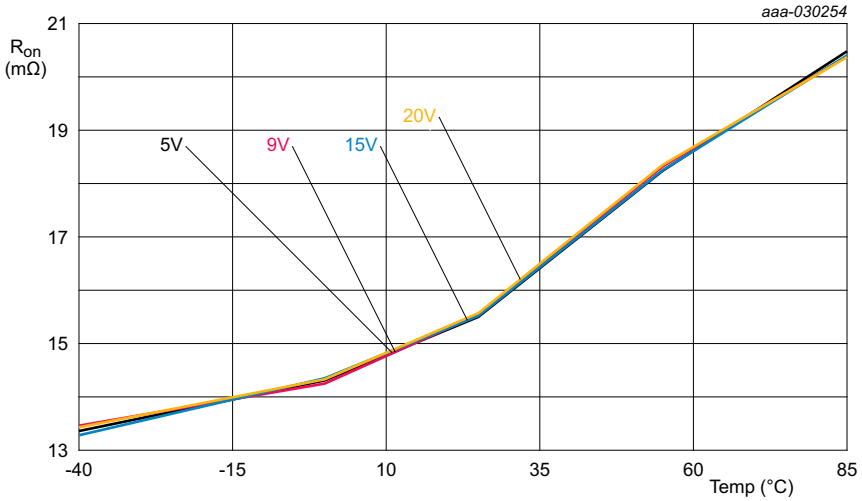


Fig 15. ON resistance versus temperature

14. Dynamic characteristics

Table 30. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 17.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{en}	Enable Time	From $\overline{EN}$ to $V_{(VOUT)}$ = 10 % of $V_{(VIN)}$; (Including debounce time); $V_{I(VIN)}$ = 5 V; C_{Load} = 22 µF; R_{Load} = 100 Ω	-	15	-	10	20	ms
t_{TLH}	VOUT rise time	$V_{(VOUT)}$ from 10 % to 90 % $V_{(VIN)}$; C_{Load} = 22 µF; R_{Load} = 100 Ω						
		$V_{I(VIN)}$ = 5 V	-	0.9	-	-	2	ms
		$V_{I(VIN)}$ = 20 V	-	1.8	-	-	3	ms
$t_{dis(OVP)}$	OVLO turn off time	From $V_{(VIN)}$>V_{OVLO} to $V_{(VOUT)}$ = 80 % of $V_{(VIN)}$; R_{load} = 100 Ω,; C_{load} = 0 µF; $V_{I(VIN)}$ = 20 V; ADJ pin short to GND; VIN rise >2 V/us	-	30	-	-	100	ns
t_{start}	VIN start time	$\overline{EN}$ = 0; from VIN > V_{UVLO} to $V_{(VOUT)}$ = 10 % of $V_{(VIN)}$	-	15	-	10	20	ms
t_{dis}	Disable time	From $\overline{EN}$ to $V_{(VOUT)}$ = 90 % of $V_{(VIN)}$; $V_{I(VIN)}$ = 5 V; C_{Load} = 0 µF; R_{Load} = 100 Ω	-	0.2	-	0.1	0.5	µs
t_{DEB}	Debounce time	Time from V_{UVLO} < VIN < V_{OVLO} to $V_{(VOUT)}$ = 10 % of $V_{(VIN)}$	-	13.5	-	-	-	ms
t_{WAKEUP}[1]	Sleep to VIN detection wake up time	Time from DETC_EN = 1 to device ready for VIN impedance detection	-	1.5	3	-	3	ms
t_{SCP}	Short circuit protection response time	VIN=5 V; Time from short circuit happened to switch turn off	-	3	-	-	-	µs
$t_{VINDISCHARGE}$	Time taken for VIN discharge	VDD = 3.3 V; Load Capacitance = 10 µF VBUS pin going down below Vsafe0V after VBUS detached and switch disabled	-	-	-	-	650	ms
		VDD = 3.3 V; Load Capacitance = 10 µF VBUS pin going down below Vsafe5V (when initial voltage is >5 V) after VBUS detached and switch disabled	-	-	-	-	275	ms

[1] Guaranteed by design

Table 31. I²C-bus interface timing requirements

At recommended operating conditions; T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
f_{SCL}	I²C SCL clock frequency		0	100	0	1000	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{SP}	pulse width of spikes that will be suppressed by the input filter		-	50	-	50	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20+0.1C_b$ [1]	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20+0.1C_b$ [1]	300	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	µs
$t_{VD;DAT}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA LOW	-	3.45	-	0.9	µs

[1] C_b = total capacitance of one bus line in pF.

14.1 Waveforms and test circuit

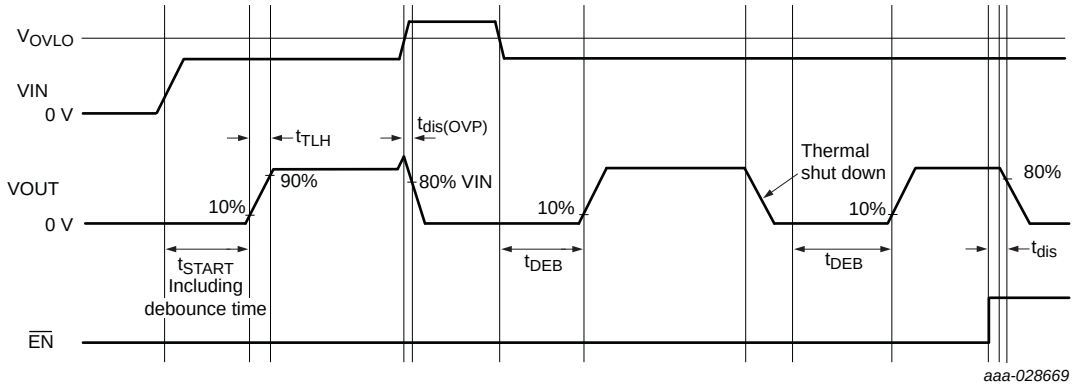
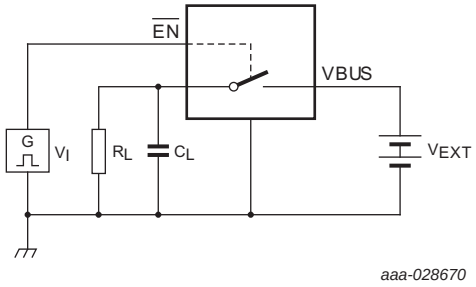


Fig 16. Timing diagram



Test Condition is given in Table 32

R_L = Load resistance.

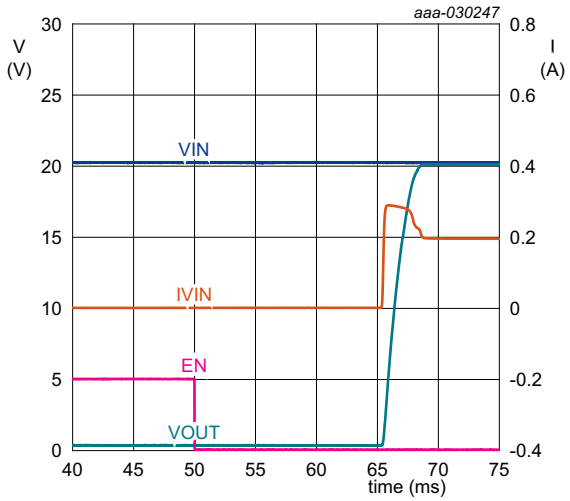
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 17. Test circuit for measuring switching times

Table 32. Test Condition

Supply voltage V_{EXT}	Load	
VIN	**C_L**	**R_L**
2.8 V to 20V	22 µF	100 Ω



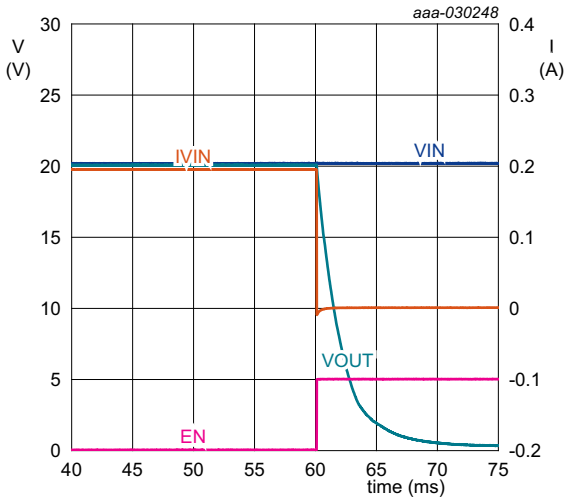
$V_{I(VIN)}$ = 20.0 V; R_L = 100 Ω; C_L = 22µF

(1) VOUT

(2) $\overline{EN}$

(3) $I_{I(VIN)}$

Fig 18. Turn-on time and in-rush current at 20V



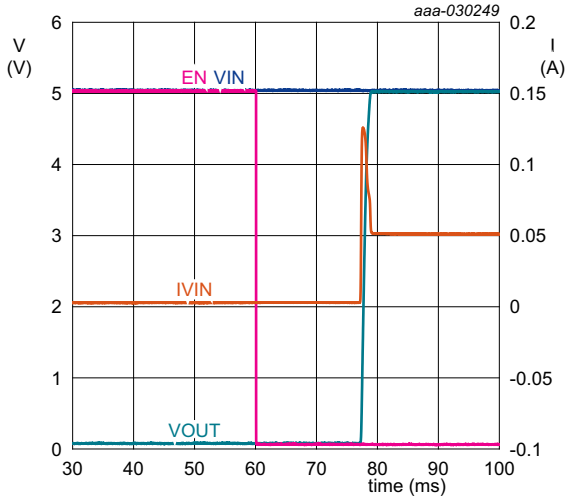
$V_{I(VIN)}$ = 20.0 V; R_L = 100 Ω; C_L = 22µF

(1) VOUT

(2) $\overline{EN}$

(3) $I_{I(VIN)}$

Fig 19. Turn-off time at 20V



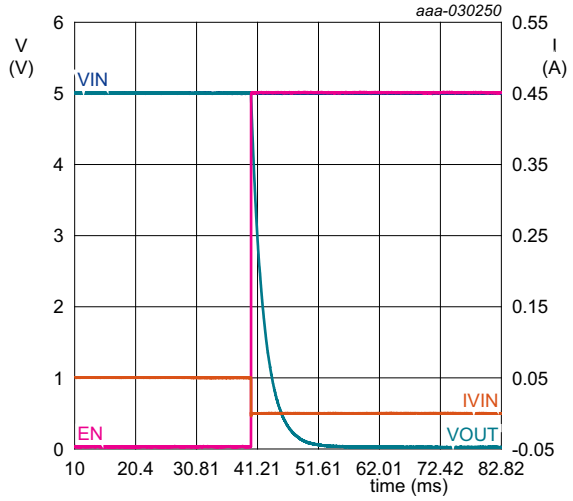
$V_{I(VIN)}$ = 5V; R_L = 100 Ω; C_L = 22 µF

(1) VOUT

(2) $\overline{EN}$

(3) $I_{I(VIN)}$

Fig 20. Turn-on time and in-rush current at 5V



$V_{I(VIN)}$ = 5V; R_L = 100 Ω; C_L = 22 µF

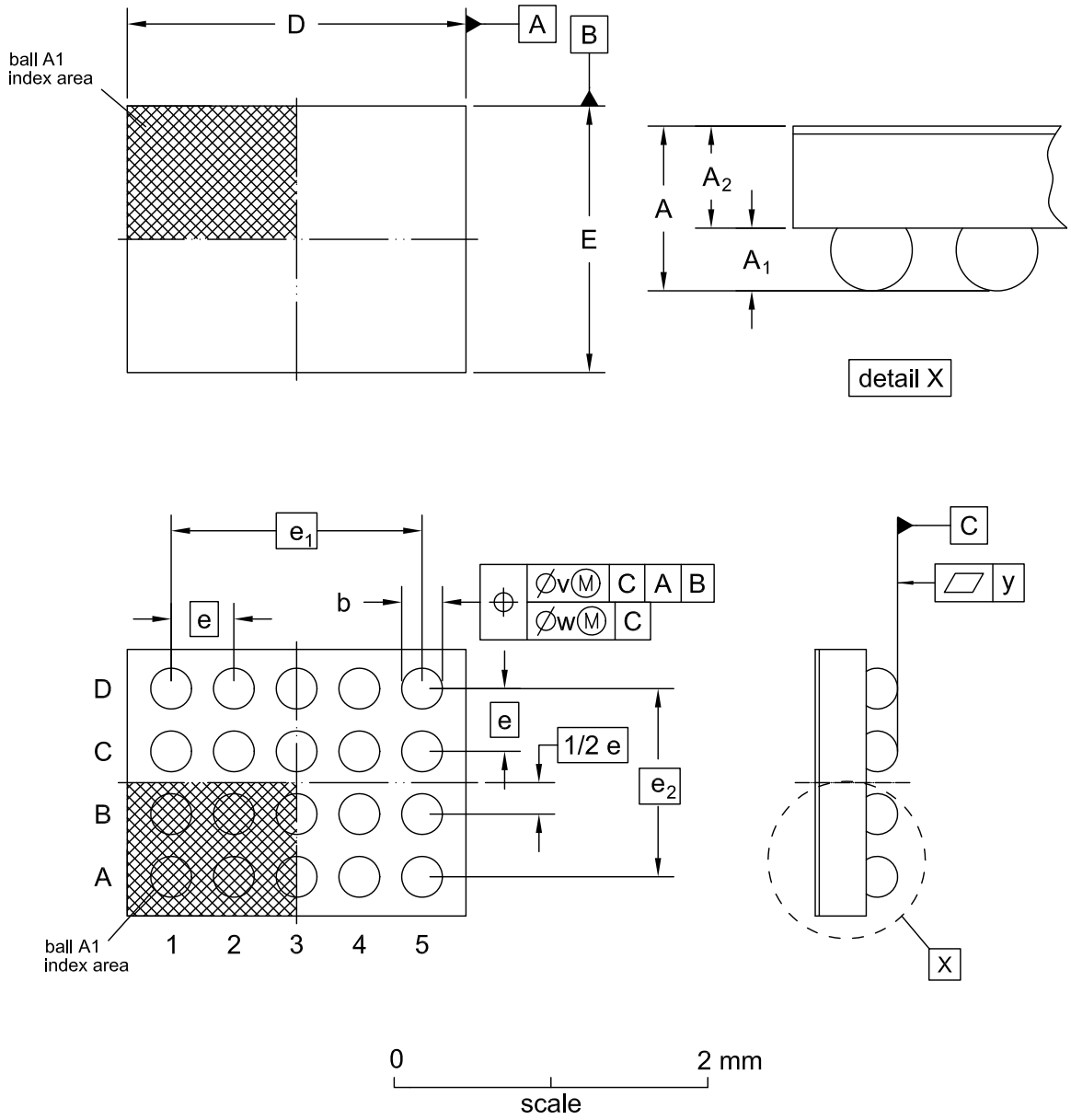
(1) VOUT

(2) $\overline{EN}$

(3) $I_{I(VIN)}$

Fig 21. Turn-off time at 5V

15. Package outline



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX.	0.565	0.230	0.350	0.290	2.19	1.73	0.4	1.6	1.2	0.15	0.05	0.03
	NOM.	0.525	0.200	0.325	0.260	2.16	1.70						
	MIN.	0.485	0.170	0.300	0.230	2.13	1.67						

NOTE: Backside coating 25 um

Fig 22. Package outline SOT1397-6 (WLCSP20)

16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX30P6093A v.1	20180816	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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