NX5P3290

USB PD and Type-C current-limited power switch

Rev. 1.2 — 7 June 2019 Product data sheet

1. General description

The NX5P3290 is a precision adjustable current-limited power switch for USB PD application. The device includes under voltage lockout, over-temperature protection, and reverse current protection circuits to automatically isolate the switch terminals when a fault condition occurs. The 29 V tolerance on VBUS pin ensures the device is able to work on a USB PD port; a current limit input (ILIM) pin defines the overcurrent limit threshold; an open-drain fault output ($\overline{FLT}$) indicates when a fault condition has occurred.

The overcurrent limit threshold can be programmed from 400 mA to 3.3 A, using an external resistor between the ILIM pin and GND pin. In the overcurrent condition, the device will clamp the output current to the value set by ILIM and keep the switch on while asserting the $\overline{FLT}$ flag.

To minimize current surges during normal turn on, the device has built in soft start by limiting the power switch turn on slew rate. However, user can disable the soft start and request a fast output by pulling FO pin HIGH.

A fast RCP recovery circuit has been added to the switch to prevent any reverse current flowing back to power source at all times. When exiting from reverse current protection state, the power MOSFET will turn on within 50 us. The fast RCP recovery ensures the voltage on VBUS doesn't drop too much in a power source swap application.

NX5P3290 is offered in a 2.05 x 2.05 mm, 16 bump WLCSP package.

2. Features and benefits

- VIN supply voltage range from 4.0 V to 5.5 V
- All time reverse current protection with ultra fast RCP recovery
- Adjustable current limit from 400 mA to 3.3 A
- Clamped current output in overcurrent condition
- 29 V high voltage tolerance on VBUS pin
- Low ON resistance of the power FETs: 35 mΩ (typical) in total
- Over temperature protection
- Safety approvals
  - UL 62368-1, 2nd edition, file no. 20161017-E470128
  - IEC 62368-1, 2nd edition, file no. DK-57975-UL
- ESD protection
  - IEC61000-4-2 contact discharge exceeds 8 kV on VBUS
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM AEC standard Q100-01 (JESD22-C101E) exceeds 500 V
- Specified from –40 °C to +85 °C ambient temperature

3. Applications

- Notebook, ultrabook and desktop
- USB PD and Type C port/hubs
- Tablet and smart phone

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NX5P3290UK	X5PT4	WLCSP16	wafer level chip-scale package; 16 bumps; 2.05 x 2.05 mm x 0.555 mm (Backside coating included)	SOT1394-2

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX5P3290UK	NX5P3290UKZ	WLCSP16	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	3000	T_{amb} = –40 °C to +85 °C

5. Marking

Table 3. Marking

Line	Marking	Description
A	X5PT4	basic type name
B	mmmmmmmnn	wafer lot code (mmmmmm) and wafer number (nn)
C	XtDYYWW	manufacturing code: X = foundry location t = assembly location D = RoHS code (dark green) YY = assembly year code WW = assembly week code

6. Functional diagram

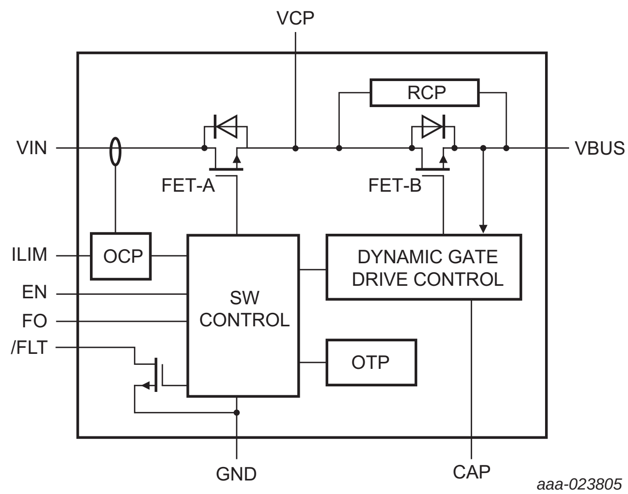


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

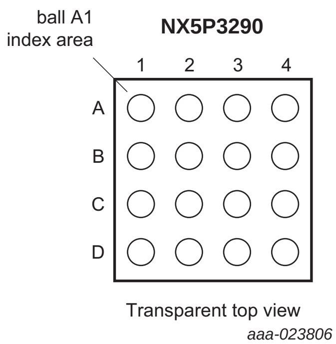


Fig 2. Pin configuration for WLCSP16

	1	2	3	4
A	VIN	VIN	ILIM	/FLT
B	VCP	VCP	GND	EN
C	VCP	VBUS	GND	FO
D	VBUS	VBUS	GND	CAP

Transparent top view

aaa-023807

Fig 3. Ball mapping for WLCSP16

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
VIN	A1, A2	input voltage
VCP	B1, B2, C1	Central point of two power MOSFETs.
VBUS	C2, D1, D2	output voltage
ILIM	A3	current limiter. connect a resistor to GND to adjust the current limit level
$\overline{\text{FLT}}$	A4	fault condition indicator (open-drain output)
EN	B4	enable input (active HIGH with internal 1 MΩ pull down resister)
GND	B3, C3, D3	ground (0 V)
FO	C4	Fast turn on. Pull this pin HIGH to enable fast turn-on feature. 1 MΩ pull down resister integrated.
CAP	D4	connect a capacitor to GND

8. Functional description

Table 5. Function table[1]

EN	FO	VIN	$\overline{FLT}$	Main Power Switch
X	X	< 4.0 V	Z	under voltage lockout, Switch open
L	X	4.0 V to 5.5 V	Z	disabled; switch open
H	L	4.0 V to 5.5 V	Z	enabled; switch turns on with slew rate control
H	H	4.0 V to 5.5 V	Z	enabled; switch turns on without slew rate control; fast turn on
H	X	4.0 V to 5.5 V	L	In current limit condition or over temperature protection
X	X	4.0 V to 5.5 V and VIN <= VBUS	Z	Reverse protection; switch open

[1] H = HIGH voltage level; L = LOW voltage level.

8.1 EN input

When the EN is set LOW, all the FETs will be disabled, the device will enter low-power mode disabling all protection circuits and setting the $\overline{FLT}$ output high impedance. When EN is set HIGH, all protection circuits will be enabled and then, if no fault condition exists, the main power MOSFETs will be turn on.

8.2 Fast recovery Reverse-Current Protection (RCP)

NX5P3290 uses dynamic gate drive control loop to implement reverse-current protection. During normal operation, device will always try to regulate the VBUS output voltage to be VIN - 70 mV.

When the load current produces a drop voltage greater than 70 mV, the gate control loop will drive the power MOS to lower its Rdson to try to achieve the 70 mV. In the heavy load condition, the gate control loop will keep increasing the gate driving current of the MOSFET until it is fully on and will remain fully on if the voltage drop at that time still exceeds 70 mV.

In light load condition, when the drop voltage is below 70 mV, the gate control loop will reduce the gate driving current to increase the Rdson to try to achieve the 70 mV drop voltage, which leads to the complete shutdown of the power MOSFET in reverse voltage condition.

If VBUS voltage is higher than VIN when enabling the device, the power MOSFET will never turn on. The device will always do pre-check before switching on the power MOSFETs.

In the RCP state, EN is HIGH; when the VBUS drops below VIN, the device will exit the RCP state and turn on the power FET again within 50 us. The fast recovery of the power MOSFET is assisted by the external boost capacitor at CAP pin. The boost capacitor will be charged whenever EN is pulled HIGH.

The RCP circuit, together with dynamic gate drive control circuit, act like an “ideal diode” that protects any reverse current when VBUS rise slew rate is slower than 30mV/us according to USB PD spec. If the VBUS rise slew rate is faster than 30mV/us, there may be reverse current; the current value depends on different slew rate and voltage level.

The input voltage level of FO pin has nothing to do with RCP recovery time.

8.3 Fast Turn ON

In order to reduce the power on inrush current, NX5P3290 has deployed slew rate control for normal turn on; there will be around 2 ms rising time. However, in the quick-swap application, fast turn on is requested. A customer can achieve this by pulling FO pin HIGH. By doing this, rise time will be reduced to the 100 us level. There is an internal 1 MΩ pull-down resister on this pin.

To support the Fast role swap, the user shall pull up FO pin first, then enable the EN pin of NX5P3290 when the FRS is requested. Depending on the voltage on VBUS, there will be two scenarios:

- V(VBUS) > V(VIN)

  The switch will enter RCP mode. Once the voltage on VBUS drops below VIN voltage, switch will be immediately turn on within 50 us.

- V(VBUS) <= V(VIN)

  The switch will perform a fast turn ON as the FO is HIGH; the turn on time is 150 us.

8.4 Under-voltage lock-out

Independently of the logic level on the EN pin, the under-voltage lockout (UVLO) circuit disables the N-channel MOSFET and enters low power mode until the input voltage reaches the UVLO turn-on threshold VUVLO.

8.5 ILIM

The overcurrent protection circuit's (OCP) trigger value I_{OCP} can be set using an external resistor R_{ILIM} connected between ILIM pin and GND pin. When EN is set HIGH and the ILIM pin is grounded, the N-channel MOSFET will be disabled and the $\overline{FLT}$ output set LOW. The I_{OCP} setting is given in Table 12.

8.6 Main Power FET Overcurrent protection (OCP)

The device offer overcurrent protection when enabled, three possible overcurrent conditions can occur. These conditions are:

- Overcurrent at start-up, $I_{SW} > I_{OCP}$ when enabling the N-channel MOSFET.
- Overcurrent when enabled, $I_{SW} > I_{OCP}$ when the N-channel MOSFET is enabled.
- Short circuit when enabled, I_{SW} > 10 A (typical).

In the overcurrent condition, because the device clamps the output current rather than completely shut down the switch, the power dissipation on the device might be increased which could lead to over temperature protection (see Section 8.8).

8.6.1 Overcurrent at start-up

If the device senses a VBUS short to GND or overcurrent while enabling the N-channel MOSFET, OCP is triggered. It limits the output current to I_{OCP} and after the de-glitch time sets the $\overline{FLT}$ output LOW.

8.6.2 Overcurrent when enabled

If the device senses $I_{SW} > I_{OCP}$ when enabled, OCP is triggered. It limits the output current to I_{OCP} and after the de-glitch time sets the $\overline{FLT}$ output LOW. As a consequence, limiting the output current will reduce $V_{O(VBUS)}$.

8.6.3 Short circuit when enabled

If the device senses I_{SW} > 10 A when enabled, a short circuit is detected. The device disables the N-channel MOSFET immediately. It then enables the N-channel MOSFET again, output current is limited to I_{OCP} and after the de-glitch time the $\overline{FLT}$ output is set LOW. Thermal protection will be triggered due to the big power consumption on the device.

8.7 $\overline{FLT}$ output

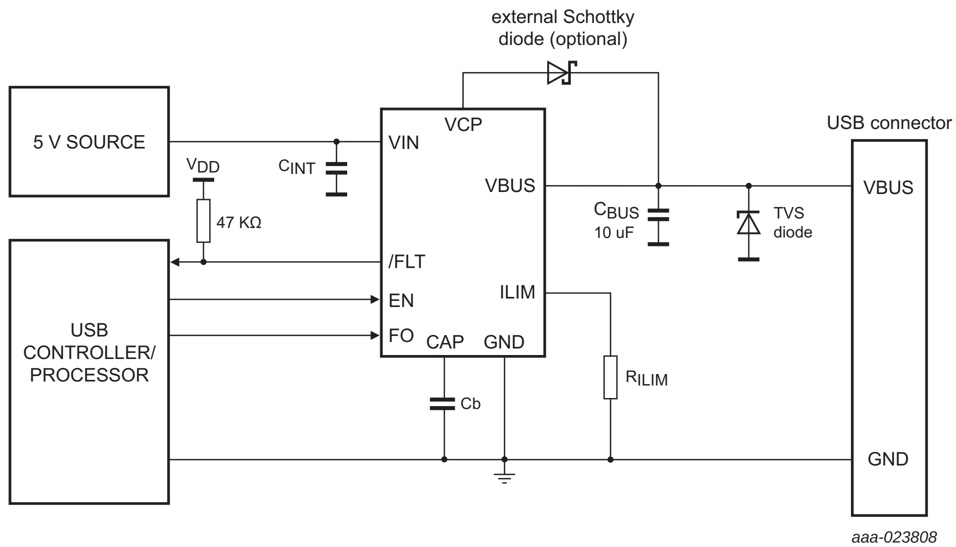
The $\overline{FLT}$ output is an open-drain output that requires an external pull-up resistor. The $\overline{FLT}$ output will be set LOW to indicate an OCP or OTP condition has occurred. The $\overline{FLT}$ output will return to the high impedance state automatically once the fault condition is removed. An internal 8 ms de-glitch circuit for the overcurrent protection is used when entering fault conditions. Over-temperature condition doesn’t have de-glitch time, the $\overline{FLT}$ signal will be asserted immediately. The RCP circuit won’t trigger $\overline{FLT}$ signal.

8.8 Over-temperature protection

If the device temperature exceeds 140 °C when EN is set HIGH, the over-temperature protection (OTP) circuit will disable the Power MOSFET and indicate a fault condition by setting the $\overline{FLT}$ pin LOW. Any transition on the EN pin will have no effect. Once the device temperature decreases to below 115 °C the device will return to the defined state.

In the overcurrent limiting condition, the increased power dissipation on the device will result the OTP, especially in the output-short-to-GND error.

9. Application diagram



A 0.1 µF ceramic capacitor (C_{INT}) is required for local decoupling. Higher capacitor values C_{INT} further reduce the voltage drop at the input. When driving inductive loads, a larger capacitance C_{INT} prevents voltage spikes from exceeding absolute maximum voltage of VIN. The CBUS capacitor should be placed as closer as possible to VBUS pin.

The recommended Cb is 1 nF with at least 16 V voltage tolerance.

The external Schottky diode is optional, NX5P3290 works well without it. To improve the lowest VBUS voltage during fast role swap, it is recommended to add a lower forward voltage diode, for example VF = 0.3 V.

When NX5P3290 is not used in conjunction with NX20P5090, a TVS diode should be added on VBUS node to protect surge event, such as hot plug in.

Fig 4. Application diagram

10. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VBUS [1]	–0.5	+29	V
		VIN; VCP; ILIM; EN; FO [1]	–0.5	+6	V
		CAP [1]	–0.5	+12	V
V_O	output voltage	$\overline{\text{FLT}}$ [1]	–0.5	+6	V
I_{IK}	input clamping current	input EN: $V_{I(EN)} < -0.5$ V	–50	-	mA
$I_{I(source)}$	input source current	input ILIM	-	1	mA
I_{SK}	switch clamping current	input VIN: $V_{I(VIN)} < -0.5$ V	–50	-	mA
		output VOUT: $V_{O(VBUS)} < -0.5$ V	–50	-	mA
I_{SW}	Main Power switch continuous current	$V_{SW} > -0.5$ V [2]	-	3.6	A
$T_{j(max)}$	maximum junction temperature		–40	+125	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	[3]	-	1.7	W

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] Internally limited.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two layer PCB.

11. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VIN	4.0	5.5	V
		EN; FO	0	5.5	V
		VBUS (OFF state)	0	23	V
V_O	Output voltage	VBUS; $\overline{\text{FLT}}$	0	5	V
I_{SW}	switch current	T_{amb} = –40 °C to +85 °C	0	3	A
$I_{O(sink)}$	output sink current	$\overline{\text{FLT}}$	0	10	mA
R_{ILIM}	current limit resistance	ILIM pin to GND	16	140	kΩ
C_{Bus}	VBUS output capacitance	VBUS to GND	10	100	μF
T_{amb}	ambient temperature		–40	+85	°C

12. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	58.4	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, ensure all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13. Static characteristics

Table 9. Static characteristics

At recommended operating conditions; $V_{I(VIN)} = V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 9

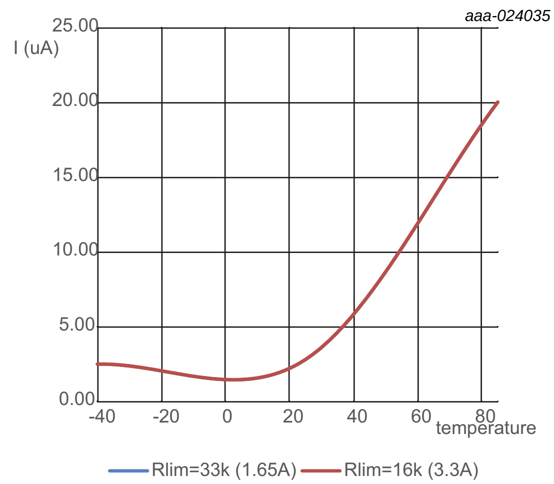
Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	EN; FO; $V_{I(VIN)}$ = 4.0 V to 5.5 V;	1.2	-	-	V
V_{IL}	LOW-level input voltage	EN; FO; $V_{I(VIN)}$ = 4.0 V to 5.5 V;	-	-	0.4	V
I_I	input leakage current	EN; FO; $V_{I(VIN)}$ = 5.0 V;	-	-	7	μA
$I_{(VIN)}$	supply current	VBUS open; $V_{I(VIN)}$ = 5.0 V				
		EN = GND (low power mode);	-	3	55	μA
		EN = $V_{I(VIN)}$; R_{ILIM} = 33 kΩ	-	1.3	1.65	mA
		EN = $V_{I(VIN)}$; R_{ILIM} = 16 kΩ	-	1.35	1.65	mA
$I_{S(OFF)}$	VBUS OFF-State leakage current	$V_{I(VIN)}$ = 5.0 V; $V_{I(VBUS)}$ = 0 V; EN = LOW [2]	–5	0.1	-	μA
	VIN OFF-state leakage current	$V_{I(VBUS)}$ = 5.0 V; $V_{I(VIN)}$ = 0 V; EN = LOW [2]	–2	0.1	-	μA
		$V_{I(VBUS)}$ = 20 V; $V_{I(VIN)}$ = 0 V; EN = LOW [2]	–2	0.1	-	μA
$I_{S(ON)}$	FET-B leakage current in RCP	$V_{I(VIN)}$ = 5 V; $V_{I(VBUS)}$ = 20 V; EN = 5 V [2] [3]	–2	0.1	-	μA
R_{pd}	Pull-down resistance	EN; FO; $V_{I(VIN)}$ = 5 V	-	1	-	MΩ
V_{UVLO}	under voltage lockout voltage	VIN pin	-	3.6	3.8	V
$V_{hys(UVLO)}$	under voltage lockout hysteresis voltage		-	100	-	mV
V_{OL}	LOW-level output voltage	$\overline{FLT}$; I_O = 4 mA	-	-	0.3	V
$C_{I(EN)}$	EN pin		-	3	-	pF
$C_{I(FO)}$	FO pin		-	4	-	pF

[1] Typical values are measured at T_j = 25 °C.

[2] Currents are defined with respect to conventional current flow into the respective terminal. Negative value means the current flows out of the respective terminal of the chip.

[3] Guaranteed by design

13.1 Graphs



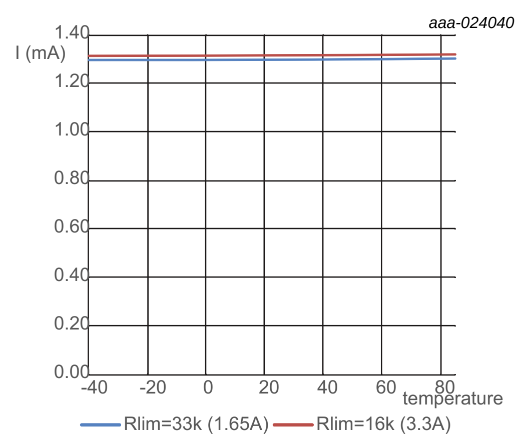
$V_{I(EN)}$ = GND; $V_{I(VIN)}$ = 5.0 V

X = T_{amb}, Y = $I_{(VIN)}$

(1) R_{ILIM} = 33 K (1.65 A)

(2) R_{ILIM} = 16 k (3.3 A)

Fig 5. OFF state supply current versus temperature



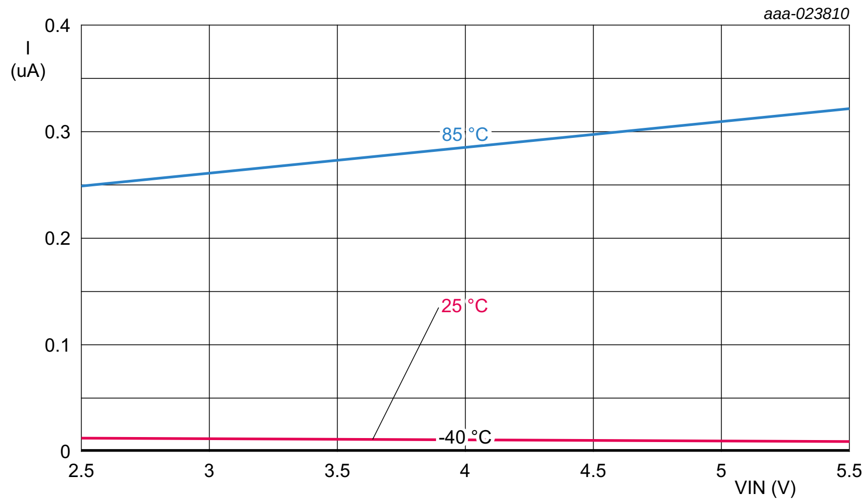
$V_{I(EN)} = V_{I(VIN)}$; $V_{I(VIN)}$ = 5.0 V

X = T_{amb}, Y = $I_{(VIN)}$

(1) R_{ILIM} = 33 K (1.65 A)

(2) R_{ILIM} = 16 k (3.3 A)

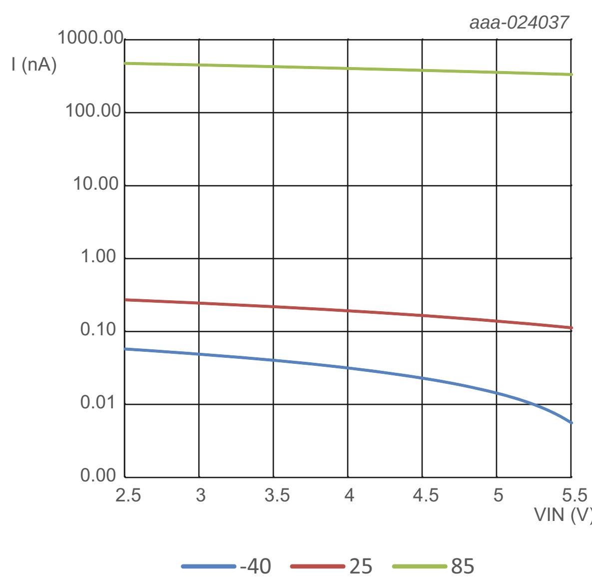
Fig 6. ON state supply current versus temperature



$V_{I(EN)}$ = GND; $V_{I(VBUS)}$ = 0 V; R_{ILIM} = 16 k (3.3 A)

X = $V_{I(VIN)}$ from 2.5 V to 5.5 V; Y = $I_{(VIN)}$

Fig 7. VBUS off state leakage versus temperature



$V_{I(EN)}$ = GND; $V_{I(VIN)}$ = 0 V; R_{ILIM} = 16 k (3.3 A)

X = $V_{I(VBUS)}$ from 2.5 V to 5.5 V; Y = $I_{(VIN)}$

Fig 8. VIN off state leakage versus temperature

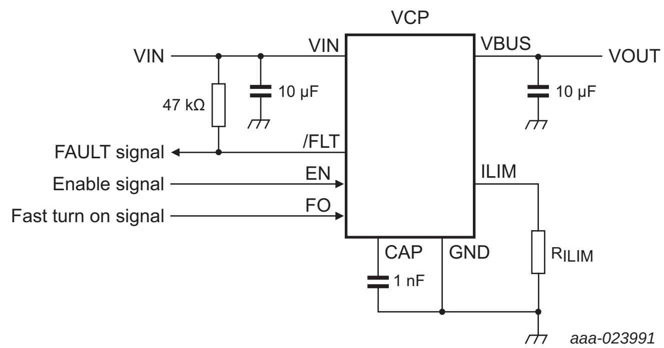


Fig 9. Typical characteristics reference schematic

13.2 Thermal shutdown

Table 10. Thermal shutdown

$V_{I(VIN)} = V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{th(ots)}$	over temperature shutdown threshold temperature	$V_{I(VIN)}$ = 4.0 V to 5.5 V	-	140	-	°C
$T_{th(otp)hys}$	hysteresis of over temperature protection threshold temperature	$V_{I(VIN)}$ = 4.0 V to 5.5 V	-	25	-	°C

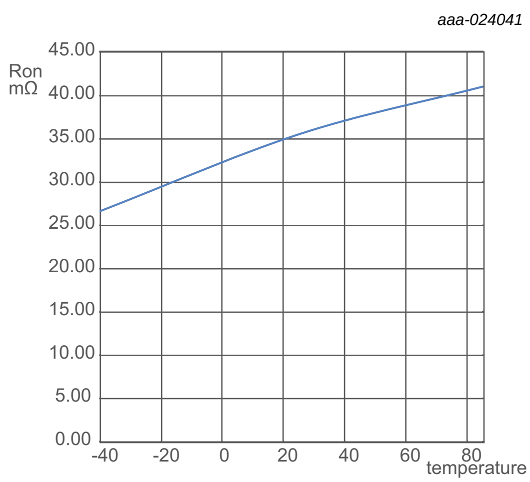
13.3 ON resistance

Table 11. ON resistance

$V_{I(VIN)} = V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 9

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ON}	ON resistance	$R_{FETA} + R_{FETB}$; $V_{I(VIN)}$ = 4.0 to 5.5 V; see Figure 10				
		T_{amb} = 25 °C	-	35	42	mΩ
		T_{amb} = –40 °C to +85 °C	-	-	49	mΩ

13.4 ON resistance graphs



X = T_{amb}, Y = Ron; $V_{I(VIN)}$ = 5.0 V

Fig 10. Typical ON resistance versus temperature

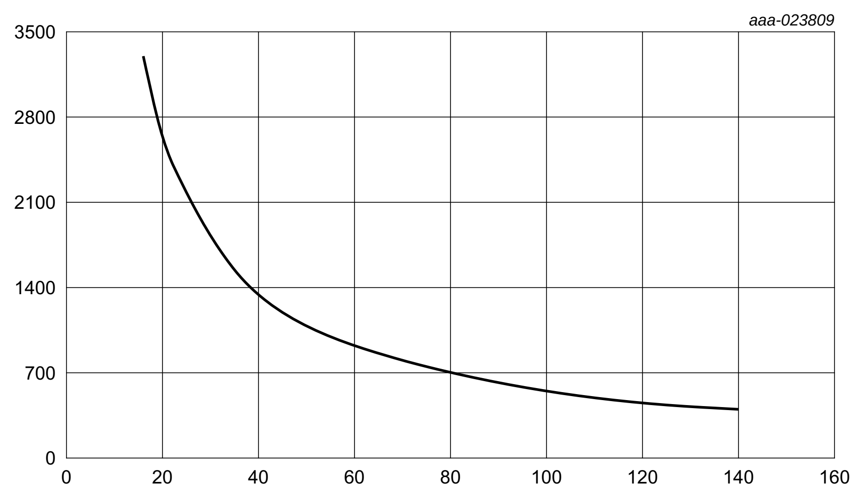
13.5 Current limit

Table 12. Current limit
$V_{I(VIN)} = V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 9

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OCP}	overcurrent protection current	$V_{I(VIN)}$ = 4.0 to 5.5 V; T_{amb} = –40 °C to +85 °C; see Figure 11,				
		R_{ILIM} = 140 kΩ	330	400	465	mA
		R_{ILIM} = 100 kΩ	480	550	625	mA
		R_{ILIM} = 54 kΩ	915	1013	1107	mA
		R_{ILIM} = 33 kΩ	1505	1650	1780	mA
		R_{ILIM} = 24.5 kΩ	2024	2220	2398	mA
		R_{ILIM} = 20 kΩ	2450	2640	2820	mA
		R_{ILIM} = 16 kΩ	3100	3300	3531	mA
		ILIM shorted to VIN	168	210	273	mA

[1] 1% tolerance resistor is recommend for R_{ILIM}

13.6 Current limit graphs



$V_{I(VIN)}$ = 5.0 V; X = R_{ILIM}, Y = $49750x^{-0.976}$

Fig 11. Typical overcurrent protection current versus external resistor value R_{ILIM}

14. Dynamic characteristics

Table 13. Dynamic characteristics

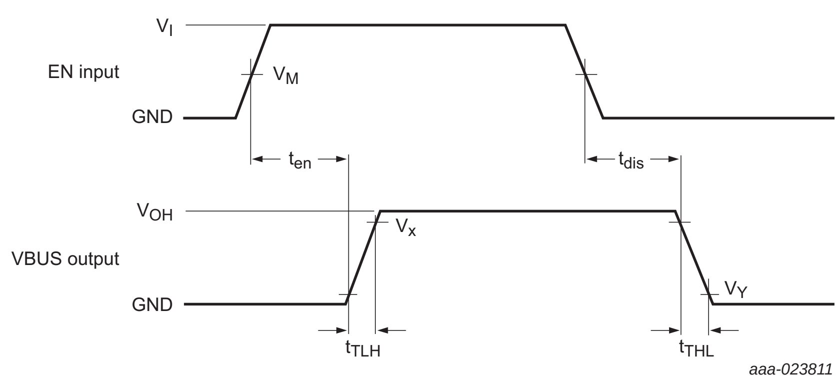
At recommended operating conditions; $V_{I(VIN)} = V_{I(EN)}$, $R_{FAULT} = 10\ k\Omega$ unless otherwise specified; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{TLH}	LOW to HIGH output transition time	VBUS; $V_{I(VIN)}$ = 5.0 V; C_L = 10 uF; R_L = 100 Ω; see Figure 12 and Figure 13				
		$V_{I(FO)}$ = GND	-	2	-	ms
		$V_{I(FO)}$ = 5.0 V	-	50	100	μs
t_{THL}	HIGH to LOW output transition time	VOUT; C_L = 10uF; R_L = 100 Ω; see Figure 12 and Figure 13				
		$V_{I(VIN)}$ = 5.0 V	-	2.2	-	ms
t_{en}	enable time	EN to VOUT; C_L = 10uF; R_L = 100 Ω; seeFigure 14 and Figure 15				
		$V_{I(VIN)}$ = 5.0 V; $V_{I(FO)}$ = GND	-	0.75	-	ms
		$V_{I(VIN)}$ = 5.0 V; $V_{I(FO)}$ = 5.0 V	-	60	-	μs
t_{dis}	disable time	EN to VOUT; $V_{I(VIN)}$ = 5.0 V; C_L = 10 uF; R_L = 100Ω; see Figure 16 and Figure 17	-	70	-	μs
$t_{on(RCP)}$	RCP recovery time	$V_{I(VIN)}$ = 5.0 V; EN = HIGH; From VBUS drops below VIN to FET-B ON; C_L = 10uF	-	30	50	μs
$t_{dis(RCP)}$	RCP turn off time	FET-B RCP turn OFF time [2]	-	10	-	μs
t_{degl}	de-glitch time	$\overline{FLT}$ in OCP; $V_{I(VIN)}$ = 5 V; see Figure 20 to Figure 21	-	8	-	ms

[1] Typical values are measured at T_j = 25 °C.

[2] Guaranteed by design

14.1 Waveform and test circuits



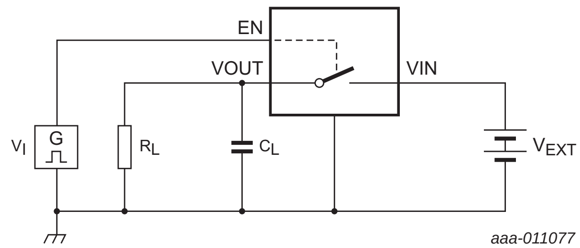
Measurement points are given in Table 14.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 12. Switching times and rise and fall times

Table 14. Measurement points

Supply voltage	EN Input	Output	
$V_{I(VIN)}$	V_M	V_X	V_Y
5.0 V	$0.5 \times V_{I(EN)}$	$0.9 \times V_{OH}$	$0.1 \times V_{OH}$



Test data is given in Table 15.

Definitions test circuit:

R_L = Load resistance.

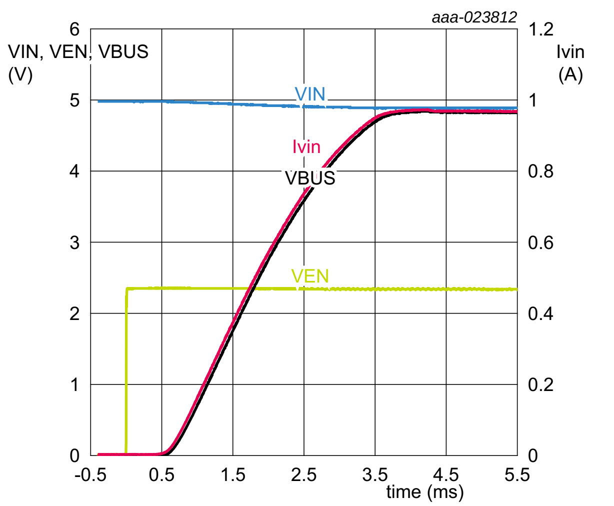
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 13. Test circuit for measuring switching times

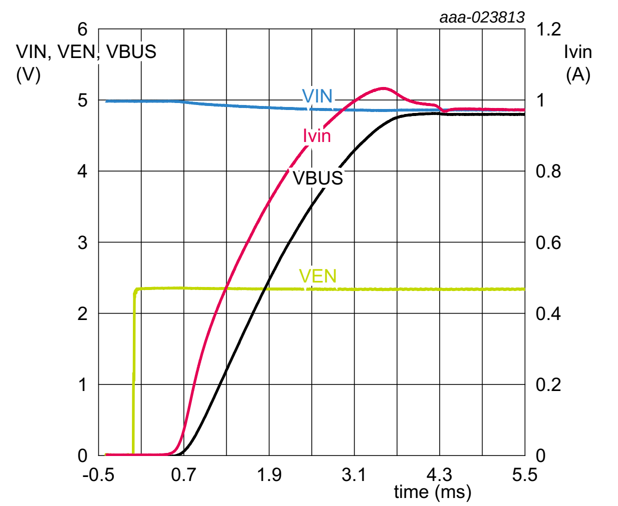
Table 15. Test data

Supply voltage	EN Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	R_L
5.0 V	0 to $V_{I(VIN)}$	10 μF	100 Ω



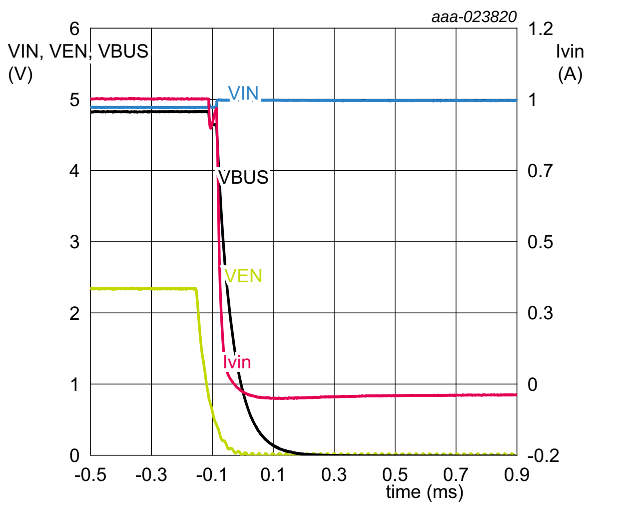
$V_{I(VIN)}$ = 5 V; R_L = 5 Ω; C_L = 10 uF; R_{ILIM} = 33 kΩ (1.5 A)

Fig 14. Typical 10 uF enable time versus inrush current



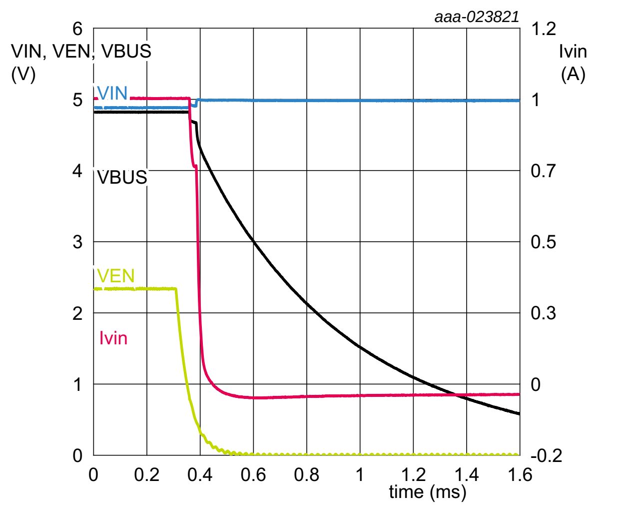
$V_{I(VIN)}$ = 5 V; R_L = 5 Ω; C_L = 100uF; R_{ILIM} = 33 kΩ (1.5 A)

Fig 15. Typical 100 uF enable time versus inrush current



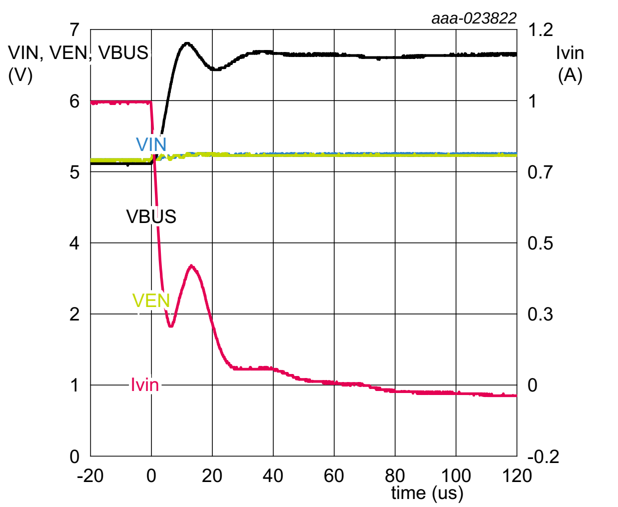
$V_{I(VIN)}$ = 5 V; R_L = 5 Ω; C_L = 10 uF; R_{ILIM} = 33 kΩ (1.5 A)

Fig 16. Typical 10 uF disable time



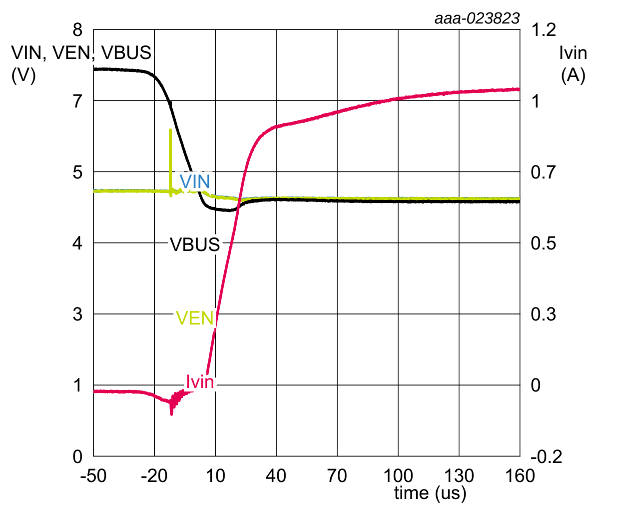
$V_{I(VIN)}$ = 5 V; R_L = 5 Ω; C_L = 100uF; R_{ILIM} = 33 kΩ (1.5 A)

Fig 17. Typical 100 uF disable time



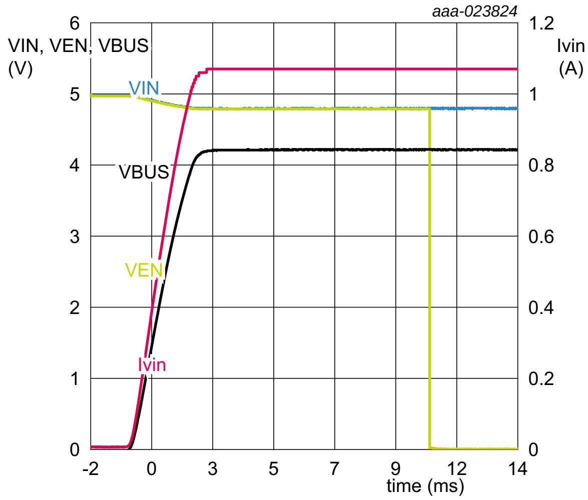
$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ

Fig 18. Reverse-current protection response



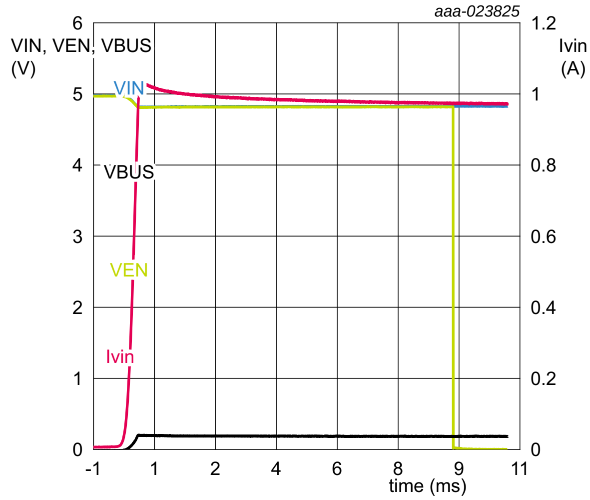
$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ

Fig 19. Reverse-current protection recovery



$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ (1.5 A)

Fig 20. Device enabled into current limit mode

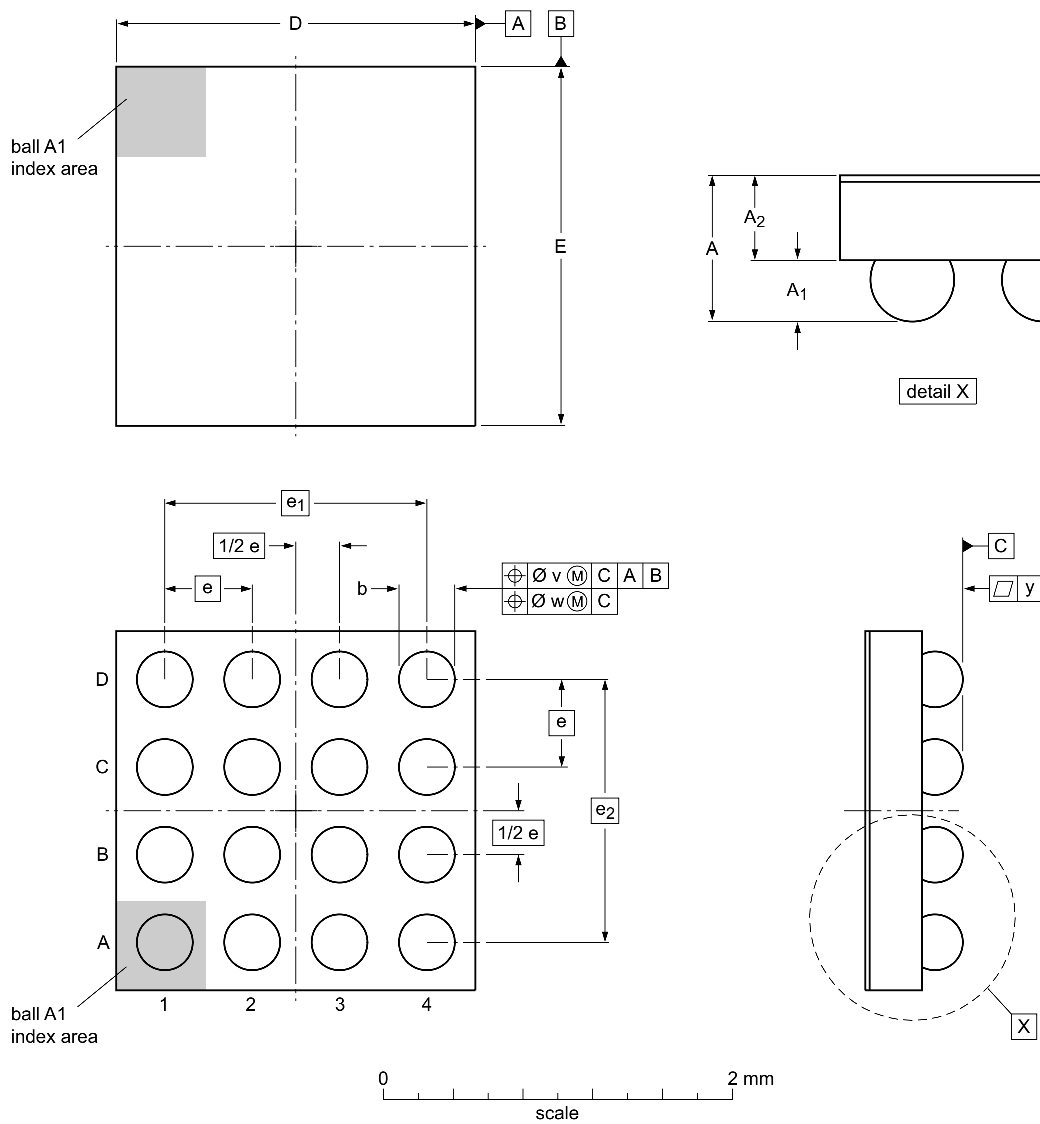


$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ

Fig 21. Device start up in VBUS short to GND

15. Package outline

WLCSP16: wafer level chip-scale package; 16 bumps; 2.05 x 2.05 x 0.555 mm (Backside coating included) **SOT1394-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.595	0.26	0.350	0.35	2.08	2.08						
	nom	0.555	0.23	0.325	0.32	2.05	2.05	0.5	1.5	1.5	0.05	0.015	0.03
	min	0.515	0.20	0.300	0.29	2.02	2.02						

Note: Backside coating 25 µm

sot1394-2_po

Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT1394-2		- - -				~~15-12-24~~ 16-08-29

Fig 22. Package outline SOT1394-2 (WLCSP16)

16. Abbreviations

Table 16. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
CDM	Charged Device Model
HBM	Human Body Model
USB	Universal Serial Bus
VOIP	Voice over Internet Protocol

17. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5P3290 v.1.2	20190607	Product data sheet	-	NX5P3290 v.1.1
Modifications:	• Table 6 “Limiting values”, V_I: Created separate row for pin CAP			
NX5P3290 v.1.1	20170613	Product data sheet	-	NX5P3290 v.1
Modifications:	• Table 7 “Recommended operating conditions”, V_I: Created separate row for pins EN and FO			
NX5P3290 v.1	20161101	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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