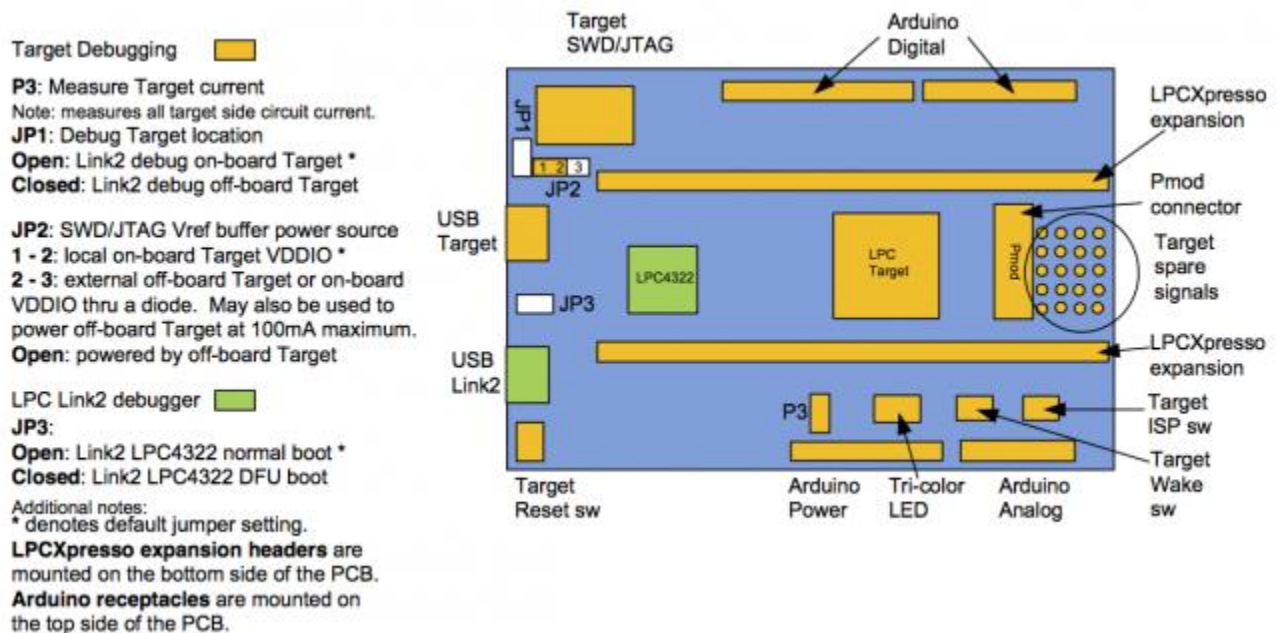# LPCXpresso V2 Board Family

LPCXpresso V2 Board Family

Since the introduction of the first variant in 2009, the original LPCXpresso board has reenergised the whole MCU evaluation board market. NXP is now proud to introduce the new generation of LPCXpresso V2 boards which build upon the original design, providing many new and exciting features.

The standard LPCXpresso V2 board design offers the following features:

- Built in Link2 debug probe, based on NXP LPC4322 MCU.
  - Compatible with LPCXpresso IDE and with other toolchains using CMSIS-DAP protocol
  - Segger J-Link firmware option (downloadable using LPCScrypt utility).
- Debug connector to allow debug of target MCU via an external probe.
- Can be configured to act as a standalone probe to allowing debugging of an external board.
- Tri-color LED, ISP and WAKE buttons
- Target Reset button
- Connector for target MCU's USB device peripheral
- Expansion
  - MCU pins available on 'standard LPCXpresso/mbed' expansion connector (board bottom side)
  - Arduino connectors compatible with the "Arduino UNO" platform (board top side)
- Powered from multiple sources
  - Link2 USB
  - Target USB
  - LPCXpresso/mbed header
- P3 allows measurement of current of all target side circuitry
-

Target Debugging ▭

P3: Measure Target current
Note: measures all target side circuit current.
JP1: Debug Target location
Open: Link2 debug on-board Target *
Closed: Link2 debug off-board Target

JP2: SWD/JTAG Vref buffer power source
1 - 2: local on-board Target VDDIO *
2 - 3: external off-board Target or on-board VDDIO thru a diode. May also be used to power off-board Target at 100mA maximum.
Open: powered by off-board Target

LPC Link2 debugger ▭
JP3:
Open: Link2 LPC4322 normal boot *
Closed: Link2 LPC4322 DFU boot

Additional notes:
* denotes default jumper setting.
LPCXpresso expansion headers are mounted on the bottom side of the PCB.
Arduino receptacles are mounted on the top side of the PCB.

Debugging

Debugging via the built-in debug probe

LPCXpresso IDE

As supplied, (JP1 - no jumper fitted, JP2 - jumpered across 1-2, JP3 - no jumper fitted), the built in LPC-Link2 based debug probe works as a plug'n'play debug probe with the LPCXpresso IDE. The first time you start an LPCXpresso debug session, a compatible debug firmware image is downloaded to the debug probe allowing you the debug the onboard target MCU.

Other toolchains

A number of other debug firmware images are available for the built-in debug probe to enable its use with other toolchains. These images are programmed into the flash memory of the LPC43xx MCU used for the debug probe using:

- [LPCScrypt](#)

Images available include

- J-Link by Segger
  - For compatibility with development tools that support the J-Link protocol, such as IAR Embedded Workbench, Keil MDK, Rowley CrossWorks, Atollic TrueSTUDIO, Somnium DRT as well as GDB-based tool chains such as emIDE.
- CMSIS-DAP
  - For compatibility with development tools that support the CMSIS-DAP protocol, such as Keil MDK, IAR Embedded Workbench and the LPCXpresso IDE

Debugging the onboard MCU via an external debug probe

To debug the LPCXpresso V2 board's target MCU using an external debug probe rather than the built-in probe, the follow jumper settings are required:

- JP1 - must be open (no jumper fitted)
- JP2 - connect a jumper across pins 1-2

IMPORTANT NOTE:

When using an external debug probe, do **NOT** connect a USB cable to the Link2 USB micro-B connector - as the Link2 side of the LPCXpresso V2 board must not be powered. This means the board should be powered from the Target USB micro-B connector (J3) or from the External Vin on the LPCXpresso connector (P2 pin 2). You cannot power from the Link2 USB micro-B connector and use an external debug probe.

Debugging an external board using the built-in debug probe

To debug the MCU fitted to an external board using the LPCXpresso V2 board's built-in debug probe, the follow jumper settings are required:

- JP1 - must be closed (jumper fitted)
- JP2 - connect a jumper across pins 2-3

You can then use the LPCXpresso V2 debug probe in the same way as if you were debugging the onboard target MCU.

Debug header and cables

For details of the 10-pin debug header (P1) fitted to the LPCXpresso V2 board, plus cable requirements, see the FAQ "Design Considerations for Debug."

Use of JP3

There are two reasons for installing the jumper at JP3:

- First of all, fitting JP3 allows LPCXpresso IDE to download the most up-to-date debug firmware to RAM via DFU rather than make use of any debug firmware image held in the debug probe's internal flash.
- Secondly, installing the jumper allows the user to update or reprogram the LPC43xx internal flash with a different image. If the jumper is installed at JP3 to update the LPC43xx internal flash, once the update is complete, the jumper will need to be removed and the board power cycled for the LPC43xx to boot from the new internal flash code. For more details, please see LPCScrypt information on nxp.com.

Support for mbed

The following LPCXpresso boards are compatible with the ARM mbed development system:

- LPCXpresso1549 - http://developer.mbed.org/platforms/LPCXpresso1549/
- LPCXpresso11U68 - http://developer.mbed.org/platforms/LPCXpresso11U68/

In order to be used for mbed development, you will need to download and install the latest mbed firmware onto your board, available from the mbed website at the above links.

Windows users: If you intend to use your mbed configured LPCXpresso V2 under Windows, you will also need to install the mbed Windows serial port driver.

Additional board specific information

LPCXpresso11U37H (OM13062)

The LPCXpresso11U37H board is an extended variant of the standard LPCXpresso V2 board design, designed to allow evaluation of the I/O Handler functionality available on parts such as the LPC11U37HFBD64. The I/O Handler is a software library-supported hardware engine that can be used to add performance, connectivity and flexibility to system designs. The I/O Handler can emulate serial interfaces such as UART, I2C, and I2S with no or very low additional CPU load and can off-load the CPU by performing processing-intensive functions like DMA transfers in hardware.

The most notable changes in the design of the LPCXpresso11U37H board are:

1. µSD card slot replaces the PMOD connector and the "target spare signals" prototyping area.
2. 12-pin (2*6) I/OH connector.
3. UART connector, 6-pin FTDI cable (TTL-232R-3V3) compatible.
4. Four additional LEDs.
5. Two potentiometers.
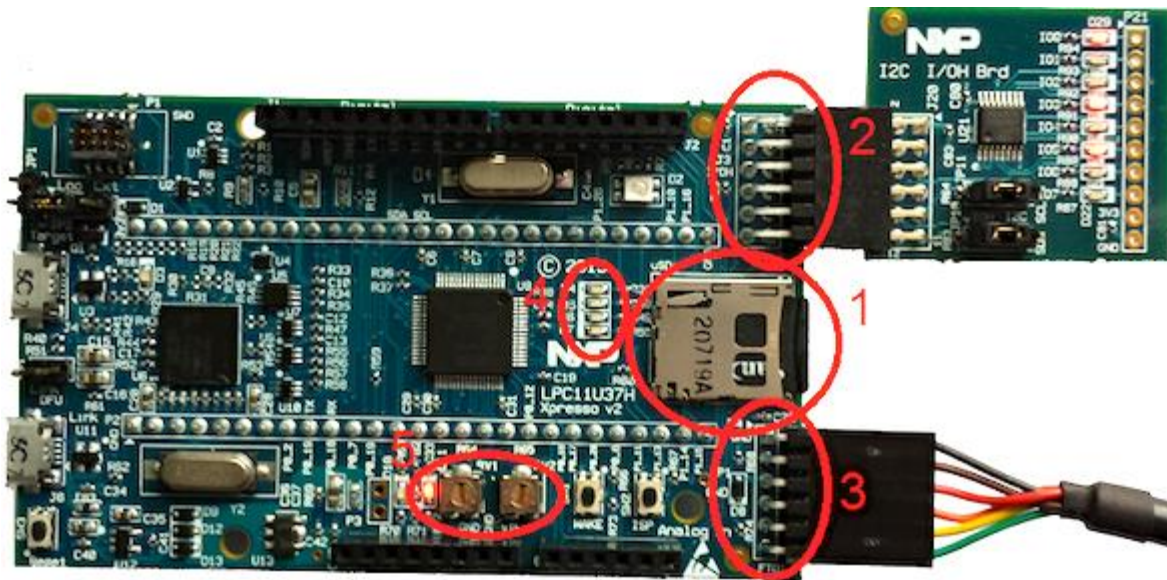
PModTM Support

LPCXpresso V2 boards have different PMOD support depending on their target applications. Further information below:

LPCXpresso1549:
a. pins 1 – 6 (left side) will support Pmod Type 2 (SPI) or Type 1 (GPIO).
b. pins 7 – 12 (right side) not designed to support I^{2}C. Does support Pmod Type 1 (GPIO) interface.

LPCXpresso11U68:
a. pins 1 – 6 (left side) will support Pmod Type 2 (SPI) or Type 1 (GPIO).
b. pins 7 – 12 (right side) designed to support I^{2}C, but does not have 2.2k pull up. Will support Pmod Type 1 (GPIO).

Note: LPCXpresso11U68 (Rev C) does have a pull up on the target I^{2}C SCL and SDA lines (these were not present on the previous revision).

LPCX11U37H:
(IOH connector)
a. pins 1 – 6 (left side) will support Pmod Type 2 (SPI) or Type 1 (GPIO).
b. pins 7 – 12 (right side) supports I2C and has 2.2k pull up or Type 1 (GPIO).
The LPCX11U37H I/O handler kit uses the PMOD interface connections for the specialized I2C and DALI daughter cards, with the LPCXpresso-side connector being male rather than female. In the LPCXpresso11U37H only version (available July 2014) does not have a PMOD connector fitted, so one can be added for use with standard PMOD-compatible cards.

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