

# UM10946

LPCXpresso4367/43S67/18S37 Rev B Boards

Rev. 1.0 — 18 November 2015

User manual

## Document information

Info	Content
<b>Keywords</b>	LPCXpresso4337, LPCXpresso43S37, LPCXpresso43S67, LPC4300, LPC43S00, LPC43xx, LPC43Sxx
<b>Abstract</b>	LPCXpresso4367/43S67 User Manual



**Revision history**

Rev	Date	Description
1.0	20151118	Initial version

**Contact information**

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 1. Introduction

The LPCXpresso™ family of boards provides a powerful and flexible development system for NXP's Cortex®-M family of MCUs. They can be used with a wide range of development tools, including the NXP's LPCXpresso IDE. The LPCXpresso4367 (OM13088), LPCXpresso43S67 (OM13084) and Revision B LPCXpresso18S37 (OM13076) boards have been developed by NXP to enable evaluation of and prototyping with the LPC4300, LPC43S00 and LPC18S00 MCUs respectively, and are based on the 100 pin BGA versions of these MCUs.

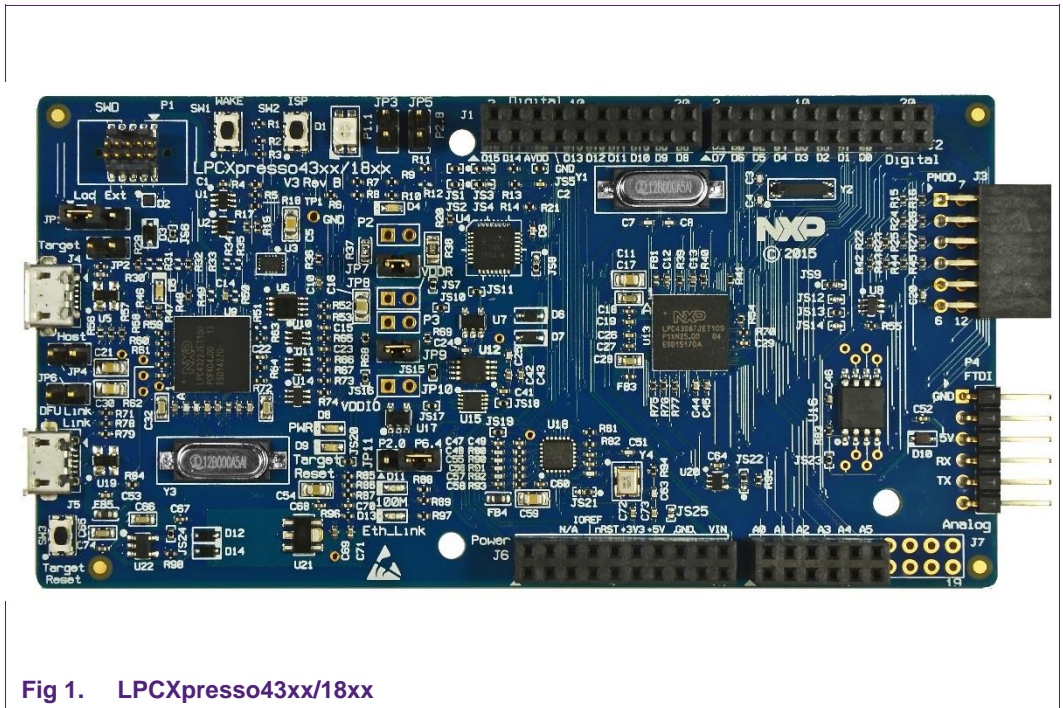


Fig 1. LPCXpresso43xx/18xx

This document describes the LPCXpresso4367, LPCXpresso43S67 and LPCXpresso18S37 board hardware. These boards are functionally identical (using an underlying Revision B circuit board) with the exception of target MCU and the inclusion/exclusion of the A7001CM Secure Element device. The name LPCXpresso4367 is used throughout this document to refer to all boards. The term “Target MCU” is used to refer to the Target microcontroller (LPC4367, LPC43S67 or LPC18S37). The following aspects of interfacing to the boards are covered by this guide:

- Main board features
- Setup for use with development tools
- Supporting software drivers
- Board interface connector pin out
- Jumper settings
- Powering the board
- Mechanical drawing

Note that Revision A LPCXpresso18S37 boards have different circuit designators and fewer functions. Please refer to User Manual UM10889 for that version of the board. The board revision is printed on the silkscreen directly below the ISP button (see [Fig 1.](#))

## 2. Feature summary

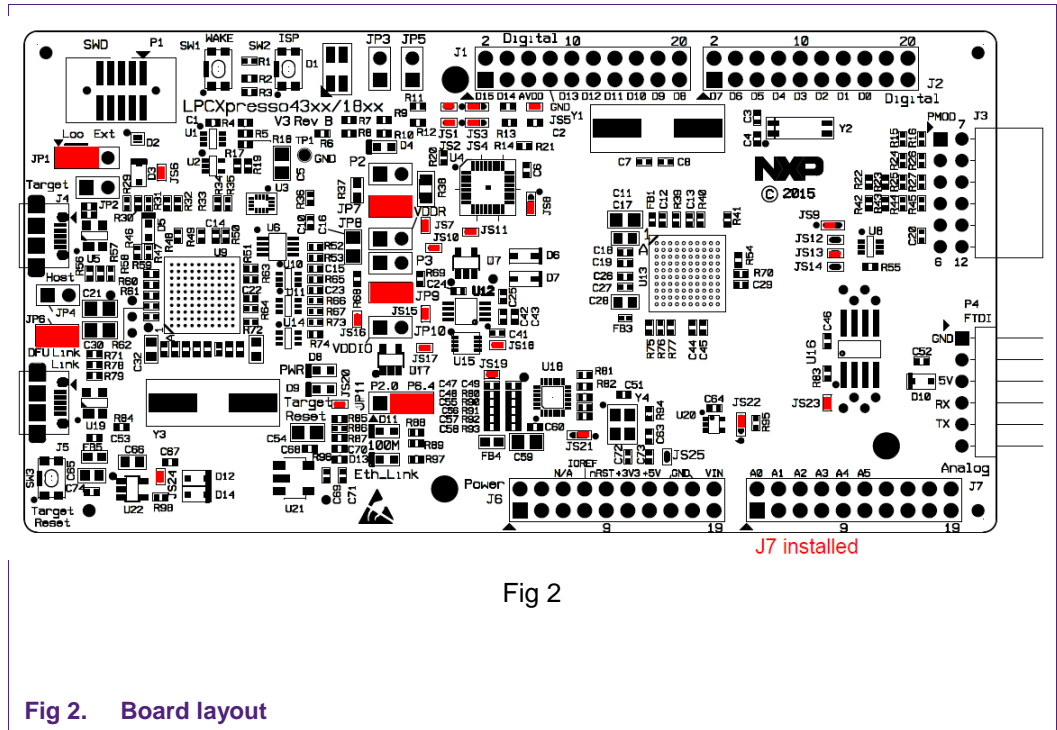
---

The LPCXpresso4367 board includes the following features:

- On-board, high-speed USB based, Link2 debug probe with support for ARM's CMSIS-DAP and SEGGER J-Link protocol options
- Link2 probe can be used with on-board Target MCU or external target
- Built-in current measurement
- Support for external debug probes
- Tri-color LED
- Target Reset, ISP and WAKE buttons
- Expansion options based on Arduino UNO and PMod™, plus additional expansion port pins
- UART, I<sup>2</sup>C and SPI port bridging from Target MCU to USB via the on-board debug probe
- FTDI UART connector
- 8Mb Macronix Quad SPI flash (MX25L8035EM2I-10G)
- Ethernet PHY (LAN8720A)
- A7001CM Secure Element (LPCXpresso43S67/18S37 only)

### 2.1 Board layout and settings

This section provides a quick reference guide to the main board components, configurable items, visual indicators and expansion connectors. The layout of the components on the LPCXpresso4367 board is shown in [Fig 2.](#) Default jumper positions are shown in red:



The function of each identified component is listed in [Table 1](#).

**Table 1. Connectors, indicators and jumpers**

Designator	Description	Reference section
D1	Tri-color LED – Driven by Target MCU. JP6 must be shunted for +3.3V to be applied to D2 anode. The default shunt for JP6 is a 0Ω resistor installed at JS17.	n/a
D4	Target MCU BOOT0_LED indicator. Reflects the state of Target MCU P1_1. When the boot process fails, D1 will toggle at a 1 Hz rate for 60 seconds. After 60 seconds, the Target MCU is reset.	n/a
D5	Link2 MCU BOOT0_LED indicator. Reflects the state of Link2 MCU P1_1. When the boot process fails, D1 will toggle at a 1 Hz rate for 60 seconds. After 60 seconds, the Link2 MCU is reset. It will be ON when the Link2 MCU is Booting using DFU (See description for JP6).	n/a
D8	Target MCU Power LED.	n/a
D9	Target MCU Reset LED – this LED is on anytime the Target RESETn is pulled low.	n/a
D13	Ethernet link active indication (controlled via LAN8729A)	n/a
D11	Ethernet 100Mbps indication (controlled via LAN8729A)	n/a
J1, J2, J6, J7	Expansion connectors, including Arduino UNO rev3 compatible connectivity.	7
J3	PMod™ (SPI / I2C) Bridge connector. An external Application Processor (AP) or PMod™ peripheral may be	7

Designator	Description	Reference section
	connected to the Target MCU SPI0 and I2C0 via this connector.	
J4	Target MCU Power / USB Device/Host connector. Connect this micro USB A/B-type connector to a +5V power source when it is desired to power only the Target MCU, and leave the on-board Link2 debug probe unpowered. This is useful when an external debug probe is used to debug the Target MCU.  If this target USB port is being used in a USB Host configuration (i.e. powering a USB device plugged into the board), install JP4.	5
J5	<b>CAUTION: Do not install JP4 when applying external power to J4.</b> Link2 micro USB B-type connector. Powers both the Link2 side of the board and Target MCU side of the board. Power the board from this connector when using the on-board debug probe to debug the Target MCU.	5
JP1	SWD VREF power selection – 3 position jumper pins. Jumper 1 – 2 (default) when on-board Target MCU is connected to either the on-board Link2 debug probe or an external debug probe. Jumper 2 – 3 when on-board Link2 debug probe is used to debug an off-board Target MCU.	5
JP2	Target MCU SWD disable – 2-position jumper pins. Jumper open (default) the Target MCU SWD interface enabled. Normal operating mode where the Target SWD is connected to either the on-board Link2 debug probe or an external debug probe. Jumper shunted, the Target MCU SWD interface is disabled and the Target MCU is held in the reset state. Use this setting only when the on-board Link2 debug probe is used to debug an off-board Target MCU.	6
JP3, JP5	These jumpers are used to ISP boot select between booting the Target MCU from the USART, USB or SPI flash when the ISP button is pressed as the board is released from Reset. See Section 8.2 for more information	8.2
JP4	Provides 4.7V power to the Target MCU USB A/B connector. Install JP4 only when the Target MCU is being used as a Host USB controller. <b>CAUTION: Do not install JP4 when the Target MCU is used as a USB Device or anytime external power is applied at J4.</b>	n/a
JP6	Link2 force DFU boot – 2 position jumper pins. Jumper open (default) for Link2 to follow the normal boot sequence. The Link2 will boot from internal flash if image is found there. With the internal flash erased the Link2 normal boot sequence will fall through to DFU boot.	n/a

Designator	Description	Reference section
	Jumper shunted to force the Link2 to DFU boot mode. Use this setting to reprogram the Link2 internal flash with a new image or to use the LPCXpresso IDE with Redlink protocol.	
JP7, JP9	The on-board current measurement circuitry includes a choice of two sense resistors for both the Target and I/O supplies in order to enable more accurate current measurement when the Target MCU is running in low power modes. JP7 and JP9 are used to select short a second sense resistor in the path of the current supplies of the Target and I/O supplies respectively.	5.1.3
JP8, JP10	A current meter may be installed across JP8 terminals to measure the Target MCU core current consumption. Pin 1 (square pad) is positive and pin 2 is negative. By default JP5 is shunted by a 0Ω resistor installed at JS7. Remove the resistor at JS7 to measure current at JP8.  A current meter may be installed across JP10 terminals to measure the Target MCU I/O current consumption. Pin 1 (square pad) is positive and pin 2 is negative. By default JP7 is shunted by a 0Ω resistor installed at JS15. Remove the resistor at JS15 to measure current at JP7.	5.1.2
P1	10-pin SWD connector – The SWD connector is used to debug the Target MCU from an external debug probe. The same SWD connector can also be used to connect the on-board Link2 debug probe to an off-board Target MCU (for this JP1 must shunted 2–3, and JP2 must have a shunt installed).	6
P2, P3	A voltmeter installed across P2 terminals may be used to measure the voltage across a sense resistor (R66, 200 mohm) in order to determine current flow into the target MCU. Pin 1 (square pad) is positive and pin 2 is negative. Similarly, the current flow into the I/O supply of the Target MCU may be determined by measuring the voltage drop across a 3 ohm sense resistor (R77) via the P3 terminals.	5.1.1
P4	FTDI serial header. In addition to provide a serial output from Target MCU, the Target side of the board can be powered from the FTDI header. <b>CAUTION: Users must make sure the GND side of the FTDI cable is connected to PIN1, connecting it in the reverse might damage the MCU.</b>	4.1
SW1	Target MCU WAKEUP pushbutton. When pressed the WAKEUP switch will drive Target MCU WAKEUP0 to a low level, and will wake the part from various SLEEP/POWER_DOWN modes.	8.3
SW2	Target MCU ISP Bootload enable pushbutton. This switch drives Target MCU P2_7 low. Holding SW2 pressed while powering up or resetting and the Target MCU will skip the image in internal flash and proceed with booting based on JP3 settings..	8.2

Designator	Description	Reference section
SW3	Target MCU Reset pushbutton.	8.1
TP1	Ground terminal test point.	n/a
U8	Link2 MCU	n/a
U11	Target MCU	n/a

### 3. Getting Started

By default, the LPCXpresso4367 is configured to use the on-board debug probe (Link2) to debug the on-board target (Target MCU). The Link2 is unprogrammed at manufacture, so will boot into DFU mode. The LPCXpresso IDE (available for free download at <http://www.lpcware.com/lpcxpresso/home>) will automatically load the Redlink debug protocol via DFU, so can be used in the default configuration, i.e. with the Link2 flash unprogrammed. The Link2 On-board Debug Processor's flash memory can also be programmed with CMSIS-DAP or J-link OB protocols using the LPC-Link2 Configuration Tool (LCT) or LPCScript (see <http://www.lpcware.com/LPCUtilities> for more information.) To program the Link2 flash, a shunt must be installed at JP6. After programming the flash, remove JP6 and power cycle the board to force the Link2 to boot with that protocol. These alternate protocols enable the board to be used with tool chains from vendors such as Keil, IAR, Atollic, Rowley and SEGGER. Note that the board can also be used with LPCXpresso IDE when the CMSIS-DAP firmware has been programmed (note that it may be necessary to manually select SWD instead of JTAG from the debug configuration.)

Check with your toolchain vendor for availability of specific device support packs for the LPC4300/43S00/18S00 family of devices.

Installation steps for use with LPCXpresso IDE:

- 1) Download and install the LPCXpresso IDE (version 7.6.2 or later) installer from <http://www.lpcware.com/lpcxpresso/download>.
- 2) Connect the LPCXpresso4367 board to the USB port of your host computer, connecting a micro USB cable to connector J5 ("Link").
- 3) Download the LPCOpen examples & drivers from <http://www.lpcware.com/content/nxpfile/lpcopen-platform>, selecting the version for the toolchain you are using; project files for LPCXpresso IDE, Keil and IAR tools are available.
- 4) Start the LPCXpresso IDE and import the LPCOpen zip file by clicking Import project(s) in the "Start here panel."
- 5) The simplest example is `periph_blinky`, which will blink the tricolor LED on the LPCXpresso4367. Click on the `periph_blinky` in the "Project Explorer" panel, then click Debug 'periph\_blinky' in the "Start here" panel. This will build the project and then launch the debug session.

Note that if the jumper setting of JP6 is changed with the board powered then the USB connection must be removed and reconnected to J5 in order to force the Link2 to reset and enter DFU boot mode and force drivers to enumerate on the host computer running the tools. Redlink protocol is required for multicore debug using the LPCXpresso IDE.



Installation steps for use with Keil and IAR tool chains (using CMSIS-DAP or J-Link OB protocols):

- 1) Program the firmware of the Link2 using the LCT tool or LPCScript, following the instructions provided for those tools. Note that part of this process will involve installing device drivers for the board on Windows platforms.
- 2) Ensuring JP6 is not installed, unplug then reconnect the board to board to the USB port of your host computer, connecting a micro USB cable to connector J5 ("Link").
- 3) Download the LPCOpen examples & drivers from <http://www.lpcware.com/content/nxpfile/lpcopen-platform>, selecting the version for the toolchain you are using; project files for LPCXpresso IDE, Keil and IAR tools are available.
- 4) Import the project file.

## 4. Target MCU Serial ports

By default the Target MCU UART0 is connected to the FTDI header at P4. This can be used for sending debug messages out to a host computer via a suitable cable. The Target MCU UART0 can also be connected through a virtual communication port (VCOM) UART bridge Link2 function to a host computer connected to the USB Link2 (J5).

The Redlink protocol firmware for the Link2 (downloaded by default by the LPCXpresso IDE) includes UART bridge functionality (VCOM support). A version of the CMSIS-DAP Link2 firmware is also available with this functionality (called "CMSIS-DAP with bridges"), and can be programmed into the Link2 using the LPC-Link2 Configuration Tool (LCT), available at <http://www.lpcware.com/LPCUtilities>. When running this firmware the default source of data to the Target MCU RXD is the FTDI header. Once the Link2 receives any data via the VCOM port of a host computer it will set P2\_2 low to select the Link2 UART0 data to the Target MCU. Once the VCOM port has been used it is necessary to power cycle the board before FTDI connection can be used.

### 4.1 P4 FTDI header

The FTDI header P4 mates with FTDI cable TTL-232R-3V3. P4 interfaces the Target MCU UART0 to a Host PC virtual serial port. The P4 location is shown in Fig 2. The pin out and a description of the signals at P4 are listed in Fig 3. By default there may be no header installed at P4.

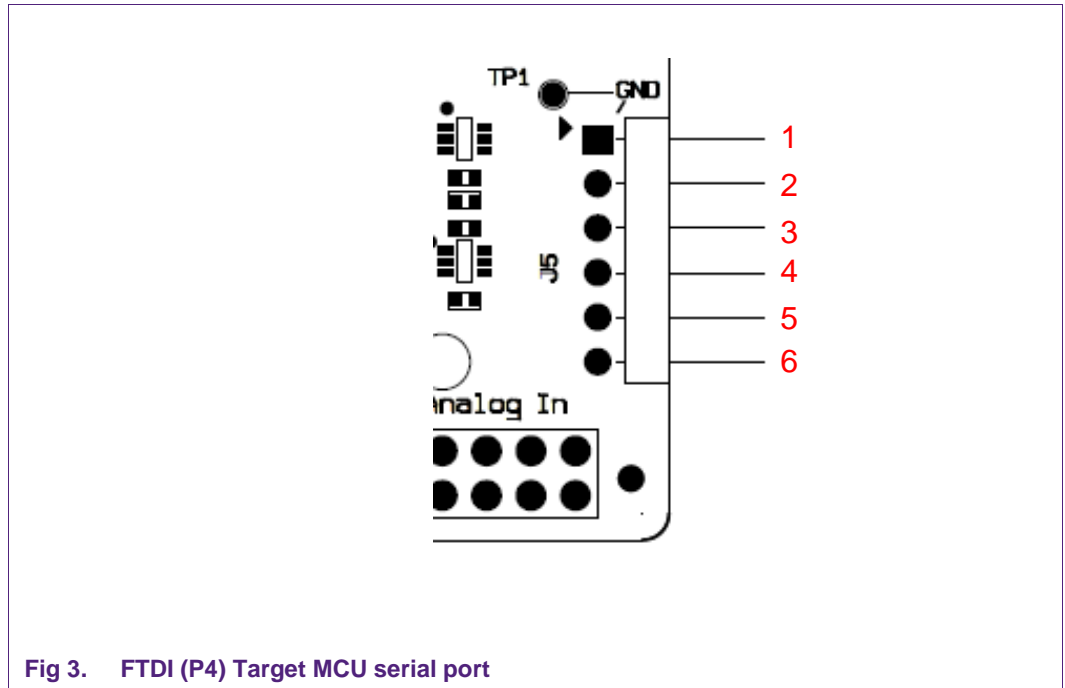


Table 2. P4 FTDI interface

Target MCU Signal	FTDI Signal	Pin #	Direction
GND	GND	1	
No connect	CTS	2	
Board +5V	5V	3	
UART0_RXD	TXD	4	From host
UART0_TXD	RXD	5	To host
No connect	RTS	6	

## 5. Board power connections & measurement

The LPCXpresso4367 board requires +5V input to power the on-board voltage regulators which in turn power the Link2 debug probe and other +3.3V circuits, the Target MCU and the Arduino +5V and +3.3V power rails. When the main external power source is from the Link2 side USB micro B-type connector (J5), both the Link side and Target MCU sections of the board are powered. When the main external power is from the Target side USB micro B-type connector (J4) or FTDI header (P4) only the Target MCU section of the board is powered.

When the Target MCU is to be debugged from an external debug probe, instead of the on-board Link2 debug probe, the Link USB connector (J5) must be disconnected.

### 5.1 Target MCU current measurement

The Target MCU current can be determined by measuring the voltage across a sense resistor in series with the supply, using a current meter or using the built-in power measurement circuitry with the LPCXpresso IDE tools. Each of these methods will be described in subsections below. There is no current monitoring of the Link section circuits on the board.

#### 5.1.1 Target MCU current measurement using voltage sense resistor

The voltage across a series 200m $\Omega$  resistor with the Target MCU Core VDD can be manually measured at P2 on the PCB. The voltmeter positive probe is applied to P2 pin 1 (square pad) and negative probe to P2 pin 2. Use Ohm's law to calculate the current (Target MCU current = measured voltage / 0.2).

The voltage across a series 3 $\Omega$  resistor with the Target MCU I/O VDD can be manually measured at P3 on the PCB. The voltmeter positive probe is applied to P3 pin 1 (square pad) and negative probe to P3 pin 2. Use Ohm's law to calculate the current (Target MCU current = measured voltage / 3).

#### 5.1.2 Target MCU VDD and VDD I/O current measurement using a current meter

A current meter may be installed across JP5 to measure the Target MCU VDD input current. The 0 $\Omega$  resistor at JS11 must be removed and the current meter connected at the positive input at JP5 pin 1 (square pad) and negative input at JP5 pin 2.

A current meter may be installed across JP7 to measure the Target MCU I/O VDD input current. The 0 $\Omega$  resistor at JS14 must be removed and the current meter connected at the positive input at JP7 pin 1 (square pad) and negative input at JP7 pin 2.

#### 5.1.3 Built-in current measurement

The LPCXpresso4367 includes an on-board current measurement system consisting of a pair of amplifiers and a fast, 2 channel ADC, which is controlled by the on-board Link2 debug probe. Each amplifier measures the voltage drop across of two series resistors, one pair of resistors being in line with the Target MCU supply and one in line with the I/O supply. By default, one of the series resistors in each of these circuits is shorted by (JP7 for Target supply, JP9 for I/O supply) in order to allow the ADC to measure up to 235mA (Target supply) / 32mA (I/O supply) without the ADC input saturating. JP7 can be removed to make more accurate measurements when the Target MCU is consuming 52mA or less, and/or JP9 can be removed if the I/O supply current is 32mA or less. Note that the current measurement system will not be damaged if the amplifier outputs saturate.

Table 3. Current measurement system range selection

Jumper	Position	Supply	Current range
JP7	Shunted (default)	Target	58uA-235mA
JP7	Open	Target	12.6uA-52mA
JP9	Shunted (default)	I/O	8uA-32mA
JP9	Open	I/O	4uA-16mA

The ADC can sample the amplifier out at up to 200k samples/second, configurable under control of the Link2 probe.

The current measurement system is supported by version 8.0 and later versions of the LPCXpresso IDE, which includes controls to select sample rate and enter the sense resistor values selected by JP7 and JP9.

## 6. Debug Configurations

The LPCXpresso4367 board has a built-in debug probe known as Link2, implemented in an LPC43xx MCU. The Target MCU can be debugged by the on-board Link debugging probe, or from an external debug probe installed at P1. On-board jumpers JP1 and JP2 must be correctly positioned for each mode. The on-board Link debug probe is capable of debugging target MCU's with a VDDIO range  $3.3V \pm 10\%$ . Check the sections below for the appropriate jumper settings and how to properly power the board.

### 6.1 Debugging on-board Target MCU using on-board debug probe

To use the on-board Link debug probe, the LPCXpresso4367 board must be powered from the Link2 USB connector J5, and jumper JP2 must be fitted in position pin 1 - 2 (Local Target). Jumper JP1 must be open to enable the Target MCU. Connecting the micro USB J5 to a host computer will power the Link and Target sections of the board and provide the USB link to the debug tool software.

### 6.2 Debug on-board Target MCU using external debug probe

To use an external debug probe, connect the probe to the SWD (P1) connector, power the Target MCU section of the board from the Target power only micro USB connector J4, and fit a jumper to JP2 across pin 1 - 2 (Local Target). Jumper JP1 must be open to enable the Target MCU. The on-board Link debug probe must be unpowered, by leaving J5 unconnected.

### 6.3 Using on-board Link2 to debug an off-board target LPC MCU

The LPCXpresso4367 board's Link2 debug probe may be used to debug an off-board target MCU. The on-board Link debug probe is capable of debugging target MCU's with a VDDIO range of  $3.3V \pm 10\%$ . To keep the on-board Target MCU from interfering with the SWD interface, JP1 must be fitted. The Link2 debug probe SWD is connected by a ribbon cable between the P1 connector to the off-board target MCU SWD interface. Power the LPCXpresso4367 board from the Link USB connector J5, and jumper JP2 must be fitted across pins 2 - 3 (External Target.)

## 7. Expansion connectors

The LPCXpresso4367 board includes four expansion connectors plus a PMod™ compatible connector (J3). The expansion connectors (J1, J2, J6 and J7) incorporate an Arduino Uno revision 3 footprint in their inner rows. Not all connector locations are populated on the expansion connectors since the Target MCU does not have enough I/O to utilize all of the available connections (additional pin locations are provided for compatibility with future LPCXpresso boards.)

Table 4. Expansion Connectors

Reference	Description
J1	The odd number pins are compatible with Arduino Uno rev3 Digital 15:8, AREF, SDA & SCL connector. The even numbered pins are used for external access and expansion of Target MCU signals not used by the Arduino Uno rev3 compatible interface.
J2	The odd numbered pins 1 – 15 are compatible with Arduino Uno rev3 Digital 7:0 connector. The even numbered pins, and odd numbered pins 17 and 19, are used for external access and expansion of Target MCU signals not used by the Arduino Uno rev3 compatible interface.
J3	PMod™ connector. Connected to the Target MCU SPI0 and I2C2.
J6	The even numbered pins 6 – 20 are compatible with Arduino Uno rev3 Power connector. The odd number pins are used for external access and expansion of Target MCU signals not used by the Arduino Uno rev3 compatible interface.
J7	The even numbered pins 2 – 12 are compatible with Arduino Uno rev3 Analog connector. The odd numbered pins are used for external access and expansion of Target MCU signals not used by the Arduino Uno rev3 compatible interface.

## 8. Buttons

The LPCXpresso4367 board has 3 push buttons available to control the operation of the Target MCU (target) MCU. Their functions are as described below.

### 8.1 Reset

This button is used to reset the Target MCU.

### 8.2 ISP

This button connects to the Target MCU P2\_7 pin and may be used to force the TARGET MCU into ISP boot mode. To force ISP boot, hold the ISP button down while pressing and releasing the reset button. The ISP mode selected when using this function is determined by JP3 and JP5, as shown below.

Table 5. ISP boot mode selection

Mode	JP3	JP5	JP11
SW2 not pressed – Flash boot	X	x	x

Mode	JP3	JP5	JP11
ISP USB	Open	Open	x
ISP SPIFI	Open	Fitted	x
ISP USART0	Fitted	Fitted	Fitted at 1-2

This can be useful when the TARGET MCU flash has been programmed with code that disables the SWD debug pins or changes timing settings such that the debug probe has problems communicating with it.

The ISP button can also be used to trigger an interrupt by configuring the P2\_7 pin and associated interrupt controls within your application code.

### 8.3 WAKEUP

Depressing this button triggers a wake interrupt by pulling down the WAKEUP0 input of the TARGET MCU.

## 9. A7001CM Secure Element (LPCXpresso43S67/18S37 only)

---

The LPCXpresso43S67 boards feature an A7001CM Secure Element device – a specific integrated circuit for handling and storing secured data. The Secure Element features non-volatile memory, a security CPU and crypto coprocessor and features additional security measures to protect it against tampering and attacks. The A7001CM device is interfaced to the LPC43S67 I<sup>2</sup>C (I2C0 by default, with an option to move to I2C1 by moving solder jumpers JS3 and JS4 from position 1-2 to position 3-4.)

Contact NXP Semiconductors for more information on third party software solutions for the LPC43S67 that utilize the A7001CM device.

## 10. Legal information

### 10.1 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned

application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Evaluation products** — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

### 10.2 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

**LPCXpresso** — is a trademark of NXP B.V.



## 11. List of figures

---

Fig 1.	LPCXpresso43xx/18xx .....	3
Fig 2.	Board layout.....	5
Fig 3.	FTDI (P4) Target MCU serial port .....	10

## 12. List of tables

---

Table 1.	Connectors, indicators and jumpers.....	5
Table 2.	P4 FTDI interface.....	10
Table 3.	Current measurement system range selection	12
Table 4.	Expansion Connectors.....	13
Table 5.	ISP boot mode selection.....	13

## 13. Contents

---

<b>1.</b>	<b>Introduction .....</b>	<b>3</b>
<b>2.</b>	<b>Feature summary .....</b>	<b>4</b>
2.1	Board layout and settings.....	4
<b>3.</b>	<b>Getting Started .....</b>	<b>8</b>
<b>4.</b>	<b>Target MCU Serial ports.....</b>	<b>9</b>
4.1	P4 FTDI header.....	9
<b>5.</b>	<b>Board power connections &amp; measurement.....</b>	<b>11</b>
5.1	Target MCU current measurement.....	11
5.1.1	Target MCU current measurement using voltage sense resistor.....	11
5.1.2	Target MCU VDD and VDD I/O current measurement using a current meter .....	11
5.1.3	Built-in current measurement .....	11
<b>6.</b>	<b>Debug Configurations.....</b>	<b>12</b>
6.1	Debugging on-board Target MCU using on-board debug probe .....	12
6.2	Debug on-board Target MCU using external debug probe .....	12
6.3	Using on-board Link2 to debug an off-board target LPC MCU.....	12
<b>7.</b>	<b>Expansion connectors .....</b>	<b>13</b>
<b>8.</b>	<b>Buttons.....</b>	<b>13</b>
8.1	Reset.....	13
8.2	ISP .....	13
8.3	WAKEUP.....	14
<b>9.</b>	<b>A7001CM Secure Element (LPCXpresso43S67/18S37 only).....</b>	<b>15</b>
<b>10.</b>	<b>Legal information .....</b>	<b>16</b>
10.1	Disclaimers.....	16
10.2	Trademarks.....	16
<b>11.</b>	<b>List of figures.....</b>	<b>17</b>
<b>12.</b>	<b>List of tables .....</b>	<b>18</b>
<b>13.</b>	<b>Contents.....</b>	<b>19</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in the section 'Legal information'.

---

© NXP B.V. 2015.

All rights reserved.

For more information, please visit: <http://www.nxp.com>  
For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 18 November 2015

Document identifier: UM10946

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [NXP](#) manufacturer:*

Other Similar products are found below :

[MC13211R2](#) [P2020COME-DS-PB](#) [P5020NXE7TNB](#) [LFSTBEB865X](#) [CLF1G0060S-10U](#) [P5020NXE1TNB](#) [MPC875CZT66](#)  
[MPC8241LZQ200D](#) [MPC852TVR80A](#) [MCIMX6G1AVM05AA](#) [SPC5742PK1MLQ5](#) [MC33399PEFR2](#) [PCA9551PW,112](#) [74ABT00DB,118](#)  
[MPC859DSLVR66A](#) [PUSBM15VX4-TL,115](#) [MPC852TCVR80A](#) [CBT3306D-Q100J](#) [MC34708VMR2](#) [MC34825EPR2](#) [IP4048CX5/LF,135](#)  
[74AUP1Z04GF,132](#) [PMP4201G,135](#) [PCF8583P](#) [MC68340AB16E](#) [EVBCRTOUCH](#) [MC9S08PT16AVLC](#) [MC9S08PT8AVTG](#)  
[MC9S08SH32CTL](#) [MCF54415CMJ250](#) [MCIMX6Q-SDB](#) [MCIMX6SX-SDB](#) [74ALVC125BQ,115](#) [74HC4050N](#) [74HC4514N](#)  
[MK21FN1M0AVLQ12](#) [FRDM-KW40Z](#) [FRDM-MC-LVBLDC](#) [PMF63UNEX](#) [PSMN026-80YS,115](#) [PSMN4R0-60YS,115](#)  
[PTN3460IBSF1MP](#) [HEF4028BPN](#) [RAPPID-567XFSW](#) [MPC565MVR56](#) [MPC574XG-176DS](#) [MPC860PCVR66D4](#) [BT137-600E](#) [BUK7628-100A118](#) [P2020NXE2HHC](#)