DATA SHEET

PCF8576
Universal LCD driver for low multiplex rates

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Philips
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CONTENTS

Universal LCD driver for low multiplex rates PCF8576

1 FEATURES

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, ½ or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- Optimized pinning for plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic very small outline package (VSO56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8576T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8576U	–	chip in tray	–
PCF8576U/2	–	chip with bumps in tray	–
PCF8576U/5	–	unsawn wafer	–
PCF8576U/10	FFC	chip on film frame carrier (FFC)	–
PCF8576U/12	FFC	chip with bumps on film frame carrier (FFC)	–

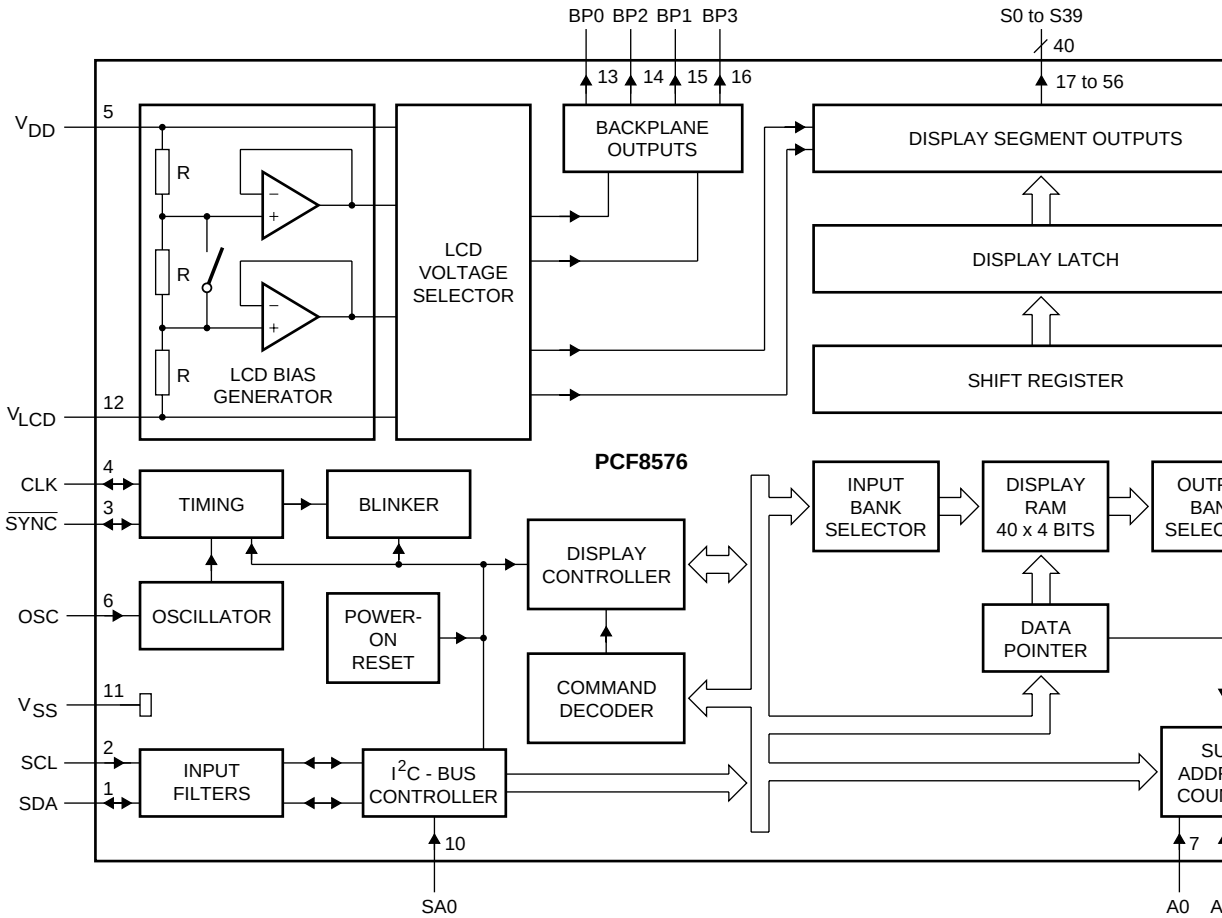


Fig.1 Block diagram (for VSO56 package; SOT190-1).

5 PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I^2C-bus serial data input/output
SCL	2	I^2C-bus serial clock input
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	external clock input/output
V_{DD}	5	supply voltage
OSC	6	oscillator input
A0 to A2	7 to 9	I^2C-bus subaddress inputs
SA0	10	I^2C-bus slave address input; bit 0
V_{SS}	11	logic ground
V_{LCD}	12	LCD supply voltage
BP0, BP2, BP1 and BP3	13 to 16	LCD backplane outputs
S0 to S39	17 to 56	LCD segment outputs

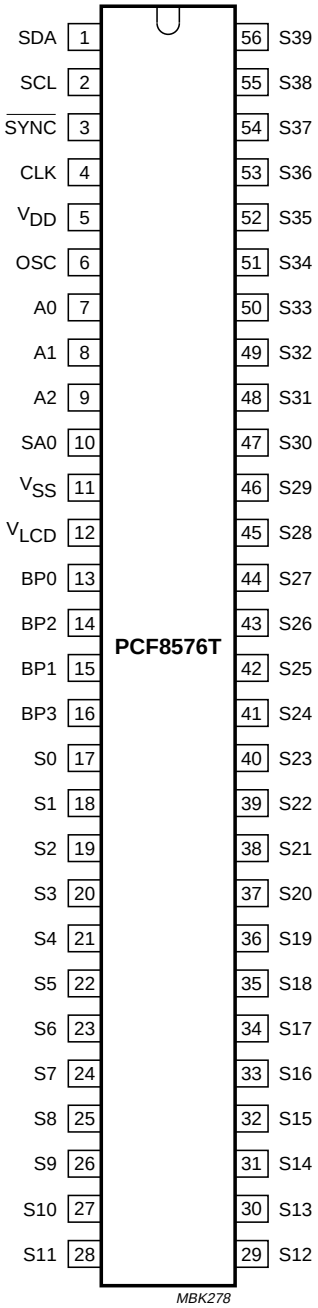


Fig.2 Pin configuration; SOT190-1.

6 FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface to any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table .

All of the display configurations given in Table can be implemented in the typical system shown in Fig.3.

The host microprocessor/microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8576. The internal oscillator is selected by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel chosen for the application.

Selection of display configurations

NUMBER OF		7-SEGMENTS NUMERIC		14-SEGMENTS ALPHANUMERIC		DOT MATRIX
BACKPLANES	SEGMENTS	DIGITS	INDICATOR SYMBOLS	CHARACTERS	INDICATOR SYMBOLS	
4	160	20	20	10	20	160 dots (4 × 40)
3	120	15	15	8	8	120 dots (3 × 40)
2	80	10	10	5	10	80 dots (2 × 40)
1	40	5	5	2	12	40 dots (1 × 40)

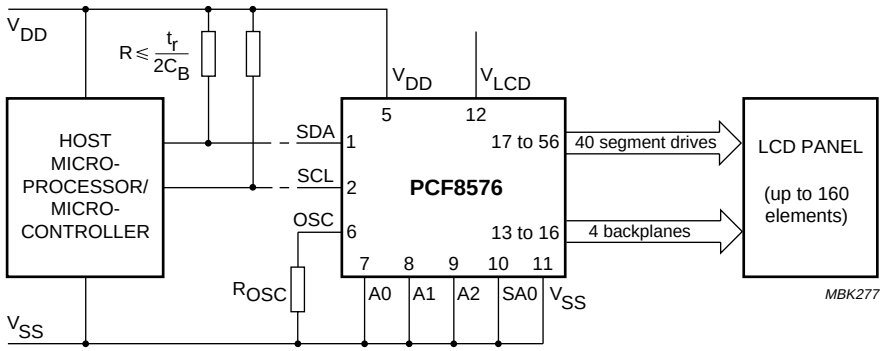


Fig.3 Typical system configuration.

6.1 Power-on reset

At power-on the PCF8576 resets to a starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with $\frac{1}{3}$bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 4).
6. The I^2C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of the circuit to provide a $\frac{1}{2}$bias voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 1.

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} > 3V_{th}$ approximately.

Multiplex drive ratios of 1 : 3 and 1 : 4 with $\frac{1}{2}$bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3}$ = 1.732 for 1 : 3 multiplex or $\frac{\sqrt{21}}{3}$ = 1.528 for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage V_{op} as follows:

- 1 : 3 multiplex ($\frac{1}{2}$bias):

  $V_{op} = \sqrt{6} \times V_{off\langle rms\rangle} = 2.449\ V_{off(rms)}$

- 1 : 4 multiplex ($\frac{1}{2}$bias):

  $V_{op} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when $\frac{1}{3}$bias is used.

Table 1 Preferred LCD drive modes: summary of characteristics

LCD DRIVE MODE	NUMBER OF		LCD BIAS CONFIGURATION	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
	BACKPLANES	LEVELS				
static	1	2	static	0	1	∞
1 : 2	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1 : 2	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1 : 3	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1 : 4	4	4	$\frac{1}{3}$	0.333	0.577	1.732

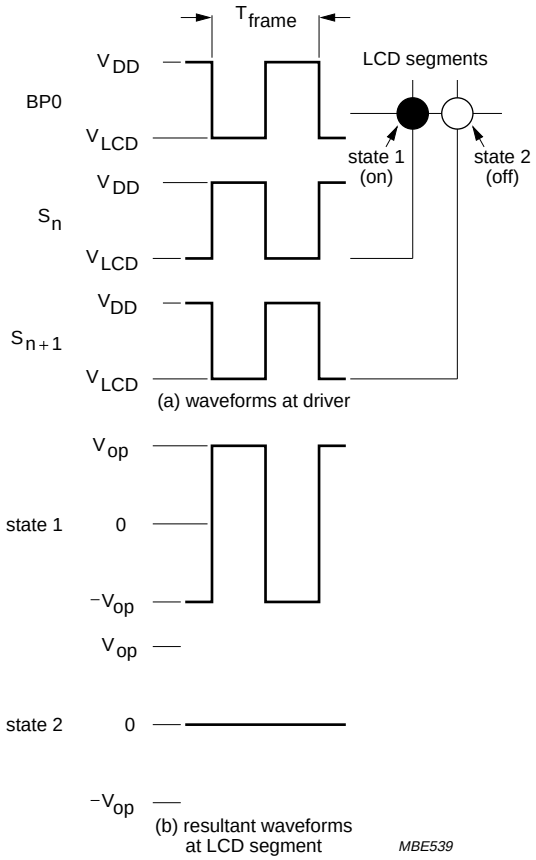
6.4 LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.4.

When two backplanes are provided in the LCD, the 1 : 2 multiplex mode applies. The PCF8576 allows use of ½bias or ⅓bias in this mode as shown in Figs 5 and 6.

When three backplanes are provided in the LCD, the 1 : 3 multiplex drive mode applies, as shown in Fig.7.

When four backplanes are provided in the LCD, the 1 : 4 multiplex drive mode applies, as shown in Fig.8.



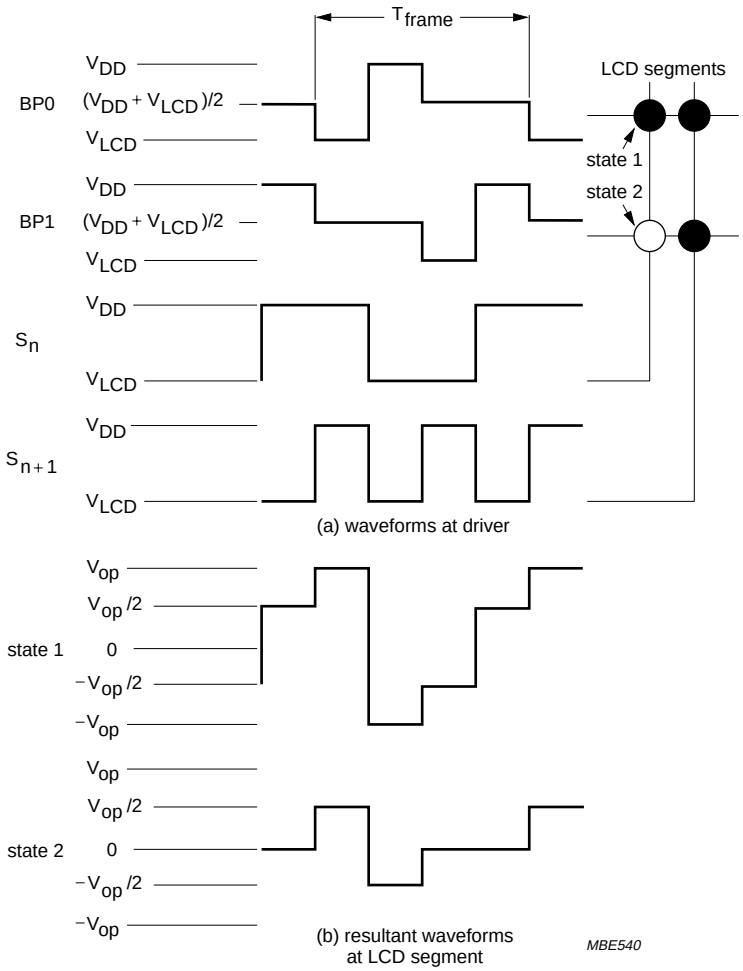
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

$V_{state2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig.4 Static drive mode waveforms ($V_{op} = V_{DD} - V_{LCD}$).



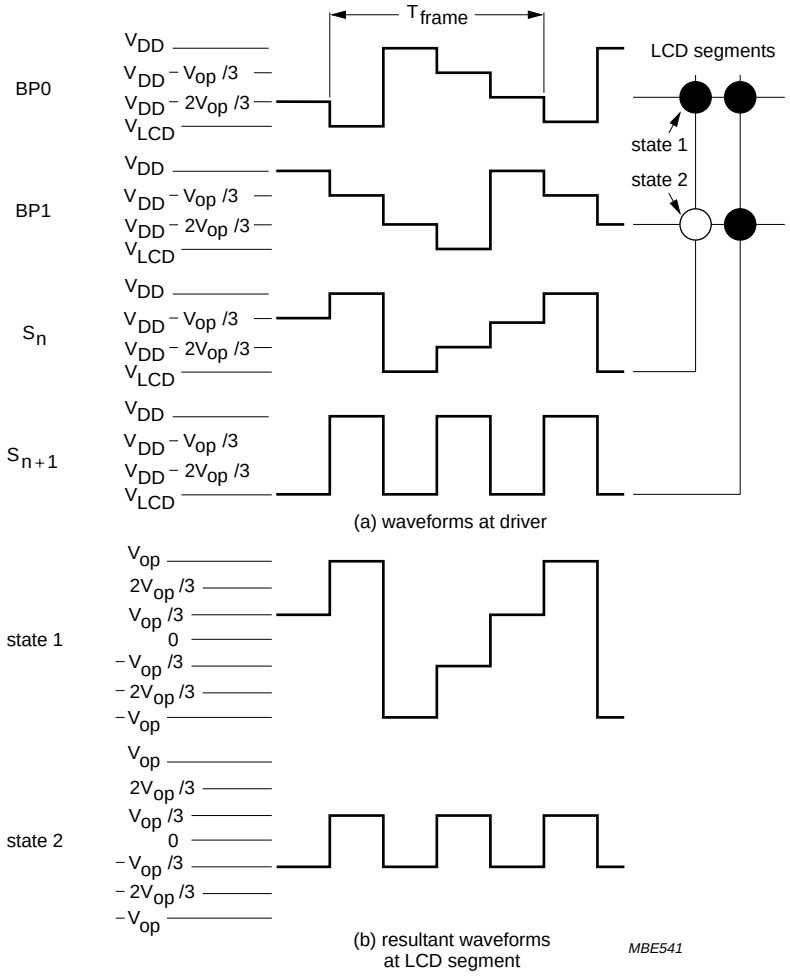
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.791V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.354V_{op}$

Fig.5 Waveforms for the 1 : 2 multiplex drive mode with ½bias ($V_{op} = V_{DD} - V_{LCD}$).



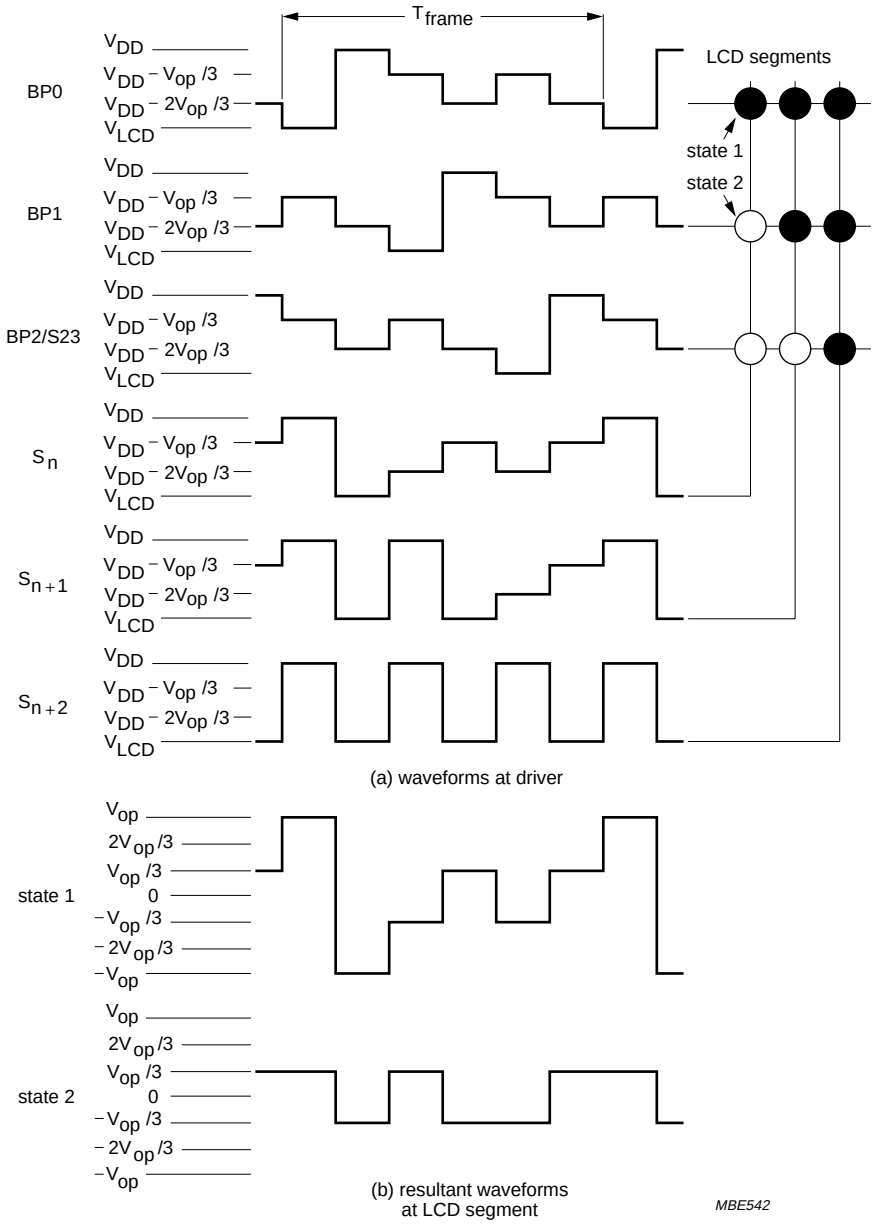
$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.745V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.6 Waveforms for the 1 : 2 multiplex drive mode with ⅓bias ($V_{op} = V_{DD} - V_{LCD}$).



$V_{state1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = 0.638V_{op}$

$V_{state2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = 0.333V_{op}$

Fig.7 Waveforms for the 1 : 3 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

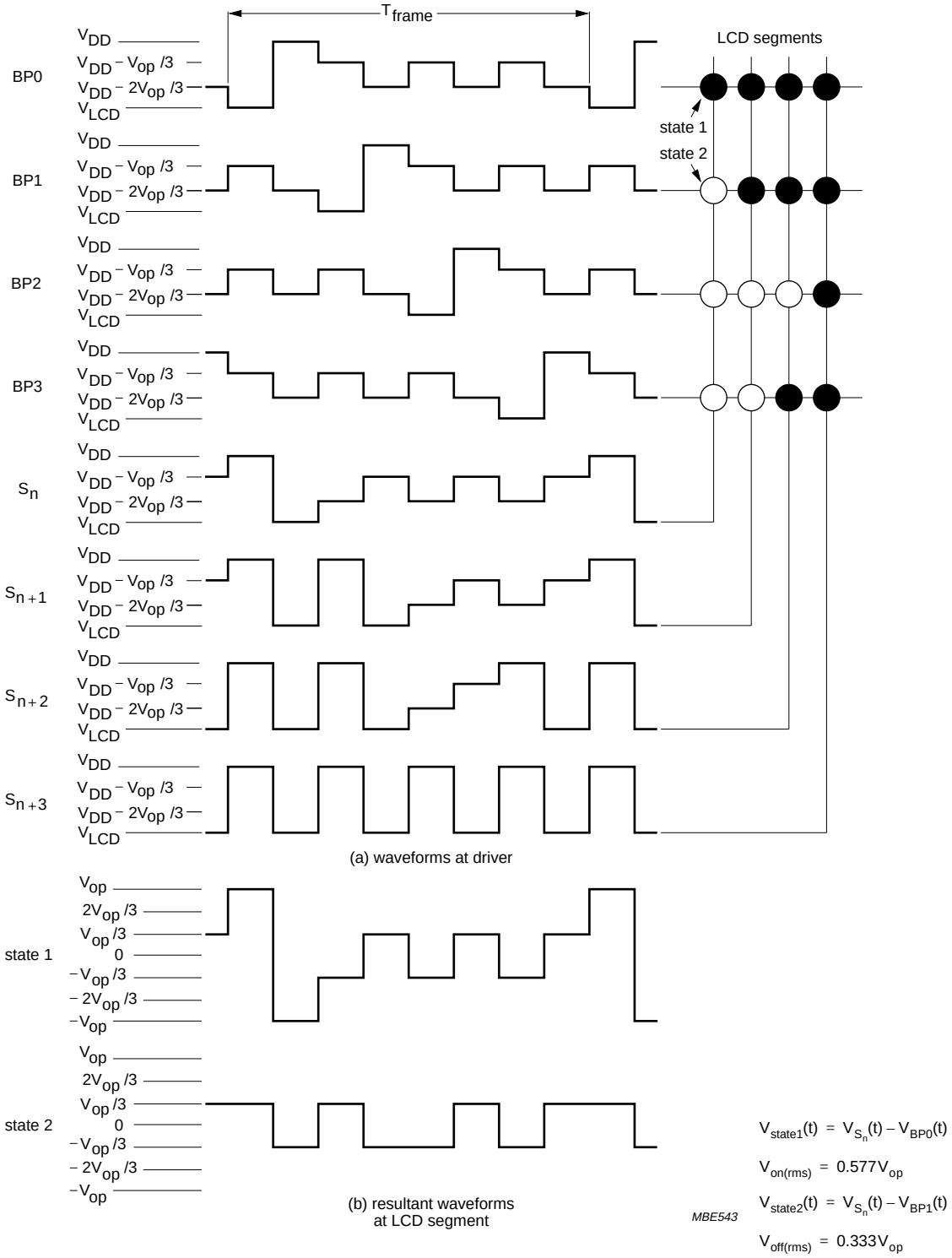


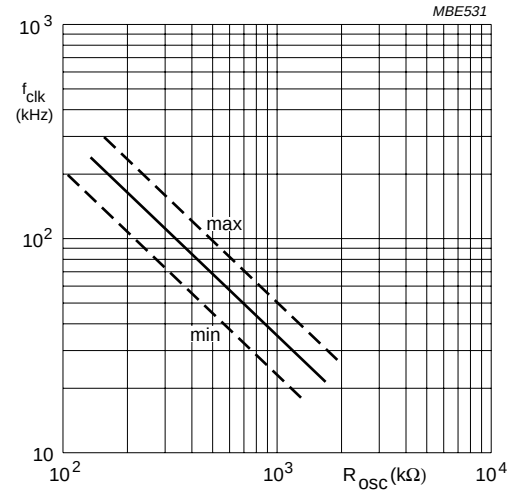
Fig.8 Waveforms for the 1 : 4 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

6.5 Oscillator

6.5.1 INTERNAL CLOCK

The internal logic and the LCD drive signals of the PCF8576 are timed either by the internal oscillator or from an external clock. When the internal oscillator is used, pin OSC should be connected to pin V_{SS}. In this event, the output from pin CLK provides the clock signal for cascaded PCF8566s in the system.

Where resistor R_{osc} to V_{SS} is present, the internal oscillator is selected. The relationship between the oscillator frequency on pin CLK (f_{clk}) and R_{osc} is shown in Fig.9.



$$f_{clk} \approx \left(\frac{3.4 \times 10^7}{R_{osc}}\right)(kHz)$$

Fig.9 Oscillator frequency as a function of R_{osc}.

6.5.2 EXTERNAL CLOCK

The condition for external clock is made by connecting pin OSC to pin V_{DD}; pin CLK then becomes the external clock input.

The clock frequency (f_{clk}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C-bus. To allow I^2C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (see Table 2). The frame frequency is set by the MODE SET commands when internal clock is used, or by the frequency applied to pin CLK when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C-bus.

When a device is unable to digest a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C-bus but no data loss occurs.

Table 2 LCD frame frequencies

PCF8576 MODE	FRAME FREQUENCY	NOMINAL FRAME FREQUENCY (Hz)
Normal mode	$\frac{f_{clk}}{2880}$	64
Power-saving mode	$\frac{f_{clk}}{480}$	64

6.7 Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.8 Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

6.9 Segment outputs

The LCD drive section includes 40 segment outputs pins S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open-circuit.

6.10 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be connected together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

6.11 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (see Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8576 the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

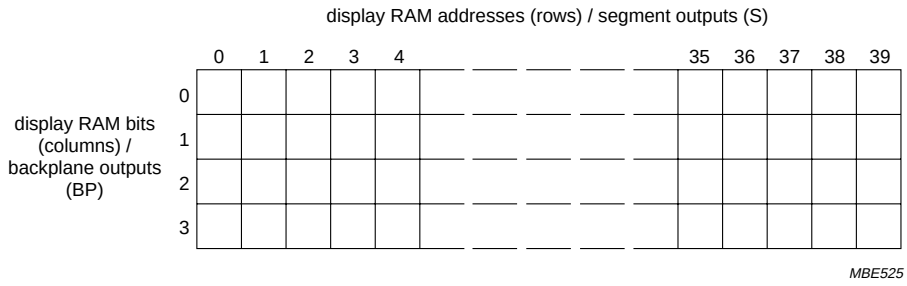


Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

6.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

6.13 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

6.14 Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.15 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independent of the output bank selector.

6.16 Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 3.

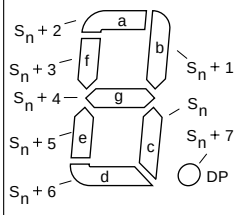
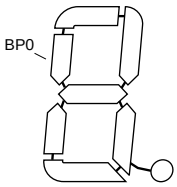
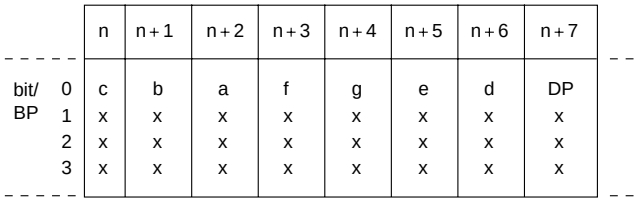
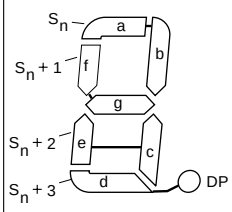
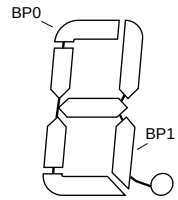
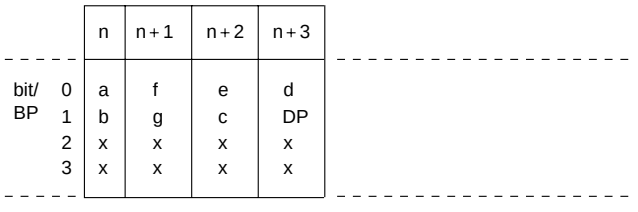
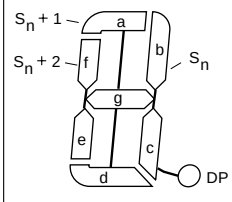
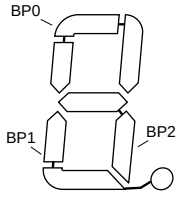
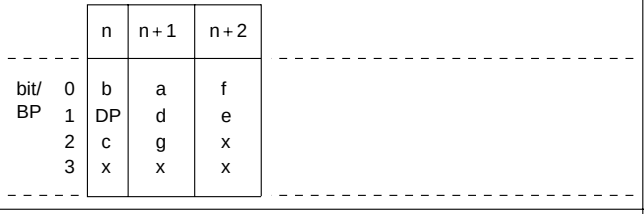
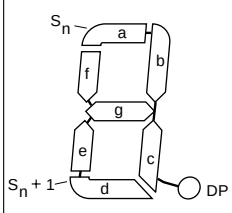
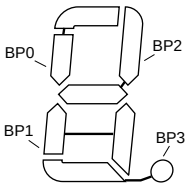
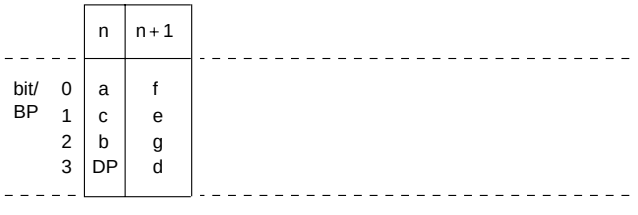
An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 3 Blinking frequencies

BLINKING MODE	NORMAL OPERATING MODE RATIO	POWER-SAVING MODE RATIO	NOMINAL BLINKING FREQUENCY
Off	–	–	blinking off
2 Hz	$\frac{f_{clk}}{92160}$	$\frac{f_{clk}}{15360}$	2 Hz
1 Hz	$\frac{f_{clk}}{184320}$	$\frac{f_{clk}}{30720}$	1 Hz
0.5 Hz	$\frac{f_{clk}}{368640}$	$\frac{f_{clk}}{61440}$	0.5 Hz

drive mode	LCD segments	LCD backplanes	display RAM filling order	tra
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

x = data bit unchanged.

Fig.11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted ov

7 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer (see Fig.12)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

7.2 START and STOP conditions (see Fig.13)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

7.3 System configuration (see Fig.14)

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

7.4 Acknowledge (see Fig.15)

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

7.5 PCF8576 I²C-bus controller

The PCF8576 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally connected to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are connected to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line to LOW until its internal operations are completed. This is known as the ‘clock synchronization feature’ of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576. The least significant bit of the slave address that a PCF8576 will respond to is defined by the level connected at its input pin SA0. Therefore, two types of PCF8576 can be distinguished on the same I²C-bus which allows:

- Up to 16 PCF8576s on the same I²C-bus for very large LCD applications
- The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Fig.16. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel with the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8576. After the last display byte, the I^2C-bus master issues a STOP condition (P).

7.8 Command decoder

The command decoder identifies command bytes that arrive on the I^2C-bus. All available commands carry a continuation bit C in their most significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8576 are defined in Table 4.

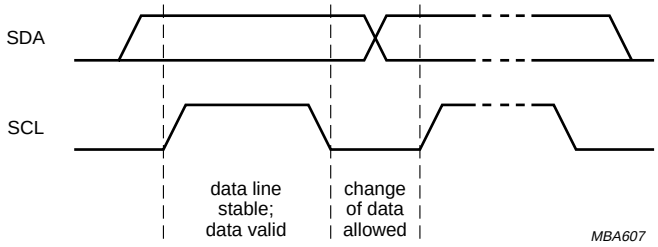


Fig.12 Bit transfer.

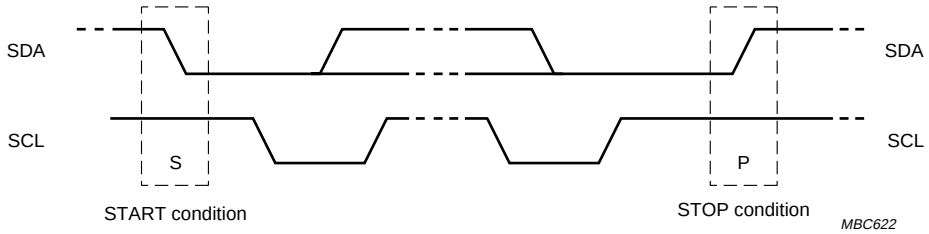


Fig.13 Definition of START and STOP conditions.

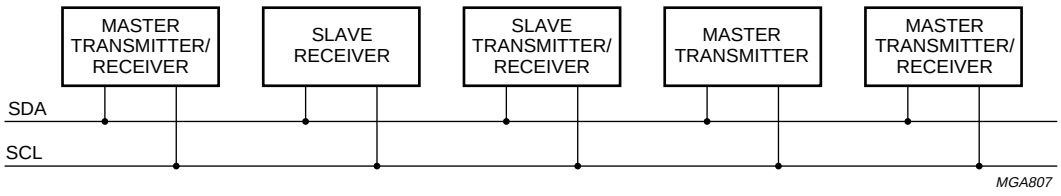


Fig.14 System configuration.

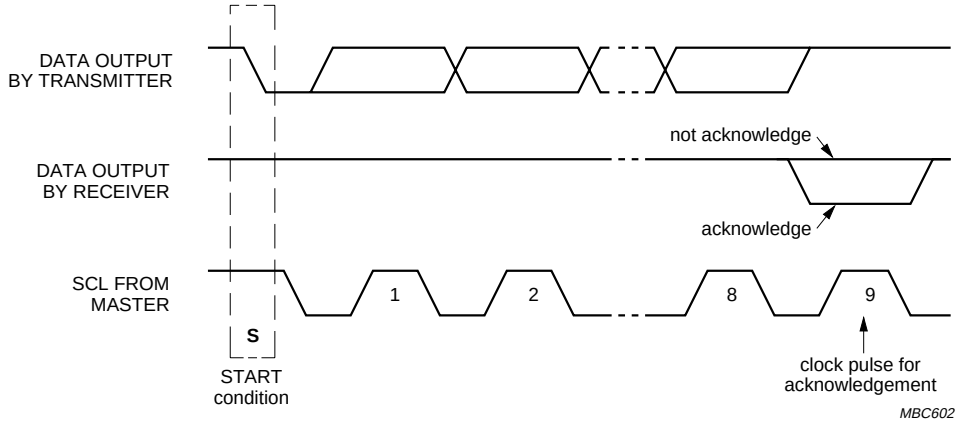


Fig.15 Acknowledgement on the I^2C-bus.

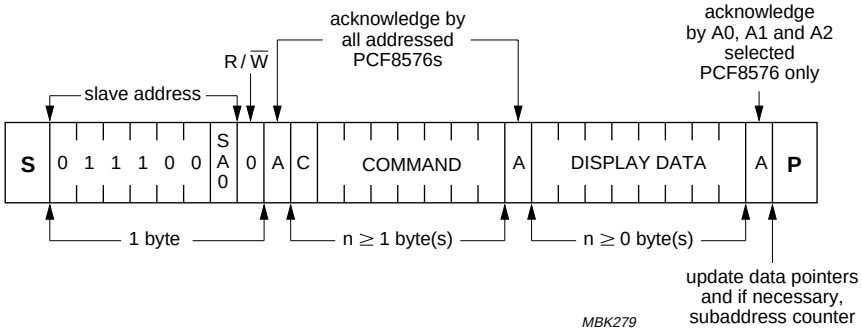
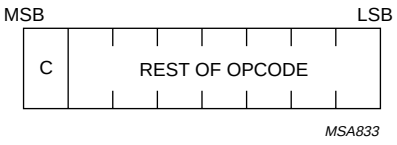


Fig.16 I^2C-bus protocol.



C = 0; last command.
C = 1; commands continue.

Fig.17 General format of command byte.

Table 4 Definition of PCF8576 commands

COMMAND	OPCODE	OPTIONS	DESCRIPTION
MODE SET	C 1 0 LP E B M1 M0	Table 5	Defines LCD drive mode.
		Table 6	Defines LCD bias configuration.
		Table 7	Defines display status. The possibility to disable the display allows implementation of blinking under external control.
		Table 8	Defines power dissipation mode.
LOAD DATA POINTER	C 0 P5 P4 P3 P2 P1 P0	Table 9	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses.
DEVICE SELECT	C 1 1 0 0 A2 A1 A0	Table 10	Three bits of immediate data, bits A2 to A0, are transferred to the subaddress counter to define one of eight hardware subaddresses.
BANK SELECT	C 1 1 1 1 0 I O	Table 11	Defines input bank selection (storage of arriving display data).
		Table 12	Defines output bank selection (retrieval of LCD display data). The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.
BLINK	C 1 1 1 0 A BF1 BF0	Table 13	Defines the blinking frequency.
		Table 14	Selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.

Table 5 MODE SET option 1

LCD DRIVE MODE		BITS	
DRIVE MODE	BACKPLANE	M1	M0
Static	1 BP	0	1
1 : 2	MUX (2 BP)	1	0
1 : 3	MUX (3 BP)	1	1
1 : 4	MUX (4 BP)	0	0

Table 6 MODE SET option 2

LCD BIAS	BIT B
$\frac{1}{3}$bias	0
$\frac{1}{2}$bias	1

Table 7 MODE SET option 3

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 8 MODE SET option 4

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 9 LOAD DATA POINTER option 1

DESCRIPTION	BITS					
6-bit binary value of 0 to 39	P5	P4	P3	P2	P1	P0

Table 10 DEVICE SELECT option 1

DESCRIPTION	BITS		
3-bit binary value of 0 to 7	A2	A1	A0

Table 11 BANK SELECT option 1

STATIC	1 : 2 MUX	BIT I
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 12 BANK SELECT option 2

STATIC	1 : 2 MUX	BIT O
RAM bit 0	RAM bits 0 and 1	0
RAM bit 2	RAM bits 2 and 3	1

Table 13 BLINK option 1

BLINK FREQUENCY	BITS	
	BF1	BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 14 BLINK option 2

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

7.9 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and co-ordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

7.10 Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0). When cascaded PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Fig.18).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the Power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig.19.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see Chapter 12.

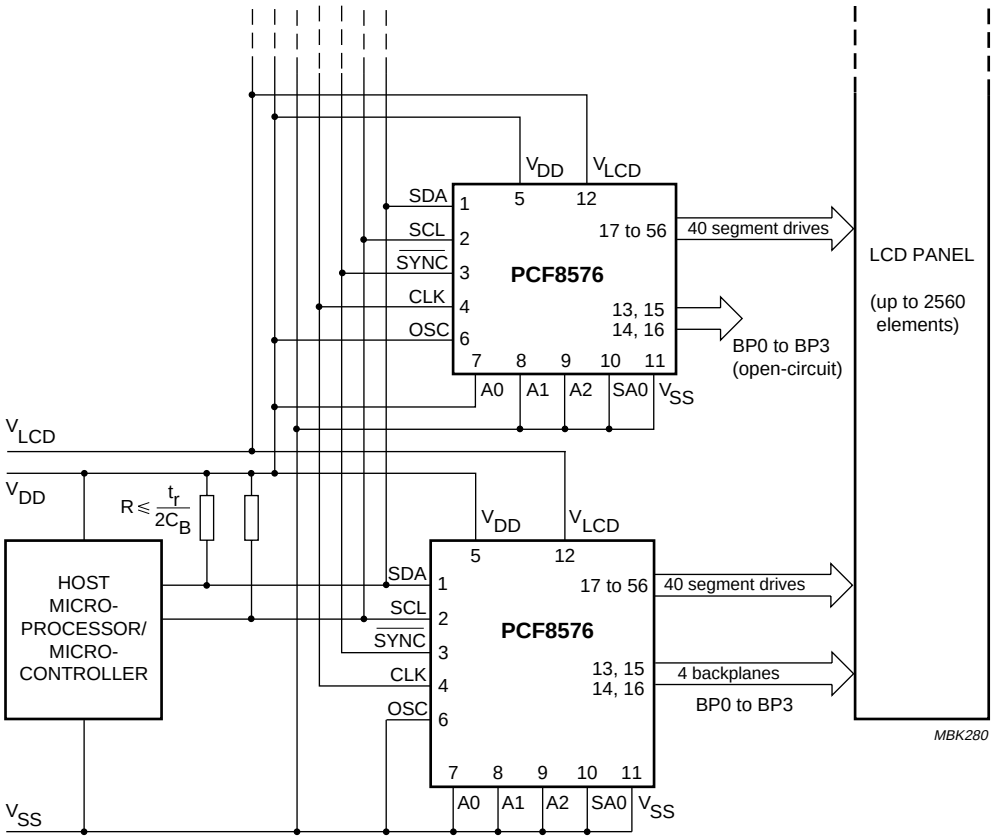
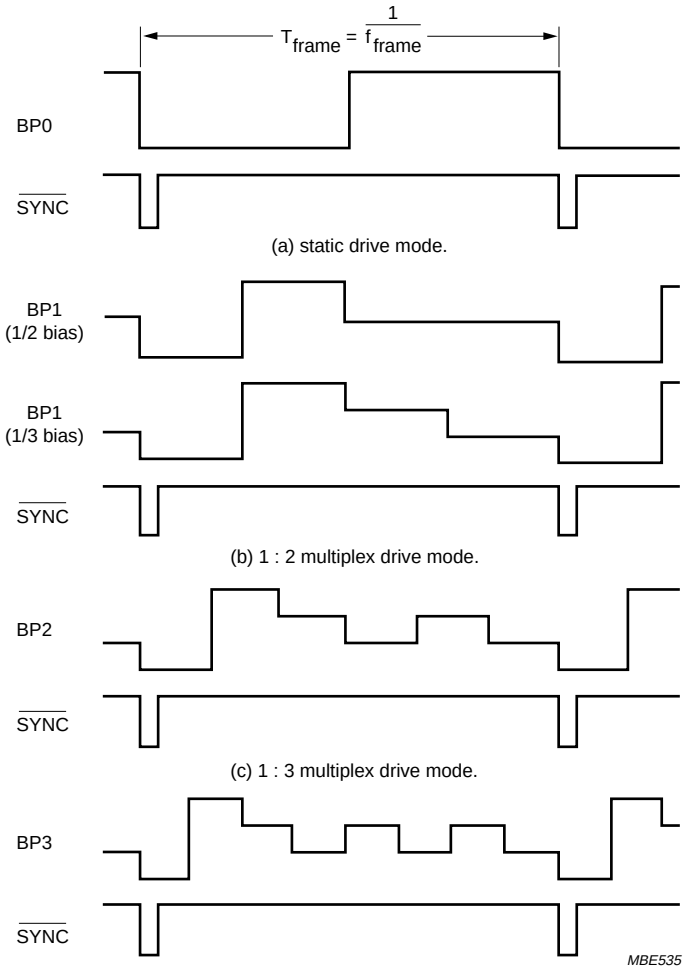


Fig.18 Cascaded PCF8576 configuration.



Excessive capacitive coupling between SCL or CLK and $\overline{SYNC}$ may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig.19 Synchronization of the cascade for the various PCF8576 drive modes.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+11.0	V
V_{LCD}	LCD supply voltage	V_{DD} – 11.0	V_{DD}	V
V_I	input voltage SDA, SCL, CLK, $\overline{SYNC}$, SA0, OSC, A0 to A2	V_{SS} – 0.5	V_{DD} + 0.5	V
V_O	output voltage S0 to S39, BP0 to BP3	V_{LCD} – 0.5	V_{DD} + 0.5	V
I_I	DC input current	–	20	mA
I_O	DC output current	–	25	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	–	50	mA
P_{tot}	total power dissipation	–	400	mW
P_O	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS Devices”*).

10 DC CHARACTERISTICS

V_{DD} = 2 to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2	–	9	V
V_{LCD}	LCD supply voltage	note 1	V_{DD} − 9	–	V_{DD} − 2	V
I_{DD}	supply current	note 2				
	normal mode	f_{clk} = 200 kHz	–	–	180	μA
	power-saving mode	f_{clk} = 35 kHz; V_{DD} = 3.5 V; V_{LCD} = 0 V; A0, A1 and A2 connected to V_{SS}	–	–	60	μA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 0 mA	–	–	0.05	V
V_{OH}	HIGH-level output voltage	I_{OH} = 0 mA	V_{DD} − 0.05	–	–	V
I_{OL1}	LOW-level output current CLK, $\overline{SYNC}$	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH-level output current CLK	V_{OH} = 4 V; V_{DD} = 5 V	1	–	–	mA
I_{OL2}	LOW-level output current SDA and SCL	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current SA0, A0 to A2, CLK, SDA and SCL	V_I = V_{DD} or V_{SS}	–	–	1	μA
I_{L2}	leakage current OSC	V_I = V_{DD}	–	–	1	μA
I_{pd}	A0, A1, A2 and OSC pull-down current	V_I = 1 V; V_{DD} = 5 V	20	50	150	μA
R_{SYNC}	pull-up resistor ($\overline{SYNC}$)		20	50	150	kΩ
V_{POR}	Power-on reset voltage level	note 3	–	1.0	1.6	V
C_I	input capacitance	note 4	–	–	7	pF
LCD outputs						
V_{BP}	DC voltage component BP0 to BP3	C_{BP} = 35 nF	–	20	–	mV
V_S	DC voltage component S0 to S39	C_S = 5 nF	–	20	–	mV
R_{BP}	output resistance BP0 to BP3	note 5; V_{LCD} = V_{DD} − 5 V	–	–	5	kΩ
R_S	output resistance S0 to S39	note 5; V_{LCD} = V_{DD} − 5 V	–	–	7.5	kΩ

Notes

1. $V_{LCD} \leq V_{DD} - 3$ V for $\frac{1}{3}$bias.
2. LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I^2C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.

11 AC CHARACTERISTICS

V_{DD} = 2 to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 2 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clk}	oscillator frequency on pin CLK					
	normal mode	V_{DD} = 5 V; note 1	125	200	288	kHz
	power-saving mode	V_{DD} = 3.5 V	21	31	48	kHz
t_{clkH}	CLK HIGH time	see Fig.21	1	–	–	µs
t_{clkL}	CLK LOW time		1	–	–	µs
$t_{P\overline{SYNC}}$	$\overline{SYNC}$ propagation delay time		–	–	400	ns
$t_{\overline{SYNC}L}$	$\overline{SYNC}$ LOW time		1	–	–	µs
t_{PLCD}	driver delays with test loads	V_{LCD} = V_{DD} − 5 V; see Fig.20	–	–	30	µs
Timing characteristics: I²C-bus; note 2; see Fig.22						
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs

Notes

1. At f_{clk} < 125 kHz, I²C-bus maximum transmission speed is derated.
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

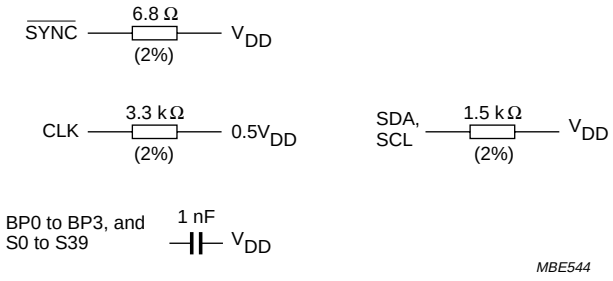


Fig.20 Test loads.

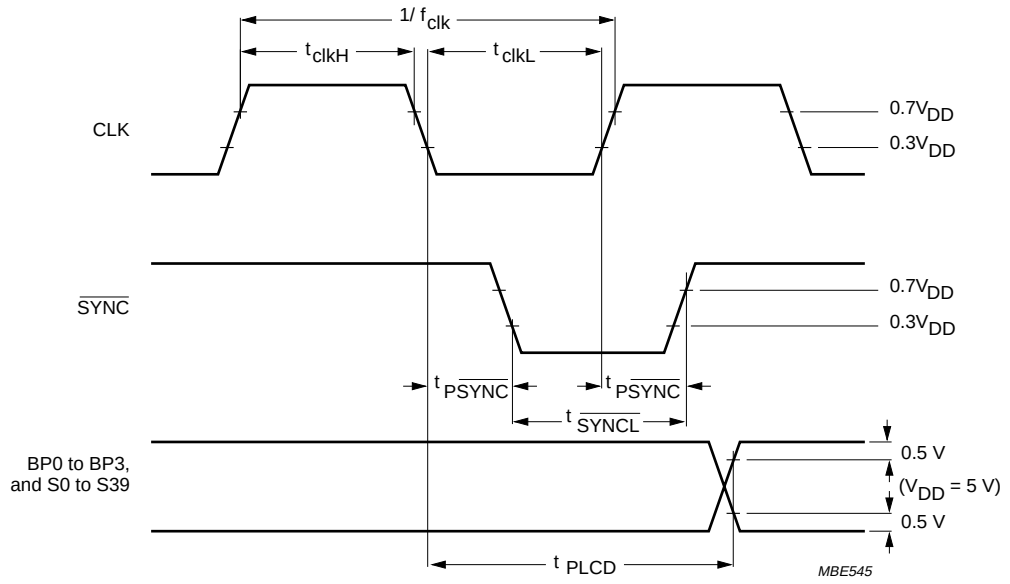


Fig.21 Driver timing waveforms.

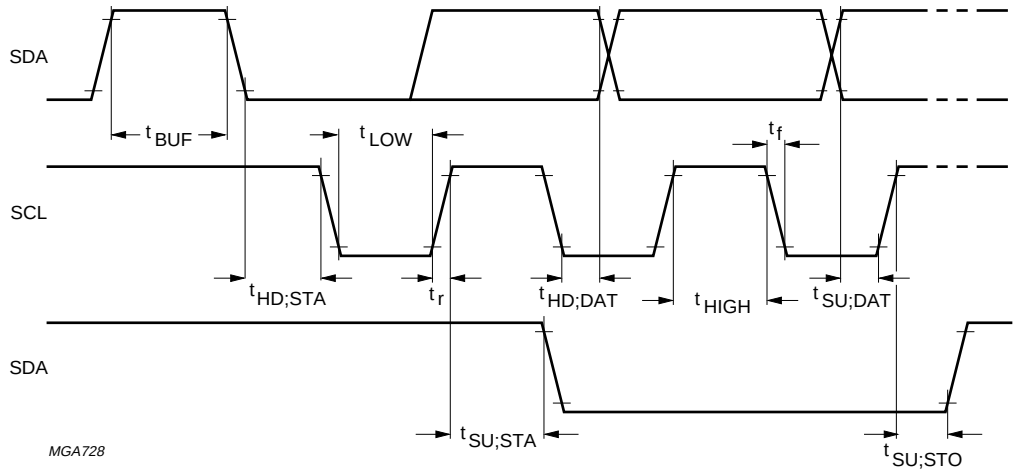
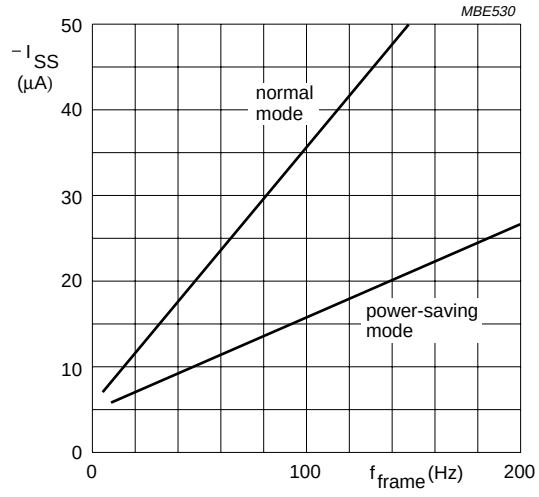


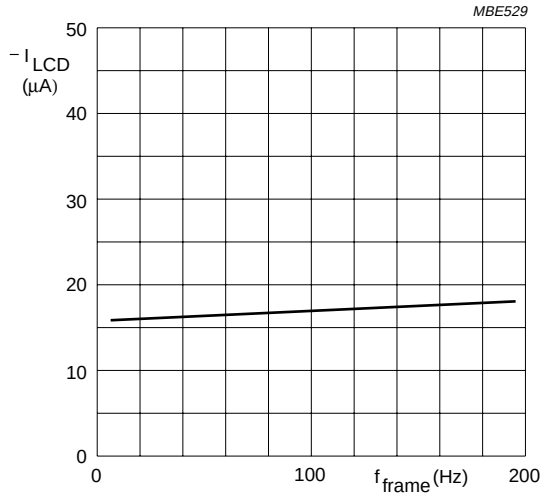
Fig.22 I²C-bus timing waveforms.

11.1 Typical supply current characteristics



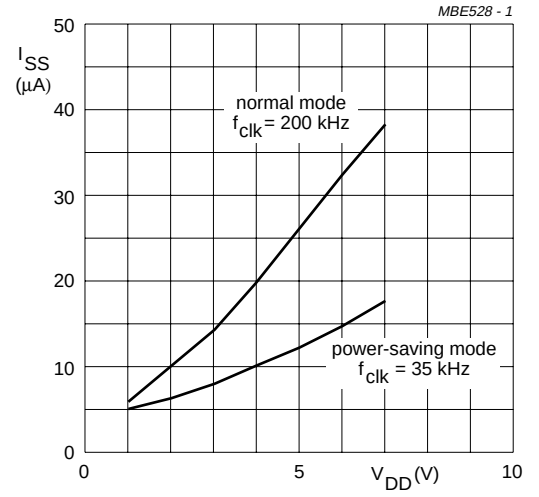
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.23 $-I_{SS}$ as a function of f_{frame}.



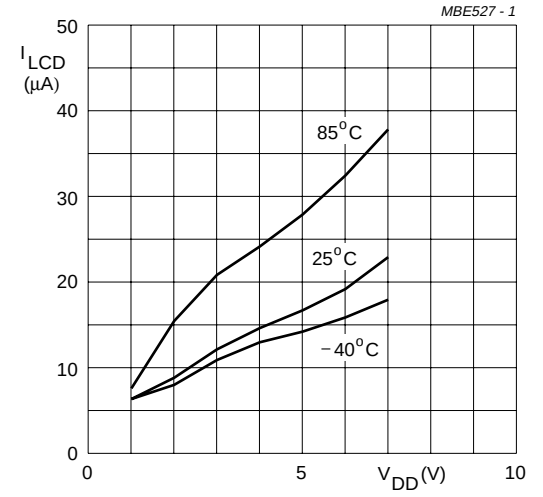
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.24 $-I_{LCD}$ as a function of f_{frame}.



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C.

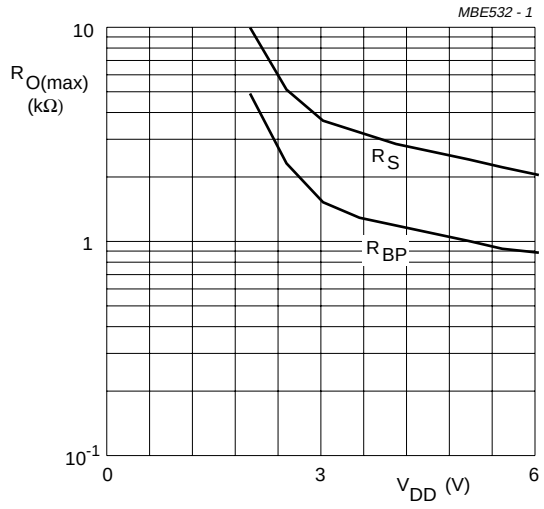
Fig.25 I_{SS} as a function of V_{DD}.



V_{LCD} = 0 V; external clock; f_{clk} = nominal frequency.

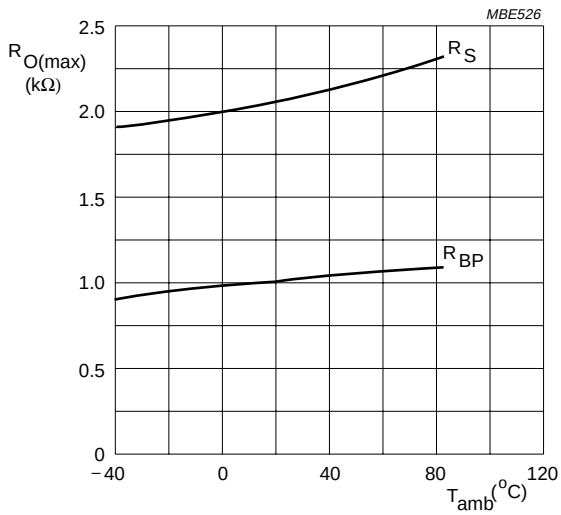
Fig.26 I_{LCD} as a function of V_{DD}.

11.2 Typical characteristics of LCD outputs



V_{LCD} = 0 V; T_{amb} = 25 °C.

Fig.27 $R_{O(max)}$ as a function of V_{DD}.



V_{DD} = 5 V; V_{LCD} = 0 V.

Fig.28 $R_{O(max)}$ as a function of T_{amb}.

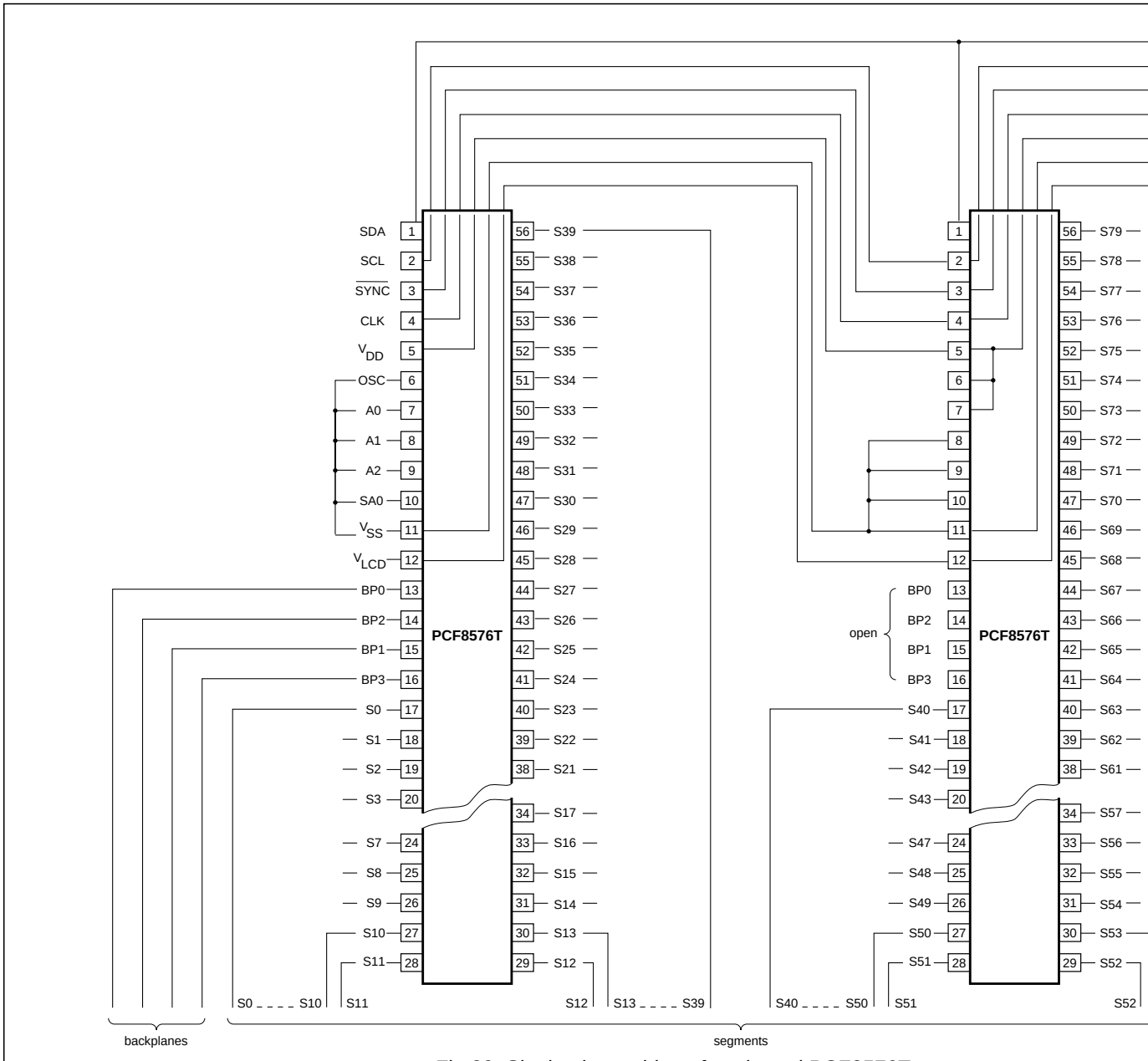


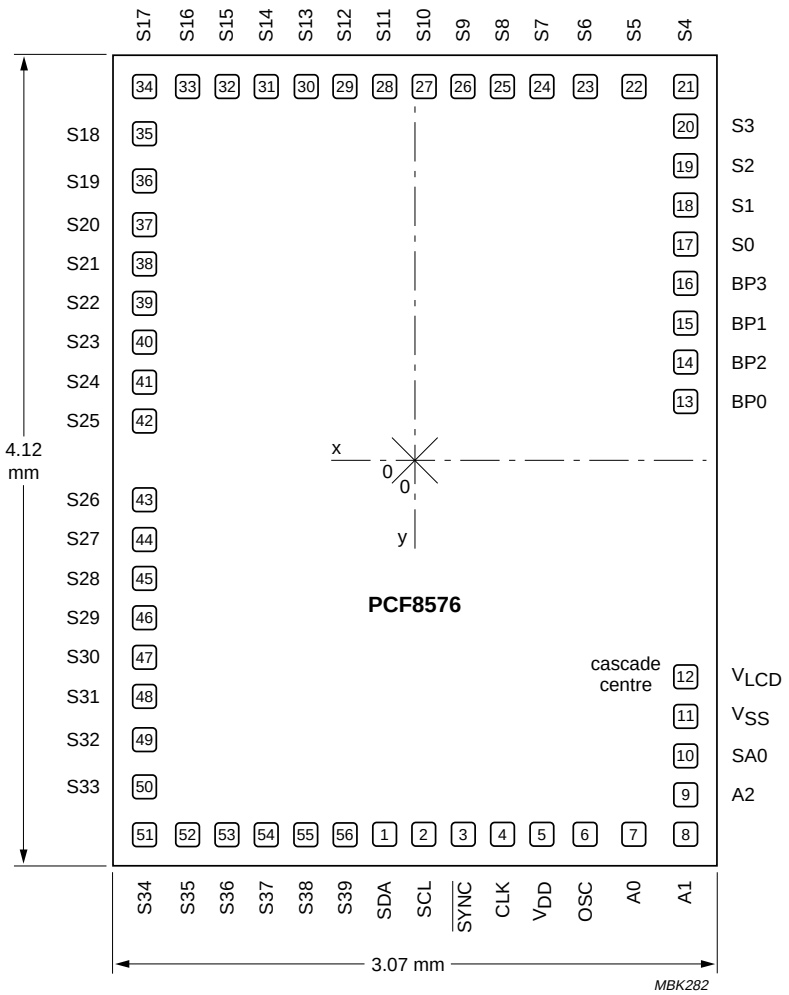
Fig.29 Single plane wiring of packaged PCF8576Ts.

12.1 Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (see Fig.30). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between V_{LCD} pad and the backplane output pads. The only bus line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be connected together.

When an external clocking source is to be used, OSC of all devices should be connected to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

13 BONDING PAD INFORMATION



Bonding pad dimensions: 120 × 120 μm.
Gold bump dimensions: 94 × 94 × 25 μm.

Fig.30 Bonding pad locations.

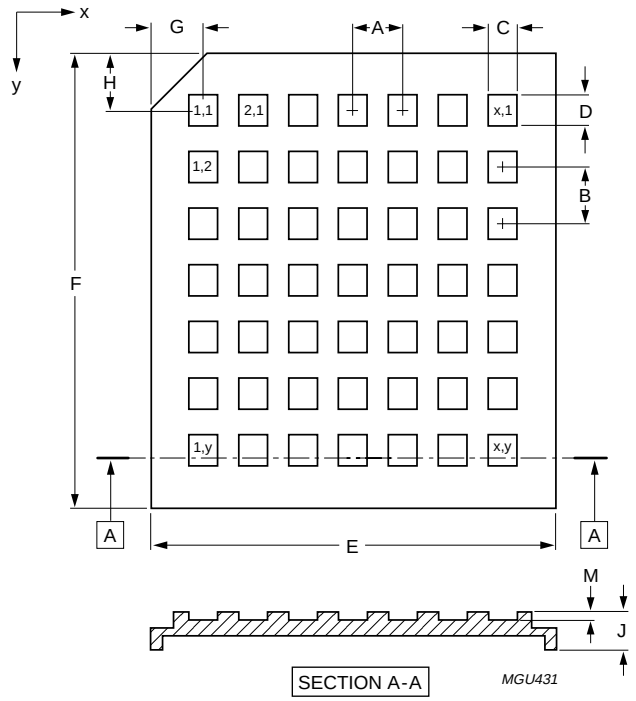
Table 15 Bonding pad locations (dimensions in μm)
All x and y coordinates are referenced to centre of chip (see Fig.30).

SYMBOL	PAD	COORDINATES	
		x	y
SDA	1	−155	−1900
SCL	2	45	−1900
$\overline{SYNC}$	3	245	−1900
CLK	4	445	−1900
V_{DD}	5	645	−1900
OSC	6	865	−1900
A0	7	1105	−1900
A1	8	1375	−1900
A2	9	1375	−1700
SA0	10	1375	−1500
V_{SS}	11	1375	−1300
V_{LCD}	12	1375	−1100
BP0	13	1375	300
BP2	14	1375	500
BP1	15	1375	700
BP3	16	1375	900
S0	17	1375	1100
S1	18	1375	1300
S2	19	1375	1500
S3	20	1375	1700
S4	21	1375	1900
S5	22	1105	1900
S6	23	865	1900
S7	24	645	1900
S8	25	445	1900
S9	26	245	1900
S10	27	45	1900
S11	28	−155	1900
S12	29	−355	1900
S13	30	−555	1900
S14	31	−755	1900
S15	32	−955	1900
S16	33	−1155	1900
S17	34	−1375	1900
S18	35	−1375	1660
S19	36	−1375	1420
S20	37	−1375	1200
S21	38	−1375	1000
S22	39	−1375	800
S23	40	−1375	600
S24	41	−1375	400
S25	42	−1375	200
S26	43	−1375	−200
S27	44	−1375	−400
S28	45	−1375	−600
S29	46	−1375	−800
S30	47	−1375	−1000
S31	48	−1375	−1200
S32	49	−1375	−1420
S33	50	−1375	−1660
S34	51	−1375	−1900
S35	52	−1155	−1900
S36	53	−955	−1900
S37	54	−755	−1900
S38	55	−555	−1900
S39	56	−355	−900

Table 16 Bonding pad dimensions

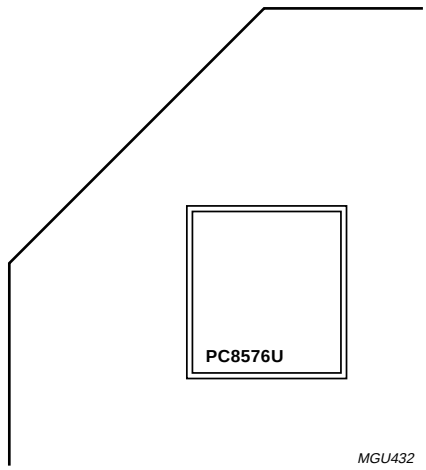
Pad pitch	200 μm
Pad size, aluminium	120 × 120 μm
Gold bump dimensions	94 × 94 × 25 μm

14 TRAY INFORMATION: PCF8576U



For dimensions see Table 18.

Fig.31 Tray details.



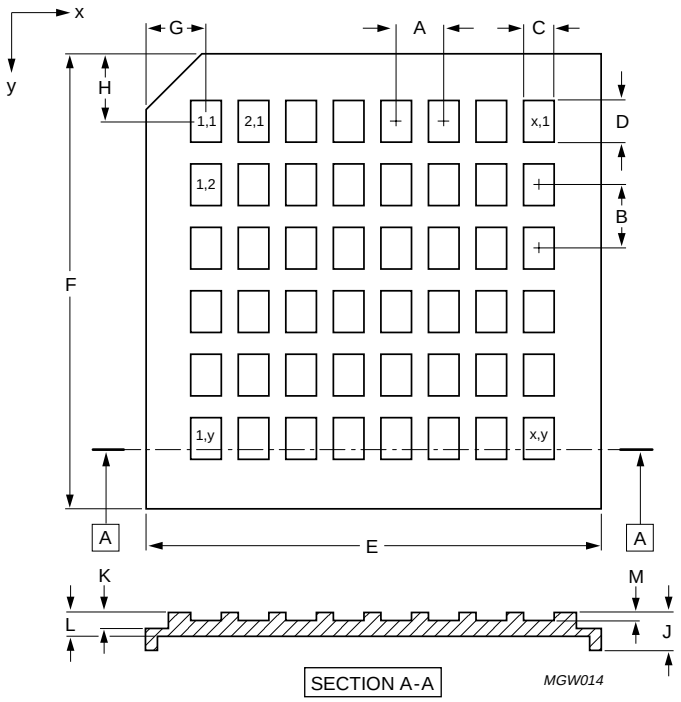
The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray.

Fig.32 Tray alignment.

Table 17 Tray dimensions (see Fig.33)

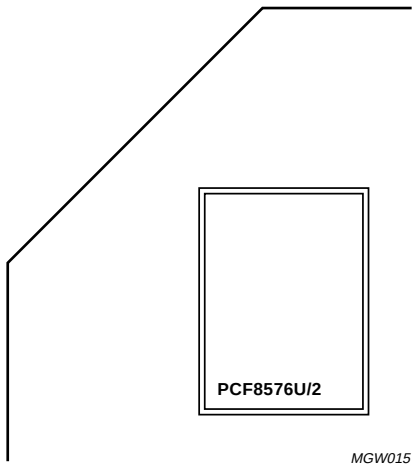
SYMBOL	DESCRIPTION	VALUE
A	pocket pitch; x direction	6.32 mm
B	pocket pitch; y direction	6.32 mm
C	pocket width; x direction	4.55 mm
D	pocket width; y direction	4.55 mm
E	tray width; x direction	50.67 mm
F	tray width; y direction	50.67 mm
G	cut corner to pocket 1,1 centre	6.32 mm
H	cut corner to pocket 1,1 centre	6.32 mm
J	tray thickness	3.94 mm
M	pocket depth	0.61 mm
x	number of pockets; x direction	7
y	number of pockets; y direction	7

15 TRAY INFORMATION: PCF8576U/2



For dimensions see Table 17.

Fig.33 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray.

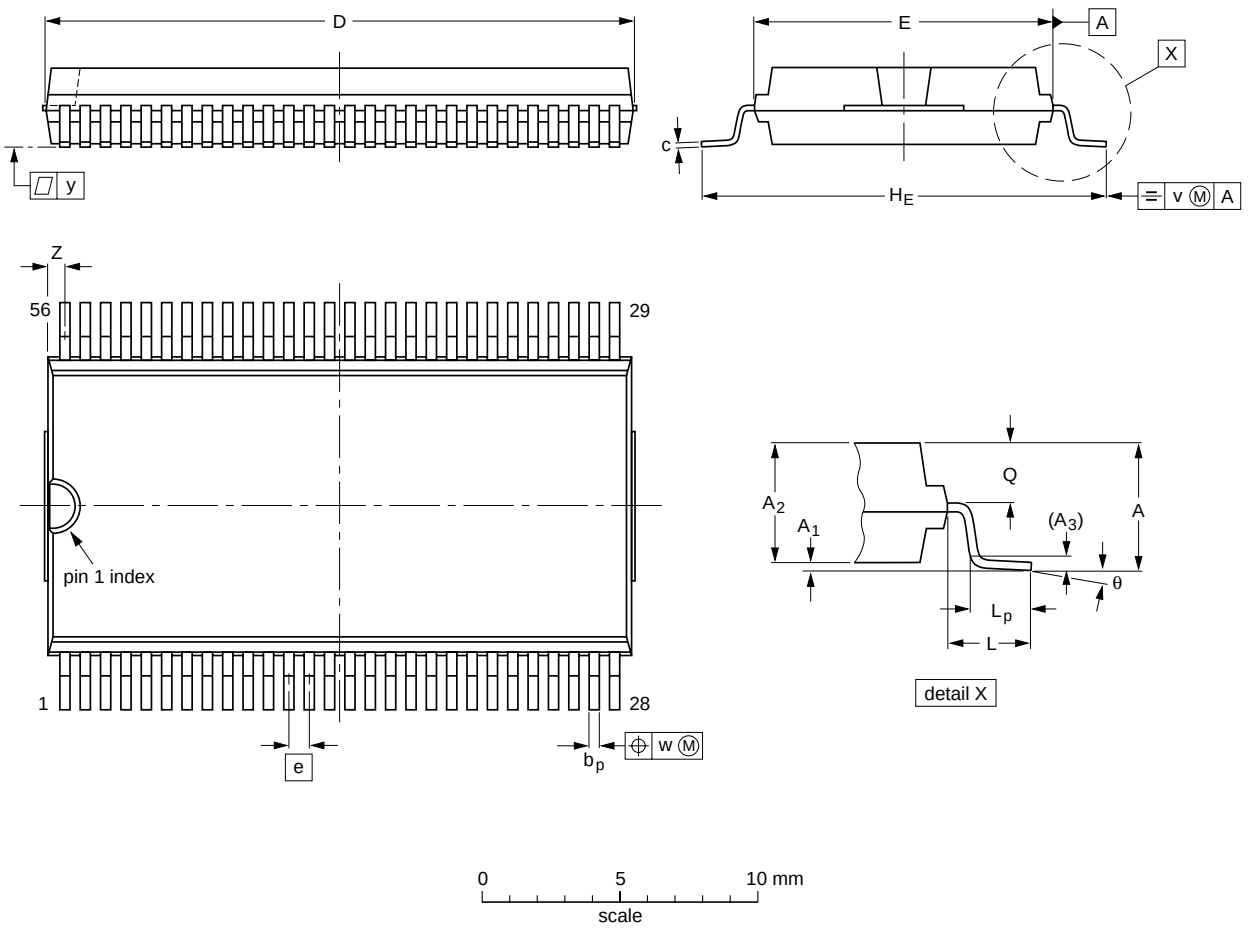
Fig.34 Tray alignment.

Table 18 Tray dimensions (see Fig.31)

SYMBOL	DESCRIPTION	VALUE
A	pocket pitch; x direction	5.33 mm
B	pocket pitch; y direction	7.11 mm
C	pocket width; x direction	3.43 mm
D	pocket width; y direction	4.67 mm
E	tray width; x direction	50.67 mm
F	tray width; y direction	50.67 mm
G	cut corner to pocket 1,1 centre	6.67 mm
H	cut corner to pocket 1,1 centre	7.56 mm
J	tray thickness	3.94 mm
K	tray cross section	1.76 mm
L	tray cross section	2.46 mm
M	pocket depth	0.89 mm
x	number of pockets; x direction	8
y	number of pockets; y direction	6

16 PACKAGE OUTLINES

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7^o 0^o
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~96-04-02~~ 97-08-11

17 SOLDERING

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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