



# PBSS5330PAS

30 V, 3 A PNP low  $V_{CEsat}$  (BISS) transistor

11 September 2014

Product data sheet

## 1. General description

PNP low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) transistor, encapsulated in an ultra thin DFN2020D-3 (SOT1061D) leadless small Surface-Mounted Device (SMD) plastic package with medium power capability and visible and solderable side pads.

NPN complement: PBSS4330PAS

## 2. Features and benefits

- Low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High collector current gain ( $h_{FE}$ ) at high  $I_C$
- High efficiency due to less heat generation
- High temperature applications up to 175 °C
- Reduced Printed-Circuit Board (PCB) area requirements
- Leadless small SMD plastic package with solderable side pads
- Exposed heat sink for excellent thermal and electrical conductivity
- Suitable for Automatic Optical Inspection (AOI) of solder joint
- AEC-Q101 qualified

## 3. Applications

- Loadswitch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

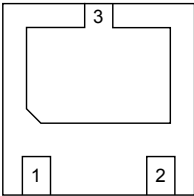
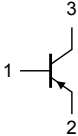
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CEO}$	collector-emitter voltage	open base	-	-	-30	V
$I_C$	collector current		-	-	-3	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-5	A
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = -3$ A; $I_B = -300$ mA; pulsed; $t_p \leq 300$ $\mu$ s; $\delta \leq 0.02$ ; $T_{amb} = 25$ °C	-	75	107	m $\Omega$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 <p>Transparent top view <b>DFN2020D-3 (SOT1061D)</b></p>	 <p>sym013</p>
2	E	emitter		
3	C	collector		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS5330PAS	DFN2020D-3	DFN2020D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 2 x 2 x 0.65 mm	SOT1061D

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS5330PAS	E2

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter		-	-30	V
$V_{CEO}$	collector-emitter voltage	open base		-	-30	V
$V_{EBO}$	emitter-base voltage	open collector		-	-6	V
$I_C$	collector current			-	-3	A
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms		-	-5	A
$I_B$	base current			-	-500	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	600	mW
			[2][3]	-	1.2	W
			[4]	-	1.5	W
			[5][6]	-	2.5	W
$T_j$	junction temperature			-	175	°C
$T_{amb}$	ambient temperature			-55	175	°C
$T_{stg}$	storage temperature			-65	175	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

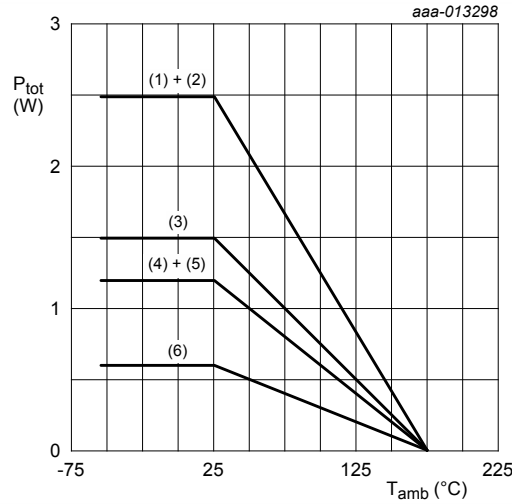
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

[3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

[4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.

[5] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and mounting pad for collector 1 cm<sup>2</sup>.

[6] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.



- (1) Ceramic PCB, single-sided copper, standard footprint
- (2) FR4 PCB, 4-layer copper, 1 cm<sup>2</sup>
- (3) FR4 PCB, single-sided copper, 6 cm<sup>2</sup>
- (4) FR4 PCB, single-sided copper, 1 cm<sup>2</sup>
- (5) FR4 PCB, 4-layer copper, standard footprint
- (6) FR4 PCB, single-sided copper, standard footprint

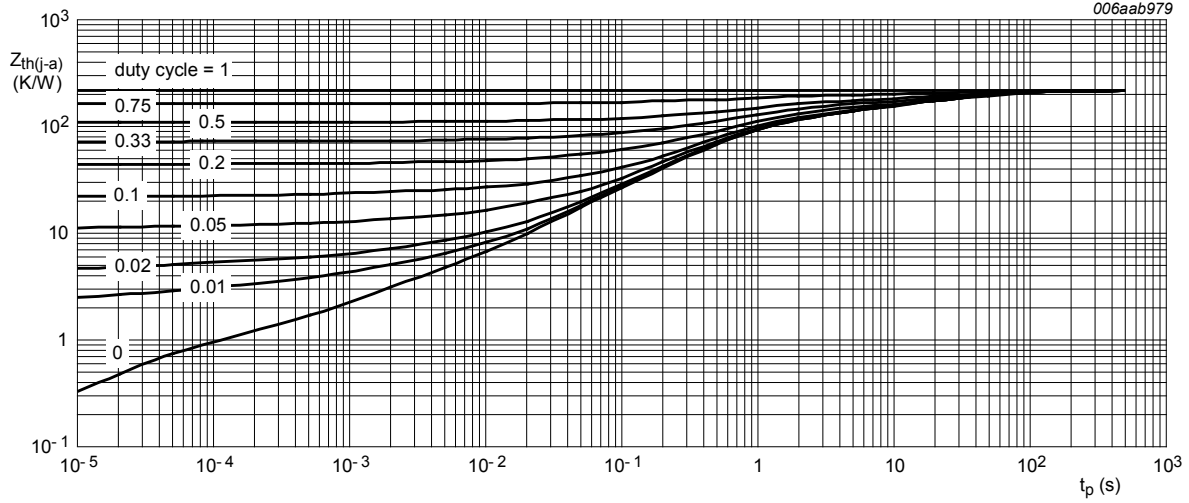
Fig. 1. Power derating curves

## 9. Thermal characteristics

Table 6. Thermal characteristics

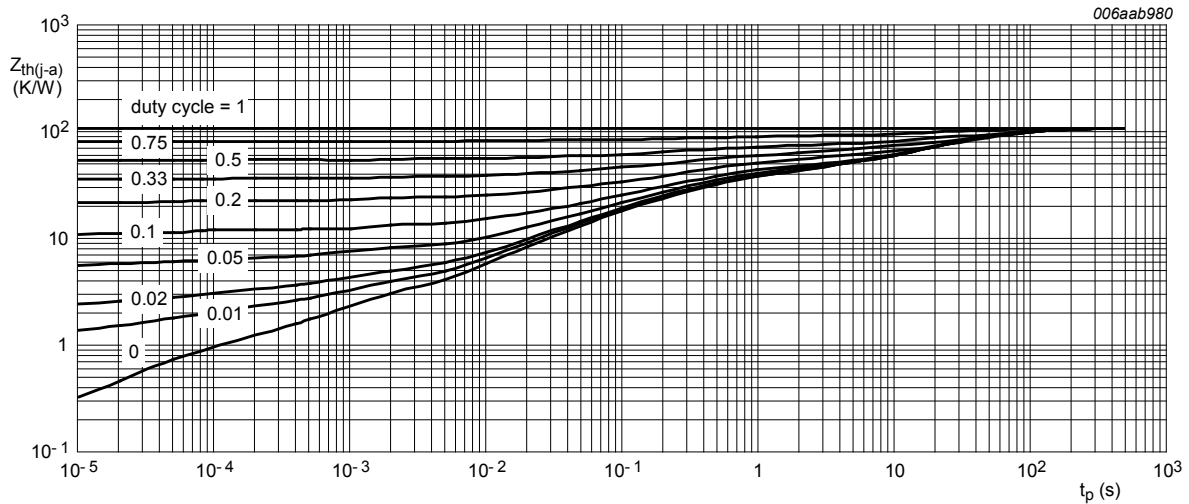
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W
			[2][3]	-	-	125	K/W
			[4]	-	-	100	K/W
			[5][6]	-	-	60	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [5] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.
- [6] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and mounting pad for collector 1 cm<sup>2</sup>.



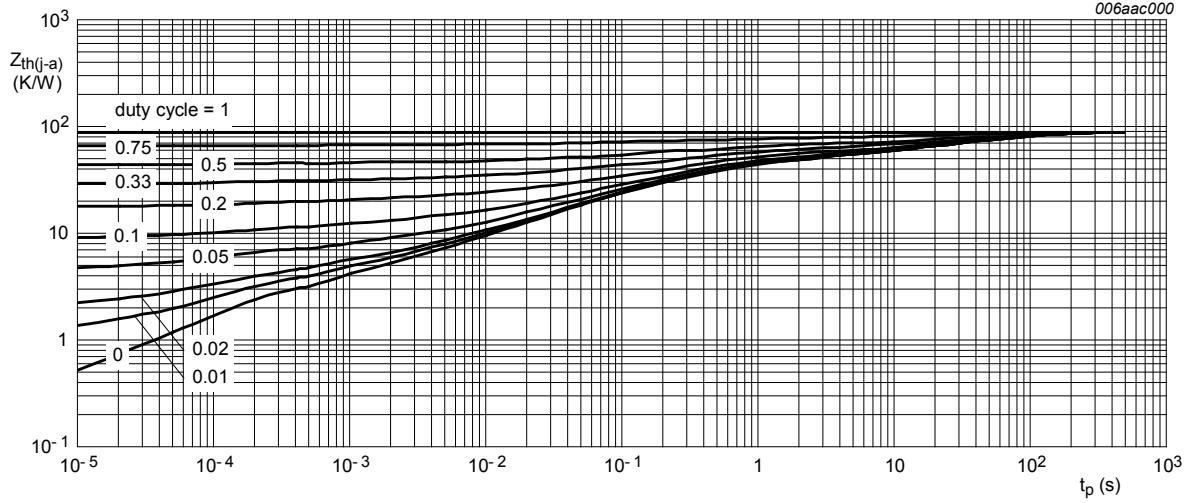
FR4 PCB, standard footprint

Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



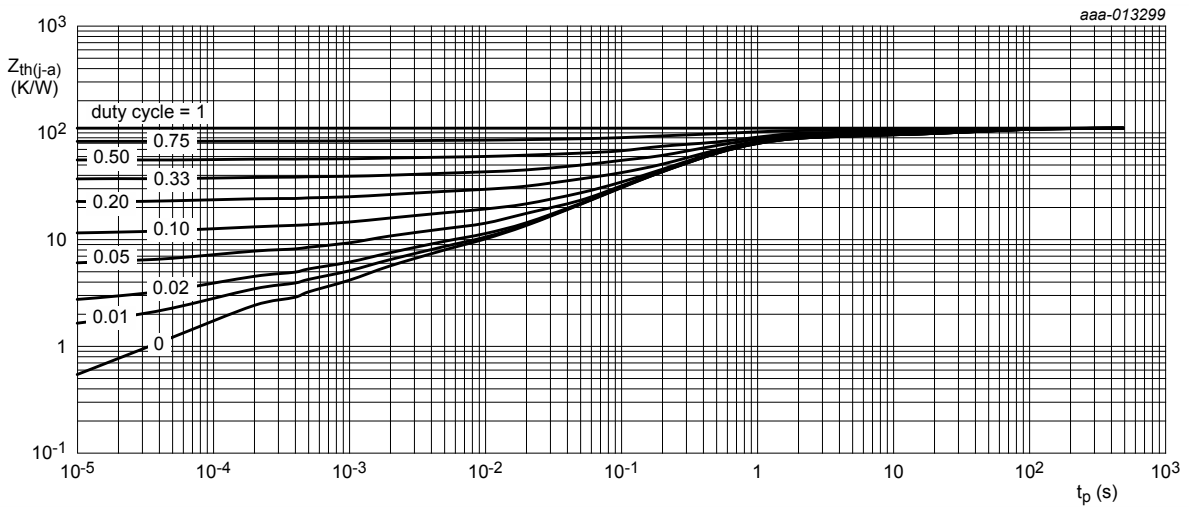
FR4 PCB, mounting pad for collector 1 cm<sup>2</sup>

Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



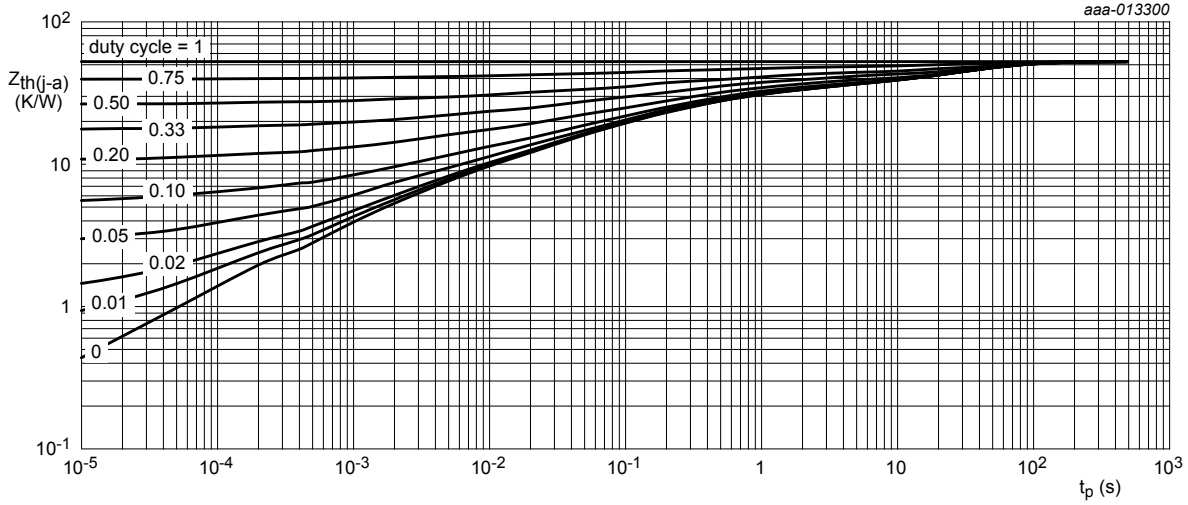
FR4 PCB, mounting pad for collector 6 cm<sup>2</sup>

**Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



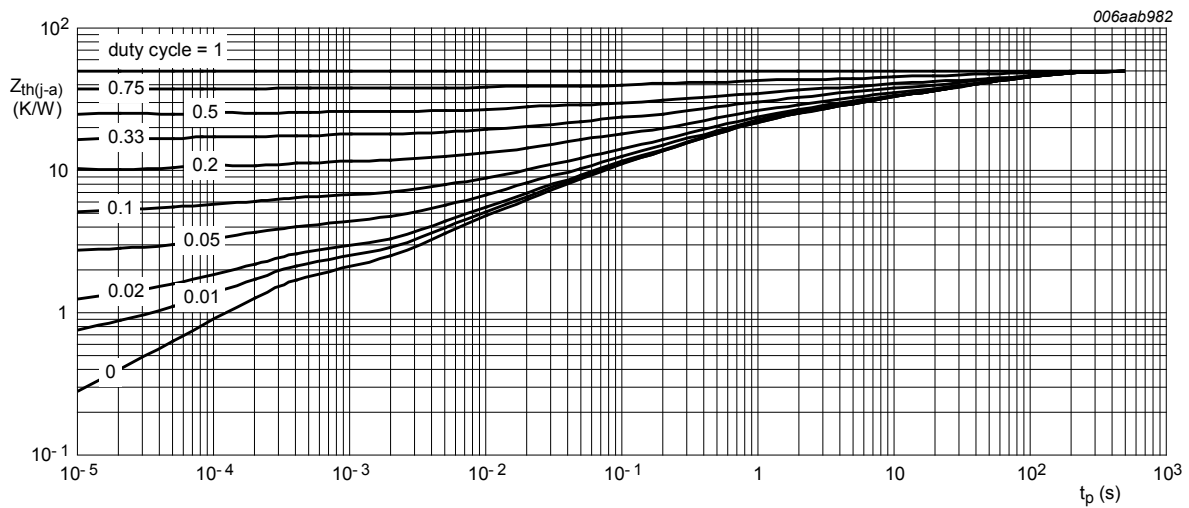
FR4 PCB, 4-layer copper, standard footprint

**Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



FR4 PCB, 4-layer copper, mounting pad for collector  $1\text{ cm}^2$

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB,  $\text{Al}_2\text{O}_3$ , standard footprint

Fig. 7. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

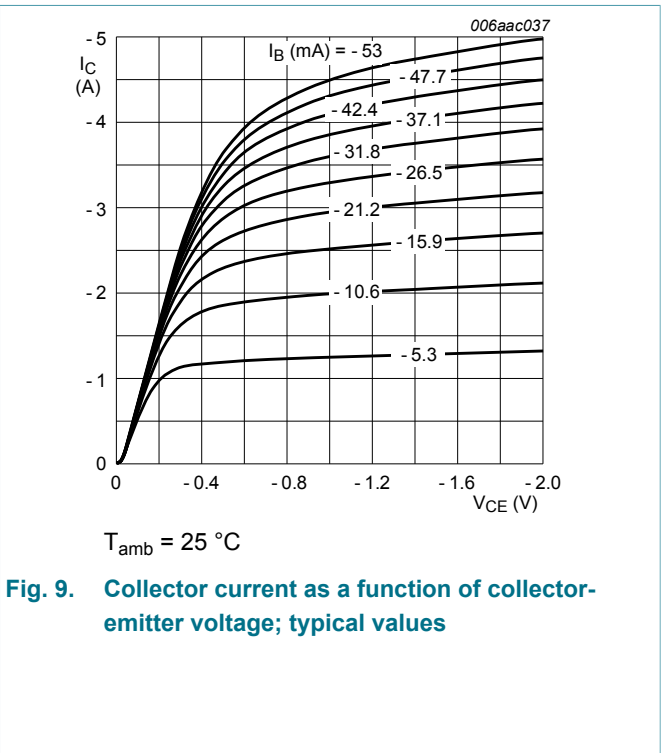
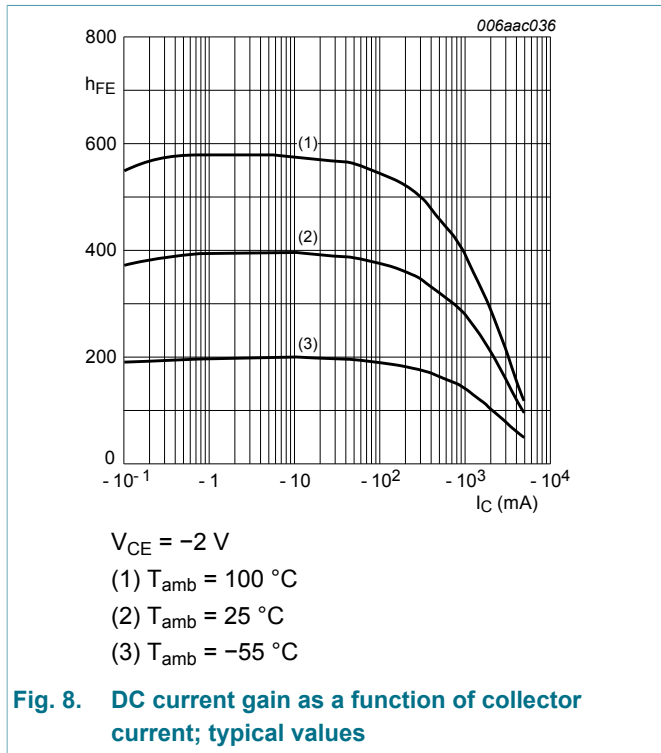
## 10. Characteristics

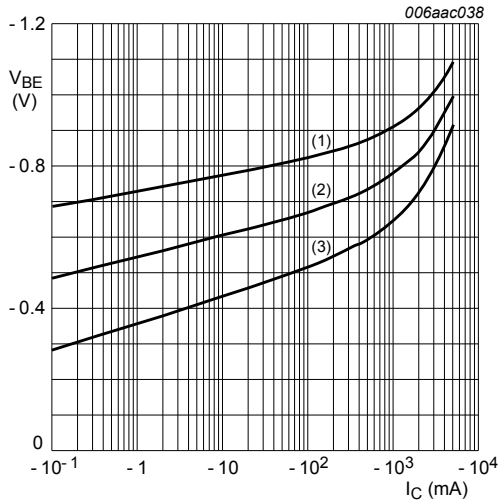
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -24 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-100	nA
		V <sub>CB</sub> = -24 V; I <sub>E</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-50	μA
I <sub>CES</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -24 V; V <sub>BE</sub> = 0 V; T <sub>amb</sub> = 25 °C	-	-	-100	nA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-100	nA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -2 V; I <sub>C</sub> = -0.5 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	200	320	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -1 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	175	280	450	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -2 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	140	210	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -3 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	100	160	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -0.5 A; I <sub>B</sub> = -50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-45	-70	mV
		I <sub>C</sub> = -1 A; I <sub>B</sub> = -50 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-90	-130	mV
		I <sub>C</sub> = -2 A; I <sub>B</sub> = -100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-170	-240	mV
		I <sub>C</sub> = -3 A; I <sub>B</sub> = -300 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-230	-320	mV
R <sub>CEsat</sub>	collector-emitter saturation resistance	t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	75	107	mΩ
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = -2 A; I <sub>B</sub> = -100 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-0.89	-1.1	V
		I <sub>C</sub> = -3 A; I <sub>B</sub> = -300 mA; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-0.97	-1.2	V
V <sub>BEon</sub>	base-emitter turn-on voltage	V <sub>CE</sub> = -2 V; I <sub>C</sub> = -1 A; pulsed; t <sub>p</sub> ≤ 300 μs; δ ≤ 0.02; T <sub>amb</sub> = 25 °C	-	-0.75	-1	V
t <sub>d</sub>	delay time	V <sub>CC</sub> = -9 V; I <sub>C</sub> = -2 A; I <sub>Bon</sub> = -0.1 A; I <sub>Boff</sub> = 0.1 A; T <sub>amb</sub> = 25 °C	-	11	-	ns
t <sub>r</sub>	rise time		-	59	-	ns
t <sub>on</sub>	turn-on time		-	70	-	ns
t <sub>s</sub>	storage time		-	165	-	ns
t <sub>f</sub>	fall time		-	35	-	ns
t <sub>off</sub>	turn-off time		-	200	-	ns



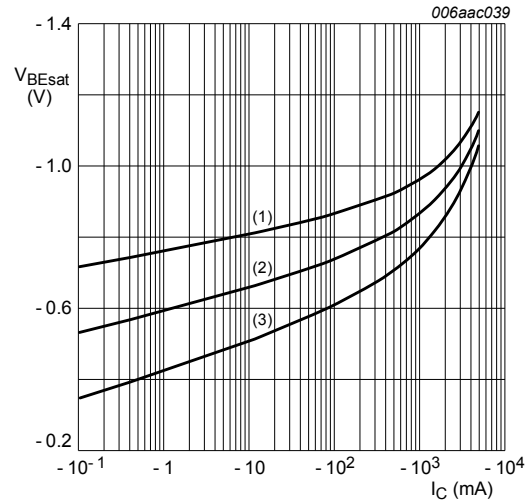
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_T$	transition frequency	$V_{CE} = -5 \text{ V}; I_C = -100 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$	100	165	-	MHz
$C_c$	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$	-	38	45	pF





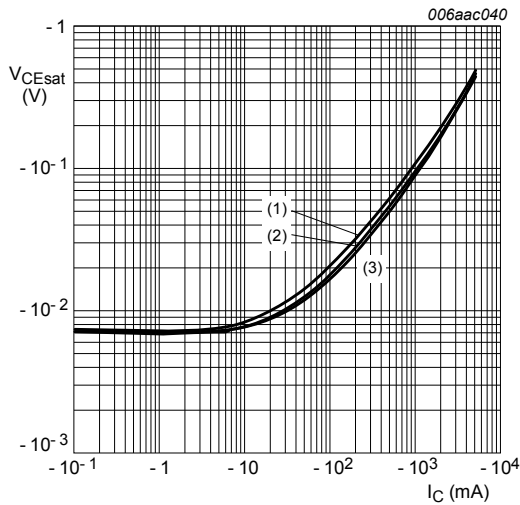
$V_{CE} = -2\text{ V}$   
 (1)  $T_{amb} = -55\text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

**Fig. 10. Base-emitter voltage as a function of collector current; typical values**



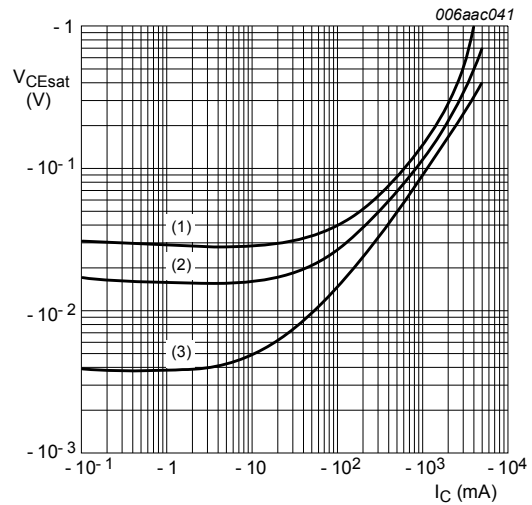
$I_C/I_B = 20$   
 (1)  $T_{amb} = -55\text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 100\text{ }^{\circ}\text{C}$

**Fig. 11. Base-emitter saturation voltage as a function of collector current; typical values**



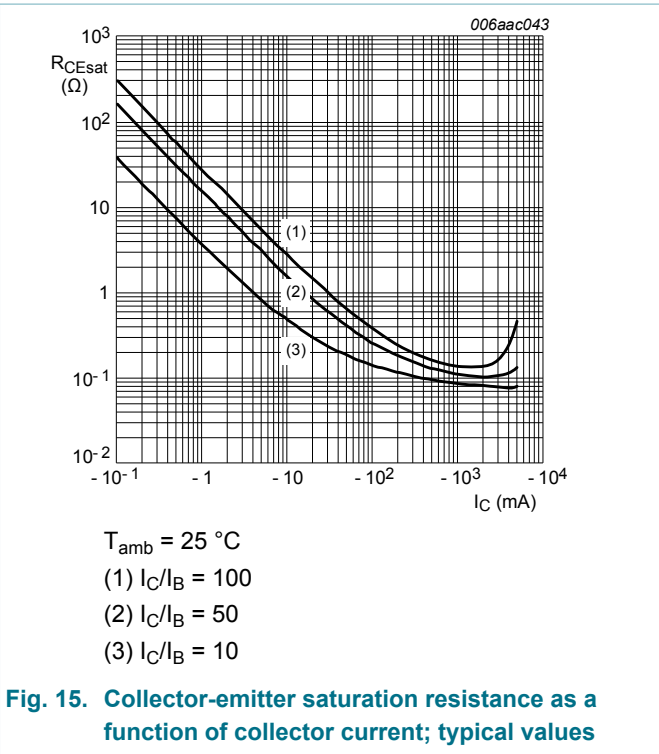
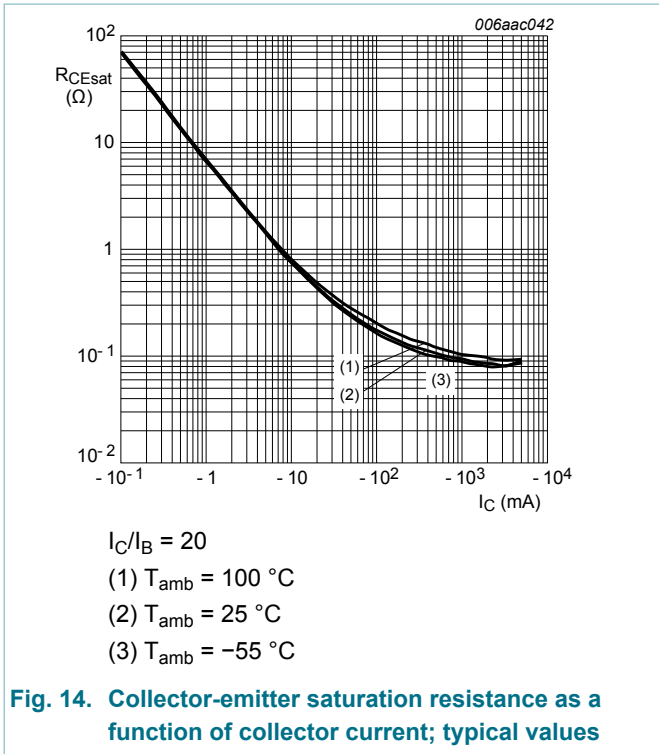
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25\text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = -55\text{ }^{\circ}\text{C}$

**Fig. 12. Collector-emitter saturation voltage as a function of collector current; typical values**



$T_{amb} = 25\text{ }^{\circ}\text{C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig. 13. Collector-emitter saturation voltage as a function of collector current; typical values**



### 11. Test information

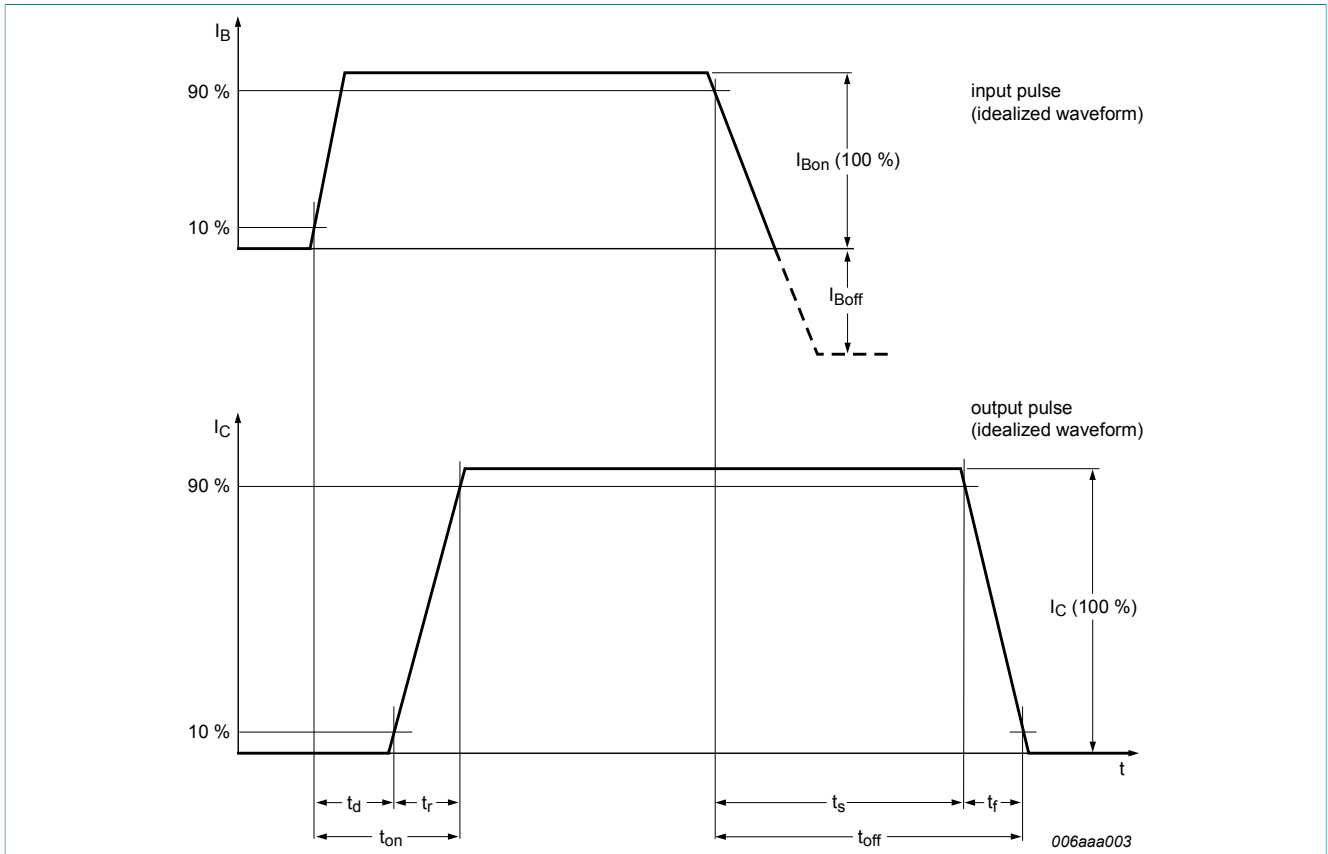


Fig. 16. BISS transistor switching time definition

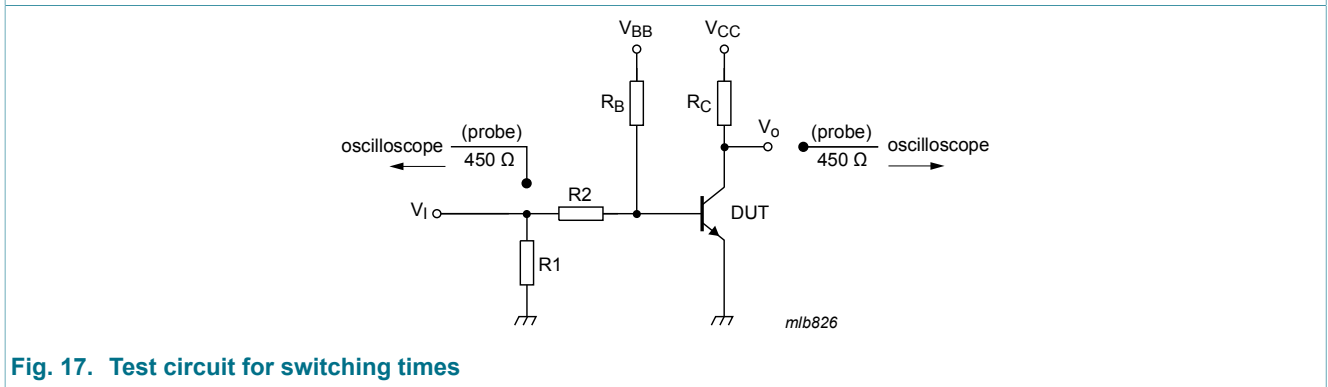


Fig. 17. Test circuit for switching times

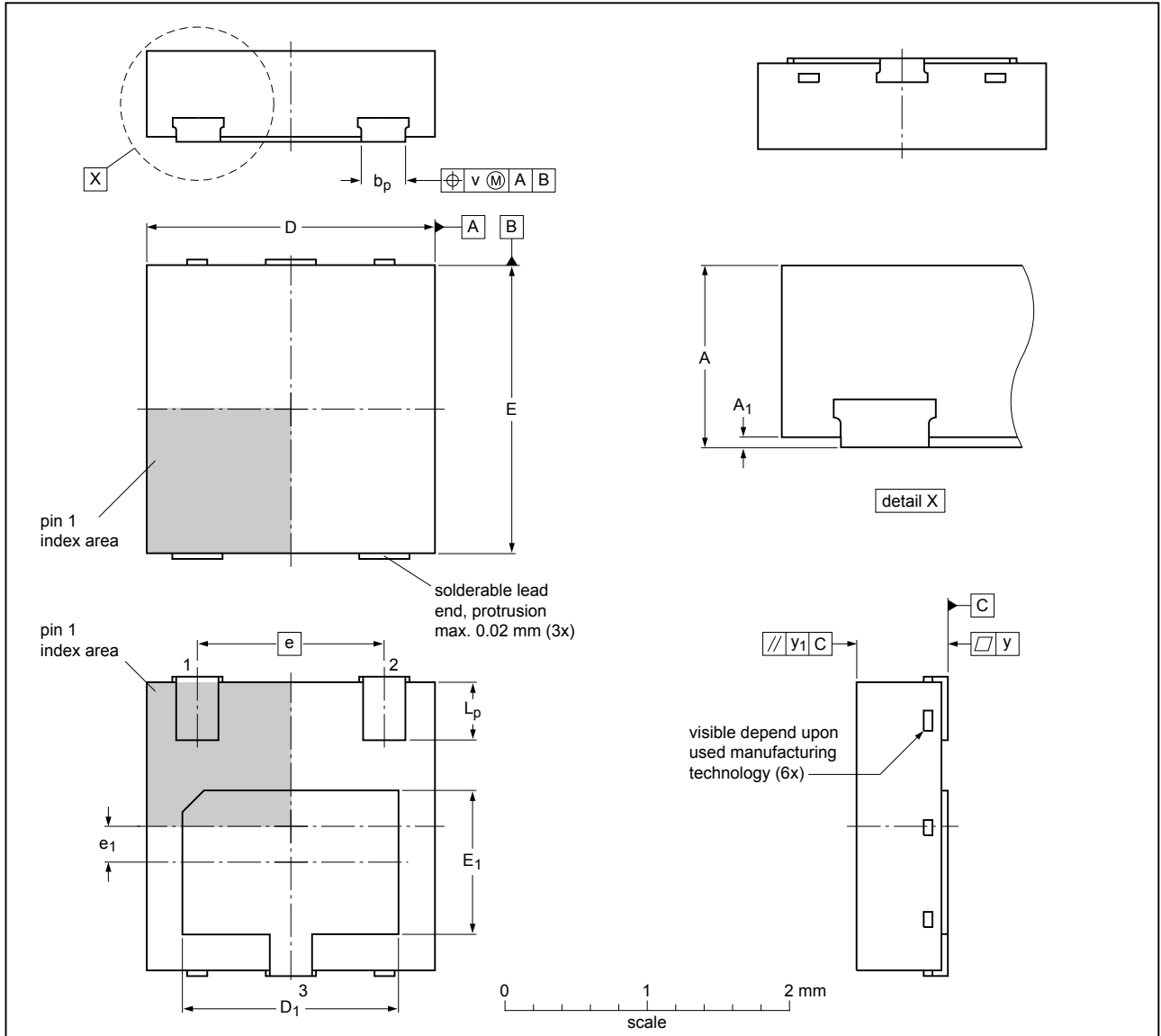
#### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

DFN2020D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 2 x 2 x 0.65 mm

SOT1061D



Dimensions (mm are the original dimensions)

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b <sub>p</sub>	D	D <sub>1</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	L <sub>p</sub>	v	y	y <sub>1</sub>
mm	max	0.65	0.04	0.35	2.1	1.6	2.1	1.1	0.3	0.45			
	nom							1.3			0.1	0.05	0.05
	min		0.25	1.9	1.4	1.9	0.9		0.2	0.35			

Note

1. Dimension A is including plating thickness

sot1061d\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1061D		---			14-03-11 14-03-12

Fig. 18. Package outline DFN2020D-3 (SOT1061D)

### 13. Soldering

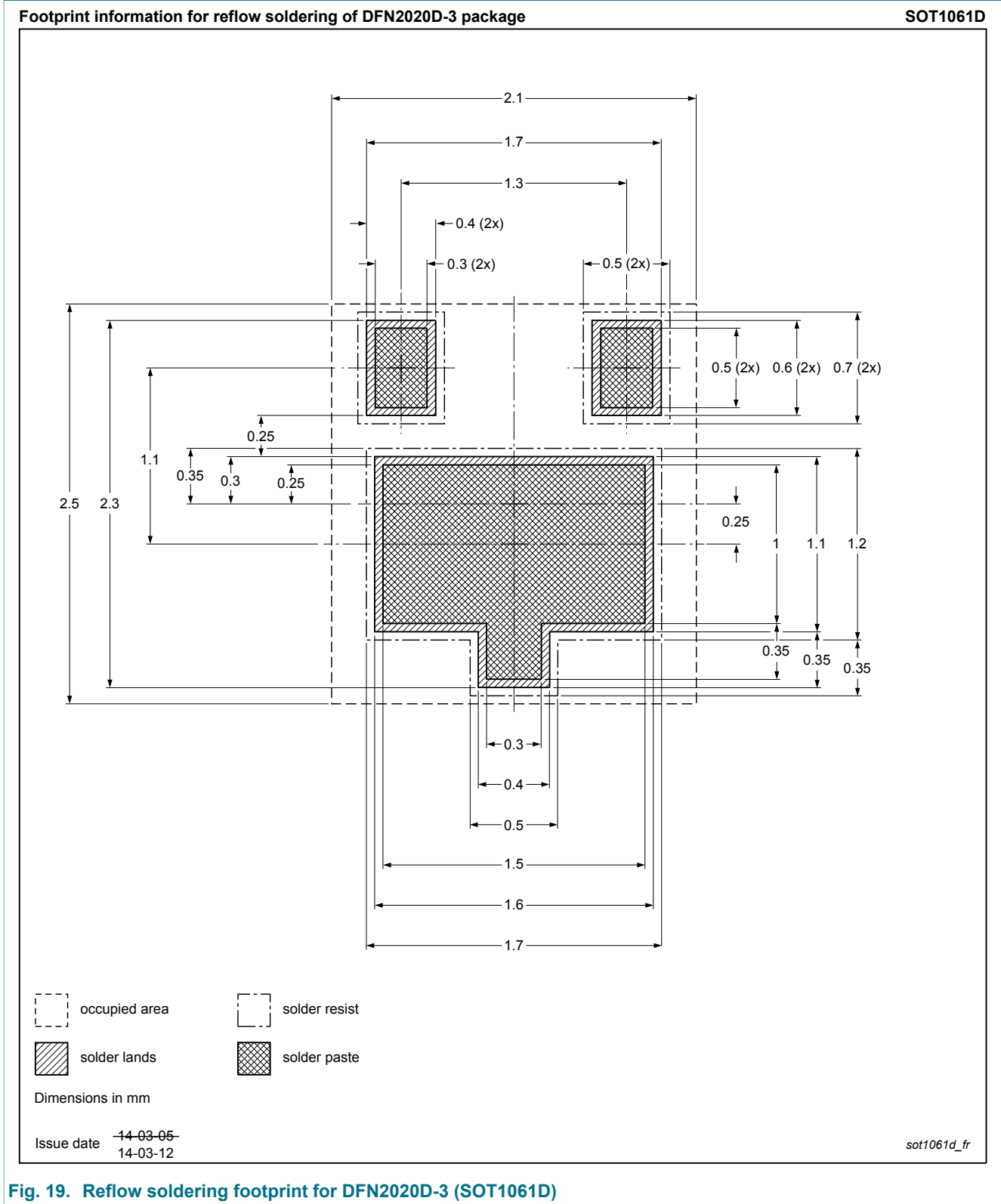


Fig. 19. Reflow soldering footprint for DFN2020D-3 (SOT1061D)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS5330PAS v.1	20140911	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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