

# PCA9537

## 4-bit I<sup>2</sup>C-bus and SMBus low power I/O port with interrupt and reset

Rev. 7 — 8 September 2021

Product data sheet  
COMPANY PUBLIC

## 1 General description

The PCA9537 is a 10-pin CMOS device that provides 4 bits of General Purpose parallel Input/Output (GPIO) expansion with interrupt and reset for I<sup>2</sup>C-bus/SMBus applications. It was developed to enhance the NXP Semiconductors family of I<sup>2</sup>C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push-buttons, LEDs, fans, etc.

The PCA9537 consists of a 4-bit Configuration register (input or output selection), 4-bit Input Port register, 4-bit Output Port register and a 4-bit Polarity Inversion register (active HIGH or active LOW operation). The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller.

The PCA9537 open-drain interrupt output ( $\overline{\text{INT}}$ ) is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. The  $\overline{\text{RESET}}$  pin causes the same reset/initialization to occur without de-powering the device.

The I<sup>2</sup>C-bus address is fixed and allows only one device on the same I<sup>2</sup>C-bus/SMBus.

## 2 Features and benefits

- 4-bit I<sup>2</sup>C-bus GPIO with interrupt and reset
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Active LOW reset input
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 4 I/O pins that default to 4 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in TSSOP10 package



### 3 Ordering information

Table 1. Ordering information

T<sub>amb</sub> = -40 °C to +85 °C

Type number	Topside mark	Package		Version
		Name	Description	
PCA9537DP	9537	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1

#### 3.1 Ordering options

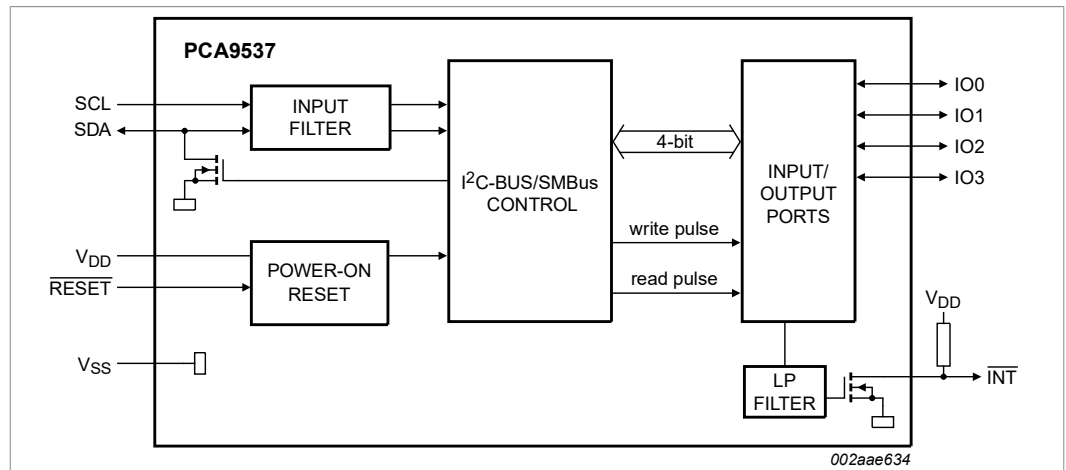
Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9537DP	PCA9537DP,118 <sup>[1]</sup>	TSSOP10	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	T <sub>amb</sub> = -40 °C to +85 °C
	PCA9537DPZ	TSSOP10	REEL 13" Q1/T1 *STANDARD MARK SSB <sup>[2]</sup>	2500	T <sub>amb</sub> = -40 °C to +85 °C

[1] Discontinued in 202104010DN - drop in replacement is PCA9537DPZ - this is documented in PCN 2020104008A.

[2] This packing method uses a Static Shielding Bag (SSB) solution. Material should be kept in the sealed bag between uses.

### 4 Block diagram

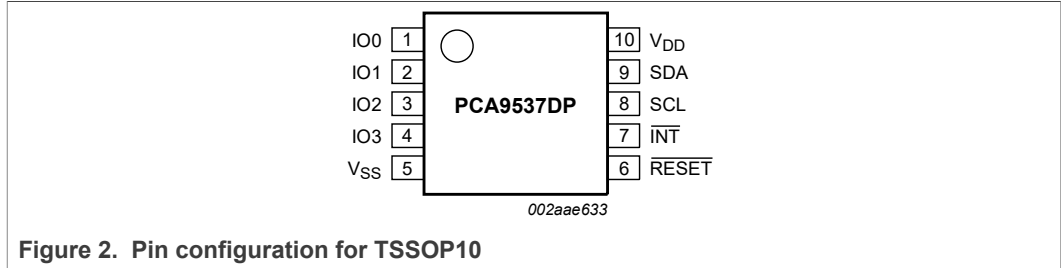


**Remark:** All I/Os are set to inputs at reset.

Figure 1. Block diagram of PCA9537

## 5 Pinning information

### 5.1 Pinning



### 5.2 Pin description

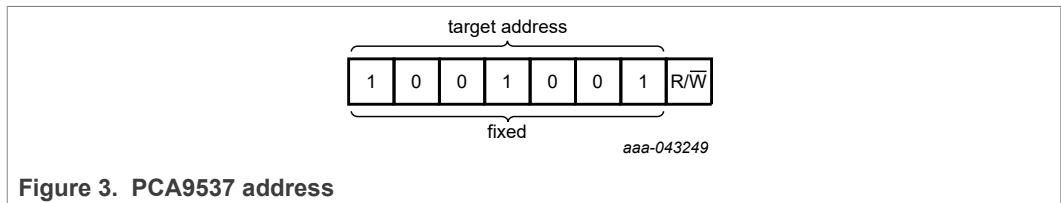
Table 3. Pin description

Symbol	Pin	Description
IO0	1	input/output 0
IO1	2	input/output 1
IO2	3	input/output 2
IO3	4	input/output 3
V <sub>SS</sub>	5	supply ground
RESET	6	active LOW reset input
INT	7	interrupt output (open-drain)
SCL	8	serial clock line
SDA	9	serial data line
V <sub>DD</sub>	10	supply voltage

## 6 Functional description

Refer to [Figure 1](#).

### 6.1 Device address



### 6.2 Registers

### 6.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the registers will be written or read.

Table 4. Command byte

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

### 6.2.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 5. Register 0 - Input Port register bit description

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	I7	read only	1*	not used
6	I6	read only	1*	
5	I5	read only	1*	
4	I4	read only	1*	
3	I3	read only	X*	value 'X' is determined by externally applied logic level
2	I2	read only	X*	
1	I1	read only	X*	
0	I0	read only	X*	

### 6.2.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 6. Register 1 - Output Port register bit description

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	O7	R	1*	not used
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	

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Table 6. Register 1 - Output Port register bit description...continued

Legend: \* default value.

Bit	Symbol	Access	Value	Description
3	O3	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

## 6.2.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with 1), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a 0), the Input Port data polarity is retained.

Table 7. Register 2 - Polarity Inversion register bit description

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	not used
6	N6	R/W	0*	
5	N5	R/W	0*	
4	N4	R/W	0*	
3	N3	R/W	0*	inverts polarity of Input Port register data 0 = Input Port register data retained (default value) 1 = Input Port register data inverted
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

## 6.2.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs.

Table 8. Register 3 - Configuration register bit description

Legend: \* default value.

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	not used
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	configures the directions of the I/O pins 0 = corresponding port pin enabled as an output 1 = corresponding port pin configured as an input (default value)
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

### 6.3 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the PCA9537 in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9537 registers and state machine will initialize to their default states. Thereafter,  $V_{DD}$  must be lowered below 0.2 V to reset the device.

For a power reset cycle,  $V_{DD}$  must be lowered below 0.2 V and then restored to the operating voltage.

### 6.4 RESET input

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of  $t_{w(\text{rst})}$ . The PCA9537 registers and SMBus/I<sup>2</sup>C-bus state machine will be held in their default state until the  $\overline{\text{RESET}}$  input is once again HIGH. This input requires a pull-up resistor to  $V_{DD}$  if no active connection is used.

### 6.5 Interrupt output

The open-drain interrupt output ( $\overline{\text{INT}}$ ) is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is de-activated when the input returns to its previous state or the Input Port register is read.

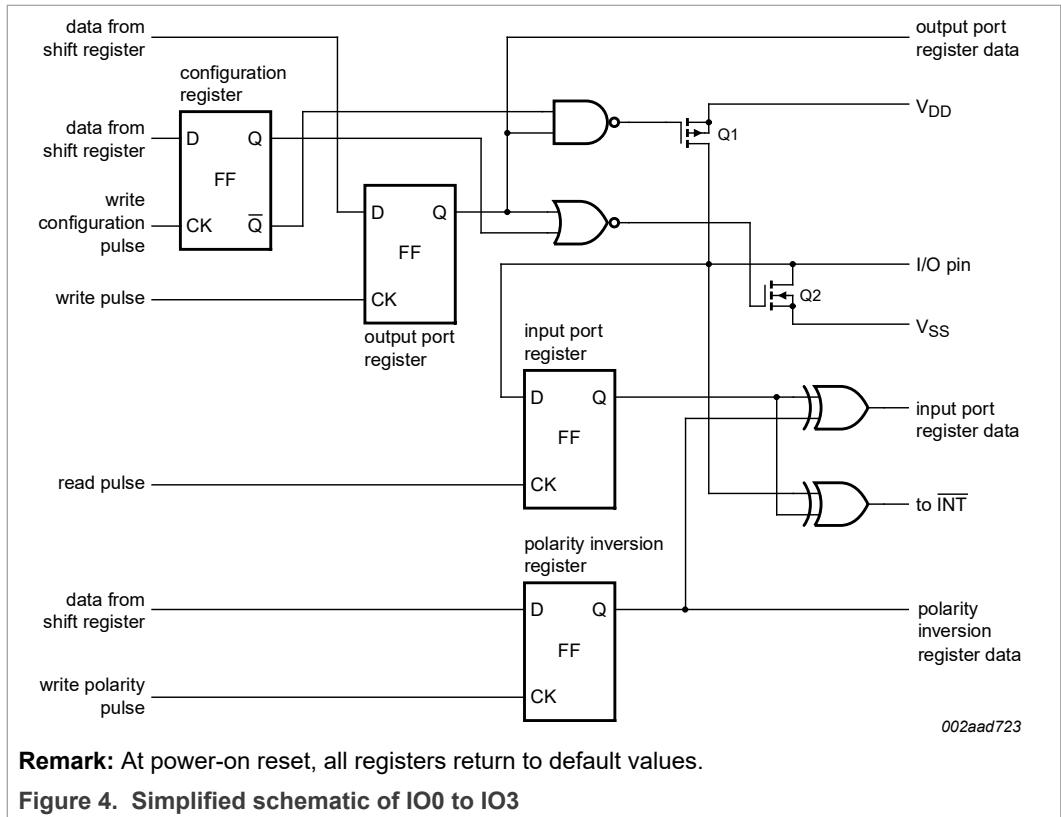
Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

### 6.6 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above  $V_{DD}$  to a maximum of 5.5 V.

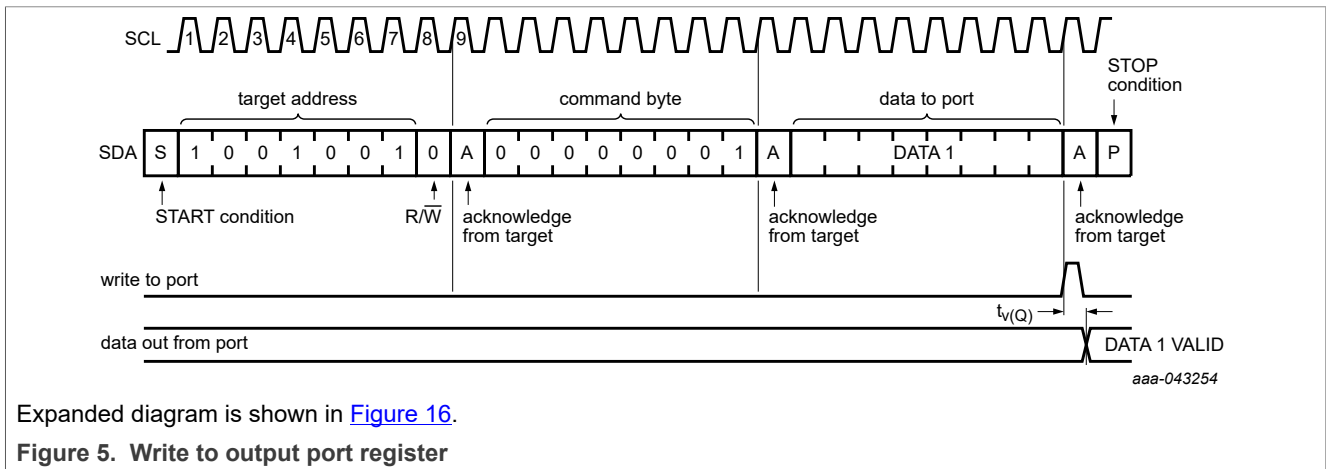
If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either  $V_{DD}$  or  $V_{SS}$ .

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6.7 Bus transactions

Data is transmitted to the PCA9537 registers using the write mode as shown in Figure 5 and Figure 6. Data is read from the PCA9537 registers using the read mode as shown in Figure 7 and Figure 8. These devices do not implement an auto-increment function so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.



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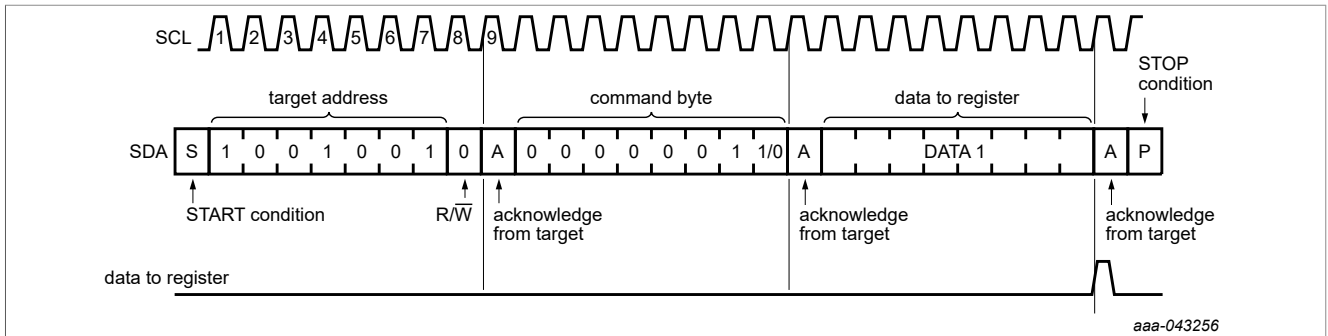


Figure 6. Write to configuration or polarity inversion registers

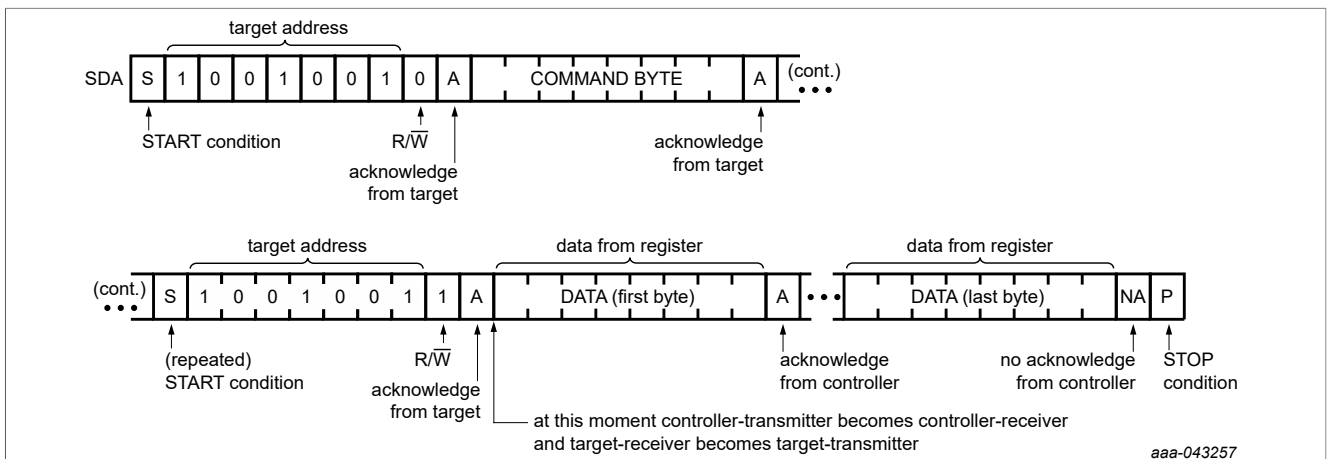
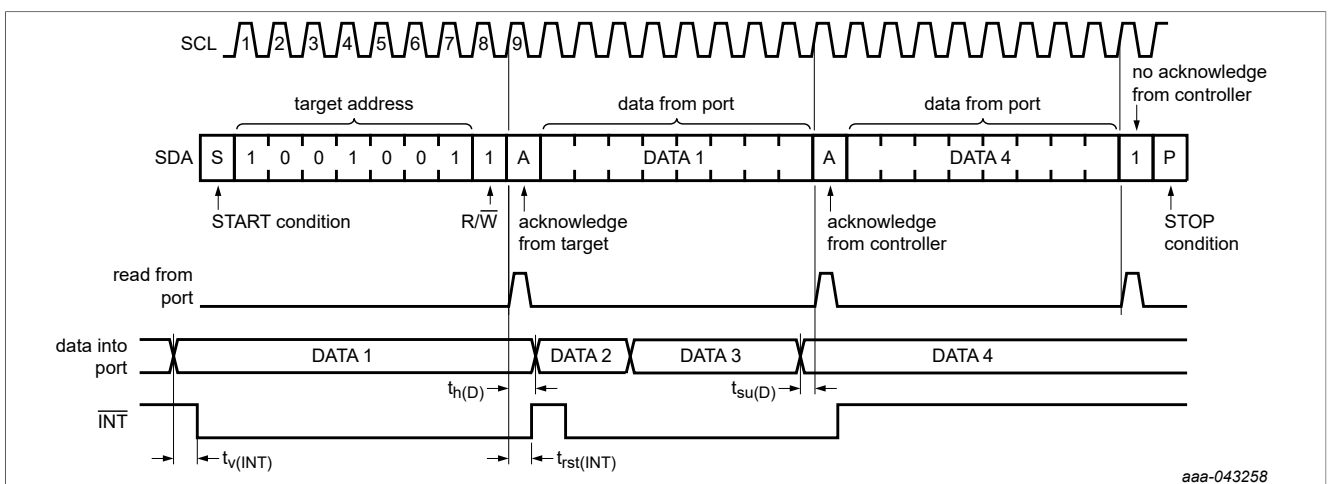


Figure 7. Read from register

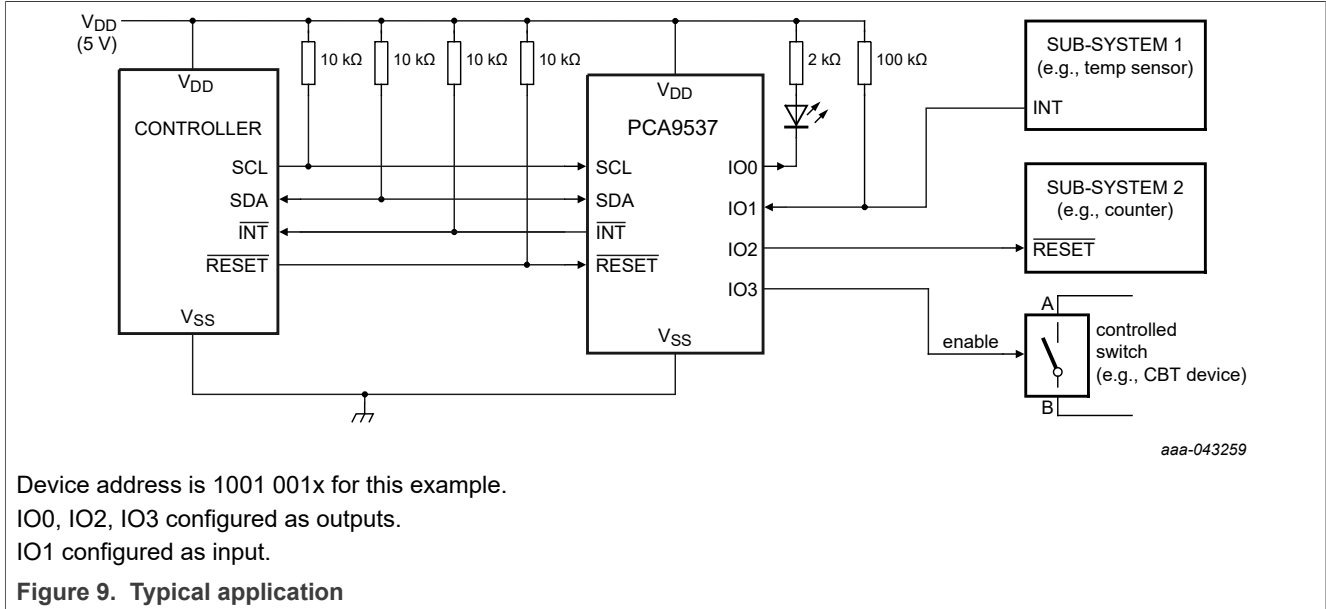


This figure assumes the command byte has previously been programmed with 00h. Transfer of data can be stopped at any moment by a STOP condition. Expanded diagram is shown in [Figure 15](#).

Figure 8. Read input port register



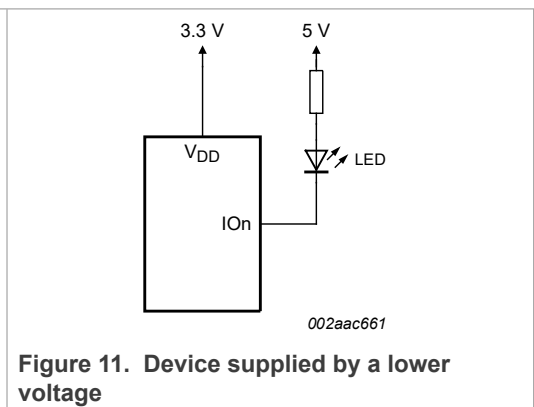
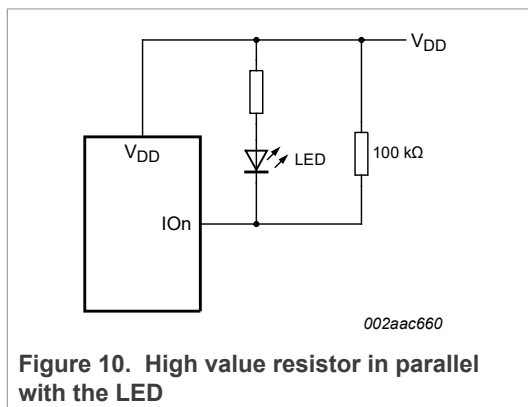
7 Application design-in information



7.1 Minimizing I<sub>DD</sub> when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>DD</sub> through a resistor as shown in Figure 9. Since the LED acts as a diode, when the LED is off the I/O V<sub>I</sub> is about 1.2 V less than V<sub>DD</sub>. The supply current, I<sub>DD</sub>, increases as V<sub>I</sub> becomes lower than V<sub>DD</sub>.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V<sub>DD</sub> when the LED is off. Figure 10 shows a high value resistor in parallel with the LED. Figure 11 shows V<sub>DD</sub> less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>I</sub> at or above V<sub>DD</sub> and prevents additional supply current consumption when the LED is off.



## 8 Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+6.0	V
I <sub>I</sub>	input current		-	±20	mA
V <sub>I/O</sub>	voltage on an input/output pin		V <sub>SS</sub> - 0.5	5.5	V
I <sub>O(IOn)</sub>	output current on pin IOn		-	±50	mA
I <sub>DD</sub>	supply current		-	85	mA
I <sub>SS</sub>	ground supply current		-	100	mA
P <sub>tot</sub>	total power dissipation		-	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature	operating	-40	+85	°C
T <sub>j(max)</sub>	maximum junction temperature		-	+125	°C

## 9 Static characteristics

Table 10. Static characteristics

V<sub>DD</sub> = 2.3 V to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
V <sub>DD</sub>	supply voltage		2.3	-	5.5	V
I <sub>DD</sub>	supply current	operating mode; V <sub>DD</sub> = 5.5 V; no load; f <sub>SCL</sub> = 100 kHz	-	104	175	µA
I <sub>stbL</sub>	LOW-level standby current	Standby mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>SS</sub> ; f <sub>SCL</sub> = 0 kHz; I/O = inputs	-	0.25	1	µA
I <sub>stbH</sub>	HIGH-level standby current	Standby mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> ; f <sub>SCL</sub> = 0 kHz; I/O = inputs	-	0.25	1	µA
V <sub>POR</sub>	power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	[1] -	1.7	2.2	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	5.5	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	7	-	mA
I <sub>L</sub>	leakage current	V <sub>I</sub> = V <sub>DD</sub> = V <sub>SS</sub>	-1	-	+1	µA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	5	10	pF
<b>I/Os</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.8	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	5.5	V

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Table 10. Static characteristics...continued

$V_{DD} = 2.3\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$I_{OL}$	LOW-level output current	$V_{OL} = 0.5\text{ V}$					
		$V_{DD} = 2.3\text{ V}$	[2]	8	10	-	mA
		$V_{DD} = 3.0\text{ V}$	[2]	8	14	-	mA
		$V_{DD} = 4.5\text{ V}$	[2]	8	17	-	mA
		$V_{OL} = 0.7\text{ V}$					
		$V_{DD} = 2.3\text{ V}$	[2]	10	13	-	mA
		$V_{DD} = 3.0\text{ V}$	[2]	10	19	-	mA
		$V_{DD} = 4.5\text{ V}$	[2]	10	24	-	mA
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -8\text{ mA}$					
		$V_{DD} = 2.3\text{ V}$	[3]	1.8	-	-	V
		$V_{DD} = 3.0\text{ V}$	[3]	2.6	-	-	V
		$V_{DD} = 4.5\text{ V}$	[3]	4.1	-	-	V
		$I_{OH} = -10\text{ mA}$					
		$V_{DD} = 2.3\text{ V}$	[3]	1.7	-	-	V
		$V_{DD} = 3.0\text{ V}$	[3]	2.5	-	-	V
		$V_{DD} = 4.5\text{ V}$	[3]	4.0	-	-	V
$I_L$	leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	$\mu\text{A}$	
$C_i$	input capacitance		-	5	10	pF	
<b>Interrupt <math>\overline{\text{INT}}</math></b>							
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	13	-	mA	
$I_{OH}$	HIGH-level output current	$V_{OL} = 0.4\text{ V}$	-1	-	+1	$\mu\text{A}$	
<b>Select input RESET</b>							
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.8	V	
$V_{IH}$	HIGH-level input voltage		2.0	-	5.5	V	
$I_L$	leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	$\mu\text{A}$	

[1]  $V_{DD}$  must be lowered to 0.2 V in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

## 10 Dynamic characteristics

Table 11. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
$f_{SCL}$	SCL clock frequency		0	100	0	400	kHz
$t_{BUF}$	bus free time between a STOP and START condition		4.7	-	1.3	-	$\mu\text{s}$

Table 11. Dynamic characteristics...continued

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
t <sub>HD;STA</sub>	hold time (repeated) START condition		4.0	-	0.6	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t <sub>SU;STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	μs
t <sub>HD;DAT</sub>	data hold time		0	-	0	-	ns
t <sub>VD;ACK</sub>	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	μs
t <sub>VD;DAT</sub>	data valid time	[2]	300	-	50	-	ns
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	ns
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	20 + 0.1C <sub>b</sub> <sup>[3]</sup>	300	ns
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	20 + 0.1C <sub>b</sub> <sup>[3]</sup>	300	ns
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
<b>Port timing</b>							
t <sub>v(Q)</sub>	data output valid time		-	200	-	200	ns
t <sub>su(D)</sub>	data input set-up time		100	-	100	-	ns
t <sub>h(D)</sub>	data input hold time		1	-	1	-	μs
<b>Interrupt timing</b>							
t <sub>v(INT)</sub>	valid time on pin INT		-	4	-	4	μs
t <sub>rst(INT)</sub>	reset time on pin INT		-	4	-	4	μs
<b>RESET</b>							
t <sub>w(rst)</sub>	reset pulse width		4	-	4	-	ns
t <sub>rec(rst)</sub>	reset recovery time		0	-	0	-	ns
t <sub>rst</sub>	reset time		400	-	400	-	ns

[1] t<sub>VD;ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] t<sub>VD;DAT</sub> = minimum time for the SDA data out to be valid following SCL LOW.

[3] C<sub>b</sub> = total capacitance of one bus line in pF.

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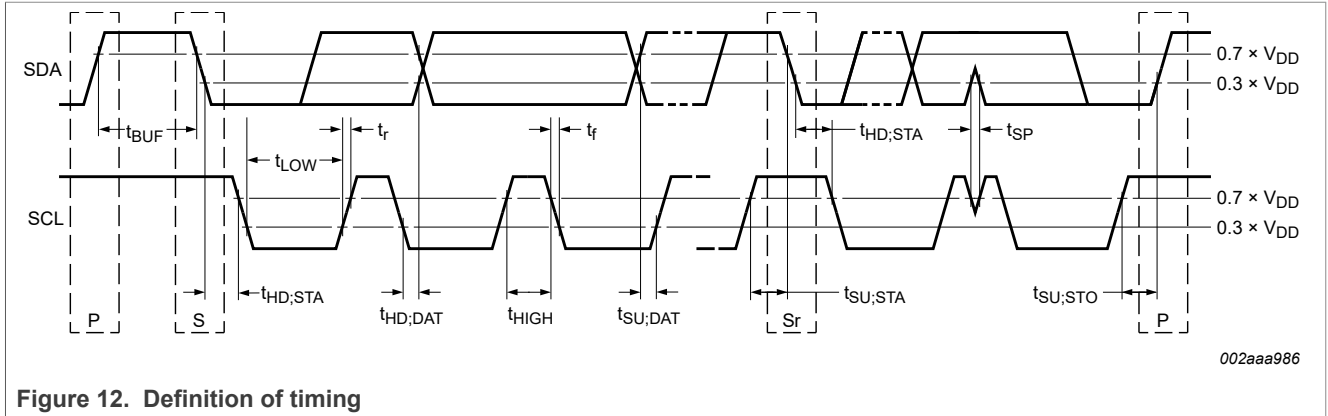
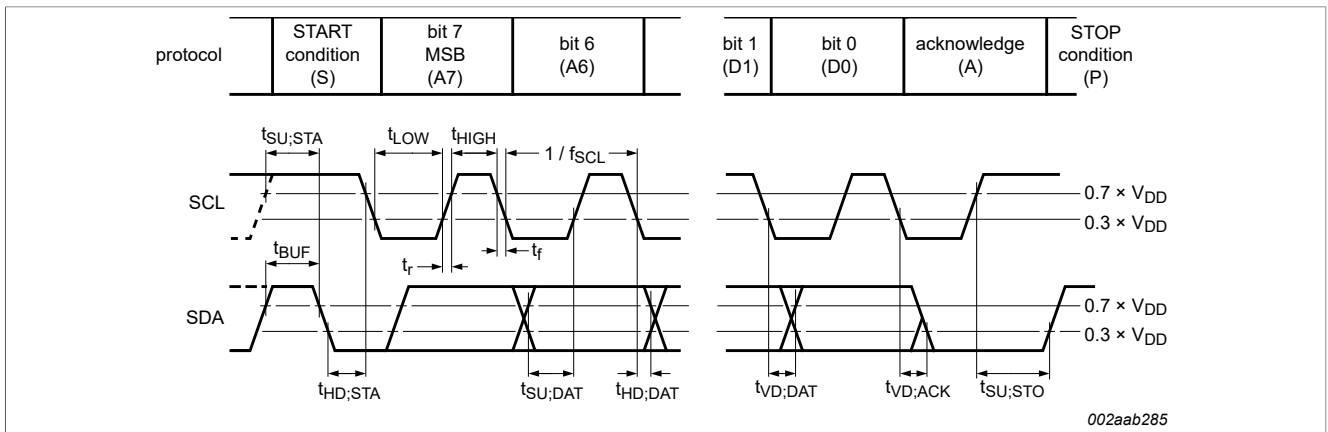


Figure 12. Definition of timing



Rise and fall times refer to  $V_{IL}$  and  $V_{IH}$ .

Figure 13. I<sup>2</sup>C-bus timing diagram

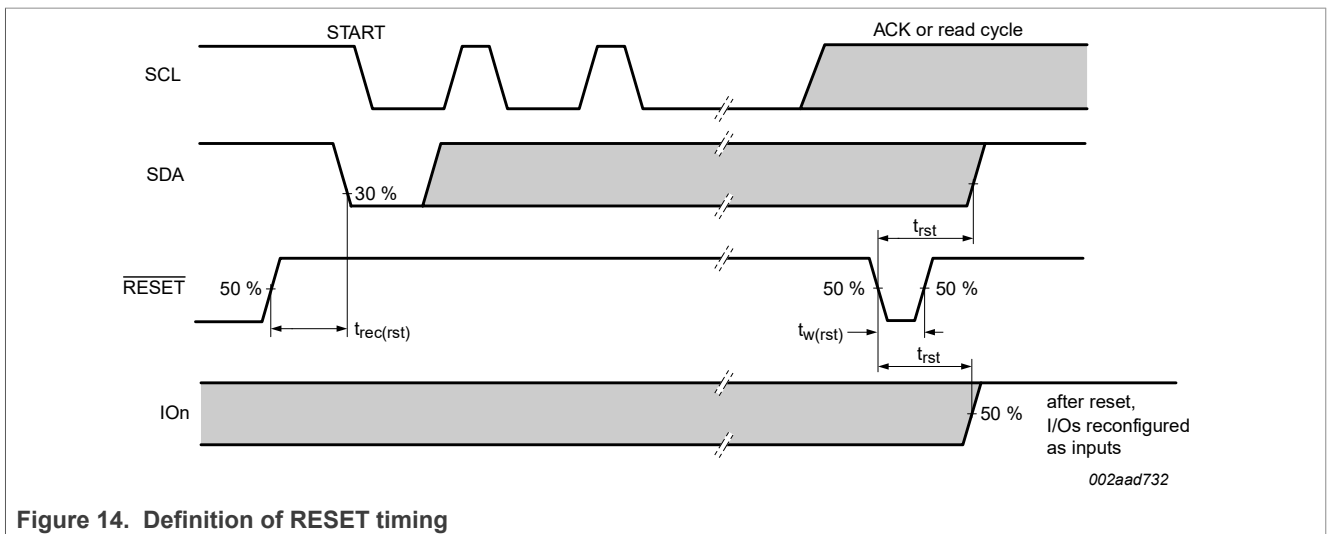


Figure 14. Definition of RESET timing

4-bit I<sup>2</sup>C-bus and SMBus low power I/O port with interrupt and reset

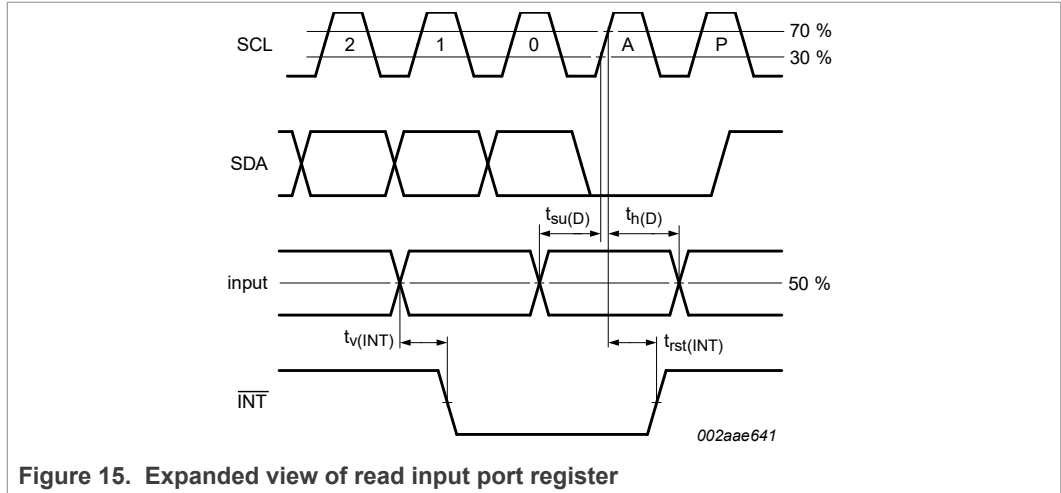


Figure 15. Expanded view of read input port register

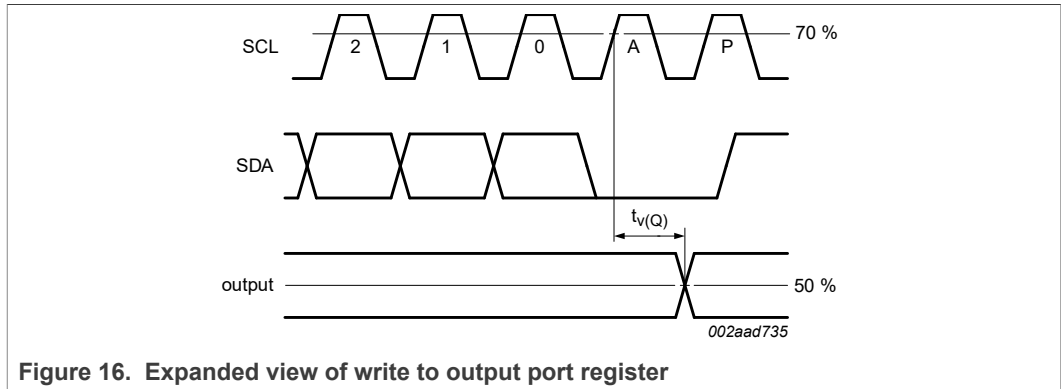


Figure 16. Expanded view of write to output port register

11 Test information

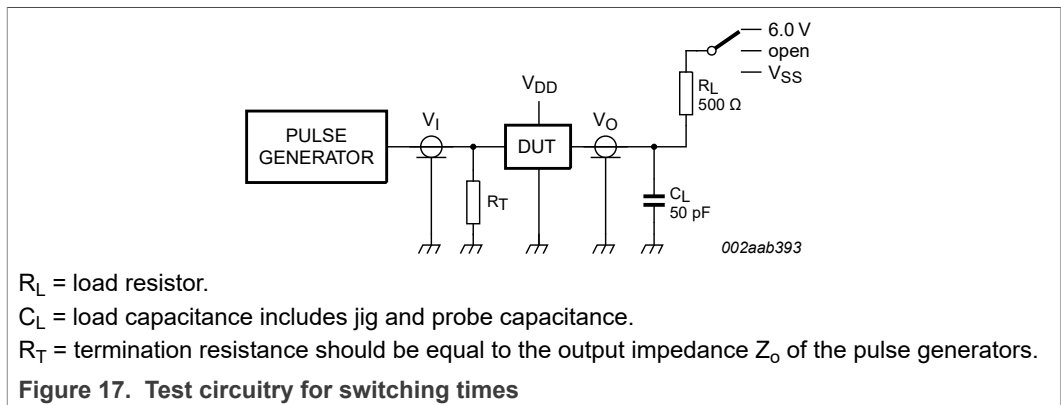


Figure 17. Test circuitry for switching times

4-bit I<sup>2</sup>C-bus and SMBus low power I/O port with interrupt and reset

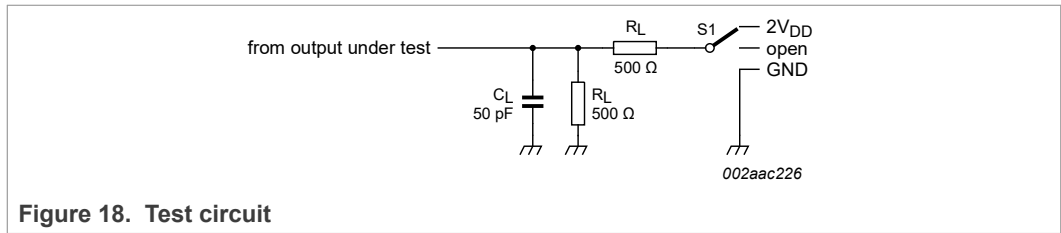


Figure 18. Test circuit

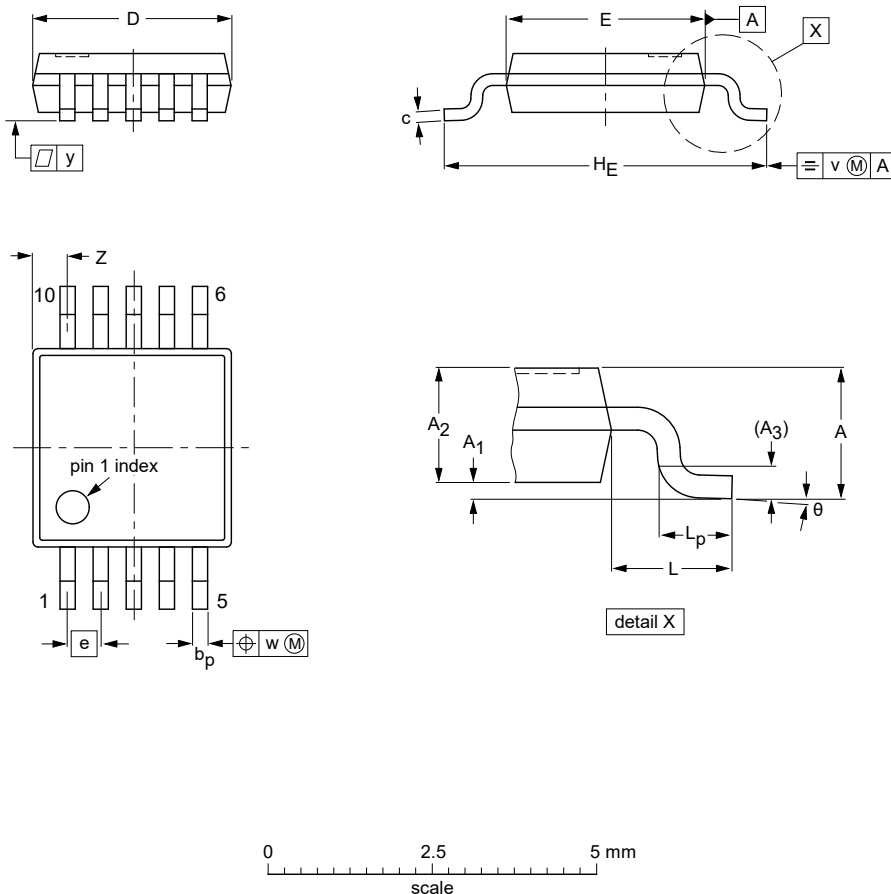
Table 12. Test data

Test	Load		Switch
	$R_L$	$C_L$	
$t_{v(Q)}$	500 $\Omega$	50 pF	$2 \times V_{DD}$

12 Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm

SOT552-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT552-1					99-07-29 03-02-18

Figure 19. Package outline SOT552-1 (TSSOP10)



## 13 Handling information

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All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 14 Soldering of SMD packages

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This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

**14.4 Reflow soldering**

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 20](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 13](#) and [Table 14](#)

**Table 13. SnPb eutectic process (from J-STD-020D)**

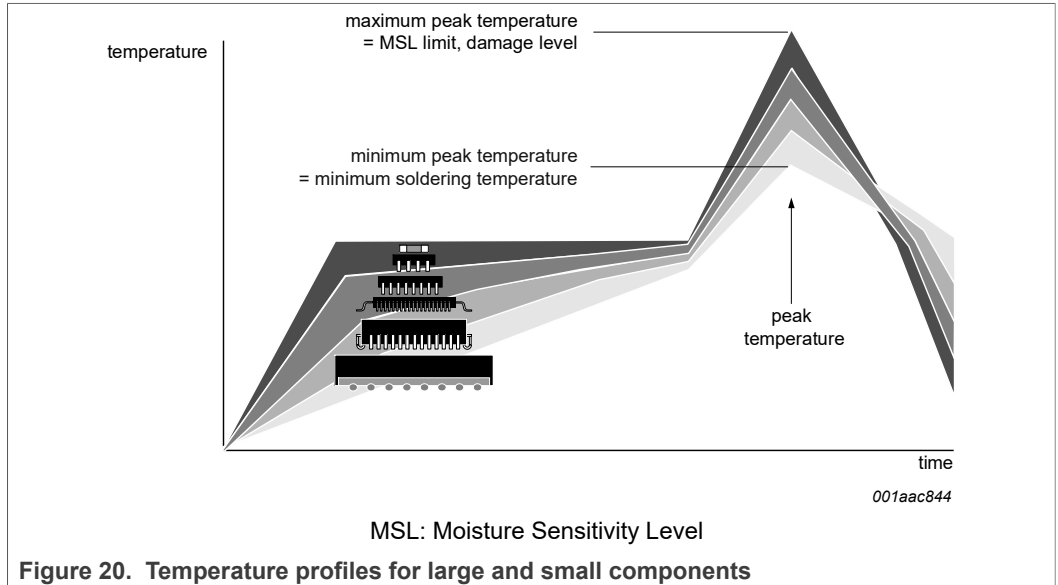
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 14. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 20](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 15 Abbreviations

Table 15. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General Purpose Input/Output
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
LP	Low-Pass
MM	Machine Model
POR	Power-On Reset
SMBus	System Management Bus

## 16 Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9537 v.7	20210908	Product data sheet	202104008A	PCA9537 v.6
Modifications	<ul style="list-style-type: none"> <li>Updated ordering information to reflect discontinuation of ATP-1 device and move to ASEN. See change notice column.</li> <li>The terms "master" and "slave" changed to "controller" and "target" to comply with NXP inclusive language policy.</li> </ul>			
PCA9537 v.6	20171107	Product data sheet	201710002I	PCA9537_5
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 10</a>: Corrected V<sub>POR</sub> typ and max limit</li> <li>Added <a href="#">Section 3.1</a></li> </ul>			
PCA9537_5	20090507	Product data sheet	-	PCA9537_4
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Pin names changed from "I/O0, I/O1, I/O2, I/O3" to "IO0, IO1, IO2, IO3", respectively</li> <li><a href="#">Section 6.4</a>, 1st sentence: changed symbol from "t<sub>W</sub>" to "t<sub>w(rst)</sub>"</li> <li><a href="#">Figure 5</a>: changed symbol from "t<sub>pV</sub>" to "t<sub>v(Q)</sub>"</li> <li><a href="#">Figure 8</a>: <ul style="list-style-type: none"> <li>changed symbol from "t<sub>ph</sub>" to "t<sub>h(D)</sub>"</li> <li>changed symbol from "t<sub>ps</sub>" to "t<sub>su(D)</sub>"</li> <li>changed symbol from "t<sub>iv</sub>" to "t<sub>v(INT)</sub>"</li> <li>changed symbol from "t<sub>ir</sub>" to "t<sub>rst(INT)</sub>"</li> </ul> </li> <li><a href="#">Table 9</a>: <ul style="list-style-type: none"> <li>parameter description for symbol V<sub>I/O</sub> changed from "DC voltage on an I/O" to "voltage on an input/output pin"</li> <li>parameter description for symbol I<sub>SS</sub> changed from "supply current" to "ground supply current"</li> <li>symbol/parameter changed from "I<sub>I/O</sub>, DC output current on an I/O" to "I<sub>O(ION)</sub>, output current on pin ION"</li> </ul> </li> <li><a href="#">Table 10</a>, sub-section "Supplies": <ul style="list-style-type: none"> <li>symbol/parameter changed from "I<sub>stbl</sub>, Standby current" to "I<sub>stbL</sub>, LOW-level standby current"</li> <li>symbol/parameter changed from "I<sub>stbh</sub>, Standby current" to "I<sub>stbH</sub>, HIGH-level standby current"</li> </ul> </li> <li><a href="#">Table 11</a>, sub-section "Port timing": <ul style="list-style-type: none"> <li>symbol/parameter changed from "t<sub>pV</sub>, Output data valid" to "t<sub>v(Q)</sub>, data output valid time"</li> <li>symbol/parameter changed from "t<sub>ps</sub>, Input data setup time" to "t<sub>su(D)</sub>, data input set-up time"</li> <li>symbol/parameter changed from "t<sub>ph</sub>, Input data hold time" to "t<sub>h(D)</sub>, data input hold time"</li> </ul> </li> <li><a href="#">Table 11</a>, sub-section "Interrupt timing": <ul style="list-style-type: none"> <li>symbol/parameter changed from "t<sub>iv</sub>, Interrupt valid" to "t<sub>v(INT)</sub>, valid time on pin <math>\overline{INT}</math>"</li> <li>symbol/parameter changed from "t<sub>ir</sub>, Interrupt reset" to "t<sub>rst(INT)</sub>, reset time on pin <math>\overline{INT}</math>"</li> </ul> </li> </ul>			

Table 16. Revision history...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications (continued):	<ul style="list-style-type: none"> <li>• <a href="#">Table 11</a>, sub-section "RESET": <ul style="list-style-type: none"> <li>– symbol changed from "t<sub>W</sub>" to "t<sub>w(rst)</sub>"</li> <li>– symbol changed from "t<sub>REC</sub>" to "t<sub>rec(rst)</sub>"</li> <li>– symbol/parameter changed from "t<sub>RESET</sub>, Time to reset" to "t<sub>rst</sub>, reset time"</li> </ul> </li> <li>• <a href="#">Figure 14</a>: <ul style="list-style-type: none"> <li>– symbol changed from "t<sub>W</sub>" to "t<sub>w(rst)</sub>"</li> <li>– symbol changed from "t<sub>REC</sub>" to "t<sub>rec(rst)</sub>"</li> <li>– symbol changed from "t<sub>RESET</sub>" to "t<sub>rst</sub>"</li> </ul> </li> <li>• <a href="#">Figure 15</a>: <ul style="list-style-type: none"> <li>– changed symbol from "t<sub>PH</sub>" to "t<sub>h(D)</sub>"</li> <li>– changed symbol from "t<sub>PS</sub>" to "t<sub>su(D)</sub>"</li> <li>– changed symbol from "t<sub>IV</sub>" to "t<sub>v(INT)</sub>"</li> <li>– changed symbol from "t<sub>IR</sub>" to "t<sub>rst(INT)</sub>"</li> </ul> </li> <li>• <a href="#">Figure 16</a>: changed symbol from "t<sub>PV</sub>" to "t<sub>v(Q)</sub>"</li> <li>• (Old) Figure 18, "Test circuit" split into <a href="#">Figure 18</a> and <a href="#">Table 12</a> <ul style="list-style-type: none"> <li>– symbol changed from "t<sub>PV</sub>" to "t<sub>v(Q)</sub>"</li> </ul> </li> <li>• Added soldering information</li> <li>• Added <a href="#">Table 15</a></li> </ul>			
PCA9537_4	20060921	Product data sheet	-	PCA9537_3
PCA9537_3 (9397 750 14259)	20041129	Product data sheet	-	PCA9537_2
PCA9537_2 (9397 750 14052)	20040930	Objective data sheet	-	PCA9537_1
PCA9537_1 (9397 750 12894)	20040820	Objective data sheet	-	-

## 17 Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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**4-bit I<sup>2</sup>C-bus and SMBus low power I/O port with interrupt and reset**

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