



# PCA9846

4-channel ultra-low voltage, Fm+ I<sup>2</sup>C-bus switch with reset

Rev. 1.1 — 4 April 2017

Product data sheet

## 1. General description

---

The PCA9846 is an ultra-low voltage, quad bidirectional translating switch controlled via the I<sup>2</sup>C-bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any or all SCx/SDx channels can be selected, determined by the programmable control register. This feature allows multiple devices with the same I<sup>2</sup>C-bus address to reside on the same bus. The switch device can also separate a heavily loaded I<sup>2</sup>C-bus into separate bus segments, eliminating the need for a bus buffer.

An active LOW reset input allows the PCA9846 to recover from a situation where one of the downstream I<sup>2</sup>C-buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I<sup>2</sup>C-bus state machine and deselects all the channels, as does the internal Power-On Reset (POR) function.

The pass gates of the switches are constructed such that the V<sub>DD1</sub> pin is used to limit the maximum high voltage which is passed by the PCA9846. This allows the use of different bus voltages on each channel, so that 0.8 V, 1.8 V, 2.5 V or 3.3 V parts can communicate without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 3.6 V tolerant.

## 2. Features and benefits

---

- Ultra-low voltage operation, down to 0.8 V to interface with next-generation CPUs
- 1-of-4 bidirectional translating switch
- Fm+ I<sup>2</sup>C-bus interface logic; compatible with SMBus standards
- Active LOW reset input
- 2 address pins allowing up to 16 devices on the I<sup>2</sup>C-bus
- Channel selection via I<sup>2</sup>C-bus
- Power-up with all switch channels deselected
- Low R<sub>on</sub> switches
- Allows voltage level translation between 0.8 V, 1.8 V, 2.5 V and 3.3 V buses
- Reset via I<sup>2</sup>C-bus software command
- I<sup>2</sup>C Device ID function
- No glitch on power-up
- Supports hot insertion since all channels are de-selected at power-on
- Low standby current



- 3.6 V tolerant inputs
- 0 Hz to 1 MHz clock frequency
- ESD protection exceeds 6000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Two packages offered: TSSOP16 and HVQFN16

### 3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9846BS <sup>[1]</sup>	846	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm	SOT629-1
PCA9846PW	PCA9846	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

[1] Package is in development. Contact NXP for availability.

#### 3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9846BS <sup>[1]</sup>	PCA9846BSJ	HVQFN16	Reel 13" Q1/T1 *Standard mark SMD	6000	T <sub>amb</sub> = -40 °C to +85 °C
PCA9846PW	PCA9846PWJ	TSSOP16	Reel 13" Q1/T1 *Standard mark SMD	2500	T <sub>amb</sub> = -40 °C to +85 °C
PCA9846PW	PCA9846PWZ	TSSOP16	Reel 13" Q1/T1 *Standard mark SMD	500	T <sub>amb</sub> = -40 °C to +85 °C

[1] Package is in development. Contact NXP for availability.

4. Block diagram

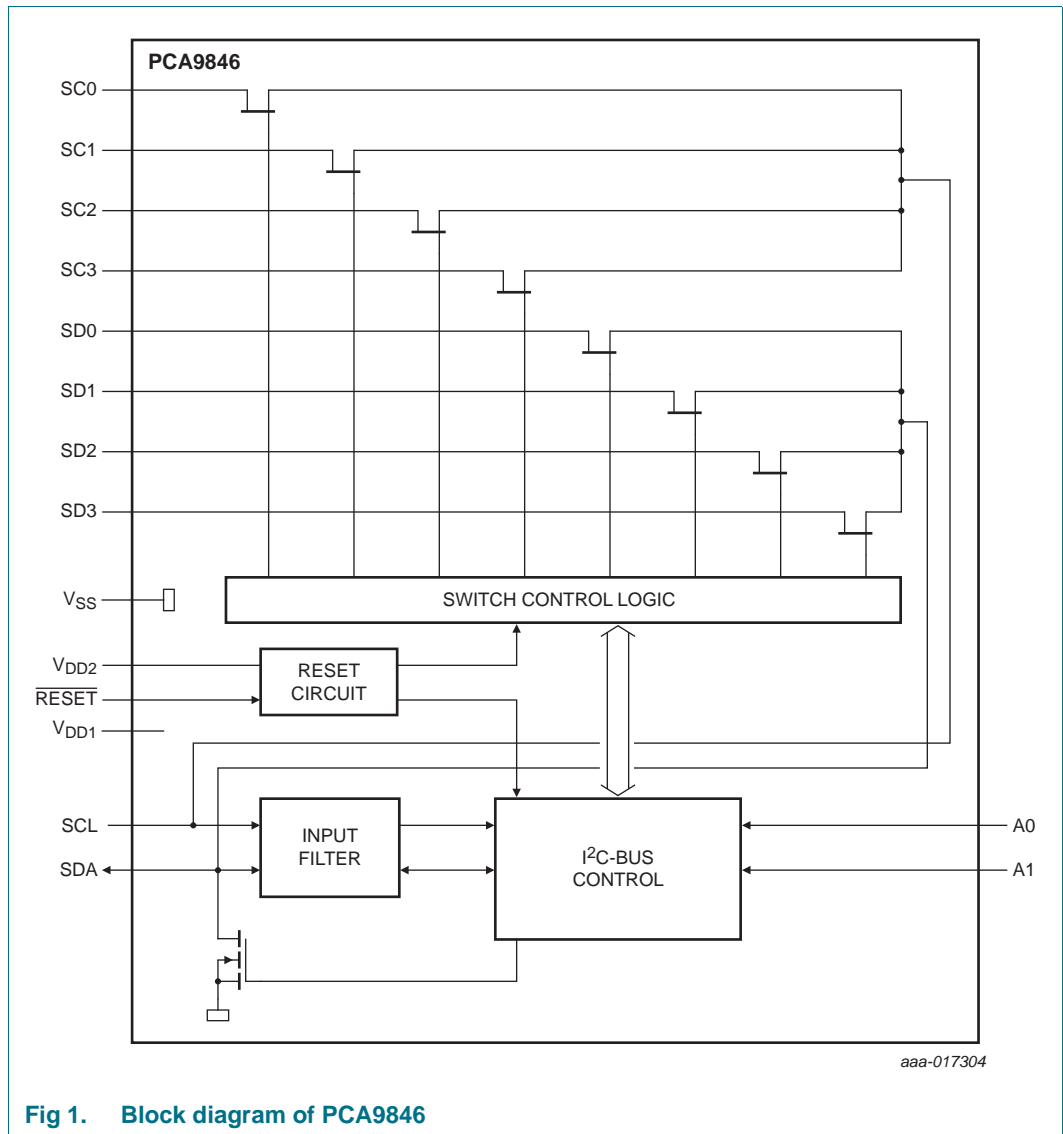


Fig 1. Block diagram of PCA9846

## 5. Pinning information

### 5.1 Pinning

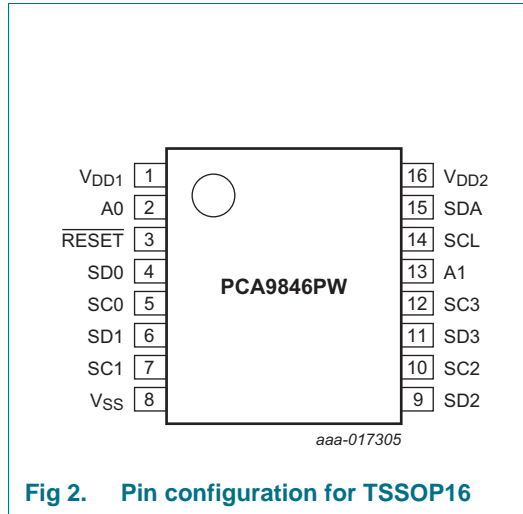


Fig 2. Pin configuration for TSSOP16

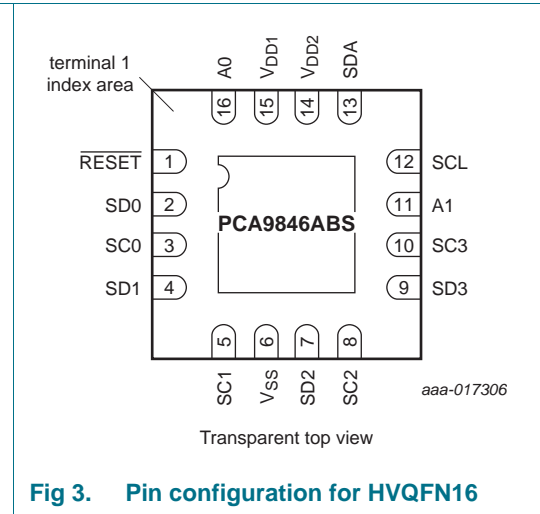


Fig 3. Pin configuration for HVQFN16

### 5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP16	HVQFN16	
V <sub>DD1</sub>	1	15	logic level power supply
A0	2	16	address input 0
RESET	3	1	active LOW reset input
SD0	4	2	serial data 0
SC0	5	3	serial clock 0
SD1	6	4	serial data 1
SC1	7	5	serial clock 1
V <sub>SS</sub>	8	6 <sup>[1]</sup>	supply ground
SD2	9	7	serial data 2
SC2	10	8	serial clock 2
SD3	11	9	serial data 3
SC3	12	10	serial clock 3
A1	13	11	address input 1
SCL	14	12	serial clock line
SDA	15	13	serial data line
V <sub>DD2</sub>	16	14	core logic power supply

[1] HVQFN16 package die supply ground is connected to both the V<sub>SS</sub> pin and the exposed center pad. The V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9846”](#).

### 6.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9846 is shown in [Figure 4](#). The device pins A0 and A1 must be connected to a valid logic signal — HIGH, LOW, SCL or SDA — to ensure a valid slave address, since no internal pull-up resistors are provided.

1	X	1	X	X	X	X	R/W
---	---	---	---	---	---	---	-----

X = programmable by hardware

aaa-011933

See [Table 4](#).

**Fig 4. Slave address**

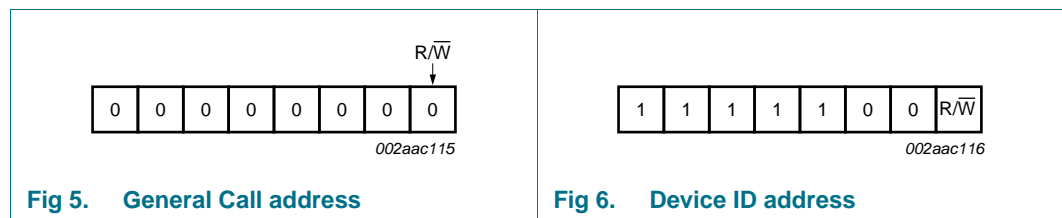
Table 4. Address selection

PCA9846 address pins		8-bit I <sup>2</sup> C-bus address	Slave address/bit pattern master must send							
A1	A0		A7	A6	A5	A4	A3	A2	A1	A0 - R/W
0	SCL	0xE0h	1	1	1	0	0	0	0	0/1
0	0	0xE2h	1	1	1	0	0	0	1	0/1
0	SDA	0xE4h	1	1	1	0	0	1	0	0/1
0	1	0xE6h	1	1	1	0	0	1	1	0/1
1	SCL	0xE8h	1	1	1	0	1	0	0	0/1
1	0	0xEAh	1	1	1	0	1	0	1	0/1
1	SDA	0xECh	1	1	1	0	1	1	0	0/1
1	1	0xEEh	1	1	1	0	1	1	1	0/1
SCL	SCL	0xB0h	1	0	1	1	0	0	0	0/1
SCL	0	0xB2h	1	0	1	1	0	0	1	0/1
SCL	SDA	0xB4h	1	0	1	1	0	1	0	0/1
SCL	1	0xB6h	1	0	1	1	0	1	1	0/1
SDA	SCL	0xB8h	1	0	1	1	1	0	0	0/1
SDA	0	0xBAh	1	0	1	1	1	0	1	0/1
SDA	SDA	0xBCh	1	0	1	1	1	1	0	0/1
SDA	1	0xBEh	1	0	1	1	1	1	1	0/1

## 6.2 Software Reset General Call, and device ID addresses

Two other different addresses can be sent to the device.

- General Call address: allows to reset the device through the I<sup>2</sup>C-bus upon reception of the right I<sup>2</sup>C-bus sequence. See [Section 6.2.1 “Software Reset”](#) for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See [Section 6.2.2 “Device ID \(PCA9846 ID field\)”](#) for more information.



6.2.1 Software Reset

The Software Reset Call allows all the devices in the I<sup>2</sup>C-bus to be reset to the power-up state value through a specific formatted I<sup>2</sup>C-bus command. To be performed correctly, it implies that the I<sup>2</sup>C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I<sup>2</sup>C-bus master.
2. The reserved General Call I<sup>2</sup>C-bus address '0000 000' with the R/W bit set to 0 (write) is sent by the I<sup>2</sup>C-bus master.
3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/W bit is set to 1 (read), no acknowledge is returned to the I<sup>2</sup>C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
  - a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

If more than 1 byte of data is sent, the device does not acknowledge any more.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I<sup>2</sup>C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in [Figure 7](#).

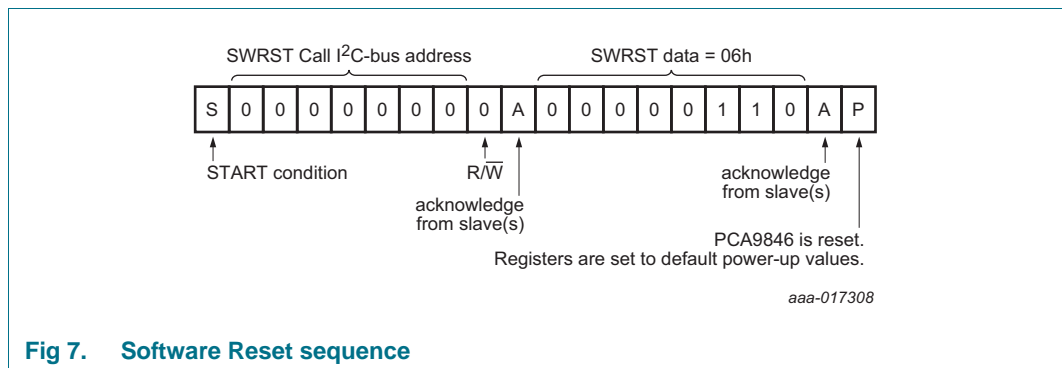


Fig 7. Software Reset sequence

### 6.2.2 Device ID (PCA9846 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I<sup>2</sup>C-bus address followed by the R/W bit set to 0 (write): '1111 1000'.
3. The master sends the I<sup>2</sup>C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I<sup>2</sup>C-bus slave address).
4. The master sends a Re-START command.

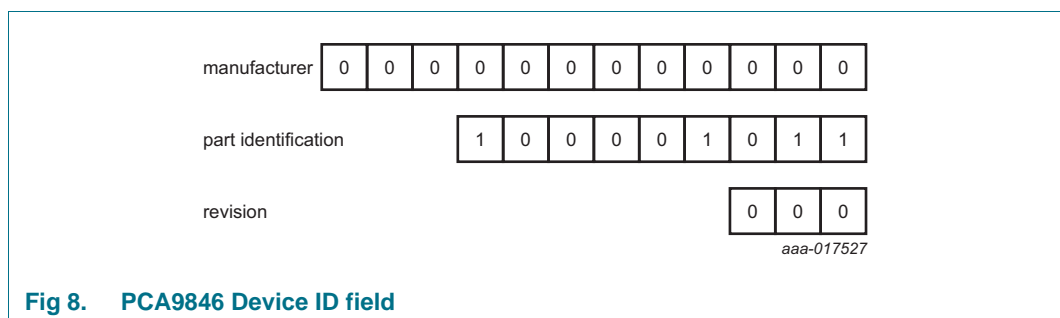
**Remark:** A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.

5. The master sends the Reserved Device ID I<sup>2</sup>C-bus address followed by the R/W bit set to 1 (read): '1111 1001'.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

**Remark:** The reading of the Device ID can be stopped anytime by sending a NACK command.

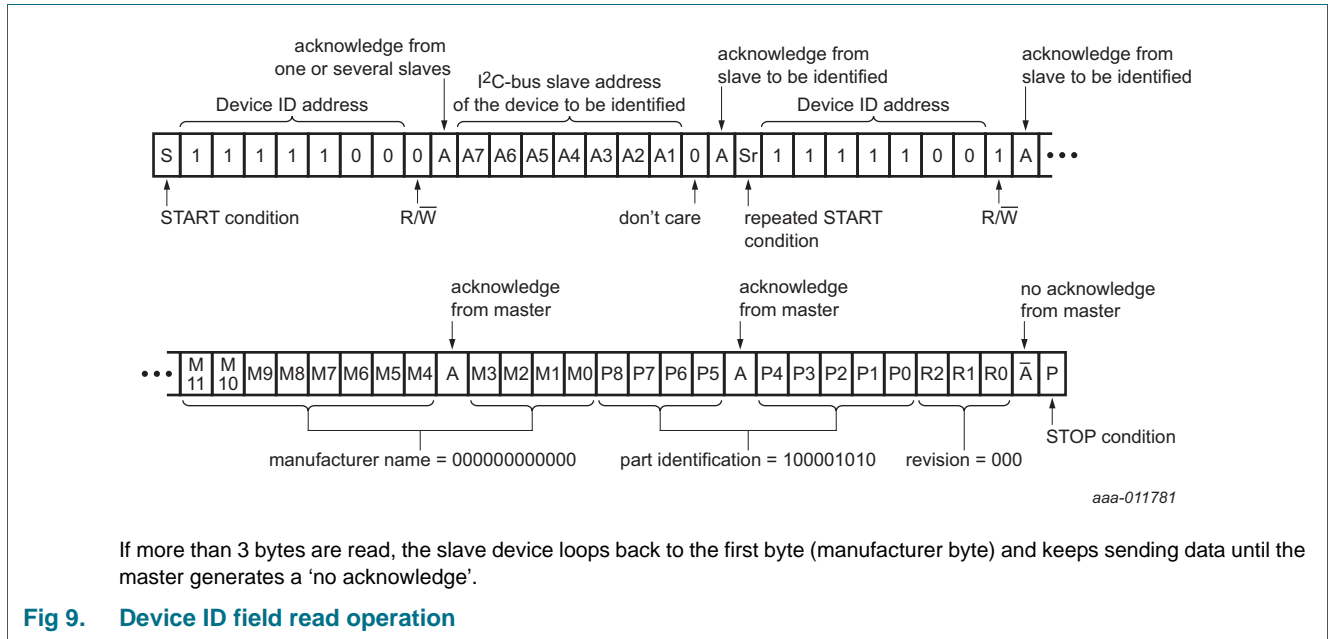
If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCA9846, the Device ID is shown in [Figure 8](#).



**Fig 8. PCA9846 Device ID field**





If more than 3 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

Fig 9. Device ID field read operation

### 6.3 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9846, which will be stored in the control register. If multiple bytes are received by the PCA9846, it will save the last byte received. This register can be written and read via the I<sup>2</sup>C-bus.

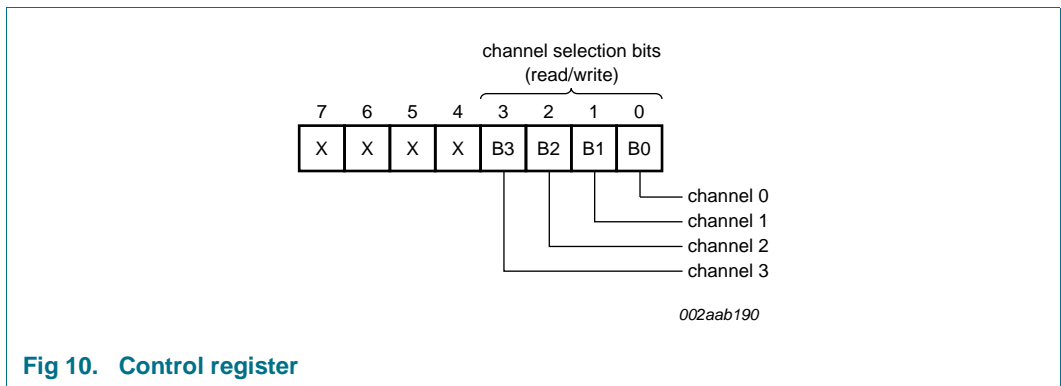


Fig 10. Control register

### 6.3.1 Control register definition

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9846 has been addressed. All 8 bits of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, it will become active after a STOP condition has been placed on the I<sup>2</sup>C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection. Notice that multiple channels may simultaneously be selected.

**Table 5. Control register**

*Write = channel selection; Read = channel status*

D7	D6	D5	D4	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
								1
X	X	X	X	X	0	X	X	channel 2 disabled
								1
X	X	X	X	0	X	X	X	channel 3 disabled
								1
0	0	0	0	0	0	0	0	no channel selected; power-up/reset default state

**Remark:** Several channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and channel 3 are disabled and channel 1 and channel 2 are enabled. Care should be taken not to exceed the maximum bus capacitance.

### 6.4 RESET input

The  $\overline{\text{RESET}}$  input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of  $t_{w(\text{rst})L}$ , the PCA9846 will reset its registers and I<sup>2</sup>C-bus state machine and will deselect all channels.

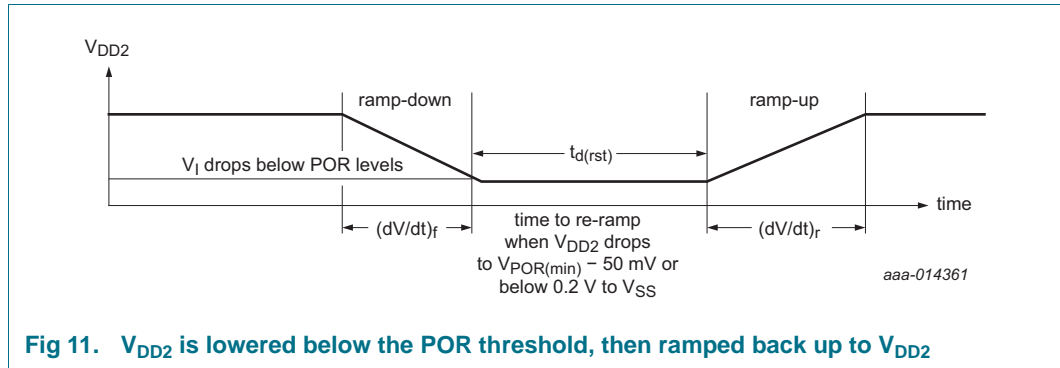
### 6.5 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the PCA9846 in a reset condition until  $V_{DD2}$  has reached  $V_{POR}$ . At this point, the reset condition is released and the PCA9846 registers and I<sup>2</sup>C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected.

### 6.6 Power-on reset requirements

In the event of a glitch or data corruption, PCA9846 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

Power-on reset is shown in [Figure 11](#).



**Fig 11.** V<sub>DD2</sub> is lowered below the POR threshold, then ramped back up to V<sub>DD2</sub>

Table 6 specifies the performance of the power-on reset feature for PCA9846 for both types of power-on reset.

**Table 6. Recommended supply sequencing and ramp rates**

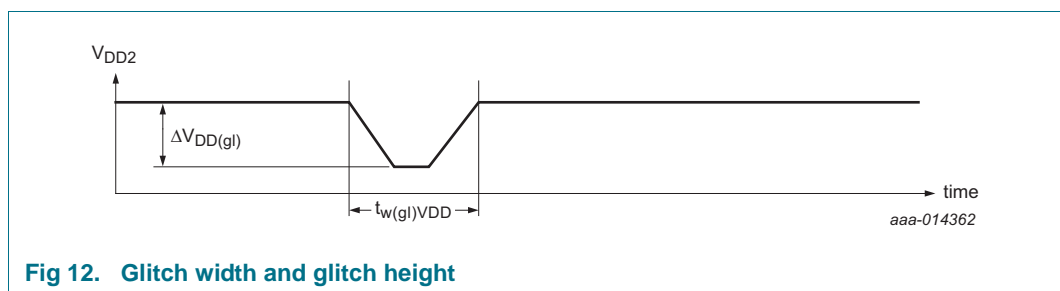
T<sub>amb</sub> = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
(dV/dt) <sub>f</sub>	fall rate of change of voltage	Figure 11	0.1	-	2000	ms
(dV/dt) <sub>r</sub>	rise rate of change of voltage	Figure 11	0.1	-	2000	ms
t <sub>d(rst)</sub>	reset delay time	Figure 11; re-ramp time when V <sub>DD2</sub> drops to V <sub>POR(min)</sub> - 50 mV) or below 0.2 V to V <sub>SS</sub>	1	-	-	μs
ΔV <sub>DD(gl)</sub>	glitch supply voltage difference	Figure 12	[1]	-	-	V
t <sub>w(gl)VDD</sub>	supply voltage glitch pulse width	Figure 12	[2]	-	-	μs
V <sub>POR(trip)</sub>	power-on reset trip voltage	falling V <sub>DD2</sub>	0.7	-	-	V
		rising V <sub>DD2</sub>	-	-	1.5	V

[1] Level that V<sub>DD2</sub> can glitch down to with a ramp rate = 0.4 μs/V, but not cause a functional disruption when t<sub>w(gl)VDD</sub> < 1 μs.

[2] Glitch width that will not cause a functional disruption when ΔV<sub>DD(gl)</sub> = 0.5 × V<sub>DD2</sub>.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t<sub>w(gl)VDD</sub>) and glitch height (ΔV<sub>DD(gl)</sub>) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 12 and Table 6 provide more information on how to measure these specifications.



**Fig 12.** Glitch width and glitch height

V<sub>POR</sub> is critical to the power-on reset. V<sub>POR</sub> is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C-bus/SMBus state machine are initialized to their default states. The value of V<sub>POR</sub> differs based on the V<sub>DD2</sub> being lowered to or from 0 V. Figure 13 and Table 6 provide more details on this specification.

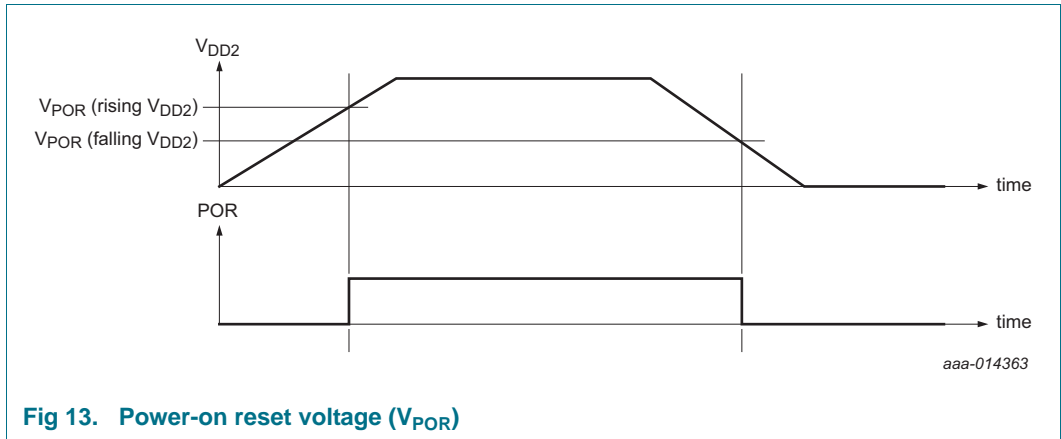


Fig 13. Power-on reset voltage ( $V_{POR}$ )

## 6.7 Voltage level translation between I<sup>2</sup>C-buses

Today's complex systems often use multiple power supplies to maximize power savings and to meet the operating specifications of the devices used. This means that various I<sup>2</sup>C-buses are also operating at differing voltage levels and cannot simply connect together. In addition, modern microcontrollers operate down to 0.8 V to save power, further complicating the connection of I<sup>2</sup>C-buses.

The PCA9846 is specifically designed to seamlessly handle these voltage level translation issues. Any combination of bus voltages can be intermixed on the PCA9846 and correctly translated to the other bus at Fm+ (1 MHz) speed.

[Figure 14](#) shows a typical application. The microcontroller acts as the master and operates at 0.8 V with its I<sup>2</sup>C-bus swinging between 0 V and 0.8 V. The temperature sensor on channel 0 of the PCA9846 has a operates at 3.3 V, while the GPIO Expander on channel 1 operates down to 1.8 V to interface with chip select and reset inputs on various other ICs also operating at 1.8 V. Channel 2 of the PCA9846 is connected to the I<sup>2</sup>C-bus of a power management device, operating at 2.5 V. The other channels of PCA9846 are simply left unconnected.

In this example,  $V_{DD1}$  of the PCA9846 is a bias supply and is set at the lowest bus voltage, or 0.8 V of the microcontroller.  $V_{DD1}$  sets the input switching points of each SCL and SDA at  $0.3 \times V_{DD1}$  for a LOW level and  $0.7 \times V_{DD1}$  for a HIGH level.

$V_{DD2}$  is the core logic supply from which most of the PCA9846 circuitry runs and must be greater than 1.65 V.

The I<sup>2</sup>C-bus is open-drain, so pull-up resistors are needed on each I<sup>2</sup>C-bus segment. This is where the voltage level translation happens. The pass transistor internal to the PCA9846 limit the output voltage to the lower of  $V_{DD1}$  or  $V_{DD2}$ . The pull-up resistors will then limit the HIGH level of each bus segment to the power supply of the devices on that segment. Note that the pull-up resistors on channel 0 are connected to 3.3 V, the and resistors on channel 1 are connected to 1.8 V, while the resistors on channel 2 are connected to 2.5 V — effectively translating the 0.8 V signal swing of the microcontroller to the correct voltage level for each peripheral.

It is possible to level shift from a higher voltage microcontroller connected to  $V_{DD1}$  to lower voltage peripherals on the downstream side — the opposite of this particular example, as long as  $V_{DD1} > 0.8$  V and  $V_{DD2} > 1.65$  V.

One thing to note is noise margin on each I<sup>2</sup>C-bus segment is somewhat reduced due to the input levels set by  $V_{DD1}$ . Especially in this example, the I<sup>2</sup>C-bus LOW level is  $0.3 \times V_{DD1}$  or 0.24 V, so extreme care must be taken to ensure all bus segments meet this specification. It also means that static offset buffers may not work correctly if the offset side is connected to the PCA9846.

Another point to examine is that there is no buffering capability between the upstream and the downstream buses. This is simply a pass transistor, which acts like a switch and a series resistor, between these bus segments. The series resistance is the  $R_{on}$  of the pass transistor and is inversely proportional to the minimum of  $V_{DD1} + V_{TH}$  or  $V_{DD2}$ , where  $V_{TH}$  is approximately 0.8 V. Refer to [Table 8](#) for some representative  $R_{on}$  values. An upcoming application note will explain  $R_{on}$  more thoroughly. Therefore, a careful analysis of bus capacitance and pull-up resistor values is called for.

4-channel ultra-low voltage, Fm+ I<sup>2</sup>C-bus switch with reset

A further point to consider is pull-up resistor selection. Since multiple channels can be simultaneously selected, the pull-up resistors on each channel are connected in parallel. Ensure each device can correctly drive the effective pull-up resistor value and still meet the LOW-level specifications.

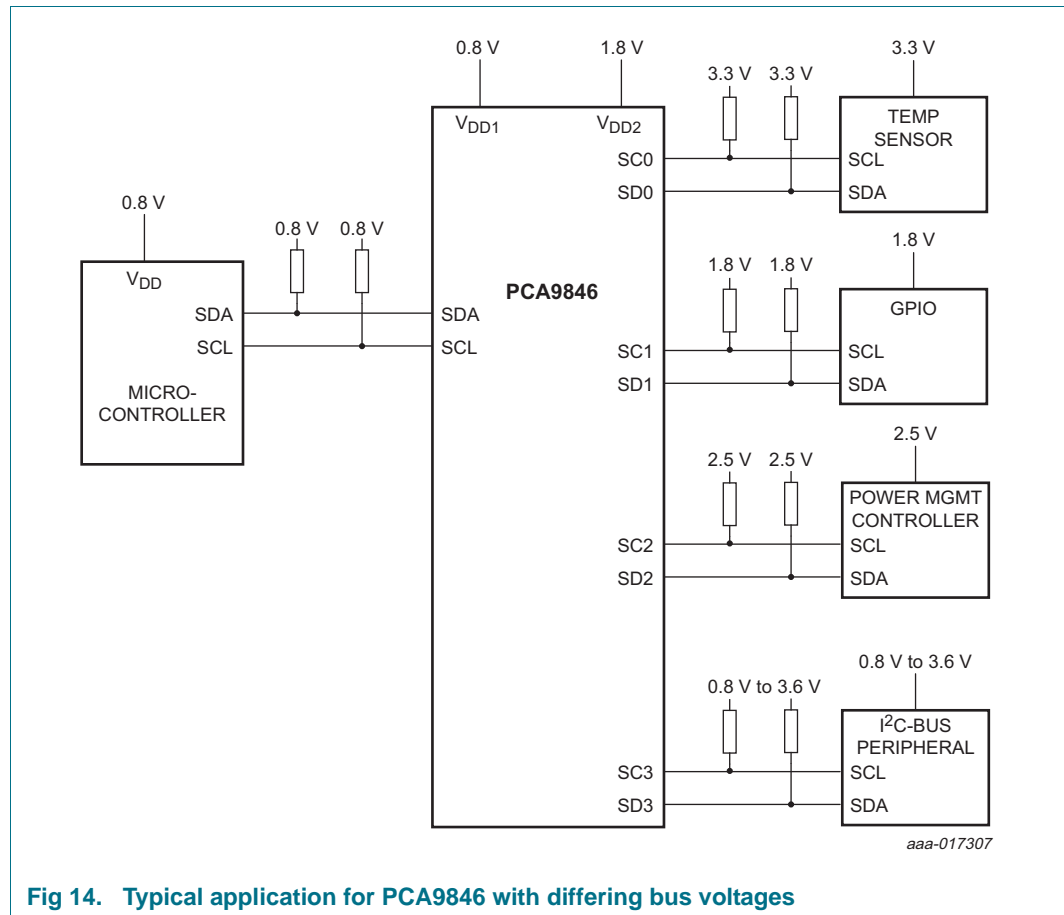


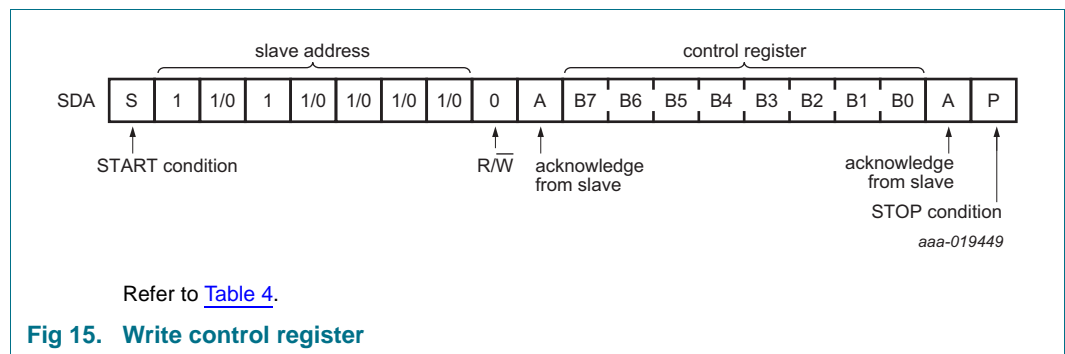
Fig 14. Typical application for PCA9846 with differing bus voltages

## 7. Characteristics of the I<sup>2</sup>C-bus

The PCA9846 is an I<sup>2</sup>C slave device. Data is exchanged between the master and the PCA9846 through write and read commands conforming to the I<sup>2</sup>C-bus protocol. The two communication lines are SCL (serial clock) and SDA (serial data), both of which must be connected to V<sub>DD1</sub> through pull-up resistors.

### 7.1 Write commands

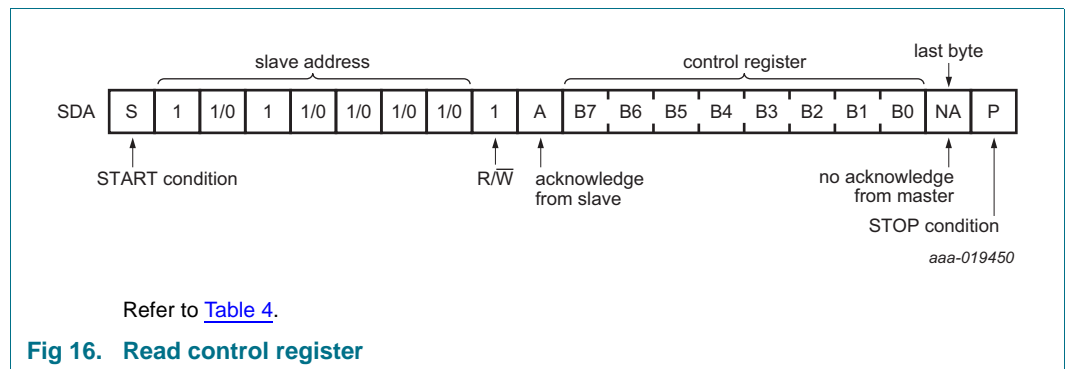
Data is transmitted to the PCA9846 by sending its device address and setting the Least Significant Bit (LSB) to a logic 0 (see [Table 4](#) for device addresses), which the PCA9846 acknowledges (ACK). The control register byte is sent after the address that determines which downstream channel is connected to the upstream channel by bit 0 through bit 2. Bit 7 through bit 3 are ignored and can be written with any data. There is no limit on the number of bytes sent after the address and before a STOP condition, only the last byte written before the STOP condition is recognized and the selected channel is enabled only at the following STOP condition.



### 7.2 Read commands

Data is read from the PCA9846 by sending its device address and setting the Least Significant Bit (LSB) to a logic 1 (see [Table 4](#) for device addresses), which the PCA9846 acknowledges. The control register byte is read by the master with each byte either ACK or NACK by the master. If the master ACKs the control register byte, it continues to send register data until the master NACKs, signaling the transaction is complete. There is no limit on the number of bytes read from the PCA9846.

The control register bit definitions are shown in [Figure 10](#). Bit 0 through bit 2 will show the enabled channels (as determined by the last write).



## 8. Limiting values

**Table 7. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages are referenced to  $V_{SS}$  (ground = 0 V)<sup>[1]</sup>.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+4.0	V
$V_I$	input voltage		-0.5	+4.0	V
$I_I$	input current		-	±20	mA
$I_O$	output current		-	±25	mA
$I_{DD}$	supply current		-	±100	mA
$I_{SS}$	ground supply current		-	±100	mA
$P_{tot}$	total power dissipation		-	400	mW
$T_{stg}$	storage temperature		-60	+150	°C
$T_{amb}$	ambient temperature	operating	-40	+85	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

## 9. Static characteristics

**Table 8. Static characteristics**

$V_{SS} = 0$  V;  $T_{amb} = -40$  °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
$V_{DD1}$	supply voltage 1		0.8	-	3.6	V
$V_{DD2}$	supply voltage 2		1.65	-	3.6	V
$I_{DD}(V_{DD2})$	supply current on pin $V_{DD2}$	$V_{DD1} = 3.6$ V, $V_{DD2} = 3.6$ V; SC0 to SC7 and SD0 to SD7 not connected; RESET = $V_{DD1}$ ; A0 = A1 = SCL; continuous register read/write				
		$f_{SCL} = 0$ kHz	-	5	12	μA
		$f_{SCL} = 100$ kHz	-	8	20	μA
		$f_{SCL} = 1000$ kHz	-	65	150	μA
$I_{DD}(V_{DD1})$	supply current on pin $V_{DD1}$	$V_{DD1} = 3.6$ V, $V_{DD2} = 3.6$ V; SC0 to SC7 and SD0 to SD7 not connected; RESET = $V_{DD1}$ ; A0 = A1 = SCL; continuous register read/write				
		$f_{SCL} = 0$ kHz	-5	-2	+2	μA
		$f_{SCL} = 100$ kHz	-	5	15	μA
		$f_{SCL} = 1000$ kHz	-	45	100	μA
$V_{POR}$	power-on reset voltage		-	1.2	1.5	V



**Table 8. Static characteristics ...continued** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C}$  to  $+85\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Input SCL; input/output SDA</b>						
$V_{IL}$	LOW-level input voltage	$V_{DD1} \leq 1.1\text{ V}$	-0.5	-	$+0.2V_{DD1}$	V
		$V_{DD1} > 1.1\text{ V}$	-0.5	-	$+0.3V_{DD1}$	V
$V_{IH}$	HIGH-level input voltage	$V_{DD1} \leq 1.1\text{ V}$	$0.8V_{DD1}$	-	3.6	V
		$V_{DD1} > 1.1\text{ V}$	$0.7V_{DD1}$	-	3.6	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$ ; $V_{DD2} \leq 2\text{ V}$	15	-	-	mA
		$V_{OL} = 0.4\text{ V}$ ; $V_{DD2} > 2\text{ V}$	20	-	-	mA
$I_L$	leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$ ; all channels disabled	[1]	20	40	pF
<b>Select inputs A0 to A1, RESET</b>						
$V_{IL}$	LOW-level input voltage	$V_{DD1} \leq 1.1\text{ V}$	-0.5	-	$+0.2V_{DD1}$	V
		$V_{DD1} > 1.1\text{ V}$	-0.5	-	$+0.3V_{DD1}$	V
$V_{IH}$	HIGH-level input voltage	$V_{DD1} \leq 1.1\text{ V}$	$0.8V_{DD1}$	-	3.6	
		$V_{DD1} > 1.1\text{ V}$	$0.7V_{DD1}$	-	3.6	V
$I_{LI}$	input leakage current	pin at $V_{DD2}$ to 3.6 V or $V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$ or $V_{DD1}$	[1]	5	10	pF
<b>Pass gate</b>						
$R_{on}$	ON-state resistance	ON resistance of the pass transistor between SCL and SCx, and SDA and SDx				
		$V_{DD1} = 0.8\text{ V}$ ; $V_{DD2} \geq 1.65\text{ V}$ ; $V_{i(sw)} = 0.16\text{ V}$ ; $I_O = 3\text{ mA}$	-	15	24	$\Omega$
		$V_{DD1} = 1.2\text{ V}$ ; $V_{DD2} \geq 1.8\text{ V}$ ; $V_{i(sw)} = 0.24\text{ V}$ ; $I_O = 6\text{ mA}$	-	12	18	$\Omega$
		$V_{DD1} > 2\text{ V}$ ; $V_{DD2} \geq 2.5\text{ V}$ ; $V_{i(sw)} = 0.4\text{ V}$ ; $I_O = 20\text{ mA}$	-	7	10	$\Omega$
$I_{o(sw)}$	switch output current	$V_{DD2} = 1.65\text{ V}$ to $3.6\text{ V}$ ; $V_{i(sw)} = V_{DD1}$ to $3.6\text{ V}$ ; $V_{o(sw)} = V_{DD1}$ to $3.6\text{ V}$	0	-	100	$\mu\text{A}$
$I_L$	leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_{io}$	input/output capacitance	$V_I = V_{SS}$ ; all switches disabled	[1]	8	15	pF

[1] Not tested in production. Guaranteed by design and characterization.

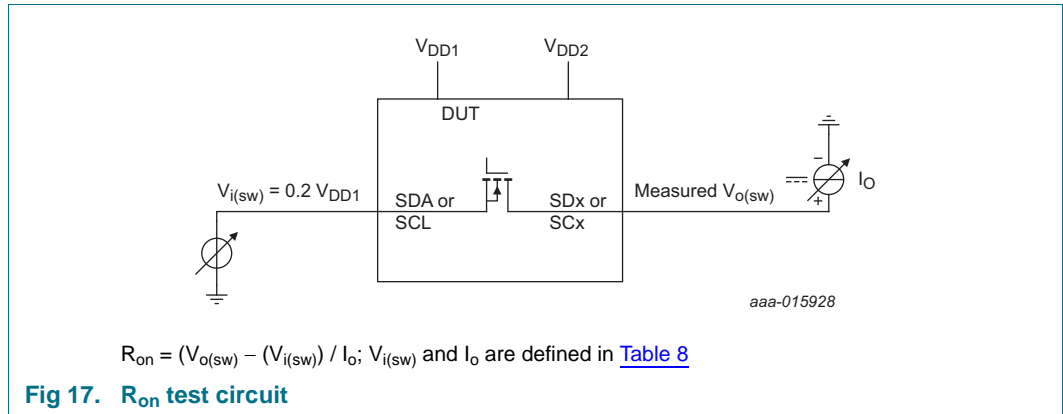


Table 9. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Fast-mode Plus I <sup>2</sup> C-bus	
			Min	Max	Min	Max	Min	Max
t <sub>PD</sub>	propagation delay	from SDA to SDx, or SCL to SCx	-	1 <sup>[1]</sup>	-	1 <sup>[1]</sup>	-	1
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	0	1000
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-
t <sub>HD;STA</sub>	hold time (repeated) START condition	<sup>[2]</sup>	4.0	-	0.6	-	0.26	-
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-
t <sub>SU;STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	0.26	-
t <sub>HD;DAT</sub>	data hold time		0 <sup>[3]</sup>	3.45	0 <sup>[3]</sup>	0.9	0	-
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	50	-
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	20 × (V <sub>DD</sub> / 5.5 V) <sup>[4]</sup>	300	-	-
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	20 × (V <sub>DD</sub> / 5.5 V) <sup>[4]</sup>	300	20 × (V <sub>DD</sub> / 5.5 V) <sup>[4]</sup>	1000
C <sub>b</sub>	capacitive load for each bus line		-	400	-	400	-	-
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	0	50
t <sub>VD;DAT</sub>	data valid time	<sup>[7]</sup>	-	3.45	-	0.9	-	0
t <sub>VD;ACK</sub>	data valid acknowledge time		-	1	-	1	-	0
<b>RESET</b>								
t <sub>w(rst)L</sub>	LOW-level reset time		100	-	100	-	100	-
t <sub>rst</sub>	reset time	SDA clear	500	-	500	-	500	-
t <sub>REC;STA</sub>	recovery time to START condition		0	-	0	-	0	-

- [1] Pass gate propagation delay is calculated from the 20 Ω typical R<sub>on</sub> and the 50 pF load capacitance.
- [2] After this period, the first clock pulse is generated.
- [3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH(min)</sub> of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
- [4] Necessary to be backwards compatible to Fast-mode.
- [5] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- [6] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
- [7] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.
- [8] The maximum t<sub>HD;DAT</sub> could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode, but must be less than the maximum of t<sub>VD;DAT</sub> or t<sub>VD;ACK</sub> by a transition time. This maximum must only be met if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

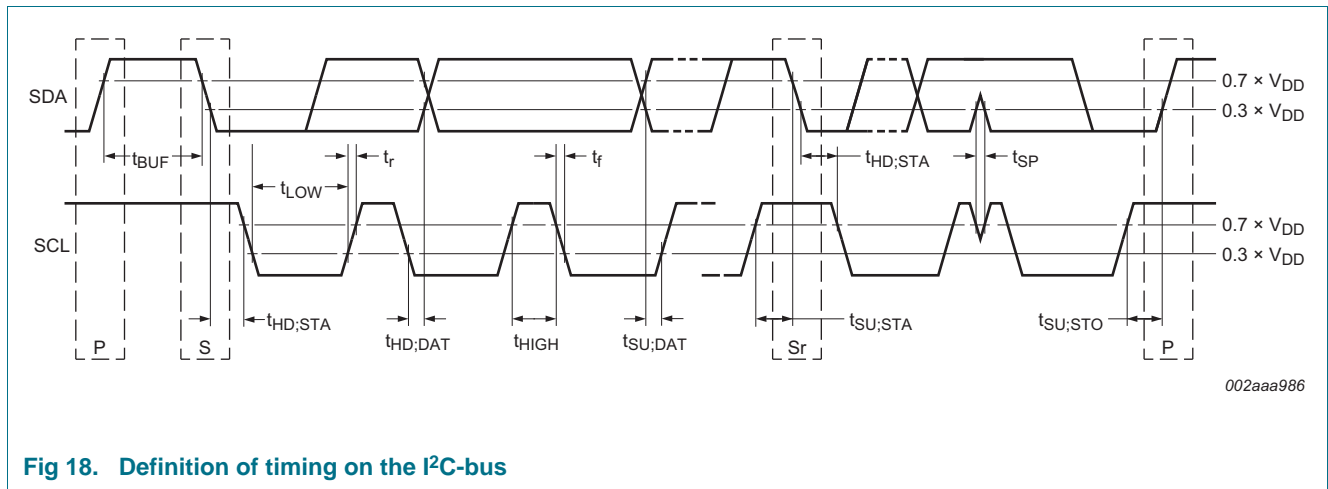


Fig 18. Definition of timing on the I<sup>2</sup>C-bus

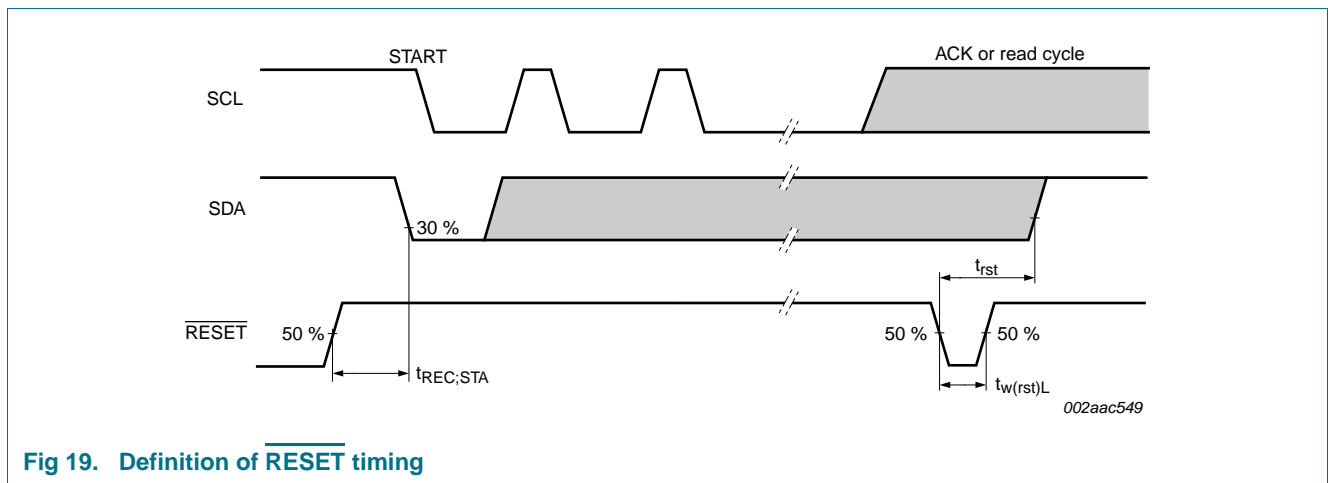
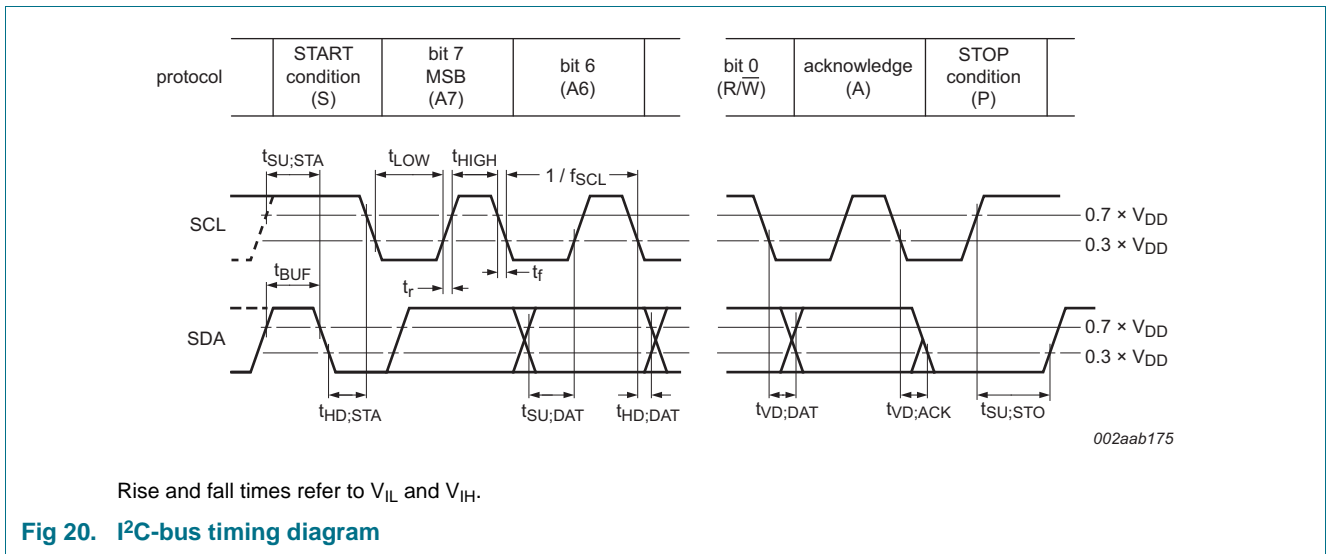


Fig 19. Definition of RESET timing



### 11. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

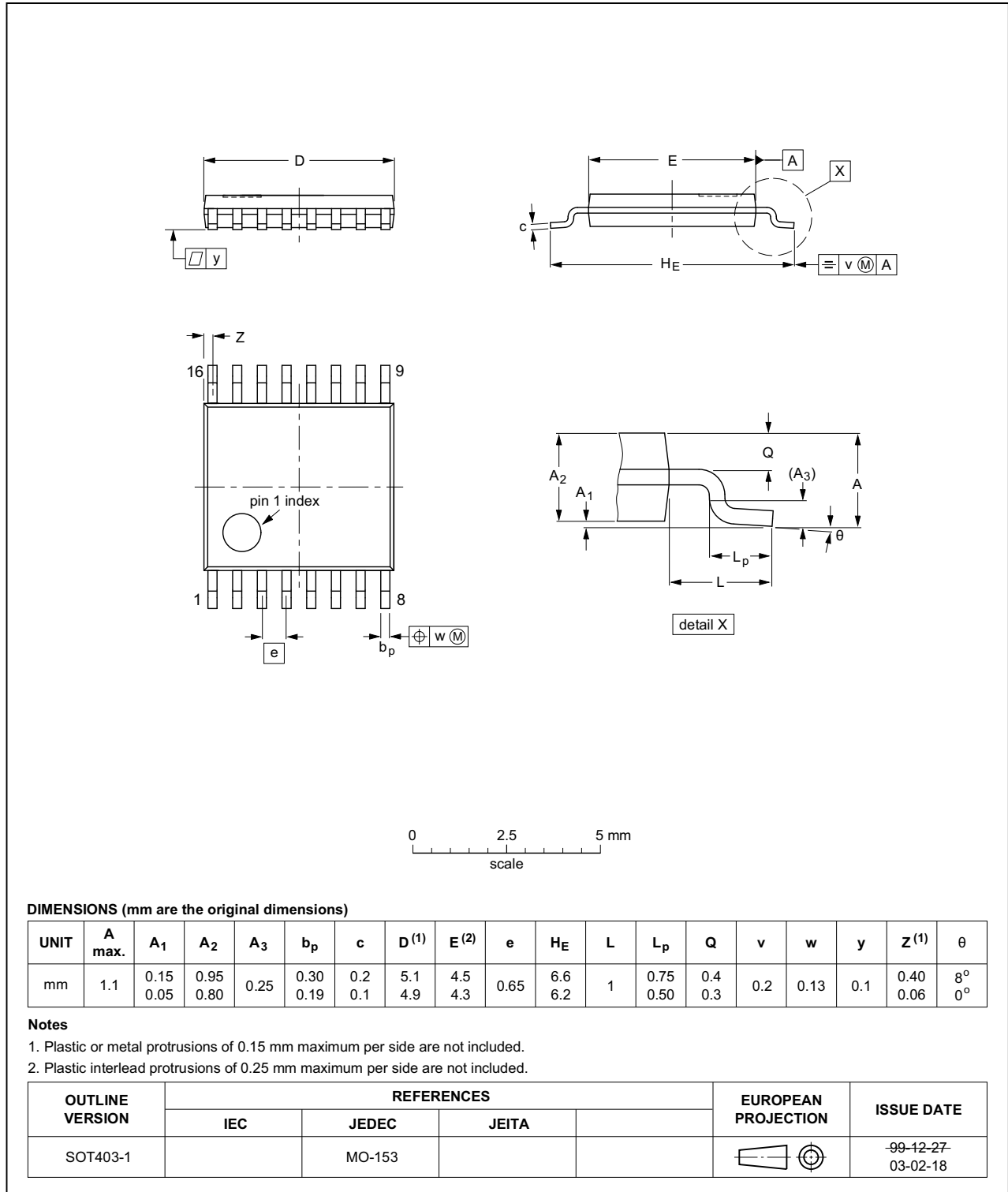


Fig 21. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads;  
16 terminals; body 4 x 4 x 0.85 mm

SOT629-1

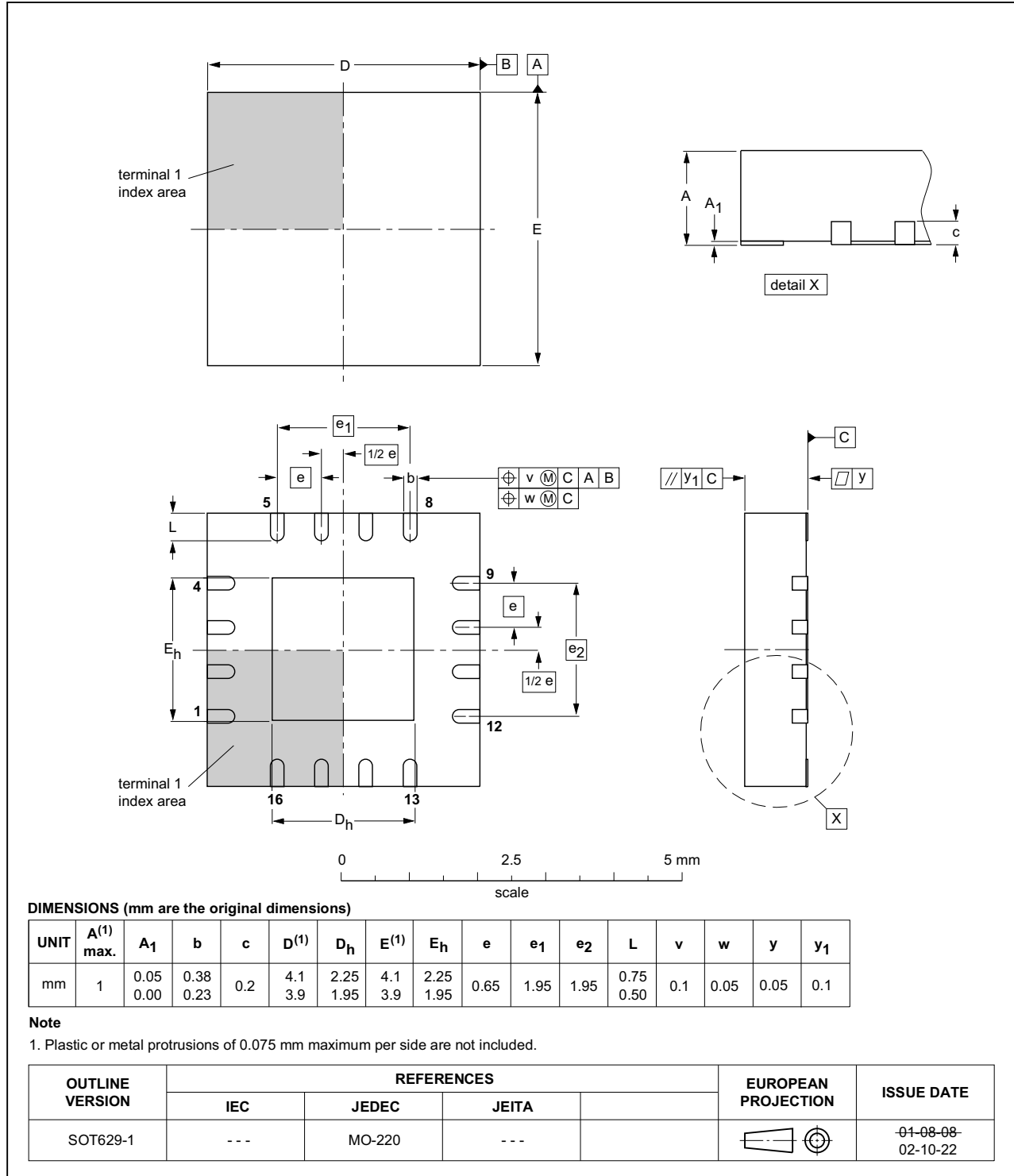


Fig 22. Package outline SOT629-1 (HVQFN16)

## 12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities



## 12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 23](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [11](#)

**Table 10. SnPb eutectic process (from J-STD-020D)**

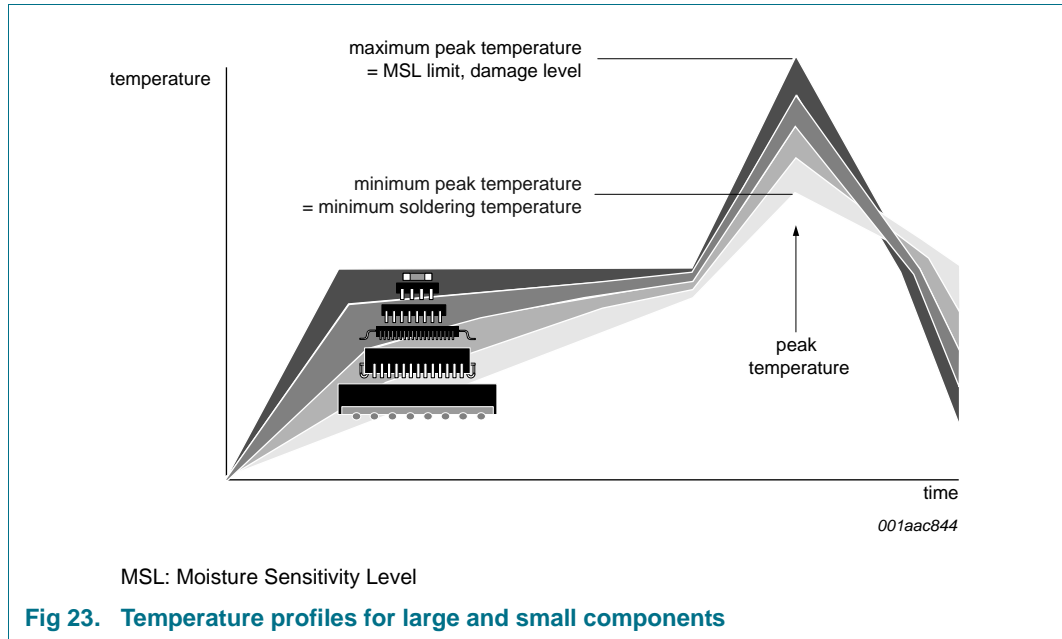
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 11. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 23](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

### 13. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP16 package

SOT403-1

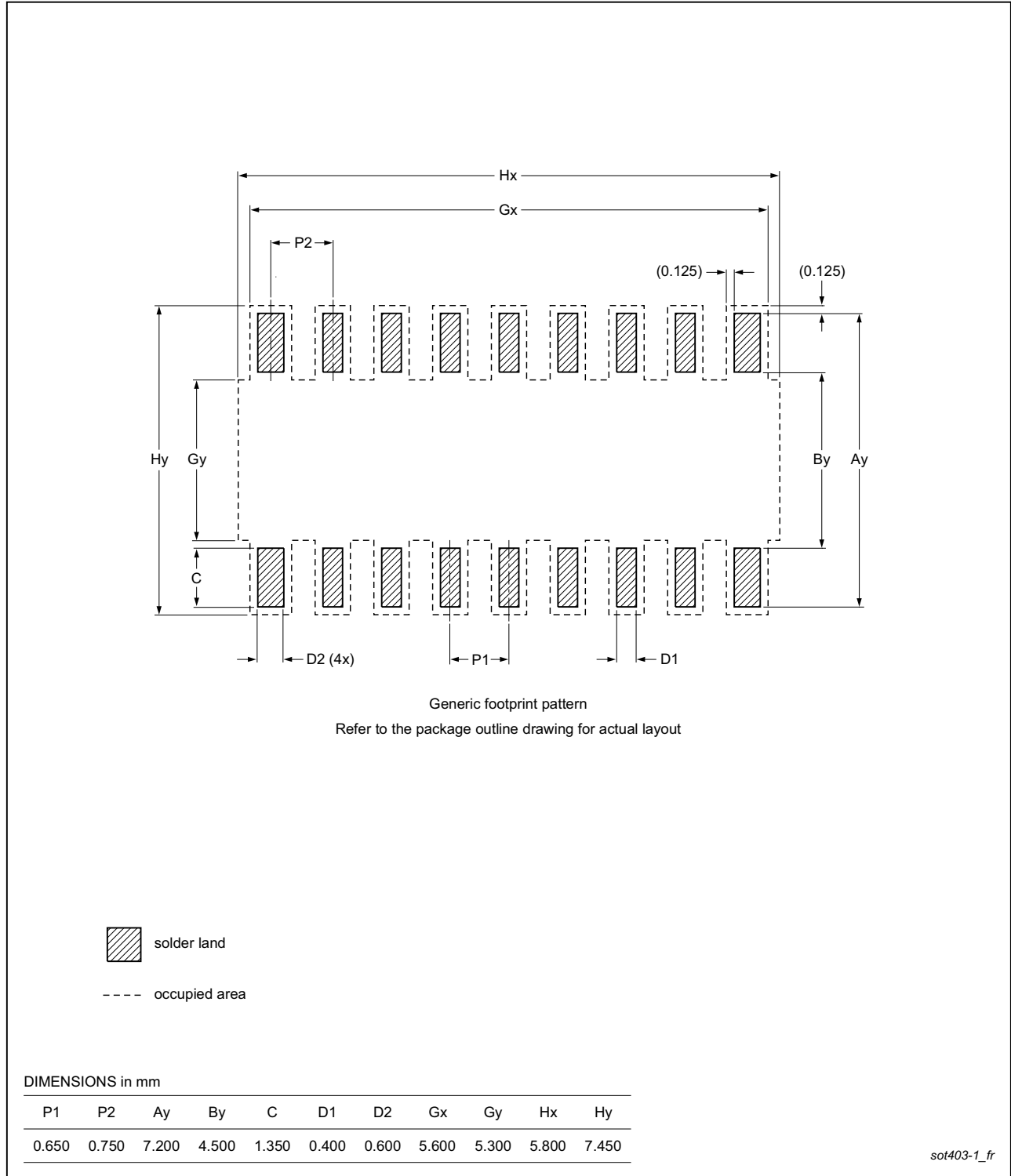


Fig 24. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

Footprint information for reflow soldering of HVQFN16 package

SOT629-1

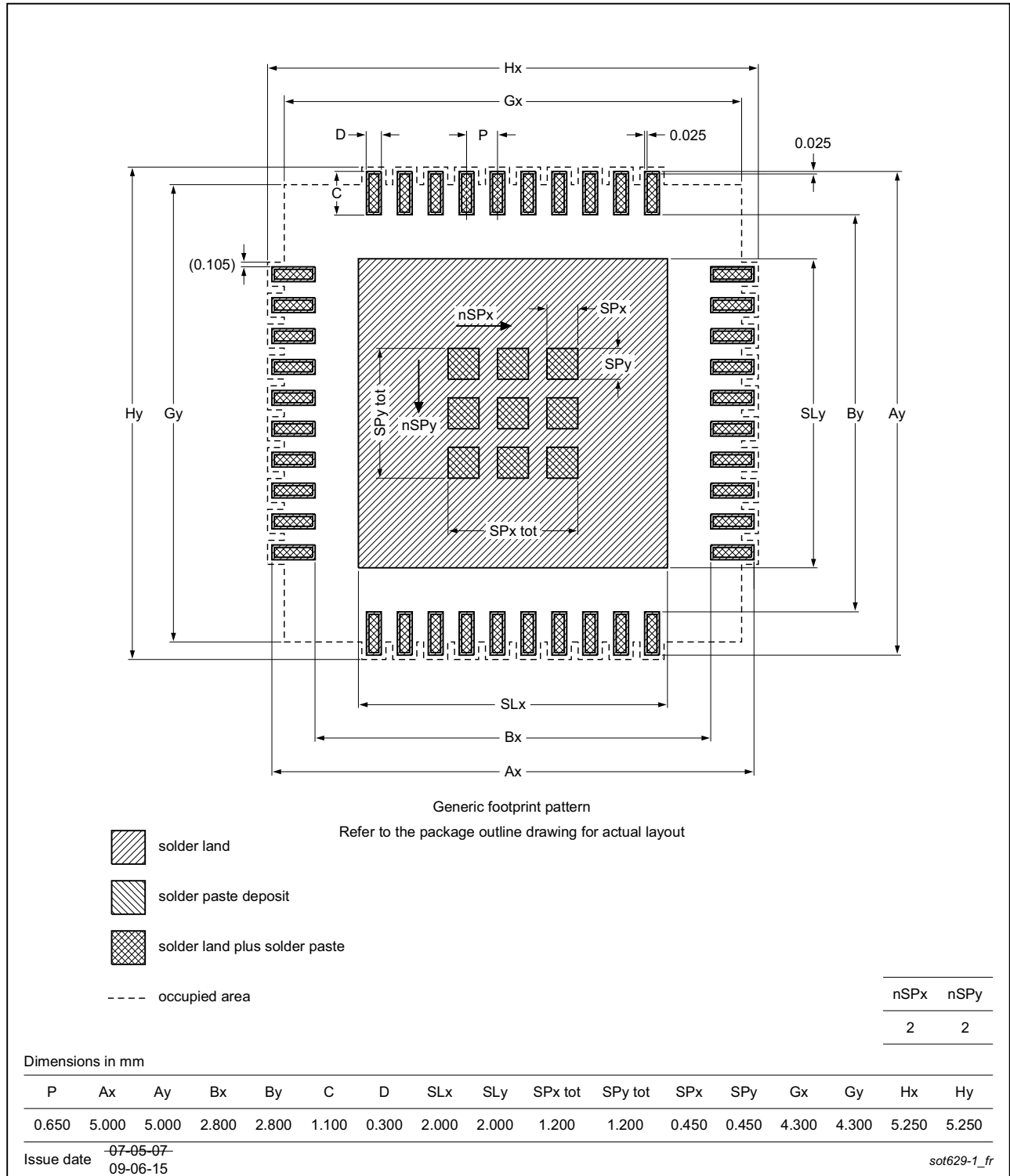


Fig 25. PCB footprint for SOT629-1 (HVQFN16); reflow soldering

## 14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CPU	Central Processing Unit
ESD	ElectroStatic Discharge
Fm+	Fast-mode Plus
HBM	Human Body Model
IC	Integrated Circuit
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
SMBus	System Management Bus

## 15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9846 v.1.1	20170404	Product data sheet	201703016I	PCA9846 v.1
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 6.7 “Voltage level translation between I<sup>2</sup>C-buses”</a>: Minor text edits to clarify operation of device.</li> <li>• <a href="#">Table 1 “Ordering information”</a>: Corrected topside marking for PCA9846PW; no change to device.</li> </ul>			
PCA9846 v.1	20151109	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP Semiconductors N.V.

## 17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 18. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
3.1	Ordering options . . . . .	2
<b>4</b>	<b>Block diagram</b> . . . . .	<b>3</b>
<b>5</b>	<b>Pinning information</b> . . . . .	<b>4</b>
5.1	Pinning . . . . .	4
5.2	Pin description . . . . .	4
<b>6</b>	<b>Functional description</b> . . . . .	<b>5</b>
6.1	Device address . . . . .	5
6.2	Software Reset General Call, and device ID addresses . . . . .	6
6.2.1	Software Reset . . . . .	7
6.2.2	Device ID (PCA9846 ID field) . . . . .	8
6.3	Control register . . . . .	9
6.3.1	Control register definition . . . . .	10
6.4	RESET input . . . . .	10
6.5	Power-on reset . . . . .	10
6.6	Power-on reset requirements . . . . .	11
6.7	Voltage level translation between I <sup>2</sup> C-buses . . . . .	13
<b>7</b>	<b>Characteristics of the I<sup>2</sup>C-bus</b> . . . . .	<b>15</b>
7.1	Write commands . . . . .	15
7.2	Read commands . . . . .	15
<b>8</b>	<b>Limiting values</b> . . . . .	<b>16</b>
<b>9</b>	<b>Static characteristics</b> . . . . .	<b>16</b>
<b>10</b>	<b>Dynamic characteristics</b> . . . . .	<b>19</b>
<b>11</b>	<b>Package outline</b> . . . . .	<b>22</b>
<b>12</b>	<b>Soldering of SMD packages</b> . . . . .	<b>24</b>
12.1	Introduction to soldering . . . . .	24
12.2	Wave and reflow soldering . . . . .	24
12.3	Wave soldering . . . . .	24
12.4	Reflow soldering . . . . .	25
<b>13</b>	<b>Soldering: PCB footprints</b> . . . . .	<b>27</b>
<b>14</b>	<b>Abbreviations</b> . . . . .	<b>29</b>
<b>15</b>	<b>Revision history</b> . . . . .	<b>29</b>
<b>16</b>	<b>Legal information</b> . . . . .	<b>30</b>
16.1	Data sheet status . . . . .	30
16.2	Definitions . . . . .	30
16.3	Disclaimers . . . . .	30
16.4	Trademarks . . . . .	31
<b>17</b>	<b>Contact information</b> . . . . .	<b>31</b>
<b>18</b>	<b>Contents</b> . . . . .	<b>32</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2017.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 4 April 2017

Document identifier: PCA9846



## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Switch ICs - Various category](#):*

*Click to view products by [NXP manufacturer](#):*

Other Similar products are found below :

[CPC7514Z](#) [BCM56440XB0IFSBG](#) [NL3S325FCT2G](#) [89H48T12G2ZCBLG](#) [ADG5462FBCPZ-RL7](#) [ADG5462FBRUZ](#) [LTC1043CN#PBF](#)  
[LTC1470ES8#PBF](#) [LTC1470CS8#PBF](#) [LTC1315CG#PBF](#) [74HC4053N](#) [74HC139N](#) [74HC138N](#) [XD74LS138](#) [XD74LS139](#) [XD74LS147](#)  
[XD4051](#) [XD4052](#) [XD4053](#) [XD14051](#) [XD14052](#) [XD14053](#) [XD74LS151](#) [XD74HC4514Z](#) [XD4514](#) [XD14514](#) [CPC7512Z](#) [CPC7592BCTR](#)  
[MAX4936ACTO+](#) [HT18LG-G](#) [PI4MSD5V9543ALEX](#) [MD0100DK6-G](#) [MIC2560-1YWM](#) [MIC2560-0YWM](#) [NJM2750M](#) [NJM2521M](#)  
[PCA9848PWJ](#) [FSA8009UMX](#) [FSA8028UMX](#) [FSA8039AUMSX](#) [FSA8049UCX](#) [FSA8108BUCX](#) [FSA850UCX](#) [BD3375KV-CE2](#) [74F138D](#)  
[74HC4051M/TR](#) [74HC138M/TR](#) [74HC4053M/TR](#) [74HC4052M/TR](#) [XL74LS138](#)