PCA9848

8-channel ultra-low voltage, Fm+ I²C-bus switch with reset

Rev. 1.1 — 2 November 2016 Product data sheet

1. General description

The PCA9848 is an ultra-low voltage, octal bidirectional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any or all SCx/SDx channels can be selected, determined by the programmable control register. This feature allows multiple devices with the same I²C-bus address to reside on the same bus. The switch device can also separate a heavily loaded I²C-bus into separate bus segments, eliminating the need for a bus buffer.

An active LOW reset input allows the PCA9848 to recover from a situation where one of the downstream I²C-buses is stuck in a LOW state. Pulling the $\overline{\text{RESET}}$ pin LOW resets the I²C-bus state machine and deselects all the channels, as does the internal Power-On Reset (POR) function.

The pass gates of the switches are constructed such that the V_{DD1} pin is used to limit the maximum high voltage which is passed by the PCA9848. This allows the use of different bus voltages on each channel, so that 0.8 V, 1.8 V, 2.5 V or 3.3 V parts can communicate without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 3.6 V tolerant.

2. Features and benefits

- Ultra-low voltage operation, down to 0.8 V to interface with next-generation CPUs
- 1-of-8 bidirectional translating switch
- Fm+ I²C-bus interface logic; compatible with SMBus standards
- Active LOW reset input
- 2 address pins allowing up to 16 devices on the I²C-bus
- Channel selection via I²C-bus
- Power-up with all switch channels deselected
- Low R_{on} switches
- Allows voltage level translation between 0.8 V, 1.8 V, 2.5 V and 3.3 V buses
- Reset via I²C-bus software command
- I²C Device ID function
- No glitch on power-up
- Supports hot insertion since all channels are de-selected at power-on
- Low standby current
- 3.6 V tolerant inputs
- 0 Hz to 1 MHz clock frequency
- ESD protection exceeds 6000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

- Two packages offered: TSSOP24 and HVQFN24

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9848BS[1]	PCA9848	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1
PCA9848PW	PCA9848	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

[1] Package is in development. Contact NXP for availability.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9848BS[1]	PCA9848BSJ	HVQFN24	Reel 13” Q1/T1 *Standard mark SMD	6000	T_{amb} = –40 °C to +85 °C
PCA9848PW	PCA9848PWJ	TSSOP24	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = –40 °C to +85 °C
PCA9848PW	PCA9848PWZ	TSSOP24	Reel 13” Q1/T1 *Standard mark SMD	500	T_{amb} = –40 °C to +85 °C

[1] Package is in development. Contact NXP for availability.

4. Block diagram

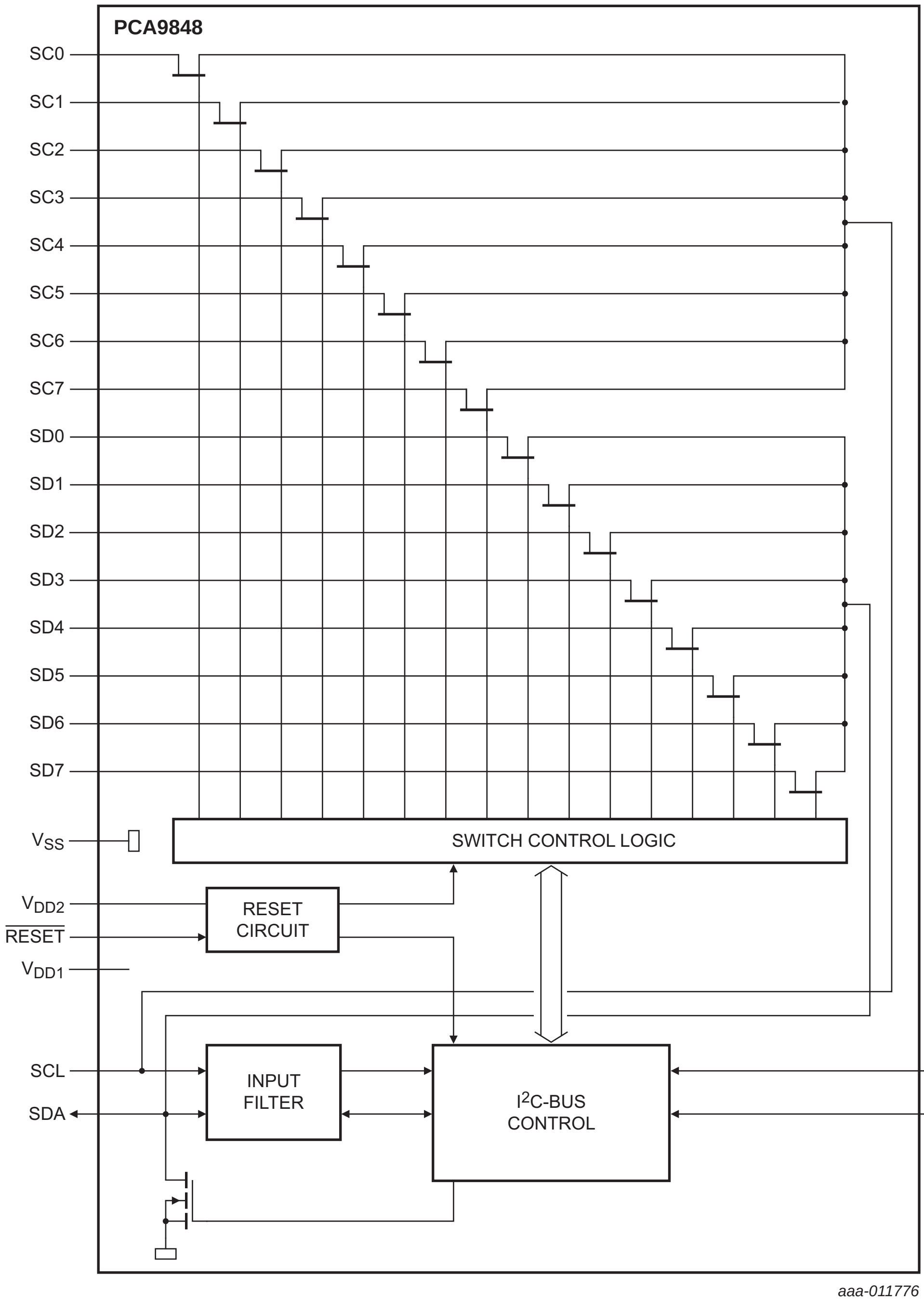


Fig 1. Block diagram of PCA9848

5. Pinning information

5.1 Pinning

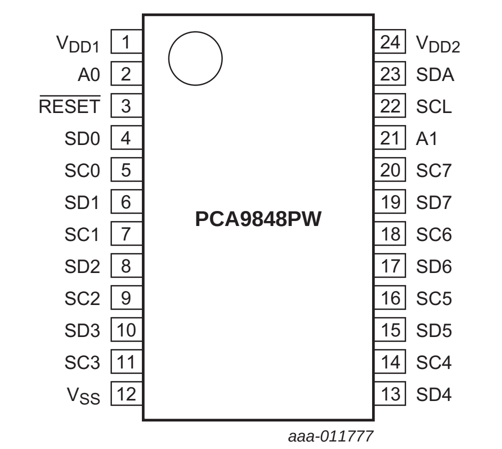


Fig 2. Pin configuration for TSSOP24

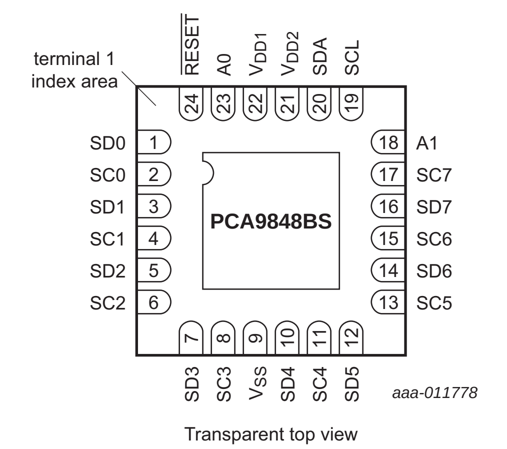


Fig 3. Pin configuration for HVQFN24

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP24	HVQFN24	
V_{DD1}	1	22	logic level power supply
A0	2	23	address input 0
$\overline{RESET}$	3	24	active LOW reset input
SD0	4	1	serial data 0
SC0	5	2	serial clock 0
SD1	6	3	serial data 1
SC1	7	4	serial clock 1
SD2	8	5	serial data 2
SC2	9	6	serial clock 2
SD3	10	7	serial data 3
SC3	11	8	serial clock 3
V_{SS}	12	9[1]	supply ground
SD4	13	10	serial data 4
SC4	14	11	serial clock 4
SD5	15	12	serial data 5
SC5	16	13	serial clock 5
SD6	17	14	serial data 6
SC6	18	15	serial clock 6
SD7	19	16	serial data 7
SC7	20	17	serial clock 7

Table 3. Pin description *...continued*

Symbol	Pin		Description
	TSSOP24	HVQFN24	
A1	21	18	address input 1
SCL	22	19	serial clock line
SDA	23	20	serial data line
V_{DD2}	24	21	core logic power supply

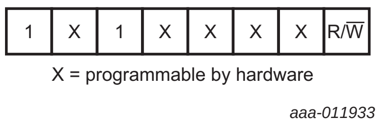
[1] HVQFN24 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

6. Functional description

Refer to Figure 1 "Block diagram of PCA9848".

6.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9848 is shown in Figure 4. the device pins A0 and A1 must be connected to a valid logic signal — HIGH, LOW, SCL or SDA — to ensure a valid slave address, since no internal pull-up resistors are provided.



See Table 4.

Fig 4. Slave address

Table 4. Address selection

PCA9848 address pins		8-bit I^{2}C-bus address	Slave address/bit pattern master must send							
A1	A0		A7	A6	A5	A4	A3	A2	A1	A0 - R/$\overline{\text{W}}$
0	SCL	0xE0h	1	1	1	0	0	0	0	0/1
0	0	0xE2h	1	1	1	0	0	0	1	0/1
0	SDA	0xE4h	1	1	1	0	0	1	0	0/1
0	1	0xE6h	1	1	1	0	0	1	1	0/1
1	SCL	0xE8h	1	1	1	0	1	0	0	0/1
1	0	0xEAh	1	1	1	0	1	0	1	0/1
1	SDA	0xECh	1	1	1	0	1	1	0	0/1
1	1	0xEEh	1	1	1	0	1	1	1	0/1
SCL	SCL	0xB0h	1	0	1	1	0	0	0	0/1
SCL	0	0xB2h	1	0	1	1	0	0	1	0/1
SCL	SDA	0xB4h	1	0	1	1	0	1	0	0/1
SCL	1	0xB6h	1	0	1	1	0	1	1	0/1
SDA	SCL	0xB8h	1	0	1	1	1	0	0	0/1
SDA	0	0xBAh	1	0	1	1	1	0	1	0/1
SDA	SDA	0xBCh	1	0	1	1	1	1	0	0/1
SDA	1	0xBEh	1	0	1	1	1	1	1	0/1

6.2 Software Reset General Call, and device ID addresses

Two other different addresses can be sent to the device.

- General Call address: allows to reset the device through the I^{2}C-bus upon reception of the right I^{2}C-bus sequence. See Section 6.2.1 "Software Reset" for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See Section 6.2.2 "Device ID (PCA9848 ID field)" for more information.

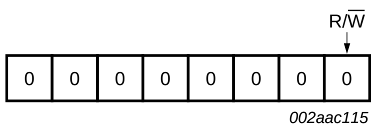


Fig 5. General Call address

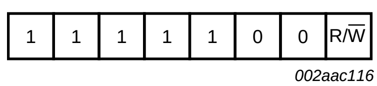


Fig 6. Device ID address

6.2.1 Software Reset

The Software Reset Call allows all the devices in the I2C-bus to be reset to the power-up state value through a specific formatted I2C-bus command. To be performed correctly, it implies that the I2C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I2C-bus master.
2. The reserved General Call I2C-bus address '0000 000' with the R/$\overline{W}$ bit set to 0 (write) is sent by the I2C-bus master.
3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I2C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
   a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

   If more than 1 byte of data is sent, the device does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I2C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 7.

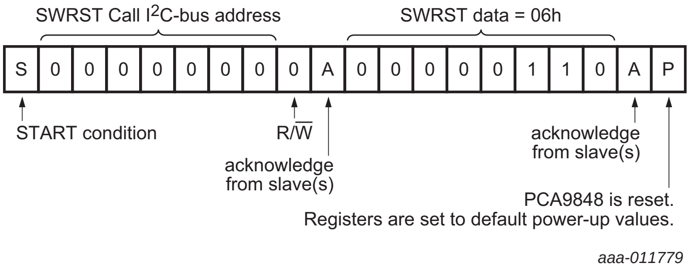


Fig 7. Software Reset sequence

6.2.2 Device ID (PCA9848 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I²C-bus address followed by the $R/\overline{W}$ bit set to 0 (write): ‘1111 1000’.
3. The master sends the I²C-bus slave address of the slave device it needs to identify. The LSB is a ‘Don’t care’ value. Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
4. The master sends a Re-START command.

   Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.
5. The master sends the Reserved Device ID I²C-bus address followed by the $R/\overline{W}$ bit set to 1 (read): ‘1111 1001’.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

   Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.

   If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

   For the PCA9848, the Device ID is shown in Figure 8.

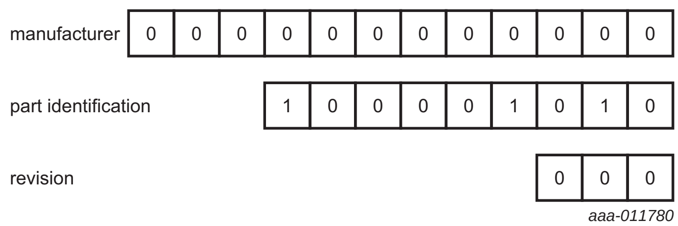
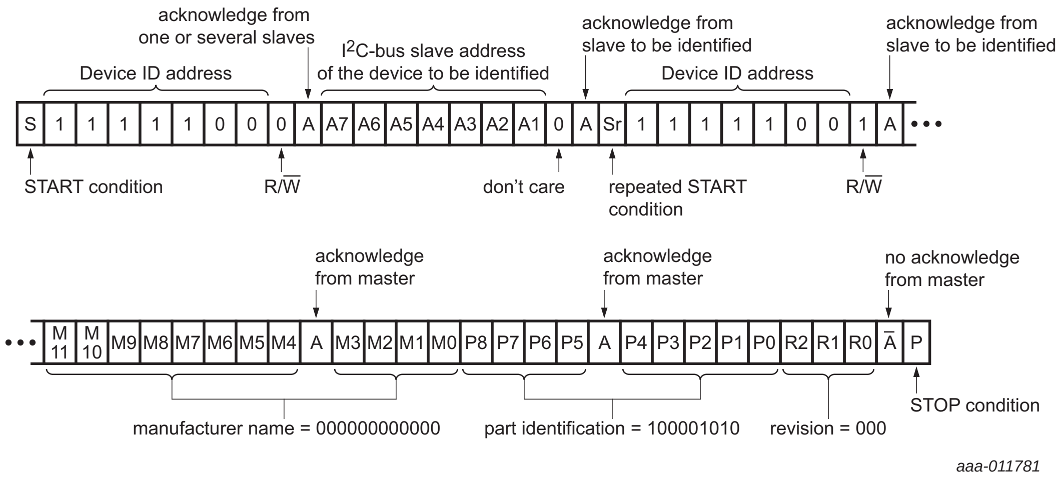


Fig 8. PCA9848 Device ID field



If more than 3 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

Fig 9. Device ID field read operation

6.3 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9848, which will be stored in the control register. If multiple bytes are received by the PCA9848, it will save the last byte received. This register can be written and read via the I²C-bus.

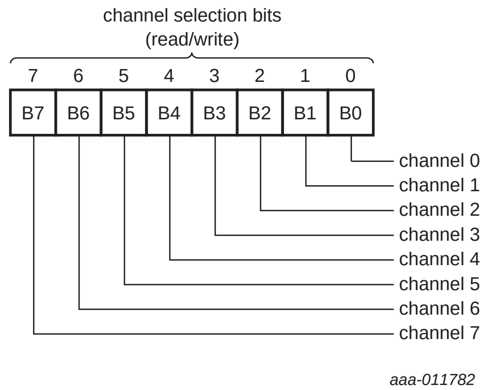


Fig 10. Control register

6.3.1 Control register definition

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9848 has been addressed. All 8 bits of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, it will become active after a STOP condition has been placed on the I^2C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection. Notice that multiple channels may simultaneously be selected.

Table 5. Control register

Write = channel selection; Read = channel status

B7	B6	B5	B4	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
						1		channel 1 enabled
X	X	X	X	X	0	X	X	channel 2 disabled
					1			channel 2 enabled
X	X	X	X	0	X	X	X	channel 3 disabled
				1				channel 3 enabled
X	X	X	0	X	X	X	X	channel 4 disabled
			1					channel 4 enabled
X	X	0	X	X	X	X	X	channel 5 disabled
		1						channel 5 enabled
X	0	X	X	X	X	X	X	channel 6 disabled
	1							channel 6 enabled
0	X	X	X	X	X	X	X	channel 7 disabled
1								channel 7 enabled

Remark: Multiple channels can be enabled at the same time. Example: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, means that channels 7, 5, 4, 1 and 0 are disabled and channels 6, 3, and 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. Default condition is all zeroes.

6.4 $\overline{\text{RESET}}$ input

The $\overline{\text{RESET}}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of $t_{w(rst)L}$, the PCA9848 will reset its registers and I^2C-bus state machine and will deselect all channels.

6.5 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9848 in a reset condition until V_{DD2} has reached V_{POR}. At this point, the reset condition is released and the PCA9848 registers and I^2C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected.

6.6 Power-on reset requirements

In the event of a glitch or data corruption, PCA9848 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

Power-on reset is shown in Figure 11.

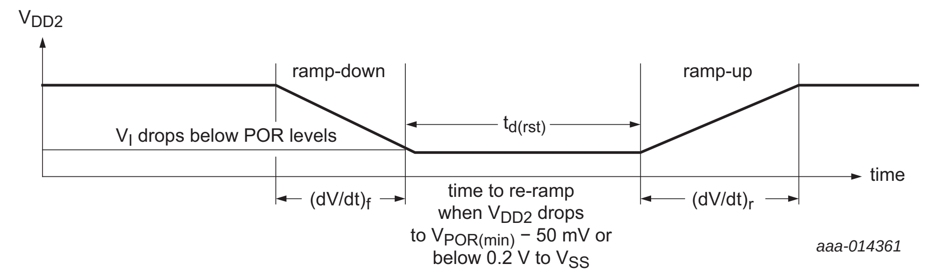


Fig 11. V_{DD2} is lowered below the POR threshold, then ramped back up to V_{DD2}

Table 6 specifies the performance of the power-on reset feature for PCA9848 for both types of power-on reset.

Table 6. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 11		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 11		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 11; re-ramp time when V_{DD2} drops to $V_{POR(min)}$ − 50 mV) or below 0.2 V to V_{SS}		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 12	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 12	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling V_{DD2}		0.7	-	-	V
		rising V_{DD2}		-	-	1.5	V

[1] Level that V_{DD2} can glitch down to with a ramp rate = 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD2}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 12 and Table 6 provide more information on how to measure these specifications.

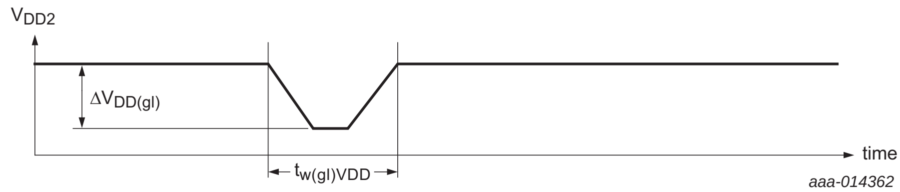


Fig 12. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD2} being lowered to or from 0 V. Figure 13 and Table 6 provide more details on this specification.

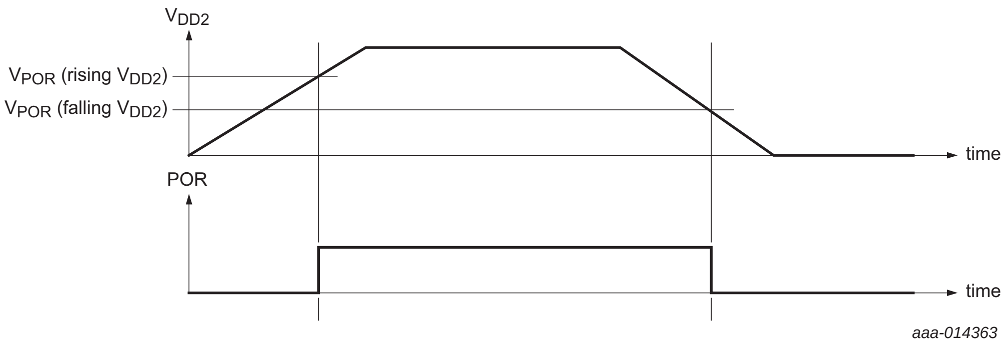


Fig 13. Power-on reset voltage (V_{POR})

6.7 Voltage level translation between I²C-buses

Today's complex systems often use multiple power supplies to maximize power savings and to meet the operating specifications of the devices used. This means that various I²C-buses are also operating at differing voltage levels and cannot simply connect together. In addition, modern microcontrollers operate down to 0.8 V to save power, further complicating the connection of I²C-buses.

The PCA9848 is specifically designed to seamlessly handle these voltage level translation issues. Any combination of bus voltages can be intermixed on the PCA9848 and correctly translated to the other bus at Fm+ (1 MHz) speed.

Figure 14 shows a typical application. The microcontroller acts as the master and operates at 0.8 V with its I²C-bus swinging between 0 V and 0.8 V. The temperature sensor on channel 0 of the PCA9848 has a operates at 3.3 V, while the GPIO Expander on channel 1 operates down to 1.8 V to interface with chip select and reset inputs on various other ICs also operating at 1.8 V. Channel 2 of the PCA9848 is connected to the I²C-bus of a power management device, operating at 2.5 V. The other channels of PCA9848 are simply left unconnected.

In this example, V_{DD1} of the PCA9848 is a bias supply and is set at the lowest bus voltage, or 0.8 V of the microcontroller. V_{DD1} sets the input switching points of each SCL and SDA at $0.3 \times V_{DD1}$ for a LOW level and $0.7 \times V_{DD1}$ for a HIGH level.

V_{DD2} is the core logic supply from which most of the PCA9848 circuitry runs and must be larger than 1.65 V.

The I²C-bus is open-drain, so pull-up resistors are needed on each I²C-bus segment. This is where the voltage level translation happens. The pass transistor internal to the PCA9848 limit the output voltage to the lower of V_{DD1} or V_{DD2}. The pull-up resistors will then limit the HIGH level of each bus segment to the power supply of the devices on that segment. Note that the pull-up resistors on channel 0 are connected to 3.3 V, and the resistors on channel 1 are connected to 1.8 V, while the resistors on channel 2 are connected to 2.5 V — effectively translating the 0.8 V signal swing of the microcontroller to the correct voltage level for each peripheral.

It is possible to level shift from a higher voltage microcontroller connected to V_{DD1} to lower voltage peripherals on the downstream side — the opposite of this particular example, as long as $V_{DD1} > 0.8$ V and $V_{DD2} > 1.65$ V.

One thing to note is noise margin on each I²C-bus segment is somewhat reduced due to the input levels set by V_{DD1}. Especially in this example, the I²C-bus LOW level is $0.3 \times V_{DD1}$ or 0.24 V, so extreme care must be taken to ensure all bus segments meet this specification. It also means that static offset buffers may not work correctly if the offset side is connected to the PCA9848.

Another point to examine is that there is no buffering capability between the upstream and the downstream buses. This is simply a pass transistor, which acts like a switch and a series resistor, between these bus segments. The series resistance is the R_{on} of the pass transistor and is inversely proportional to the minimum of $V_{DD1} + V_{TH}$ or V_{DD2}, where V_{TH} is approximately 0.8 V. Refer to Table 8 for some representative R_{on} values. An upcoming application note will explain R_{on} more thoroughly. Therefore, a careful analysis of bus capacitance and pull-up resistor values is called for.

A further point to consider is pull-up resistor selection. Since multiple channels can be simultaneously selected, the pull-up resistors on each channel are connected in parallel. Ensure each device can correctly drive the effective pull-up resistor value and still meet the LOW-level specifications.

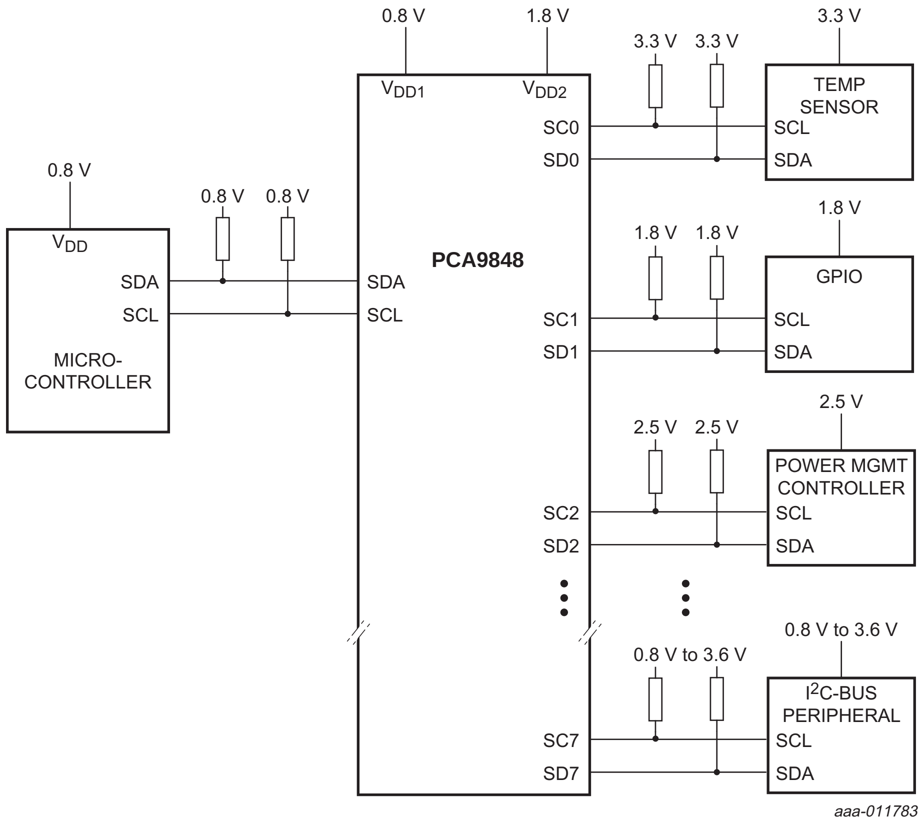


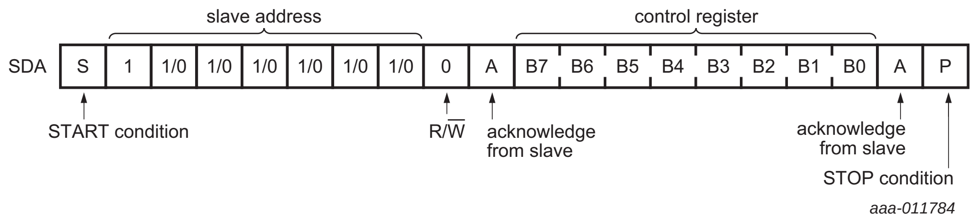
Fig 14. Typical application for PCA9848 with differing bus voltages

7. Characteristics of the I²C-bus

The PCA9848 is an I²C slave device. Data is exchanged between the master and the PCA9848 through write and read commands conforming to the I²C-bus protocol. The two communication lines are SCL (serial clock) and SDA (serial data), both of which must be connected to V_{DD1} through pull-up resistors.

7.1 Write commands

Data is transmitted to the PCA9848 by sending its device address and setting the Least Significant Bit (LSB) to a logic 0 (see Table 4 for device addresses), which the PCA9848 acknowledges (ACK). The control register byte is sent after the address that determines which downstream channel is connected to the upstream channel by bit 0 through bit 2. Bit 7 through bit 3 are ignored and can be written with any data. There is no limit on the number of bytes sent after the address and before a STOP condition, only the last byte written before the STOP condition is recognized and the selected channel is enabled only at the following STOP condition.



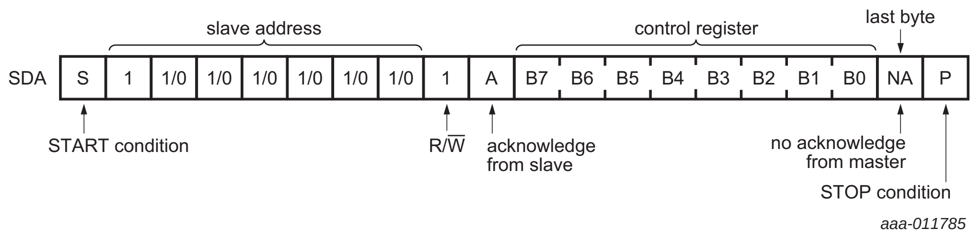
Refer to Table 4.

Fig 15. Write control register

7.2 Read commands

Data is read from the PCA9848 by sending its device address and setting the Least Significant Bit (LSB) to a logic 1 (see Table 4 for device addresses), which the PCA9848 acknowledges. The control register byte is read by the master with each byte either ACK or NACK by the master. If the master ACKs the control register byte, it continues to send register data until the master NACKs, signaling the transaction is complete. There is no limit on the number of bytes read from the PCA9848.

The control register bit definitions are shown in Figure 10. Bit 0 through bit 2 will show the enabled channels (as determined by the last write).



Refer to Table 4.

Fig 16. Read control register

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to V_{SS} (ground = 0 V)[1].

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+4.0	V
V_I	input voltage		–0.5	+4.0	V
I_I	input current		-	±20	mA
I_O	output current		-	±25	mA
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±100	mA
P_{tot}	total power dissipation		-	400	mW
T_{stg}	storage temperature		–60	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

9. Static characteristics

Table 8. Static characteristics

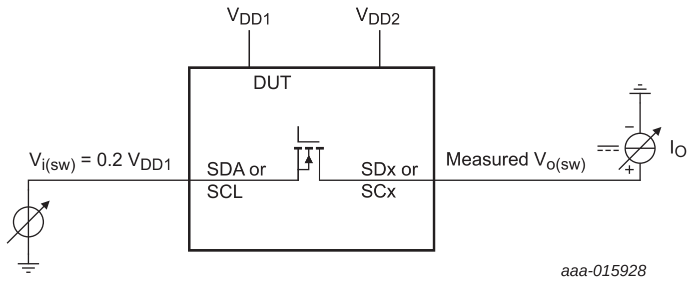
V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD1}	supply voltage 1		0.8	-	3.6	V
V_{DD2}	supply voltage 2		1.65	-	3.6	V
$I_{DD(VDD2)}$	supply current on pin V_{DD2}	V_{DD1} = 3.6 V, V_{DD2} = 3.6 V; SC0 to SC7 and SD0 to SD7 not connected; $\overline{RESET}$ = V_{DD1}; A0 = A1 = SCL; continuous register read/write				
		f_{SCL} = 0 kHz	-	5	12	µA
		f_{SCL} = 100 kHz	-	8	20	µA
		f_{SCL} = 1000 kHz	-	65	150	µA
$I_{DD(VDD1)}$	supply current on pin V_{DD1}	V_{DD1} = 3.6 V, V_{DD2} = 3.6 V; SC0 to SC7 and SD0 to SD7 not connected; $\overline{RESET}$ = V_{DD1}; A0 = A1 = SCL; continuous register read/write				
		f_{SCL} = 0 kHz	–5	–2	+2	µA
		f_{SCL} = 100 kHz	-	5	15	µA
		f_{SCL} = 1000 kHz	-	45	100	µA
V_{POR}	power-on reset voltage		-	1.2	1.5	V

Table 8. Static characteristics *...continued*

V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage	$V_{DD1} \leq 1.1$ V	–0.5	-	$+0.2V_{DD1}$	V
		$V_{DD1} > 1.1$ V	–0.5	-	$+0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage	$V_{DD1} = \leq 1.1$ V	$0.8V_{DD1}$	-	3.6	V
		$V_{DD1} > 1.1$ V	$0.7V_{DD1}$	-	3.6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; $V_{DD2} \leq 2$ V	15	-	-	mA
		V_{OL} = 0.4 V; $V_{DD2} > 2$ V	20	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$; all channels disabled	-	20	40	pF
Select inputs A0 to A1, $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage	$V_{DD1} \leq 1.1$ V	–0.5	-	$+0.2V_{DD1}$	V
		$V_{DD1} > 1.1$ V	–0.5	-	$+0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage	$V_{DD1} \leq 1.1$ V	$0.8V_{DD1}$	-	3.6	
		$V_{DD1} > 1.1$ V	$0.7V_{DD1}$	-	3.6	V
I_{LI}	input leakage current	pin at V_{DD2} to 3.6 V or V_{SS}	–1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$ or V_{DD1}	-	5	10	pF
Pass gate						
R_{on}	ON-state resistance	ON resistance of the pass transistor between SCL and SCx, and SDA and SDx				
		V_{DD1} = 0.8 V; $V_{DD2} \geq 1.65$ V; $V_{i(sw)}$ = 0.16 V; I_O = 3 mA	-	15	24	Ω
		V_{DD1} = 1.2 V; $V_{DD2} \geq 1.8$ V; $V_{i(sw)}$ = 0.24 V; I_O = 6 mA	-	12	18	Ω
		$V_{DD1} > 2$ V; $V_{DD2} \geq 2.5$ V; $V_{i(sw)}$ = 0.4 V; I_O = 20 mA	-	7	10	Ω
$I_{o(sw)}$	switch output current	V_{DD2} = 1.65 V to 3.6 V; $V_{i(sw)} = V_{DD1}$ to 3.6 V; $V_{o(sw)} = V_{DD1}$ to 3.6 V	0	-	100	μA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	-	+1	μA
C_{io}	input/output capacitance	$V_I = V_{SS}$; all switches disabled	-	8	15	pF



$R_{on} = (V_{o(sw)} - (V_{i(sw)}) / I_o$; $V_{i(sw)}$ and I_o are defined in Table 8

Fig 17. R_{on} test circuit

Table 9. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I^2C-bus		Fast-mode I^2C-bus		Fast
			Min	Max	Min	Max	Mi
t_{PD}	propagation delay	from SDA to SDx, or SCL to SCx	-	1[1]	-	1[1]	-
f_{SCL}	SCL clock frequency		0	100	0	400	0
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5
$t_{HD;STA}$	hold time (repeated) START condition	[2]	4.0	-	0.6	-	0.2
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.2
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.2
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.2
$t_{HD;DAT}$	data hold time		0[3]	3.45	0[3]	0.9	0
$t_{SU;DAT}$	data set-up time		250	-	100	-	50
t_r	rise time of both SDA and SCL signals		-	1000	20 × (V_{DD} / 5.5 V)[4]	300	-
t_f	fall time of both SDA and SCL signals		-	300	20 × (V_{DD} / 5.5 V)[4]	300	20 × (V_{DD} / 5.
C_b	capacitive load for each bus line		-	400	-	400	-
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	0
$t_{VD;DAT}$	data valid time	[7]	-	3.45	-	0.9	-
$t_{VD;ACK}$	data valid acknowledge time		-	1	-	1	-
RESET							
$t_{w(rst)L}$	LOW-level reset time		100	-	100	-	10
t_{rst}	reset time	SDA clear	500	-	500	-	50
$t_{REC;STA}$	recovery time to START condition		0	-	0	-	0

[1] Pass gate propagation delay is calculated from the 20 Ω typical R_{on} and the 50 pF load capacitance.

[2] After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] Necessary to be backwards compatible to Fast-mode.

[5] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[6] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

[7] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

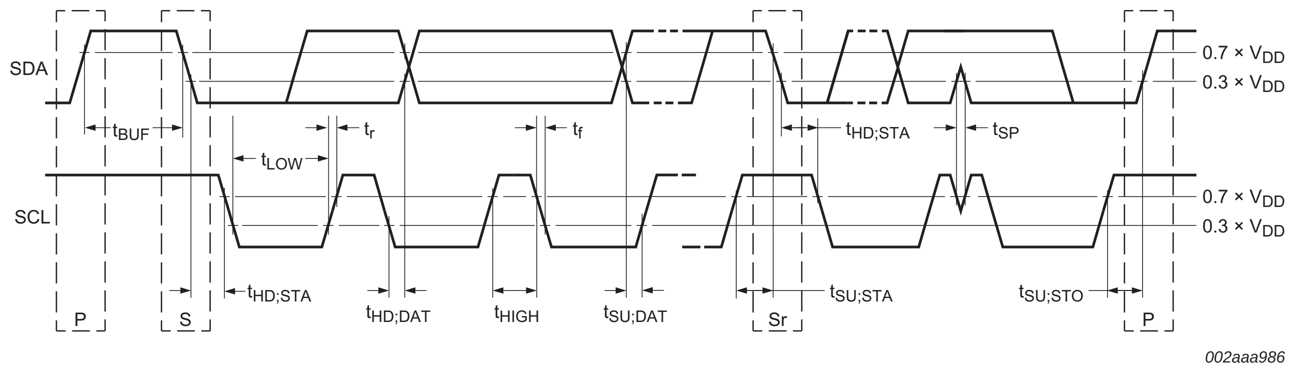


Fig 18. Definition of timing on the I²C-bus

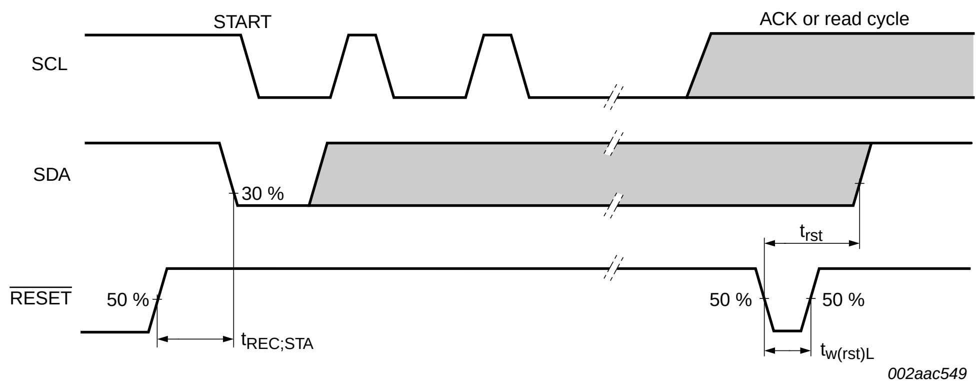
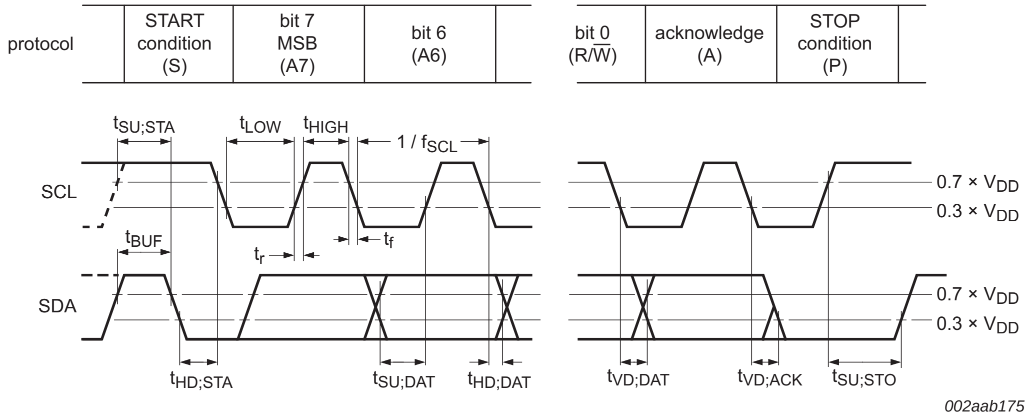


Fig 19. Definition of RESET timing

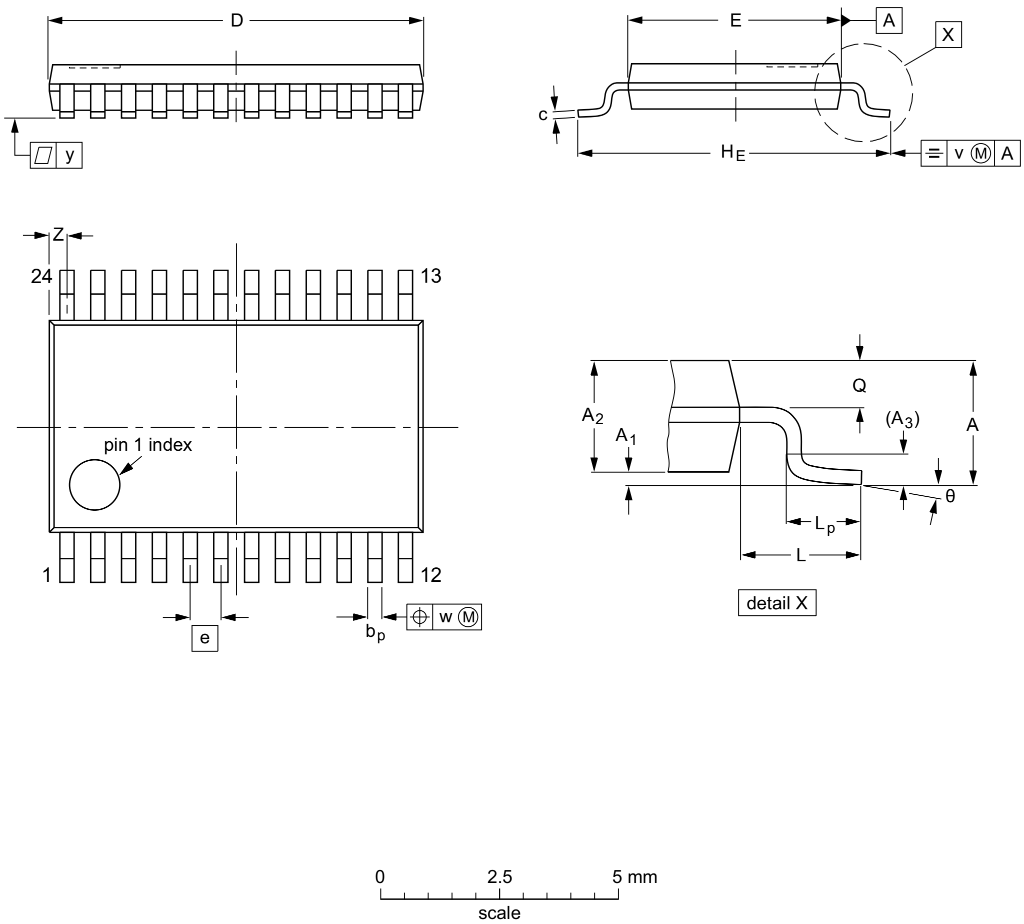


Rise and fall times refer to V_{IL} and V_{IH}.

Fig 20. I²C-bus timing diagram

11. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

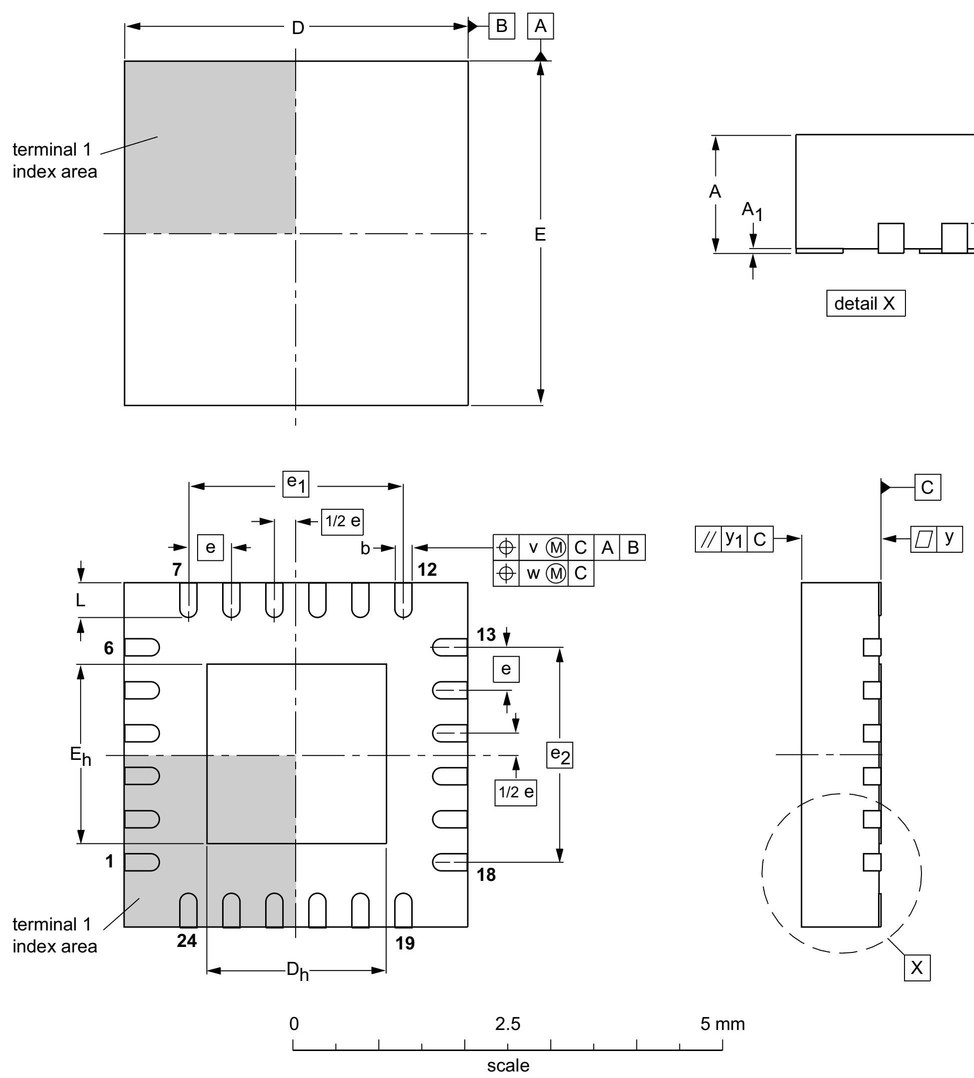
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 21. Package outline SOT355-1 (TSSOP24)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 22. Package outline SOT616-1 (HVQFN24)

12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020D)

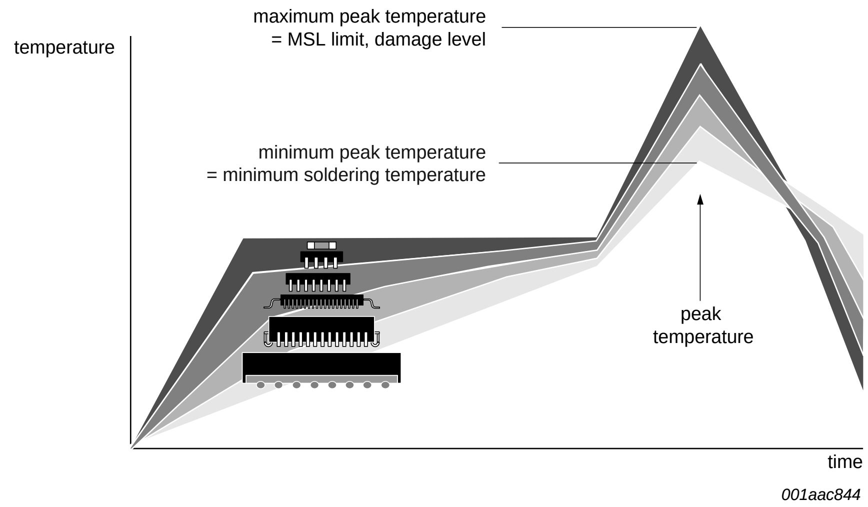
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.



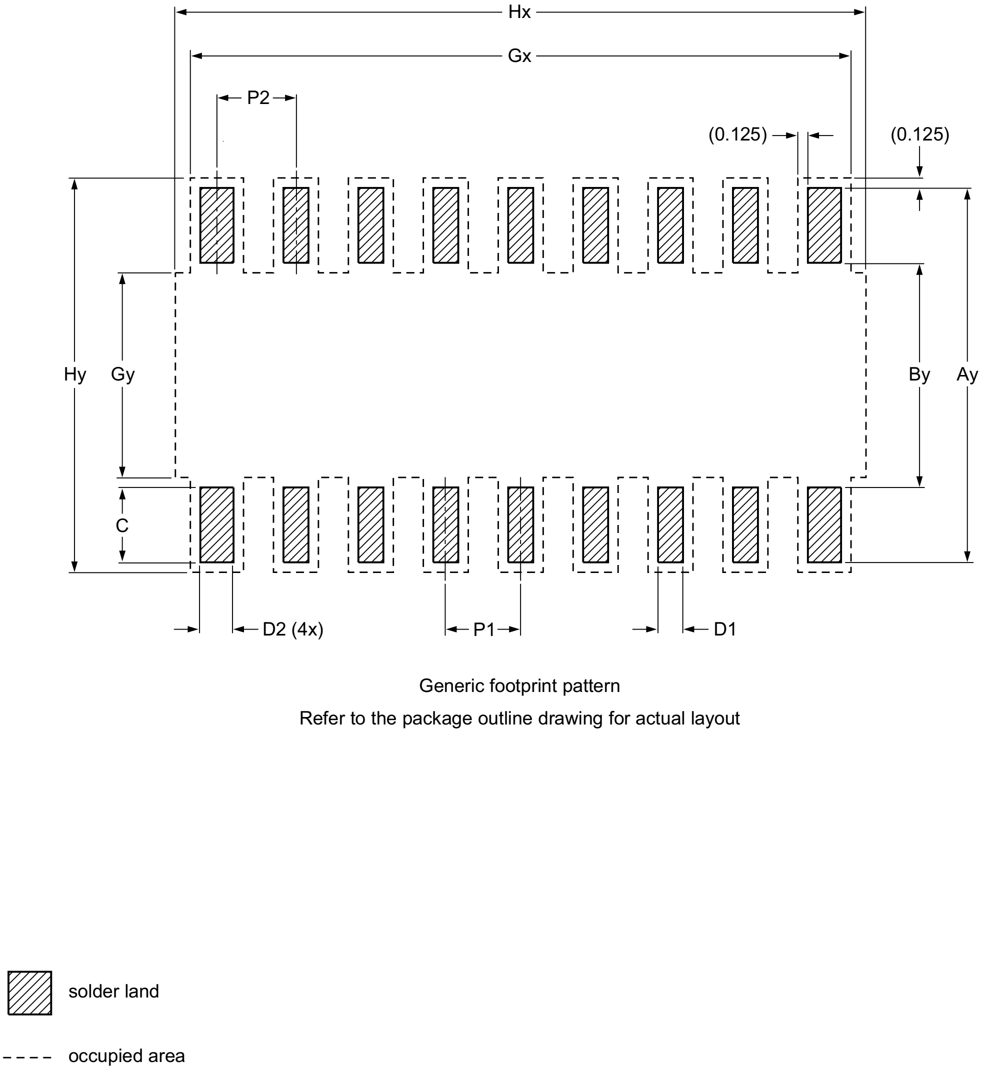
MSL: Moisture Sensitivity Level

Fig 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

13. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP24 package — SOT355-1



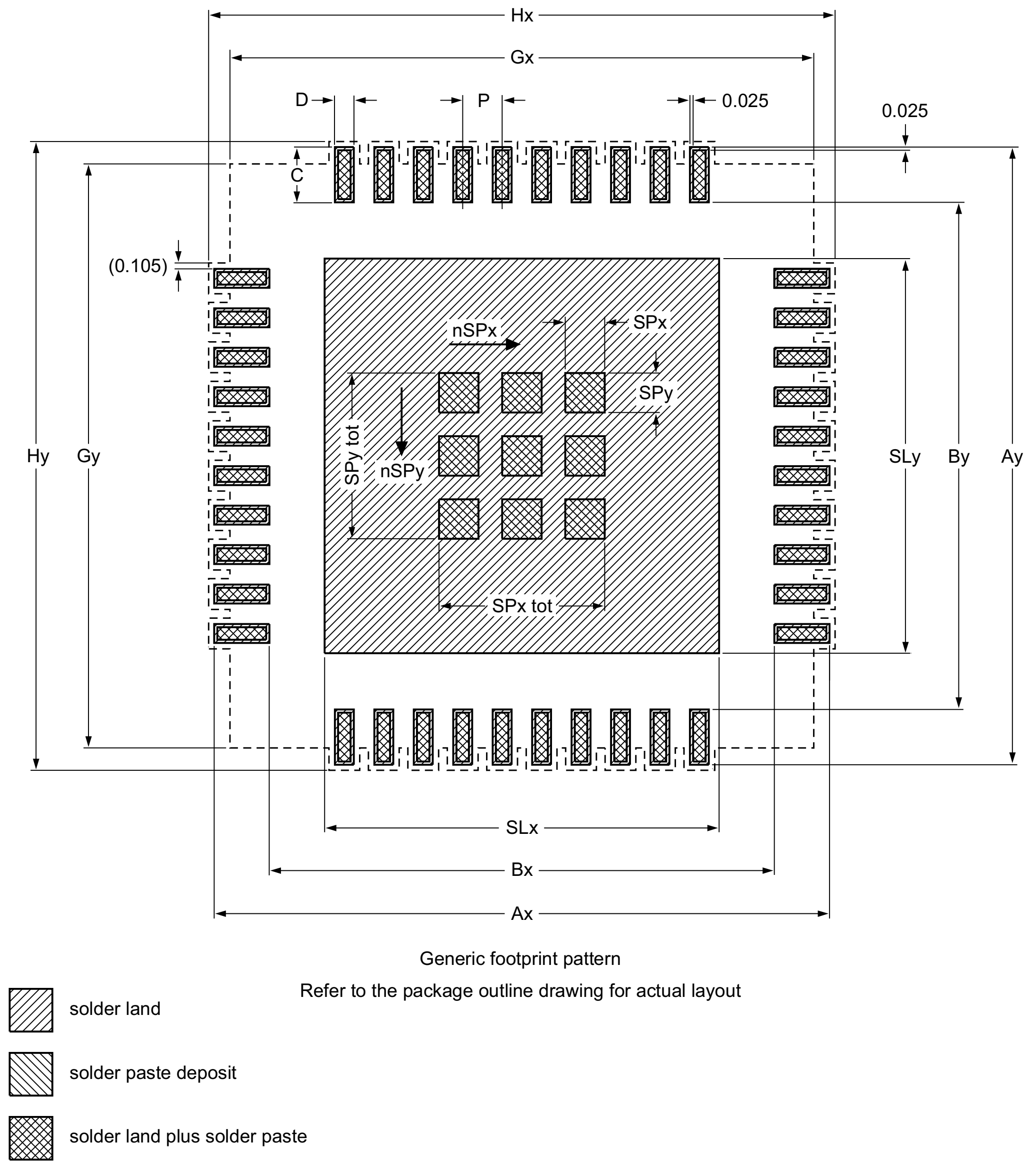
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	8.200	5.300	8.600	7.450

sot355-1_fr

Fig 24. PCB footprint for SOT355-1 (TSSOP24); reflow soldering

Footprint information for reflow soldering of HVQFN24 package **SOT616-1**



nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	5.000	5.000	3.200	3.200	0.900	0.240	2.100	2.100	1.200	1.200	0.450	0.450	4.300	4.300	5.250	5.250

Issue date ~~07-05-07~~ 09-06-15 *sot616-1_fr*

Fig 25. PCB footprint for SOT616-1 (HVQFN24); reflow soldering

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CPU	Central Processing Unit
ESD	ElectroStatic Discharge
Fm+	Fast-mode Plus
HBM	Human Body Model
IC	Integrated Circuit
I²C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
SMBus	System Management Bus

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9848 v.1.1	20161102	Product data sheet	-	PCA9848 v.1
Modifications:	• Section 6.7 "Voltage level translation between I²C-buses": Minor text edits to clarify operation of device • Table 1 "Ordering information": Corrected topside marking for PCA9848PW; no change to device			
PCA9848 v.1	20141215	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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18. Contents

Date of release: 2 November 2016
Document identifier: PCA9848