PCF2116 family

LCD controller / drivers

Rev. 05.01 — 20 July 2007 **Product data sheet**

1. General description

The PCF2116 is a low-power CMOS LCD controller and driver, designed to drive a split screen dot matrix LCD display of 1 or 2 lines by 24 characters or 2 or 4 lines by 12 characters with 5×8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system power consumption. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The PCF2116 interfaces to most microcontrollers using a 4 or 8-bit bus or via the 2-wire I^2C-bus. To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connection to V_{DD}.

The 'x' in 'PCF2116x' represents a specific letter code for a character set in the character generator ROM (CGROM). The different character sets currently available are specified by the letters A, C, and G (see Figure 5, Figure 6 and Figure 7). Other character sets are available on request.

Remark: The notation for hexadecimal numbers used in this datasheet is consistent with NXP house style and uses a suffix 'h' following the number e.g. 00h.

2. Features

- Single chip LCD controller/driver
- 1 or 2-line display of up to 24 characters per line, or 2 or 4 lines of up to 12 characters per line
- 5×7 character format plus cursor; 5×8 for kana (Japanese syllabary) and user defined symbols
- On chip:
  - generation of LCD supply voltage (external supply also possible)
  - generation of intermediate LCD bias voltages
  - oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 characters
- Character generator RAM: 16 characters
- 4 or 8-bit parallel bus or 2-wire I^2C-bus interface
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1:32 and 1:16
- Uses common 11 code instruction set
- Logic supply voltage range, $V_{DD} - V_{SS}$: 2.5 to 6 V
- Display supply voltage range, $V_{DD} - V_{LCD}$: 3.5 to 9 V

- Low power consumption
- I^2C-bus address: 011101 SA0.

3. Applications

- Telecom equipment.
- Portable instruments.
- Point-of-sale terminals.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2116xU	-	chip in tray	-
PCF2116xU/2	-	chip with gold bumps in tray	-
PCF2116xU/10	-	wafer sawn and delivered on film frame carrier (FFC)	-
PCF2116xU/12	-	wafer sawn with gold bumps and delivered on film frame carrier (FFC)	-

[1] The letter ‘x’ in the type number represents the letter of the required built-in character set: A, C or G.

5. Block diagram

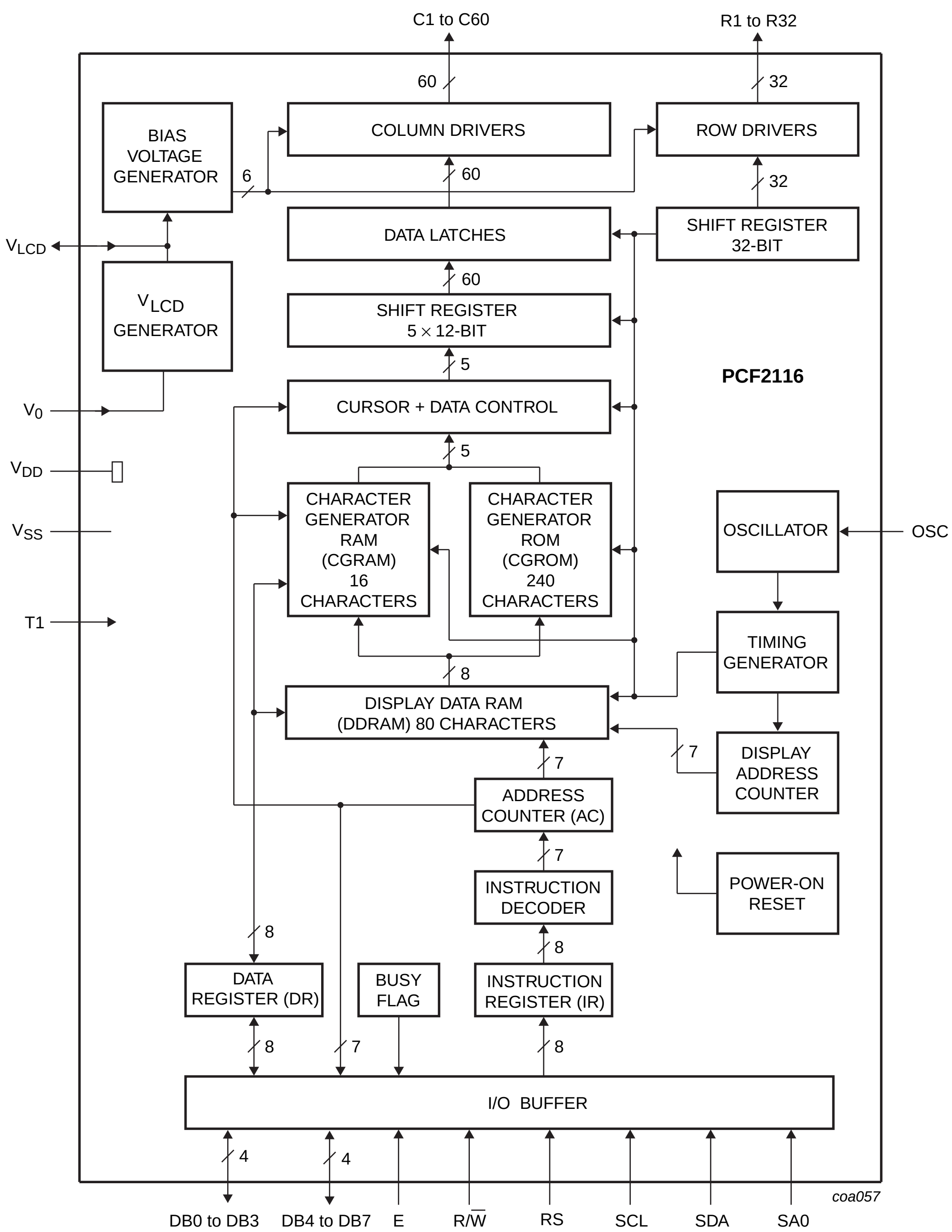
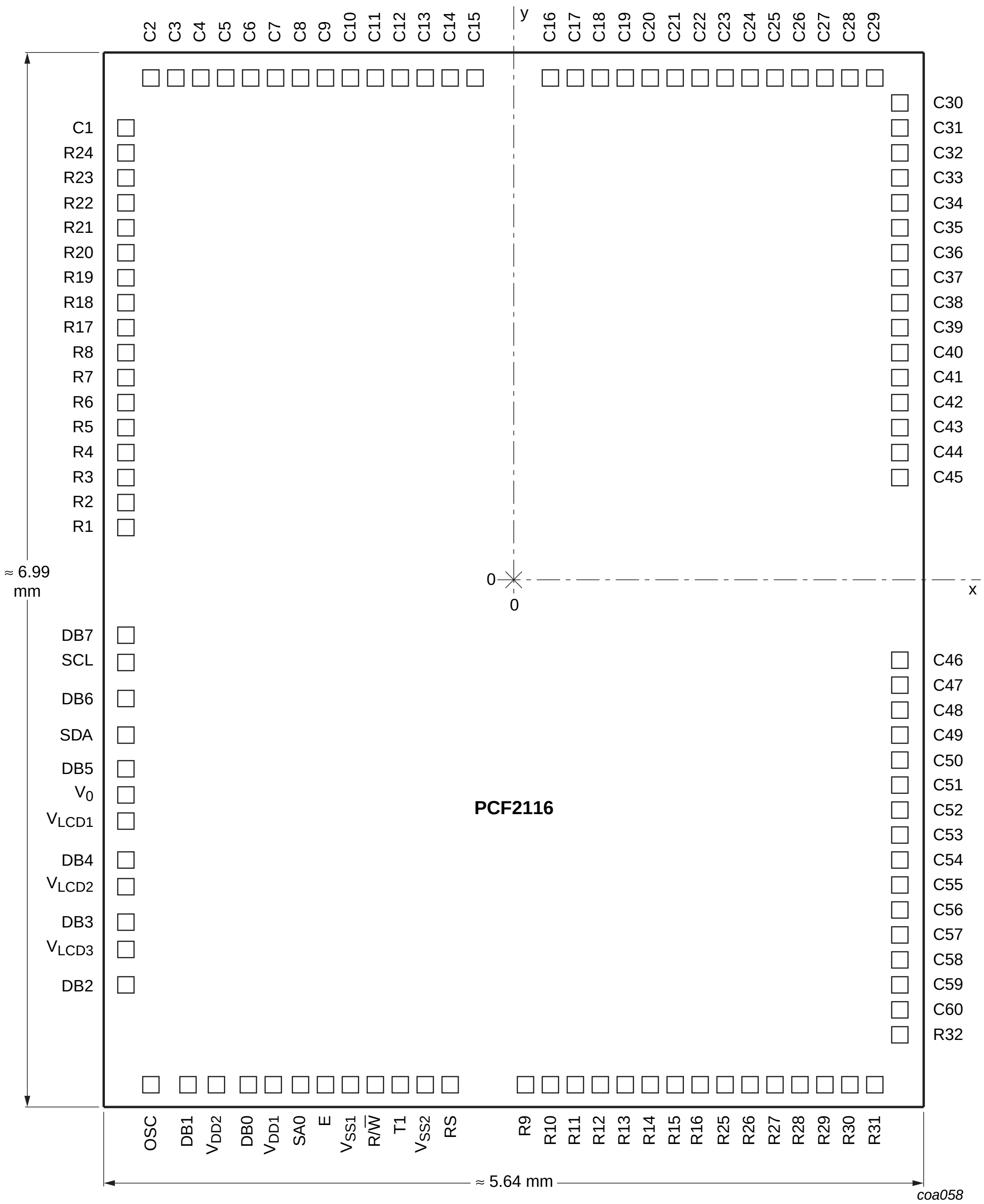


Fig 1. Block diagram of the pcf2116 family

6. Pinning information

6.1 Pinning



(1) Pad area 0.0121 mm^2

(2) Bonding pad dimensions: 110 × 110 µA

Fig 2. Bonding pad location for PCF2116x

Table 2. Pad allocation table

Symbol	Pad	Symbol	Pad
OSC	1	C29 to C1	60 to 88
DB1	2	R24 to R17	89 to 96
V_{DD2}	3	R8 to R1	97 to 104
DB0	4	DB7	105
V_{DD1}	5	SCL	106
SA0	6	DB6	107
E	7	SDA	108
V_{SS1}	8	DB5	109
R/$\overline{W}$	9	V_0	110
T1	10	V_{LCD1}	111
V_{SS2}	11	DB4	112
RS	12	V_{LCD2}	113
R9 to R16	13 to 20	DB3	114
R25 to R32	21 to 28	V_{LCD3}	115
C60 to C30	29 to 59	DB2	116

6.2 Pin description

Table 3. Bonding pad description

All x/y coordinates represent the position of the centre of each pad with respect to the centre (x/y = 0) of the chip (see Figure 2).

Symbol	Pad	X (μm)	Y (μm)	Description
OSC	1	–2445	–3300	oscillator/external clock input
DB1	2	–2211	–3300	1 bit of 8 bit bi-directional data bus
V_{DD2}	3	–2034	–3300	supply voltage 2
DB0	4	–1806	–3300	1 bit of 8 bit bi-directional data bus
V_{DD1}	5	–1627	–3300	supply voltage 1
SA0	6	–1437	–3300	I^2C-bus address pin
E	7	–1245	–3300	data bus clock input (parallel control)
V_{SS1}	8	–1056	–3300	logic ground 1
R/W	9	–867	–3300	read/write input (parallel control)
T1	10	–672	–3300	test pad (connect to V_{SS})
V_{SS2}	11	–486	–3300	logic ground 2
RS	12	–297	–3300	register select input (parallel control)
R9	13	77	–3300	LCD row driver output 9
R10	14	247	–3300	LCD row driver output 10
R11	15	417	–3300	LCD row driver output 11
R12	16	587	–3300	LCD row driver output 12
R13	17	757	–3300	LCD row driver output 13
R14	18	927	–3300	LCD row driver output 14
R15	19	1097	–3300	LCD row driver output 15
R16	20	1267	–3300	LCD row driver output 16

Table 3. Bonding pad description *...continued*

All x/y coordinates represent the position of the centre of each pad with respect to the centre (x/y = 0) of the chip (see Figure 2).

Symbol	Pad	X (µm)	Y (µm)	Description
R25	21	1436	–3300	LCD row driver output 25
R26	22	1606	–3300	LCD row driver output 26
R27	23	1776	–3300	LCD row driver output 27
R28	24	1976	–3300	LCD row driver output 28
R29	25	2116	–3300	LCD row driver output 29
R30	26	2286	–3300	LCD row driver output 30
R31	27	2456	–3300	LCD row driver output 31
R32	28	2626	–3013	LCD row driver output 32
C60	29	2626	–2760	LCD column driver output 60
C59	30	2626	–2590	LCD column driver output 59
C58	31	2626	–2420	LCD column driver output 58
C57	32	2626	–2250	LCD column driver output 57
C56	33	2626	–2080	LCD column driver output 56
C55	34	2626	–1910	LCD column driver output 55
C54	35	2626	–1740	LCD column driver output 54
C53	36	2626	–1570	LCD column driver output 53
C52	37	2626	–1400	LCD column driver output 52
C51	38	2626	–1230	LCD column driver output 51
C50	39	2626	–1060	LCD column driver output 50
C49	40	2626	–890	LCD column driver output 49
C48	41	2626	–720	LCD column driver output 48
C47	42	2626	–550	LCD column driver output 47
C46	43	2626	–380	LCD column driver output 46
C45	44	2626	582	LCD column driver output 45
C44	45	2626	752	LCD column driver output 44
C43	46	2626	922	LCD column driver output 43
C42	47	2626	1092	LCD column driver output 42
C41	48	2626	1262	LCD column driver output 41
C40	49	2626	1432	LCD column driver output 40
C39	50	2626	1602	LCD column driver output 39
C38	51	2626	1772	LCD column driver output 38
C37	52	2626	1942	LCD column driver output 37
C36	53	2626	2112	LCD column driver output 36
C35	54	2626	2282	LCD column driver output 35
C34	55	2626	2452	LCD column driver output 34
C33	56	2626	2622	LCD column driver output 33
C32	57	2626	2792	LCD column driver output 32
C31	58	2626	2962	LCD column driver output 31
C30	59	2626	3132	LCD column driver output 30

Table 3. Bonding pad description *…continued*

All x/y coordinates represent the position of the centre of each pad with respect to the centre (x/y = 0) of the chip (see Figure 2).

Symbol	Pad	X (µm)	Y (µm)	Description
C29	60	2339	3302	LCD column driver output 29
C28	61	2169	3302	LCD column driver output 28
C27	62	1999	3302	LCD column driver output 27
C26	63	1829	3302	LCD column driver output 26
C25	64	1659	3302	LCD column driver output 25
C24	65	1489	3302	LCD column driver output 24
C23	66	1319	3302	LCD column driver output 23
C22	67	1149	3302	LCD column driver output 22
C21	68	979	3302	LCD column driver output 21
C20	69	809	3302	LCD column driver output 20
C19	70	639	3302	LCD column driver output 19
C18	71	469	3302	LCD column driver output 18
C17	72	299	3302	LCD column driver output 17
C16	73	129	3302	LCD column driver output 16
C15	74	–245	3302	LCD column driver output 15
C14	75	–415	3302	LCD column driver output 14
C13	76	–585	3302	LCD column driver output 13
C12	77	–755	3302	LCD column driver output 12
C11	78	–925	3302	LCD column driver output 11
C10	79	–1095	3302	LCD column driver output 10
C9	80	–1265	3302	LCD column driver output 9
C8	81	–1435	3302	LCD column driver output 8
C7	82	–1605	3302	LCD column driver output 7
C6	83	–1775	3302	LCD column driver output 6
C5	84	–1945	3302	LCD column driver output 5
C4	85	–2115	3302	LCD column driver output 4
C3	86	–2285	3302	LCD column driver output 3
C2	87	–2455	3302	LCD column driver output 2
C1	88	–2625	3015	LCD column driver output 1
R24	89	–2625	2846	LCD row driver output 24
R23	90	–2625	2676	LCD row driver output 23
R22	91	–2625	2506	LCD row driver output 22
R21	92	–2625	2336	LCD row driver output 21
R20	93	–2625	2166	LCD row driver output 20
R19	94	–2625	1996	LCD row driver output 19
R18	95	–2625	1826	LCD row driver output 18
R17	96	–2625	1656	LCD row driver output 17
R8	97	–2625	1487	LCD row driver output 8
R7	98	–2625	1317	LCD row driver output 7

Table 3. Bonding pad description *...continued*

All x/y coordinates represent the position of the centre of each pad with respect to the centre (x/y = 0) of the chip (see Figure 2).

Symbol	Pad	X (μm)	Y (μm)	Description
R6	99	–2625	1147	LCD row driver output 6
R5	100	–2625	977	LCD row driver output 5
R4	101	–2625	807	LCD row driver output 4
R3	102	–2625	637	LCD row driver output 3
R2	103	–2625	467	LCD row driver output 2
R1	104	–2625	297	LCD row driver output 1
DB7	105	–2625	–290	1 bit of 8 bit bi-directional data bus
SCL	106	–2625	–479	I^2C-bus serial clock input
DB6	107	–2625	–716	1 bit of 8 bit bi-directional data bus
SDA	108	–2625	–976	I^2C-bus serial data input/output
DB5	109	–2625	–1202	1 bit of 8 bit bi-directional data bus
V_0	110	–2625	–1388	control input for V_{LCD}
V_{LCD1}	111	–2625	–1580	LCD supply voltage input/output 1
DB4	112	–2625	–1808	1 bit of 8 bit bi-directional data bus
V_{LCD2}	113	–2625	–1985	LCD supply voltage input/output 2
DB3	114	–2625	–2213	1 bit of 8 bit bi-directional data bus
V_{LCD3}	115	–2625	–2390	LCD supply voltage input/output 3
DB2	116	–2625	–2621	1 bit of 8 bit bi-directional data bus

7. Pin functions

7.1 RS: register select (parallel control)

RS selects the register to be accessed for read and write when the device is controlled by the parallel interface. RS = logic ‘0’ selects the instruction register for write and the Busy Flag and Address Counter for read. RS = logic ‘1’ selects the data register for both read and write. There is an internal pull-up on pin RS.

7.2 R/$\overline{W}$: read/write (parallel control)

R/$\overline{W}$ selects either the read (R/$\overline{W}$ = logic ‘1’) or write (R/$\overline{W}$ = logic ‘0’) operation when control is by the parallel interface. There is an internal pull-up on this pin.

7.3 E: data bus clock

The E pin is set HIGH to signal the start of a read or write operation when the device is controlled by the parallel interface. Data is clocked in or out of the chip on the negative edge of the clock. Note that this pin must be connected to logic ‘0’ (V_{SS}) when the I^2C-bus control is used.

7.4 DB0 to DB7: data bus

The bidirectional, 3-state data bus transfers data between the system controller and the PCF2116. DB7 may be used as the Busy Flag signalling that internal operations are not yet complet. In 4-bit operations the 4 higher order lines DB4 to DB7 are used; DB0 to DB3 must be left open circuit. There is an internal pull-up on each of the data lines. Note that these pins must be left open circuit when the I^2C-bus control is used.

7.5 C1 to C60: column driver outputs

These pins output the data for pairs of columns.This arrangement permits an optimized chip-on-glass (COG) design for 4-line, 12 character layouts.

7.6 R1 to R32: row driver outputs

These pins output the row select waveforms to the left and right halves of the display.

7.7 V_{LCD}: LCD power supply

Negative power supply for the liquid crystal display.
This may be generated on-chip or supplied externally.

7.8 V_0: V_{LCD} control input

The input level at this pin determines the generated V_{LCD} output voltage.

7.9 OSC: oscillator

When the on-chip oscillator is used this pin must be connected to V_{DD}. This pin is the input for an external clock signal, if used.

7.10 SCL: serial clock line

Input for the I^2C-bus clock signal.

7.11 SDA: serial data line

Input/output for the I^2C-bus data line.

7.12 SA0: address pin

The hardware sub-address line is used to program the device sub-address for 2 different PCF2116s on the same I^2C-bus.

7.13 T1: test pad

Must be connected to V_{SS}. Not user accessible.

8. Functional description

8.1 LCD supply voltage generator for PCF2116x

The on-chip voltage generator is controlled by bit G of the ‘Function set’ instruction and V_0.

V_0 is a high-impedance input and draws no current from the system power supply. Its range is between V_{SS} and V_{DD} – 1 V. When V_0 is connected to V_{DD} the generator is switched off and an external voltage must be supplied to pin V_{LCD}. This can be more negative than V_{SS}.

When G = logic ‘1’ the generator produces a negative voltage at pin V_{LCD}, controlled by the input voltage at pin V_0. The LCD operating voltage is given by the relationship:

$$V_{OP} = (1.8V_{DD} - V_0)$$

Where:

$$V_{OP} = (V_{DD} - V_{LCD})$$

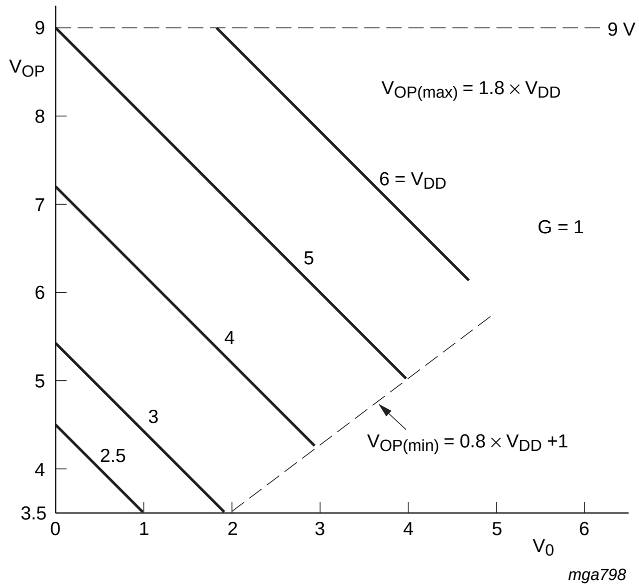
and

$$V_{LCD} = (V_0 - 0.8V_{DD})$$

When G = logic ‘0’, the generated output voltage V_{LCD} is equal to V_0 (between V_{SS} and V_{DD}). In this instance:

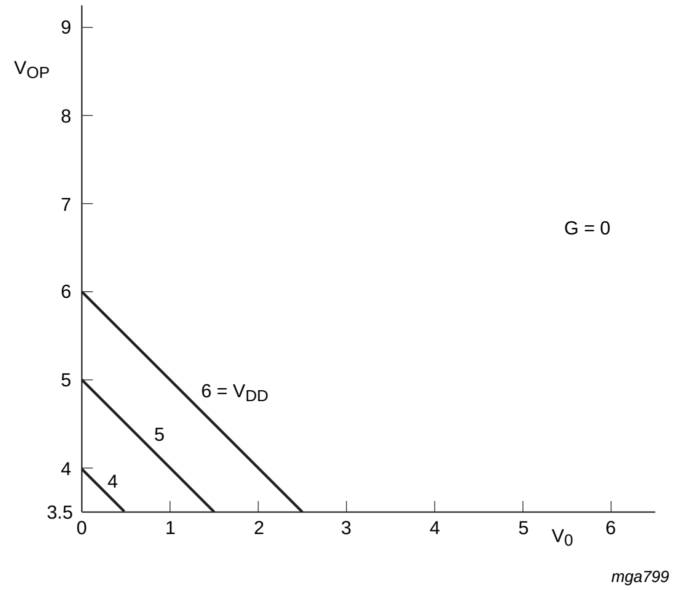
$$V_{OP} = V_{DD} - V_0$$

When V_{LCD} is generated on-chip the V_{LCD} pin must be de-coupled to V_{DD} with a suitable capacitor. V_{DD} and V_0 must be selected to limit the maximum value of V_{OP} to 9 V. Figure 3 and Figure 4 show the two generator control characteristics.



(1) High voltage mode: $V_{OP} = 1.8V_{DD} - V_0$

Fig 3. V_{OP} as a function of V_0 control characteristics (1)



(1) Buffer mode: $V_{OP} = V_{DD} - V_0$

Fig 4. V_{OP} as a function of V_0 control characteristics (2)

8.2 Character generator ROM (CGROM)

The character generator ROM generates 240 character patterns in 5 × 8 dot format from 8-bit character codes. Figure 5, Figure 6 and Figure 7 show the character sets currently available.

The standard character sets A, C and G are available for the PCF2116x.

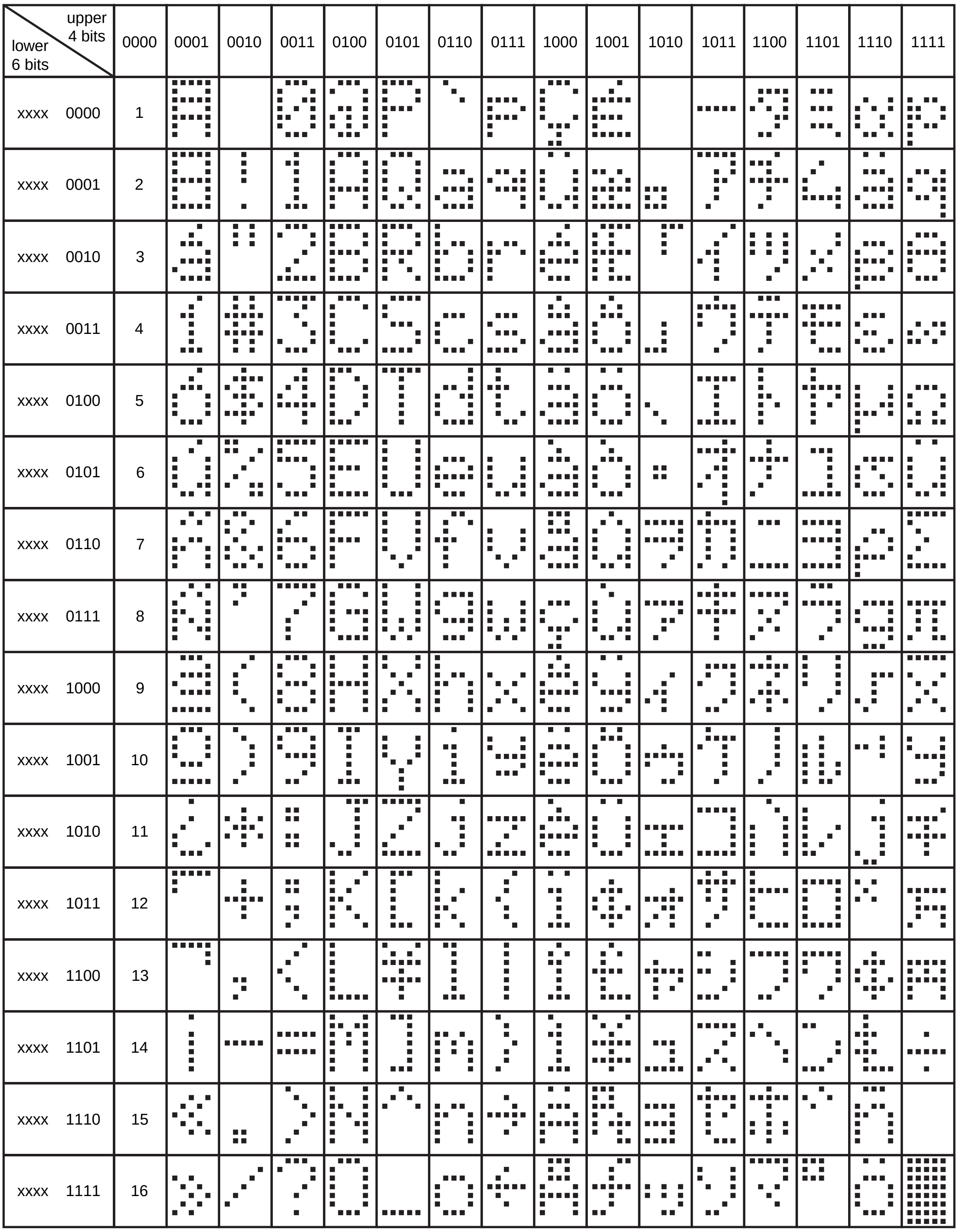


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Fig 5. Character set ‘A’ in CGROM: PCF2116A

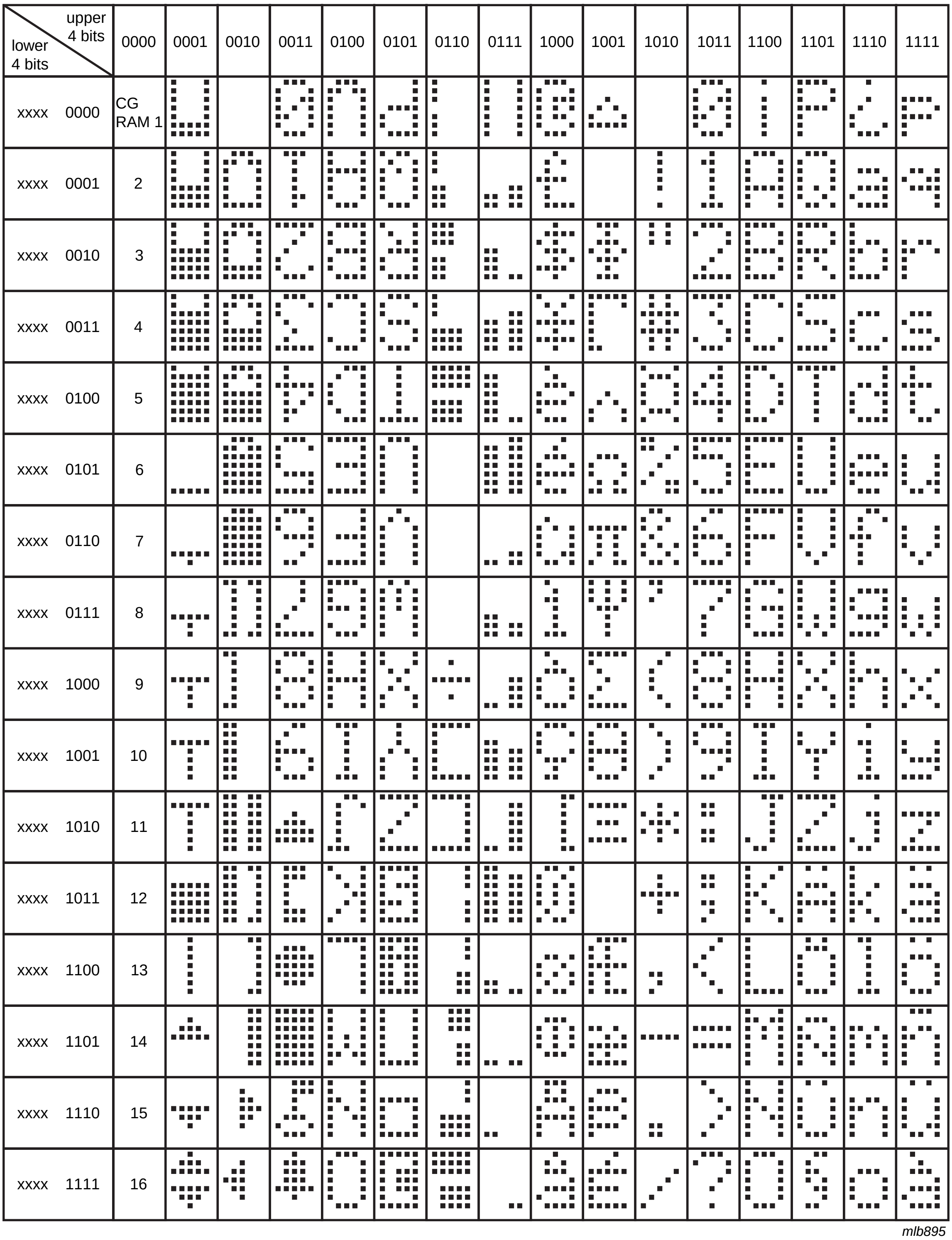


Fig 6. Character set ‘C’ in CGROM: PCF2116C

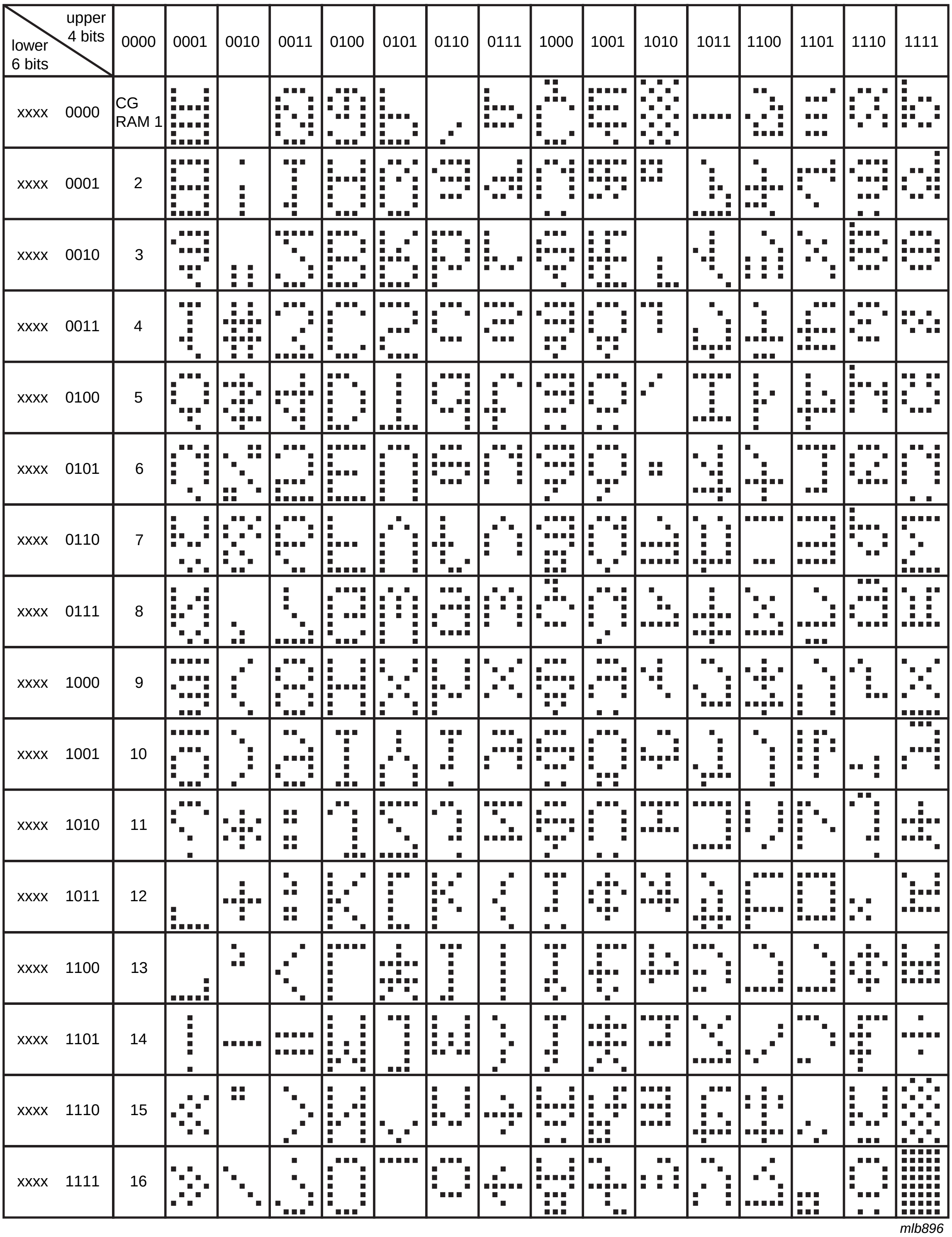


Fig 7. Character set ‘G’ in CGROM: PCF2116G

8.3 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for external bias chain resistors and significantly reduces the system power consumption. The optimum levels depend on the multiplex rate and are selected automatically when the number of lines in the display is defined.

The optimum value of V_{OP} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships in Table 4. Using a 5-level bias scheme for 1:16 MUX rate allows V_{OP} < 5 V for most LCD liquids. The effect on the display contrast is negligible.

Table 4. Optimum values for V_{OP}

MUX rate	Number of bias levels	V_{OP}/V_{th}	Discrimination V_{on}/V_{off}
1:16	5	3.67	1.277
1:32	6	5.19	1.196

8.4 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required. Pin OSC must be connected to V_{DD}.

8.5 External clock

If an external clock is to be used, it must be input at pin OSC. The resulting display frame frequency is given by $f_{frame} = \frac{1}{2304} f_{osc}$. A clock signal must always be present, otherwise the LCD is frozen in a DC state.

8.6 Power-on reset

The power-on reset block initializes the chip after power-on or power failure.

8.7 Registers

The PCF2116 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed.

The instruction register stores instruction codes such as ‘Display clear’ and ‘Cursor shift’, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to, but not read, by the system controller.

The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the Address Counter is written to the data register prior to being read by the ‘Read data’ instruction.

8.8 Busy flag

The Busy Flag indicates the free/busy status of the PCF2116. Logic ‘1’ indicates that the chip is busy and further instructions will not be accepted. The Busy Flag is output to pin DB7 when RS = logic ‘0’ and $R/\overline{W}$ = logic ‘1’. Instructions must only be written after checking that the Busy Flag is logic ‘0’ or waiting for the required number of clock cycles.

8.9 Address counter (AC)

The Address Counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the instructions 'Set CGRAM address' and 'Set DDRAM address'. After a read/write operation the Address Counter is automatically incremented or decremented by 1.The Address Counter contents are output to the bus (DB0 to DB6) when RS = logic '0' and R/W̄ = logic '1'.

8.10 Display data RAM (DDRAM)

The display data RAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations not used for storing display data can be used as general purpose RAM. The basic DDRAM-to-display mapping scheme is shown in Figure 8 and Figure 9.

With no display shift the characters represented by the codes in the first 12 or 24 RAM locations starting at address 00 in line 1 are displayed. Subsequent lines display data starting at addresses 20h, 40h, or 60h. Figure 10, Figure 11, Figure 12 and Figure 13 show the DDRAM-to-display mapping principle when the display is shifted.

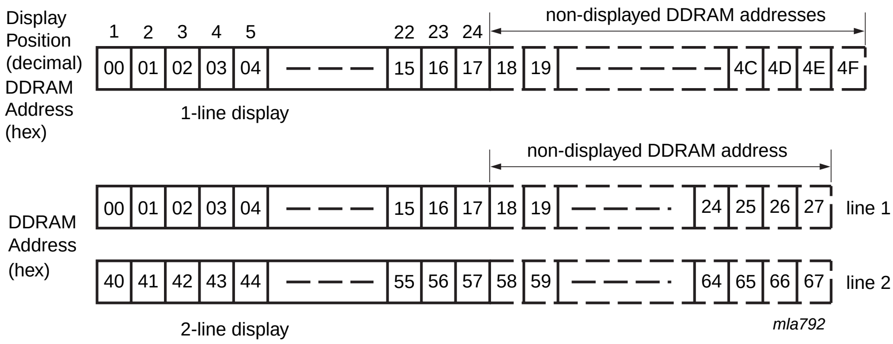


Fig 8. DDRAM-to display mapping (1); no shift.

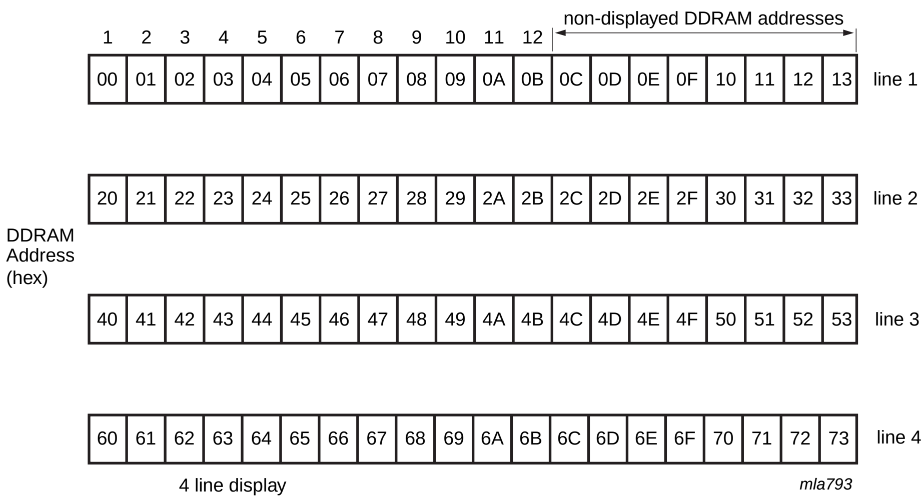


Fig 9. DDRAM-to display mapping (2); no shift.

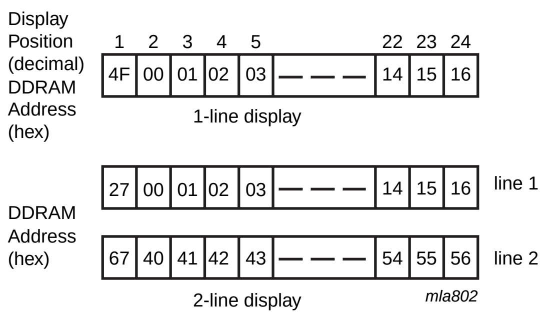


Fig 10. DDRAM-to display mapping (1); right shift.

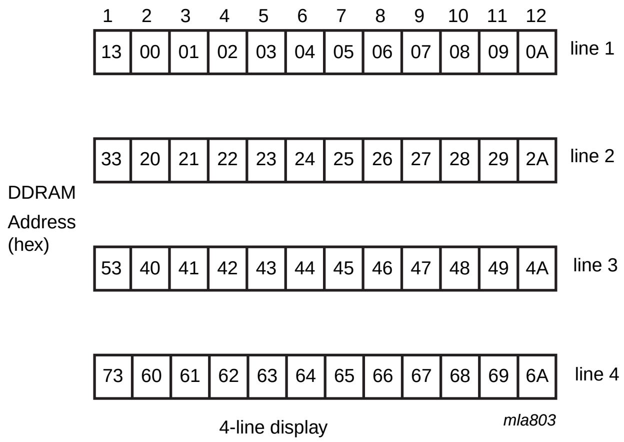


Fig 11. DDRAM-to display mapping (2); right shift.

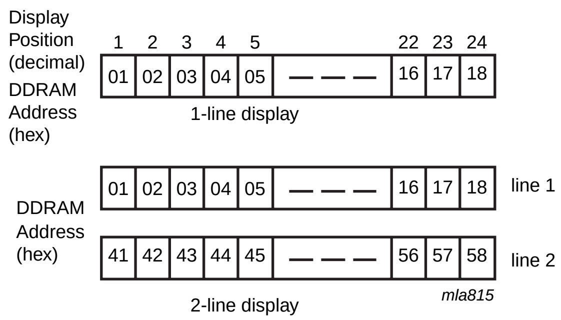


Fig 12. DDRAM-to display mapping (1); left shift.

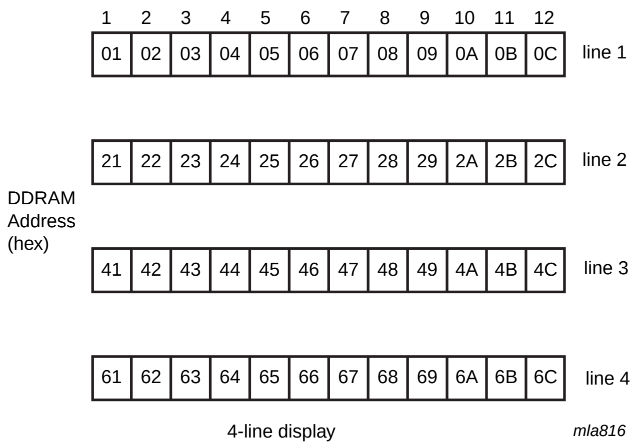


Fig 13. DDRAM-to display mapping (2); left shift.

The display address ranges are shown in Table 5.

Table 5. Display address ranges

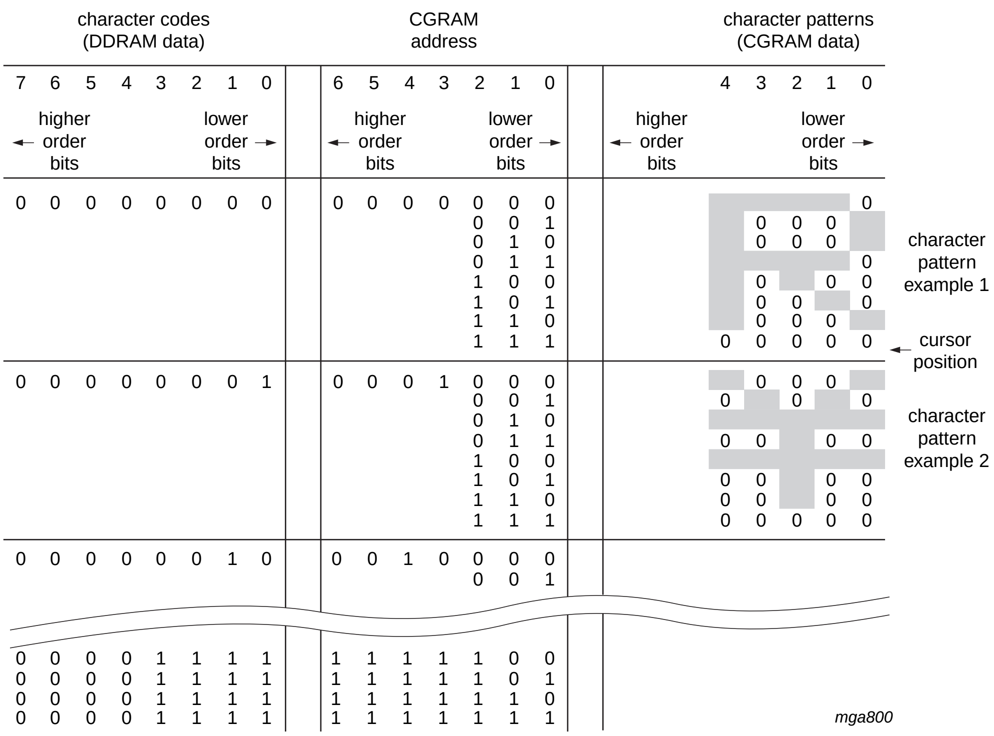
1-line display	2-line display	4-line display
00 to 4F	line 1: 00 to 27	line 1: 00 to 13
-	line 2: 40 to 67	line 2: 20 to 33
-	-	line 3: 40 to 53
-	-	line 4: 60 to 73

For 2 and 4-line displays the end address of one line and the start address of the next line are not consecutive. When the display is shifted each line wraps around independently of the others (Figure 10, Figure 11, Figure 12 and Figure 13).

When data is written into the DDRAM wrap-around occurs from 4F to 00 in 1-line mode and from 27 to 40 and 67 to 00 in 2-line mode; from 13 to 20, 33 to 40, 53 to 60 and 73 to 00 in 4-line mode.

8.11 Character generator RAM (CGRAM)

Up to 16 user-defined characters may be stored in the character generator RAM. The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Figure 5). Figure 14 shows the addressing principle for the CGRAM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th line will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Figure 14 (bit 4 being at the left end).

As shown in Figure 5 and Figure 14, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the ‘Set CGRAM address’ instruction. Bit 6 can be set using the ‘Set DDRAM address’ instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the ‘Read busy flag and address’ instruction.

Fig 14. Relationship between CGRAM addresses and data / display patterns

8.12 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or character blink as shown in Figure 15) at the DDRAM address contained in the Address Counter. When the Address Counter contains the CGRAM address the cursor will be inhibited.

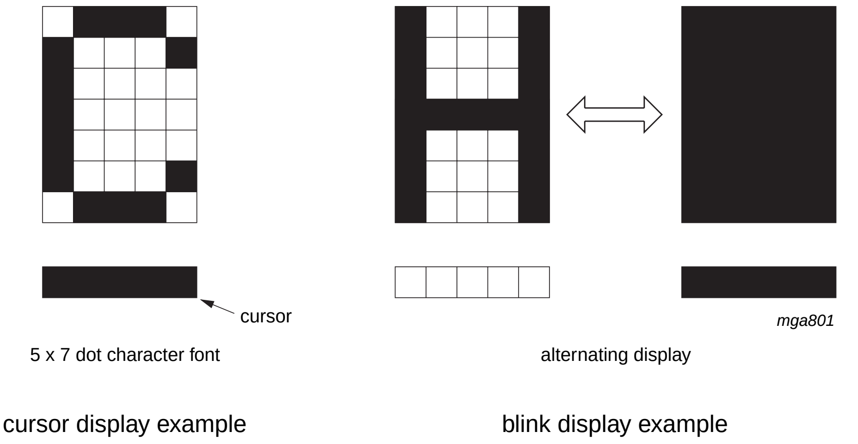


Fig 15. Cursor and blink display examples

8.13 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

8.14 LCD row and column drivers

The PCF2116 contains 32 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display, in accordance with the data to be displayed. The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figure 16 and Figure 17 show typical waveforms.

In 1-line mode (1:16) the row outputs are driven in pairs: R1/R17, R2/R18 for example. This allows the output pairs to be connected in parallel, providing greater drive capability.

Unused outputs should be left unconnected.

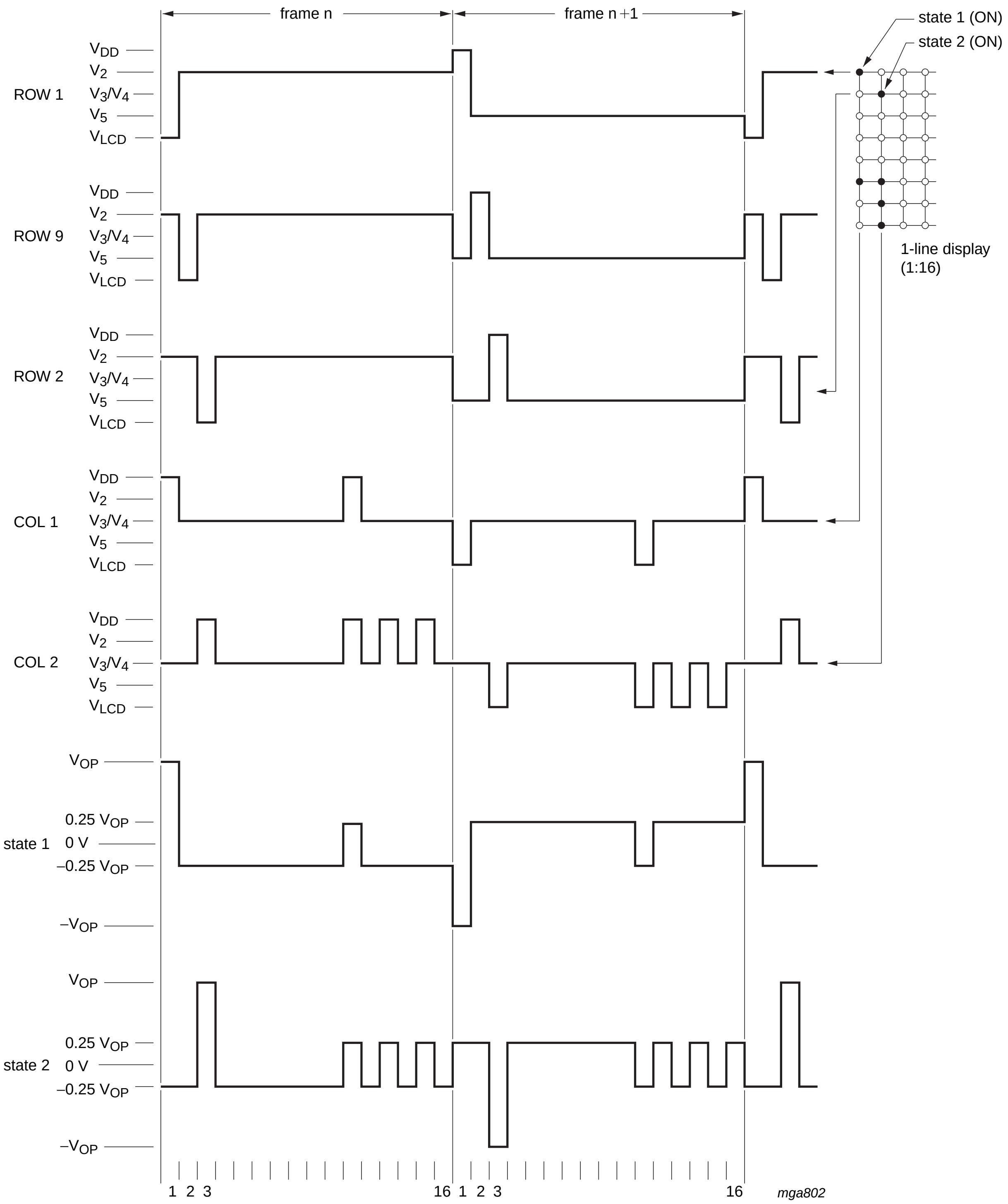


Fig 16. Typical LCD waveforms; 1-line mode

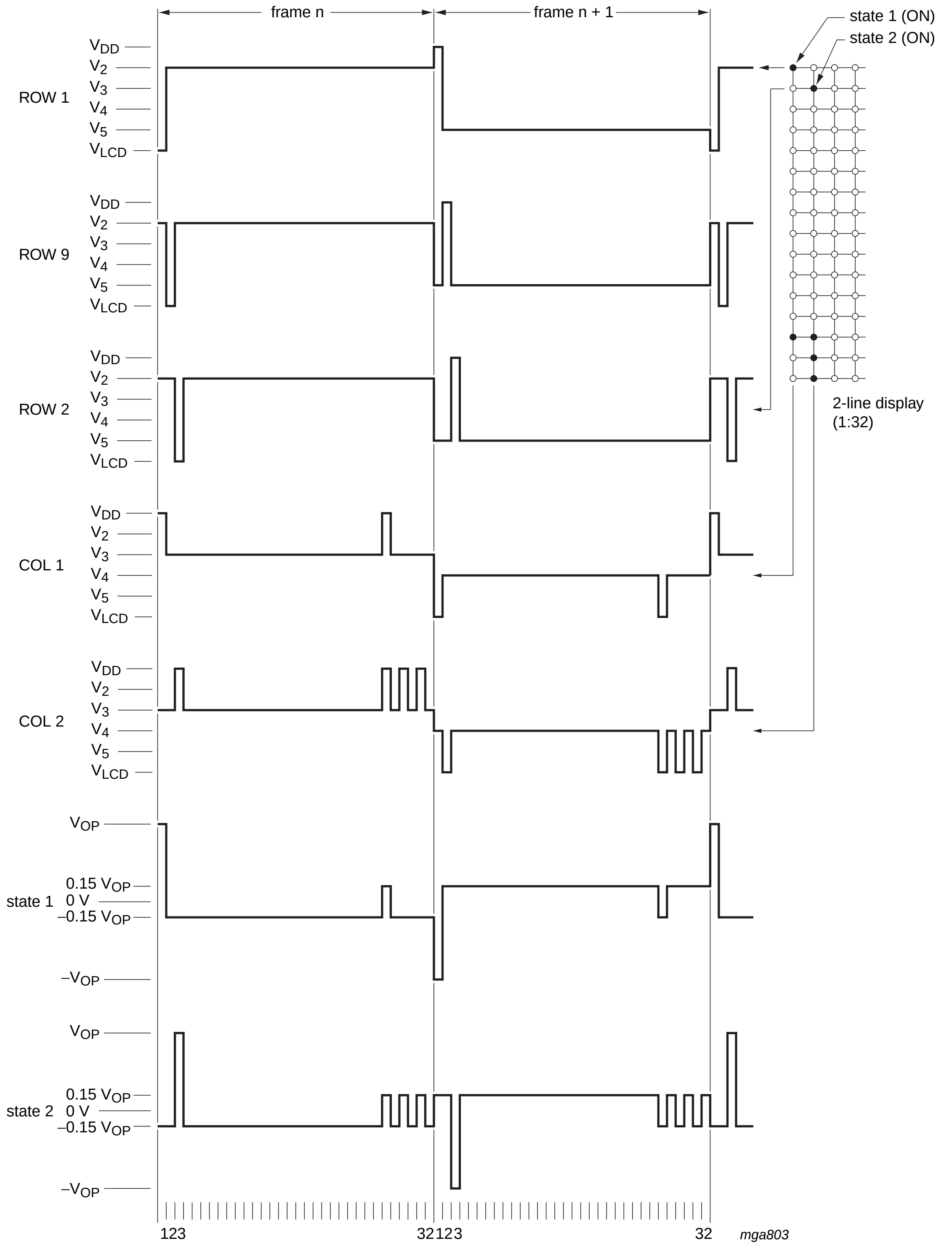


Fig 17. Typical LCD waveforms; 2-line mode

8.15 Reset function

The PCF2116 automatically initializes (resets) when power is turned on. After reset the chip has the following state (see Table 6):

Table 6. State after reset

Step	Description		
1	display clear		
2	function set	DL = 1	8-bit interface
		M, N = 0	1-line display
		G = 0	voltage generator; $V_{LCD} = V_0$
3	display on/off control	D = 0	display off
		C = 0	cursor off
		B = 0	blink off
4	entry mode set	I/D = 1	+1 increment
		S = 0	no shift
5	Default address pointer to DDRAM. The Busy Flag (BF) indicates the busy state (BF = logic '1') until initialization ends. The busy state lasts for 2 ms. The chip can also be initialized by software. (see Figure 18 and Figure 29).		
6	I^2C-bus interface reset		

9. Instructions

Only two PCF2116 registers, the Instruction Register (IR) and the Data Register (DR) are directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow an interface to various types of microcontrollers which operate at different speeds or to allow an interface to peripheral control ICs.
PCF2116 operation is controlled by the instructions shown in Table 8 together with their execution time.

There are 4 categories of instructions, those that:

- designate PCF2116 functions such as display format, data length, etc.
- set internal RAM addresses
- perform data transfer with internal RAM
- others.

In normal use, the data transfer instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation no instruction other than 'Read busy flag and address' is executed.

Because the Busy Flag is set to logic ‘1’ while an instruction is being executed, check to make sure it is on logic ‘0’ before sending the next instruction or wait for the maximum instruction execution time, as given in Table 8. An instruction sent while the Busy Flag is HIGH will not be executed.

Table 7. Command bit identities

Bit	0	1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	character at cursor position does not blink	character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
G	voltage generator: VLCD = V0	voltage generator; VLCD = V0 - 0.8VDD
N, (M = 0)		
PCF2116x	1 line × 24 characters; MUX 1:16	2 lines × 24 characters; MUX 1:32
N, (M = 1)	reserved	4 lines × 12 characters; MUX 1:32
BF	end of internal operation	internal operation in progress
Co	last control byte, only data bytes to follow	next two bytes are a data byte and another control byte

Table 8. Instructions

Instruction	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
NOP	0	0	0	0	0	0	0	0	0	0	No operation.
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display DDRAM address 0 i Counter.
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM addre Counter. Also return display to original po contents remain und
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move di specifies shift of dis operations are perfo data write and read.
Display control	0	0	0	0	0	0	1	D	C	B	Sets entire display c cursor on/off (C) and position character (B
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor and s without changing DD
Function set	0	0	0	0	1	DL	N	M	G	0	Sets interface data l number of display lin voltage generator co
Set CGRAM address	0	0	0	1	ACG						Sets CGRAM addre
Set DDRAM address	0	0	1	ADD							Sets DDRAM addre
Read busy flag and address	0	1	BF	AC							Reads Busy Flag (B internal operation is performed and read Counter contents.
Read data	1	1	read data								Reads data from CG DDRAM.
Write data	1	0	write data								Writes data to CGRA

[1] In the I^{2}C-bus mode the DL bit is don't care. 8-bit mode is assumed.

[2] In the I^{2}C-bus mode a control byte is required when RS or R/$\overline{W}$ is changed; control byte: Co, RS, R/$\overline{W}$, 0, 0, 0, 0, 0; command byte: DB7 to D

[3] Example: f_{osc} = 150 kHz, $T_{CY} = \frac{1}{f_{OSC}} = 6.67\mu s$; 3 cycles = 20 µs, 165 cycles = 1.1 ms.

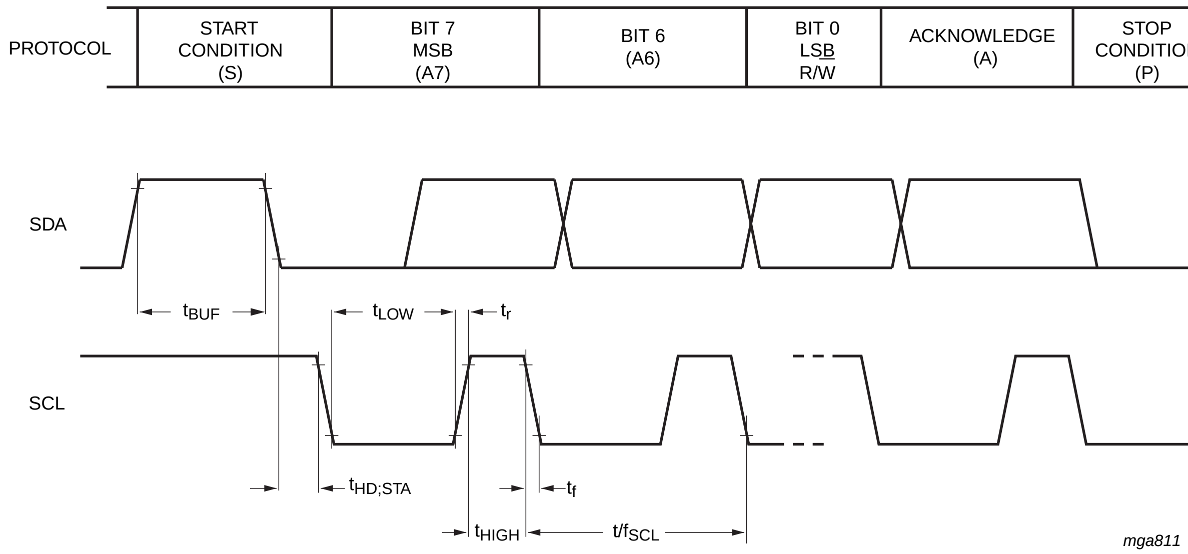


Fig 18. I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}

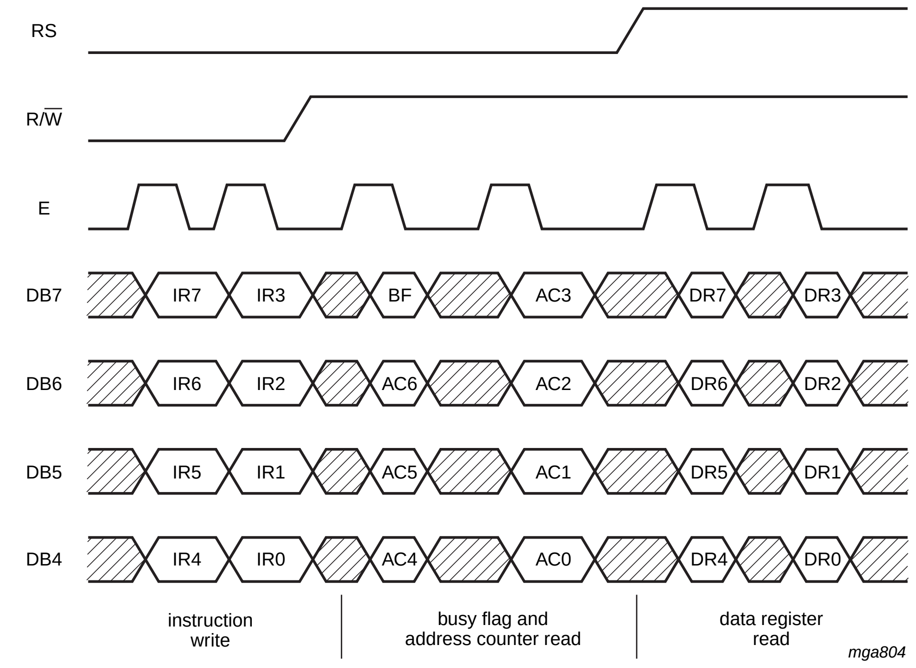
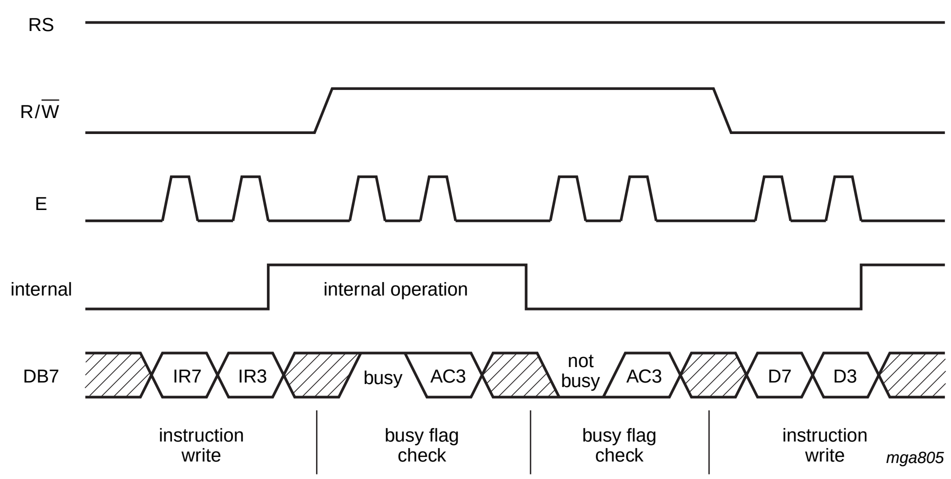


Fig 19. 4-bit transfer example



(1) IR7, IR3: instruction 7th bit, 3rd bit.

(2) AC3: Address counter 3rd bit.

Fig 20. 4-bit transfer timing sequence

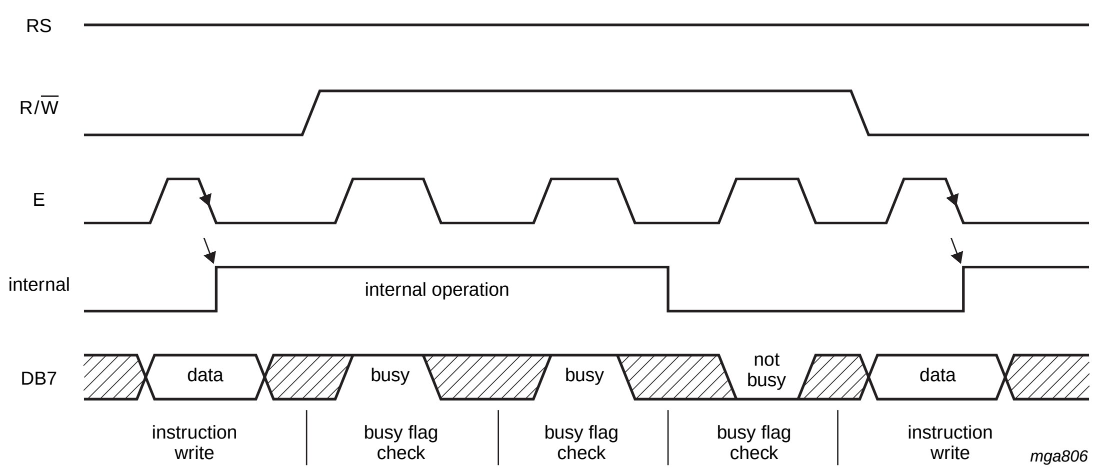


Fig 21. Busy flag check timing sequence

9.1 Clear display

‘Clear display’ writes space code 20h into all DDRAM addresses (The character pattern for character code 20 must be a blank pattern). Sets the DDRAM Address Counter to logic ‘0’. Returns the display to its original position if it was shifted. So, the display disappears and the cursor or blink position goes to the left edge of the display (the first line if 2 or 4 lines are displayed). Sets entry mode I/D = logic ‘1’ (increment mode). S of entry mode does not change.

The instruction ‘Clear display’ requires extra execution time. This is accommodated by checking the busy-flag (BF) or waiting for 2 ms. The latter must be applied where no read-back options are foreseen, as in some chip-on-glass (COG) applications.

9.2 Return home

‘Return home’ sets the DDRAM Address Counter to logic ‘0’ and returns the display to its original position if it was shifted. The DDRAM contents do not change. The cursor or blink position goes to the left of the display (the first line if 2 or 4 lines are displayed). I/D and S of entry mode do not change.

9.3 Entry mode set

9.3.1 I/D

When I/D = logic ‘1’ (or ‘0’) the DDRAM or CGRAM address increments (or decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor and blink are inhibited when the CGRAM is accessed.

9.3.2 S

When S = logic ‘1’, the entire display shifts either to the right (I/D = logic ‘0’) or to the left (I/D = logic ‘1’) during a DDRAM write. So, it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading from the CGRAM. When S = logic ‘0’ the display does not shift.

9.4 Display on/off control

9.4.1 D

The display is on when D = logic ‘1’ and off when D = logic ‘0’. Display data in the DDRAM is not affected and can be displayed immediately by setting D to logic ‘1’.

9.4.2 C

The cursor is displayed when C = logic ‘1’ and inhibited when C = logic ‘0’. Even if the cursor disappears, the display functions e.g. I/D, remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Figure 15).

9.4.3 B

The character indicated by the cursor blinks when B = logic ‘1’. The blink is displayed by switching between display characters and all dots on with a period of 1 second when f_{osc} = 150 kHz (see Figure 15). At other clock frequencies the blink period is equal to 150 kHz/f_{osc}.

The cursor and the blink can be set to display simultaneously.

9.5 Cursor display shift

‘Cursor/display shift’ moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2 or 4-line displays, the cursor moves to the next line when it passes the last position (40 or 20 decimal) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.
The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the cursor shift.

9.6 Function set

9.6.1 DL (parallel mode only)

Defines interface data width when the parallel data interface is used.

Data is sent or received in bytes (bits DB7 to DB0) when DL = logic ‘1’, or in two 4-bit nibbles (DB7 to DB4) when DL = logic ‘0’. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus.

In a 4-bit application DB3 to DB0 are left open (internal pull-ups). Hence in the first ‘Function set’ instruction after power-on, G and H are set to 1. A second ‘Function set’ must then be sent (2 nibbles) to set G and H to their required values.

When using the I^2C-bus interface the DL should not previously have been set to 0 using the parallel interface.

9.6.2 N, M

Sets the number of display lines.

9.6.3 G

Controls the V_{LCD} voltage generator characteristic.

9.7 Set CGRAM address

‘Set CGRAM address’ sets bit 0 to 5 of the CGRAM address (A_{CG} in Table 8) into the Address Counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Only bits 0 to 5 of the CGRAM address are set by the ‘Set CGRAM address’ instruction. Bit 6 can be set using the ‘Set DDRAM address’ instruction or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the ‘Read busy flag and address’ instruction.

9.8 Set DDRAM address

‘Set DDRAM address’ sets the DDRAM address (A_{DD} in Table 8) into the Address Counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

Table 9. Hexadecimal address ranges (pcf2116)

Address (h)	Function
00 to 4F	1-line by 24
00 to 27 and 40 to 67	2-lines by 24
00 to 13, 20 to 33, 40 to 53 and 60 to 73	4-lines by 12

9.9 Read busy flag and address

‘Read busy flag and address’ reads the Busy Flag (BF). BF = logic 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = logic 0, so BF should be checked before sending another instruction.

At the same time, the value of the Address Counter (A_C in Table 8) expressed in binary A[6] to A[0] is read out. The Address Counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

9.10 Write data to CGRAM or DDRAM

Writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous specification of the CGRAM or DDRAM address setting.

After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are ‘don’t care’ CGRAM addresses.

9.11 Read data from CGRAM or DDRAM

Reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent ‘Set address’ instruction determines whether the CGRAM or DDRAM is to be read.

The ‘Read data’ instruction gates the content of the data register (DR) to the bus while E = HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

Remark: the only three instructions which update the data register (DR) are:

- ‘Set CGRAM address’
- ‘Set DDRAM address’
- ‘Read data’ from CGRAM or DDRAM.

Other instructions (e.g. ‘Write data’, ‘Cursor/Display shift’, ‘Clear display’, ‘Return home’) do not modify the data register content.

10. Interface to microcontroller (parallel interface)

The PCF2116 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB0 to DB7. Three further control lines E, RS, and R/$\overline{W}$ are required.

In 4-bit mode data is transferred in two cycles of 4-bits each. The higher order bits (corresponding to DB4 to DB7 in 8-bit mode) are sent in the first cycle and the lower order bits (DB0 to DB3 in 8-bit mode) in the second.
Data transfer is complete after two 4-bit data transfers.
It should be noted that two cycles are also required for the Busy Flag check. 4-bit operation is selected by instruction. See Figure 19, Figure 20 and Figure 21 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

11. Interface to microcontroller (I²C-bus interface)

11.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL).
Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

11.2 Bit transfer

One data bit is transferred during each clock pulse.
The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

11.3 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

11.4 System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

11.5 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

11.6 I^2C-bus protocol

Before any data is transmitted on the I^2C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I^2C-bus configuration for the different PCF2116 READ and WRITE cycles is shown in Figure 22, Figure 23 and Figure 24.

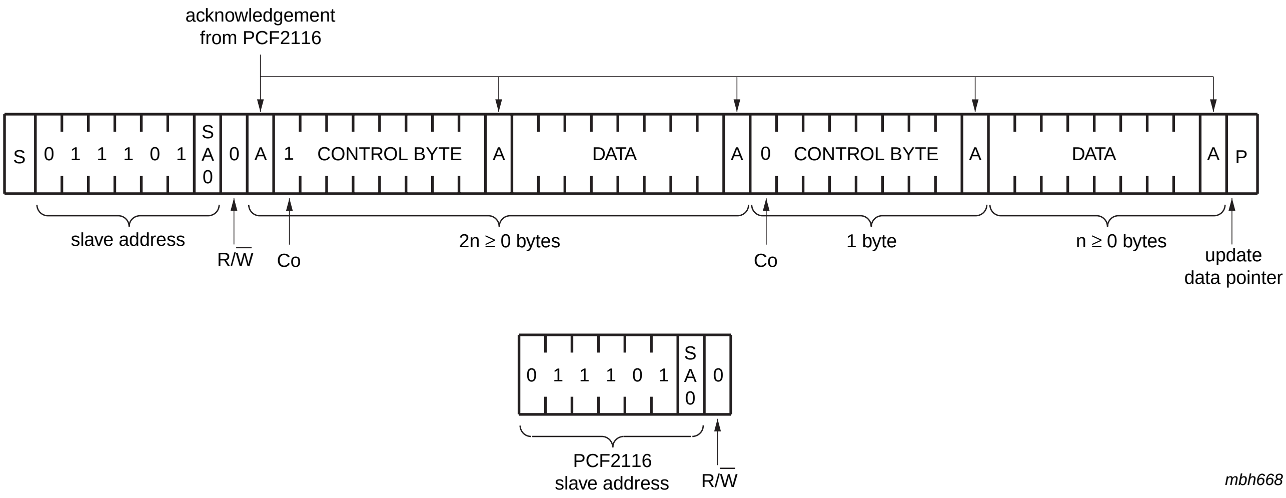


Fig 22. Master transmits to slave receiver; WRITE mode

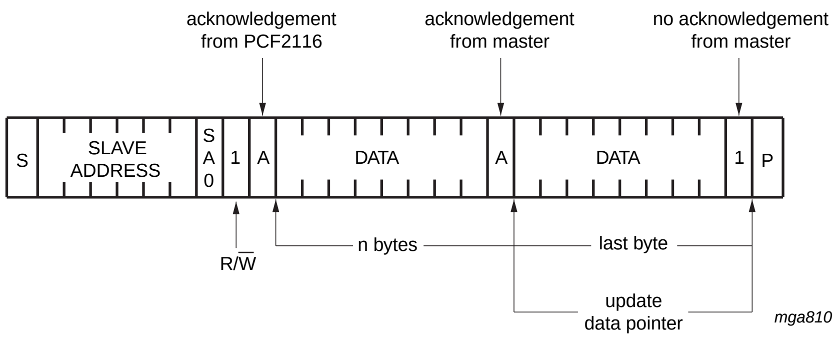
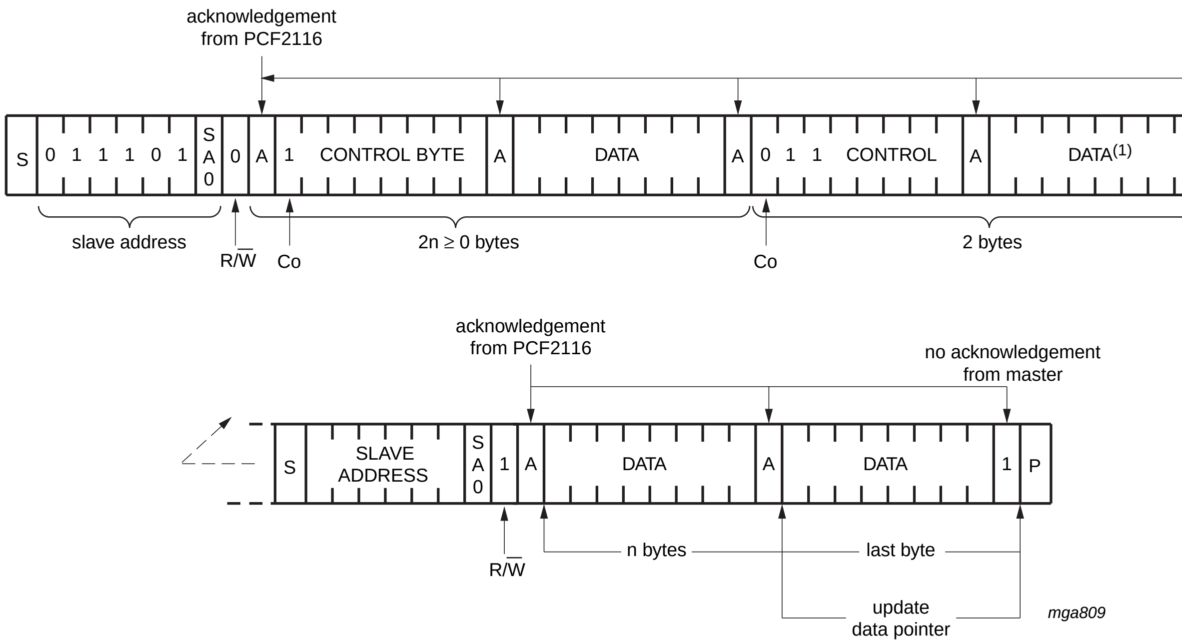


Fig 23. Master reads slave immediately after first byte; READ mode (RS previously defined)



(1) Last data byte is a dummy byte (may be omitted).

Fig 24. Master reads after setting word address; write word address, set RS/$\overline{\text{RW}}$; READ data

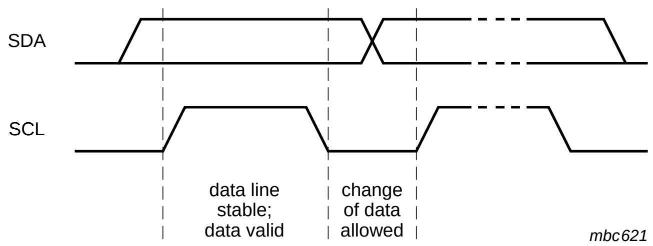


Fig 25. Bit transfer

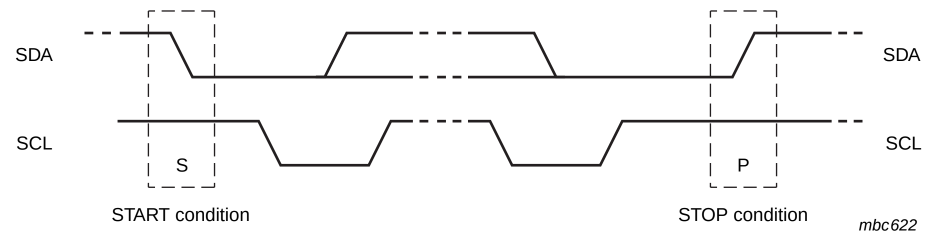


Fig 26. Definition of START and STOP conditions

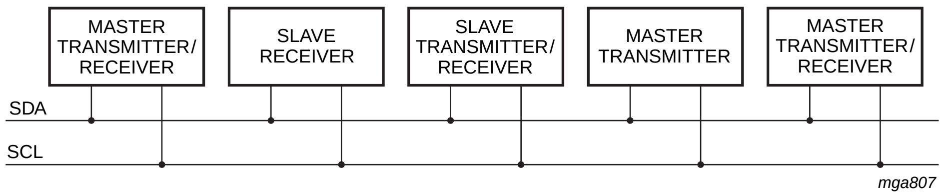


Fig 27. System configuration

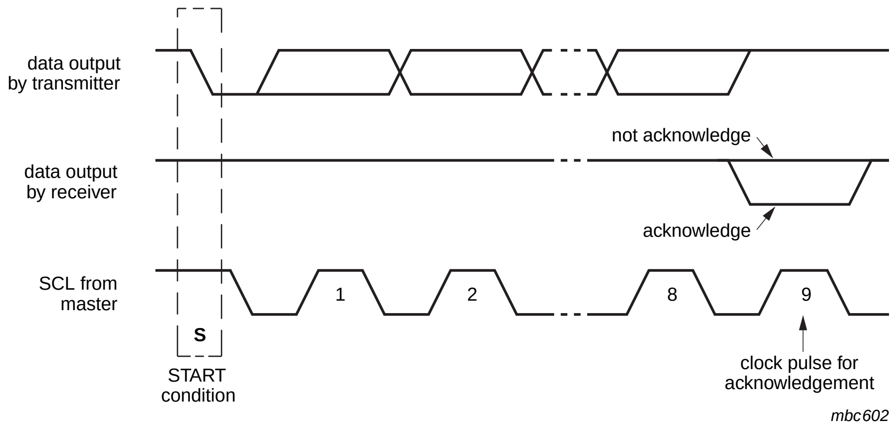


Fig 28. Acknowledgement on the I2C-bus

12. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	8.0	V
V_{LCD}	LCD supply voltage		V_{DD} – 11	V_{DD}	V
V_I	input voltage	on each of the pins OSC, V_0, RS, R/$\overline{W}$, E, and DB0 to DB7	V_{SS} – 0.5	V_{DD} + 0.5	V
V_O	output voltage	on each of the pins R1 to R32, C1 to C60 and V_{LCD}	V_{LCD} – 0.5	V_{DD} + 0.5	V
I_I	input current		–10	+10	mA
I_O	output current		–10	+10	mA
I_{DD}	supply current		–50	+50	mA
I_{SS}	ground supply current		–50	+50	mA
I_{LCD}	LCD supply current		–50	+50	mA
P_{tot}	total power dissipation		-	400	mW
P_O	output power		-	100	mW
T_{stg}	storage temperature		–65	+150	°C

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

12.1 ESD values

- ESD protection exceeds 5000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101.
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA.

13. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} – 3.5 V to V_{DD} – 9.0 V; T_{AMB} = –40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.5	-	6.0	V
V_{LCD}	LCD supply voltage			V_{DD} – 9	-	V_{DD} – 3.5	V
I_{DD}	supply current external V_{LCD}		[1]				
I_{DD1}	supply current 1	external V_{LCD}	[1]	-	200	500	µA
I_{DD2}	supply current 2	V_{DD} = 5 V; V_{OP} = 9 V; f_{OSC} = 150 kHz; T_{amb} = 25 °C	[1]	-	200	300	µA

Table 11. Static characteristics *...continued*

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9.0 V; T_{AMB} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD3}	supply current 3	V_{DD} = 3 V; V_{OP} = 5 V; f_{OSC} = 150 kHz; T_{amb} = 25 °C	[1]	-	150	200	µA
I_{DD4}	supply current 4	internal V_{LCD}	[1] [2] [8]	-	700	1100	µA
I_{DD5}	supply current 5	V_{DD} = 5 V; V_{OP} = 9 V; f_{OSC} = 150 kHz; T_{amb} = 25 °C	[1] [2] [8]	-	600	900	µA
I_{DD6}	supply current 6	V_{DD} = 3 V; V_{OP} = 5 V; f_{OSC} = 150 kHz; T_{amb} = 25 °C	[1] [2] [8]	-	500	800	µA
I_{LCD}	LCD supply current		[1] [7]	-	50	100	µA
V_{POR}	power on reset supply voltage		[3]	-	1.3	1.8	V
Logic							
V_{IL1}	LOW-level input voltage	input voltage on pins E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		V_{SS}	-	0.3 V_{DD}	V
V_{IH1}	HIGH-level input voltage	input voltage on pins E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		0.7 V_{DD}	-	V_{DD}	V
$V_{IL(OSC)}$	LOW-level input voltage on pin OSC			V_{SS}	-	V_{DD} − 1.5	V
$V_{IL(V0)}$	LOW-level input voltage on pin V_0			V_{SS}	-	V_{DD} − 1.5	V
$V_{IH(OSC)}$	HIGH-level input voltage on pin OSC			V_{DD} − 0.1	-	V_{DD}	V
$V_{IH(V0)}$	HIGH-level input voltage on pin V_0			V_{DD} − 0.05	-	V_{DD}	V
I_{PU}	pull-up current	pull-up current on pins DB0 to DB7; V_I = V_{SS}		0.04	0.15	1.0	µA
$I_{OL(DB)}$	LOW-level output current	low level output current on pins DB0 to DB7; V_{OL} = 0.4 V; V_{DD} = 5 V		1.6	-	-	mA
$I_{OH(DB)}$	HIGH-level output current	high level output current on pins DB0 to DB7; V_{OL} = 0.4 V; V_{DD} = 5 V		−1.0	-	-	mA
I_{L1}	leakage current	V_I = V_{DD} or V_{SS}; leakage current on pins OSC, V_0, E, RS, R/$\overline{W}$, DB0 to DB7 and SA0		−1.0	-	+1.0	µA
LCD outputs							
V_{tol2}	output voltage variation	LCD supply voltage (V_{LCD}) tolerance	[2]	−300	40	+300	mV
V_{tol1}	output voltage variation	bias voltage tolerance on each pin: R1 - R32 and C1 to C60	[7]	−300	40	+300	mV
R_{ROW}	output resistance	output resistance on each pin: R1 - R32	[6]	-	1.5	3.0	kΩ

Table 11. Static characteristics *...continued*

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9.0 V; T_{AMB} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{COL}	output resistance	output resistance on each pin: C1 - C60	[6]	-	3.0	6.0	kΩ
I²C-bus							
SDA, SCL							
V_{IL2}	LOW-level input voltage		[4]	V_{SS}	-	0.3 V_{DD}	V
V_{IH2}	HIGH-level input voltage		[4]	0.7 V_{DD}	-	V_{DD}	V
I_{L2}	leakage current	V_I = V_{DD} or V_{SS}; leakage current on pins SDA and SCL		−1.0	-	+1.0	µA
C_i	input capacitance		[5]	-	-	7	pF
$I_{OL(SDA)}$	LOW level output current on pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V		3	-	-	mA

[1] LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; V_0 = V_{DD}; bus inactive; internal or external clock with duty cycle 50% (I_{DD1} only).

[2] LCD outputs are open-circuit; LCD supply voltage generator is on; load current at V_{LCD} = 20 µA.

[3] Resets all logic when $V_{DD} < V_{POR}$.

[4] When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ± 0.5 mA.

[5] Tested on sample basis.

[6] Resistance of output terminals (R1 to R32 and C1 to C60) with load current = 150 µA; V_{OP} = V_{DD} − V_{LCD} = 9 V; outputs measured one at a time; (external V_{LCD}).

[7] LCD outputs open-circuit; external V_{LCD}.

[8] Maximum value occurs at 85 °C.

14. Dynamic characteristics

Table 12. Dynamic characteristics

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9.0 V; T_{AMB} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{osc}	clock frequency	external clock frequency		90	150	225	kHz
f_{FR}	LCD frame frequency	internal clock	[1]	40	65	100	Hz
Timing characteristics: Parallel interface			[1] [2]				
Write operation (writing data from microcontroller to PCF2116)							
T_{CY}	enable cycle time			500	-	-	ns
PW_{EH}	enable pulse width			220	-	-	ns
t_{ASU}	address set-up time			50	-	-	ns
t_{AH}	address hold time			25	-	-	ns
t_{DSW}	data set-up time			60	-	-	ns
t_{HD}	data hold time			25	-	-	ns
Read operation (reading data from PCF2116 to microcontroller)							
T_{CY}	enable cycle time			500	-	-	ns
PW_{EH}	enable pulse width			220	-	-	ns

Table 12. Dynamic characteristics *...continued*

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9.0 V; T_{AMB} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ASU}	address set-up time		50	-	-	ns
t_{AH}	address hold time		25	-	-	ns
t_{DHD}	data delay time		-	-	150	ns
t_{HD}	data hold time		20	-	100	ns
Timing characteristics: I^2C-bus		[2]				
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{SW}	tolerable spike pulse width	on the I^2C-bus	-	-	100	ns
t_{BUF}	bus free time between a STOP and START		4.7	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	-	µs
$t_{HD;STA}$	START condition hold time		4.0	-	-	µs
t_{LOW}	SCL LOW time		4.7	-	-	µs
t_{HIGH}	SCL HIGH time		4.0	-	-	µs
t_r	rise time of both SDA and SCL signals		-	-	1.0	µs
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0.0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	-	µs

[1] V_{DD} = 5 V.

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

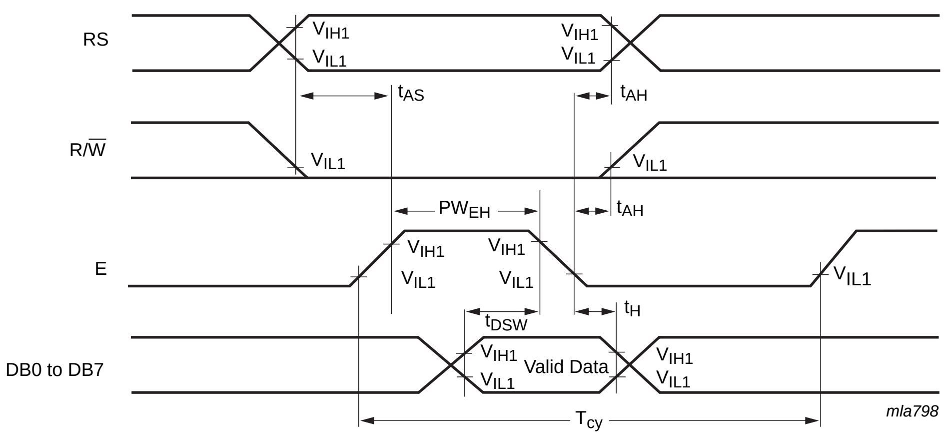


Fig 29. Parallel bus write operation sequence; writing data from microcontroller to PCF2116

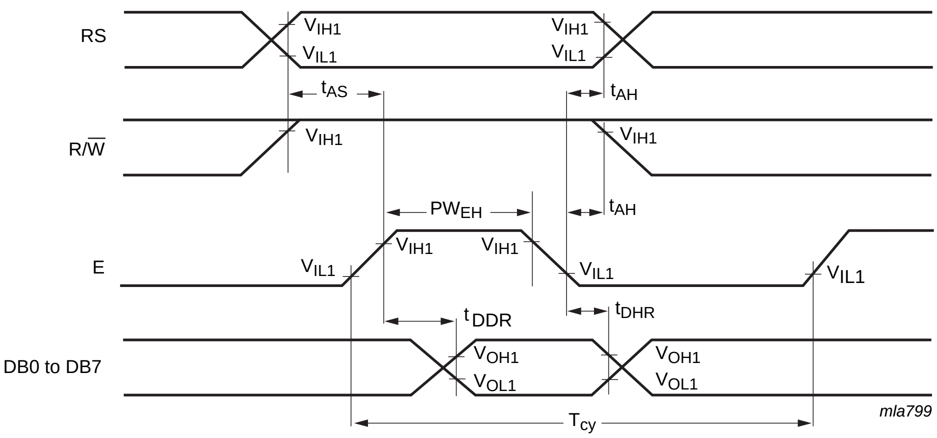


Fig 30. Parallel bus read operation sequence; reading data from PCF2116 to microcontroller

15. Application information

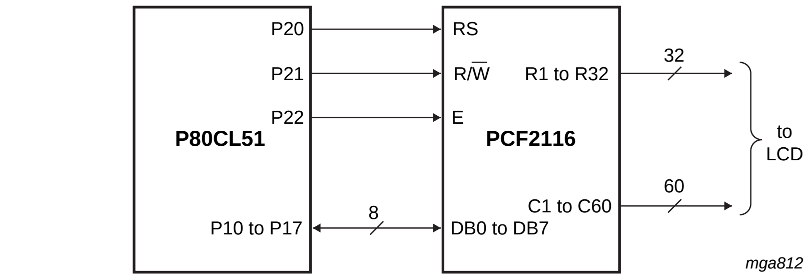


Fig 31. Direct connection to 8-bit microcontroller, 8-bit bus

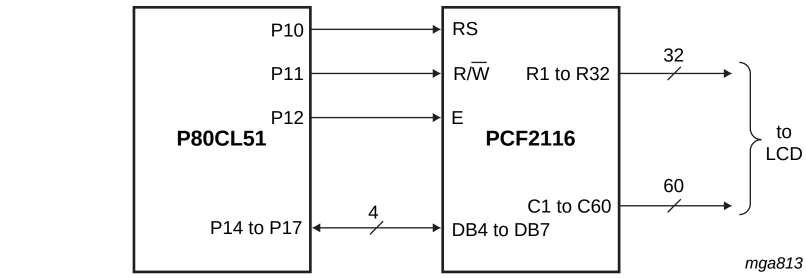


Fig 32. Direct connection to 8-bit microcontroller, 4-bit bus

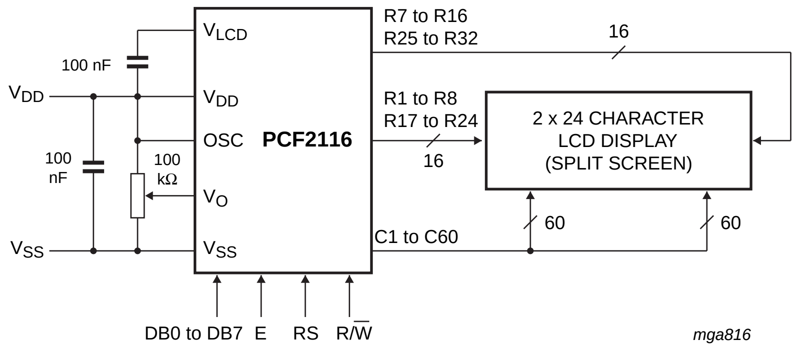


Fig 33. Typical application using parallel interface

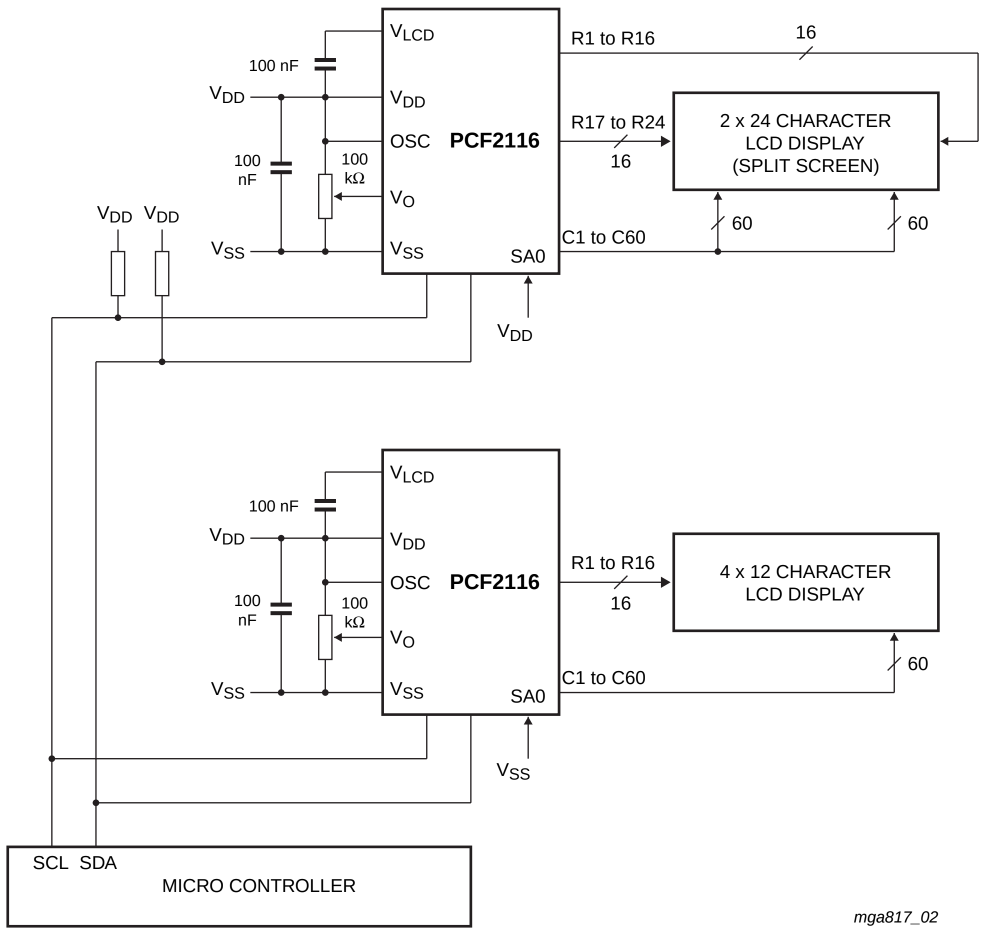


Fig 34. Application using I²C-bus interface

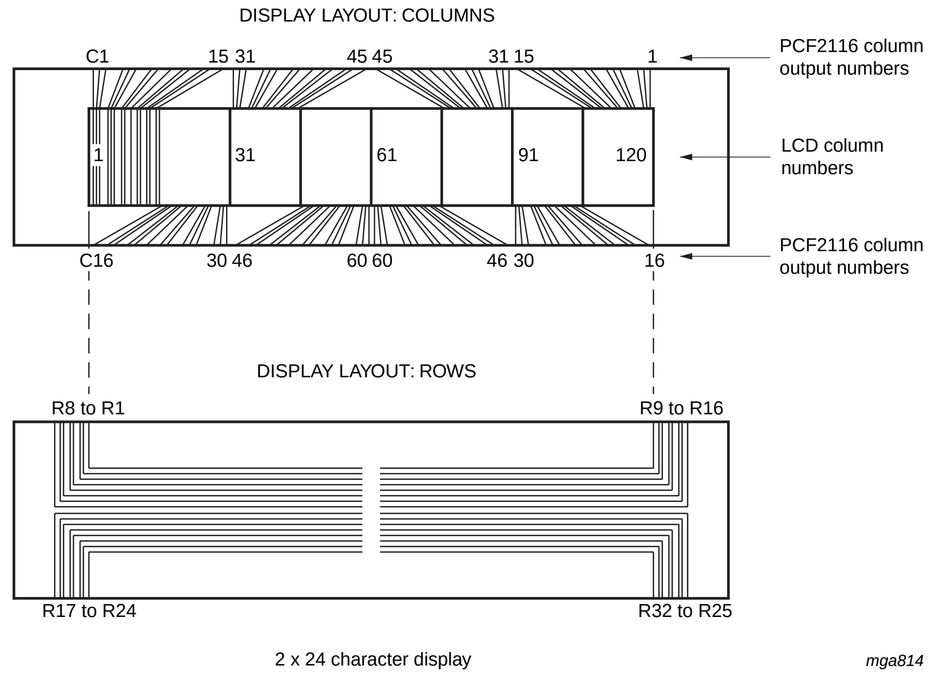


Fig 35. 2 × 24 display layout example (PCF2116x)

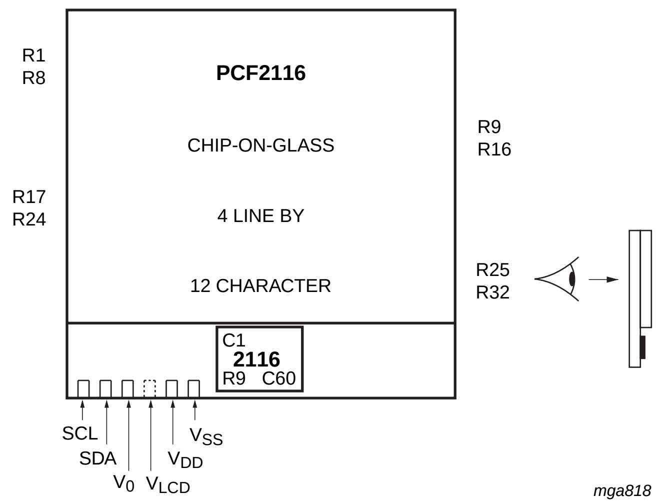


Fig 36. Chip-on-glass application

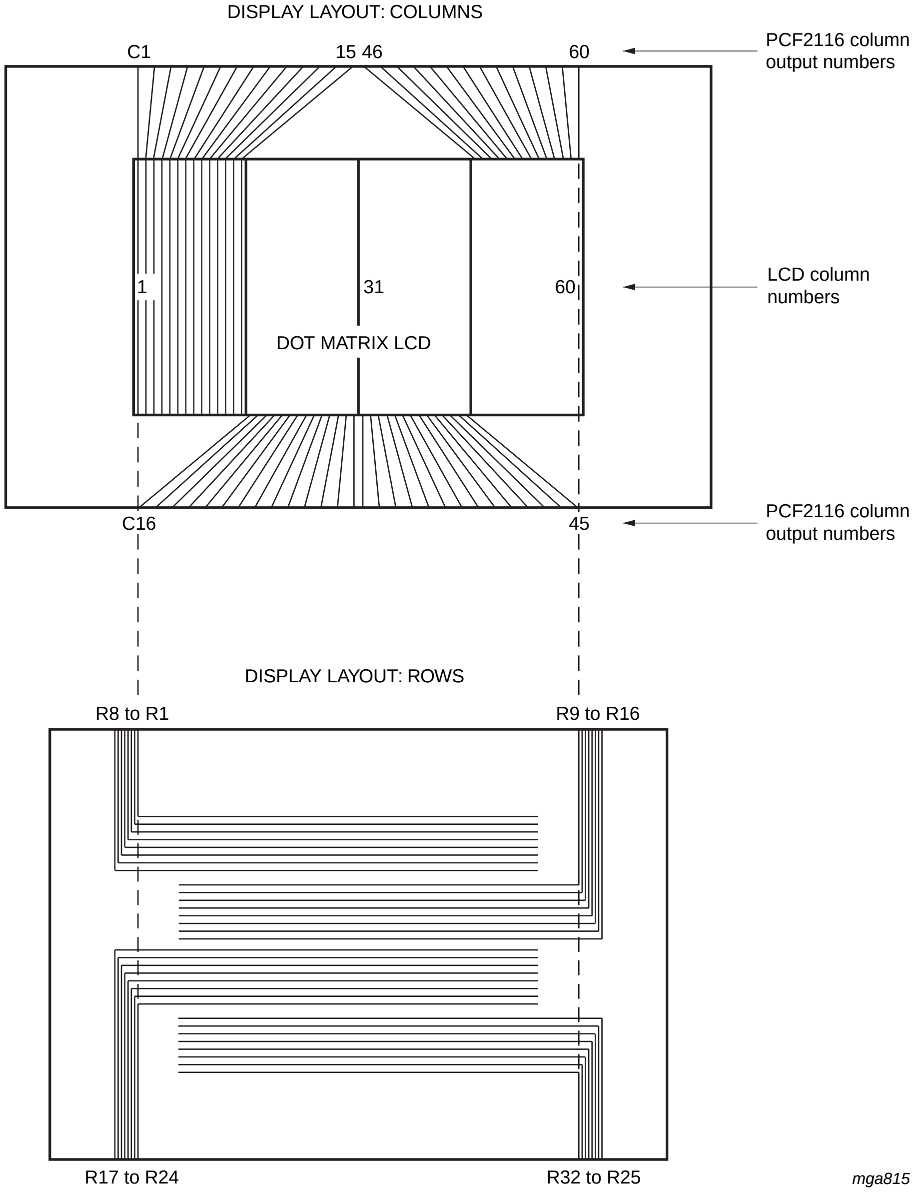


Fig 37. 4 × 12 display layout example (PCF2116)

15.1 4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation. Table 13 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2116 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 13 step 3).

So, DB4 to DB7 of the function set are written twice.

Table 13. 4-bit operation, 1-line display example; using internal reset

Step	Instruction						Display	Operation
1	power supply on (PCF2116 is initialized by the internal reset circuit)							Initialized. No display appears.
2	function set							
	RS	R/W	DB7	DB6	DB5	DB4		Sets to 4-bit operation. In this instance operation is handled as 8-bits by initialization and only this instruction completes with one write.
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		Sets to 4-bit operation, selects 1-line display and VLCD = V0. 4-bit operation starts from this point and resetting is needed.
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	Turns on display and cursor. Entire display is blank after initialization.
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	Sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
	0	0	0	1	1	0		
6	write data to CGRAM/DDRAM							
	1	0	0	1	0	1	P_	Writes ‘P’. The DDRAM has already been selected by initialization at power-on. The cursor is incremented by 1 and shifted to the right.
	1	0	0	0	0	0		

15.2 8-bit operation, 1-line display using internal reset

Table 14 shows an example of a 1-line display in 8-bit operation. The PCF2116 functions must be set by the ‘Function set’ instruction prior to display. Since the display data RAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation. Since the display shift operation changes the display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the Return Home operation is performed.

15.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line is written. So, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 15). Note that both lines of the display are always shifted together; data does not shift from one line to the other.

15.4 I^{2}C-bus operation, 1-line display

A control byte is required with most instructions (see Table 16).

15.5 Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, the PCF2116 must be initialized by instruction. Table 17 and Table 18 show how this may be performed for 8-bit and 4-bit operation.

Table 14. 8-bit operation, 1-line display example; using internal reset (character set 'A')

Step	Instruction										Display	Operation
1	power supply on (PCF2116 is initialized by the internal reset function)											Initialized. No display app
2	function set											
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Sets to 8-bit operation, se VLCD = V0.
	0	0	0	0	1	1	0	0	0	0		
3	display mode on/off control											Turns on display and curs initialization.
	0	0	0	0	0	0	1	1	1	0	–	
4	entry mode set											Sets mode to increment th cursor to the right at the t DD/CGRAM. Display is no
	0	0	0	0	0	0	0	1	1	0	–	
5	write data to CGRAM/DDRAM											Writes 'P'. The DDRAM h initialization at power-on. and shifted to the right.
	1	0	0	1	0	1	0	0	0	0	P_	
6	write data to CGRAM/DDRAM											
	1	0	0	1	0	0	1	0	0	0	PH_	Writes 'H'.
7											⋮	
8	write data to CGRAM/DDRAM											
	1	0	0	1	0	1	0	0	1	1	PHILIPS_	Writes 'S'.
9	entry mode set											
	0	0	0	0	0	0	0	1	1	1	PHILIPS_	Sets mode for display shi
10	write data to CGRAM/DDRAM											
	1	0	0	0	1	0	0	0	0	0	PHILIPS_	Writes space.
11	write data to CGRAM/DDRAM											
	1	0	0	1	0	0	1	1	0	1	PHILIPS M_	Writes 'M'.
12											⋮	
13	write data to CGRAM/DDRAM											
	1	0	0	1	0	0	1	1	1	1	MICROKO	Writes 'O'.
14	cursor or display shift											
	0	0	0	0	0	1	0	0	0	0	MICROKO	Shifts only the cursor pos

Table 14. 8-bit operation, 1-line display example; using internal reset (character set 'A')

Step	Instruction										Display	Operation
15	cursor or display shift											
	0	0	0	0	0	1	0	0	0	0	MICROKO	Shifts only the cursor pos
16	write data to CGRAM/DDRAM											
	1	0	0	1	0	0	0	0	1	1	ICROCO	Writes 'C' correction. The
17	cursor or display shift											
	0	0	0	0	0	1	1	1	0	0	MICROCO	Shifts the display and cur
Z18	cursor or display shift											
	0	0	0	0	0	1	0	1	0	0	MICROCO_	Shifts only the cursor to tl
19	write data to CGRAM/DDRAM											
	1	0	0	1	0	0	1	1	0	1	ICROCOM_	Writes 'M'.
20											| | |	
21	Return Home											
	0	0	0	0	0	0	0	0	1	0	PHILIPS M	Returns both display and (address 0).

Table 15. 8-bit operation, 2-line display example; using internal reset

Step	Instruction										Display	Operation
1	power supply on (PCF2116 is initialized by the internal reset function)											Initialized. No display app
2	function set											Sets to 8-bit operation, se generator off.
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
	0	0	0	0	1	1	1	0	0	0		
3	display on/off control										_	Turns on display and curs initialization.
	0	0	0	0	0	0	1	1	1	0		
4	entry mode set										_	Sets mode to increment th cursor to the right at the ti Display is not shifted.
	0	0	0	0	0	0	0	1	1	0		
5	Write data to CGRAM/DDRAM										P_	Writes 'P'. The DDRAM h initialization at power-on. and shifted to the right.
	1	0	0	1	0	1	0	0	0	0		
6											| | |	
7	write data to CGRAM/DDRAM										PHILIPS_	Writes 'S'.
	1	0	0	1	0	1	0	0	1	1		
8	set DDRAM address										PHILIPS	Sets DDRAM address to of the 2nd line.
	0	0	1	1	0	0	0	0	0	0	_	
9	write data to CGRAM/ DDRAM										PHILIPS	Writes 'M'.
	1	0	0	1	0	0	1	1	0	1	M_	
10											| | |	

Table 15. 8-bit operation, 2-line display example; using internal reset

Step	Instruction										Display	Operation
11	write data to CGRAM/ DDRAM										PHILIPS	Writes ‘O’.
	1	0	0	1	0	0	1	1	1	1	MICROCO_	
12	write data to CGRAM/ DDRAM										PHILIPS	Sets mode for display shi
	0	0	0	0	0	0	0	1	1	1	MICROCO_	
13	write data to CGRAM/ DDRAM										PHILIPS	Writes ‘M’. Display is shift second lines shift togethe
	1	0	0	1	0	0	1	1	0	1	ICROCOM_	
14											| | |	
15	return Home										PHILIPS	Returns both display and (address 0).
	0	0	0	0	0	0	0	0	1	0	MICROCOM	

Table 16. Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS} [1])

Step	Instruction									Display	Operation
1	I²C START										Initialized. No display appears.
2	slave address for write										During the acknowledge cycle SDA PCF2116.
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack		
	0	1	1	1	0	1	0	0	1		
3	send a control byte for function set										Control byte sets RS and R/W for f
	Co	RS	R/$\overline{W}$						Ack		
	0	0	0	X	X	X	X	X	1		
4	function set										Selects 1-line display and VLCD = acknowledge cycle starts executior
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	1	X	0	0	0	0	1		
5	display on/off control										Turns on display and cursor. Entire (blank in ASCII-like character sets)
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	0	0	1	1	1	0	1	_	
6	entry mode set										Sets mode to increment the addres the right at the time of write to the I not shifted.
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	0	0	0	0	1	1	0	1	_	
7	I²C START									_	For writing data to DDRAM, RS mu control byte is needed.
8	slave address for write										
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/$\overline{W}$	Ack		
	0	1	1	1	0	1	0	0	1	_	
9	send a control byte for write data										
	Co	RS	R/$\overline{W}$						Ack		
	0	1	0	X	X	X	X	X	1	_	
10	write data to DDRAM										Writes ‘P’. The DDRAM has been s The cursor is incremented by 1 and
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	1	0	1	0	0	0	0	1	P_	
11	write data to DDRAM										Writes ‘H’.
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		
	0	1	0	0	1	0	0	0	1	PH_	

Table 16. Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS} [1])

Step	Instruction	Display	Operation
12 to 15		| | |	
16	write data to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	PHILIPS_	Writes ‘S’.
17	(optional I²C stop) I²C start + slave address for write (as step 8)	PHILIPS_	
18	control byte Co RS R/W Ack 1 0 0 X X X X X 1	PHILIPS_	
19	Return Home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	PHILIPS	Sets DDRAM address 0 in Addres display to original position. DDRAM instruction does not update the Dat
20	control byte for read Co RS R/$\overline{W}$ Ack 0 1 1 X X X X X 1	PHILIPS	DDRAM content will be read from f The R/$\overline{W}$ has to be set to 1 while st
21	I²C START	PHILIPS	
22	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W Ack 0 1 1 1 0 1 0 1 1	PHILIPS	During the acknowledge cycle the c the internal I²C interface to be shift instruction neither a ‘Set address’ r performed. Therefore the content c
23	read data: 8 × SCL + master acknowledge [2] DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	PHILIPS	8 × SCL; content loaded into interfa acknowledge cycle is shifted out ov master acknowledge content of DD the I²C interface.
24	read data: 8 × SCL + master acknowledge [2] DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	PHILIPS	8 × SCL; code of letter ‘H’ is read fi acknowledge code of ‘I’ is loaded in
25	read data: 8 × SCL + no master acknowledge [2] DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	PHILIPS	No master acknowledge; After the register is shifted out no internal ac is loaded to the interface register, D updated, Address Counter (AC) is not shifted.
26	I²C stop	PHILIPS	

[1] X = don’t care.

[2] SDA is left at high-impedance by the microcontroller during the READ acknowledge.

Table 17. Initialization by instruction, 8 bit interface [1]

Step										Description
power-on or unknown state										
wait 2 ms after V_{DD} rises above V_{POR}										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	×	×	×	×	Function set (interface is 8 bits long)
wait 2 ms										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	×	×	×	×	Function set (interface is 8 bits long)
wait more than 40 μs										
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	×	×	×	×	Function set (interface is 8 bits long)
										BF can be checked after the following instructio checked the waiting time between instructions i (see Table 8).
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function set (interface is 8 bits long). Specify th voltage generator characteristics.
0	0	0	0	1	1	N	M	G	0	
0	0	0	0	0	0	1	0	0	0	Display off.
0	0	0	0	0	0	0	0	0	1	Clear display.
0	0	0	0	0	0	0	1	I/D	S	Entry mode set.
Initialization ends										

[1] X = don’t care.

Table 18. Initialization by instruction, 4 bit interface. Not applicable for I²C-bus operation.

Step						Description
power-on or unknown state						
wait 2 ms after V_{DD} rises above V_{POR}						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	Function set (interface is 8 bits long)
wait 2 ms						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	Function set (interface is 8 bits long)
wait more than 40 μs						
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	Function set (interface is 8 bits long)
						BF can be checked after the following instructions. When the BF is r between instructions is the specified instruction time (see Table 8).
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	Function set (set interface to 4 bits long).
0	0	0	0	1	1	Interface is 8 bits long
0	0	0	0	1	0	Function set (interface is 4 bits long).
0	0	N	M	G	0	Specify the number of display lines and voltage generator character
0	0	0	0	0	0	
0	0	1	0	0	0	Display off.
0	0	0	0	0	0	Clear display.
0	0	0	0	0	1	
0	0	0	0	0	0	Entry mode set.
0	0	0	1	I/D	S	
Initialization ends						

16. Package outline

Not applicable.

17. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

18. Packing information

Table 19. Tray dimensions (see Figure 38)

Symbol	Description	Value
A	pocket pitch in x direction	5.64 mm
B	pocket pitch in y direction	5.64 mm
C	pocket width in x direction	4.08 mm
D	pocket width in y direction	4.08 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
G	cut corner to pocket 1.1 centre	5.66 mm
H	cut corner to pocket 1.1 centre	5.66 mm
x	number of pockets, x direction	8
y	number of pockets, y direction	8

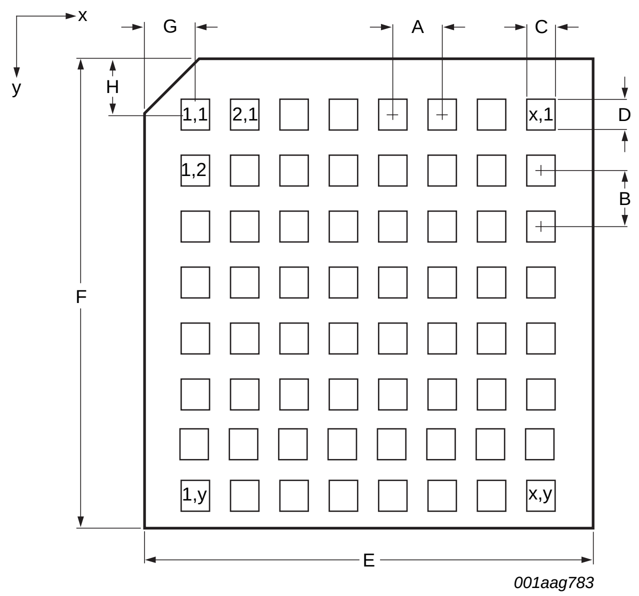


Fig 38. Tray details

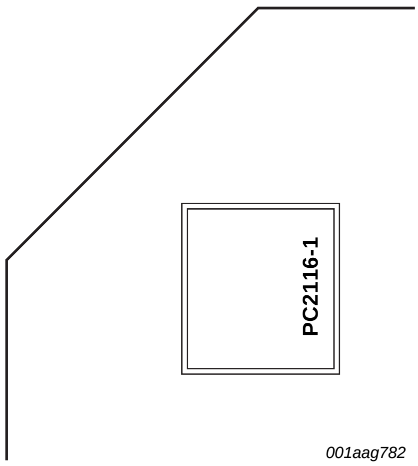


Fig 39. Tray alignment

19. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2116_FAM_5.01	<tbd>	Product data sheet	20070711 (date)	PCF2116_FAM_4
Modifications:	• Character set ‘A’ in CGROM corrected, Section 8.2. • Packing information added, Section 18 • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PCF2116_FAM_4	19970407	Product data sheet		PCF2116_3
PCF2116_3	19961025	Product data sheet		PCF2116_2
PCF2116_2	19941010	Product data sheet		PCF2116A_1
PCF2116A_1	19931215	Product data sheet		-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

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Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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Date of release: 20 July 2007

Document identifier: PCF2116_family_05