PCF2131

Nano-power highly accurate RTC with integrated quartz crystal

Rev. 1.1 — 15 October 2021 Product data sheet

1 General description

The PCF2131 is a CMOS Real Time Clock (RTC) and calendar with an integrated Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal optimized for very high accuracy and ultra low power consumption. The PCF2131 has a selectable I^2C-bus or SPI-bus, a backup battery switch-over circuit, a programmable watchdog function, four timestamps function, and many other features.

For a selection of NXP Real-Time Clocks, see Section 15.1.

2 Features and benefits

- Operating temperature range from -40 °C to +85 °C
- Temperature Compensated Crystal Oscillator (TCXO) with trimmed integrated capacitors
- Ultra low supply current: typical 64 nA at V_{DD} = 3.3 V
- Temperature compensated RTC, typical accuracy ±3 ppm from -40 °C to +85 °C
- Integration of a 32.768 kHz quartz crystal and oscillator in the same package
- Provides year, month, day, weekday, hours, minutes, seconds and 1/100 seconds
- Provides leap year correction
- Timestamp function
  - with interrupt capability
  - detection of four different events on four input pins (for example, for tamper detection)
- 2-line bidirectional 400 kHz Fast-mode I^2C-bus interface
- 4-line SPI-bus with separate data input and output (maximum speed 6.5 Mbit/s)
- Battery backup input pin and switch-over circuitry
- Battery backed output voltage
- Battery low detection function
- Power-On Reset (POR)
- Power-On Reset Override (PORO) function
- Software reset function
- Two interrupt outputs (open-drain)
- Programmable 1 second or 1 minute interrupt
- Programmable watchdog timer with interrupt
- Programmable alarm function with interrupt capability
- Programmable square output
- Clock operating voltage: 1.2 V to 5.5 V

3 Applications

- Electronic metering for electricity, water, and gas
- Precision timekeeping
- Access to accurate time of the day
- GPS equipment to reduce time to first fix
- Applications that require an accurate process timing
- Products with long automated unattended operation time

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCF2131TF	F31	HLSON16	thermal enhanced low profile small outline; no leads, 16 terminals, 0.125 dimple wettable flank, 0.5 mm pitch, 4.5 mm x 3.5 mm x 1.45 mm body	SOT1992-1

4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Package	Packing method	Minimum Order Quantity	Temperature
PCF2131TF	PCF2131TFY	HLSON16	REEL 13" Q1 DP	4000	T_{amb} = -40 °C to +85 °C

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

5 Block diagram

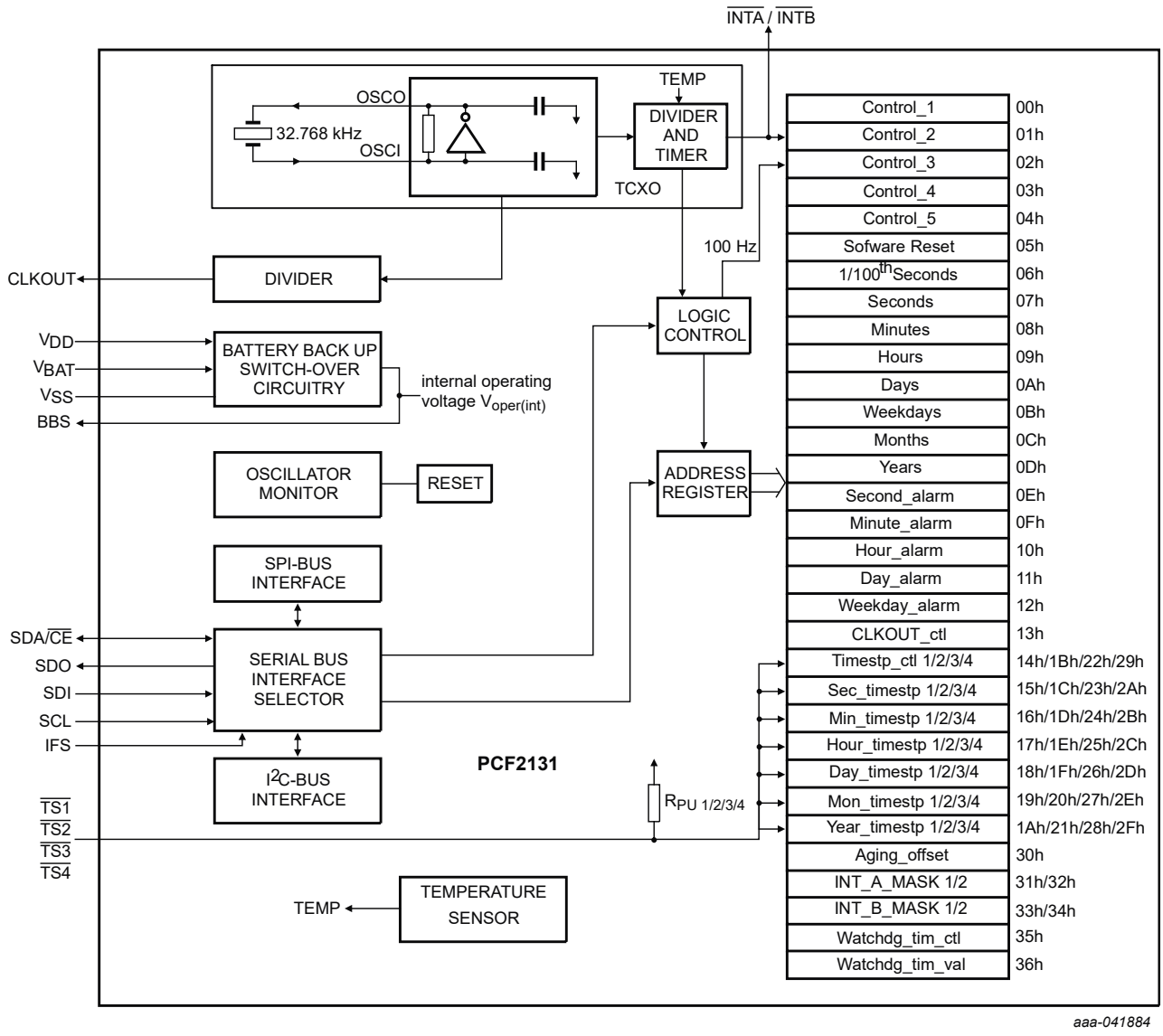


Figure 1. Block diagram of PCF2131

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

6 Pinning information

6.1 Pinning

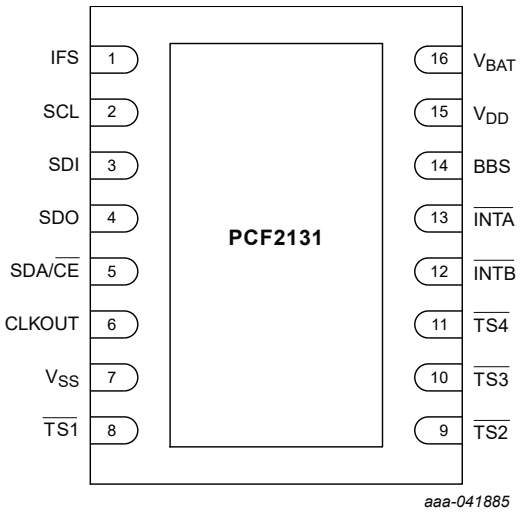


Figure 2. Pin configuration for PCF2131 (transparent top view)

6.2 Pin description

Table 3. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
SCL	2	combined serial clock input for both I^2C-bus and SPI-bus
SDI	3	serial data input for SPI-bus connect to pin V_{SS} if I^2C-bus is selected
SDO	4	serial data output for SPI-bus, push-pull leave open or connect to pin V_{SS} if I^2C-bus is selected
SDA/$\overline{CE}$	5	combined serial data input and output for the I^2C-bus and chip enable input (active LOW) for the SPI-bus
IFS	1	interface selector input connect to pin V_{SS} to select the SPI-bus connect to pin V_{DD} to select the I^2C-bus
$\overline{TS1}$,$\overline{TS2}$,$\overline{TS3}$,$\overline{TS4}$,	8,9,10,11	timestamp input (active LOW) with 500 kΩ internal pull-up resistor (R_{PU})
CLKOUT	6	clock output (push-pull)
V_{SS}	7	ground supply voltage
$\overline{INTB}$	12	interrupt B output (open-drain; active LOW)
$\overline{INTA}$	13	interrupt A output (open-drain; active LOW)
BBS	14	output voltage (battery backed)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 3. Pin description...*continued*

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
V_{BAT}	16	battery supply voltage (backup) connect to V_{SS} if battery switch-over is not used
V_{DD}	15	supply voltage
Exposed Pad		Tie to V_{SS} (preferred)[1] or leave floating

[1] This protects against signal feedback to the oscillator if routed close to the part.

7 Functional description

The PCF2131 is a Real Time Clock (RTC) and calendar with an on-chip Temperature Compensated Crystal (Xtal) Oscillator (TCXO) and a 32.768 kHz quartz crystal integrated into the same package.

Address and data are transferred by a selectable 400 kHz Fast-mode I^2C-bus or a 4-line SPI-bus with separate data input and output (see Section 7.16). The maximum speed of the SPI-bus is 6.5 Mbit/s.

The PCF2131 has a backup battery input pin and backup battery switch-over circuit which monitors the main power supply. The backup battery switch-over circuit automatically switches to the backup battery when a power failure condition is detected (see Section 7.5.1). Accurate timekeeping is maintained even when the main power supply is interrupted.

A battery low detection circuit monitors the status of the battery (see Section 7.5.2). When the battery voltage drops below a certain threshold value, a flag is set to indicate that the battery must be replaced soon. This ensures the integrity of the data during periods of battery backup.

7.1 Register overview

The PCF2131 contains an auto-incrementing address register: the built-in address register will increment automatically after each read or write of a data byte up to the register 36h. After register 36h, the auto-incrementing will wrap around to address 00h (see Figure 3).

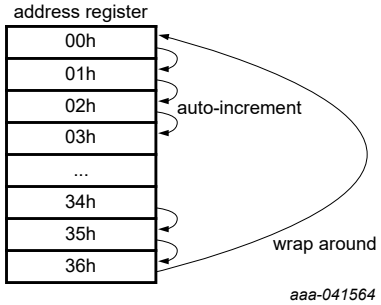


Figure 3. Handling address registers

- The first five registers (memory address 00h, 01h, 02h, 03h and 04h) are used as control registers (see Section 7.2).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

- The register at address 05h is for software reset.
- The memory addresses 06h through to 0Dh are used as counters for the clock function (1/100 seconds up to years). The date is automatically adjusted for months with fewer than 31 days, including corrections for leap years. The clock can operate in 12-hour mode with an AM/PM indication or in 24-hour mode (see Section 7.9).
- The registers at addresses 0Eh through 12h define the alarm function. It can be selected that an interrupt is generated when an alarm event occurs (see Section 7.10).
- The register at address 13h defines the temperature measurement period and the clock out mode. The temperature measurement can be selected from every 32 minutes (default) down to every 4minutes (see Table 17). CLKOUT frequencies of 32.768 kHz (default) down to 1 Hz for use as system clock, microcontroller clock, and so on, can be chosen (see Table 18).
- The registers at addresses 14h to 2Fh are used for the timestamp function. When the trigger event happens, the actual time is saved in the timestamp registers (see Section 7.12).
- The register at address 30h is used for the correction of the crystal aging effect (see Section 7.4.1).
- The registers at addresses 31h to 34h are used for interrupt configration.
- The registers at addresses 35h and 36h are used for the watchdog timer functions. The watchdog timer has four selectable source clocks allowing for timer periods from less than 20 ms to greater than 4 hours (see Table 59). An interrupt is generated when the watchdog times out.
- The registers 100th Seconds, Seconds, Minutes, Hours, Days, Months, and Years are all coded in Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bit-wise or standard binary.

When one of the RTC registers is written or read, the content of all counters is temporarily frozen, all registers hold their state during SPI or I2C transactions. The time stamp registers would update as soon as the bus transaction completes. This prevents a faulty writing or reading of the clock and calendar during a carry condition (see Section 7.9.9).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 4. Register overview

Bit positions labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control registers									
00h	Control_1	EXT_TEST	TC_DIS	STOP	100TH_S_DIS	POR_OVRD	12_24	MI	SI
01h	Control_2	MSF	WDTF	T	AF	T	T	AIE	T
02h	Control_3	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE
03h	Control_4	TSF1	TSF2	TSF3	TSF4	T	T	T	T
04h	Control_5	TSIE1	TSIE2	TSIE3	TSIE4	T	T	T	T
Software Reset									
05h	SR_Reset	CPR	T	T	T	SR	T	T	CTS
Time and date registers									
06h	100th_Seconds	100TH_SECONDS(0 to 99)							
07h	Seconds	OSF	SECONDS (0 to 59)						
08h	Minutes	-	MINUTES (0 to 59)						
09h	Hours	-	-	AMPM	HOURS (1 to 12) in 12-hour mode				
				HOURS (0 to 23) in 24-hour mode					
0Ah	Days	-	-	DAYS (1 to 31)					
0Bh	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)		
0Ch	Months	-	-	-	MONTHS (1 to 12)				
0Dh	Years	YEARS (0 to 99)							
Alarm registers									
0Eh	Second_alarm	AE_S	SECOND_ALARM (0 to 59)						
0Fh	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)						
10h	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
				HOUR_ALARM (0 to 23) in 24-hour mode					
11h	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)					
12h	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		
CLKOUT control register									

Table 4. Register overview*...continued*

Bit positions labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
13h	CLKOUT_ctl	TCR[1:0]		OTPR	-	-	COF[2:0]		
Timestamp1 registers									
14h	Timestp_ctl1	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]				
15h	Sec_timestp1	-	SECOND_TIMESTP (0 to 59)						
16h	Min_timestp1	-	MINUTE_TIMESTP (0 to 59)						
17h	Hour_timestp1	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				
					HOUR_TIMESTP (0 to 23) in 24-hour mode				
18h	Day_timestp1	-	-	DAY_TIMESTP (1 to 31)					
19h	Mon_timestp1	-	-	-	MONTH_TIMESTP (1 to 12)				
1Ah	Year_timestp1	YEAR_TIMESTP (0 to 99)							
Timestamp2 registers									
1Bh	Timestp_ctl2	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]				
1Ch	Sec_timestp2	-	SECOND_TIMESTP (0 to 59)						
1Dh	Min_timestp2	-	MINUTE_TIMESTP (0 to 59)						
1Eh	Hour_timestp2	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				
					HOUR_TIMESTP (0 to 23) in 24-hour mode				
1Fh	Day_timestp2	-	-	DAY_TIMESTP (1 to 31)					
20h	Mon_timestp2	-	-	-	MONTH_TIMESTP (1 to 12)				
21h	Year_timestp2	YEAR_TIMESTP (0 to 99)							
Timestamp3 registers									
22h	Timestp_ctl3	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]				
23h	Sec_timestp3	-	SECOND_TIMESTP (0 to 59)						
24h	Min_timestp3	-	MINUTE_TIMESTP (0 to 59)						
25h	Hour_timestp3	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				
					HOUR_TIMESTP (0 to 23) in 24-hour mode				
26h	Day_timestp3	-	-	DAY_TIMESTP (1 to 31)					
27h	Mon_timestp3	-	-	-	MONTH_TIMESTP (1 to 12)				

Table 4. Register overview*...continued*

Bit positions labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
28h	Year_timestp3	YEAR_TIMESTP (0 to 99)							
Timestamp4 registers									
29h	Timestp_ctl4	TSM	TSOFF	-	SUBSEC_TIMESTP[4:0]				
2Ah	Sec_timestp4	-	SECOND_TIMESTP (0 to 59)						
2Bh	Min_timestp4	-	MINUTE_TIMESTP (0 to 59)						
2Ch	Hour_timestp4	-	-	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				
					HOUR_TIMESTP (0 to 23) in 24-hour mode				
2Dh	Day_timestp4	-	-	DAY_TIMESTP (1 to 31)					
2Eh	Mon_timestp4	-	-	-	MONTH_TIMESTP (1 to 12)				
2Fh	Year_timestp4	YEAR_TIMESTP (0 to 99)							
Aging offset register									
30h	Aging_offset	-	-	-	-	AO[3:0]			
Interrupt mask registers									
31h	INT_A_MASK1	-	-	MIA	SIA	WD_CDA	AIEA	BIEA	BLIEA
32h	INT_A_MASK2	-	-	-	-	TSIE1A	TSIE2A	TSIE3A	TSIE4A
33h	INT_B_MASK1	-	-	MIB	SIB	WD_CDB	AIEB	BIEB	BLIEB
34h	INT_B_MASK2	-	-	-	-	TSIE1B	TSIE2B	TSIE3B	TSIE4B
Watchdog registers									
35h	Watchdg_tim_ctl	WD_CD	T	TI_TP	-	-	-	TF[1:0]	
36h	Watchdg_tim_val	WATCHDG_TIM_VAL[7:0]							

7.2 Control registers

The first five registers of the PCF2131, with the addresses 00h, 01h, 02h, 03h and 04h, are used as control registers.

7.2.1 Register Control_1

Table 5. Control_1 - control and status register 1 (address 00h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	EXT_TEST	TC_DIS	STOP	100TH_S_DIS	POR_OVRD	12_24	MI	SI
Reset value	0	0	0	0	1	0	0	0

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0	normal mode	Section 7.14
		1	external clock test mode	
6	TC_DIS	0	Temperature compensation enabled	Section 7.3.1
		1	Temperature compensation disabled	
5	STOP	0	RTC source clock runs	Section 7.15
		1	RTC clock is stopped; RTC divider chain flip-flops are asynchronously set logic 0; CLKOUT output frequencies are still available	
4	100TH_S_DIS	0	100th seconds counter enabled	-
		1	100th seconds counter Disabled, register 06h reset to 00h.	-
3	POR_OVRD	0	Power-On Reset Override (PORO) facility disabled; **set logic 0 for normal operation**	Section 7.7.2
		1	Power-On Reset Override (PORO) sequence reception enabled	
2	12_24	0	24-hour mode selected	Table 34, Table 50, Table 71
		1	12-hour mode selected	
1	MI	0	minute interrupt disabled	Section 7.13.1
		1	minute interrupt enabled	
0	SI	0	second interrupt disabled	
		1	second interrupt enabled	

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7.2.2 Register Control_2

Table 7. Control_2 - control and status register 2 (address 01h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	MSF	WDTF	T	AF	T	T	AIE	T
Reset value	0	0	0	0	0	0	0	0

Table 8. Control_2 - control and status register 2 (address 01h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7	MSF	0	no minute or second interrupt generated	Section 7.13
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt	
6	WDTF	0	no watchdog timer interrupt generated	Section 7.13.3
		1	flag set when watchdog timer interrupt generated; flag cannot be cleared by command (read-only)	
5	T	0	unused	-
4	AF	0	no alarm interrupt triggered	Section 7.10.6
		1	flag set when alarm triggered; flag must be cleared to clear interrupt	
3:2	T	0	unused	-
1	AIE	0	no interrupt generated from the alarm flag	Section 7.13.4
		1	interrupt generated when alarm flag set	
0	T	0	unused	-

7.2.3 Register Control_3

Table 9. Control_3 - control and status register 3 (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PWRMNG[2:0]			BTSE	BF	BLF	BIE	BLIE
Reset value	1	1	1	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 10. Control_3 - control and status register 3 (address 02h) bit description

Bit	Symbol	Value	Description	Reference
7 to 5	PWRMNG[2:0]	see Table 22	control of the battery switch-over, battery low detection, and extra power fail detection functions	Section 7.5
4	BTSE	0	no timestamp when battery switch-over occurs	Section 7.12.4
		1	time-stamped when battery switch-over occurs	
3	BF	0	no battery switch-over interrupt occurred	Section 7.5.1 and Section 7.12.4
		1	flag set when battery switch-over occurs; flag must be cleared to clear interrupt	
2	BLF	0	battery status ok; no battery low interrupt generated	Section 7.5.2
		1	battery status low; flag cannot be cleared by command, flag is automatically cleared when battery is replaced.	
1	BIE	0	no interrupt generated from the battery flag (BF)	Section 7.13.6
		1	interrupt generated when BF is set	
0	BLIE	0	no interrupt generated from battery low flag (BLF)	Section 7.13.7
		1	interrupt generated when BLF is set	

7.2.4 Register Control_4

Table 11. Control_4 - control and status register 4 (address 03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TSF1	TSF2	TSF3	TSF4	T	T	T	T
Reset value	0	0	0	0	0	0	0	0

Table 12. Control_4 - control and status register 4 (address 03h) bit description

Bit	Symbol	Value	Description	Reference
7	TSF1	0	no timestamp interrupt generated for pin $\overline{TS1}$	Section 7.12.1
		1	flag set when $\overline{TS1}$ input is driven to ground; flag must be cleared to clear interrupt	
6	TSF2	0	no timestamp interrupt generated when pin $\overline{TS2}$	Section 7.12.1
		1	flag set when $\overline{TS2}$ input is driven to ground; flag must be cleared to clear interrupt	
5	TSF3	0	no timestamp interrupt generated for pin $\overline{TS3}$	Section 7.12.1
		1	flag set when $\overline{TS3}$ input is driven to ground; flag must be cleared to clear interrupt	
4	TSF4	0	no timestamp interrupt generated when pin $\overline{TS4}$	Section 7.12.1
		1	flag set when $\overline{TS4}$ input is driven to ground; flag must be cleared to clear interrupt	
3	T	0	Unused	

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 12. Control_4 - control and status register 4 (address 03h) bit description...*continued*

Bit	Symbol	Value	Description	Reference
2	T	0	Unused	
1	T	0	Unused	
0	T	0	Unused	

7.2.5 Register Control_5

Table 13. Control_5 - control and status register 5 (address 04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TSIE1	TSIE2	TSIE3	TSIE4	T	T	T	T
Reset value	0	0	0	0	0	0	0	0

Table 14. Control_5 - control and status register 5 (address 04h) bit description

Bit	Symbol	Value	Description	Reference
7	TSIE1	0	no interrupt generated from timestamp flag of $\overline{TS1}$	Section 7.13.5
		1	interrupt generated when timestamp flag set of $\overline{TS1}$	
6	TSIE2	0	no interrupt generated from timestamp flag of $\overline{TS2}$	Section 7.13.5
		1	interrupt generated when timestamp flag set of $\overline{TS2}$	
5	TSIE3	0	no interrupt generated from timestamp flag of $\overline{TS3}$	Section 7.13.5
		1	interrupt generated when timestamp flag set of $\overline{TS3}$	
4	TSIE4	0	no interrupt generated from timestamp flag of $\overline{TS4}$	Section 7.13.5
		1	interrupt generated when timestamp flag set of $\overline{TS4}$	
3 to 0	T	0	unused	-

7.3 Register CLKOUT_ctl

Table 15. CLKOUT_ctl - CLKOUT control register (address 13h) bit allocation

Bits labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	TCR[1:0]		OTPR	T	T	COF[2:0]		
Reset value	0	0	X	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 16. CLKOUT_ctl - CLKOUT control register (address 13h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description	Reference
7 to 6	TCR[1:0]	see Table 17	temperature measurement period	
5	OTPR	0	no OTP refresh	Section 7.3.2
		1	OTP refresh performed	
4	T	0	unused [1]	
3	T	0	unused	
2 to 0	COF[2:0]	see Table 18	CLKOUT frequency selection	Section 7.3.3

[1] programming this bit to 1 may lead to a decrease of timing accuracy.

7.3.1 Temperature compensated Real Time Clock

The frequency of tuning fork quartz crystal oscillators is temperature-dependent. In the PCF2131, the frequency deviation caused by temperature variation is corrected by adjusting the RTC frequency divider with digital method.

The load capacitance is trimmed to the required value at 25 °C in order to compensate the frequency deviation over process variation.

The frequency accuracy at 25 °C can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT. However, the selection of f_{CLKOUT} = 32.768 kHz (default value) can lead to inaccurate measurements. Accurate frequency measurement occurs when f_{CLKOUT} = 16.384 kHz or lower is selected (see Table 18).

The temperature compensated frequency input for the Real Time Clock cannot be observed at the CLKOUT pin but can be evaluated by following these steps.

- Set Second Interrupt, bit SI in register Control_1 to 1
- Set bit TI_TP in register Watchdg_tim_ctl to 1 for a pulsed interrupt signal
- Set bit SIA in register INTA_MASK_1 to 0 to direct the Second Interrupt to pin INTA for a 1 Hz pulse output.

The RTC temperature compensation works by adding or deleting pulses at the 32.768 kHz level. These correction pulses are spaced evenly over a sufficiently long period of time to reach the required resolution and accuracy. Every second corrections with a resolution of about 30.5 ppm (1/32768) can be generated by the temperature compensation engine. If for instance a 10 ppm correction is called for, the correction pulses will be generated approximately once every 3 seconds, for a 50 ppm correction every 0.6 s and so on.

The 1 Hz interrupt output signal can be measured with a counter and by selecting an appropriate gating time the measurement resolution can be set to the desired level. A gating time of 100 s for instance will determine the averaged 1 second period with a resolution of 0.3 ppm.

The feature of temperature compensation can be turned off for ultra low power consumption by first performing a software reset (SR) followed by setting TC_DIS to ‘1’ within 5 seconds.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7.3.1.1 Temperature measurement

The PCF2131 has a temperature sensor circuit used to perform temperature compensation of the clock input to the RTC. The temperature is measured immediately after power-on and then periodically with a period set by the temperature conversion rate TCR[1:0] in the register CLKOUT_ctl. During the first approximately 60 s after start-up the compensation will be inactive, after this period the temperature compensation is active.

Table 17. Temperature measurement period

TCR[1:0]		Temperature measurement period
00	[1]	32 min
01		16 min
10		8 min
11		4 min

[1] Default value.

7.3.2 OTP refresh

Each IC is calibrated during production and testing of the device. The calibration parameters are stored on EPROM cells called One Time Programmable (OTP) cells. It is recommended to process an OTP refresh once after the power is up and the oscillator is operating stable. The OTP refresh takes less than 100 ms to complete.

To perform an OTP refresh, bit OTPR has to be cleared (set to logic 0) and then set to logic 1 again.

When read OTPR bit, its state is:

"0" until the OTP read state machine completes copying of the eFuse data into the shadow registers. This could be due to a POR event or to writing a 0 > 1 to the OTPR register bit.

"1" when the OTP read state machine completes copying to the shadow registers from the eFuse instances. During normal operation OTPR must be kept at 1 to prevent higher power usage.

The OTP logic is not reset nor affected by the Software Reset. The OTPR functionality is only reset by the initial digital POR.

During OTP refresh, V_{DD} has to be above 1.8 V, the rising speed to 1.8 V needs to be faster than 2 V/100 ms. After OTP refresh has finished, PCF2131 can operate with V_{DD} as low as 1.2 V.

7.3.3 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] control bits in register CLKOUT_ctl. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as system clock, microcontroller clock, charge pump input, or for calibrating the oscillator at 25 °C to determine aging offset. The CLKOUT output is not temperature compensated to prevent jitter due to digital compensation method.

CLKOUT is a push-pull output and is enabled at power-on. When disabled, the output is high-impedance.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 18. CLKOUT frequency selection

COF[2:0]		CLKOUT frequency (Hz)	Typical duty cycle [1]
000	[2]	32 768	60 : 40 to 40 : 60
001		16 384	50 : 50
010		8 192	50 : 50
011		4 096	50 : 50
100		2 048	50 : 50
101		1 024	50 : 50
110		1	50 : 50
111		CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time: % LOW-level time.
[2] Default value.

The duty cycle of the selected clock is not controlled, however, due to the nature of the clock generation all but the 32.768 kHz frequencies are 50 : 50.

7.4 Register Aging_offset

Table 19. Aging_offset - crystal aging offset register (address 30h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	T	AO[3:0]			
Reset value	0	0	0	0	1	0	0	0

Table 20. Aging_offset - crystal aging offset register (address 30h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 4	T	0000	unused
3 to 0	AO[3:0]	see Table 21	aging offset value

7.4.1 Crystal aging correction

The PCF2131 has an offset register Aging_offset to correct the crystal aging effects [1].

The accuracy of the frequency of a quartz crystal depends on its aging. The aging offset adds an adjustment, positive or negative, in the temperature compensation circuit which allows correcting the aging effect.

The aging offset bits allow a frequency correction of typically 2 ppm per AO[3:0] value, from -14 ppm to +16 ppm.

1 For further information, refer to the application note [1].

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 21. Frequency correction at 25 °C, typical

AO[3:0]			ppm
Decimal	Binary		
0	0000		+16
1	0001		+14
2	0010		+12
3	0011		+10
4	0100		+8
5	0101		+6
6	0110		+4
7	0111		+2
8	1000	[1]	0
9	1001		-2
10	1010		-4
11	1011		-6
12	1100		-8
13	1101		-10
14	1110		-12
15	1111		-14

[1] Default value.

7.5 Power management functions

The PCF2131 has two power supplies:

V_{DD} - the main power supply

V_{BAT} - the battery backup supply

Internally, PCF2131 operates with the internal operating voltage $V_{oper(int)}$ which is also available as V_{BBS} on the battery backed output voltage pin, BBS. Depending on the condition of the main power supply and the selected power management function, $V_{oper(int)}$ is either on the potential of V_{DD} or V_{BAT}.

Two power management functions are implemented:

Battery switch-over function - monitors the main power supply V_{DD} and switching to V_{BAT} in case a power fail condition is detected (see Section 7.5.1).

Battery low detection function - monitors the status of the battery, V_{BAT} (see Section 7.5.2).

The power management functions are controlled by the control bits PWRMNG[2:0] (see Table 22) in register Control_3 (see Table 10):

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 22. Power management control bit description

PWRMNG[2:0]		Function
000		battery switch-over function is enabled in standard mode; battery low detection function is enabled
001,010		battery switch-over function is enabled in standard mode; battery low detection function is disabled
011		battery switch-over function is enabled in direct switching mode; battery low detection function is enabled
100,101		battery switch-over function is enabled in direct switching mode; battery low detection function is disabled
110,111	[1] [2]	battery switch-over function is disabled, only one power supply (V_{DD}); battery low detection function is disabled

[1] Default value.
[2] When the battery switch-over function is disabled, the device works only with the power supply V_{DD}. V_{BAT} must be put to ground and the battery low detection function is disabled.

7.5.1 Battery switch-over function

PCF2131 has a backup battery switch-over circuit which monitors the main power supply V_{DD}. When a power failure condition is detected, it automatically switches to the backup battery.

One of two operation modes can be selected:

Standard mode - the power failure condition happens when:

$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$

$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V. The battery switch-over in standard mode works only for $V_{DD} > 2.5$ V. Applying back-up battery voltage to V_{BAT} without applying V_{DD} supply will not power on the device; only when V_{DD} main power is supplied the device will start operating.

Direct switching mode - the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BF (register Control_3) is set to logic 1.
2. An interrupt is generated if the control bit BIE (register Control_3) is enabled (see Section 7.13.6).
3. If the control bit BTSE (register Control_3) is logic 1, the timestamp 4 registers store the time and date when the battery switch occurred (see Section 7.12.4).
4. The battery switch flag BF is cleared by command; it must be cleared to clear the interrupt.

The interface and CLKOUT output are disabled in battery backup operation:

- Interface inputs are not recognized, preventing extraneous data being written to the device
- Interface outputs are high-impedance

All information provided in this document is subject to legal disclaimers.

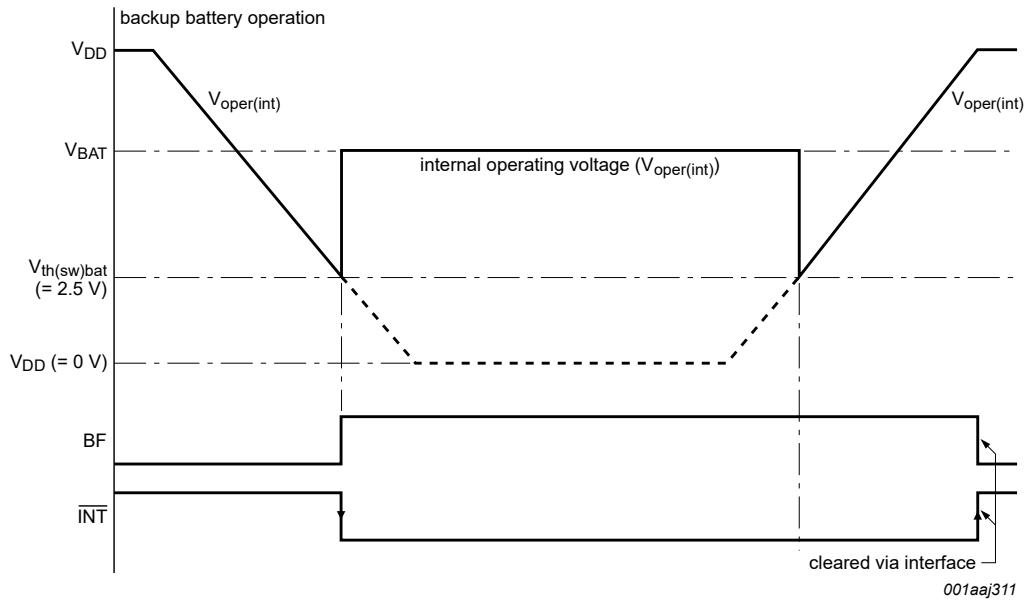
© NXP B.V. 2021. All rights reserved.

For further information about I^2C-bus communication and battery backup operation, see Section 7.16.3.

7.5.1.1 Standard mode

If $V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$: $V_{oper(int)}$ is at V_{DD} potential.

If $V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$: $V_{oper(int)}$ is at V_{BAT} potential.



$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5 V. In standard mode, the battery switch-over works only for $V_{DD} > 2.5$ V.

V_{DD} may be lower than V_{BAT} (for example V_{DD} = 3 V, V_{BAT} = 4.1 V).

Figure 4. Battery switch-over behavior in standard mode with bit BIE set logic 1 (enabled)

7.5.1.2 Direct switching mode

If $V_{DD} > V_{BAT}$: $V_{oper(int)}$ is at V_{DD} potential.

If $V_{DD} < V_{BAT}$: $V_{oper(int)}$ is at V_{BAT} potential.

The direct switching mode is useful in systems where V_{DD} is always higher than V_{BAT}. This mode is not recommended if the V_{DD} and V_{BAT} values are similar (for example, V_{DD} = 3.3 V, $V_{BAT} \geq 3.0$ V). In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

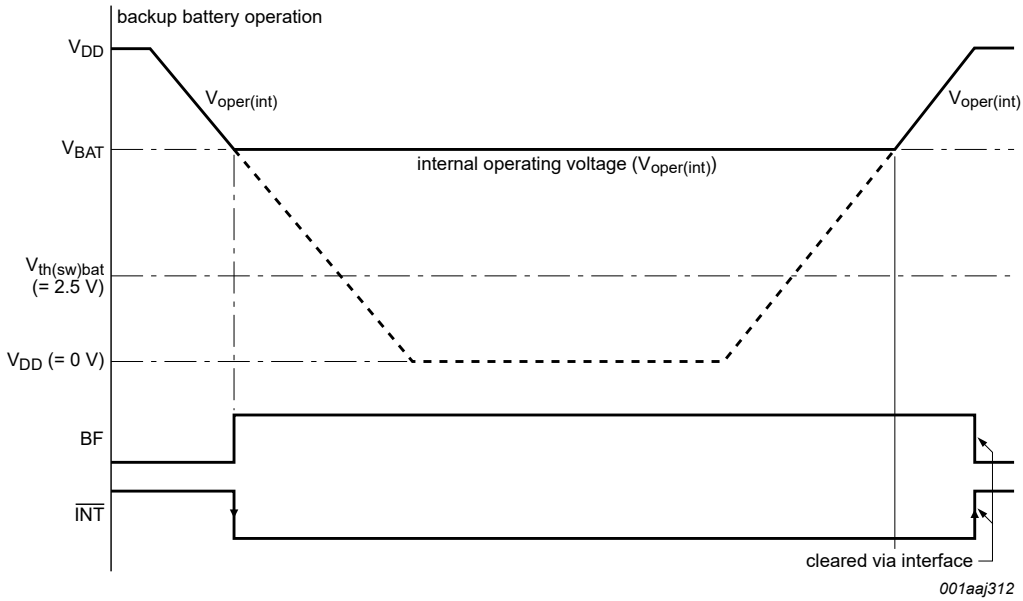


Figure 5. Battery switch-over behavior in direct switching mode with bit BIE set logic 1 (enabled)

7.5.1.3 Battery switch-over disabled: only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin
- The V_{BAT} pin must be connected to ground
- $V_{oper(int)}$ is at V_{DD} potential
- The battery flag (BF) is always logic 0

7.5.1.4 Battery switch-over architecture

The architecture of the battery switch-over circuit is shown in Figure 6.

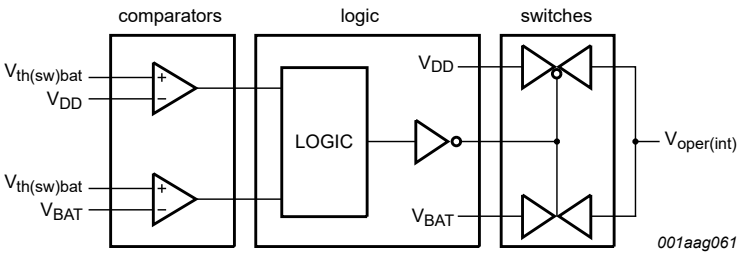


Figure 6. Battery switch-over circuit, simplified block diagram

$V_{oper(int)}$ is at V_{DD} or V_{BAT} potential.

Remark: It has to be assured that there are decoupling capacitors on the pins V_{DD}, V_{BAT}, and BBS.

7.5.2 Battery low detection function

The PCF2131 has a battery low detection circuit which monitors the status of the battery V_{BAT}.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

When V_{BAT} drops below the threshold value $V_{th(bat)low}$ (typical 2.5 V), the BLF flag (register Control_3) is set to indicate that the battery is low and that it must be replaced. Monitoring of the battery voltage also occurs during battery operation.

An unreliable battery cannot prevent the supply voltage from dropping below V_{low} (typical 1.2 V) and with that the data integrity gets lost. (For further information about V_{low} see Section 7.6.)

When V_{BAT} drops below the threshold value $V_{th(bat)low}$, the following sequence occurs (see Figure 7):

1. The battery low flag BLF is set logic 1.
2. An interrupt is generated if the control bit BLIE (register Control_3) is enabled (see Section 7.13.7).
3. The flag BLF remains logic 1 until the battery is replaced. BLF cannot be cleared by command. It is automatically cleared by the battery low detection circuit when the battery is replaced or when the voltage rises again above the threshold value. This could happen if a super capacitor is used as a backup source and the main power is applied again.

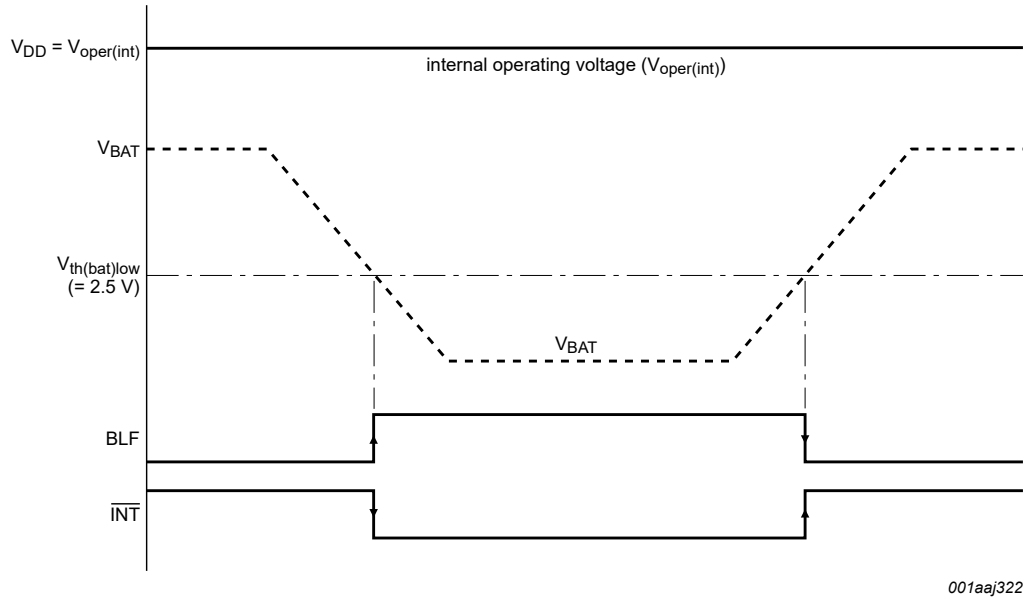


Figure 7. Battery low detection behavior with bit BLIE set logic 1 (enabled)

7.5.3 Battery backup supply

The V_{BBS} voltage on the output pin BBS is at the same potential as the internal operating voltage $V_{oper(int)}$, depending on the selected battery switch-over function mode:

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 23. Output pin BBS

Battery switch-over function mode	Conditions	Potential of $V_{oper(int)}$ and V_{BBS}
standard	$V_{DD} > V_{BAT}$ OR $V_{DD} > V_{th(sw)bat}$	V_{DD}
	$V_{DD} < V_{BAT}$ AND $V_{DD} < V_{th(sw)bat}$	V_{BAT}
direct switching	$V_{DD} > V_{BAT}$	V_{DD}
	$V_{DD} < V_{BAT}$	V_{BAT}
disabled	only V_{DD} available, V_{BAT} must be put to ground	V_{DD}

The output pin BBS can be used as a supply for external devices with battery backup needs, such as SRAM (see [1]).

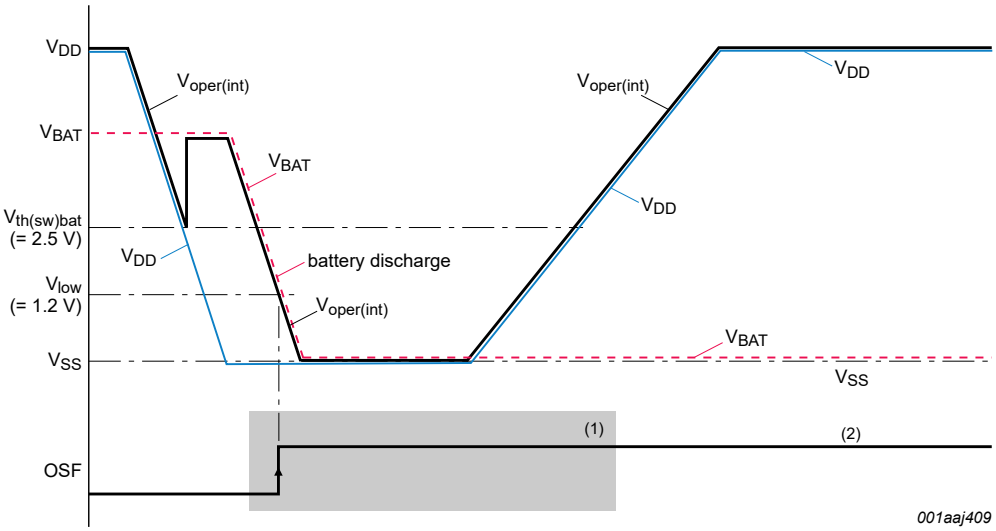
7.6 Oscillator stop detection function

The PCF2131 has an on-chip oscillator detection circuit which indicates the status of the oscillation by monitoring the supply of oscillator: whenever the supply is out of the expected range, a reset occurs and the oscillator stop flag OSF (in register Seconds) is set logic 1.

- **Power-on:**
  1. The oscillator is not running, the chip is in reset (OSF is logic 1).
  2. When the oscillator starts running and supply is OK after power-on, the chip exits from reset.
  3. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.
- **Power supply failure:**
  1. When the power supply of the chip drops below a certain value (V_{low}), typically 1.2 V, the oscillator supply also fails and a reset occurs.
  2. When the power supply returns to normal operation, the oscillator supply is OK again, the chip exits from reset.
  3. The flag OSF is still logic 1 and can be cleared (OSF set logic 0) by command.
  4. When OSF flag is cleared an OTP refresh should be performed (see Section 7.3.2).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.



1. Theoretical state of the signals since there is no power.
2. The oscillator stop flag (OSF), set logic 1, indicates that the oscillation has stopped and a reset has occurred since the flag was last cleared (OSF set logic 0). In this case, the integrity of the clock information is not guaranteed. The OSF flag is cleared by command.

Figure 8. Power failure event due to battery discharge: reset occurs

7.7 Power-On Reset function

The PCF2131 has a Power-On Reset (POR) and a Power-On Reset Override (PORO) function implemented.

7.7.1 Power-On Reset (POR)

The POR is active whenever the oscillator is stopped. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance (see Figure 9). This time may be in the range of 200 ms to 2 s depending on temperature and supply voltage. Whenever an internal reset occurs, the oscillator stop flag is set (OSF set logic 1).

The OTP refresh (see Section 7.3.2) should ideally be executed as the first instruction after start-up and also after a reset due to an oscillator stop.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

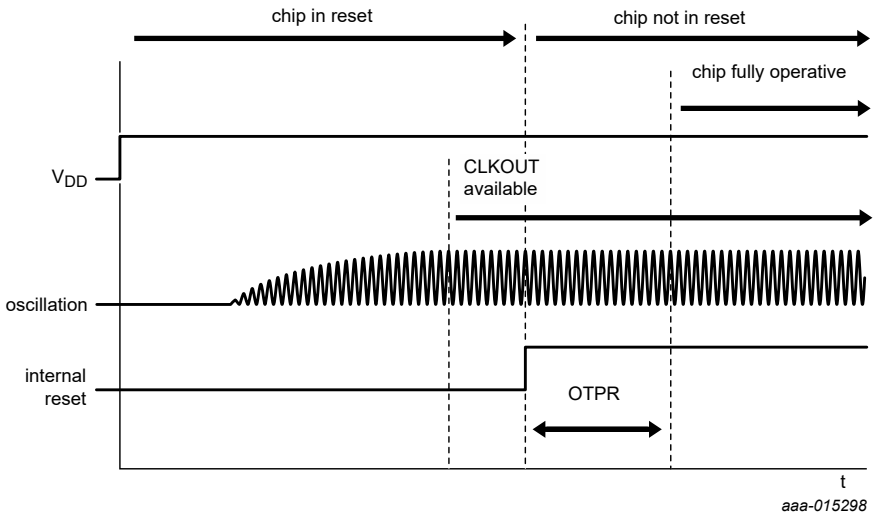


Figure 9. Dependency between POR and oscillator

After POR, the following mode is entered:

- 32.768 kHz CLKOUT active
- Power-On Reset Override (PORO) available to be set
- 24-hour mode is selected
- Battery switch-over function disabled, only one power supply (V_{DD})
- Temperature compensation enabled
- 100th second enabled
- Time 00:00:00.00
- Date 2001.01.01
- Weekday Monday

The register values after power-on are shown in Table 4.

7.7.2 Power-On Reset Override (PORO)

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and therefore speed up the on-board test of the device.

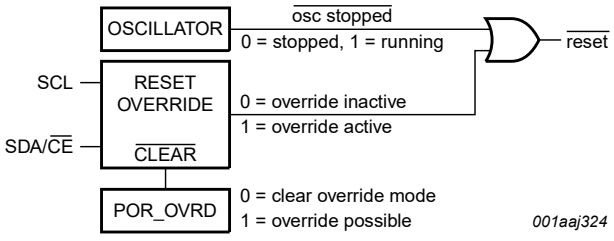


Figure 10. Power-On Reset (POR) system

The setting of the PORO mode requires that POR_OVRD in register Control_1 is set logic 1 and that the signals at the interface pins SDA/$\overline{CE}$ and SCL are toggled as illustrated in Figure 11. All timings shown are required minimum.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

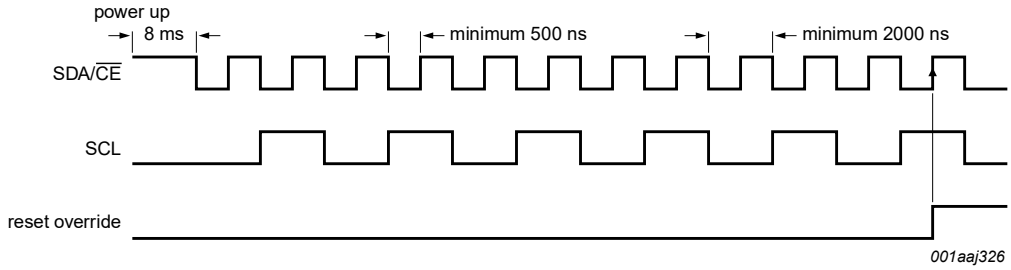


Figure 11. Power-On Reset Override (PORO) sequence, valid for both I²C-bus and SPI-bus

Once the override mode is entered, the device is immediately released from the reset state and the set-up operation can commence.

The PORO mode is cleared by writing logic 0 to POR_OVRD. POR_OVRD must be logic 1 before a re-entry into the override mode is possible. Setting POR_OVRD logic 0 during normal operation has no effect except to prevent accidental entry into the PORO mode.

7.8 Software Reset register

Table 24. Reset - software reset control (address 05h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	CPR	0	1	0	SR	1	0	CTS
Section	Section 7.8.2				Section 7.8.1			Section 7.8.3

To

- trigger a software reset (SR), 0010 1100 (2Ch) must be sent to register Reset (address 05h). A software reset also triggers CPR and CTS
- clear prescaler (CPR), 1010 0100 (A4h) must be sent to register Reset (address 05h)
- clear timestamp (CTS), 0010 0101 (25h) must be sent to register Reset (address 05h)

It is possible to combine CPR and CTS by sending 1010 0101 (A5h).

Read of the SR_RESET register will return a fixed pattern of 00100100;

Remark: Any other value sent to this register is ignored.

7.8.1 SR - Software reset

A reset is automatically generated at power-on as Power-On Reset as described in Section 7.7. A reset can also be initiated with the software reset command.

After software reset, the following mode is entered:

- 32.768 kHz CLKOUT active
- Power-On Reset Override (PORO) unchanged
- OTP not reloaded, OTPR unchanged.
- 24-hour mode is selected
- Battery switch-over function disabled, only one power supply (V_{DD})
- Temperature compensation enabled
- 100th second enabled
- Time 00:00:00.00
- Date 2001.01.01

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

- Weekday Monday

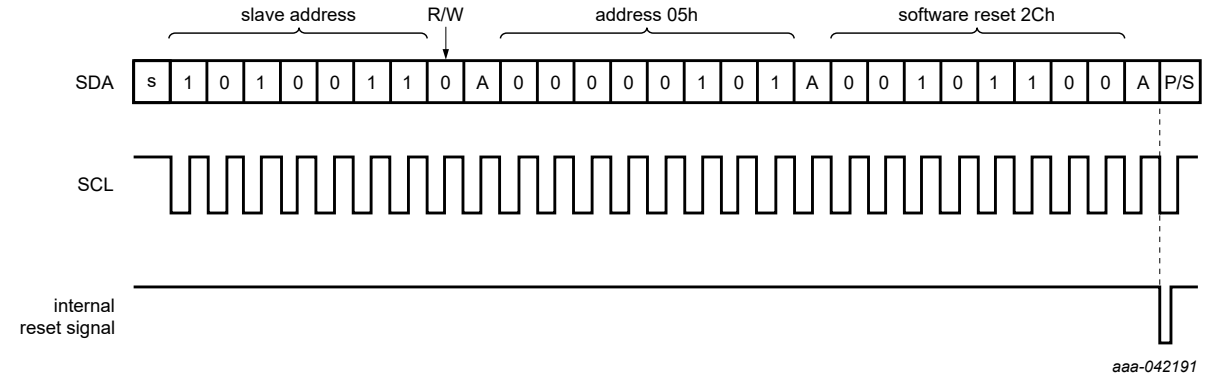


Figure 12. Software reset command

7.8.2 CPR: clear prescaler

To set the time for RTC mode, the clear prescaler instruction is needed.

Before sending this instruction, it is mandatory to first set *stop* by the STOP bit.

See STOP definition for an explanation on using this instruction.

7.8.3 CTS: clear timestamp

The timestamp registers (address 14h to 2Fh) can be set to all 0 with this instruction.

7.9 Time and date function

Most of these registers are coded in the Binary Coded Decimal (BCD) format.

7.9.1 Register 100th Seconds

Table 25. 100th Seconds - 100th seconds (address 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	100TH SECONDS (0 to 99)							
Reset value	0	0	0	0	0	0	0	0

Table 26. 100th Seconds - 100th seconds register (address 06h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	100TH SECONDS	0 to 9	ten's place	actual seconds coded in BCD format
3 to 0		0 to 9	unit place	

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 27. 100th Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)				Digit (unit place)			
	Bit 6	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
98	1	0	0	1	1	0	0	0
99	1	0	0	1	1	0	0	1

7.9.2 Register Seconds

Table 28. Seconds - seconds and clock integrity register (address 07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OSF	SECONDS (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

Table 29. Seconds - seconds and clock integrity register (address 07h) bit description

Bit	Symbol	Value	Place value	Description
7	OSF	0	-	clock integrity is guaranteed
		1	-	clock integrity is not guaranteed: oscillator has stopped and chip reset has occurred since flag was last cleared
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format
3 to 0		0 to 9	unit place	

Table 30. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 30. Seconds coded in BCD format*...continued*

Seconds value in decimal	Upper-digit (ten's place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

7.9.3 Register Minutes

Table 31. Minutes - minutes register (address 08h) bit allocation

Bits labeled as T are unused and return 0 when read

Bit	7	6	5	4	3	2	1	0
Symbol	T	MINUTES (0 to 59)						
Reset value	0	0	0	0	0	0	0	0

Table 32. Minutes - minutes register (address 08h) bit description

Bits labeled as T are unused and return 0 when read

Bit	Symbol	Value	Place value	Description
7	T	0	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

7.9.4 Register Hours

Table 33. Hours - hours register (address 09h) bit allocation

Bits labeled as T are unused and return 0 when read

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	AMPM	HOURS (1 to 12) in 12-hour mode				
			HOURS (0 0to 23) in 24-hour mode					
Reset value	0	0	0	0	0	0	0	0

Table 34. Hours - hours register (address 09h) bit description

Bits labeled as T are unused and return 0 when read

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	unused
12-hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 34. Hours - hours register (address 09h) bit description...*continued*

Bits labeled as T are unused and return 0 when read

Bit	Symbol	Value	Place value	Description
4	HOURS	0 to 1	ten's place	actual hours coded in BCD format when in 12-hour mode
3 to 0		0 to 9	unit place	
24-hour mode[1]				
5 to 4	HOURS	0 to 2	ten's place	actual hours coded in BCD format when in 24-hour mode
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1 (see Table 6).

7.9.5 Register Days

Table 35. Days - days register (address 0Ah) bit allocation

Bits labeled as T are unused and return 0 when read

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	DAYS (1 to 31)					
Reset value	0	0	0	0	0	0	0	0

Table 36. Days - days register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] If the year counter contains a value which is exactly divisible by 4, excluding the year 00, the RTC compensates for leap years by adding a 29th day to February. Note that next time the year will roll over to 00 will be year 2100, which is not going to be leap year.

7.9.6 Register Weekdays

Table 37. Weekdays - weekdays register (address 0Bh) bit allocation

Bits labeled as T are unused and return 0 when read

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	T	T	WEEKDAYS (0 to 6)		
Reset value	0	0	0	0	0	0	0	1

Table 38. Weekdays - weekdays register (address 0Bh) bit description

Bits labeled as T are unused and return 0 when read

Bit	Symbol	Value	Description
7 to 3	T	000	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday value, see Table 39

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Although the association of the weekdays counter to the actual weekday is arbitrary, the PCF2131 assumes that Sunday is 000 and Monday is 001 for the purpose of determining the increment for calendar weeks.

Table 39. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be reassigned by the user.

7.9.7 Register Months

Table 40. Months - months register (address 0Ch) bit allocation

Bits labeled as T are unused and return 0 when read

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	MONTHS (1 to 12)				
Reset value	0	0	0	0	0	0	0	1

Table 41. Months - months register (address 0Ch) bit description

Bits labeled as T are unused and return 0 when read

Bit	Symbol	Value	Place value	Description
7 to 5	T	000	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format, see Table 42
3 to 0		0 to 9	unit place	

Table 42. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 42. Month assignments in BCD format...*continued*

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

7.9.8 Register Years

Table 43. Years - years register (address 0Dh) bit allocation

Bits labeled as T are unused and return 0 when read

Bit	7	6	5	4	3	2	1	0
Symbol	YEARS (0 to 99)							
Reset value	0	0	0	0	0	0	0	1

Table 44. Years - years register (address 0Dh) bit description

Bits labeled as T are unused and return 0 when read

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

7.9.9 Setting and reading the time

Figure 13 shows the data flow and data dependencies starting from the 100 Hz/1 Hz clock tick.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

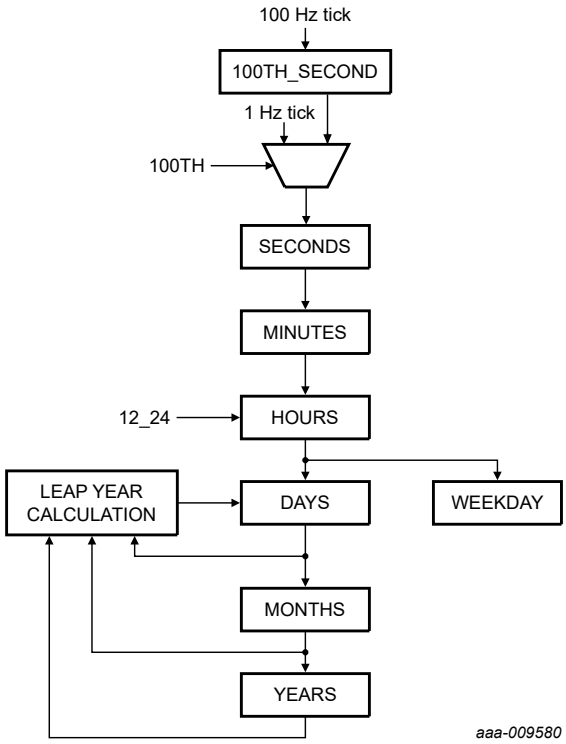


Figure 13. Data flow for the time function

Write access requires setting the STOP bit. The flow for accurately setting the time in RTC mode is:

- start an I2C access at register control_1
- set STOP bit
- set CPR (register SR_RESET, CPR is logic 1)
- address counter rolls over to address 06h
- set time (100th seconds, seconds to years)
- end I2C access
- wait for external time reference to indicate that time counting should start
- start an I2C access at register control_1
- clear STOP bit (time starts counting from now)
- end I2C access

The first increment of the time circuits is between 0 s and 122 ms after STOP is released. See description for STOP bit in Section 7.15

During read operations, the time counting circuits (memory locations 06h through 0Dh) are blocked. This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read access is completed, the time circuit is released again. Any pending request to increment the time counters that occurred during the read access is serviced.

As a consequence of this method, it is very important to make a read access in one go. That is, reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

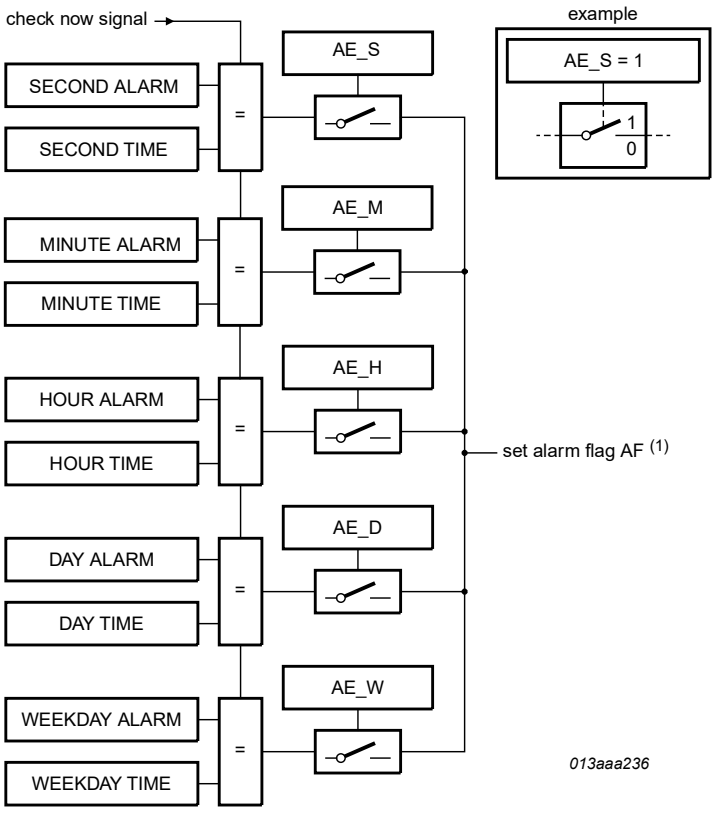
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

As an example, a roll-over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore it is advised to read all time and date registers in one access.

7.10 Alarm function

When one or more of the alarm bit fields are loaded with a valid second, minute, hour, day, or weekday and its corresponding alarm enable bit (AE_x) is logic 0, then that information is compared with the actual second, minute, hour, day, and weekday (see Figure 14).



1. Only when all enabled alarm settings are matching.

Figure 14. Alarm function block diagram

The generation of interrupts from the alarm function is described in Section 7.13.4.

7.10.1 Register Second_alarm

Table 45. Second_alarm - second alarm register (address 0Eh) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_S	SECOND_ALARM (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 46. Second_alarm - second alarm register (address 0Eh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_S	0	-	second alarm is enabled
		1	-	second alarm is disabled
6 to 4	SECOND_ALARM	0 to 5	ten's place	second alarm information coded in BCD format
3 to 0		0 to 9	unit place	

7.10.2 Register Minute_alarm

Table 47. Minute_alarm - minute alarm register (address 0Fh) bit allocation

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_M	MINUTE_ALARM (0 to 59)						
Reset value	1	0	0	0	0	0	0	0

Table 48. Minute_alarm - minute alarm register (address 0Fh) bit description

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_M	0	-	minute alarm is enabled
		1	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

7.10.3 Register Hour_alarm

Table 49. Hour_alarm - hour alarm register (address 10h) bit allocation

Bits labeled as T are unused and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_H	T	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
			HOUR_ALARM (0 to 23) in 24-hour mode					
Reset value	1	0	0	0	0	0	0	0

Table 50. Hour_alarm - hour alarm register (address 10h) bit description

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_H	0	-	hour alarm is enabled
		1	-	hour alarm is disabled

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 50. Hour_alarm - hour alarm register (address 10h) bit description*...continued*

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
6	T	0	-	unused
12-hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_ALARM	0 to 1	ten's place	hour alarm information coded in BCD format when in 12-hour mode
3 to 0		0 to 9	unit place	
24-hour mode[1]				
5 to 4	HOUR_ALARM	0 to 2	ten's place	hour alarm information coded in BCD format when in 24-hour mode
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1.

7.10.4 Register Day_alarm

Table 51. Day_alarm - day alarm register (address 11h) bit allocation

Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_D	T	DAY_ALARM (1 to 31)					
Reset value	1	0	0	0	0	0	0	0

Table 52. Day_alarm - day alarm register (address 11h) bit description

Bits labeled as T are unused and return 0 when readBits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Place value	Description
7	AE_D	0	-	day alarm is enabled
		1	-	day alarm is disabled
6	T	0	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7.10.5 Register Weekday_alarm

Table 53. Weekday_alarm - weekday alarm register (address 12h) bit allocation

Bits labeled as T are unused and return 0 when read.Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	7	6	5	4	3	2	1	0
Symbol	AE_W	T	T	T	T	WEEKDAY_ALARM (0 to 6)		
Reset value	1	0	0	0	0	0	0	0

Table 54. Weekday_alarm - weekday alarm register (address 12h) bit description

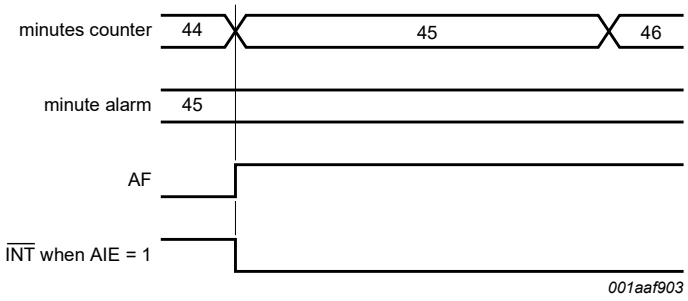
Bit positions labeled as - are not implemented and return 0 when read. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7	AE_W	0	weekday alarm is enabled
		1	weekday alarm is disabled
6 to 3	T	0	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information

7.10.6 Alarm flag

When all enabled comparisons first match, the alarm flag AF (register Control_2) is set. AF remains set until cleared by command. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. For clearing the flags, see Section 7.11.5

Alarm registers which have their alarm enable bit AE_x at logic 1 are ignored.



Example where only the minute alarm is used and no other interrupts are enabled.

Figure 15. Alarm flag timing diagram

7.11 Watchdog timer functions

The PCF2131 has a watchdog timer function. The timer can be switched on and off by using the control bit WD_CD in the register Watchdg_tim_ctl.

The watchdog timer has four selectable source clocks. It can, for example, be used to detect a micro-controller with interrupt and reset capability which is out of control (see Section 7.11.3)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

To control the timer function and timer output, the registers Control_2, Watchdg_tim_ctl, and Watchdg_tim_val are used.

7.11.1 Register Watchdg_tim_ctl

Table 55. Watchdg_tim_ctl - watchdog timer control register (address 35h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	WD_CD	T	TI_TP	T	T	T	TF[1:0]	
Reset value	0	0	0	0	0	0	1	1

Table 56. Watchdg_tim_ctl - watchdog timer control register (address 35h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7	WD_CD	0	watchdog timer interrupt disabled
		1	watchdog timer interrupt enabled; the interrupt pin $\overline{\text{INTA/B}}$ is activated when timed out
6	T	0	unused
5	TI_TP	0	the interrupt pin $\overline{\text{INTA/B}}$ is configured to generate a permanent active signal when MSF is set
		1	the interrupt pin $\overline{\text{INTA/B}}$ is configured to generate a pulsed signal when MSF flag is set (see Figure 17)
4 to 2	T	000	unused
1 to 0	TF[1:0]		timer source clock for watchdog timer
		00	64 Hz
		01	4 Hz
		10	$^1/_4$ Hz
		11	$^1/_{64}$ Hz

7.11.2 Register Watchdg_tim_val

Table 57. Watchdg_tim_val - watchdog timer value register (address 36h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WATCHDG_TIM_VAL[7:0]							
Reset value	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 58. Watchdg_tim_val - watchdog timer value register (address 36h) bit description

Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Bit	Symbol	Value	Description
7 to 0	WATCHDG_TIM_ VAL[7:0]	00 to FF	timer period in seconds: $TimerPeriod = \frac{(n-1)+/-0.5}{SourceClockFrequency}$ where n is the timer value (n > 1) Write Only

Table 59. Programmable watchdog timer

TF[1:0]	Timer source clock frequency	Units	Minimum timer period (n = 2)	Units	Maximum timer period (n = 255)	Units
00	64	Hz	15.625	ms	3.984	s
01	4	Hz	250	ms	63.744	s
10	$^1/_4$	Hz	4	s	1020	s
11	$^1/_{64}$	Hz	64	s	16320	s

7.11.3 Watchdog timer function

The watchdog timer interrupt function is enabled or disabled by the WD_CD bit of the register Watchdg_tim_ctl (see Table 56).

The 2 bits TF[1:0] in register Watchdg_tim_ctl determine one of the four source clock frequencies for the watchdog timer: 64 Hz, 4 Hz, $^1/_4$ Hz or $^1/_{64}$ Hz (see Table 59).

When the watchdog timer function is enabled, the 8-bit timer in register Watchdg_tim_val determines the watchdog timer period (see Table 59).

The watchdog timer counts down from the software programmed 8-bit binary value n in register Watchdg_tim_val. When the counter reaches 1, the watchdog timer flag WDTF (register Control_2) is set logic 1 and an interrupt is generated. The period accuracy corresponds to n +/- 0.5.

The register Watchdg_tim_val is write only and not readable after set.

The counter does not automatically reload.

When WD_CD is logic 1/0 (watchdog timer interrupt enabled/disabled) and the Micro-controller Unit (MCU) loads a watchdog timer value n:

- the flag WDTF is reset
- $\overline{\text{INTA/B}}$ is cleared
- the watchdog timer starts again

Loading the counter with 0 or 1 will:

- reset the flag WDTF
- clear $\overline{\text{INTA/B}}$
- stop the watchdog timer

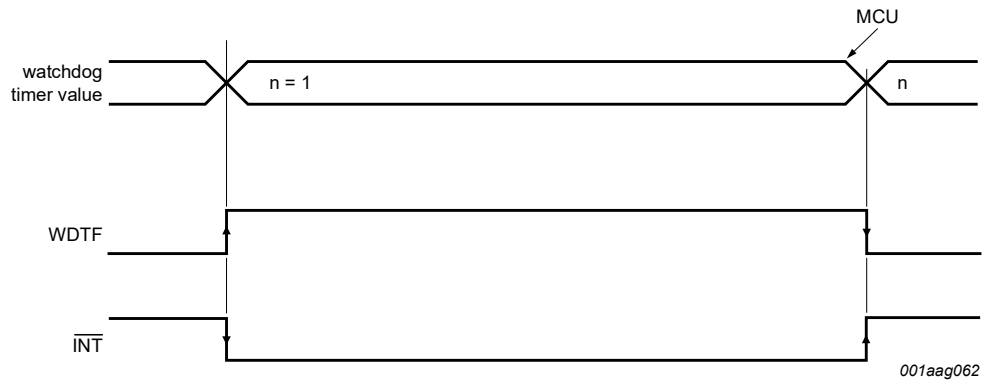
Remark: WDTF can be cleared by:

- loading a value in register Watchdg_tim_val
- writing a logic 0 to WDTF

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Writing a logic 1 to WDTF has no effect.



Counter reached 1, WDTF is logic 1, and an interrupt is generated.

Figure 16. WD_CD set logic 1: watchdog activates an interrupt when timed out

- When the watchdog timer counter reaches 1, the watchdog timer flag WDTF is set logic 1
- When a minute or second interrupt occurs, the minute/second flag MSF is set logic 1 (see Section 7.13.1).

7.11.4 Pre-defined timers: second and minute interrupt

PCF2131 has two pre-defined timers which are used to generate an interrupt either once per second or once per minute (see Section 7.13.1). The pulse generator for the minute or second interrupt operates from an internal 64 Hz clock. It is independent of the watchdog timer. Each of these timers can be enabled by the bits SI (second interrupt) and MI (minute interrupt) in register Control_1.

7.11.5 Clearing flags

The flags MSF and AF can be cleared by command. To prevent one flag being overwritten while clearing another, a logic AND is performed during the write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Two examples are given for clearing the flags. Clearing a flag is made by a write command:

- Bits labeled with - must be written with their previous values
- Bits labeled with T have to be written with logic 0
- WDTF is read only and has to be written with logic 0

Repeatedly rewriting these bits has no influence on the functional behavior.

Table 60. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	MSF	WDTF	T	AF	T	-	-	T

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 61. Example values in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	1	0	0	0	0

The following tables show what instruction must be sent to clear the appropriate flag.

Table 62. Example to clear only AF (bit 4)

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	1	0	1	0	0	0[1]	0[1]	0

[1] The bits labeled as - have to be rewritten with the previous values.

Table 63. Example to clear only MSF (bit 7)

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	0	0	1	1	0	0[1]	0[1]	0

[1] The bits labeled as - have to be rewritten with the previous values.

7.12 Timestamp function

The PCF2131 has four active LOW timestamp input pins $\overline{TS1}$, $\overline{TS2}$, $\overline{TS3}$ and $\overline{TS4}$, internally pulled with on-chip pull-up resistors to $V_{oper(int)}$. It also has a timestamp detection circuit which can detect the event when inputs on pin $\overline{TS1/2/3/4}$ are driven to ground.

The timestamp function is enabled by default after power-on and it can be switched off by setting the control bit TSOFF (register Timestp_ctl1/2/3/4).

The time recorded in the time stamps, when in 100 Hz disable mode (1 Hz mode), will be at least two 16 Hz clocks behind the timestamp event and no more than 3 clocks behind. If the exact time of the timestamp event is required then subtract 2 subseconds from the timestamp value and the result will have -0 subseconds to +1 subseconds of uncertainty.

A most common application of the timestamp function is described in [1].

See Section 7.13.5 for a description of interrupt generation from the timestamp function.

7.12.1 Timestamp flag

1. When the $\overline{TS1/2/3/4}$ input pin are driven to ground, the following sequence occurs:
   a. The actual date and time are stored in the timestamp registers.
   b. The timestamp flag TSF1/2/3/4 flag is set.
   c. If the TSIE1/2/3/4 bit is active, and corresponding interrupt mask is disabled, an interrupt on the $\overline{INTA/B}$ pin is generated.

The TSF1/2/3/4 and TSF1/2/3/4_2 flags can be cleared by command; clearing the flag clears the interrupt. Once TSF1/2/3/4 is cleared, it will only be set again when $\overline{TS1/2/3/4}$ pin is driven to ground once again.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7.12.2 Timestamp mode

The timestamp function has two different modes selected by the control bit TSM (timestamp mode) in register Timestp_ctl:

- If TSM is logic 0 (default): in subsequent trigger events without clearing the timestamp flags, the last timestamp event is stored
- If TSM is logic 1: in subsequent trigger events without clearing the timestamp flags, the first timestamp event is stored

The timestamp function also depends on the control bit BTSE in register Control_3, see Section 7.12.4.

7.12.3 Timestamp registers

7.12.3.1 Register Timestp_ctl1/2/3/4

Table 64. Timestp_ctl1/2/3/4 - timestamp control register (address 14h/1Bh/22h/29h) bit allocation

Bits labeled as T are unused and return 0 when read

Bit	7	6	5	4	3	2	1	0
Symbol	TSM	TSOFF	T	SUBSEC_TIMESTP[4:0]				
Reset value	0	0	0	0	0	0	0	0

Table 65. Timestp_ctl1/2/3/4 - timestamp control register (address 14h/1Bh/22h/29h) bit description

Bits labeled as T are unused and return 0 when read

Bit	Symbol	Value	Description
7	TSM	0	in subsequent events without clearing the timestamp flags, the last event is stored
		1	in subsequent events without clearing the timestamp flags, the first event is stored
6	TSOFF	0	timestamp function active
		1	timestamp function disabled
5	-	-	unused
4 to 0	SUBSEC_TIMESTP[4:0]		$^{1}/_{16}$ second timestamp information coded in BCD format when 100TH_S_DIS = '1'[1], $^{1}/_{20}$ second timestamp information coded in BCD format when 100TH_S_DIS = '0';

[1] The time recorded in the time stamps, when in 100 Hz disable mode (1 Hz mode), will be at least two 16 Hz clocks behind the timestamp event and no more than 3 clocks behind. If the exact time of the timestamp event is required then subtract 2 subseconds from the timestamp value and the result will have -0 subseconds to +1 subseconds of uncertainty.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7.12.3.2 Register Sec_timestp

Table 66. Sec_timestp1/2/3/4 - second timestamp register (address 15h/1Ch/23h/2Ah) bit allocation
Bits labeled as T are unused and return 0 when read

Bit	7	6	5	4	3	2	1	0
Symbol	T	SECOND_TIMESTP (0 to 59)						
Reset value	0	0	0	0	0	0	0	0

Table 67. Sec_timestp1/2/3/4 - second timestamp register (address 15h/1Ch/23h/2Ah) bit description
Bits labeled as T are unused and return 0 when read

Bit	Symbol	Value	Place value	Description
7	T	0	-	unused
6 to 4	SECOND_TIMESTP	0 to 5	ten's place	second timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.12.3.3 Register Min_timestp

Table 68. Min_timestp1/2/3/4 - minute timestamp register (address 16h/1Dh/24h/2Bh) bit allocation
Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	MINUTE_TIMESTP (0 to 59)						
Reset value	0	0	0	0	0	0	0	0

Table 69. Min_timestp1/2/3/4 - minute timestamp register (address 16h/1Dh/24h/2Bh) bit description
Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7	T	0	-	unused
6 to 4	MINUTE_TIMESTP	0 to 5	ten's place	minute timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.12.3.4 Register Hour_timestp

Table 70. Hour_timestp1/2/3/4 - hour timestamp register (address 17h/1Eh/25h/2Ch) bit allocation
Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	AMPM	HOUR_TIMESTP (1 to 12) in 12-hour mode				
			HOUR_TIMESTP (0 to 23) in 24-hour mode					
Reset value	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 71. Hour_timestp1/2/3/4 - hour timestamp register (address 17h/1Eh/25h/2Ch) bit description
Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12-hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_TIMESTP	0 to 1	ten's place	hour timestamp information coded in BCD format when in 12-hour mode
3 to 0		0 to 9	unit place	
24-hour mode[1]				
5 to 4	HOUR_TIMESTP	0 to 2	ten's place	hour timestamp information coded in BCD format when in 24-hour mode
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the bit 12_24 in register Control_1.

7.12.3.5 Register Day_timestp

Table 72. Day_timestp1/2/3/4 - day timestamp register (address 18h/1Fh/26h/2Dh) bit allocation
Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	DAY_TIMESTP (1 to 31)					
Reset value	0	0	0	0	0	0	0	0

Table 73. Day_timestp1/2/3/4 - day timestamp register (address 18h/1Fh/26h/2Dh) bit description
Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 6	T	00	-	unused
5 to 4	DAY_TIMESTP	0 to 3	ten's place	day timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.12.3.6 Register Mon_timestp

Table 74. Mon_timestp1/2/3/4 - month timestamp register (address 19h/20h/27h/2Eh) bit allocation
Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	T	T	T	MONTH_TIMESTP (1 to 12)				
Reset value	0	0	0	0	0	0	0	0

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 75. Mon_timestp1/2/3/4 - month timestamp register (address 19h/20h/27h/2Eh) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Place value	Description
7 to 5	T	000	-	unused
4	MONTH_TIMESTP	0 to 1	ten's place	month timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.12.3.7 Register Year_timestp

Table 76. Year_timestp1/2/3/4 - year timestamp register (address 1Ah/21h/28h/2Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	YEAR_TIMESTP (0 to 99)							
Reset value	0	0	0	0	0	0	0	1

Table 77. Year_timestp1/2/3/4 - year timestamp register (address 1Ah/21h/28h/2Fh) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEAR_TIMESTP	0 to 9	ten's place	year timestamp information coded in BCD format
3 to 0		0 to 9	unit place	

7.12.4 Dependency between Battery switch-over and timestamp

The timestamp function depends on the control bit BTSE in register Control_3:

Table 78. Battery switch-over and timestamp

BTSE	BF		Description
0	-	[1]	the battery switch-over does not affect the timestamp registers
1			If a battery switch-over event occurs:
	0	[1]	the timestamp 4 group registers store the time and date when the switch-over occurs; after this event occurred BF is set logic 1
	1		the timestamp 4 group registers are not modified; in this condition subsequent battery switch-over events or falling edges on pin $\overline{TS4}$ are not registered

[1] Default value.

7.13 Interrupt output, $\overline{INTA}$/$\overline{INTB}$

PCF2131 has two interrupt output pins $\overline{INTA}$ and $\overline{INTB}$ which are open-drain, active LOW (requiring a pull-up resistor if used). Interrupts may be sourced from different places:

- second or minute timer
- watchdog timer

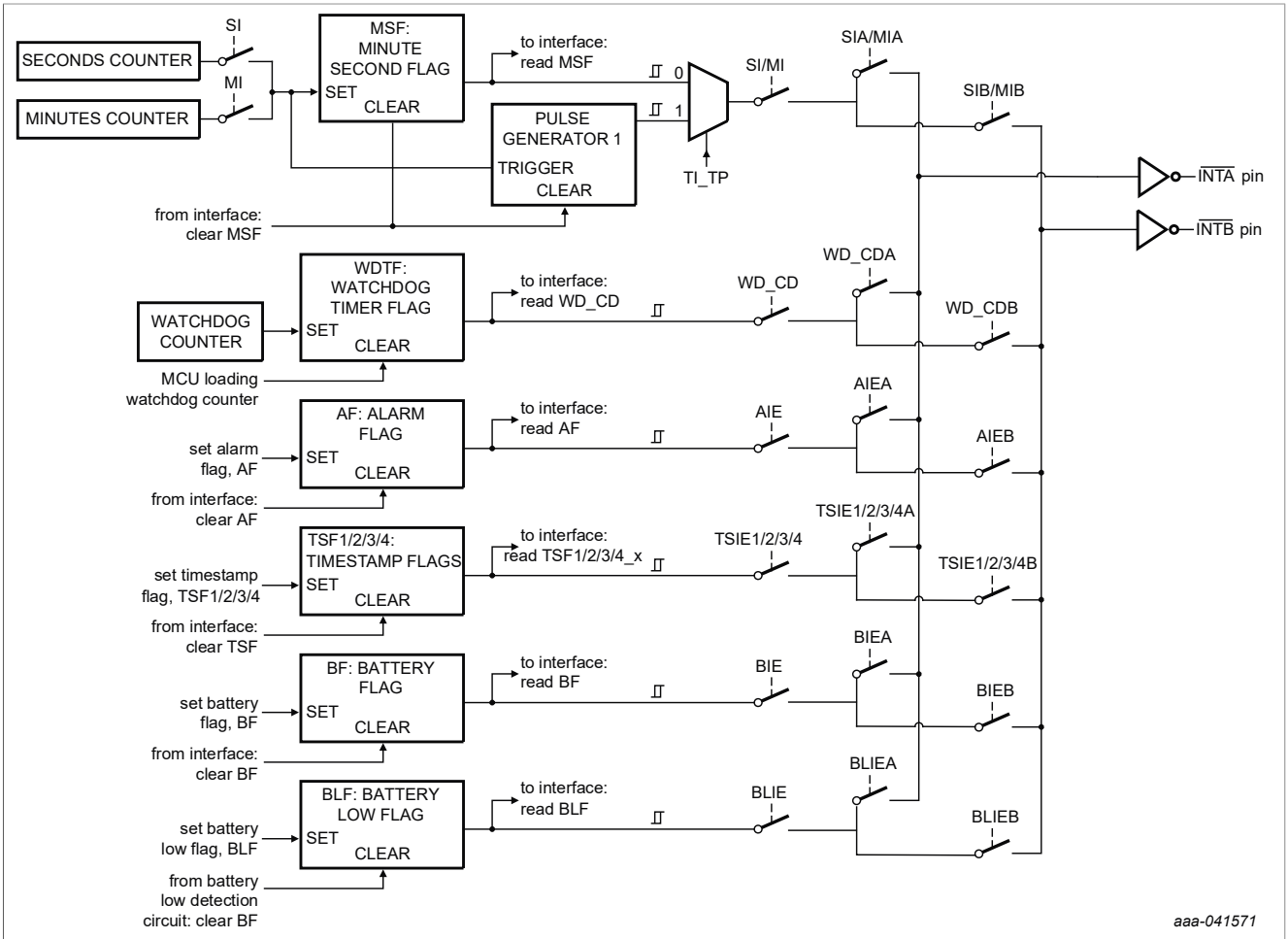
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

- alarm
- timestamp1/2/3/4
- battery switch-over
- battery low detection

The control bit TI_TP (register Watchdg_tim_ctl) is used to configure whether the interrupts generated from the second/minute timer (flag MSF in register Control_2) are pulsed signals or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal which follows the status of the corresponding flags. When the interrupt sources are all disabled, $\overline{INTA/B}$ remains high-impedance.

- The flags MSF, AF, TSFx, and BF can be cleared by command.
- The flag WDTF is read only. How it can be cleared is explained in Section 7.11.5.
- The flag BLF is read only. It is cleared automatically from the battery low detection circuit when the battery is replaced.



When SI, MI, WD_CD, AIE, TSIE1/2/3/4, BIE, BLIE are all disabled, $\overline{INTA}/\overline{INTB}$ remains high-impedance.

Figure 17. Interrupt block diagram

7.13.1 Minute and second interrupts

Minute and second interrupts are generated by predefined timers. The timers can be enabled independently from one another by the bits MI and SI in register

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Control_1. However, a minute interrupt enabled on top of a second interrupt cannot be distinguishable since it occurs at the same time.

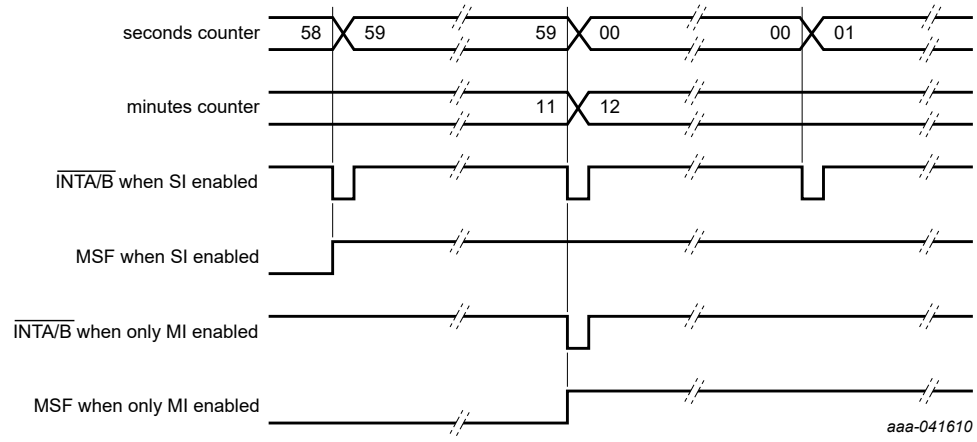
The minute/second flag MSF (register Control_2) is set logic 1 when either the seconds or the minutes counter increments according to the enabled interrupt (see Table 79). The MSF flag can be cleared by command.

Table 79. Effect of bits MI and SI on pin $\overline{\text{INTA/B}}$ and bit MSF

MI	SI	Result on $\overline{\text{INTA/B}}$	Result on MSF
0	0	no interrupt generated	MSF never set
1	0	an interrupt once per minute	MSF set when **minutes** counter increments
0	1	an interrupt once per second	MSF set when **seconds** counter increments
1	1	an interrupt once per second	MSF set when **seconds** counter increments

When MSF is set logic 1:

- If TI_TP is logic 1, the interrupt is generated as a pulsed signal if not masked.
- If TI_TP is logic 0, the interrupt is permanently active signal that remains until MSF is cleared.

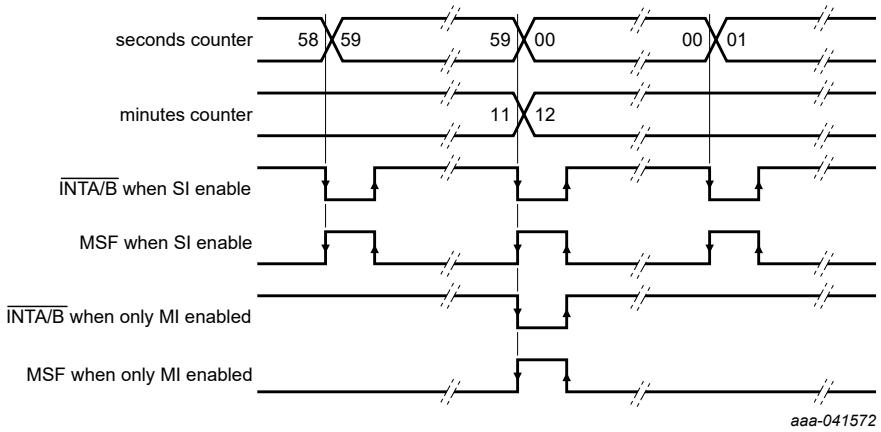


In this example, bit TI_TP is logic 1 and the MSF flag is not cleared after an interrupt.

Figure 18. $\overline{\text{INTA/B}}$ example for SI and MI when TI_TP is logic 1

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.



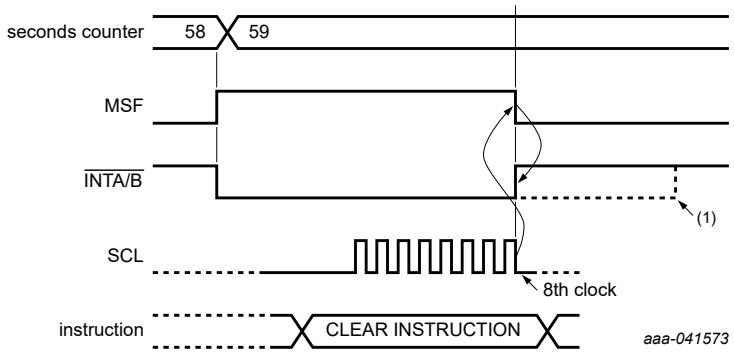
In this example, bit TI_TP is logic 0 and the MSF flag is cleared after an interrupt.

Figure 19. INTA/B example for SI and MI when TI_TP is logic 0

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and generates a pulse of $^{1}/_{64}$ seconds in duration.

7.13.2 INTA/B pulse shortening

If the MSF flag (register Control_2) is cleared before the end of the INTA/B pulse, then the INTA/B pulse is shortened. This allows the source of a system interrupt to be cleared immediately when it is serviced, that is, the system does not have to wait for the completion of the pulse before continuing; see Figure 20. Instructions for clearing the bit MSF can be found in Section 7.11.5.



1. Indicates normal duration of INTA/B pulse.

The timing shown for clearing bit MSF is also valid for the non-pulsed interrupt mode, that is, when TI_TP is logic 0, where the INTA/B pulse may be shortened by setting both bits MI and SI logic 0.

Figure 20. Example of shortening the INTA/B pulse by clearing the MSF flag

7.13.3 Watchdog timer interrupts

The generation of interrupts from the watchdog timer is controlled using the WD_CD bit (register Watchdg_tim_ctl). The interrupt is generated as an active signal which follows the status of the watchdog timer flag WDTF (register Control_2) if not masked. No pulse generation is possible for watchdog timer interrupts.

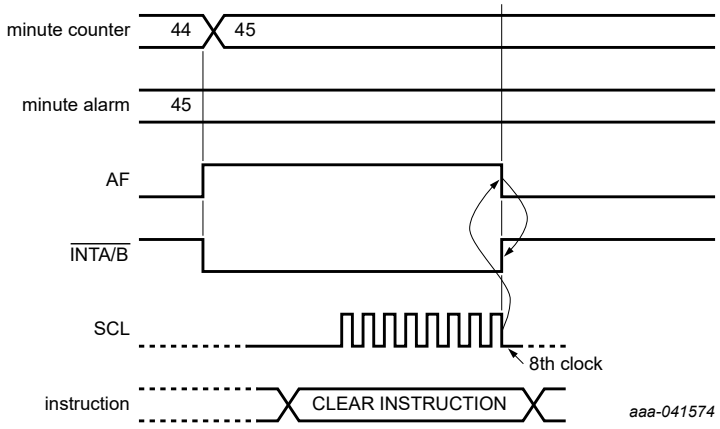
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

The interrupt is cleared when the flag WDTF is reset. Instructions for clearing it can be found in Section 7.11.5.

7.13.4 Alarm interrupts

Generation of interrupts from the alarm function is controlled by the bit AIE (register Control_2). If AIE is enabled, the $\overline{\text{INTA/B}}$ pin follows the status of bit AF (register Control_2) if not masked. Clearing AF immediately clears $\overline{\text{INTA/B}}$. No pulse generation is possible for alarm interrupts.



Example where only the minute alarm is used and no other interrupts are enabled.

Figure 21. AF timing diagram

7.13.5 Timestamp interrupts

Interrupt generation from the timestamp function is controlled using the TSIE1-4 bit (register Control_5). If TSIE1-4 is enabled, the $\overline{\text{INTA/B}}$ pin follows the status of the flags TSF1/2/3/4, if not masked. Clearing the flags TSFx immediately clears $\overline{\text{INTA/B}}$. No pulse generation is possible for timestamp interrupts.

7.13.6 Battery switch-over interrupts

Generation of interrupts from the battery switch-over is controlled by the BIE bit (register Control_3). If BIE is enabled, the $\overline{\text{INTA/B}}$ pin follows the status of bit BF in register Control_3 if not masked(see Table 78). Clearing BF immediately clears $\overline{\text{INTA/B}}$. No pulse generation is possible for battery switch-over interrupts.

7.13.7 Battery low detection interrupts

Generation of interrupts from the battery low detection is controlled by the BLIE bit (register Control_3). If BLIE is enabled, the $\overline{\text{INTA/B}}$ pin follows the status of bit BLF (register Control_3) if not masked. The interrupt is cleared when the battery is replaced (BLF is logic 0) or when bit BLIE is disabled (BLIE is logic 0). BLF is read only and therefore cannot be cleared by command.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7.13.8 Interrupt masks

Table 80. INT_A/B_MASK1 - interrupt mask 1 register (address 31h/33h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	INT_A/B_MASK1							
Reset value	-	-	1	1	1	1	1	1

Table 81. INT_A/B_MASK1 - interrupt mask 1 register (address 31h/33h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 6	T	00	unused
5	MIA/B	1	minute interrupt mask
4	SIA/B	1	second interrupt mask
3	WD_CDA/B	1	watchdog interrupt mask
2	AIEA/B	1	alarm interrupt mask
1	BIEA/B	1	battery flag interrupt mask
0	BLIEA/B	1	battery low flag interrupt mask

Table 82. INT_A/B_MASK2 - interrupt mask 2 register (address 32h/34h) bit allocation

Bits labeled as T are unused and return 0 when read.

Bit	7	6	5	4	3	2	1	0
Symbol	INT_A/B_MASK2							
Reset value	T	T	T	T	1	1	1	1

Table 83. INT_A/B_MASK2 - interrupt mask 2 register (address 32h/34h) bit description

Bits labeled as T are unused and return 0 when read.

Bit	Symbol	Value	Description
7 to 4	T	0000	unused
3	TSIE1A/B	1	time stamp 1 interrupt mask
2	TSIE2A/B	1	time stamp 2 interrupt mask
1	TSIE3A/B	1	time stamp 3 interrupt mask
0	TSIE4A/B	1	time stamp 4 interrupt mask

The registers at addresses 31h to 32h are used to configure interrupt source for $\overline{\text{INTA}}$ pin, and the registers at addresses 33h to 34h are for $\overline{\text{INTB}}$ pin.

All of above interrupts could be masked from either $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$, with corresponding bit set to ‘1’, as shown in Figure 17.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7.14 External clock test mode

A test mode is available which allows on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bits COF[2:0] logic 111 (register CLKOUT_ctl) and bit EXT_TEST logic 1 (register Control_1). Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal (8192 Hz) with the signal applied to pin CLKOUT. Every 8192 positive edges applied to pin CLKOUT generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a minimum period of 1 000 ns. The internal clock, now sourced from CLKOUT, is divided down by a divider chain called prescaler. The prescaler can be set into a known state by using bit STOP and CPR. When bit STOP and CPR are logic 1, the prescaler is reset to 0. STOP and CPR must be cleared before the prescaler can operate again.

From a stop condition, the first 1 second increment will take place after 8192 positive edges on pin CLKOUT. Thereafter, every 8192 positive edges cause a 1 second increment. In 100 Hz mode, the first 100th of a second increment will take place after 80 pulses on pin CLKOUT, and the first 1 second increment will take place after 8176 pulses on pin CLKOUT. Thereafter, every 8192 pulses cause a 1 second increment. The 100 Hz clock is generated from a dithered state machine which runs on the 256 Hz clock, so the number of pulses for each subsequent 100ths change is not constant. After the first 1 second increment the 25-bit dither pattern proceeds as follows from left to right: 11010101011010101101010

Where 1 == 96 CLKOUT pulses, and 0 == 64 CLKOUT pulses. This pattern repeats 4 times every second.In the first second, after 80 clock pulses trigger the first 100th,the left pattern is 10101010110101011010101, 11010101011010101101010, 11010101011010101101010, 11010101011010101101010, which means 96 pulses for 100ths == 2, then 64 pulses for 100ths == 3, 96 for 100ths == 4, and so on.

Remark: Entry into test mode is not synchronized to the internal 8192 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operating example:

1. Set CLKOUT = high-Z (register CLKOUT_ctl, COF[2:0] = 111).
2. Set EXT_TEST test mode (register Control_1, EXT_TEST is logic 1).
3. Set bit STOP (register Control_1, STOP is logic 1).
4. Set bit CPR (register SR_RESET, CPR is logic 1).
5. Set time registers to desired value.
6. Clear STOP (register Control_1, STOP is logic 0).
7. Apply 8192 clock pulses to CLKOUT.
8. Read time registers to see the first change.
9. Apply 8192 clock pulses to CLKOUT.
10. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

Operating example (100 Hz mode):

1. Set CLKOUT = high-Z (register CLKOUT_ctl, COF[2:0] = 111.
2. Set EXT_TEST test mode (register Control_1, EXT_TEST is logic 1).
3. Set bit STOP (register Control_1, STOP is logic 1).
4. Set bit CPR (register SR_RESET, CPR is logic 1).
5. Set time registers to desired value.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

6. Clear STOP (register Control_1, STOP is logic 0).
7. Apply 80 clock pulses to CLKOUT.
8. Read hundredths registers to see the first change.
9. Apply 8096 clock pulses to CLKOUT (8096 + 80 = 8176 total pulses).
10. Read seconds registers to see the first change.
11. Apply the number of pulses needed for the current dither value.
12. Read the hundredths register to see subsequent changes.
13. Read the seconds register every 8192 pulses to see subsequent changes.

7.15 STOP bit function

The STOP bit stops the time from counting in both RTC mode and external clock test mode. STOP must be set to unlock the time and date registers to set the time.

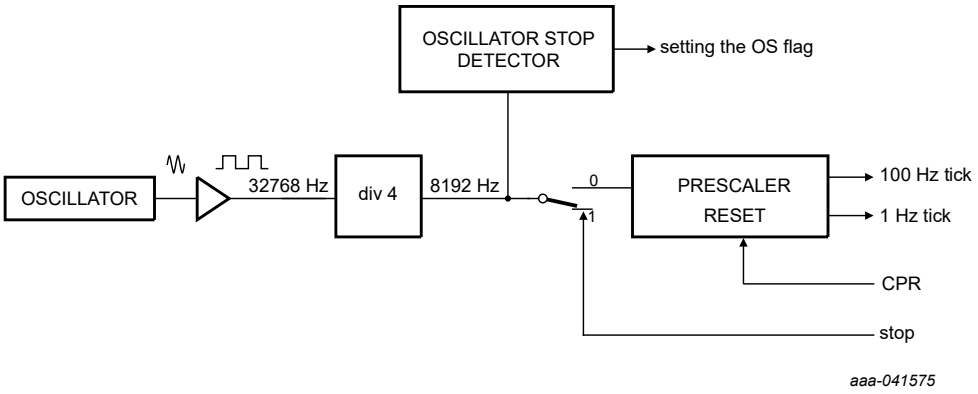


Figure 22. CPR and STOP bit functional diagram

The *stop* signal blocks the 8.192 kHz clock from generating system clocks and freezes the time. In this state, the prescaler can be cleared with the CPR command in the Resets register.

Remark: The CLKOUT output of clock frequencies is not affected.

The time circuits can then be set and do not increment until the STOP bit is released. There is a slight chance that STOP is set during a carry over of multiple time registers, which may have been executed incomplete. Therefore time must be set before clearing STOP to maintain time integrity.

The *stop* acts on the 8.192 kHz signal. Because the I^2C-bus or TS pin input is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8.192 kHz cycle (see Figure 23).

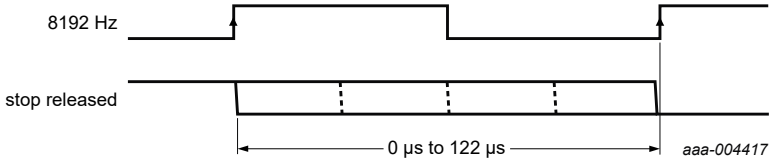


Figure 23. STOP release timing

The first increment of the time circuits is between 0 s and 122 µs after STOP is released.

All information provided in this document is subject to legal disclaimers.

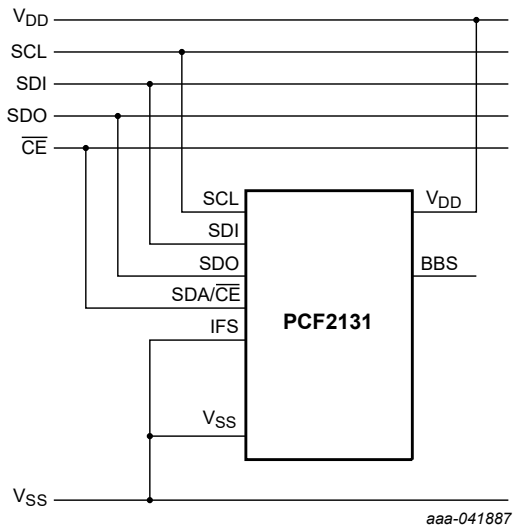
© NXP B.V. 2021. All rights reserved.

7.16 Interfaces

The PCF2131 has an I^2C-bus or SPI-bus interface using the same pins. The selection is done using the interface selection pin IFS (see Table 84).

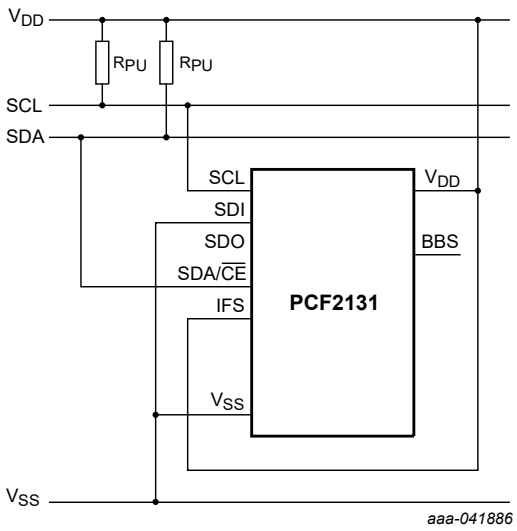
Table 84. Interface selection input pin IFS

Pin	Connection	Bus interface	Reference
IFS	V_{SS}	SPI-bus	Section 7.16.1
	V_{DD}	I^2C-bus	Section 7.16.2



To select the SPI-bus interface, pin IFS has to be connected to pin V_{SS}.

a. SPI-bus interface selection



To select the I^2C-bus interface, pin IFS has to be connected to pin V_{DD}.

b. I^2C-bus interface selection

Figure 24. Interface selection

7.16.1 SPI-bus interface

Data transfer to and from the device is made by a 4-line SPI-bus (see Table 85). The data lines for input and output are split. The SPI-bus is initialized whenever the chip enable line pin SDA/$\overline{CE}$ is inactive.

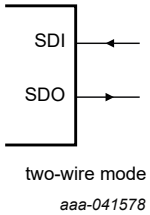


Figure 25. SDI, SDO configurations

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 85. Serial interface

Symbol	Function		Description
SDA/$\overline{CE}$	chip enable input; active LOW	[1]	when HIGH, the interface is reset; input may be higher than V_{DD}
SCL	serial clock input		when SDA/$\overline{CE}$ is HIGH, input may float; input may be higher than V_{DD}
SDI	serial data input		when SDA/$\overline{CE}$ is HIGH, input may float; input may be higher than V_{DD}; input data is sampled on the rising edge of SCL
SDO	serial data output		push-pull output; drives from V_{SS} to $V_{oper(int)}$ (V_{BBS}); output data is changed on the falling edge of SCL

[1] The chip enable must not be wired permanently LOW.

7.16.1.1 Data transmission

The chip enable signal is used to identify the transmitted data. Each data transfer is a whole byte, with the Most Significant Bit (MSB) sent first.

The transmission is controlled by the active LOW chip enable signal SDA/$\overline{CE}$. The first byte transmitted is the command byte. Subsequent bytes are either data to be written or data to be read (see Figure 26).

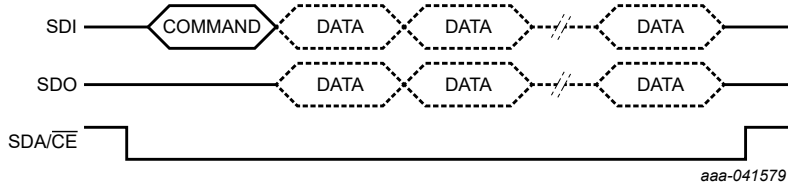


Figure 26. Data transfer overview

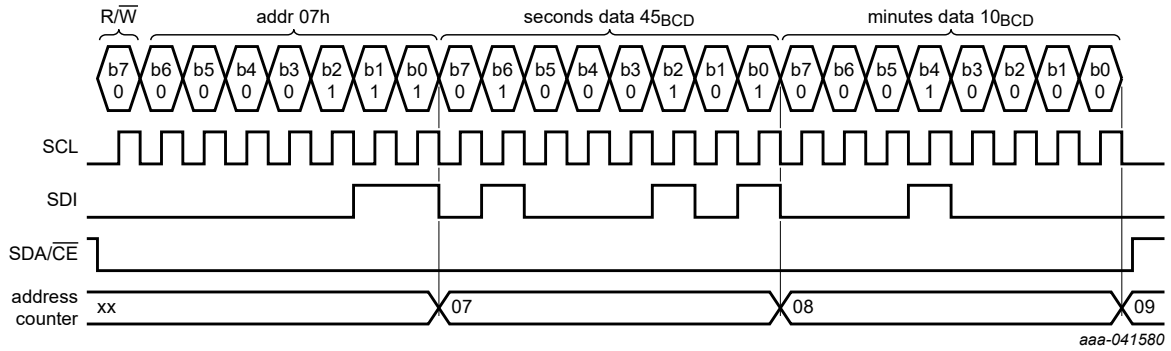
The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will reset to zero after the last valid register is accessed. The R/$\overline{W}$ bit defines if the following bytes are read or write information.

Table 86. Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		data read or write selection
		0	write data
		1	read data
6 to 0	RA	00h to 36h	register address

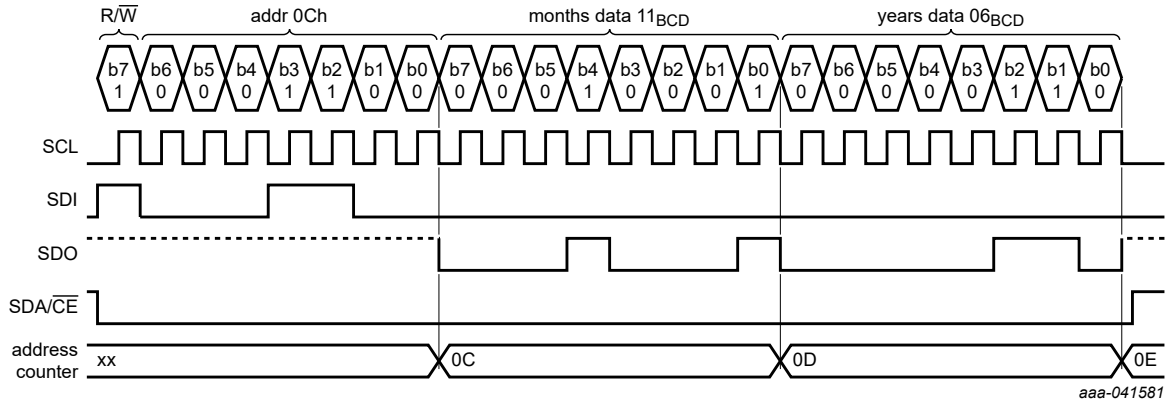
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.



In this example, the Seconds register is set to 45 seconds and the Minutes register to 10 minutes.

Figure 27. SPI-bus write example



In this example, the registers Months and Years are read. The pins SDI and SDO are not connected together. For this configuration, it is important that pin SDI is never left floating. It must always be driven either HIGH or LOW. If pin SDI is left open, high I_{DD} currents may result.

Figure 28. SPI-bus read example

7.16.2 I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines are connected to a positive supply by a pull-up resistor. Data transfer is initiated only when the bus is not busy.

7.16.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 29).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

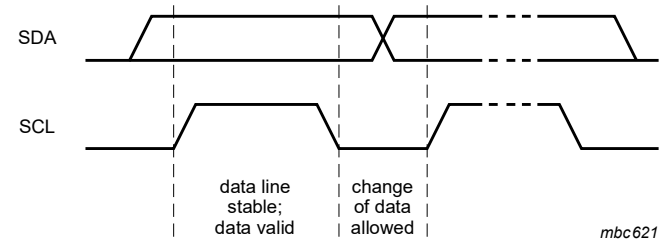


Figure 29. Bit transfer

7.16.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition S. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition P (see Figure 30).

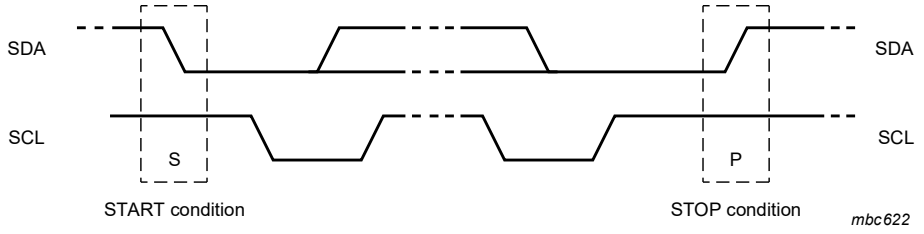


Figure 30. Definition of START and STOP conditions

7.16.2.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves.

The PCF2131 can act as a slave transmitter and a slave receiver.

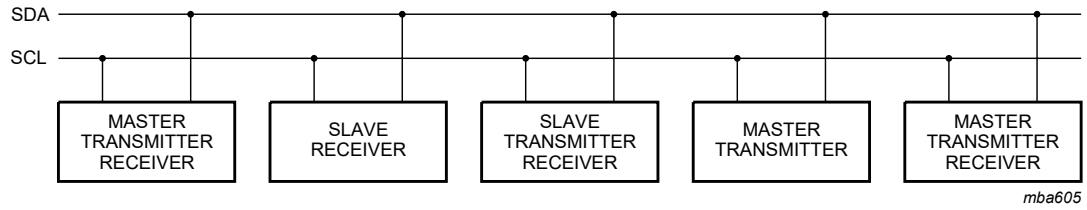


Figure 31. System configuration

7.16.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgment on the I^{2}C-bus is illustrated in Figure 32.

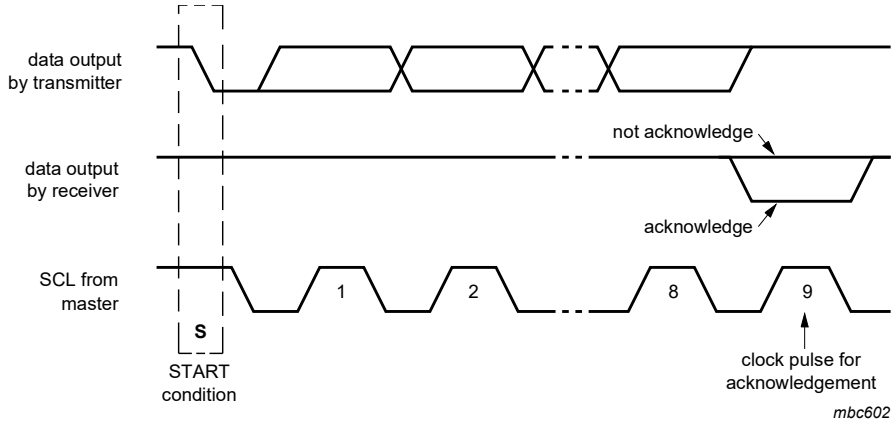


Figure 32. Acknowledgment on the I^{2}C-bus

7.16.2.5 I^{2}C-bus protocol

After a start condition, a valid hardware address has to be sent to a PCF2131 device. The appropriate I^{2}C-bus slave address is 1010 011. The entire I^{2}C-bus slave address byte is shown in Table 87.

Table 87. I^{2}C slave address byte

	Slave address							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MSB							**LSB**
	1	0	1	0	0	1	1	R/$\overline{W}$

The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer (read is logic 1, write is logic 0).

For the format and the timing of the START condition (S), the STOP condition (P), and the acknowledge (A) refer to the I^{2}C-bus specification [3] and the characteristics table (Table 92). In the write mode, a data transfer is terminated by sending a STOP condition.

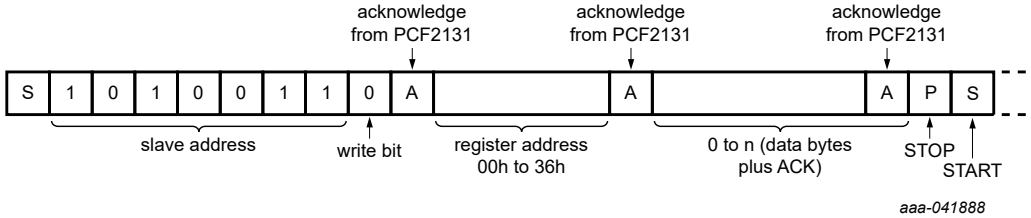


Figure 33. Bus protocol, writing to registers

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

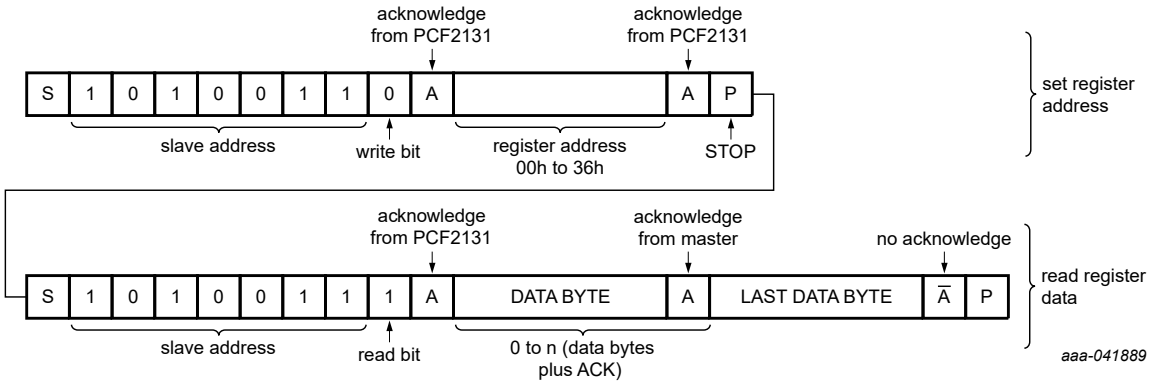


Figure 34. Bus protocol, reading from registers

7.16.3 Bus communication and battery backup operation

To save power during battery backup operation (see Section 7.5.1), the bus interfaces are inactive. Therefore the communication via I^2C- or SPI-bus should be terminated before the supply of the PCF2131 is switched from V_{DD} to V_{BAT}.

With I2C interface, PCF2131 will terminate transaction before switching from V_{DD} to V_{BAT}, with SPI interface, PCF2131 will corrupt SPI write and read data when battery switchover occurs.

Remark: If the I^2C-bus communication was terminated uncontrolled, the I^2C-bus has to be reinitialized by sending a STOP followed by a START after the device switched back from battery backup operation to V_{DD} supply operation.

7.17 Internal circuitry

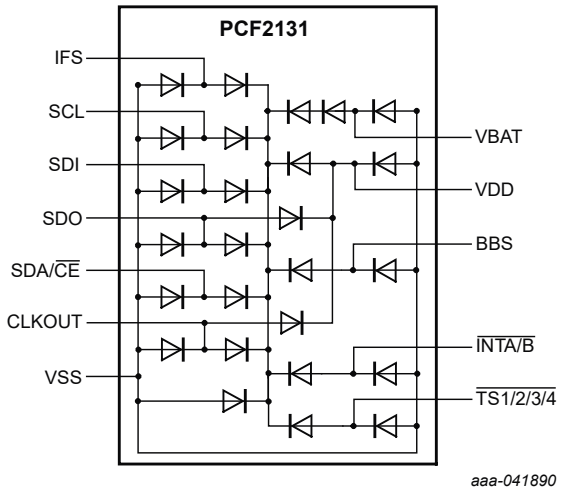


Figure 35. Device diode protection diagram of PCF2131

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

7.18 Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

8 Limiting values

Table 88. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+6.5	V
I_{DD}	supply current			-50	+50	mA
V_i	input voltage			-0.5	+6.5	V
I_I	input current			-10	+10	mA
V_O	output voltage			-0.5	+6.5	V
I_O	output current			-10	+10	mA
		at pin SDA/$\overline{CE}$		-10	+20	mA
V_{BAT}	battery supply voltage			-0.5	+6.5	V
P_{tot}	total power dissipation			-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±2 000	V
		CDM	[2]	-	±500	V
I_{lu}	latch-up current		[3]	-	1 00	mA
T_{stg}	storage temperature		[4]	-55	+85	°C
T_{amb}	ambient temperature	operating device		-40	+85	°C

[1] Pass level; Human Body Model (HBM) according to AEC Q100-002.
[2] Pass level (750 V for corner pins); Charged-Device Model (CDM), according to AEC Q100-011.
[3] Pass level; latch-up testing according to AEC Q100-004 at maximum ambient temperature ($T_{amb(max)}$).
[4] According to the store and transport requirements (see [4]) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

Note: *The PCF2131 part is not guaranteed (nor characterized) above the operating range as denoted in the data sheet. NXP recommends not to bias the PCF2131 device during reflow (e.g. if utilizing a 'coin' type battery in the assembly). If customer so chooses to use this assembly method, there must be the allowance for a full \Q0 V' level Power supply \Qreset' to re-enable the device. Without a proper POR, the device may remain in an indeterminate state.*

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

9 Static characteristics

Table 89. Static characteristics

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage		[1]	1.2	-	5.5	V
V_{BAT}	battery supply voltage			1.2	-	5.5	V
V_{low}	low voltage			-	1.15	-	V
I_{DD} supply current [2]		interface active; supplied by V_{DD}					
		SPI-bus (f_{SCL} = 6.5 MHz)		-	-	800	µA
		I^2C-bus (f_{SCL} = 400 kHz)		-	-	200	µA
		interface inactive (f_{SCL} = 0 Hz) [3] ; TCR[1:0] = 00 (see Table 16)					
		PWRMNG[2:0] = 111 (see Table 22); COF[2:0] = 111 (see Table 18) TC_DIS = 1 (see Table 5); 100TH_S_DIS = 1 (see Table 5)					
		V_{DD} = 1.2 V		-	88	400	nA
		V_{DD} = 3.3 V		-	64	350 [4]	nA
		V_{DD} = 5.5 V		-	71	450	nA
		PWRMNG[2:0] = 111 (see Table 22); COF[2:0] = 111 (see Table 18) TC_DIS = 0 (see Table 5); 100TH_S_DIS = 1 (see Table 5)					
		V_{DD} = 1.2 V		-	101	500	nA
		V_{DD} = 3.3 V		-	70	450	nA
		V_{DD} = 5.5 V		-	76	550	nA
		PWRMNG[2:0] = 111 (see Table 22); COF[2:0] = 000 (see Table 18) TC_DIS = 0 (see Table 5); 100TH_S_DIS = 0 (see Table 5);					
		V_{DD} = 1.2 V	[5]	-	460	770	nA
		V_{DD} = 3.3 V	[5]	-	1035	1365	nA
		V_{DD} = 5.5 V	[5]	-	1670	2135	nA
		PWRMNG[2:0] = 000 (see Table 22); COF[2:0] = 111 (see Table 18) TC_DIS = 0 (see Table 5); 100TH_S_DIS = 0 (see Table 5)					
		V_{DD} = 1.8 V, V_{BAT} = 1.5 V		-	118	500	nA
		V_{DD} = 3.3 V, V_{BAT} = 3.3 V		-	104	500	nA
		V_{DD} = 5.5 V, V_{BAT} = 3.3 V		-	107	550	nA
		V_{BAT} = 1.2 V, I_{BAT}	[6]	-	104	565	nA
		V_{BAT} = 3.3 V, I_{BAT}:	[6]	-	83	450	nA
		V_{BAT} = 5.5 V, I_{BAT}:	[6]	-	91	625	nA

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 89. Static characteristics...*continued*

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD} supply current [2]		PWRMNG[2:0] = 000 (see Table 22); COF[2:0] = 000 (see Table 18) TC_DIS = 0 (see Table 5); 100TH_S_DIS = 0 (see Table 5)					
		V_{DD} = 1.8 V, V_{BAT} = 1.5 V	[5]	-	640	945	nA
		V_{DD} = 3.3 V, V_{BAT} = 3.3 V	[5]	-	1060	1410	nA
		V_{DD} = 5.5 V, V_{BAT} = 3.3 V	[5]	-	1705	2190	nA
		V_{BAT} = 1.2 V, I_{BAT}	[6]	-	130	390	nA
		V_{BAT} = 3.3 V, I_{BAT}	[6]	-	145	390	nA
		V_{BAT} = 5.5 V, I_{BAT}	[6]	-	210	500	nA
$I_{L(bat)}$	battery leakage current	V_{DD} is active supply; V_{BAT} = 3.0 V		-	0.1	-	nA
Power management							
$V_{th(sw)bat}$	battery switch threshold voltage			2.3	2.5		V
$V_{th(bat)low}$	low battery threshold voltage			2.3	2.5		V
Inputs [7]							
V_I	input voltage			-0.5	-	V_{DD} + 0.5	V
V_{IL}	LOW-level input voltage			-	-	$0.25V_{DD}$	V
		T_{amb} = -40 °C to +85 °C; V_{DD} > 2.0 V		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		-	0	-	µA
		post ESD event		-1	-	+1	µA
C_i	input capacitance		[8]	-	-	7	pF
Outputs							
V_O	output voltage	on pins $\overline{INTA/B}$, referring to external pull-up		-0.5	-	5.5	V
		on pin BBS	[9]	1.2	-	5.5	V
V_{OH}	HIGH output voltage	on pin SDO, CLKOUT at 1 mA source current		$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW output voltage	on pins CLKOUT, $\overline{INTA/B}$ and SDO at 1 mA sink current		V_{SS}	-	$0.2V_{DD}$	V
		on pin SDA, V_{DD} > 2.0 V, 3 mA sink current		-	-	0.4	V
		on pin SDA, V_{DD} < 2.0 V, 2 mA sink current		-	-	$0.2V_{DD}$	V

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

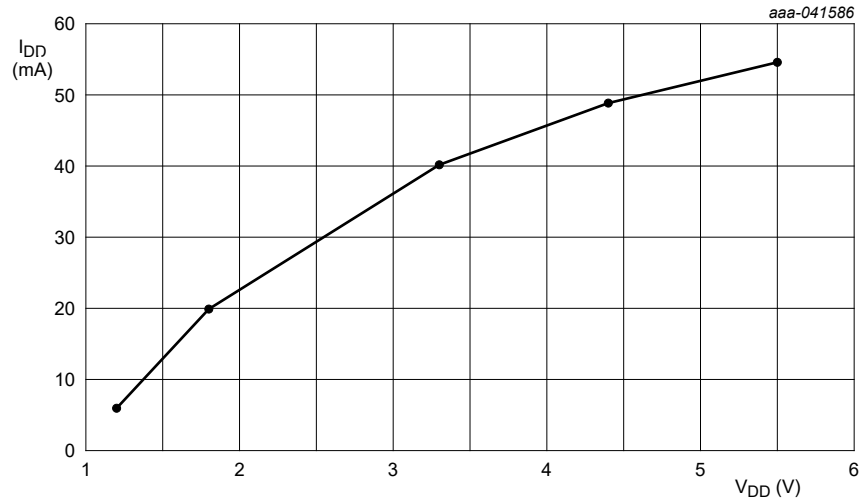
Table 89. Static characteristics...*continued*

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V					
		on pin SDA/$\overline{CE}$	[10]	3	-	-	mA
		on all other outputs		1.0	-	-	mA
I_{OH}	HIGH-level output current	output source current; on pin SDO, CLKOUT; V_{OH} = 0.8 * V_{DD}		1.0	-	-	mA
I_{LO}	output leakage current	V_O = V_{DD} or V_{SS}		-	0	-	µA
		post ESD event		-1	-	+1	µA

[1] For reliable oscillator start-up and OTP refresh at power-on: V_{DD} needs to be above 1.8 V.
[2] MAX I_{DD} and I_{BAT} determined by characterization.
[3] Timer source clock = $^{1}/_{60}$ Hz, level of pins SDA/$\overline{CE}$, SDI, and SCL is V_{DD} or V_{SS}.
[4] Production tested I_{DD}parameter.
[5] Any load in the application driven by CLKOUT adds to this value, e.g. 10 pF, Vdd = 3v3 will add 32768 Hz * 10 pF * 3.3 V = 1.1 µA.
[6] When the device is supplied by the V_{BAT} pin instead of the V_{DD} pin, V_{DD} = 0 V. The device can only start up from V_{DD}.
[7] The I^2C-bus and SPI-bus interfaces of PCF2131 are 5 V tolerant.
[8] Tested on sample basis.
[9] Pin BBS is internally connected to either V_{DD} or V_{BAT}, see section Section 7.5.3.
[10] For further information, see Figure 36.

9.1 Current consumption characteristics, typical

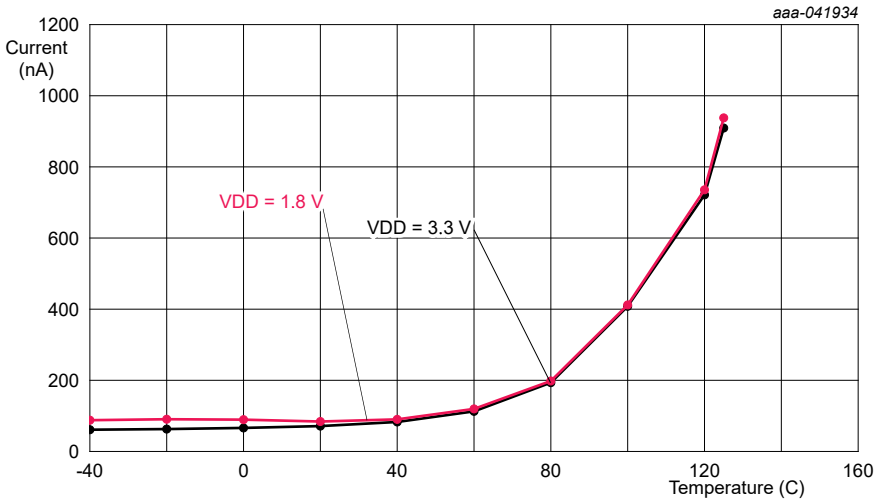


Typical value; V_{OL} = 0.4 V.

Figure 36. I_{OL} on pin SDA/$\overline{CE}$

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

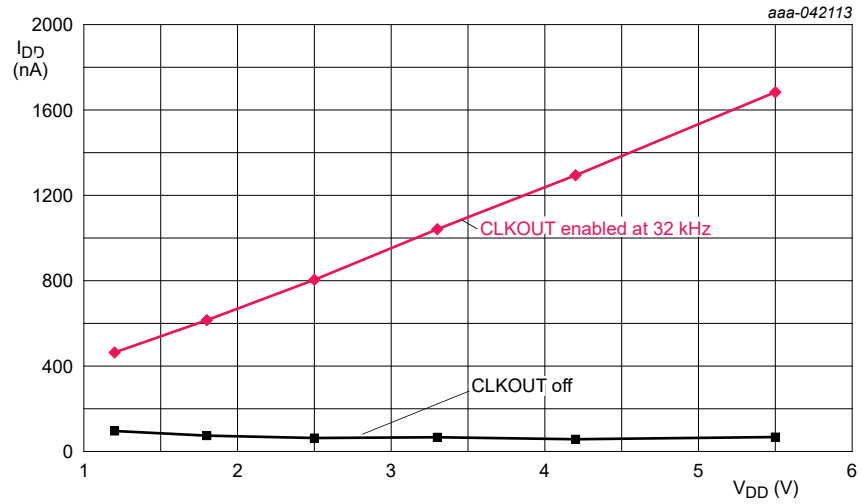


CLKOUT disabled; PWRMNG[2:0] = 111; TSOFF = 1; $\overline{TS}$ input floating.

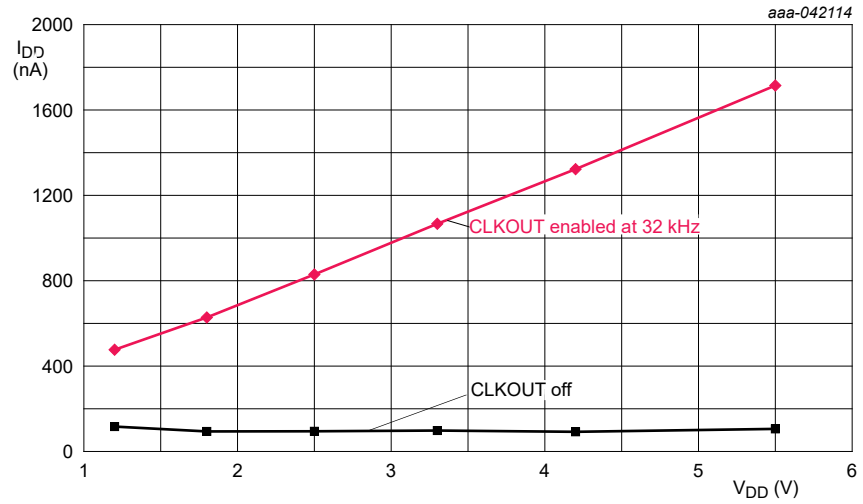
Figure 37. I_{DD} as a function of temperature

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.



a. PWRMNG[2:0] = 111; TSOFF = 1; T_{amb} = 25 °C; $\overline{TS}$ input floating



b. PWRMNG[2:0] = 000; TSOFF = 0; T_{amb} = 25 °C; $\overline{TS}$ input floating

Figure 38. I_{DD} as a function of V_{DD}

9.2 Frequency characteristics

Table 90. Frequency characteristics

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = +25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_o	output frequency	on pin CLKOUT; V_{DD} = 3.3 V; COF[2:0] = 000; AO[3:0] = 1000		-	32.768	-	kHz
Δf/f	time accuracy	V_{DD} or V_{BAT} = 3.3 V, Tamb = -40 °C to +85 °C					
		TC_DIS = 0	[1] [2]	-8	±3	+8	ppm
		TC_DIS = 1	[1] [2]	-200		+4	ppm

All information provided in this document is subject to legal disclaimers.

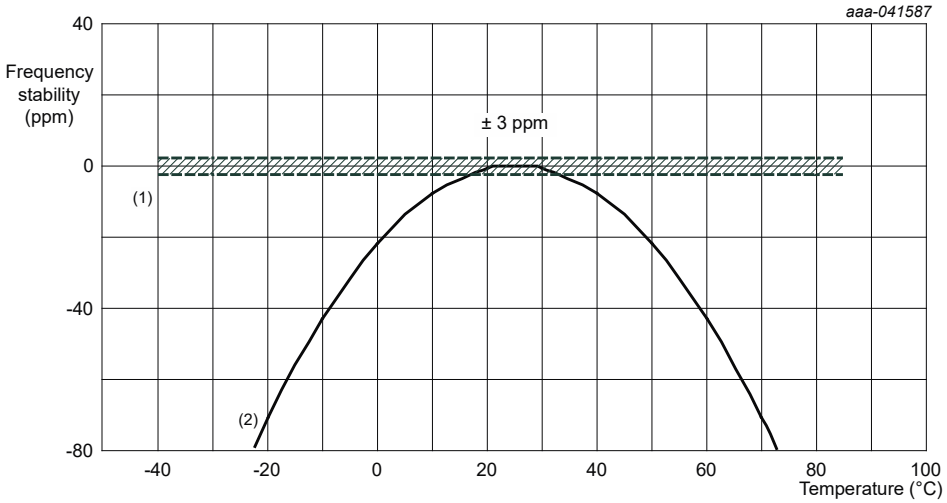
© NXP B.V. 2021. All rights reserved.

Table 90. Frequency characteristics...*continued*

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = +25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		TC_DIS = 1, Tamb = 25 °C	[1] [2]	-3		+3	ppm
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation	crystal aging					
		PCF2131					
		first year; V_{DD} or V_{BAT} = 3.3 V	[3]	-3	-	+3	ppm
$\Delta f/\Delta V$	frequency variation with voltage	on pin CLKOUT		-	±1	-	ppm/V
Jitter	Output clock peak to peak jitter	on pin CLKOUT		-	50	-	ns

[1] ±1 ppm corresponds to a time deviation of ±0.0864 seconds per day.
[2] Only valid if CLKOUT frequencies are not equal to 32.768 kHz or if CLKOUT is disabled.
[3] Not production tested. Effects of reflow soldering are included (see application note AN13203).



1. Typical temperature compensated RTC time accuracy response (TC_DIS = 0).
2. Typical CLKOUT frequency Y [ppm] = -0.035*(T-25C)^2 (TC_DIS = 0 or 1).

Figure 39. Typical characteristic of frequency with respect to temperature of PCF2131

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

10 Dynamic characteristics

10.1 SPI-bus timing characteristics

Table 91. SPI-bus characteristics

V_{DD} = 1.2 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +105 °C, unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} (see Figure 40).

Symbol	Parameter	Conditions		V_{DD} = 1.2 V to 3.3 V		V_{DD} = 3.3 V to 5.5 V		Unit
				Min	Max	Min	Max	
Pin SCL								
$f_{clk(SCL)}$	SCL clock frequency			-	0.5	-	6.5	MHz
$t_{clk(H)}$	clock HIGH time			1000	-	70	-	ns
$t_{clk(L)}$	clock LOW time			1000	-	70	-	ns
t_r	rise time	for SCL signal		-	100	-	100	ns
t_f	fall time	for SCL signal		-	100	-	100	ns
Pin SDA/$\overline{CE}$								
$t_{su(CE\_N)}$	CE_N set-up time			300	-	30	-	ns
$t_{h(CE\_N)}$	CE_N hold time			325	-	25	-	ns
$t_{rec(CE\_N)}$	CE_N recovery time			1500	-	1500	-	ns
$t_{w(CE\_N)}$	CE_N pulse width			-	0.99	-	0.99	s
Pin SDI								
t_{su}	set-up time	set-up time for SDI data		250	-	20	-	ns
t_h	hold time	hold time for SDI data		250	-	20	-	ns
Pin SDO								
$t_{d(R)SDO}$	SDO read delay time	C_L = 50 pF		-	550	-	55	ns
$t_{dis(SDO)}$	SDO disable time		[1]	-	150	-	25	ns

[1] No load value; bus is held up by bus capacitance; use RC time constant with application values.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

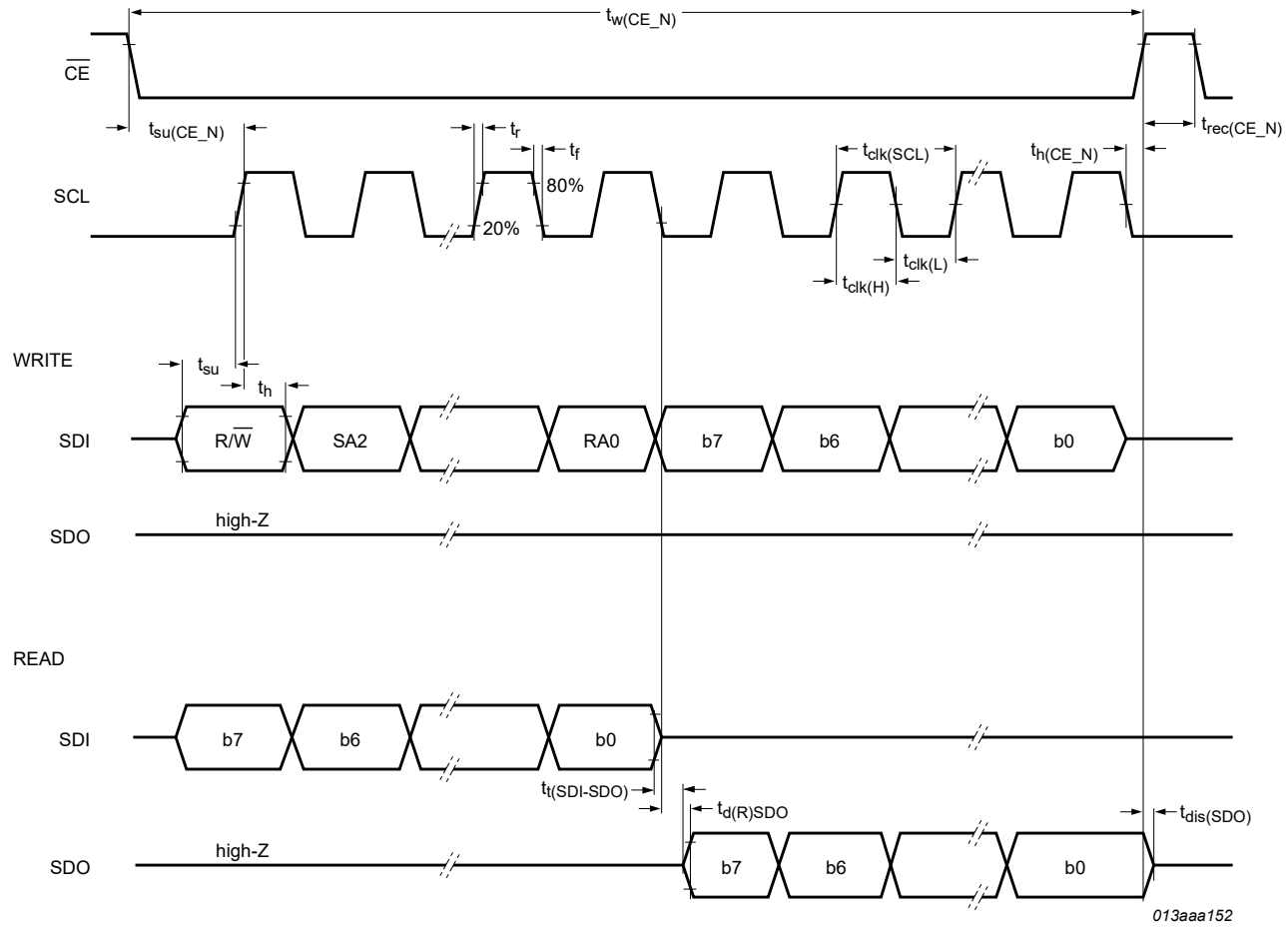


Figure 40. SPI-bus timing

10.2 I²C-bus timing characteristics

Table 92. I²C-bus characteristics

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 41).

Symbol	Parameter		Standard mode		Fast-mode (Fm)		Unit
			Min	Max	Min	Max	
Pin SCL							
f_{SCL}	SCL clock frequency	[1]	10	100	10	400	kHz
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
Pin SDA/$\overline{CE}$							
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
Pins SCL and SDA/$\overline{CE}$							
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.5	-	µs

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Table 92. I^2C-bus characteristics...*continued*

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30 % and 70 % with an input voltage swing of V_{SS} to V_{DD} (see Figure 41).

Symbol	Parameter		Standard mode		Fast-mode (Fm)		Unit
			Min	Max	Min	Max	
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
t_r	rise time of both SDA and SCL signals	[2][3][4]	-	1 000	$20 + 0.1C_b$	300	ns
t_f	fall time of both SDA and SCL signals	[2][3][4]	-	300	$20 + 0.1C_b$	300	ns
$t_{VD;ACK}$	data valid acknowledge time	[5]	-	3.45	-	0.9	µs
$t_{VD;DAT}$	data valid time	[6]	-	3.45	-	0.9	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	ns

[1] The minimum SCL clock frequency is limited by the bus time-out feature which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.
[2] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
[3] C_b is the total capacitance of one bus line in pF.
[4] The maximum t_f for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA/$\overline{CE}$ pin, the SCL pin, and the SDA/SCL bus lines without exceeding the maximum t_f.
[5] $t_{VD;ACK}$ is the time of the acknowledgment signal from SCL LOW to SDA (out) LOW.
[6] $t_{VD;DAT}$ is the minimum time for valid SDA (out) data following SCL LOW.
[7] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

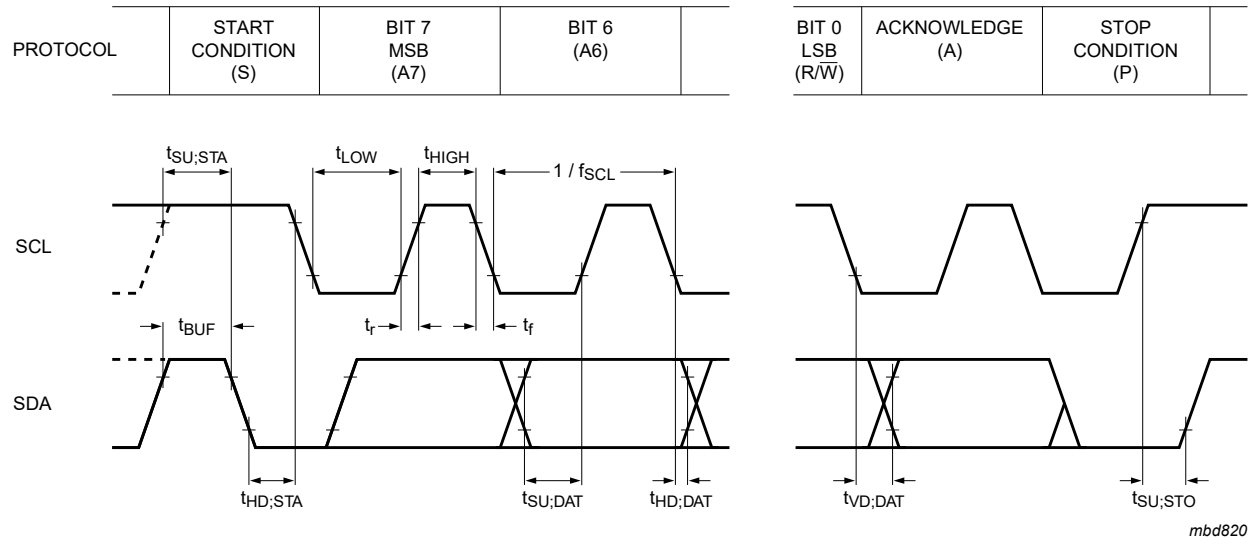
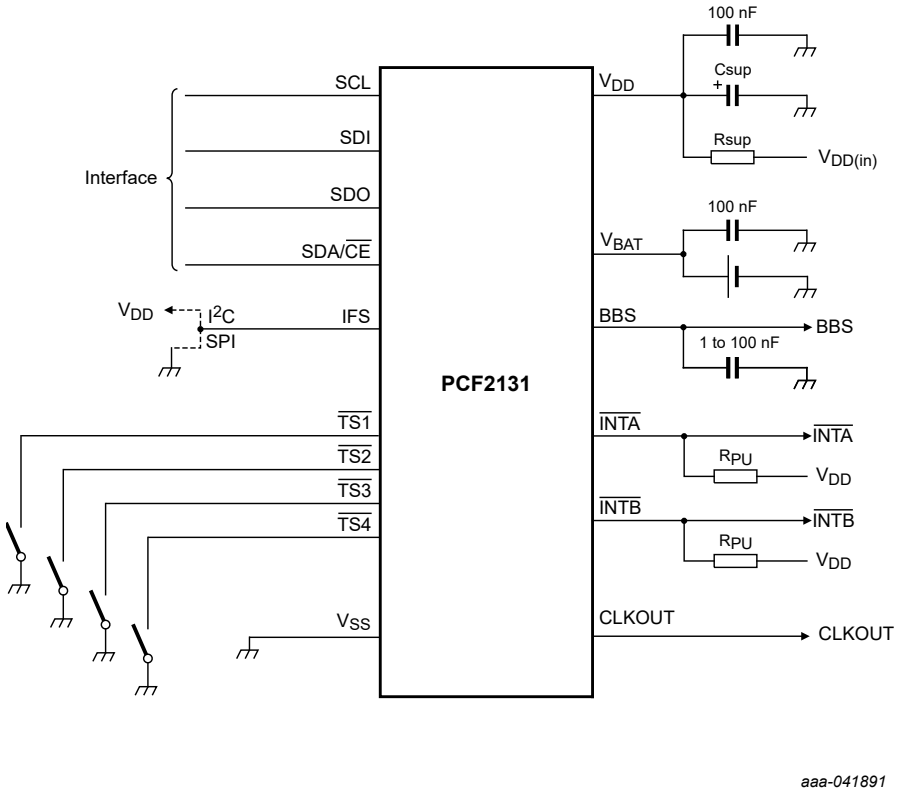


Figure 41. I^2C-bus timing diagram; rise and fall times refer to 30 % and 70 %

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

11 Application information



R_{PU}: 10 kΩ is recommended.

R_{SUP} and C_{SUP}: An appropriate RC filter needs to be added to guarantee the chip will only see <0.35 V/ms ramp down rate on supply, even if Vdd_in ramp rate is very high.

Figure 42. General application diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

12 Package outline

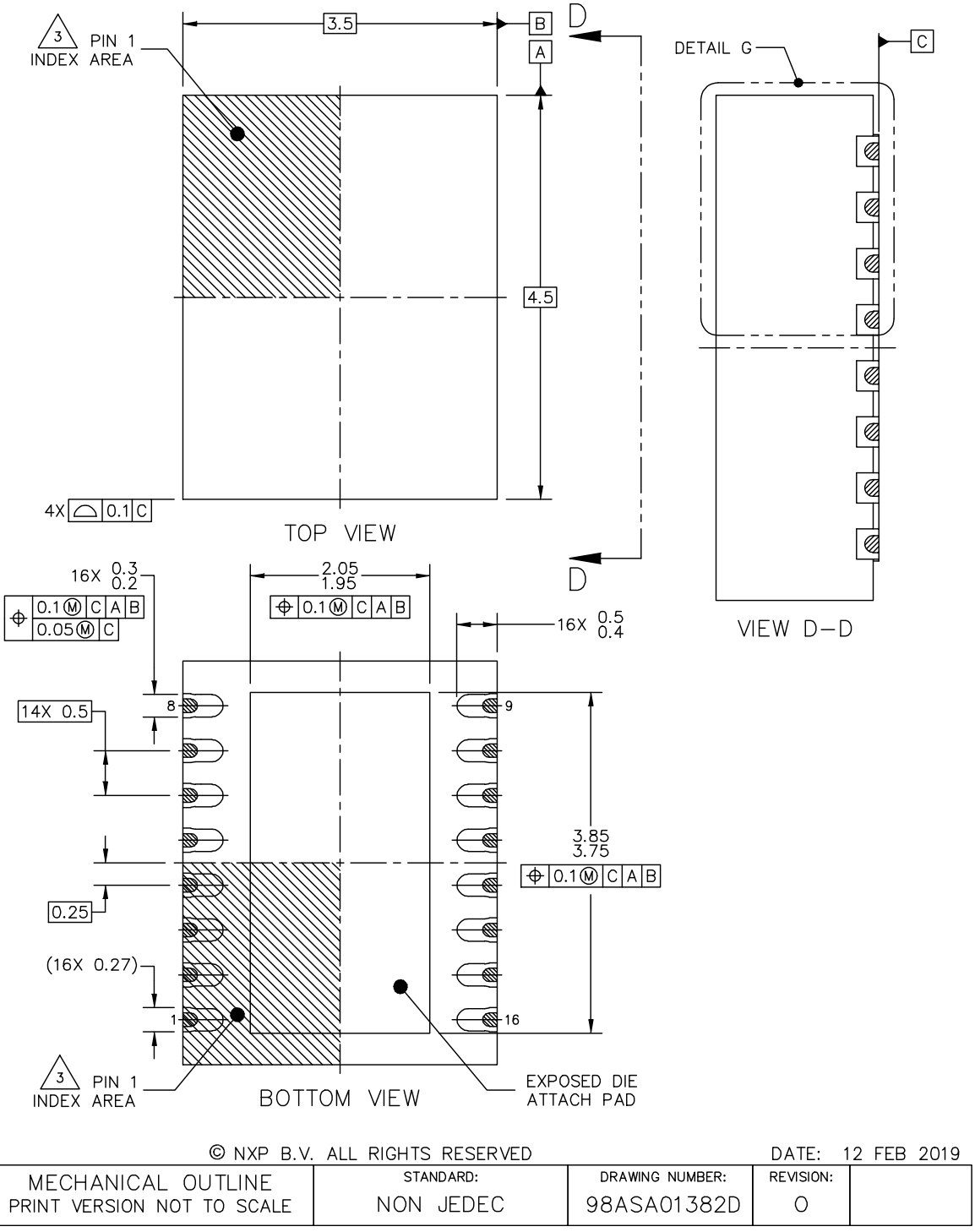
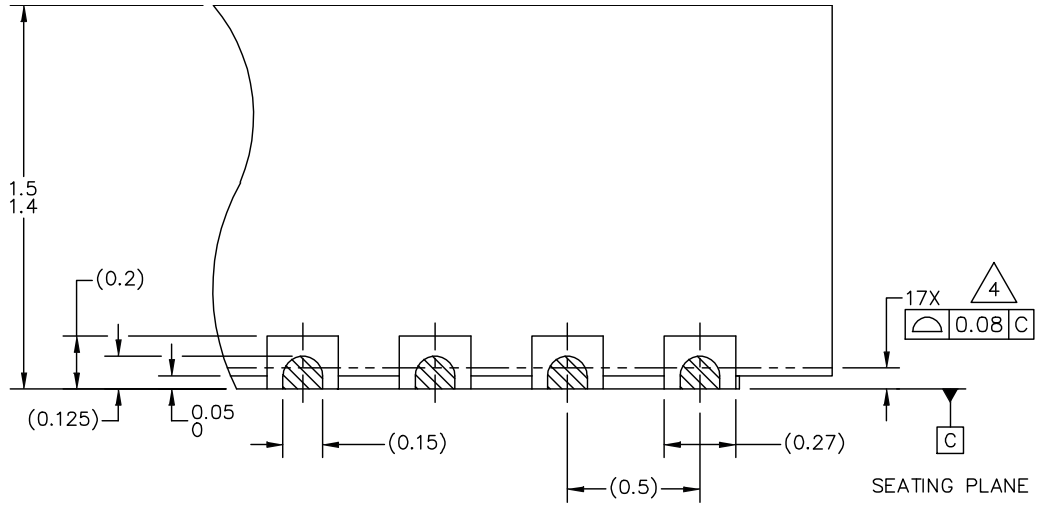


Figure 43. Package outline SOT1992-1 (HLSON16)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.



DETAIL G
VIEW ROTATED 90° CW

© NXP B.V. ALL RIGHTS RESERVED

DATE: 12 FEB 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01382D	REVISION: O	

Figure 44. Package outline SOT1992-1 (HLSON16); detail G

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

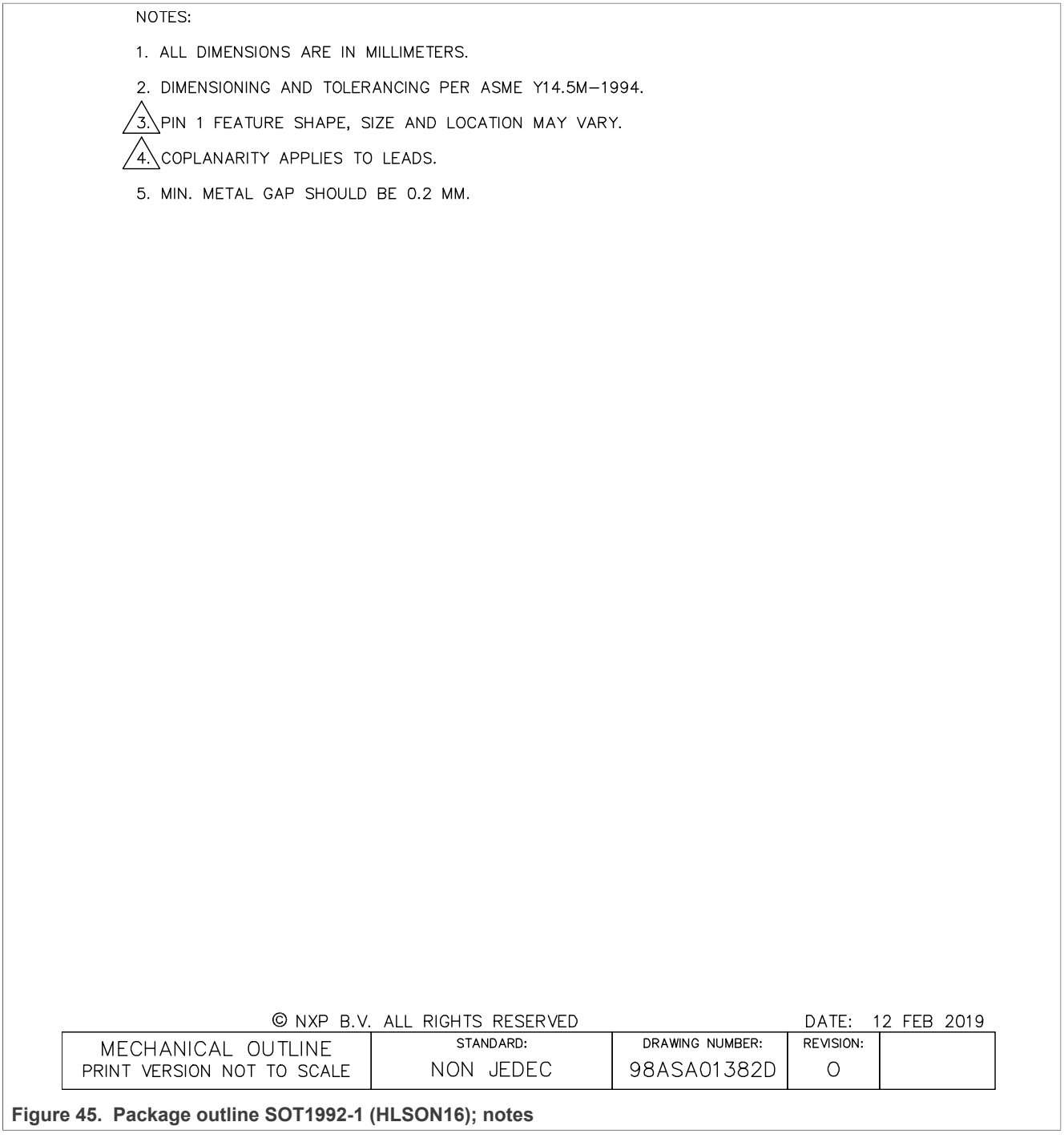


Figure 45. Package outline SOT1992-1 (HLSON16); notes

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

13 Packing information

13.1 Tape and reel information

For tape and reel packing information, see [2]

14 Soldering

For information about soldering, see [1].

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

14.1 Footprint information

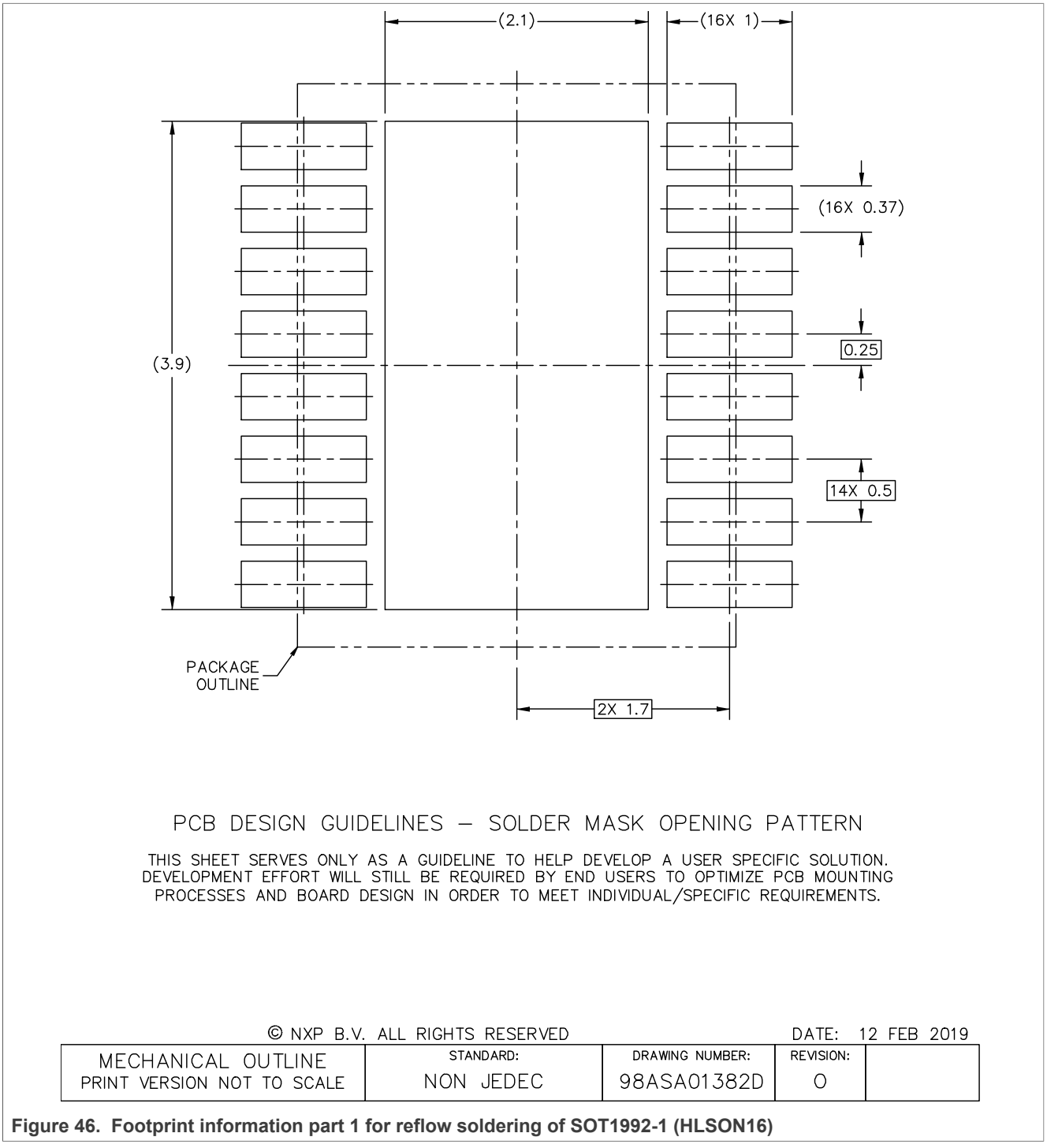
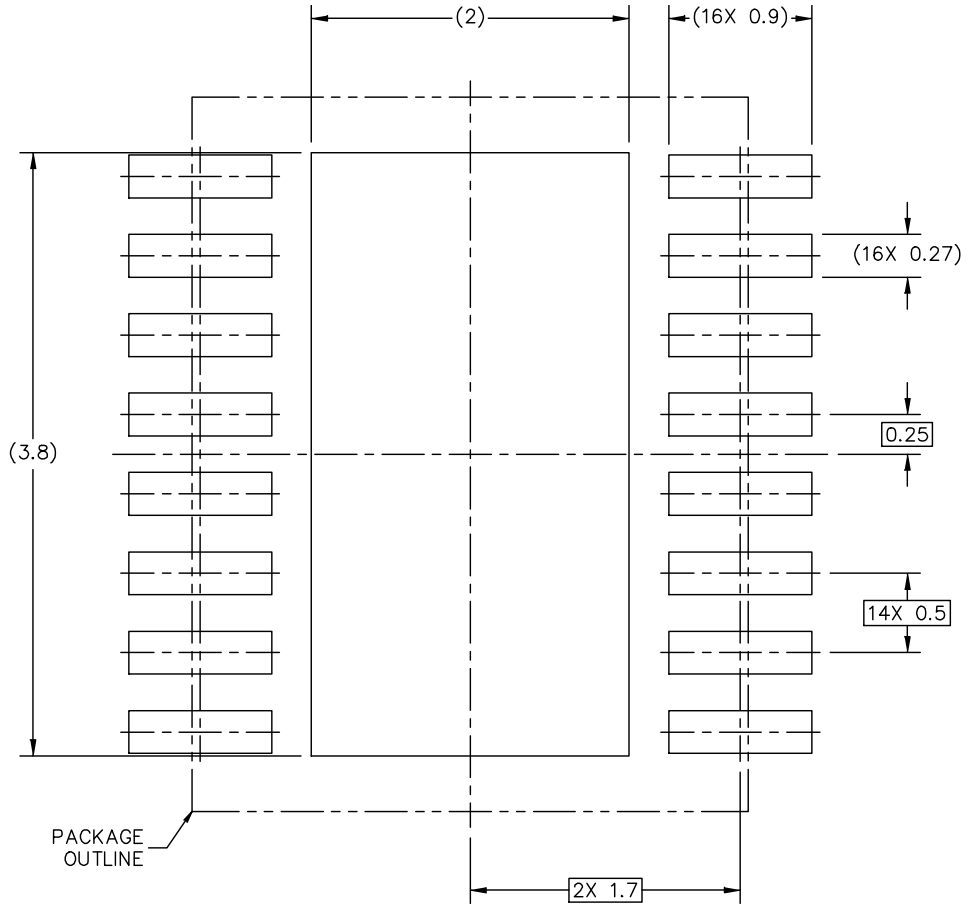


Figure 46. Footprint information part 1 for reflow soldering of SOT1992-1 (HLSON16)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

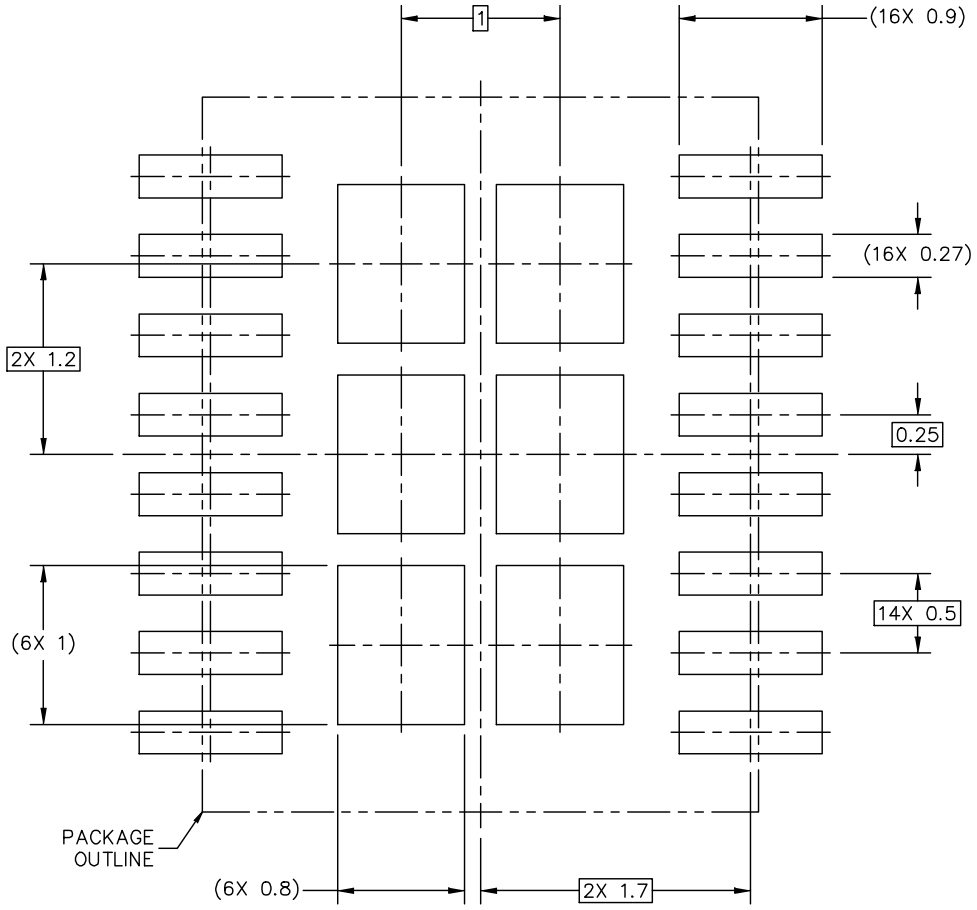
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 12 FEB 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01382D	REVISION: O	

Figure 47. Footprint information part 2 for reflow soldering of SOT1992-1 (HLSON16)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 12 FEB 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01382D	REVISION: O	

Figure 48. Footprint information part 3 for reflow soldering of SOT1992-1 (HLSON16)

15 Appendix

15.1 Real-time clock selection

Table 93. Selection of Real-Time Clocks

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD}, typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special fea
PCF8563	X	1	I^2C	250	-	-	-	-
PCF8564A	X	1	I^2C	250	-	-	-	integrated c
PCA8565	X	1	I^2C	600	-	-	segment B, grade 1	high robust T_{amb}= -40 °
PCA8565A	X	1	I^2C	600	-	-	-	integrated c T_{amb}= -40 °
PCF85063	-	1	I^2C	220	-	-	-	basic functi
PCF85063A	X	1	I^2C	220	-	-	-	tiny packag
PCF85063B	X	1	SPI	220	-	-	-	tiny packag
PCA85073A	X	1	I^2C	220	-	-	segment B, grade 2	tiny packag
PCF85263A	X	2	I^2C	230	X	1	-	time stamp stopwatch
PCF85363A	X	2	I^2C	230	X	1	-	time stamp stopwatch RAM
PCF8523	X	2	I^2C	150	X	-	-	lowest pow operation,
PCF2123	X	1	SPI	100	-	-	-	lowest pow operation
PCF2127	X	1	I^2C and SPI	500	X	1 (3-level)	-	temperatur quartz built Byte RAM

Table 93. Selection of Real-Time Clocks*...continued*

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD}, typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special fea
PCF2127A	X	1	I^2C and SPI	500	X	1 (3-level)	-	temperatur quartz built Byte RAM
PCF2129	X	1	I^2C and SPI	500	X	1 (3-level)	-	temperatur quartz built
PCF2129A	X	1	I^2C and SPI	500	X	1 (3-level)	-	temperatur quartz built
PCA2129	X	1	I^2C and SPI	500	X	1 (3-level)	segment B, grade 3	temperatur quartz built
PCA21125	X	1	SPI	820	-	-	segment B, grade 1	high robust T_{amb}= -40 °
PCF2131	X	2	I^2C and SPI	60	X	4	-	temperatur quartz built
PCA2131	X	2	I^2C and SPI	106	X	4	segment B, grade 3	temperatur quartz built T_{amb}= -40 °

16 Abbreviations

Table 94. Abbreviations

Acronym	Description
AM	Ante Meridiem
BCD	Binary Coded Decimal
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
GPS	Global Positioning System
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LSB	Least Significant Bit
MCU	Microcontroller Unit
MM	Machine Model
MSB	Most Significant Bit
PM	Post Meridiem
POR	Power-On Reset
PORO	Power-On Reset Override
PPM	Parts Per Million
RC	Resistance-Capacitance
RTC	Real-Time Clock
SCL	Serial CLock line
SDA	Serial DAta line
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCXO	Temperature Compensated Xtal Oscillator
Xtal	crystal

17 References

[1] AN13203 Application and soldering information for the PCF2131 and PCA2131 RTC

[2] SOT1992-1_518 HLSON16; Reel pack; SMD, 13", packing information

[3] UM10204 I^2C-bus specification and user manual

[4] UM10569 Store and transport requirements

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

18 Revision history

Table 95. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2131 v.1.1	20211015	Product data sheet	-	PCF2131 v.1.0
Modifications:	• Table 90: Corrected reference to AN13203			
PCF2131 v.1.0	20210528	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

19 Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

19.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

I2C-bus — logo is a trademark of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Tables

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Figures

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Contents

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

© NXP B.V. 2021. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 15 October 2021
Document identifier: PCF2131

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Real Time Clock ***category:***

Click to view products by NXP ***manufacturer:***

Other Similar products are found below :

DS1302Z-LF 710029X 879047C 405800G PT7C43390LE RV-3029-C2-32.768k-OPTION-B-TB-QA RV-2123-C2-32.768k-20PPM-TA-QA RV-3029-C2-32.768k-OPTION-A-TB-QA RV-1805-C3-32.768k-2PPM-TA-QA RV-3029-C3-32.768k-OPTION-A-TB-QA RV-2123-C2-32.768kHz-20PPM-TA-QC RX-4035LC:B3 PURE SN RX-8564LC:B PURE SN RX-8803LCUB PURE SN BULK RX-8571LCB0 PURE SN BQ32002D RTC-8564JE MCP7940M-I/P DS3231SN#T&R DS1391U-18+ DS1347T+T&R RX-8564LC:B3 PURE SN DS1338Z-33+T RX-4571SA:B3 PURE SN DS1340U-33+T&R RX-8571LC:B3 PURE SN PCF8583T/5.518 S-35190A-J8T1U RTC-4543SAB RTC-72421A RTC-72423A RX-8803LC:UB3 PURE SN RX-8803SA:UB3 PURE SN S-35390A-T8T1 AB1815-T3 AB-RTCMC-32.768kHz-AIGZ-S7-T AB-RTCMC-32.768kHz-B5GA-S3-T AB-RTCMC-32.768kHz-B5ZE-S3-T AB-RTCMC-32.768kHz-EOA9-S3-D-B-T AB-RTCMC-32.768kHz-EOZ9-S3-D-B-T AB-RTCMC-32.768KHZ-EOZ9-S3-HAT AB-RTCMC-32.768KHZ-IBO5-S3-T AB-RTCMC-32.768kHz-ZIZE-S2-T DS1672U-33+ DS1372U+ DS1337U+T&R DS1340U-18+ DS1339BU+ DS1339AU+ DS1339U-2+