PCF8811

80 x 128 pixels matrix LCD driver

Rev. 6 — 10 February 2015 Product data sheet

1. General description

The PCF8811 is a low-power CMOS[1] LCD controller and driver. It is designed to drive a graphic display of 80 rows and 128 columns or of 79 rows, 128 columns, and an icon row of 128 symbols. All necessary functions for the display are provided in a single chip, including on-chip generation of the LCD supply and bias voltages. Therefore only a minimum of external components are required and power consumption is low. The PCF8811 can interface microcontrollers via a parallel bus, serial bus, or I^2C-bus interface.

For a selection of NXP LCD graphic drivers, see Table 44 on page 85.

2. Features and benefits

- Single-chip LCD controller and driver
- 80 row and 128 column outputs
- Display data RAM 80 × 128 bit
- 128 icons (in extended command set row 79 can be configured for displaying icons)
- Low power consumption; suitable for battery operated systems
- Interfaces:
  - 8-bit parallel
  - 3- or 4-line Serial Peripheral Interface (SPI)
  - High-speed I^2C-bus
- Configurable voltage multiplier generating LCD supply voltage V_{LCD}; an external V_{LCD} is also possible
- Linear temperature compensation of V_{LCD}:
  - 8 programmable temperature coefficients (extended command set)
  - one fixed temperature coefficient which can be set as default by OTP programming (basic command set)
- Generation of intermediate LCD bias voltage
- Oscillator requires no external components
- OTP calibration for V_{LCD} and accurate frame frequency
- External reset input pin
- External clock input possible
- Multiplex rate 1:16 to 1:80 selectable
  - in steps of 8 when icon row is not used
  - in steps of 16 when the icon row is used
- Logic supply voltage range V_{DD1} to V_{SS}:
  - 1.7 V to 3.3 V

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 24.

- High-voltage multiplier supply voltage range V_{DD2}, V_{DD3} to V_{SS}:
  - 1.8 V to 3.3 V
- Display supply voltage range V_{LCD} to V_{SS}:
  - 3 V to 9 V
- Programmable bottom row pins mirroring; for compatibility with both Tape Carrier Packages (TCP) and Chip-On-Glass (COG) applications (extended command set)
- Status read, which allows for chip recognition and content checking of some registers
- Start address line which allows, for instance, the scrolling of the displayed image
- Programmable display RAM pointers for variable display sizes
- Slim chip layout, suited for COG applications
- Temperature range: T_{amb} = −40 °C to +85 °C
- CMOS compatible inputs

3. Applications

- Automotive displays
- Telecommunication equipment
- Portable instruments
- Point-of-sale terminals
- Consumer healthcare devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8811U/2DA/1	-	chip with bumps in tray (not covered by Motif license agreement)	-
PCF8811MU/2DA/1	-	chip with bumps in tray (sold under license from Motif)	-

5. Block diagram

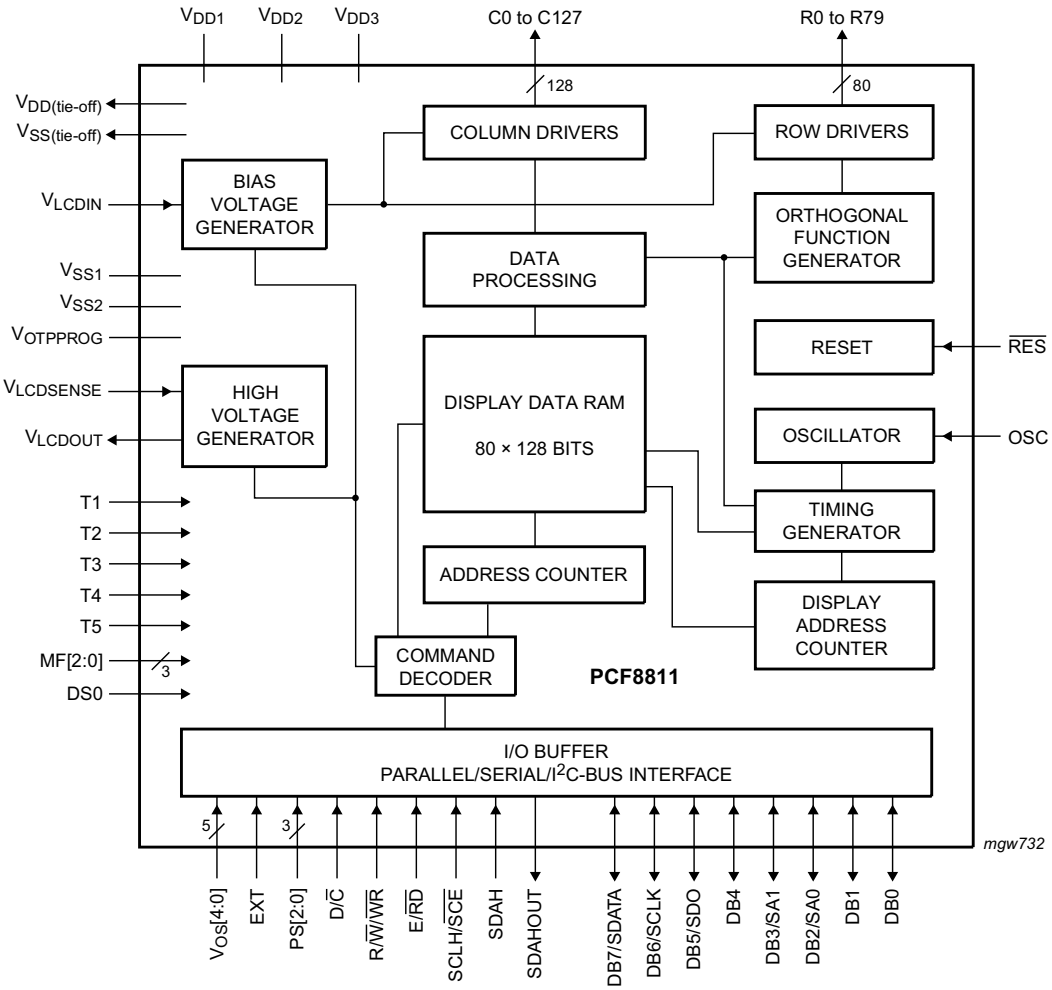
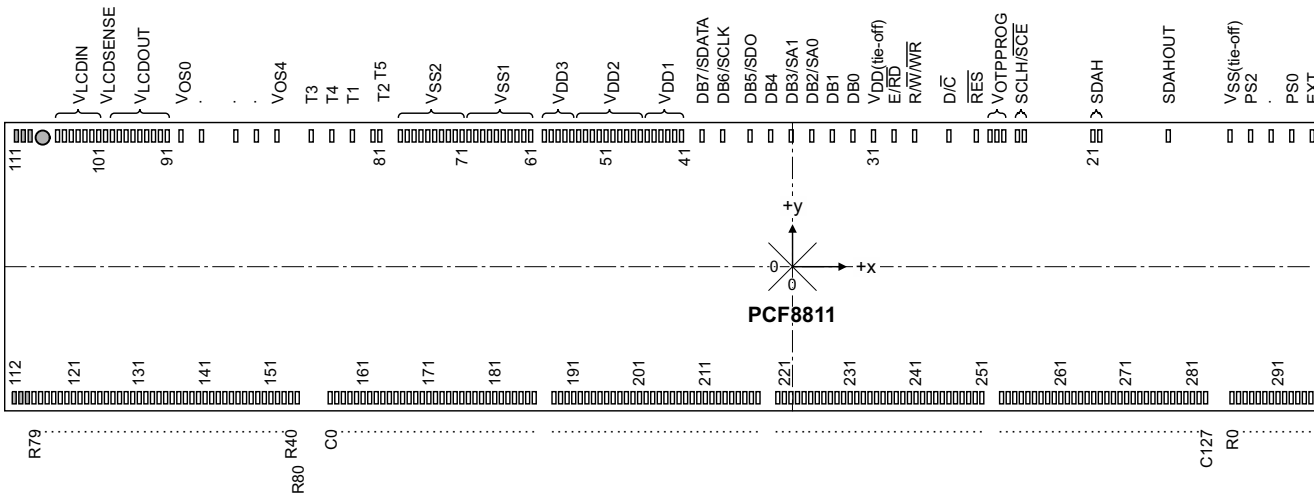


Fig 1. Block diagram of PCF8811

6. Pinning information

6.1 Pinning



Viewed from active side. Not drawn to scale.

$V_{SS(tie\text{-}off)}$ and $V_{DD(tie\text{-}off)}$ are used for local tie-offs (see Section 6.2.1).

Fig 2. Pin configuration for PCF8811

6.2 Pin description

Table 2. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
-	1	dummy_slanted
-	2	alignment mark
-	3 to 8	dummy
MF2 to MF0	9 to 11	manufacturer device ID input
DS0	12	device recognition input
OSC	13	oscillator input
EXT	14	extended command set input
PS0 to PS2	15 to 17	parallel/serial/I^2C-bus data selection input
$V_{SS(tie-off)}$	18	V_{SS} tie-off
SDAHOUT	19	I^2C-bus data output
SDAH	20, 21	I^2C-bus data input
SCLH/$\overline{SCE}$	22, 23	I^2C-bus clock input or chip enable, active LOW (6800 interface)
$V_{OTPPROG}$	24 to 26	supply voltage for OTP (can be combined with SCLH/$\overline{SCE}$)
$\overline{RES}$	27	external reset input
D/$\overline{C}$	28	data or command, active LOW input
R/$\overline{W}$/$\overline{WR}$	29	read or write, active LOW input (6800 interface)
E/$\overline{RD}$	30	clock enable or read, active LOW input (6800 interface)
$V_{DD(tie-off)}$	31	V_{DD} tie-off
DB0, DB1	32, 33	parallel data input/output
DB2/SA0	34	parallel data input/output or I^2C-bus slave address input
DB3/SA1	35	
DB4	36	parallel data input/output
DB5/SDO	37	parallel data input/output or serial data output
DB6/SCLK	38	parallel data input/output or serial clock input
DB7/SDATA	39	parallel data input/output or serial data input
V_{DD1}	40 to 45	supply voltage (logic)
V_{DD2}	46 to 55	supply voltage for the internal voltage multiplier
V_{DD3}	56 to 60	supply voltage for the internal voltage multiplier
V_{SS1}	61 to 70	ground
V_{SS2}	71 to 80	ground for voltage multiplier
T5	81	test pins
T2	82	
T1	83	
T4	84	
T3	85	

Table 2. Pin description *...continued*

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
V_{OS4}	86	V_{LCD} offset input pins
V_{OS3}	87	
V_{OS2}	88	
V_{OS1}	89	
V_{OS0}	90	
V_{LCDOUT}	91 to 99	voltage multiplier output
$V_{LCDSENSE}$	100	voltage multiplier regulation input
V_{LCDIN}	101 to 107	LCD supply voltage
-	108	alignment mark
-	109 to 114	dummy
R79 to R40	115 to 154	LCD row driver output
R80[1]	155	
C0 to C127	156 to 283	LCD column driver output
R0 to R39	284 to 323	LCD row driver output
-	324 to 333	dummy

[1] Duplicate of R79.

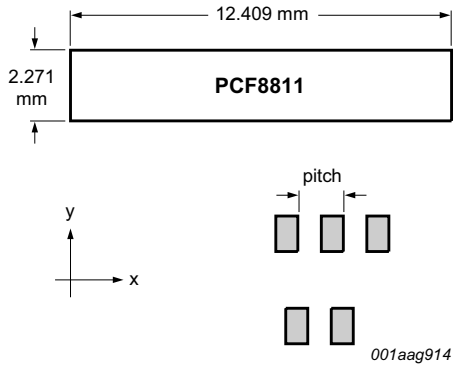
6.2.1 Tie-off pins

The PCF8811 has two tie-off pins:

- $V_{SS(tie-off)}$, pin 18, at V_{SS} potential
- $V_{DD(tie-off)}$, pin 31, at V_{DD} potential

The tie-off pins have been implemented to allow a one layer layout of the application while offering the possibility to connect, for example, the pins MF0 to MF2 and V_{OS0} to V_{OS4} to any desired combination of LOW (V_{SS} potential) and HIGH (V_{DD} potential) levels.

6.2.2 Bare die information



Dimension including saw lane. Wafer thickness (excluding bumps): 380 (±20) μm.

Fig 3. Chip dimensions

Table 3. Bump and pad dimensions

Pin	Row/Column side (μm)	Interface side (μm)
Bump dimensions	29.9 × 98.5 (±3)	32.2 × 93.5 (±3)
Pad dimension (aluminum)	42.84 × 105	50 × 100
Bump pitch	51.84 min	54.0 min

Table 4. Alignment marker position[1]

Pin	X (μm)	Y (μm)
2	5995	1017
108	−5904	1017

[1] For the position of each pin, see Table 5.

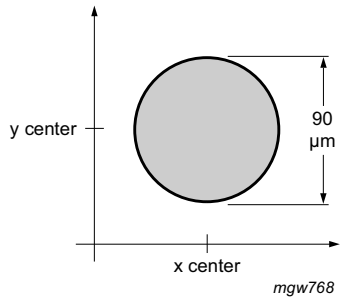


Fig 4. Alignment markers

Table 5. Bump locations

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
-	1	6092.00	1030.00	-	dummy_slanted
-	2	5995.00	1017.00	97	alignment mark
-	3	5876.00	1030.00	119	dummy
-	4	5822.00	1030.00	54	
-	5	5768.00	1030.00	54	
-	6	5714.00	1030.00	54	
-	7	5660.00	1030.00	54	
-	8	5390.00	1030.00	270	
MF2	9	5012.00	1030.00	378	manufacturer device ID input
MF1	10	4850.00	1030.00	162	
MF0	11	4688.00	1030.00	162	
DS0	12	4526.00	1030.00	162	device recognition input
OSC	13	4364.00	1030.00	162	oscillator input
EXT	14	4094.00	1030.00	270	extended command set input

Table 5. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
PS0	15	3932.00	1030.00	162	parallel/serial/I²C-bus data selection input
PS1	16	3770.00	1030.00	162	
PS2	17	3608.00	1030.00	162	
$V_{SS(tie-off)}$	18	3446.00	1030.00	162	for local tie-offs
SDAHOUT	19	2960.00	1030.00	486	I²C-bus data output
SDAH	20	2420.00	1030.00	540	I²C-bus data input
SDAH	21	2366.00	1030.00	54	
SCLH/$\overline{SCE}$	22	1826.00	1030.00	540	I²C-bus clock input or chip enable active LOW (6800 interface)
SCLH/$\overline{SCE}$	23	1772.00	1030.00	54	
$V_{OTPPROG}$	24	1664.00	1030.00	108	supply voltage for OTP (can be combined with SCLH/$\overline{SCE}$)
$V_{OTPPROG}$	25	1610.00	1030.00	54	
$V_{OTPPROG}$	26	1556.00	1030.00	54	
$\overline{RES}$	27	1448.00	1030.00	108	external reset input
D/$\overline{C}$	28	1232.00	1030.00	216	data or command active LOW input
R/$\overline{W}$/$\overline{WR}$	29	962.00	1030.00	270	read or write active LOW input (6800 interface)
E/$\overline{RD}$	30	800.00	1030.00	162	clock enable or read active LOW input (6800 interface)
$V_{DD(tie-off)}$	31	638.00	1030.00	162	for local tie-offs
DB0	32	476.00	1030.00	162	parallel data input/output
DB1	33	314.00	1030.00	162	
DB2/SA0	34	152.00	1030.00	162	parallel data input/output or I²C-bus slave address input
DB3/SA1	35	−10.00	1030.00	162	
DB4	36	−172.00	1030.00	162	parallel data input/output
DB5/SDO	37	−334.00	1030.00	162	parallel data input/output or serial data output
DB6/SCLK	38	−550.00	1030.00	216	parallel data input/output or serial clock input
DB7/SDATA	39	−712.00	1030.00	162	parallel data input/output or serial data input
V_{DD1}	40	−874.00	1030.00	162	supply voltage (logic)
V_{DD1}	41	−928.00	1030.00	54	
V_{DD1}	42	−982.00	1030.00	54	
V_{DD1}	43	−1036.00	1030.00	54	
V_{DD1}	44	−1090.00	1030.00	54	
V_{DD1}	45	−1144.00	1030.00	54	

Table 5. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
V_{DD2}	46	−1198.00	1030.00	54	supply voltage for the internal voltage multiplier
V_{DD2}	47	−1252.00	1030.00	54	
V_{DD2}	48	−1306.00	1030.00	54	
V_{DD2}	49	−1360.00	1030.00	54	
V_{DD2}	50	−1414.00	1030.00	54	
V_{DD2}	51	−1468.00	1030.00	54	
V_{DD2}	52	−1522.00	1030.00	54	
V_{DD2}	53	−1576.00	1030.00	54	
V_{DD2}	54	−1630.00	1030.00	54	
V_{DD2}	55	−1684.00	1030.00	54	
V_{DD3}	56	−1738.00	1030.00	54	supply voltage for the internal voltage multiplier
V_{DD3}	57	−1792.00	1030.00	54	
V_{DD3}	58	−1846.00	1030.00	54	
V_{DD3}	59	−1900.00	1030.00	54	
V_{DD3}	60	−1954.00	1030.00	54	
V_{SS1}	61	−2062.00	1030.00	108	ground
V_{SS1}	62	−2116.00	1030.00	54	
V_{SS1}	63	−2170.00	1030.00	54	
V_{SS1}	64	−2224.00	1030.00	54	
V_{SS1}	65	−2278.00	1030.00	54	
V_{SS1}	66	−2332.00	1030.00	54	
V_{SS1}	67	−2386.00	1030.00	54	
V_{SS1}	68	−2440.00	1030.00	54	
V_{SS1}	69	−2494.00	1030.00	54	
V_{SS1}	70	−2548.00	1030.00	54	
V_{SS2}	71	−2602.00	1030.00	54	ground for voltage multiplier
V_{SS2}	72	−2656.00	1030.00	54	
V_{SS2}	73	−2710.00	1030.00	54	
V_{SS2}	74	−2764.00	1030.00	54	
V_{SS2}	75	−2818.00	1030.00	54	
V_{SS2}	76	−2872.00	1030.00	54	
V_{SS2}	77	−2926.00	1030.00	54	
V_{SS2}	78	−2980.00	1030.00	54	
V_{SS2}	79	−3034.00	1030.00	54	
V_{SS2}	80	−3088.00	1030.00	54	
T5	81	−3250.00	1030.00	162	test input 5
T2	82	−3304.00	1030.00	54	test input 2
T1	83	−3466.00	1030.00	162	test input 1

Table 5. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
T4	84	−3628.00	1030.00	162	test input 4
T3	85	−3790.00	1030.00	162	test input 3
V_{OS4}	86	−4060.00	1030.00	270	V_{LCD} offset input pin 4
V_{OS3}	87	−4222.00	1030.00	162	V_{LCD} offset input pin 3
V_{OS2}	88	−4384.00	1030.00	162	V_{LCD} offset input pin 2
V_{OS1}	89	−4654.00	1030.00	270	V_{LCD} offset input pin 1
V_{OS0}	90	−4816.00	1030.00	162	V_{LCD} offset input pin 0
V_{LCDOUT}	91	−4924.00	1030.00	108	voltage multiplier output
V_{LCDOUT}	92	−4978.00	1030.00	54	
V_{LCDOUT}	93	−5032.00	1030.00	54	
V_{LCDOUT}	94	−5086.00	1030.00	54	
V_{LCDOUT}	95	−5140.00	1030.00	54	
V_{LCDOUT}	96	−5194.00	1030.00	54	
V_{LCDOUT}	97	−5248.00	1030.00	54	
V_{LCDOUT}	98	−5302.00	1030.00	54	
V_{LCDOUT}	99	−5356.00	1030.00	54	
$V_{LCDSENSE}$	100	−5410.00	1030.00	54	voltage multiplier regulation input
V_{LCDIN}	101	−5464.00	1030.00	54	LCD supply voltage
V_{LCDIN}	102	−5518.00	1030.00	54	
V_{LCDIN}	103	−5572.00	1030.00	54	
V_{LCDIN}	104	−5626.00	1030.00	54	
V_{LCDIN}	105	−5680.00	1030.00	54	
V_{LCDIN}	106	−5734.00	1030.00	54	
V_{LCDIN}	107	−5788.00	1030.00	54	
-	108	−5904.00	1017.00	116	alignment mark
-	109	−6004.00	1030.00	100	dummy
-	110	−6058.00	1030.00	54	
-	111	−6112.00	1030.00	54	
-	112	−6129.24	−1032.50	-	
-	113	−6077.40	−1032.50	51.84	
-	114	−6025.56	−1032.50	51.84	
R79	115	−5973.72	−1032.50	51.84	LCD row driver output (R79 is the icon row when the icon row is enabled)

Table 5. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
R78	116	−5921.88	−1032.50	51.84	LCD row driver output
R77	117	−5870.04	−1032.50	51.84	
R76	118	−5818.20	−1032.50	51.84	
R75	119	−5766.36	−1032.50	51.84	
R74	120	−5714.52	−1032.50	51.84	
R73	121	−5662.68	−1032.50	51.84	
R72	122	−5610.84	−1032.50	51.84	
R71	123	−5559.00	−1032.50	51.84	
R70	124	−5507.16	−1032.50	51.84	
R69	125	−5455.32	−1032.50	51.84	
R68	126	−5403.48	−1032.50	51.84	
R67	127	−5351.64	−1032.50	51.84	
R66	128	−5299.80	−1032.50	51.84	
R65	129	−5247.96	−1032.50	51.84	
R64	130	−5196.12	−1032.50	51.84	
R63	131	−5144.28	−1032.50	51.84	
R62	132	−5092.44	−1032.50	51.84	
R61	133	−5040.60	−1032.50	51.84	
R60	134	−4988.76	−1032.50	51.84	
R59	135	−4936.92	−1032.50	51.84	
R58	136	−4885.08	−1032.50	51.84	
R57	137	−4833.24	−1032.50	51.84	
R56	138	−4781.40	−1032.50	51.84	
R55	139	−4729.56	−1032.50	51.84	
R54	140	−4677.72	−1032.50	51.84	
R53	141	−4625.88	−1032.50	51.84	
R52	142	−4574.04	−1032.50	51.84	
R51	143	−4522.20	−1032.50	51.84	
R50	144	−4470.36	−1032.50	51.84	
R49	145	−4418.52	−1032.50	51.84	
R48	146	−4366.68	−1032.50	51.84	
R47	147	−4314.84	−1032.50	51.84	
R46	148	−4263.00	−1032.50	51.84	
R45	149	−4211.16	−1032.50	51.84	

Table 5. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
R44	150	−4159.32	−1032.50	51.84	LCD row driver output
R43	151	−4107.48	−1032.50	51.84	
R42	152	−4055.64	−1032.50	51.84	
R41	153	−4003.80	−1032.50	51.84	
R40	154	−3951.96	−1032.50	51.84	
R80	155	−3900.12	−1032.50	51.84	duplicate of R79
C0	156	−3640.92	−1032.50	259.2	LCD column driver output
C1	157	−3589.08	−1032.50	51.84	
C2	158	−3537.24	−1032.50	51.84	
C3	159	−3485.40	−1032.50	51.84	
C4	160	−3433.56	−1032.50	51.84	
C5	161	−3381.72	−1032.50	51.84	
C6	162	−3329.88	−1032.50	51.84	
C7	163	−3278.04	−1032.50	51.84	
C8	164	−3226.20	−1032.50	51.84	
C9	165	−3174.36	−1032.50	51.84	
C10	166	−3122.52	−1032.50	51.84	
C11	167	−3070.68	−1032.50	51.84	
C12	168	−3018.84	−1032.50	51.84	
C13	169	−2967.00	−1032.50	51.84	
C14	170	−2915.16	−1032.50	51.84	
C15	171	−2863.32	−1032.50	51.84	
C16	172	−2811.48	−1032.50	51.84	
C17	173	−2759.64	−1032.50	51.84	
C18	174	−2707.80	−1032.50	51.84	
C19	175	−2655.96	−1032.50	51.84	
C20	176	−2604.12	−1032.50	51.84	
C21	177	−2552.28	−1032.50	51.84	
C22	178	−2500.44	−1032.50	51.84	
C23	179	−2448.60	−1032.50	51.84	
C24	180	−2396.76	−1032.50	51.84	
C25	181	−2344.92	−1032.50	51.84	
C26	182	−2293.08	−1032.50	51.84	
C27	183	−2241.24	−1032.50	51.84	
C28	184	−2189.40	−1032.50	51.84	
C29	185	−2137.56	−1032.50	51.84	
C30	186	−2085.72	−1032.50	51.84	

Table 5. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
C31	187	−2033.88	−1032.50	51.84	LCD column driver output
C32	188	−1878.36	−1032.50	155.52	
C33	189	−1826.52	−1032.50	51.84	
C34	190	−1774.68	−1032.50	51.84	
C35	191	−1722.84	−1032.50	51.84	
C36	192	−1671.00	−1032.50	51.84	
C37	193	−1619.16	−1032.50	51.84	
C38	194	−1567.32	−1032.50	51.84	
C39	195	−1515.48	−1032.50	51.84	
C40	196	−1463.64	−1032.50	51.84	
C41	197	−1411.80	−1032.50	51.84	
C42	198	−1359.16	−1032.50	52.64	
C43	199	−1308.12	−1032.50	51.04	
C44	200	−1256.28	−1032.50	51.84	
C45	201	−1204.44	−1032.50	51.84	
C46	202	−1152.60	−1032.50	51.84	
C47	203	−1100.76	−1032.50	51.84	
C48	204	−1048.92	−1032.50	51.84	
C49	205	−997.08	−1032.50	51.84	
C50	206	−945.24	−1032.50	51.84	
C51	207	−893.40	−1032.50	51.84	
C52	208	−841.56	−1032.50	51.84	
C53	209	−789.72	−1032.50	51.84	
C54	210	−737.88	−1032.50	51.84	
C55	211	−686.04	−1032.50	51.84	
C56	212	−634.20	−1032.50	51.84	
C57	213	−582.36	−1032.50	51.84	
C58	214	−530.52	−1032.50	51.84	
C59	215	−478.68	−1032.50	51.84	
C60	216	−426.84	−1032.50	51.84	
C61	217	−375.00	−1032.50	51.84	
C62	218	−323.16	−1032.50	51.84	
C63	219	−271.32	−1032.50	51.84	
C64	220	−115.80	−1032.50	155.52	
C65	221	−63.96	−1032.50	51.84	
C66	222	−12.12	−1032.50	51.84	
C67	223	39.72	−1032.50	51.84	
C68	224	91.56	−1032.50	51.84	
C69	225	143.40	−1032.50	51.84	

Table 5. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
C70	226	195.24	−1032.50	51.84	LCD column driver output
C71	227	247.08	−1032.50	51.84	
C72	228	298.92	−1032.50	51.84	
C73	229	350.76	−1032.50	51.84	
C74	230	402.60	−1032.50	51.84	
C75	231	454.44	−1032.50	51.84	
C76	232	506.28	−1032.50	51.84	
C77	233	558.12	−1032.50	51.84	
C78	234	609.96	−1032.50	51.84	
C79	235	661.80	−1032.50	51.84	
C80	236	713.64	−1032.50	51.84	
C81	237	765.48	−1032.50	51.84	
C82	238	817.32	−1032.50	51.84	
C83	239	869.16	−1032.50	51.84	
C84	240	921.00	−1032.50	51.84	
C85	241	972.84	−1032.50	51.84	
C86	242	1024.68	−1032.50	51.84	
C87	243	1076.52	−1032.50	51.84	
C88	244	1128.36	−1032.50	51.84	
C89	245	1180.20	−1032.50	51.84	
C90	246	1232.04	−1032.50	51.84	
C91	247	1283.88	−1032.50	51.84	
C92	248	1335.72	−1032.50	51.84	
C93	249	1387.56	−1032.50	51.84	
C94	250	1439.40	−1032.50	51.84	
C95	251	1491.24	−1032.50	51.84	
C96	252	1646.76	−1032.50	155.52	
C97	253	1698.60	−1032.50	51.84	
C98	254	1750.44	−1032.50	51.84	
C99	255	1802.28	−1032.50	51.84	
C100	256	1854.12	−1032.50	51.84	
C101	257	1905.96	−1032.50	51.84	
C102	258	1957.80	−1032.50	51.84	
C103	259	2009.64	−1032.50	51.84	
C104	260	2061.48	−1032.50	51.84	
C105	261	2113.32	−1032.50	51.84	
C106	262	2165.16	−1032.50	51.84	
C107	263	2217.00	−1032.50	51.84	
C108	264	2268.84	−1032.50	51.84	

Table 5. Bump locations *...continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
C109	265	2320.68	−1032.50	51.84	LCD column driver output
C110	266	2372.52	−1032.50	51.84	
C111	267	2424.36	−1032.50	51.84	
C112	268	2476.20	−1032.50	51.84	
C113	269	2528.04	−1032.50	51.84	
C114	270	2579.88	−1032.50	51.84	
C115	271	2631.72	−1032.50	51.84	
C116	272	2683.56	−1032.50	51.84	
C117	273	2735.40	−1032.50	51.84	
C118	274	2787.24	−1032.50	51.84	
C119	275	2839.08	−1032.50	51.84	
C120	276	2890.92	−1032.50	51.84	
C121	277	2942.76	−1032.50	51.84	
C122	278	2994.60	−1032.50	51.84	
C123	279	3046.44	−1032.50	51.84	
C124	280	3098.28	−1032.50	51.84	
C125	281	3150.12	−1032.50	51.84	
C126	282	3201.96	−1032.50	51.84	
C127	283	3253.80	−1032.50	51.84	
R0	284	3461.16	−1032.50	207.36	LCD row driver output
R1	285	3513.00	−1032.50	51.84	
R2	286	3564.84	−1032.50	51.84	
R3	287	3616.68	−1032.50	51.84	
R4	288	3668.52	−1032.50	51.84	
R5	289	3720.36	−1032.50	51.84	
R6	290	3772.20	−1032.50	51.84	
R7	291	3824.04	−1032.50	51.84	
R8	292	3875.88	−1032.50	51.84	
R9	293	3927.72	−1032.50	51.84	
R10	294	3979.56	−1032.50	51.84	
R11	295	4031.40	−1032.50	51.84	
R12	296	4083.24	−1032.50	51.84	
R13	297	4135.08	−1032.50	51.84	
R14	298	4186.92	−1032.50	51.84	
R15	299	4238.76	−1032.50	51.84	
R16	300	4290.60	−1032.50	51.84	
R17	301	4342.44	−1032.50	51.84	

Table 5. Bump locations *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip, see Figure 2. Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Bump	Location		Pitch	Description
		X (μm)	Y (μm)	X (μm)	
R18	302	4394.28	−1032.50	51.84	LCD row driver output
R19	303	4446.12	−1032.50	51.84	
R20	304	4497.96	−1032.50	51.84	
R21	305	4549.80	−1032.50	51.84	
R22	306	4601.64	−1032.50	51.84	
R23	307	4653.48	−1032.50	51.84	
R24	308	4705.32	−1032.50	51.84	
R25	309	4757.16	−1032.50	51.84	
R26	310	4809.00	−1032.50	51.84	
R27	311	4860.84	−1032.50	51.84	
R28	312	4912.68	−1032.50	51.84	
R29	313	4964.52	−1032.50	51.84	
R30	314	5016.36	−1032.50	51.84	
R31	315	5068.20	−1032.50	51.84	
R32	316	5120.04	−1032.50	51.84	
R33	317	5171.88	−1032.50	51.84	
R34	318	5223.72	−1032.50	51.84	
R35	319	5275.56	−1032.50	51.84	
R36	320	5327.40	−1032.50	51.84	
R37	321	5379.24	−1032.50	51.84	
R38	322	5431.08	−1032.50	51.84	
R39	323	5482.92	−1032.50	51.84	
-	324	5638.44	−1032.50	155.52	dummy
-	325	5690.28	−1032.50	51.84	
-	326	5742.12	−1032.50	51.84	
-	327	5793.96	−1032.50	51.84	
-	328	5845.80	−1032.50	51.84	
-	329	5897.64	−1032.50	51.84	
-	330	5949.48	−1032.50	51.84	
-	331	6001.32	−1032.50	51.84	
-	332	6053.16	−1032.50	51.84	
-	333	6105.00	−1032.50	51.84	

7. Functional description

7.1 Pin functions

7.1.1 R0 to R80: row driver outputs

These pins output the display row signals. R79 is the icon row when the icon row is enabled. R80 is the duplicate of R79.

7.1.2 C0 to C127: column driver signals

These pins output the display column signals.

7.1.3 V_{SS1} and V_{SS2}: negative power supply rails

V_{SS2} is for the voltage multiplier. These 2 supply rails must be connected together.

7.1.4 V_{DD1} to V_{DD3}: positive power supply rails

- V_{DD2} and V_{DD3} are the supply voltages for the internal voltage multiplier
- V_{DD2} and V_{DD3} have the same voltage and may be connected together outside of the chip, see Section 18
- V_{DD1} is used as supply for the rest of the chip
- V_{DD1} can be connected together with V_{DD2} and V_{DD3}
- If the internal voltage multiplier is not used, then pins V_{DD2} and V_{DD3} must be connected to V_{DD1}, see Section 18
- If V_{DD1}, V_{DD2} and V_{DD3} are connected together, care must be taken with respect to the supply voltage range, see Section 15

7.1.5 $V_{OTPPROG}$: OTP power supply

Supply voltage for the OTP programming, see Section 19.

In order to reduce the external connections, $V_{OTPPROG}$ can be combined with the SCLH/$\overline{SCE}$ pin.

7.1.6 V_{LCDOUT}, V_{LCDIN}, and $V_{LCDSENSE}$: LCD power supply

Positive power supply for the liquid crystal display.

- If the internal V_{LCD} multiplier is used, then all three inputs must be connected together
- If V_{LCD} multiplier is disabled and an external voltage is supplied to V_{LCDIN}, then V_{LCDOUT} must be left open-circuit and $V_{LCDSENSE}$ must be connected to V_{LCDIN}
- V_{DD2} and V_{DD3} should be applied according to the specified voltage range
- If the PCF8811 is in power-save mode, the external LCD supply voltage can be switched off

7.1.7 T1 to T5: test pins

T1, T2 and T5 must be connected to V_{SS}. T3 and T4 must be left open-circuit. These test pins are not accessible to the user.

7.1.8 MF2 to MF0

MF2 to MF0 are device manufacturer ID pins. These pins are meant to encode an IC supplier or a module maker. A module maker may want to be able to read which IC-supplier is on a module. Similarly they can be used if various suppliers for identical modules are used in order to identify the module supplier. By reading the values for MF2 to MF0, the manufacturer ID can be detected. Any possible combination can be used.

7.1.9 DS0

The device recognition pin, DS0, allows configuring the PCF8811 for 64 rows or 80 rows, see Table 6. Other configurations of raws can be done by command, see Table 12. The status of the DS0 pin can be read back by the status register, see Table 12.

Table 6. Device recognition

DS0 pin connected to	Description
V_{SS1}	64-row driver
V_{DD1}	80-row driver

7.1.10 V_{OS4} to V_{OS0}

These 5 input pins enable the calibration of the offset of the programmed V_{LCD}, see Equation 4 and Equation 5. V_{OS4} to V_{OS0} must be connected to V_{DD1} or V_{SS1}.

7.1.11 EXT: extended command set

Input to select the basic command set or the extended command set. Must be connected on the module to have only one command set enabled, see Table 7.

Table 7. Command set selection

Pin	Level	Description
EXT	LOW (V_{SS1})	basic command set
	HIGH (V_{DD1})	extended command set

Remark: NXP Semiconductors recommends that the extended command set is used.

7.1.12 PS0, PS1, and PS2

Parallel, serial or I^2C-bus interface selection, see Table 8.

Table 8. Interface selection

PS[2:0]	Interface
000	3-line SPI
001	4-line SPI
010	no operation
011	6800 parallel interface
100 or 110	I^2C-bus interface
101 or 111	3-line serial interface

7.1.13 D/$\overline{C}$

Input to select either data or command input (see Table 9, Section 10.1.1 and Section 10.1.2). Not used for the 3-line serial interface, 3-line SPI and I^2C-bus interface. When not used, it must be connected to V_{DD1} or V_{SS1}.

7.1.14 R/$\overline{W}$/$\overline{WR}$

Input to select read or write mode when the 6800 parallel interface is selected. Not used in the serial and I^{2}C-bus mode. When not used, it must be connected to V_{DD1} or V_{SS1}.

7.1.15 E/$\overline{RD}$

E is the clock enable input for the 6800 parallel bus. Not used in the serial or I^{2}C-bus interface. When not used, it must be connected to V_{DD1} or V_{SS1}.

7.1.16 SCLH/$\overline{SCE}$

Input to select the chip and so allowing data or commands to be clocked in. Or input for the serial clock line when the I^{2}C-bus interface is selected.

7.1.17 SDAH

I^{2}C-bus serial data input. When not used, it must be connected to V_{DD1} or V_{SS1}.

7.1.18 SDAHOUT

SDAHOUT is the serial data acknowledge output for the I^{2}C-bus interface.

- By connecting SDAHOUT to SDAH externally, the SDAH line becomes fully I^{2}C-bus compatible
- The acknowledge output is separated from the serial data line due to the following reasons:
  - In COG applications, the track resistance from the SDAHOUT pin to the system SDAH line can be significant. A potential divider is generated by the bus pull-up resistor and the ITO track resistance
  - It is possible that during the acknowledge cycle, the PCF8811 is not able to create a valid LOW level
  - By splitting the SDAH input from the SDAHOUT output, the device could be used in a mode that ignores the acknowledge bit
  - In COG applications, where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAHOUT pin to the system SDAH line to guarantee a valid LOW level
- When not used, it must be connected to V_{DD1} or V_{SS1}

7.1.19 DB7 to DB0

These input/output lines are used by several interfaces as described below. When not used in the serial interface or the I^{2}C-bus, they must be connected to V_{DD1} or V_{SS1}.

7.1.19.1 DB7 to DB0 (parallel interface)

8-bit bidirectional bus. DB7 is the MSB.

7.1.19.2 DB7, DB6 and DB5 (serial interface)

- DB7 is used for serial input data (SDATA) when the serial interface is selected
- DB6 (SCLK) is used for the serial input clock when the serial interface is selected
- DB5 is used as the serial output of the serial interface (SDO)

7.1.19.3 DB3 and DB2 (I^2C-bus interface)

DB3 and DB2 are respectively the SA1 and SA0 inputs when the I^2C-bus is selected. DB3 and DB2 can be used so that up to four PCF8811s can be distinguished on one I^2C-bus.

7.1.20 OSC: oscillator

- When the on-chip oscillator is used, this input must be connected to V_{DD1}
- If an external clock signal is used, it is connected to this input
- If the oscillator and an external clock are both inhibited by connecting the OSC pin to V_{SS1}, the display is not clocked and may be left in a Direct Current (DC) state. To avoid a DC on the display, the chip should always be put into power-down mode before stopping the clock

7.1.21 $\overline{RES}$: reset

This signal resets the device and must be applied to initialize the chip properly. The signal is active LOW.

7.2 Block diagram functions

See Figure 1 for the block diagram layout.

7.2.1 Address counter

The address counter assigns addresses to the display data RAM for writing. The X address X[6:0] and the Y address Y[3:0] are set separately.

7.2.2 Display data RAM

The PCF8811 contains an 80 × 128-bit static RAM which stores the display data.

- The RAM is divided into 10 banks of 128 bytes (10 × 8 × 128 bit)
- The icon row (when enabled) is always row 79 and located in bank 9
- During RAM access, data is transferred to the RAM via the parallel interface, serial interface or I^2C-bus interface
- There is a direct correspondence between the X address and the column output number

7.2.3 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

7.2.4 Display address counter

The display content is generated by reading out the RAM content for 2, 4, or 8 rows simultaneously, depending on the selected display size. This content is processed with the corresponding set of 2, 4, or 8 orthogonal functions and so generates the signals for switching the pixels in the display on or off according to the RAM content.

Bit MP (see Table 19) allows configuration of the p value. The p value defines the number of rows which are simultaneously selected, see Table 25. It is possible to set the p value for the display sizes 64 and 80 manually to p = 4.

7.2.5 Display status

The display status (display on/off, normal display/all dots on and normal/inverse video) is set by the bits DON, DAL and E in the command display control, see Table 13.

7.2.6 LCD row and column drivers

The PCF8811 contains 80 row and 128 column drivers, which connect the appropriate LCD bias voltages in sequence to the display and in accordance with the data to be displayed.

8. Addressing

Data is written in bytes to the RAM matrix of the PCF8811 as shown in Figure 5. The display RAM has a matrix of 80 × 128 bits. The columns are addressed by the address pointer. The address ranges are: X = 0 to 127 (111 1111), Y = 0 to 9 (1001). The Y address represents the bank number. The effective X and Y addresses are programmed in such an order to use the PCF8811 with different display sizes without additional loading of the microprocessor. Addresses outside these ranges are not allowed. The icon row, when enabled, is always row 79 and therefore located in bank 9.

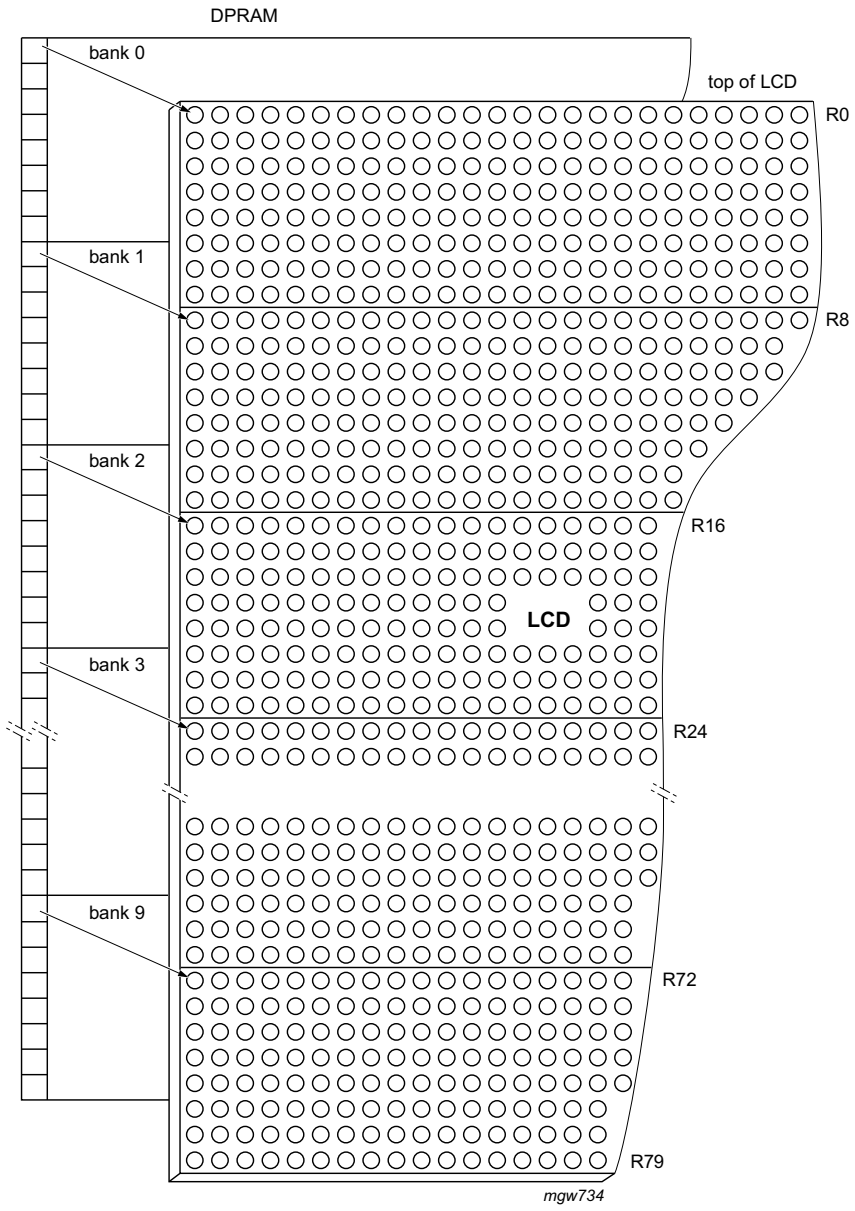


Fig 5. DDRAM to display mapping

8.1 Display data RAM structure

The mode for storing data into the data RAM depends on the selected command set.

8.1.1 Basic command set

After a write operation, the column address counter (X address) auto-increments by one, and wraps to zero after the last column is written. The number of columns (X address) after which the wrap-around must occur can be programmed.

The Y address counter does not auto-increment in the basic command set. The counter stops when a complete bank has been written to. In this case, the Y address counter must be set; for Y address, see Table 12. To write the next bank, see Figure 6.

When only a part of the RAM is used, both X (X_{max}) and Y (Y_{max}) addresses can be set.

The data order in the basic command set is as defined in Figure 6.

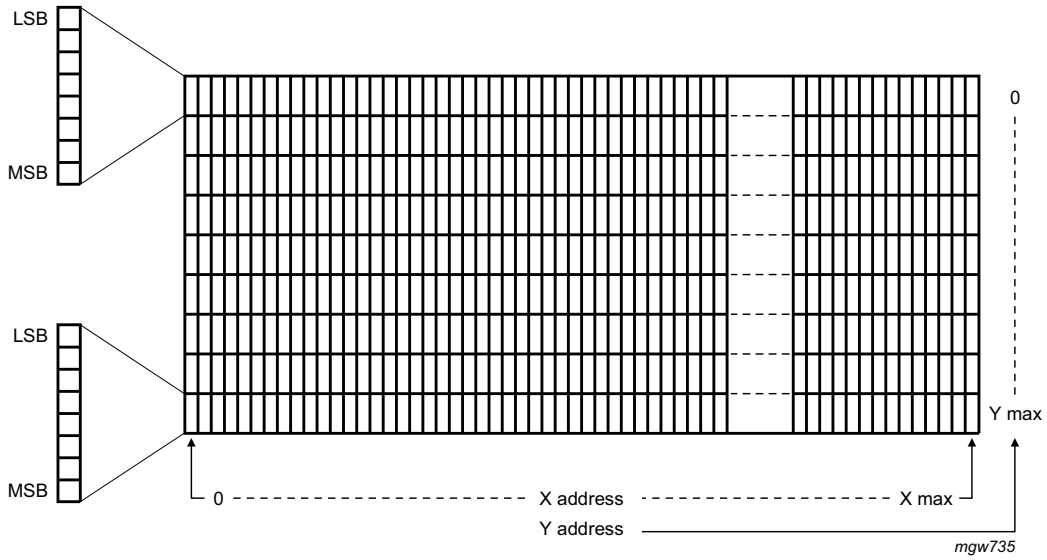


Fig 6. Sequence of writing data bytes into the RAM (basic command set)

8.1.2 Extended command set

8.1.2.1 Horizontal/vertical addressing

Two different address modes are possible with the extended command set: horizontal address mode and vertical address mode.

In the horizontal address mode (V = 0) the X address increments after each byte. After the last X address, X wraps around to 0 and Y increments to address the next row, see Figure 7. The number of columns (last X address) after which the wrap-around must occur can be programmed, see X_{max} and Y_{max} in Table 12 and Table 13. In Figure 7 it can be seen that the X address is programmed as 127, and the Y address is programmed as 9. With X_{max} and Y_{max}, the X and Y addresses can be programmed while the whole RAM is not being used.

In the vertical addressing mode (V = 1) the Y address increments after each byte. After the last Y address (Y = 9), Y wraps around to 0 and X increments to address the next column, see Figure 8. The last Y address, after which Y wraps to 0, can be programmed. In Figure 8 it can be seen that the X address is programmed as 127, and the Y address is programmed as 9. With X_{max} and Y_{max}, the X and Y addresses can be programmed while the whole RAM is not being used.

After the very last address, the address pointers wrap around to address X = 0 and Y = 0 in both horizontal and vertical addressing modes.

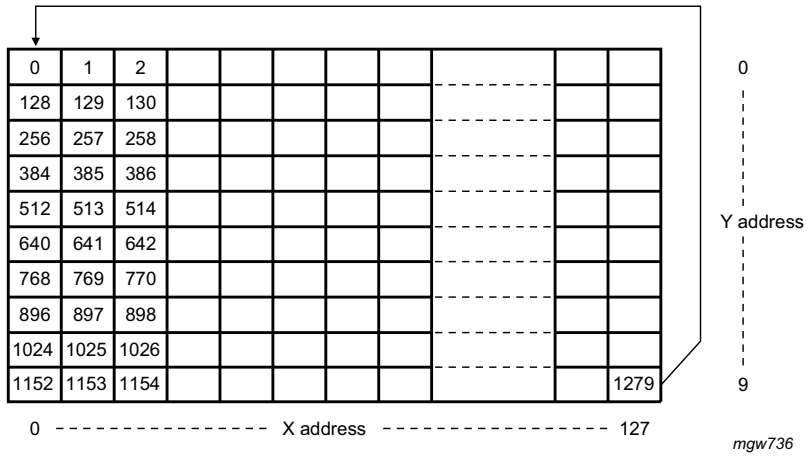


Fig 7. Sequence of writing data bytes into the RAM with horizontal addressing; V = 0 (extended command set)

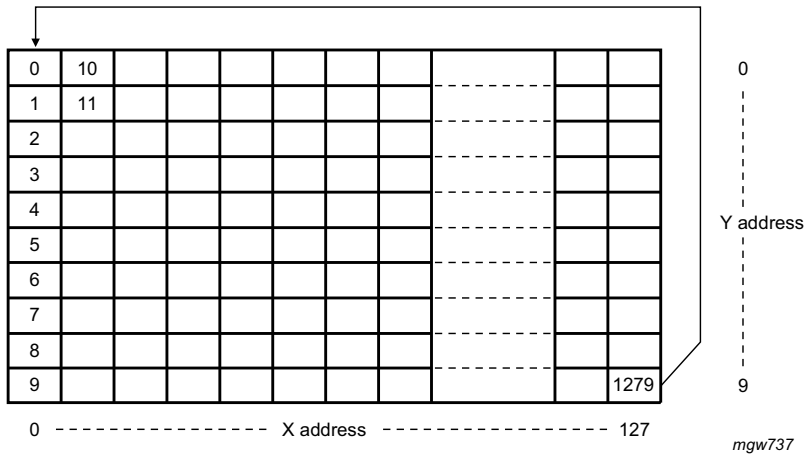


Fig 8. Sequence of writing data bytes into the RAM with vertical addressing; V = 1 (extended command set)

8.1.2.2 Data order

The data order bit (DOR, see Table 12 and Table 19) defines the bit order (LSB or MSB on top) for writing into the RAM, see Figure 9 and Figure 10. This feature is only available in the extended command set.

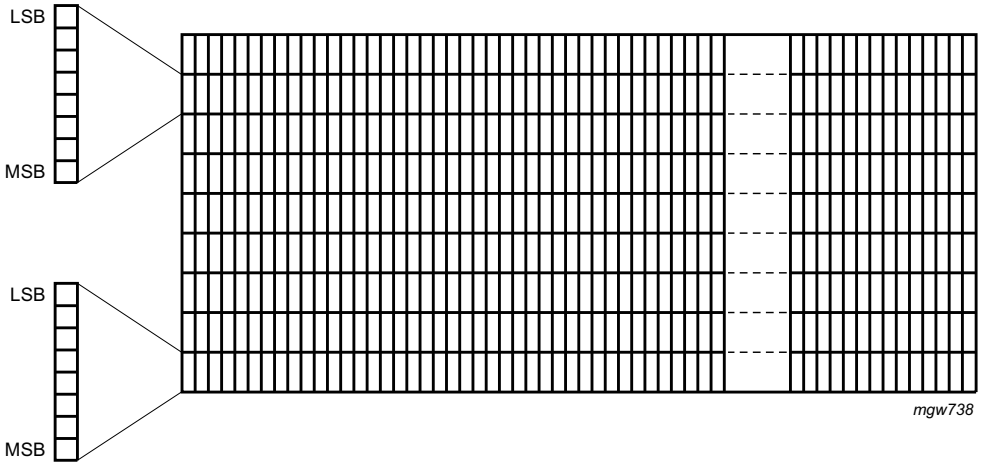


Fig 9. RAM byte organization, if DOR = 0 (extended command set)

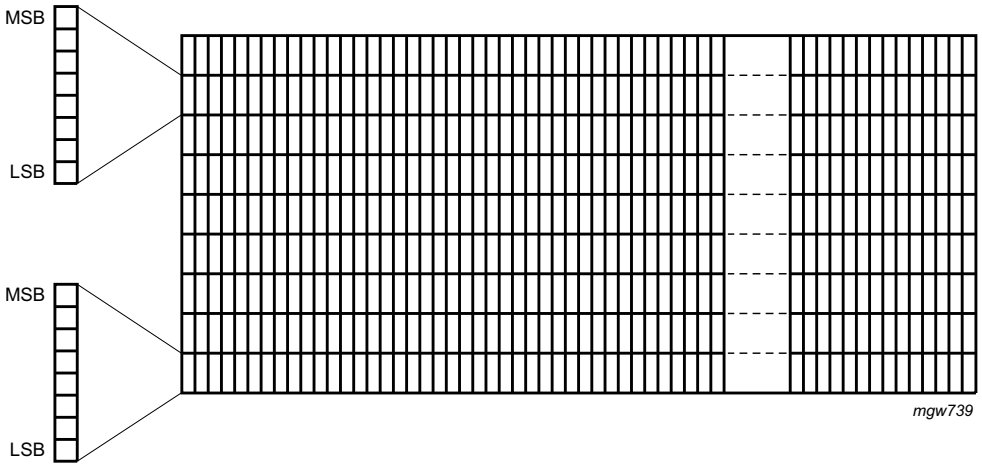


Fig 10. RAM byte organization, if DOR = 1 (extended command set)

8.1.2.3 Features available in both command sets

Mirror X (MX): The MX bit (see Table 12, Table 13 and Section 12.5.1) allows horizontal mirroring: when MX = 1, the X address space is mirrored; the address X = 0 is then located at the right side (X_{max}) of the display, see Figure 11. When MX = 0, the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display, see Figure 12.

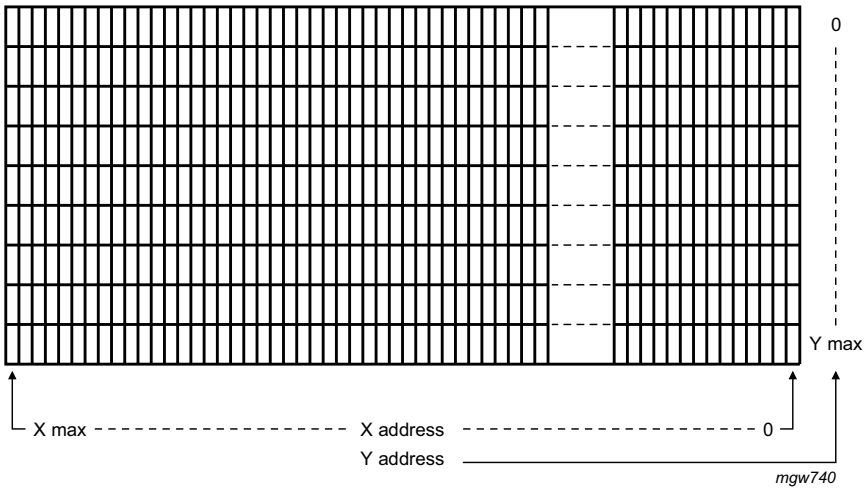


Fig 11. RAM format addressing; MX = 1 (both command sets)

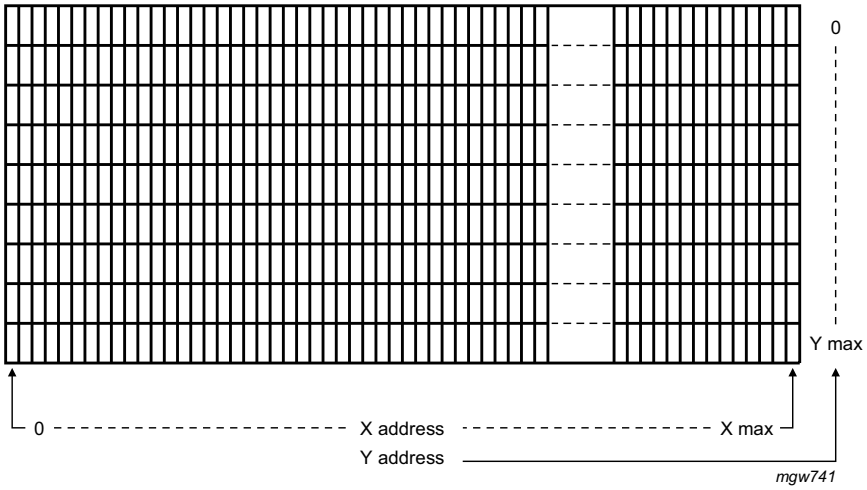


Fig 12. RAM format addressing; MX = 0 (both command sets)

Mirror Y (MY): The MY bit (see Table 12, Table 13 and Section 12.5.2) allows vertical mirroring: when MY = 1, the Y address space is mirrored; the address Y = 0 is then located at the bottom of the display, see Figure 13. When MY = 0, the mirroring is disabled and the address Y = 0 is located at top of the display, see Figure 14.

The icon row, when enabled, is always located in bank 9 and row 79.

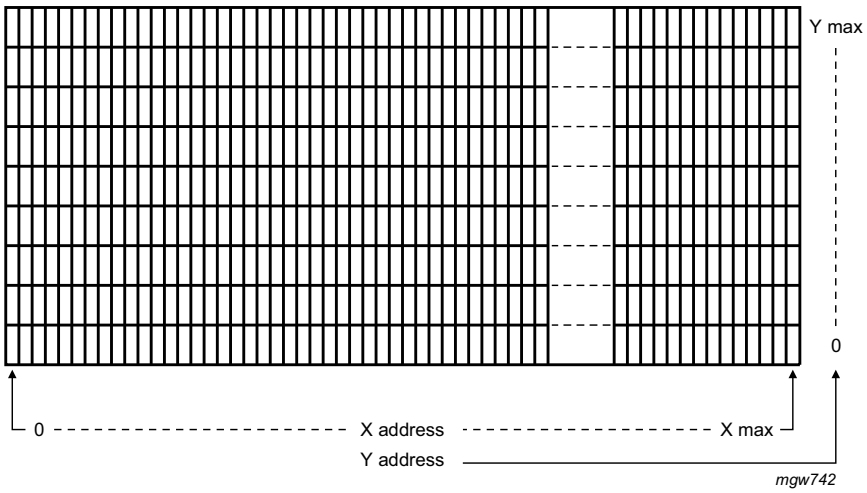


Fig 13. RAM format addressing; MY = 1 (both command sets)

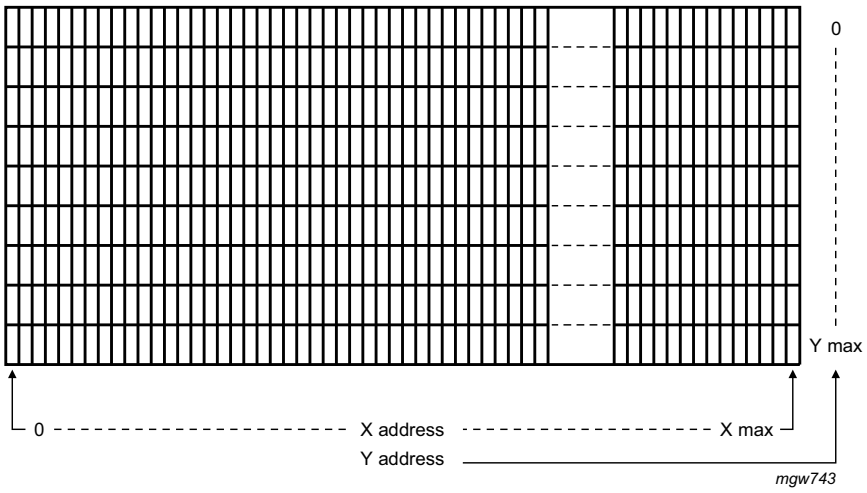


Fig 14. RAM format addressing; MY = 0 (both command sets)

9. Parallel interface

The parallel interface, which can be selected, is the 6800 series 8-bit bidirectional interface for communication between the microcontroller and the LCD driver chip. The selection of this interface is achieved with pins PS2 to PS0, see Section 7.1.12.

9.1 6800 series parallel interface

The interface functions of the 6800 series parallel interface are given in Table 9.

Table 9. 6800 series parallel interface functions

D/$\overline{C}$	R/$\overline{W}$/$\overline{WR}$	Operation
0	0	command data write
0	1	read status register
1	0	display data write
1	1	none

The parallel interface timing diagram for the 6800 series is shown in Figure 41.

10. Serial interfacing (SPI and serial interface)

Communication with the microcontroller can also occur via a clock-synchronized Serial Peripheral Interface (SPI). It is possible to select between either a 3-line (SPI or serial interface) or a 4-line serial peripheral interface. Selection is achieved via pins PS2 to PS0, see Section 7.1.12).

10.1 Serial peripheral interface lines

The serial peripheral interface is a 3-line or 4-line interface for communication between the microcontroller and the LCD driver chip. The 3 lines are:

- $\overline{SCE}$ (chip enable)
- SCLK (serial clock)
- SDATA (serial data)

For the 4-line serial peripheral interface, a separate D/$\overline{C}$ line is added.

The PCF8811 is connected to the serial data I/O (SDA) of the microcontroller by connecting the two pins SDATA (data input) and SDO (data output) together.

10.1.1 Write mode

The display data/$\overline{command}$ indication may be controlled either via software or the D/$\overline{C}$ select pin. When the D/$\overline{C}$ pin is used, display data is transmitted when D/$\overline{C}$ is HIGH, and command data is transmitted when D/$\overline{C}$ is LOW, see Figure 15 and Figure 16. When pin D/$\overline{C}$ is not used, the display data length instruction is used to indicate that a specific number of display data bytes (1 to 255) is to be transmitted, see Figure 17. The next byte after the display data string is handled as an instruction command.

When the 3-line SPI interface is used, the display data/$\overline{command}$ is controlled by software.

If $\overline{SCE}$ is pulled HIGH during a serial display data stream, the interrupted byte is invalid data but all previously transmitted data is valid. The next byte received will be handled as an instruction command, see Figure 18.

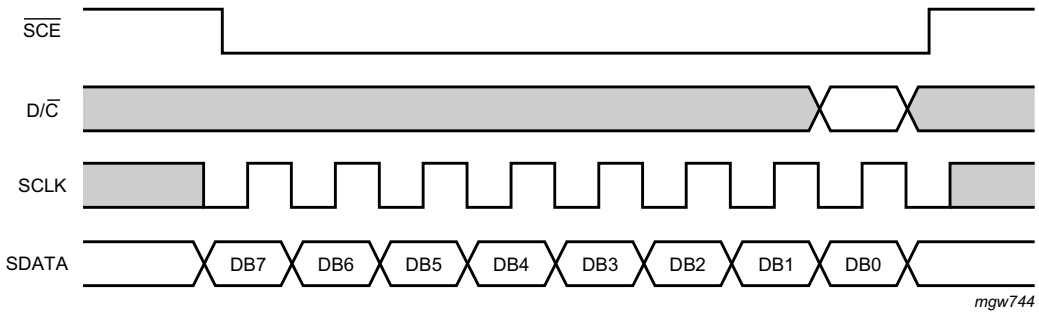


Fig 15. Serial bus protocol: transmission of 1 byte

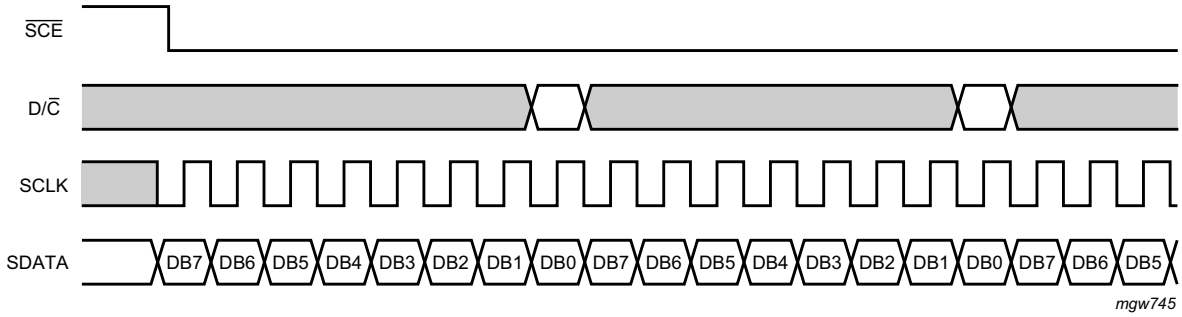


Fig 16. Serial bus protocol: transmission of several bytes

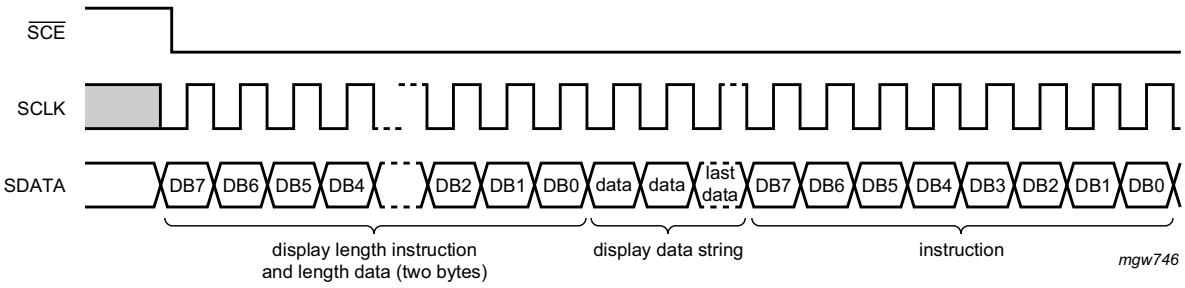


Fig 17. Transmission of several bytes

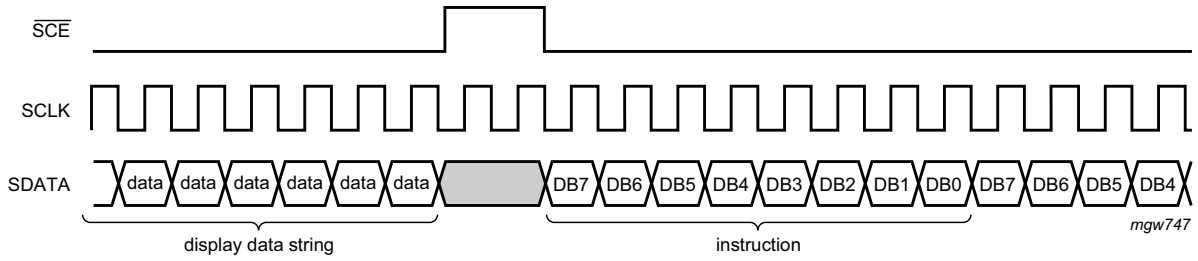


Fig 18. Transmission interrupted by $\overline{SCE}$

10.1.2 Read mode (only extended command set)

The read mode of the interface means that the microcontroller reads data from the PCF8811. The microcontroller first has to send a command (the read status command) and then the PCF8811 responds by transmitting data on the SDO line. After that, $\overline{SCE}$ is required to go HIGH, see Figure 19.

The PCF8811 samples the SDATA data on rising SCLK edges, but shifts SDO data on falling SCLK edges. So, the microcontroller is supposed to read SDO data on rising SCLK edges.

After the read status command has been sent, the SDATA line must be set to 3-state not later than the falling SCLK edge of the last bit, see Figure 19.

Serial interface timing diagrams are shown in Section 17.2.

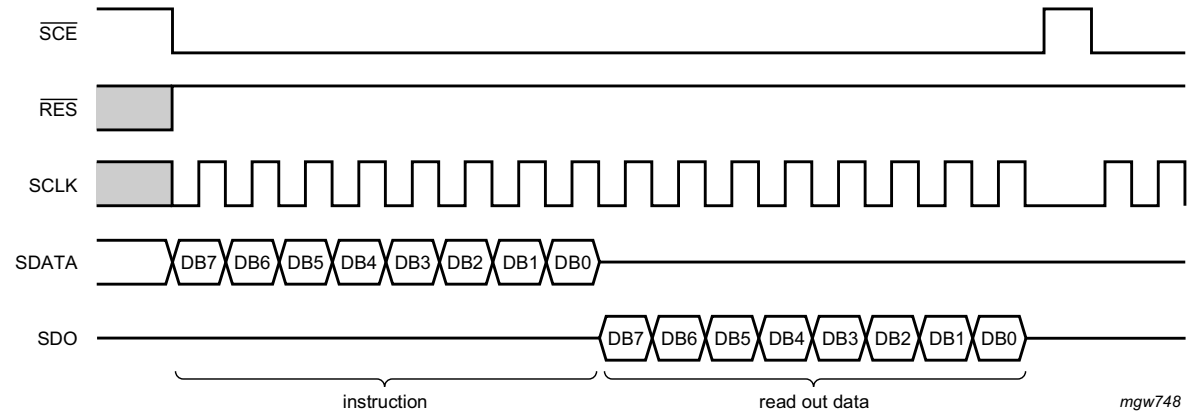


Fig 19. Read mode SPI 3-line and 4-line

10.2 Serial interface (3-line)

The serial interface is also a 3-line bidirectional interface for communication between the microcontroller and the LCD driver chip. The 3 lines are:

- $\overline{SCE}$ (chip enable)
- SCLK (serial clock)
- SDATA (serial data)

The PCF8811 is connected to the SDA of the microcontroller by two lines: SDATA (data input) and SDO (data output) which are connected together.

10.2.1 Write mode

The write mode of the interface means that the microcontroller writes commands and data to the PCF8811. Each data packet contains a control bit (D/$\overline{C}$) and a transmission byte. If D/$\overline{C}$ is LOW, the following byte is interpreted as a command byte. The instruction set is shown in Table 12. If D/$\overline{C}$ is HIGH, the following byte is stored in the display data RAM. After every data byte, the address counter is incremented automatically. Figure 20 shows the general format of the write mode and the definition of the transmission byte.

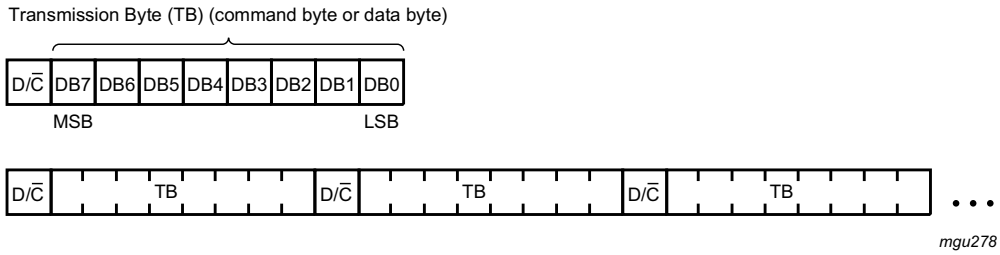


Fig 20. Serial data stream; write mode

Any instruction can be sent in any order to the PCF8811; the MSB is transmitted first. The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A falling edge on $\overline{SCE}$ enables the serial interface and indicates the start of data transmission.

Figure 21, Figure 22, and Figure 23 show the protocol of the write mode:

- when $\overline{SCE}$ is HIGH, SCLK clocks are ignored; during the HIGH time of $\overline{SCE}$, the serial interface is initialized
- SCLK must be LOW on the falling $\overline{SCE}$ edge, see Figure 42
- SDATA is sampled on the rising edge of SCLK
- D/$\overline{C}$ indicates, whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1). It is sampled on the first rising SCLK edge
- If $\overline{SCE}$ stays LOW after the last bit of a data/command byte, the serial interface receives the D/$\overline{C}$ bit of the next byte on the next rising edge of SCLK, see Figure 22
- A reset pulse $\overline{RES}$ interrupts the transmission. The data being written into the RAM may be corrupted. The registers are cleared. If $\overline{SCE}$ is LOW after the rising edge of $\overline{RES}$, the serial interface is ready to receive the D/$\overline{C}$ bit of a data/command byte, see Figure 23.

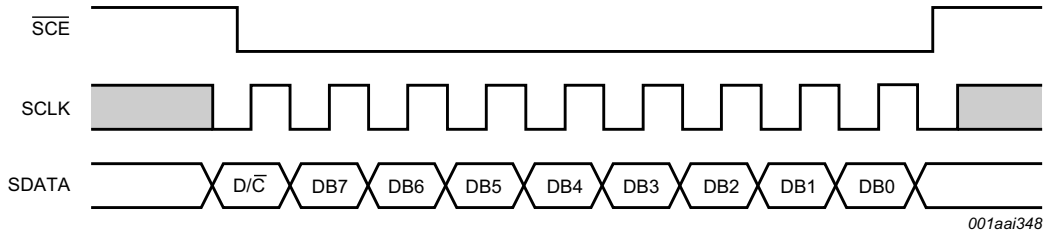


Fig 21. Write mode: a control bit followed by a transmission byte

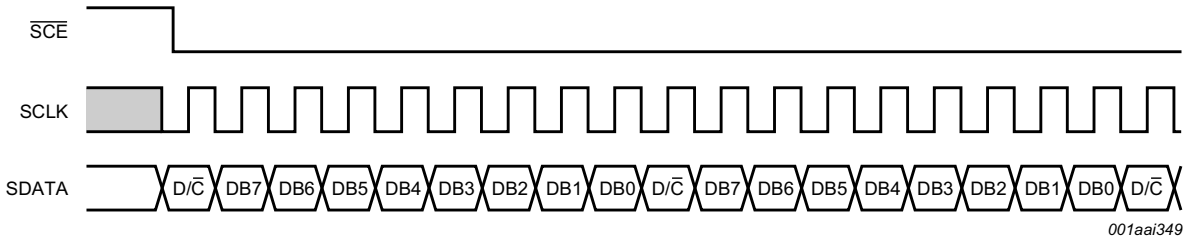


Fig 22. Write mode: transmission of several bytes

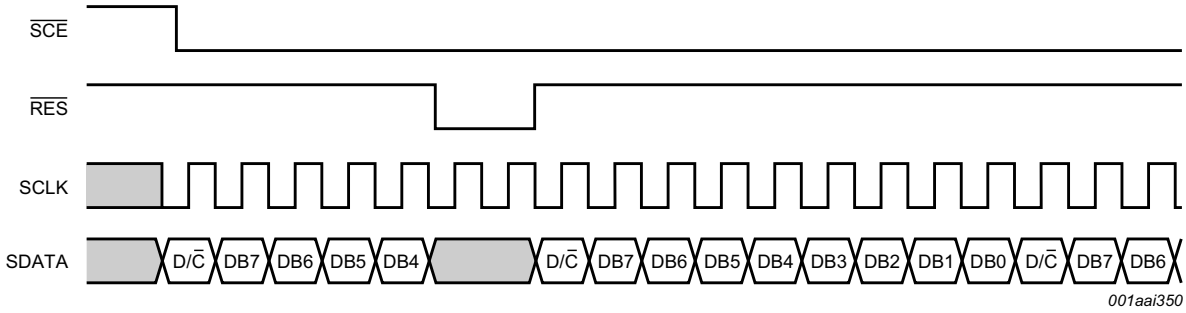


Fig 23. Write mode: interrupted by reset ($\overline{RES}$)

10.2.2 Read mode (only extended command set)

The read mode of the interface means that the microcontroller reads data from the PCF8811. To do so, the microcontroller first has to send a command (the read status command) and then the following byte is transmitted in the opposite direction using SDO, see Figure 24. After that, $\overline{SCE}$ is required to go HIGH before a new command is sent.

The PCF8811 samples the SDATA data on the rising SCLK edges, but shifts SDO data on the falling SCLK edges. Thus the microcontroller is supposed to read SDO data on rising SCLK edges.

After the read status command has been sent, the SDATA line must be set to 3-state not later than the falling SCLK edge of the last bit, see Figure 24.

The 8^{th} read bit is shorter than the others because it is terminated by the rising SCLK edge, see Figure 45. The last rising SCLK edge sets SDO to 3-state after the delay time t_4.

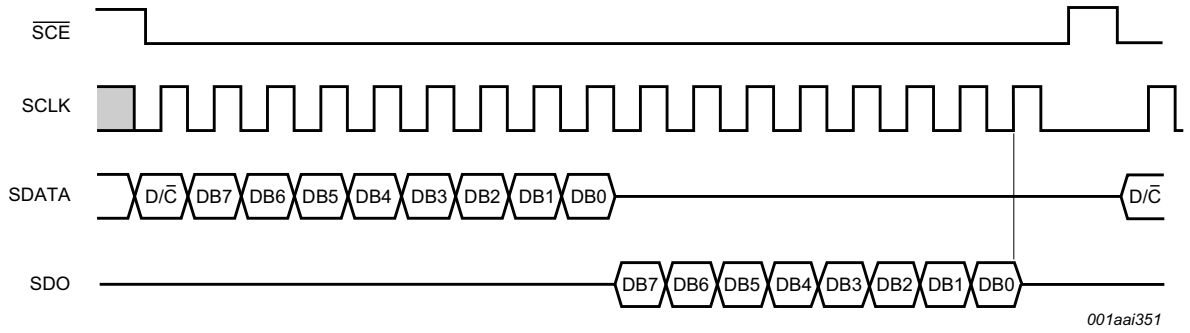


Fig 24. Read mode: serial interface 3-line

11. I²C-bus interface

11.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. Four operating speed modes are available:

- **Standard-mode (Sm)**, with a bit rate up to 100 kbit/s
- **Fast-mode (Fm)**, with a bit rate up to 400 kbit/s
- **Fast-mode Plus (Fm+)**, with a bit rate up to 1 Mbit/s
- **High-speed mode (Hs-mode)**, with a bit rate up to 3.4 Mbit/s.

Standard-mode, Fast-mode and Fast-mode Plus all use the same serial bus protocol and data format.

Hs-mode devices are fully downwards compatible and can be connected to an F/S-mode I²C-bus system. As no master code is transmitted in such a configuration (see Section 11.3), all Hs-mode master devices stay in F/S-mode and communicate at F/S-mode speeds with their current-source disabled. The SDAH and SCLH pins are used to connect to the F/S-mode bus system.

The PCF8811 is able to work in all speed modes including HS-mode. For using the HS-mode, all components - including the master (see Section 11.1.1) - have to be able to run this mode. For more information, see Ref. 11 “UM10204”.

11.1.1 System configuration

The system configuration is shown in Figure 25.

Definitions of the I²C-bus terminology:

- **transmitter:** the device which sends the data to the bus
- **receiver:** the device which receives the data from the bus
- **master:** the device which initiates a transfer, generates clock signals and terminates a transfer
- **slave:** the device addressed by a master

- **multi-master:** more than one master can attempt to control the bus at the same time without corrupting the message
- **arbitration:** procedure to ensure that only one master controls the bus, if more than one master simultaneously tries to control the bus. Therefore the message is not corrupted.
- **synchronization:** procedure to synchronize the clock signals of two or more devices

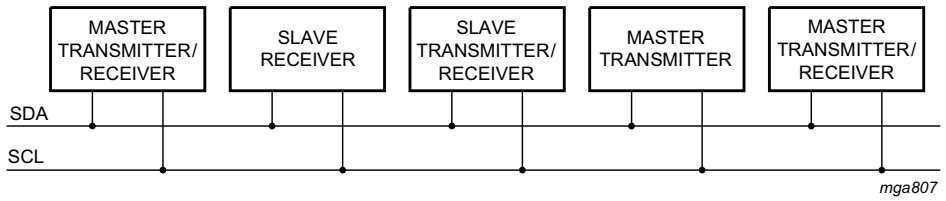


Fig 25. System configuration

11.1.2 Bit transfer

One data bit is transferred during each clock pulse, see Figure 26. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time is interpreted as a control signal.

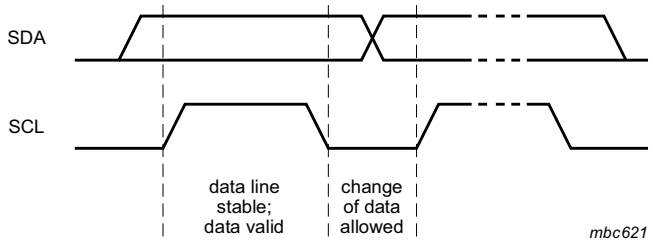


Fig 26. Bit transfer

11.1.3 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH change of the data line, while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are shown in Figure 27.

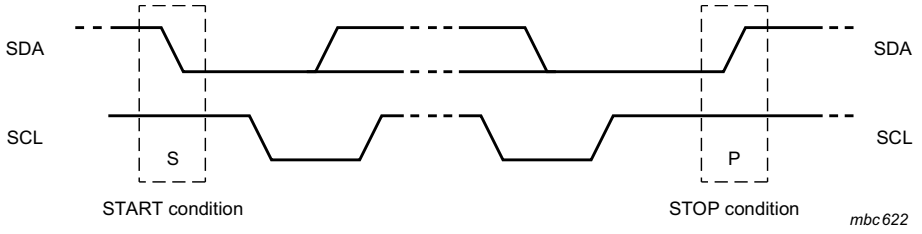


Fig 27. Definition of START and STOP conditions

11.1.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered)
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition

Acknowledgement on the I^2C-bus is shown in Figure 28.

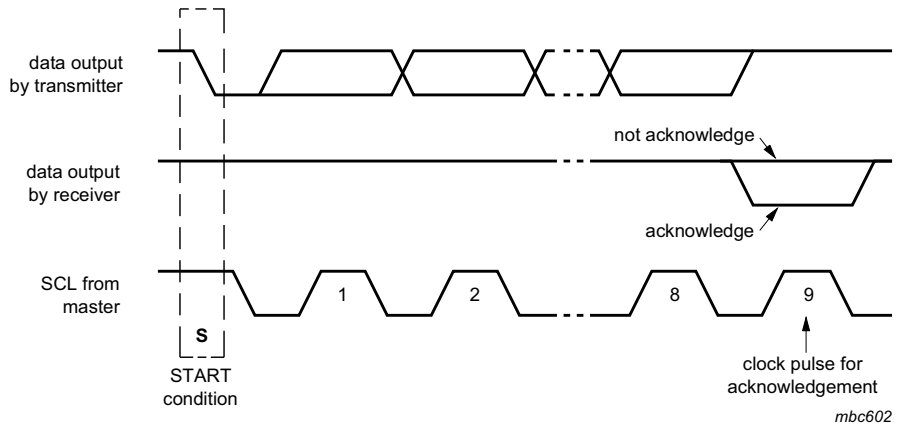


Fig 28. Acknowledge on the I^2C-bus

11.2 I^2C-bus protocol

Four I^2C-bus slave addresses (0111 100, 0111 101, 0111 110 and 0111 111) are reserved for the PCF8811.The entire I^2C-bus slave address byte is shown in Table 10.

Table 10. I^2C slave address byte

	Slave address							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MSB							**LSB**
	0	1	1	1	1	SA1	SA0	R/$\overline{W}$

Bit 1 and bit 2 of the slave address byte, that a PCF8811 responds to, are defined by the level tied to SA0 and SA1 (V_{SS} for logic 0 and V_{DD} for logic 1).

The I²C-bus protocol is shown in Figure 29. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of four possible PCF8811 slave addresses available. All slaves with the corresponding slave address acknowledge in parallel, all others ignore the I²C-bus transfer.

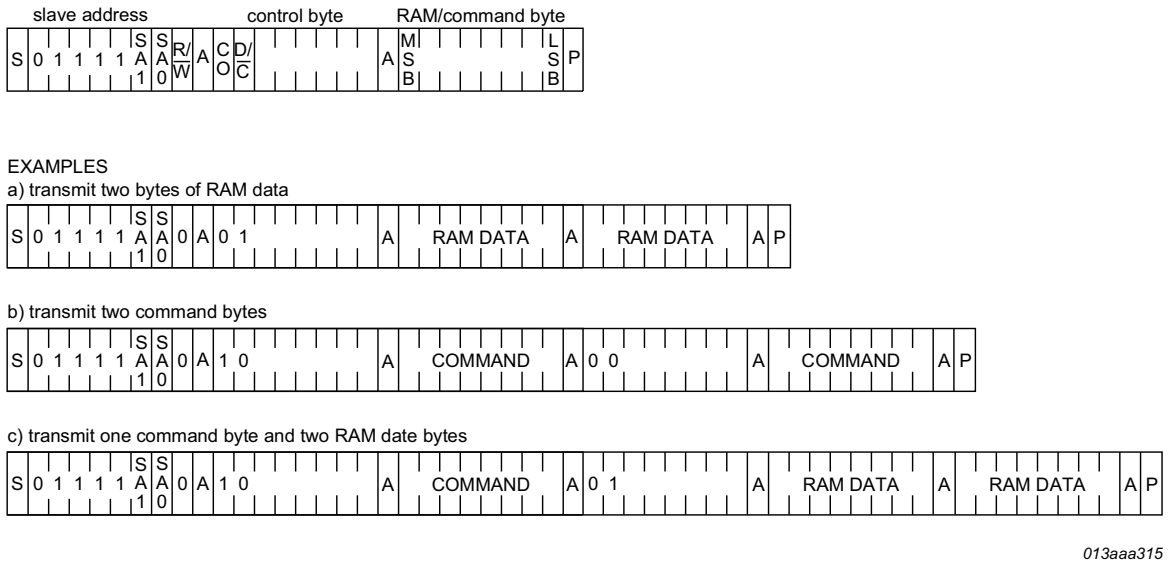


Fig 29. I²C-bus protocol

After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines bit Co and D/$\overline{C}$, plus a data byte (see Figure 29, Table 11 and Figure 30).

Table 11. Co and D/$\overline{C}$ definitions

Bit	Logic state	R/$\overline{W}$	Action
Co	0	0	last control byte to be sent; only a stream of data bytes is allowed to follow; this stream may only be terminated by a STOP or RESTART condition
	1	0	another control byte follows the data byte unless a STOP or RESTART condition is received
D/$\overline{C}$	0	0	data byte is decoded and used to set up the device
		1	data byte returns the status byte
	1	0	data byte is stored in the display RAM
		1	RAM read back is not supported

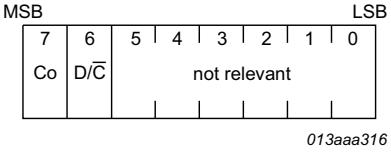


Fig 30. Control byte format

Within the last control byte, the Co bit is set logic 0. The command bytes and control bytes are also acknowledged by all addressed slaves connected to the bus. After the last control byte and depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended PCF8811 device. If the DC bit of the last control byte was set to logic 0, these command bytes are decoded and the setting of the device is changed according to the received commands. The acknowledgement after each byte is made only by the addressed PCF8811. At the end of the transmission, the I^{2}C-bus master issues a STOP condition (P).

11.3 I^{2}C-bus Hs-mode protocol

The PCF8811 is a slave receiver/transmitter. The SDAHOUT pin must be connected if data is to be read from the device or a write-only configuration with acknowledge is desired.

Hs-mode can only commence after the following conditions:

- START condition (S)
- 8-bit master code (0000 1xxx)
- Not-acknowledge bit ($\overline{A}$)

The master code has two functions: it allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winner. The master code also indicates the beginning of a Hs-mode transfer. These conditions are shown in Figure 31 and Figure 32.

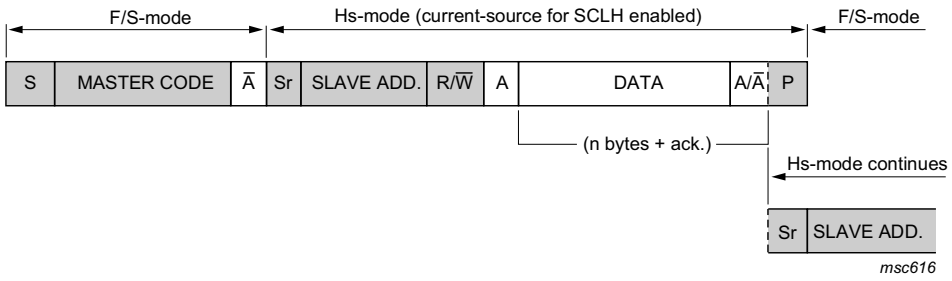


Fig 31. Data transfer format in Hs-mode

Hs-mode master codes are reserved 8-bit codes, which are not used for slave addressing or other purposes. Furthermore, as each master has its own unique master code, up to eight Hs-mode masters can be present on one I^{2}C-bus system (although master code 00001000 should be reserved for test and diagnostic purposes). The master code for a Hs-mode master device is software programmable and is chosen by the system designer.

Arbitration and clock synchronization only take place during the transmission of the master code and not-acknowledge bit ($\overline{A}$), after which one winning master remains active. The master code indicates to other devices that a Hs-mode transfer is to begin and the connected devices must meet the Hs-mode specification.

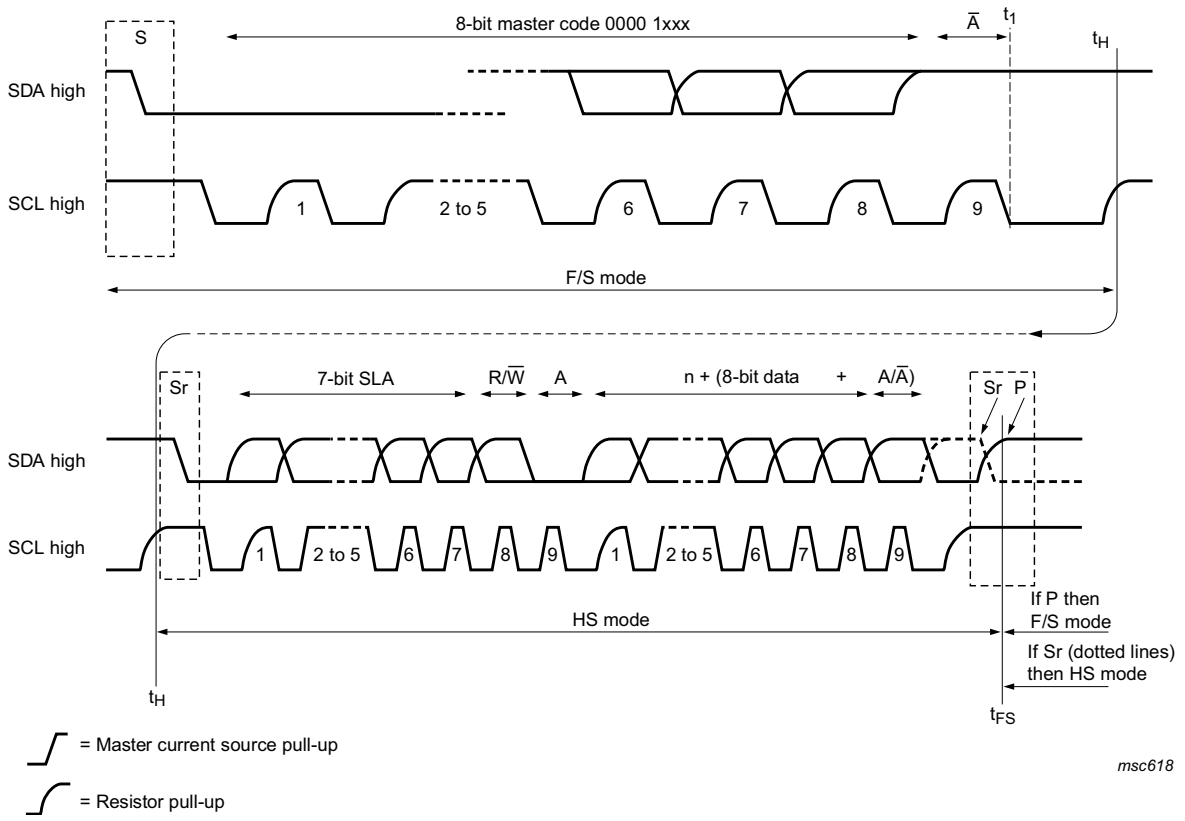


Fig 32. Data transfer timing format in F/S-mode and Hs-mode

As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge ($\overline{A}$). After this $\overline{A}$ and the SCLH line pulled up to a HIGH level, the active master switches to Hs-mode and enables at t_H the current-source pull-up circuit for the SCLH signal, see Figure 32.

The active master then sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/$\overline{W}$ bit, and receives an acknowledge bit (A) from the selected slave.

After each acknowledge bit (A) or not-acknowledge bit ($\overline{A}$), the active master disables its current source pull-up circuit. The active master re-enables its current source again when all devices have been released and the SCLH signal reaches a HIGH level. The rising of the SCLH signal is made by a pull-up resistor and therefore is slower, the last part of the SCLH rise time is speeded up because the current source is enabled. Data transfer only switches back to F/S-mode after a STOP condition (P).

A write sequence, after the Hs-mode is selected, is shown in Figure 33. The sequence is initiated with a START condition (S) from the I^2C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, the remainder ignores the I^2C-bus transfer.

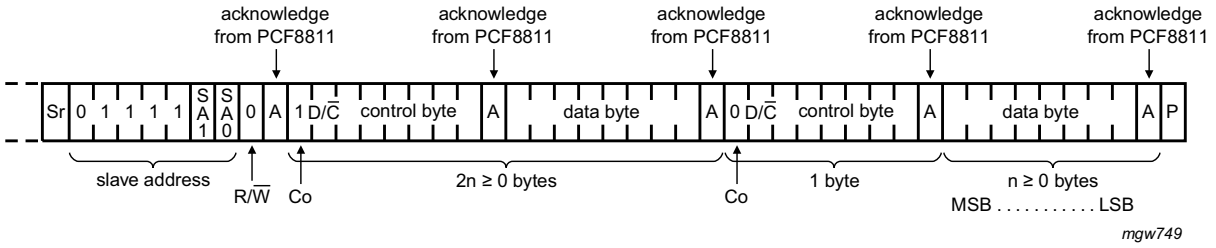


Fig 33. Master transmits in Hs-mode to slave receiver; write mode

After the acknowledgement cycle of a write ($\overline{W}$), one or more command words will follow which define the status of the addressed slaves. A command word consists of a control byte, which defines continuation bit Co and D/$\overline{C}$, plus a data byte, see Figure 33 and Table 11.

The last control byte is initiated by bit Co (a cleared MSB). The control and data bytes are also acknowledged by all addressed slaves on the bus.

A read sequence is shown in Figure 34 and again this sequence follows after the Hs-mode is selected. The PCF8811 immediately starts to output the requested data until a not-acknowledge is transmitted by the master. Before the read access, the user has to set the D/$\overline{C}$ bit to the appropriate value by a preceding write access. The write access must be terminated by a RESTART condition so that the Hs-mode is not disabled.

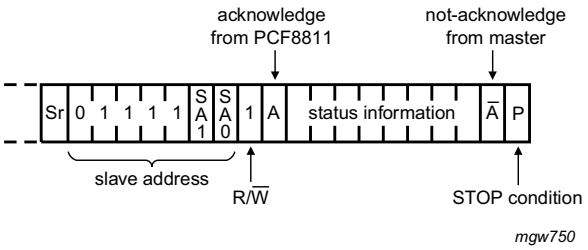


Fig 34. Master receives from slave transmitter (status register is read); read mode

After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer.

The data pointer is automatically updated and the data is directed to the intended PCF8811 device. If the D/$\overline{C}$ bit of the last control byte was set to logic 0, these command bytes are decoded and the setting of the device is changed according to the received commands. The acknowledgement after each byte is made only by the addressed PCF8811. At the end of the transmission, the I^2C-bus master issues a STOP condition (P) and switches back to the F/S-mode. However, to reduce the overhead of the master code, it is possible that a master can link a number of Hs-mode transfers, separated by repeated START conditions (Sr).

11.4 Command decoder

The command decoder identifies command words that are received on the I^2C-bus:

- pairs of bytes: information in second byte, first byte determines whether information is display or instruction data
- Stream of information bytes after Co = 0: display or instruction data depending on last D/$\overline{C}$

The most significant bit of a control byte is the continuation bit Co. If this bit is at logic 1, it indicates that only one data byte, either command or RAM data, follows. If this bit is at logic 0, it indicates that a series of data bytes, either command or RAM data, may follow. The DB6 bit of a control byte is the RAM data/command bit D/$\overline{C}$. When this bit is at logic 1, it indicates that a RAM data byte is transferred next. If the bit is at logic 0, it indicates that a command byte is transferred next.

12. Instructions

The PCF8811 interfaces via an 8-bit parallel interface, two different 3-line serial interfaces, a 4-wire serial interface or an I^2C-bus interface. Processing of the instructions does not require the display clock.

Data accesses to the PCF8811 can be broken down into two areas: one that defines the operating mode of the device, and one that fills the display RAM.

In use of the parallel and 4-wire SPI interfaces, the distinction is the D/$\overline{C}$ pin. When the D/$\overline{C}$ pin is at logic 0, the chip responds to instructions as defined in Table 12. When the D/$\overline{C}$ bit is at logic 1, the chip sends data to the RAM.

In use of the 3-wire SPI, the 3-wire serial interface or the I^2C-bus interface, the distinction between instructions defining the operating mode of the device and instructions that fill the display RAM, is made respectively:

- by the display data length instruction (3-line SPI) or
- by the D/$\overline{C}$ bit in the data stream (3-line serial interface and I^2C-bus interface).

There are 4 types of instructions which:

1. Define the PCF8811 functions, such as display configuration
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, category 3 instructions are used most frequently.

A basic and an extended instruction set is available. If the EXT pin is set LOW, the basic command set is used. If the EXT pin is set HIGH, the extended command set is used. Both command sets are detailed in Table 12.

Table 12. Instruction set[1]

Instruction	Pin			Command byte								Description
	EXT[2]	D/$\overline{C}$	R/$\overline{W}$/$\overline{WR}$	DB7[3]	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
NOP	X	0	0	0	1	0	0	1	1	X	X	both perform no
	X	0	0	1	1	1	0	0	1	0	0	be used
Reset	X	0	0	1	1	1	0	0	0	1	0	soft reset
Write data	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	write data to disp
Display data length	X	0	0	1	1	1	0	1	0	0	0	only used in 3-lin
	X	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Status read	X	0	1	BUSY	DON	$\overline{RES}$	MF2	MF1	MF0	X	DS0	read status byte
	X	0	X	1	1	0	1	1	0	1	X	read status byte
Display control	X	0	0	1	0	1	0	1	1	1	DON	display on or off
	X	0	0	1	0	1	0	0	1	1	E	normal or reverse
	X	0	0	1	0	1	0	0	1	0	DAL	all pixels on or of
	X	0	0	1	0	1	0	0	0	0	MX	mirror X
	X	0	0	1	1	0	0	MY	X	X	X	mirror Y
	1	0	0	1	1	1	0	1	1	1	IC	icon enable or di
	1	0	0	1	0	1	0	0	0	1	V	vertical or horizo
	1	0	0	1	1	1	0	1	0	1	DOR	data order[4]
	1	0	0	1	1	1	0	1	1	0	BRS	bottom row swap
Address commands	X	0	0	1	0	1	1	Y_3	Y_2	Y_1	Y_0	set Y address; 0
	X	0	0	0	0	0	1	0	X_6	X_5	X_4	set X address; 0
	X	0	0	0	0	0	0	X_3	X_2	X_1	X_0	
	X	0	0	0	0	0	1	1	0	0	1	set Y_{max}; $0 \leq Y \leq$
		0	0	X	X	X	X	Y_{max3}	Y_{max2}	Y_{max1}	Y_{max0}	
	X	0	0	0	0	0	1	1	0	0	0	set X_{max}; $0 \leq X \leq$
				X	X_{max6}	X_{max5}	X_{max4}	X_{max3}	X_{max2}	X_{max1}	X_{max0}	
Set initial display line	X	0	0	0	1	0	0	0	0	X	X	set initial display
	X	0	0	X	L_6	L_5	L_4	L_3	L_2	L_1	L_0	
Set initial row	X	0	0	0	1	0	0	0	1	X	X	set start row; $0 \leq$
	X	0	0	X	C_6	C_5	C_4	C_3	C_2	C_1	C_0	

Table 12. Instruction set[1] *…continued*

Instruction	Pin			Command byte								Description
	EXT[2]	D/$\overline{C}$	R/$\overline{W}$/$\overline{WR}$	DB7[3]	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Set-partial-display	X	0	0	0	1	0	0	1	0	X	X	set partial display
	X	0	0	X	P_6	P_5	P_4	P_3	P_2	P_1	P_0	
V_{OP} setting	0	0	0	1	0	0	0	0	0	0	1	set V_{OP}[7][8]
	0	0	0	X	X	V_{PR5}	V_{PR4}	V_{PR3}	V_{PR2}	V_{PR1}	V_{PR0}	
	0	0	0	0	0	1	0	0	V_{OFF2}	V_{OFF1}	V_{OFF0}	offset for V_{OP}[7][8
	1	0	0	1	0	0	0	0	0	0	1	set V_{OP}[4]
	1	0	0	V_{PR7}	V_{PR6}	V_{PR5}	V_{PR4}	V_{PR3}	V_{PR2}	V_{PR1}	V_{PR0}	
Power control	X	0	0	0	0	1	0	1	PC_1	PC_0	1	switch HVgen on
HVgen stages	0	0	0	0	1	1	0	0	1	S_1	S_0	set multiplication
	1	0	0	0	1	1	0	0	S_2	S_1	S_0	set multiplication
FR	1	0	0	0	0	0	1	1	1	FR_1	FR_0	set frame rate fre
TC[9]	1	0	0	0	0	1	1	1	TC_2	TC_1	TC_0	set temperature
Bias system	0	0	0	0	1	0	1	0	BS_2	BS_1	BS_0	set bias system[1
Manual p value (p = 4)	1	0	0	0	0	0	1	1	0	1	MP	set manual p val
Power-save on	X	0	0	1	0	1	0	1	0	0	1	power-save mod
Power-save off	X	0	0	1	1	1	0	0	0	0	1	exit power-save
Internal oscillator	X	0	0	1	0	1	0	1	0	1	OS	switch internal os
Internal oscillator	1	0	0	1	1	1	0	0	1	1	EC	enable or disable oscillator[4]
Enter CALMM mode	X	0	0	1	0	0	0	0	0	1	0	enter CALMM m
Reserved	X	0	0	0	0	1	0	1	X	X	0	reserved
Reserved	X	0	0	0	1	1	1	X	X	X	X	reserved
Test	X	0	0	1	1	1	1	X	X	X	X	do not use; reser

[1] X = value without meaning.

[2] NXP Semiconductors recommends that the extended command set is used.

[3] D7 = MSB.

[4] Commands only available with the extended command set, EXT = 1. If EXT = 0 these commands have no effect.

[5] When the icon mode is enabled the set initial display line $0 \leq L \leq 78$.

[6] When the icon mode is enabled the set initial row line $0 \leq C \leq 78$.

[7] Commands only used for the basic command set EXT = 0. If EXT = 1 these commands have no effect. It must be checked, when setting V_{OP} followed by another command.

[8] The programming of V_{OP} in the basic command set must be done in the following order:
   a) V_{PR}[5:0]
   b) V_{OFF}[2:0]
   c) must be followed by another command.

[9] One fixed TC is set automatically if the basic command set is used.

[10] Without function; implemented for compatibility with the Alt-Pleshko driver instruction set.

[11] Only for multiplex rates 1:64 and 1:80. The number of simultaneous rows can be set manually to p = 4, see Table 19.

12.1 Instruction set commands

12.1.1 Common instructions of the basic and extended command set

Table 13. Common commands

Bit	Logic 0	Logic 1	Reset state
DON	display off	display on	0
E	normal display	inverse video mode	0
DAL	normal display	all pixels on	0
MX	no X mirroring	X mirroring	0
MY	no Y mirroring	Y mirroring	0
OC	stop frame frequency calibration	start frame frequency calibration	0
OS	internal oscillator off	start internal oscillator	0
X[6:0]	set X address (column) for writing in the RAM		000 0000
Y[3:0]	set Y address (bank) for writing in the RAM		0000
$X_{max[6:0]}$	set wrap around X address (column)		111 1111
$Y_{max[3:0]}$	set wrap around Y address (bank)		1001
L[6:0]	sets line address of the display; this command cannot access the icon driver row, row 79, if the icon row is enabled		000 0000
C[6:0]	sets the initial row 0 of the display; this command cannot access the icon driver row, row 79, if the icon row is enabled		000 0000
P[6:0]	partial display mode 1:16 to 1:80 [1]		101 0000 (1:80)/100 0000 (1:64)
PC[1:0]	switch HV multiplier on/off		00
S[1:0]	charge pump multiplication factor		00

[1] Partial displays can be selected in steps of 8, when the icon mode is not selected. When the icon mode is selected, partial displays can be selected in steps of 16. For example, without icons the available partial display sizes are 8, 16, 24, 32, 40, 48, 56, 64 or 72 lines. With icons, there are 16, 32, 48 or 64 lines possible.

Table 14. Power control register[1]

PC[1:0]	Description
00	HVgen off
X1	HVgen on
1X	HVgen on

[1] X = value without meaning.

Table 15. Power-save mode (PSM), OS, DON, DAL and E combinations[1]

PSM	OS	DON	DAL	E	Description
Off	0	X	X	X	oscillator off; HVgen disabled
Off	1	X	0	X	oscillator on; HVgen disabled
Off	1	0	1	X	display off; pins Rn/Cn at V_{SS}; oscillator off; HVgen disabled[2]
Off	1	1	0	0	normal display mode
Off	1	1	0	1	inverse display mode
Off	1	1	1	X	all pixels on[3]
On	X	X	X	X	power-save mode: display off; pins Rn/Cn at V_{SS}; oscillator off; HVgen disabled

[1] X = value without meaning.

[2] Bit DON can only be addressed after bit DAL is activated.

[3] Bit DAL has priority over bit E.

Table 16. Read status byte

Bit	Description
BUSY	if BUSY = 0 the chip is able to accept new commands
DON	same bit as in Table 15
$\overline{RES}$	if $\overline{RES}$ = 1 a reset is in progress
MF[2:0]	device manufacturer ID
DS0	device recognition, see Table 6

Table 17. Multiplication settings

S[1:0]	Description
00	4 × voltage multiplier
01	5 × voltage multiplier
10	6 × voltage multiplier
11	7 × voltage multiplier

12.1.2 Specific commands of the basic command set

Table 18. Specific basic commands

Bit	Description	Reset state
V_{PR}[5:0]	programming value of V_{LCD}	00 0000
V_{OFF}[2:0]	offset for the programming value of V_{LCD}	000

12.1.3 Specific commands of the extended command set

Table 19. Specific extended commands

Bit	Logic 0	Logic 1	Reset state
V_{PR}[7:6] + V_{PR}[5:0]	programming value of V_{LCD}		0000 0000
FR[1:0]	frame rate frequency		11
TC[2:0]	temperature coefficient		010
S[2:0]	charge pump multiplication factor		100

Table 19. Specific extended commands *…continued*

Bit	Logic 0	Logic 1	Reset state
V	horizontal addressing	vertical addressing	0
DOR	LSB at top	MSB at top	0
IC	no icon row (multiplex rate 1:16 to 1:80)	icon row (multiplex rate 1:16 to 1:80)	0
BRS	bottom rows are not mirrored	bottom rows are mirrored	0
MP[1]	multiplex rate driven p value (automatic)	p = 4 selected for multiplex rate 1:64 and 1:80	0
EC	use internal oscillator	use external oscillator	0

[1] The default value for MP (Manual P) equals 0 and it is recommended to use that value as a starting point. However, depending on the liquid crystal properties, p = 4 may be a better choice and it is recommended to compare optical results for the automatically chosen value for p and for p=4 and use the one that gives best results.

Table 20. Frame rate frequency

FR[1:0]	Frame rate frequency
00	30 Hz
01	40 Hz
10	50 Hz
11	60 Hz

Table 21. Temperature coefficient[1]

TC[2:0]	Temperature coefficient
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

[1] For further information about temperature coefficient, see Table 31.

Table 22. Multiplication settings

S[2:0]	Description
000	2 × voltage multiplier
001	3 × voltage multiplier
010	4 × voltage multiplier
011	5 × voltage multiplier
100	4 × voltage multiplier

Table 22. Multiplication settings *…continued*

S[2:0]	Description
101	5 × voltage multiplier
110	6 × voltage multiplier
111	7 × voltage multiplier

12.2 Initialization

Reset is accomplished by applying an external reset pulse (active LOW) at pin $\overline{RES}$. When reset occurs within the specified time, all internal registers are reset, however the RAM is still undefined. The state after reset is described in Section 12.3. Pin $\overline{RES}$ must be $\leq 0.3\ V_{DD1}$ when V_{DD1} reaches $V_{DD(min)}$ (or higher) within a maximum time t_{VHRL} after V_{DD1} goes HIGH, see Figure 48.

A reset can also be achieved by sending a reset command. This command can be used during normal operation but not to initialize the chip after power-on.

12.3 Reset function

12.3.1 Basic command set

After reset, the LCD driver has the following state:

- Display setting E = 0 and DAL = 0
- Address commands X[6:0] = 0 and Y[3:0] = 0
- V_{LCD} is equal to 0, the HV multiplier is switched off (PC[1:0] = 00)
- No offset of the programming range (V_{OFF}[2:0] = 0)
- HV multiplier programming (V_{PR}[5:0] = 0)
- 4 × voltage multiplier (S[1:0] = 00)
- After power-on, RAM data is undefined, the reset signal does not change the content of the RAM
- All LCD outputs at V_{SS} (display off)
- Initial display line set to line 0 (L[6:0] = 0)
- Initial row set to row 0 (C[6:0] = 0)
- Full display selected (P[6:0] = multiplex rate 1:80 or 1:64)
- Display is not mirrored (MX = 0; MY = 0)
- Internal oscillator is off
- Power-save mode is on
- No frame calibration is running

12.3.2 Extended command set

After reset, the LCD driver has the following state:

- Display settings E = 0 and DAL = 0
- Icons disabled (IC = 0)
- Address counter X[6:0] = 0 and Y[3:0] = 0

- Temperature control mode TC2 (TC[2:0] = 010)
- V_{LCD} is equal to 0 V; the HV multiplier is switched off (PC[1:0] = 0)
- HV multiplier programming (V_{PR}[7:0] = 0)
- 4 × voltage multiplier (S[2:0] = 100)
- Frame-rate frequency (FR[1:0] = 11)
- After power-on, RAM data is undefined, the reset signal does not change the content of the RAM
- All LCD outputs at V_{SS} (display off)
- Full display selected (P[6:0] = multiplex rate 1:80 or 1:64)
- Initial display line set to line 0 (L[6:0] = 0)
- Initial row set to row 0 (C[6:0] = 0)
- Display is not mirrored (MX = 0; MY = 0)
- Internal oscillator is off
- Power-save mode is on
- Horizontal addressing enabled (V = 0)
- No data order swap (DOR = 0)
- No bottom row swap (BRS = 0)
- Internal oscillator enabled (EC = 0)
- No frame calibration running (OC = 0)

12.4 Power-save mode

In the power-save mode the LCD driver has the following state:

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator switched off; external V_{LCD} can be disconnected
- Oscillator off (external clock possible)
- RAM contents not cleared; RAM data can be written
- V_{LCD} discharged to V_{SS} in power-down mode

There are two ways to put the chip into power-save mode:

- The display must be off (DON = 0) and all the pixels on (DAL = 1)
- The power-save mode command is activated

12.5 Display control

The bits DON, E and DAL select the display mode, see Table 15.

12.5.1 Bit MX

When MX = 0: the display RAM is written from left to right (X = 0 is on the left side and X = X_{max} is on the right side of the display).

When MX = 1: the display RAM is written from right to left (X = 0 is on the right side and X = X_{max} is on the left side of the display).

The MX bit has an impact on the way the RAM is written to. So if a horizontal mirroring of the display is desired, the RAM must first be rewritten, after changing the MX bit.

12.5.2 Bit MY

When MY = 1, the display is mirrored vertically. A change to this bit has an immediate effect on the display.

12.6 Set Y address of RAM

Y[3:0] defines the Y address of the display RAM. When the icon row (row 79) is enabled, it is always in bank 9 independent of the multiplex rate which is programmed

Table 23. RAM X/Y address range

Y3	Y2	Y1	Y0	Content	Allowed X range
0	0	0	0	bank 0 (display RAM)	0 to 127
0	0	0	1	bank 1 (display RAM)	0 to 127
0	0	1	0	bank 2 (display RAM)	0 to 127
0	0	1	1	bank 3 (display RAM)	0 to 127
0	1	0	0	bank 4 (display RAM)	0 to 127
0	1	0	1	bank 5 (display RAM)	0 to 127
0	1	1	0	bank 6 (display RAM)	0 to 127
0	1	1	1	bank 7 (display RAM)	0 to 127
1	0	0	0	bank 8 (display RAM)	0 to 127
1	0	0	1	bank 9 (display RAM)	0 to 127

12.7 Set X address of RAM

The X address points to the columns. The range of X is 0 to 127 (7Fh).

12.8 Set display start line

L[6:0] (see Table 13) is used to select the display line address of the display RAM to be displayed on the initial row, row 0. The selection of L[6:0] is limited to steps of 8. When the icon row is selected, the selection of L[6:0] is limited to steps of 16. When a partial mode is selected, the selection of L[6:0] is also limited in steps. In addition, the selection of L[6:0] = 72 is not allowed when the icon row is enabled or disabled.

The initial row can, in turn, be set by C[6:0], see Table 13. Row 0 cannot be set to icon row 79 when enabled.

An example of the mapping from the RAM content to the display is shown in Figure 35. The content of the RAM is not modified. This feature allows, for instance, screen scrolling without rewriting the RAM.

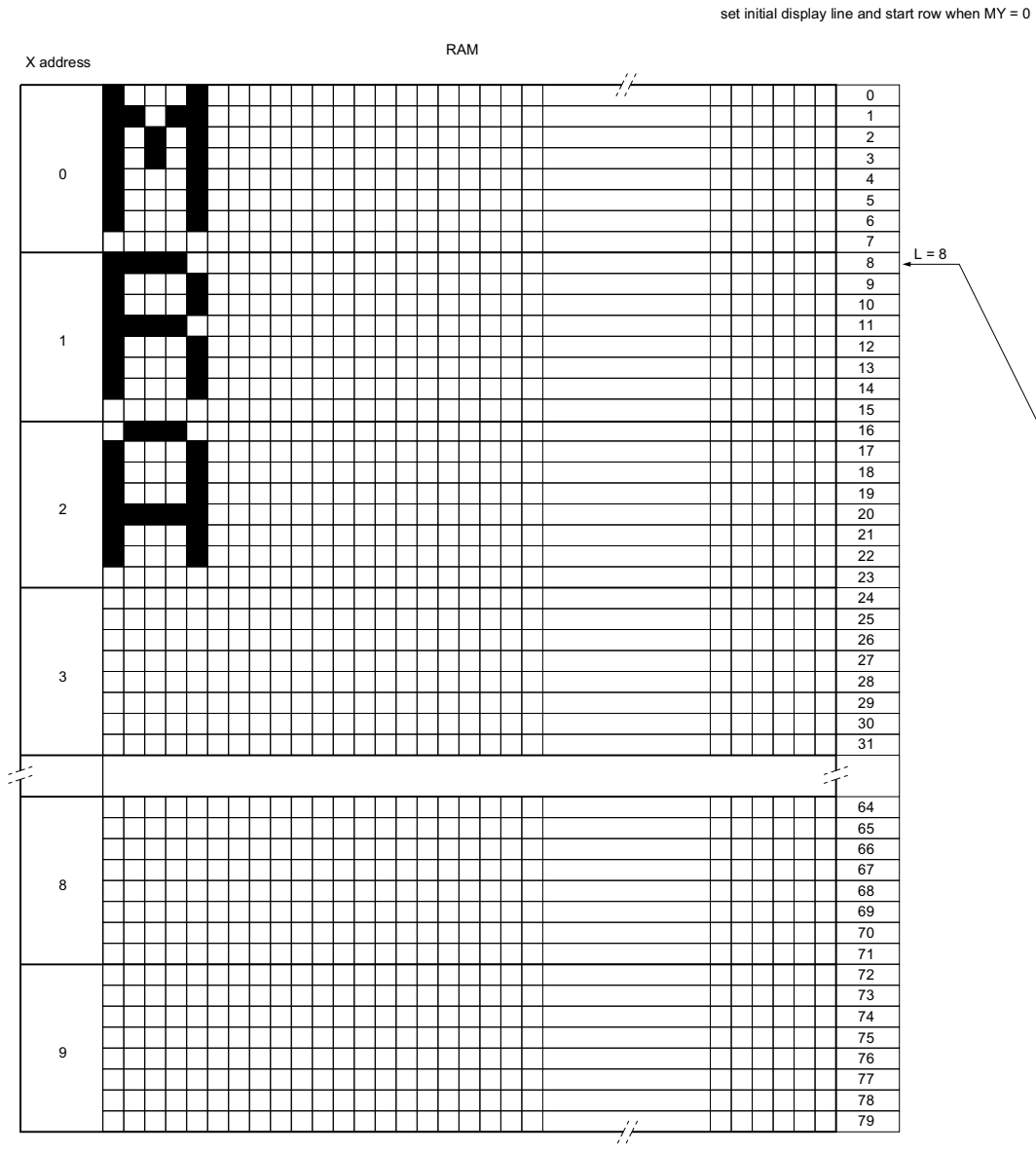


Fig 35. Programming the L[6:0] address and C[6:0] address when MY = 0

12.9 Bias levels

The PCF8811 is only a MRA (Multiple Row Addressing) driver and does not support Alt-Pleshko.

The bias levels for an MRA driving method with p = 8 are given in Figure 36 when G_{max} and F have the same value. The value p defines the number of rows which are simultaneously selected.

Fig 36. Bias levels for an MRA system with p = 8 and G_{max} = F

The row voltage F depends on the multiplex rate selected (number of rows N), the threshold voltage of the liquid (V_{TH}), the number of simultaneously selected rows (p), and the multiplexibility (m):

$$F = \frac{1}{\sqrt{p}} \times V_{TH} \times \sqrt{\frac{N}{2} \times \frac{\sqrt{m} \pm \sqrt{m-N}}{\sqrt{m}-1}} \quad (1)$$

Concerning the plus/minus sign within Equation 1: The PCF8811is designed to take the lowest possible V_{LCD}. Accordingly, the plus/minus sign is chosen in Equation 1.

If m = N, the term after the plus/minus sign becomes 0 and disappears from the equation. For specific displays, m could be larger than N: e.g. if the liquid-crystal material used allows multiplexing of more rows than denoted by N, then the equation for F can be used with the minus sign. This leads to a lower row voltage and a higher column voltage. As a consequence, the necessary supply voltage, which would be required for Alt-Pleshko driving, can be reduced for displays with m > N by using PCF8811 with MRA.

The column voltages are situated around the common level V_C. The column voltage levels are equidistant from each other. In Table 24, the column voltage levels are given as a function of F.

The row voltages (F) are not necessarily larger than the column voltages. This depends on the number of rows which are selected, the multiplexibility, and the value of p. However, the PCF8811 is designed in such a way that the maximum column voltages are always equal to the row voltages. In Table 24, the V_{LCD} and the different bias levels are given for the PCF8811.

Table 24. Bias levels for MRA driving method

$F = G_{max}$.

Symbol	Bias voltages	DC shifted bias voltages
V_{LCD}	F	V_{LCD}
V3_H	$(p-2)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1+\frac{(p-2)}{\sqrt{m}-\sqrt{m-N}}\right)$
V2_H	$(p-4)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1+\frac{(p-4)}{\sqrt{m}-\sqrt{m-N}}\right)$
V1_H	$(p-6)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1+\frac{(p-6)}{\sqrt{m}-\sqrt{m-N}}\right)$
V_C	0	$\frac{V_{LCD}}{2}$
V1_L	$-(p-6)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1-\frac{(p-6)}{\sqrt{m}-\sqrt{m-N}}\right)$
V2_L	$-(p-4)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1-\frac{(p-4)}{\sqrt{m}-\sqrt{m-N}}\right)$
V3_L	$-(p-2)\times\frac{F}{\sqrt{m}-\sqrt{m-N}}$	$\frac{V_{LCD}}{2}\times\left(1-\frac{(p-2)}{\sqrt{m}-\sqrt{m-N}}\right)$
V_{SS}	–F	V_{SS}

The parameter F in Table 24 is a mathematical function that can produce positive values only. The resulting bias voltages in Figure 36 and Table 24 can have both positive and negative values, with the largest absolute value equal to F. However, the PCF8811 uses only positive supplies. If the calculated F values get DC-shifted such that all values are positive, the common voltage V_C must be equal F. Then the DC-shifted bias voltages are not range from –F to +F, but from 0 to 2F and thus V_{LCD} is like in Equation 2:

$$V_{LCD} = 2F \tag{2}$$

Table 25. Relationship between multiplex rates and bias setting variables without icon row

Multiplex rate	Variable		
	N	m	p
1:16	16	25	2
1:24	24	49	2
1:32	32	81	2
1:40	40	49	4
1:48	48	64	4
1:56	56	81	4
1:64	64	64	8
1:72	72	81	8
1:80	80	81	8

The bias system settings for different display modes are given in Table 25. All bias levels can be calculated by using the third column of Table 24 and the variables given in Table 25. Programming of the bias levels is not necessary in the PCF8811. The selection of the appropriate bias level voltages for each display mode is made automatically. Only the appropriate V_{LCD} voltage must be programmed according to Equation 1 and Equation 2 for the display modes listed in Table 25.

The variables for calculating V_{LCD}, when the icon row is enabled, are given in Table 26. The icon row can only be addressed in the extended command set.

The PCF8811 allows the value of p for certain multiplex rates to be chosen manually. This is only possible for the multiplex rates 1:64 and 1:80. If other multiplex rates are chosen, the PCF8811 determines the optimum value of p. By setting the value of p manually, a compromise can be made between contrast and power consumption with certain liquids for the high multiplex rates 1:64 and 1:80. However, care must be taken that the liquid which is chosen ensures that the row voltages (F) and the maximum column voltages are equal.

Table 26. Relationship between multiplex rates and bias setting variables with the icon row (only extended command set)

Multiplex rate	Variable		
	N	m	p
1:16	24	49	2
1:32	40	49	4
1:48	56	81	8
1:64	80	81	8
1:80	80	81	8

12.10 Set V_{OP} value

For multiplex rate 1:80, the optimum operation voltage of a liquid can be calculated with the variables given in Table 26, Equation 1 and Equation 2, where V_{TH} is the threshold voltage of the liquid crystal material used.

$$V_{LCD} = \frac{2}{\sqrt{8}} \times V_{TH} \times \sqrt{\frac{80}{2} \times \frac{\sqrt{81} - \sqrt{81 - 80}}{\sqrt{81} - 1}} = 4.472 \times V_{TH} \quad (3)$$

The programming method for the V_{OP} value is implemented differently in the basic command set compared to the extended command set. In the basic command set two commands are sent to the PCF8811: namely V_{PR}[5:0] and V_{OFF}[2:0]. In the extended command set, only one command V_{PR}[7:0] is sent to the PCF8811. The programming of V_{OP} in the basic command set can be used when the PCF8811 is used as a replacement for an IAPT (Improved Alt-Pleshko Technique) LCD driver. The ROM look-up table Table 29 shows the possible values for V_{OFF}[2:0], V_{PR}[5:0], V_{OP}[7:0] and V_{LCD}.

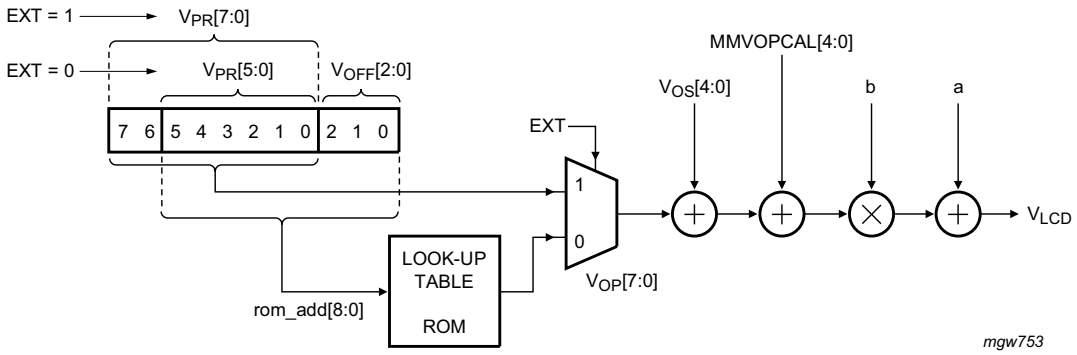


Fig 37. Setting of V_{OP} in the basic and extended command set

12.10.1 Basic command set

The V_{LCD} at T = T_{CUT} in the basic command set is determined by the conversion in the ROM look-up table with the programmed values of V_{PR}[5:0] and V_{OFF}[2:0]. It can, additionally, be adjusted with the V_{LCD} offset pins V_{OS}[4:0] to obtain the optimum optical performance.

Example: To get the value of 6 V for V_{LCD}, the following values (see Table 27) have to be taken:

Table 27. Example values of V_{PR}, V_{OP} and V_{OFF} for V_{LCD} = 6 V

Register	Value in Table 29	Binary value
V_{PR}[5:0]	15	0 1111
V_{OP}[7:0]	100	110 0100
V_{OFF}[2:0]	010	010

Instead of using the V_{LCD} offset pins (V_{OS}[4:0]) the V_{LCD} can be adjusted with the module maker calibration setting MMVOPCAL[4:0], see Section 19.

$$V_{LCD(T = T_{CUT})} = a + (V_{OS}[4:0] + V_{OP}[7:0]) \times b \quad (4)$$

Where:

- T_{CUT} is a reference temperature, see Section 12.11
- a is a fixed constant value, see Table 28
- b is a fixed constant value, see Table 28
- $V_{OP}[7:0]$ is the result of the conversion table
- $V_{OS}[4:0]/MMVOPCAL[4:0]$ is the value of the offset V_{LCD} pins or the value stored in the OTP cells

Table 28. Parameters of V_{LCD} for the basic and extended command set

Symbol	Value	Unit
T_{CUT}	40	°C
b	0.03	V
a	3	V

Table 29. ROM look-up table with values of V_{OFF}, V_{PR}, V_{OP} and V_{LCD}

V_{OFF}[000]			V_{OFF}[001]			V_{OFF}[010]			V_{OFF}[011]			V_{OFF}[100]			V_{OFF}[101]			V_{OFF}[110	
V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{O} [7:
0	13	3.39	0	48	4.44	0	82	5.46	0	116	6.48	0	150	7.5	0	185	8.55	0	21
1	14	3.42	1	49	4.47	1	83	5.49	1	118	6.54	1	152	7.56	1	187	8.61	1	22
2	15	3.45	2	50	4.5	2	84	5.52	2	119	6.57	2	154	7.62	2	189	8.67	2	22
3	15	3.45	3	51	4.53	3	86	5.58	3	121	6.63	3	156	7.68	3	191	8.73	3	22
4	16	3.48	4	52	4.56	4	87	5.61	4	122	6.66	4	157	7.71	4	192	8.76	4	22
5	17	3.51	5	53	4.59	5	88	5.64	5	123	6.69	5	159	7.77	5	194	8.82	5	23
6	18	3.54	6	54	4.62	6	89	5.67	6	125	6.75	6	161	7.83	6	196	8.88	6	23
7	19	3.57	7	55	4.65	7	90	5.7	7	126	6.78	7	162	7.86	7	198	8.94	7	23
8	19	3.57	8	56	4.68	8	92	5.76	8	128	6.84	8	164	7.92	8	200	9	8	23
9	20	3.6	9	57	4.71	9	93	5.79	9	129	6.87	9	166	7.98	9	202	9.06	9	23
10	21	3.63	10	58	4.74	10	94	5.82	10	131	6.93	10	167	8.01	10	204	9.12	10	24
11	22	3.66	11	59	4.77	11	95	5.85	11	132	6.96	11	169	8.07	11	206	9.18	11	24
12	22	3.66	12	60	4.8	12	97	5.91	12	134	7.02	12	171	8.13	12	208	9.24	12	24
13	23	3.69	13	61	4.83	13	98	5.94	13	135	7.05	13	173	8.19	13	210	9.3	13	24
14	24	3.72	14	62	4.86	14	99	5.97	14	137	7.11	14	174	8.22	14	212	9.36	14	24
15	25	3.75	15	63	4.89	15	100	6	15	138	7.14	15	176	8.28	15	214	9.42	15	25
16	25	3.75	16	64	4.92	16	102	6.06	16	140	7.2	16	178	8.34	16	216	9.48	16	25
17	26	3.78	17	65	4.95	17	103	6.09	17	141	7.23	17	179	8.37	17	218	9.54	17	25
18	27	3.81	18	66	4.98	18	104	6.12	18	143	7.29	18	181	8.43	18	220	9.6	18	25
19	28	3.84	19	66	4.98	19	105	6.15	19	144	7.32	19	183	8.49	19	221	9.63	19	25
20	29	3.87	20	68	5.04	20	106	6.18	20	145	7.35	20	184	8.52	20	223	9.69	20	25
21	29	3.87	21	69	5.07	21	108	6.24	21	147	7.41	21	186	8.58	21	225	9.75	21	25
22	30	3.9	22	70	5.1	22	109	6.27	22	148	7.44	22	188	8.64	22	227	9.81	22	25
23	31	3.93	23	71	5.13	23	110	6.3	23	150	7.5	23	190	8.7	23	229	9.87	23	25
24	32	3.96	24	72	5.16	24	111	6.33	24	151	7.53	24	191	8.73	24	231	9.93	24	25
25	32	3.96	25	73	5.19	25	113	6.39	25	153	7.59	25	193	8.79	25	233	9.99	25	25
26	33	3.99	26	74	5.22	26	114	6.42	26	154	7.62	26	195	8.85	26	235	10.05	26	25
27	34	4.02	27	75	5.25	27	115	6.45	27	156	7.68	27	196	8.88	27	237	10.11	27	25
28	35	4.05	28	76	5.28	28	116	6.48	28	157	7.71	28	198	8.94	28	239	10.17	28	25

Table 29. ROM look-up table with values of V_{OFF}, V_{PR}, V_{OP} and V_{LCD} *...continued*

V_{OFF}[000]			V_{OFF}[001]			V_{OFF}[010]			V_{OFF}[011]			V_{OFF}[100]			V_{OFF}[101]			V_{OFF}[110	
V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{O} [7:
29	35	4.05	29	77	5.31	29	118	6.54	29	159	7.77	29	200	9	29	241	10.23	29	25
30	36	4.08	30	78	5.34	30	119	6.57	30	160	7.8	30	201	9.03	30	243	10.29	30	25
31	37	4.11	31	79	5.37	31	120	6.66	31	162	7.86	31	203	9.09	31	245	10.35	31	25
32	38	4.14	32	80	5.4	32	121	6.63	32	163	7.89	32	205	9.15	32	247	10.41	32	25
33	39	4.17	33	81	5.43	33	123	6.69	33	165	7.95	33	207	9.21	33	249	10.47	33	25
34	39	4.17	34	82	5.46	34	124	6.72	34	166	7.98	34	208	9.24	34	250	10.5	34	25
35	40	4.2	35	83	5.49	35	125	6.75	35	167	8.01	35	210	9.3	35	252	10.56	35	25
36	41	4.23	36	84	5.52	36	126	6.78	36	169	8.07	36	212	9.36	36	254	10.62	36	25
37	42	4.26	37	85	5.55	37	127	6.81	37	170	8.1	37	213	9.39	37	256	10.68	37	25
38	42	4.26	38	86	5.58	38	129	6.87	38	172	8.16	38	215	9.45	38	256	10.68	38	25
39	43	4.29	39	87	5.61	39	130	6.9	39	173	8.19	39	217	9.51	39	256	10.68	39	25
40	44	4.32	40	88	5.64	40	131	6.93	40	175	8.25	40	218	9.54	40	256	10.68	40	25
41	45	4.35	41	89	5.67	41	132	6.96	41	176	8.28	41	220	9.6	41	256	10.68	41	25
42	45	4.35	42	90	5.7	42	134	7.02	42	178	8.34	42	222	9.66	42	256	10.68	42	25
43	46	4.38	43	91	5.73	43	135	7.05	43	179	8.37	43	224	9.72	43	256	10.68	43	25
44	47	4.41	44	92	5.76	44	136	7.08	44	181	8.43	44	225	9.75	44	256	10.68	44	25
45	48	4.44	45	93	5.79	45	137	7.11	45	182	8.46	45	227	9.81	45	256	10.68	45	25
46	48	4.44	46	94	5.82	46	139	7.17	46	184	8.52	46	229	9.87	46	256	10.68	46	25
47	49	4.47	47	95	5.85	47	140	7.2	47	185	8.55	47	230	9.9	47	256	10.68	47	25
48	50	4.5	48	96	5.88	48	141	7.23	48	187	8.61	48	232	9.96	48	256	10.68	48	25
49	51	4.53	49	97	5.91	49	142	7.26	49	188	8.64	49	234	10.02	49	256	10.68	49	25
50	52	4.56	50	98	5.94	50	143	7.29	50	189	8.67	50	235	10.05	50	256	10.68	50	25
51	52	4.56	51	99	5.97	51	145	7.35	51	191	8.73	51	237	10.11	51	256	10.68	51	25
52	53	4.59	52	100	6	52	146	7.38	52	192	8.76	52	239	10.17	52	256	10.68	52	25
53	54	4.62	53	101	6.03	53	147	7.41	53	194	8.82	53	241	10.23	53	256	10.68	53	25
54	55	4.65	54	102	6.06	54	148	7.44	54	195	8.85	54	242	10.26	54	256	10.68	54	25
55	55	4.65	55	103	6.09	55	150	7.5	55	197	8.91	55	244	10.32	55	256	10.68	55	25
56	56	4.68	56	104	6.12	56	151	7.53	56	198	8.94	56	246	10.38	56	256	10.68	56	25
57	57	4.71	57	105	6.15	57	152	7.56	57	200	9	57	247	10.41	57	256	10.68	57	25

Table 29. ROM look-up table with values of V_{OFF}, V_{PR}, V_{OP} and V_{LCD} *...continued*

V_{OFF}[000]			V_{OFF}[001]			V_{OFF}[010]			V_{OFF}[011]			V_{OFF}[100]			V_{OFF}[101]			V_{OFF}[110	
V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{OP} [7:0]	V_{LCD} (V)	V_{PR} [5:0]	V_{O} [7:
58	58	4.74	58	105	6.15	58	153	7.59	58	201	9.03	58	249	10.47	58	256	10.68	58	25
59	58	4.74	59	107	6.21	59	155	7.65	59	203	9.09	59	251	10.53	59	256	10.68	59	25
60	59	4.77	60	108	6.24	60	156	7.68	60	204	9.12	60	252	10.56	60	256	10.68	60	25
61	60	4.8	61	109	6.27	61	157	7.71	61	206	9.18	61	254	10.62	61	256	10.68	61	25
62	61	4.83	62	110	6.3	62	158	7.74	62	207	9.21	62	256	10.68	62	256	10.68	62	25
63	62	4.86	63	111	6.33	63	160	7.8	63	209	9.27	63	256	10.68	63	256	10.68	63	25

12.10.2 Extended command set

The V_{LCD} at T = T_{CUT} is calculated using Equation 5. In the extended command set, V_{PR}[7:0] is the same value as V_{OP}[7:0]. It can additionally be adjusted with the V_{LCD} offset pins V_{OS}[4:0] to obtain the optimum optical performance.

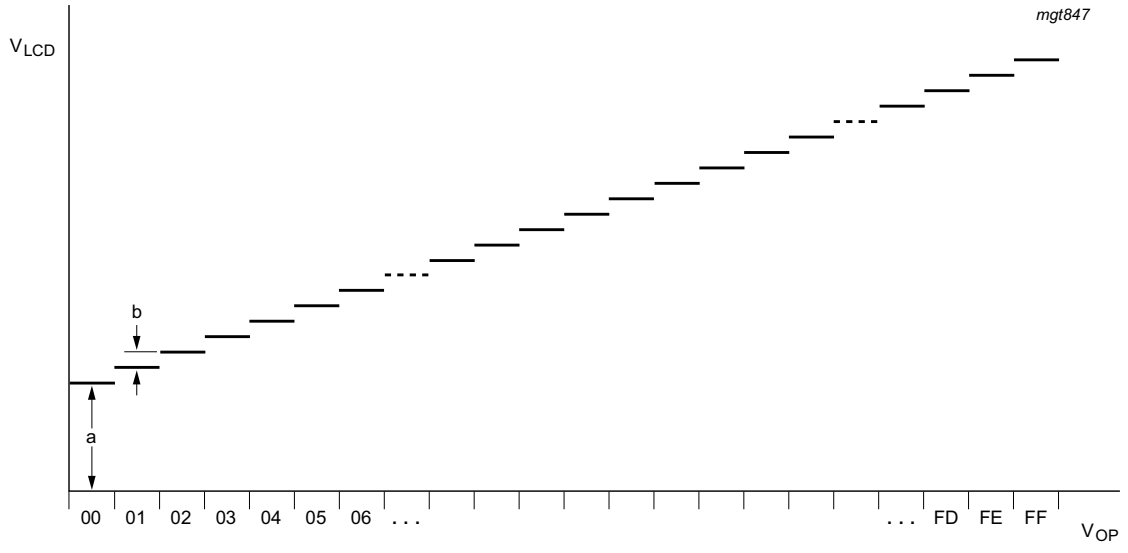
Instead of using the V_{LCD} offset pins (V_{OS}[4:0]) the V_{LCD} can be adjusted with the module maker calibration setting MMVOPCAL[4:0], see Section 19.

$$V_{LCD(T = T_{CUT})} = a + (V_{OS}[4:0] + V_{OP}[7:0]) \times b \quad (5)$$

Where:

- T_{CUT} is a reference temperature, see Section 12.11
- a is a fixed constant value, see Table 28
- b is a fixed constant value, see Table 28
- $V_{PR}[7:0]$ is the programmed V_{OP} value
- $V_{OS}[4:0]/MMVOPCAL[4:0]$ is the value of the offset V_{LCD} pins or the value stored in the OTP cells

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (9 V) the user has to ensure while setting the V_{PR} register and selecting the Temperature Compensation (TC), that under all conditions and including all tolerances the V_{LCD} remains below 9.0 V. This is valid for the two different command sets.



V_{OP}[7:0] programming (00h to FFh).

Fig 38. V_{LCD} programming of the PCF8811

12.11 Temperature control

Due to the temperature dependency of the viscosity of the liquid crystals, the LCD controlling voltage, V_{LCD}, might have to be increased at lower temperatures to maintain optimum contrast.

You can calculate the V_{LCD} at a specific temperature for both command sets. V_{LCD} (at $T = T_{CUT}$) is given by Equation 4 or Equation 5 depending on the command set which is used.

$$V_{LCD(T)} = V_{LCD(T = T_{CUT})} \times [1 + (T - T_{CUT}) \times TC] \quad (6)$$

In the extended command set and basic command set, 8 different temperature coefficients are available, see Figure 39.

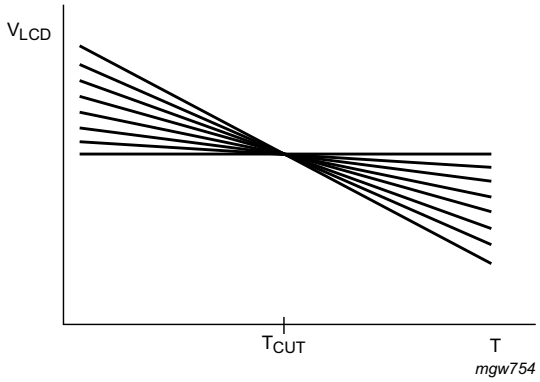


Fig 39. Temperature coefficients

The typical values of the different temperature coefficients are given in Section 16. The coefficients are proportional to the programmed V_{LCD}.

The basic and extended command set differ in the way that the temperature coefficients can be accessed. In the basic command set, only one temperature coefficient is available. However, the possibility exists to program the default temperature coefficient with OTP programming, see Section 19. In the extended command set, the different temperature coefficients are selected by the interface with 3 bits TC[2:0].

13. Internal circuitry

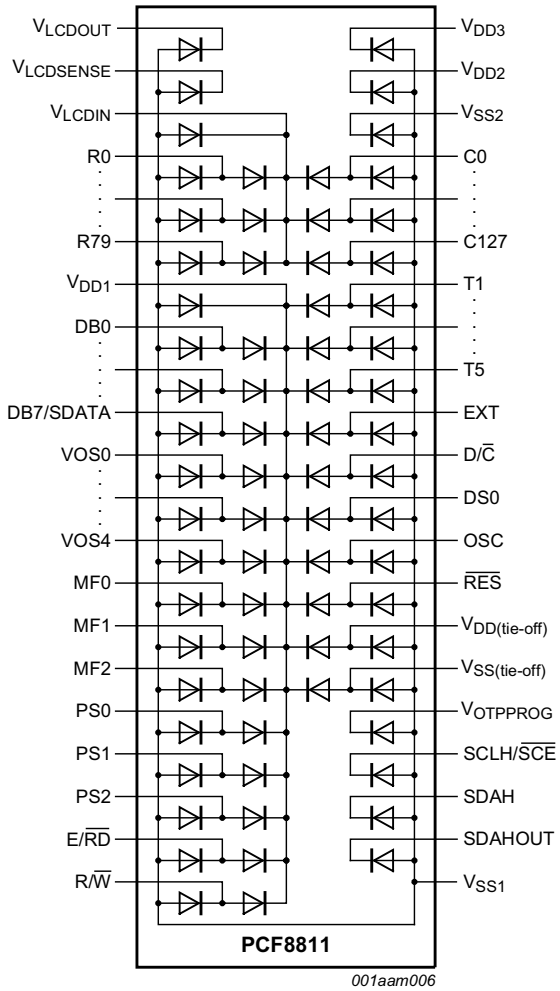


Fig 40. Device protection diagrams

14. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

15. Limiting values

Table 30. Limiting values[1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD1}	supply voltage 1	general	−0.5	+6.5	V
V_{DD2}	supply voltage 2	for internal voltage generator [2]	−0.5	+4.5	V
V_{DD3}	supply voltage 3	for internal voltage generator [2]	−0.5	+4.5	V
V_{LCD}	LCD supply voltage		−0.5	+10	V
V_i	input voltage		−0.5	+6.5	V
$V_{OTPPROG}$	voltage applied to pin $V_{OTPPROG}$		−0.5	+12	V
I_I	input current	DC level	−10	+10	mA
I_O	output current	DC level	−10	+10	mA
I_{SS}	ground supply current		−50	+50	mA
P_{tot}	total power dissipation		-	300	mW
P/out	power dissipation per output		-	30	mW
V_{ESD}	electrostatic discharge voltage	HBM [3]	-	±3000	V
		MM [4]	-	±250	V
I_{lu}	latch-up current	[5]	-	200	mA
T_{stg}	storage temperature	[6]	−65	+150	°C

[1] Parameters are valid over the whole operating temperature range unless otherwise specified. All voltages are referenced to V_{SS} unless otherwise specified.

[2] For the internal voltage multiplier.

[3] Pass level; Human Body Model (HBM), according to Ref. 6 “JESD22-A114”.

[4] Pass level; Machine Model (MM), according to Ref. 7 “JESD22-A115”.

[5] Pass level; latch-up testing according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[6] According to the store and transport requirements (see Ref. 10 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

16. Static characteristics

Table 31. Static characteristics

V_{DD1} = 1.7 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = 3 V to 9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD1}	supply voltage 1	general		1.7	-	3.3	V
		basic command set; when using ROM look-up table, see Section 12.10		2	-	3.3	V
V_{DD2}	supply voltage 2	for internal voltage multiplier		1.8	-	3.3	V
V_{DD3}	supply voltage 3	for internal voltage multiplier		1.8	-	3.3	V
V_{LCDIN}	LCD supply voltage	LCD voltage externally supplied (voltage multiplier disabled)		3	-	9	V
V_{LCDOUT}	voltage multiplier output voltage	LCD voltage internally generated (voltage multiplier enabled)	[1]	-	-	9	V
$V_{LCD(tol)}$	tolerance of generated V_{LCD}	without calibration		−300	-	+300	mV
		with calibration	[2]	−70	-	+70	mV
I_{DD1}	supply current 1	general	[3][4]	0.5	1.5	5	µA
			[4][5]	15	25	50	µA
I_{DD2}	supply current 2	for internal voltage multiplier	[3][4]	0	0.5	1	µA
			[4][5]	130	150	200	µA
I_{DD3}	supply current 3	for internal voltage multiplier	[3][4]	0	0.5	1	µA
			[4][5]	130	150	200	µA
$I_{DD(tot)}$	total supply current	$V_{DD1} + V_{DD2} + V_{DD3}$	[4][5]	145	175	250	µA
Logic inputs; MF[2:0], V_{OS}[4:0], DS0, EXT, PS[2:0], RES and OSC							
V_i	input voltage			V_{SS} − 0.5		V_{DD1} + 0.5	V
V_{IL}	LOW-level input voltage			V_{SS}	-	$0.2V_{DD1}$	V
V_{IH}	HIGH-level input voltage			$0.8V_{DD1}$	-	V_{DD1}	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}		−1	-	+1	µA
Column and row outputs							
R_{col}	column output resistance	C0 to C127; V_{LCD} = 5 V		-	-	5	kΩ
R_{row}	row output resistance	R0 to R80; V_{LCD} = 5 V		-	-	5	kΩ
$V_{bias(col)}$	bias tolerance voltage	C0 to C127		−100	0	+100	mV
$V_{bias(row)}$	bias tolerance voltage	R0 to R80		−100	0	+100	mV
LCD supply voltage multiplier							
TC0	LCD voltage temperature coefficient 0			-	0	-	$^1/_{°C}$
TC1	LCD voltage temperature coefficient 1			-	-0.16×10^{-3}	-	$^1/_{°C}$
TC2	LCD voltage temperature coefficient 2			-	-0.33×10^{-3}	-	$^1/_{°C}$
TC3	LCD voltage temperature coefficient 3			-	-0.50×10^{-3}	-	$^1/_{°C}$
TC4	LCD voltage temperature coefficient 4			-	-0.66×10^{-3}	-	$^1/_{°C}$

Table 31. Static characteristics *...continued*

V_{DD1} = 1.7 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = 3 V to 9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TC5	LCD voltage temperature coefficient 5		-	-0.833×10^{-3}	-	1/°C
TC6	LCD voltage temperature coefficient 6		-	-1.25×10^{-3}	-	1/°C
TC7	LCD voltage temperature coefficient 7	[6]	-	-1.66×10^{-3}	-	1/°C
Parallel interface; V_{DD1} = 1.8 V to 3.3 V						
V_i	input voltage		−0.5	-	V_{DD1} + 0.5	V
V_{IL}	LOW-level input voltage		V_{SS}	-	$0.2V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD1}$	-	V_{DD1}	V
Serial interface; V_{DD1} = 1.7 V to 3.3 V						
V_i	input voltage		−0.5	-	V_{DD1} + 0.5	V
V_{IL}	LOW-level input voltage		V_{SS}	-	$0.2V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{DD1}$	-	V_{DD1}	V
I²C-bus interface; V_{DD1} = 1.8 V to 3.3 V						
V_i	input voltage		−0.5	-	+3.3	V
$I_{OL(SDAH)}$	LOW-level output current on pin SDAH	V_{OL} = 0.4 V; $V_{DD1} > 2$ V	3	-	-	mA
		$V_{OL} = 0.2\ V_{DD1}$; $V_{DD1} < 2$ V	2	-	-	mA
V_{IL}	LOW-level input voltage		V_{SS}	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	V_{DD1}	V
Output levels for all interfaces						
V_{OL}	LOW-level output voltage	I_{OL} = 0.5 mA	V_{SS}	-	$0.2V_{DD1}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = −0.5 mA	$0.8V_{DD1}$	-	V_{DD1}	V

[1] The maximum possible V_{LCD} voltage that can be generated is dependent on voltage, temperature and (display) load.

[2] Valid for values of temperature, V_{PR} and TC used at calibration.

[3] During power-down, all static currents are switched off.

[4] Conditions are: V_{DD1} = 1.8 V, V_{DD2} = 2.7 V, V_{LCD} = 8.05 V, voltage multiplier 4 × V_{DD2}, inputs at V_{DD1} or V_{SS}, interface inactive, internal V_{LCD} generation, V_{LCD} output is loaded by 10 μA and T_{amb} = 25 °C.

[5] Normal mode.

[6] TC7 can only be used when $V_{DD2} = V_{DD3}$ = 2.4 V or higher.

17. Dynamic characteristics

Table 32. Dynamic characteristics[1]

V_{DD1} = 1.7 V to 3.3 V; V_{SS} = 0 V; $V_{LCD} \leq 9$ V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ext}	external frequency	external clock	-	200	-	kHz
f_{fr}	frame frequency	T_{amb} = 25 °C; V_{DD1} = 2.4 V	54	60	66	Hz
			43	58	73	Hz
t_{VHRL}	V_{DD} to $\overline{RES}$ LOW	see Figure 48 [2]	0	-	1	µs
t_{RW}	$\overline{RES}$ LOW pulse width	see Figure 48	500	-	-	ns

[1] All specified timings are based on 20 % and 80 % of V_{DD}.

[2] $\overline{RES}$ can be LOW before V_{DD} goes HIGH.

17.1 Parallel interface timing characteristics

Table 33. Parallel interface (6800 series) timing characteristics

V_{DD1} = 1.8 V to 3.3 V; V_{SS} = 0 V; $V_{LCD} \leq 9$ V; T_{amb} = −40 °C to +85 °C; unless otherwise specified, see Figure 41.

Symbol	Parameter	Min	Max	Unit
$t_{SU;DC}$	data/$\overline{command}$ set-up time	40	-	ns
$t_{HD;DC}$	data/$\overline{command}$ hold time	20	-	ns
$T_{cyc(DS)}$	data strobe cycle time	1000	-	ns
$t_{DS(L)}$	data strobe LOW time	320	-	ns
$t_{DS(H)}$	data strobe HIGH time	300	-	ns
$t_{SU;RW}$	read/$\overline{write}$ set-up time	280	-	ns
$t_{HD;RW}$	read/$\overline{write}$ hold time	20	-	ns
$t_{SU;CE}$	chip enable set-up time	280	-	ns
$t_{HD;CE}$	chip enable hold time	0	-	ns
$t_{SU;DAT}$	data set-up time	20	-	ns
$t_{HD;DAT}$	data hold time	40	-	ns
$t_{DAT;ACC}$	data output access time	-	280	ns
$t_{DAT;OH}$	data output disable time	-	20	ns

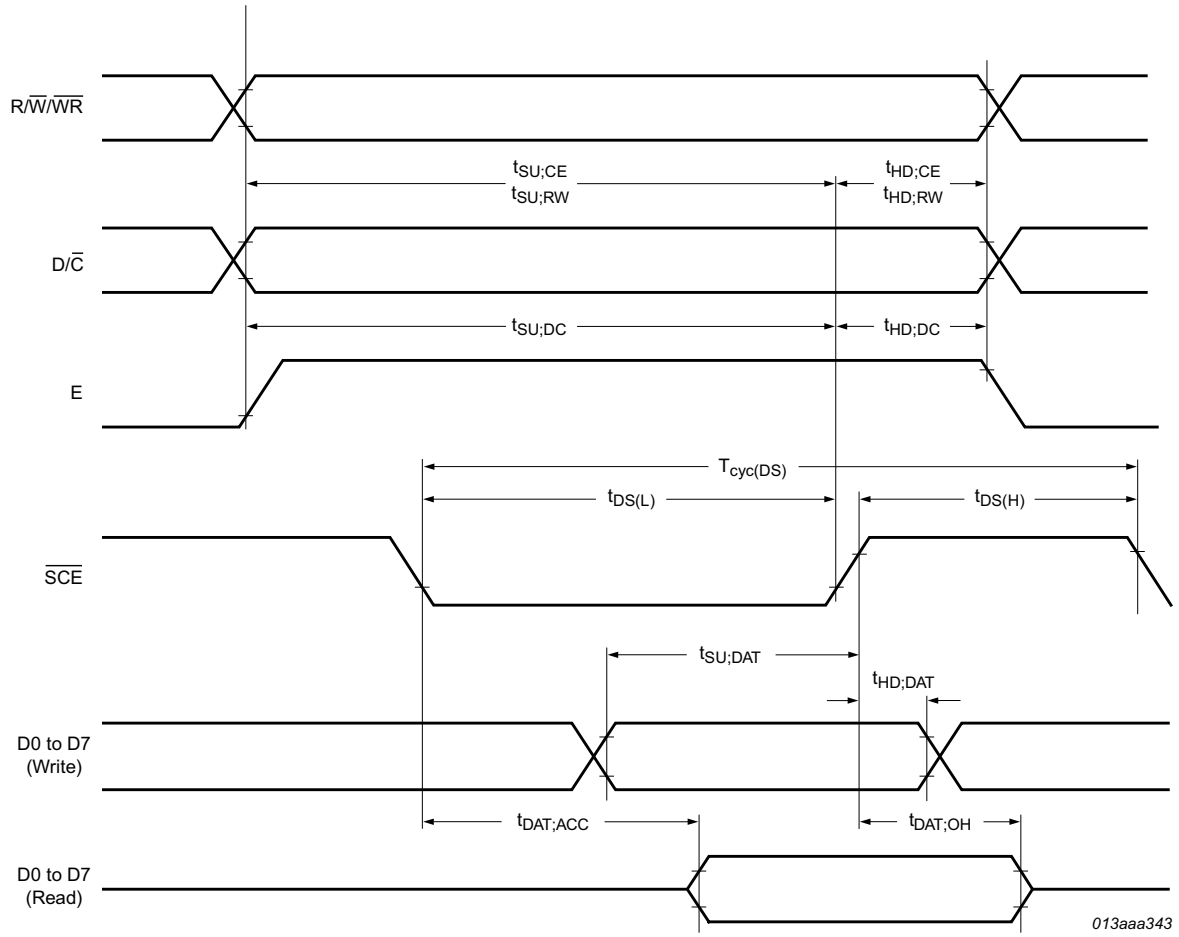


Fig 41. Parallel interface timing; 6800 series

17.2 Serial interface timing characteristics

Table 34. Serial interface timing characteristics[1]

V_{DD1} = 1.8 V to 3.3 V; V_{SS} = 0 V; $V_{LCD} \leq 9$ V; T_{amb} = −40 °C to +85 °C; unless otherwise specified, see Figure 42, Figure 43, Figure 44 and Figure 45.

Symbol	Parameter		Min	Max	Unit
f_{SCLK}	clock frequency		-	9.00	MHz
T_{cyc}	clock cycle SCLK		111	-	ns
t_{PWH1}	SCLK pulse width HIGH		45	-	ns
t_{PWL1}	SCLK pulse width LOW		45	-	ns
t_{S2}	$\overline{SCE}$ set-up time		50	-	ns
t_{H2}	$\overline{SCE}$ hold time		45	-	ns
t_{PWH2}	$\overline{SCE}$ minimum HIGH time		50	-	ns
t_{H5}	$\overline{SCE}$ start hold time	[2]	50	-	ns
t_{S3}	data/$\overline{command}$ set-up time		50	-	ns
t_{H3}	data/$\overline{command}$ hold time		50	-	ns
t_{S1}	SDATA set-up time		50	-	ns
t_{H1}	SDATA hold time		50	-	ns
t_1	SDO access time		-	50	ns
t_2	SDO disable time	[3]	-	50	ns
t_3	$\overline{SCE}$ hold time		50	-	ns
t_4	SDO disable time	[4]	25	100	ns
C_b	capacitive load for SDO	[5]	-	30	pF
R_b	series resistance for SDO	[5]	-	500	Ω

[1] All specified timings are based on 20 % and 80 % of V_{DD}.

[2] t_{H5} is the time from the previous SCLK rising edge (irrespective of the state of $\overline{SCE}$) to the falling edge of $\overline{SCE}$.

[3] SDO disable time for SPI 3-line or 4-line.

[4] SDO disable time for 3-line serial interface.

[5] Maximum values are for f_{SCLK} = 9 MHz. Series resistance includes ITO track + connector resistance + printed-circuit board.

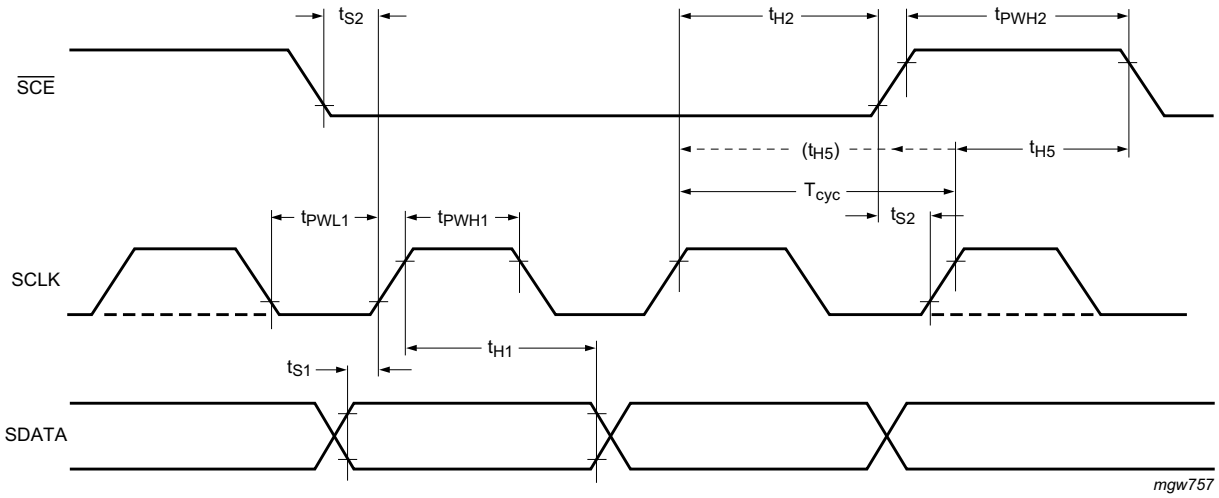


Fig 42. 3-line serial interface timing

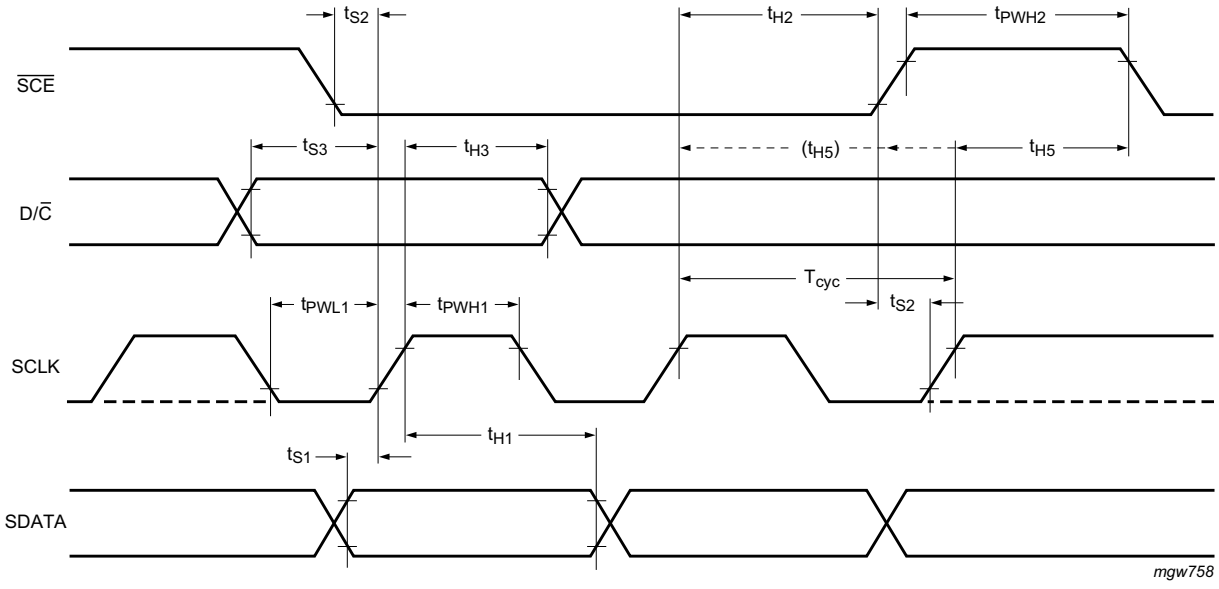


Fig 43. 4-line serial interface timing

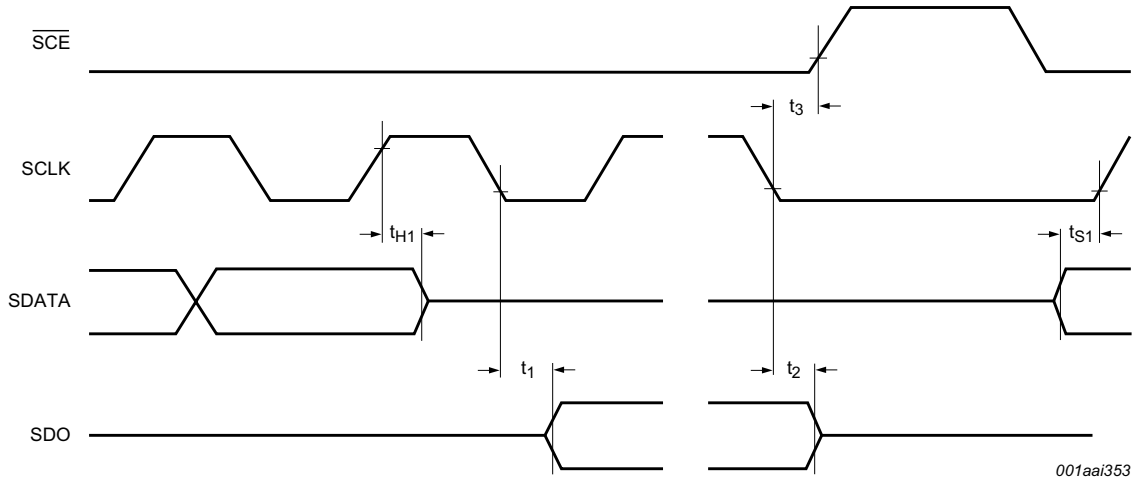


Fig 44. Serial interface timing; SPI 3-line or 4-line (read mode)

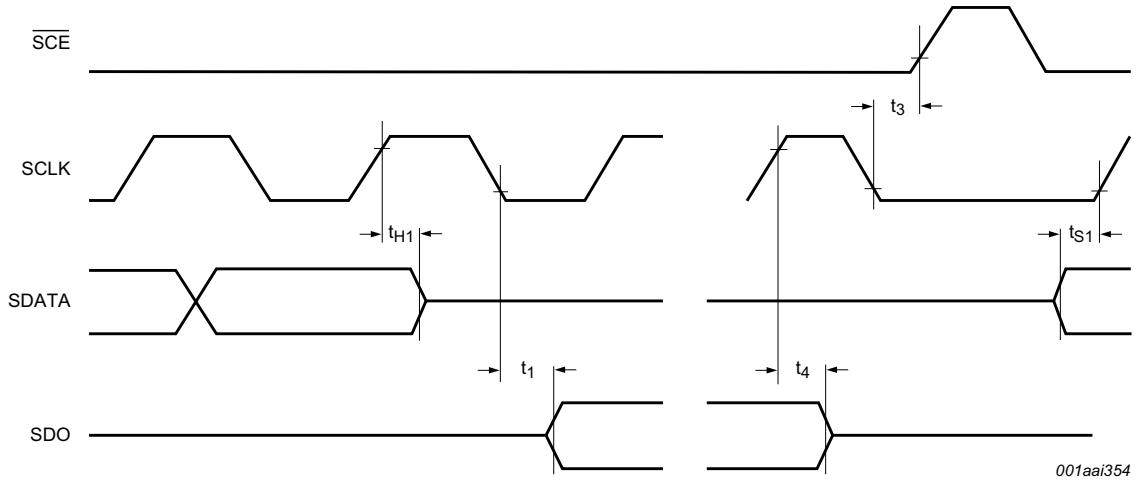


Fig 45. Serial interface timing; 3-line serial interface (read mode)

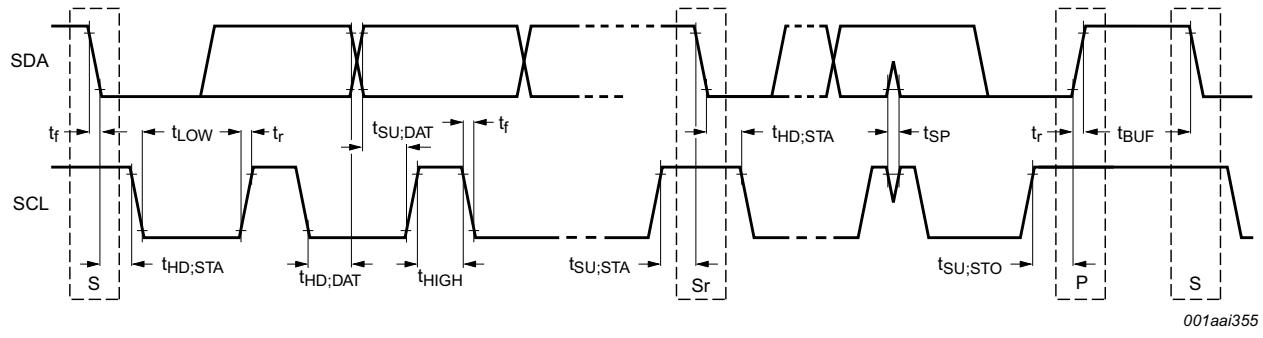
17.3 I²C-bus interface timing characteristics

Table 35. I²C-bus characteristics; F/S-mode

V_{DD1} = 1.8 V to 3.3 V; V_{SS} = 0 V; $V_{LCD} \leq 9$ V; T_{amb} = −40 °C to +85 °C; unless otherwise specified[1], see Figure 46.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		0	-	400	kHz
$t_{SU;STA}$	set-up time for a repeated START condition		600	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		600	-	-	ns
t_{LOW}	LOW period of the SCL clock		1300	-	-	ns
t_{HIGH}	HIGH period of the SCL clock		600	-	-	ns
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	900	ns
t_r	rise time of both SDA and SCL signals		20 + 0.1C_b	-	300	ns
t_f	fall time of both SDA and SCL signals		20 + 0.1C_b	-	300	ns
C_b	capacitive load for each bus line		-	-	400	pF
$t_{SU;STO}$	set-up time for STOP condition		600	-	-	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	-	50	ns
t_{BUF}	bus free time between a STOP and START condition		1300	-	-	ns
V_{nL}	noise margin at the LOW level	for each connected device (including hysteresis)	0.1V_{DD1}	-	-	V
V_{nH}	noise margin at the HIGH level	for each connected device (including hysteresis)	0.2V_{DD1}	-	-	V

[1] All specified timings are based on 20 % and 80 % of V_{DD}.



S = start

Sr = start repeated

P = stop

Fig 46. I²C-bus timing diagram (F/S-mode)

Table 36. I²C-bus characteristics; Hs-mode

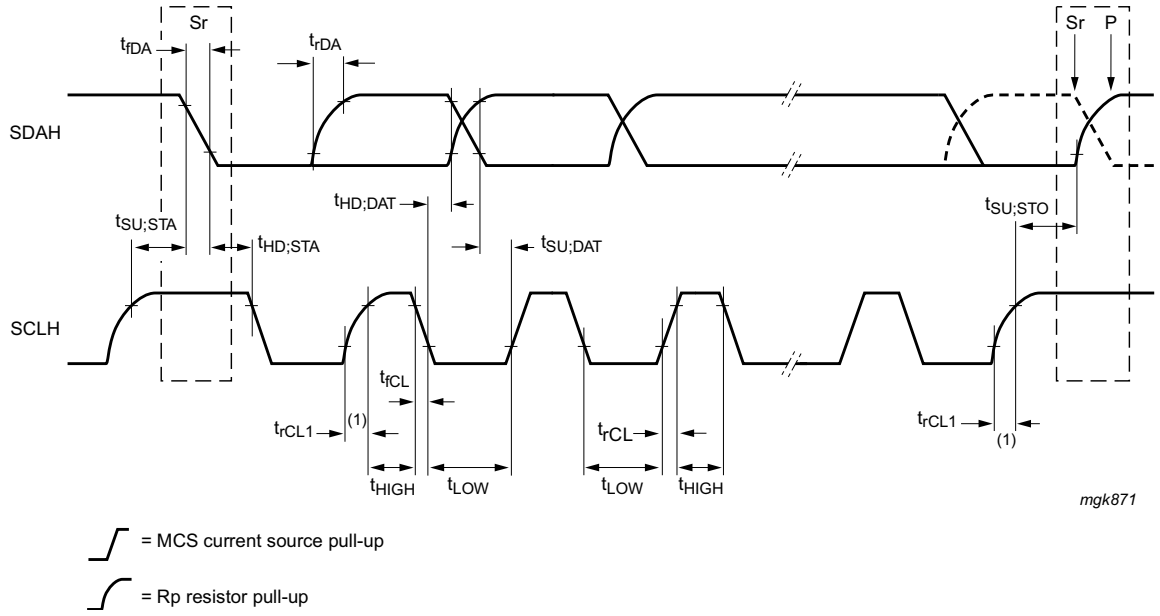
V_{DD1} = 1.8 V to 3.3 V; V_{SS} = 0 V; $V_{LCD} \leq 9$ V; T_{amb} = −40 °C to +85 °C; unless otherwise specified[1], see Figure 47.

Symbol	Parameter	Conditions	C_b = 100 pF (max)		C_b = 400 pF[2]		Unit
			Min	Max	Min	Max	
f_{SCLH}	SCLH clock frequency		0	3.4	0	1.7	MHz
$t_{SU;STA}$	set-up time for a repeated START condition		160	-	160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		160	-	160	-	ns
t_{LOW}	LOW period of the SCLH clock		160	-	320	-	ns
t_{HIGH}	HIGH period of the SCLH clock		60	-	120	-	ns
$t_{SU;DAT}$	data set-up time		10	-	10	-	ns
$t_{HD;DAT}$	data hold time		20[3]	70	20[3]	150	ns
t_{rCL}	rise time of SCLH signal		10	40	20	80	ns
t_{rCL1}	rise time of SCLH signal after a repeated START condition and after an acknowledge bit		10	80	20	160	ns
t_{fCL}	fall time of SCLH signal		10	40	20	80	ns
t_{rDA}	rise time of SDAH signal		10	80	20	160	ns
t_{fDA}	fall time of SDAH signal		10	80	20	160	ns
$t_{SU;STO}$	set-up time for STOP condition		160	-	160	-	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	SDAH and SCLH	0	5	0	5	ns
C_b	capacitive load for each bus line	SDAH and SCLH lines [2]	0	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	0	400	-	400	pF
V_{nL}	noise margin at the LOW level	for each connected device (including hysteresis)	$0.1V_{DD1}$	-	$0.1V_{DD1}$	-	V
V_{nH}	noise margin at the HIGH level	for each connected device (including hysteresis)	$0.2V_{DD2}$	-	$0.2V_{DD2}$	-	V

[1] All specified timings are based on 20 % and 80 % of V_{DD}.

[2] For bus line loads C_b between 100 pF and 400 pF the timing parameters must be linearly interpolated.

[3] A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.



(1) Rising edge of the first SCLH clock pulse after an acknowledge bit.

Fig 47. I²C-bus timing diagram (Hs-mode)

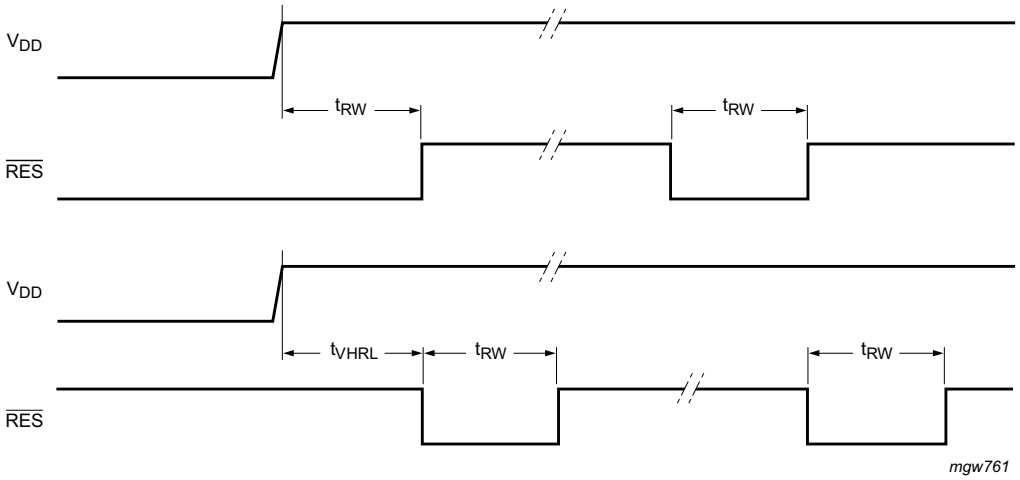


Fig 48. Reset timing

18. Application information

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. In this application, the IC must be protected against light. The protection has to be done on all sides of the IC, i.e. front, rear and all edges.

The pinning of the PCF8811 has an optimum design for single plane wiring e.g. for chip-on-glass display modules. Display size: 80 × 128 pixels.

For further application information, refer to NXP Semiconductors Application Note *AN10170 Design guidelines for COG modules with NXP monochrome LCD drivers*.

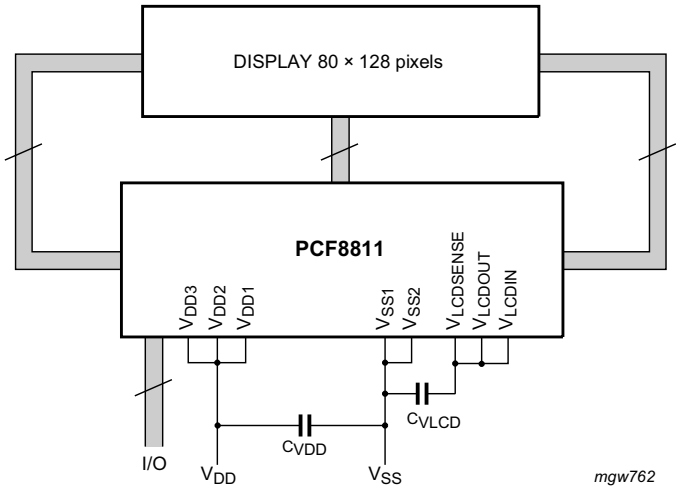


Fig 49. Application diagram: internal charge pump and a single supply

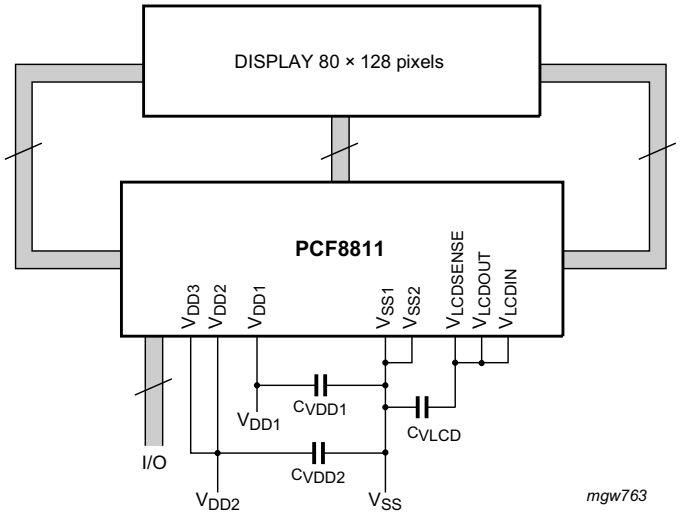


Fig 50. Application diagram: internal charge pump and two separate supplies (V_{DD1} and V_{DD2})

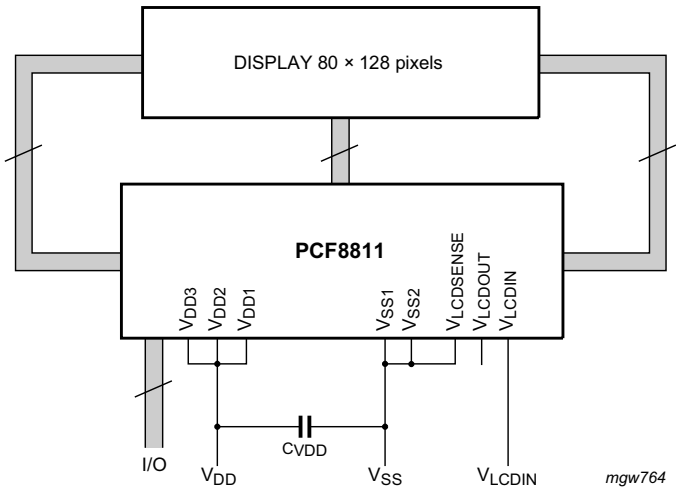


Fig 51. Application diagram: external high voltage

The required minimum value for the external capacitors in an application with the PCF8811 are:

C_{VLCD} = 1.0 μF to 4.7 μF depending on the application.

C_{VDD}, C_{VDD1}, C_{VDD2} = 1.0 μF. For these capacitors, higher values can be used.

19. Support information

19.1 Module maker programming

One Time Programmable (OTP) technology is implemented on the PCF8811. It enables the module maker to program some extended features of the PCF8811 after it has been assembled on an LCD module. Programming is made under the control of the interfaces and the use of one special pin. This pin must be made available on the module glass but do not need to be accessed by the set maker.

The PCF8811 features 3 parameters programmable by the module maker:

- V_{LCD} calibration
- Temperature coefficient selection
- Seal bit

19.1.1 V_{LCD} calibration

The first feature included is the ability to adjust the V_{LCD} voltage with a 5-bit code (MMVOPCAL). This code is implemented in two's complement notation causing a positive or negative offset to the V_{PR} register. This is in the same manner as the on-glass calibration pins V_{OS}.

In theory, both may be used together but it is recommended that the V_{OS} pins are tied to V_{SS} when OTP calibration is being used. This sets them to a default offset of zero. If both are used, then the addition of the two 5-bit numbers must not exceed a 5-bit result,

otherwise the resultant value is undefined. The final adder in the circuit has underflow and overflow protection. In the event of overflow, the output is clamped to 255; during an underflow the output is clamped to 0.

The final control to the high-voltage multiplier, V_{OP}, is the sum of all the calibration registers and pins. The V_{LCD} Equation 4 or Equation 5 given in Section 12.10.1 or Section 12.10.2 must be extended to include the OTP calibration, as follows:

$$V_{LCD(T = T_{CUT})} = a + (V_{OS}[4:0] + MMVOPCAL[4:0] + V_{OP}[7:0]) \times b \quad (7)$$

The possible values for MMVOPCAL[4:0] and V_{OS}[4:0] values are given in Table 37.

Table 37. V_{OS}/MMVOPCAL values in two's complement notation

Binary	Decimal	Binary	Decimal
0 0000	0	1 1111	–1
0 0001	+1	1 1110	–2
0 0010	+2	1 1101	–3
0 0011	+3	1 1100	–4
0 0100	+4	1 1011	–5
0 0101	+5	1 1010	–6
0 0110	+6	1 1001	–7
0 0111	+7	1 1000	–8
0 1000	+8	1 0111	–9
0 1001	+9	1 0110	–10
0 1010	+10	1 0101	–11
0 1011	+11	1 0100	–12
0 1100	+12	1 0011	–13
0 1101	+13	1 0010	–14
0 1110	+14	1 0001	–15
0 1111	+15	1 0000	–16

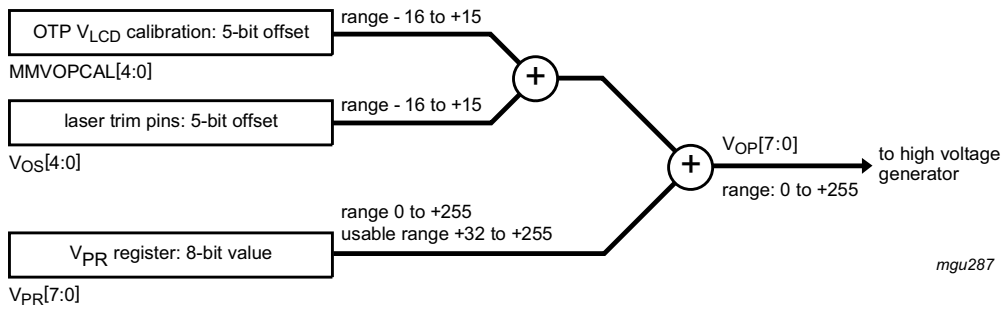


Fig 52. V_{LCD} calibration

19.1.2 Temperature coefficient selection

The second feature is an OTP factory default setting for the temperature coefficient selection (MMTC) in the basic command set. This 3-bit value will be loaded from OTP after leaving the power-save mode or by the refresh command. The idea of this feature is

to provide, in the basic command set, the complete set of temperature coefficients without an additional command. In the extended command set, the temperature coefficient can be programmed as given in Table 21 and Table 31.

19.1.3 Seal bit

The module maker programming is performed in a special mode: the calibration mode (CALMM). This mode is entered via a special interface command, CALMM, see Table 12 andTable 39. To prevent unwanted programming, a seal bit has been implemented which prevents the device from entering the calibration mode. This seal bit, once programmed, cannot be reversed so further changes in programmed values are not possible.

Applying the programming voltages when not in CALMM mode has no effect on the programmed values.

Table 38. Seal bit definition

Seal bit	Action
0	possible to enter calibration mode
1	calibration mode disabled

19.1.4 OTP architecture

The OTP circuitry in the PCF8811 contains 9 bits of data: 5 for V_{LCD} calibration (MMVOPCAL), 3 for the temperature coefficient default setting in the basic command set MMTC and 1 seal bit. The circuitry for 1-bit is called an OTP slice. Each OTP slice consists of 2 main parts: the OTP cell (a non-volatile memory cell) and the shift register cell (a flip-flop). The OTP cells are only accessible through their shift register cells: on the one hand both reading from and writing to the OTP cells is performed with the shift register cells, on the other hand only the shift register cells are visible to the rest of the circuit. The basic OTP architecture is shown in Figure 53.

This OTP architecture allows the following operations:

Reading data from the OTP cells — The content of the non-volatile OTP cells is transferred to the shift register where upon it may affect the PCF8811 operation.

Writing data to the OTP cells — All 9 data bits are shifted into the shift register via the interface. The content of the shift register is then transferred to the OTP cells. There are some limitations related to storing data in these cells, see Section 19.1.7.

Checking calibration without writing to the OTP cells — Shifting data into the shift register allows the effects on the V_{LCD} voltage to be observed.

The reading of data from the OTP cells is initiated by either:

- Exit from power-save mode
- The refresh command (power control)

Remark: In both cases, the reading operation needs up to 5 ms to complete.

The shifting of data into the shift register is performed in the special mode CALMM. In the PCF8811, the CALMM mode is entered by the CALMM command. Once in the CALMM mode the data is shifted into the shift register via the interface at the rate of 1-bit per command. After transmitting the last (9^{th}) bit and exiting the CALMM mode, the serial

interface will return to the normal mode and all other commands can be sent. Care should be taken that 9 bits of data (or a multiple of 9) are always transferred before exiting the CALMM mode, otherwise the bits are in the wrong positions.

In the shift register, the value of the seal bit is, like the others, always zero at reset. To ensure that the security feature (seal bit) works correctly, the CALMM command is disabled until a refresh has been performed. Once the refresh is completed, the seal bit value in the shift register is valid and permission to enter the CALMM mode can thus be determined.

The 9 bits are shifted into the shift register in a predefined order: first 5 bits of MMVOPCAL[4:0], 3 bits for MMTC[2:0] and lastly the seal bit. The MSB is always first, thus the first bit shifted is MMVOPCAL[4] and the two last bits are MMTC[0] and the seal bit.

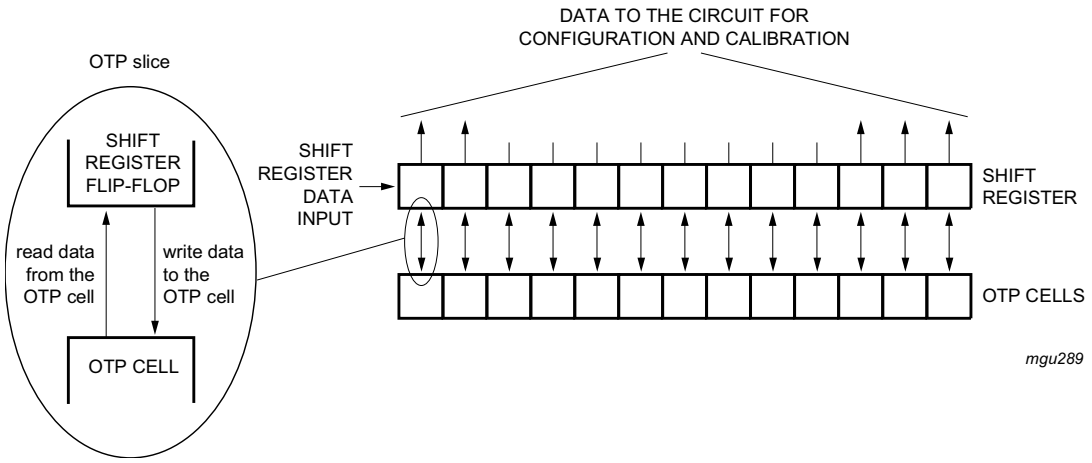


Fig 53. Basic OTP architecture

19.1.5 Interface commands

These instructions are in addition to those indicated in Table 12.

Table 39. Additional interface commands

Instruction	Pin			Command byte								Description
	EXT	D/C	R/W/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
CALMM	X[1]	0	0	1	0	0	0	0	0	1	0	enter CALMM mode
Power control (refresh)	X[1]	0	0	0	0	1	0	1	PC1	PC0	1	switch HVgen on/off to force a refresh of the shift register

[1] X = value without meaning.

19.1.5.1 CALMM

This instruction puts the device in calibration mode. This mode enables the shift register for loading and allows programming of the non-volatile OTP cells to take place. If the seal bit is set, then this mode cannot be accessed and the instruction is ignored. Once in calibration mode all commands are interpreted as shift register data. The mode can only be exited by sending data with DB7 set to logic 0. Reset also clears this mode. Each shift

register data byte is preceded by D/$\overline{C}$ = 0 and has only 2 significant bits, thus the remaining 6 bits are ignored. DB7 is the continuation bit (DB7 = 1 remain in CALMM mode, DB7 = 0 exit CALMM mode). DB0 is the data bit and its value is shifted into the OTP shift register (on the falling edge of SCLK).

19.1.5.2 Refresh

The action of the refresh instruction is to force the OTP shift register to reload from the non-volatile OTP cells. This instruction takes up to 5 ms to complete. During this time, all other instructions may be sent.

In the PCF8811, the refresh instruction is associated with the power control instruction so that the shift register is automatically refreshed every time the high voltage multiplier is enabled or disabled. If this instruction is sent while in power-save mode, the PC[1:0] bits are updated but the refreshing is ignored.

19.1.6 Example sequence for filling the shift register

An example of the sequence of commands and data is shown in Table 40. In this example the shift register is filled with the following data: MMVOPCAL = −4 (1 1100b), MMTC = 2 (010b) and the seal bit is logic 0.

It is assumed that the PCF8811 has just been reset. After transmitting the last bit the PCF8811 can either exit or remain in the CALMM mode, see Table 40, Step 1. While in CALMM mode the interface does not recognize commands in the normal sense. After this sequence has been applied, it is possible to observe the impact of the data shifted in. The described sequence is, however, not useful for OTP programming because the number of bits with the value logic 1 is greater than that allowed for programming, see Section 19.1.7. The shift register after this action is shown in Figure 54.

Table 40. Sequence for filling the shift register; example 1

X = value without meaning.

Step	Pin			Command byte								Action
	EXT	D/$\overline{C}$	R/$\overline{W}$/$\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	X	0	0	1	1	1	0	0	0	0	1	exit power-down
2	-	-	-	-	-	-	-	-	-	-	-	wait 5 ms for refresh to take effect
3	X	0	0	1	0	0	0	0	0	1	0	enter CALMM mode
4	X	0	0	1	X	X	X	X	X	X	1	shift in data; MMVOPCAL[4] is first bit [1]
5	X	0	0	1	X	X	X	X	X	X	1	MMVOPCAL[3]
6	X	0	0	1	X	X	X	X	X	X	1	MMVOPCAL[2]
7	X	0	0	1	X	X	X	X	X	X	0	MMVOPCAL[1]
8	X	0	0	1	X	X	X	X	X	X	0	MMVOPCAL[0]
9	X	0	0	1	X	X	X	X	X	X	0	MMTC[2]
10	X	0	0	1	X	X	X	X	X	X	1	MMTC[1]
11	X	0	0	1	X	X	X	X	X	X	0	MMTC[0]
12	X	0	0	0	X	X	X	X	X	X	0	seal bit; exit CALMM mode
An alternative ending could be to stay in CALMM mode												
13	X	0	0	1	X	X	X	X	X	X	0	seal bit; remain in CALMM mode

[1] The data for the bits is not in the correct shift register position until all bits have been sent.

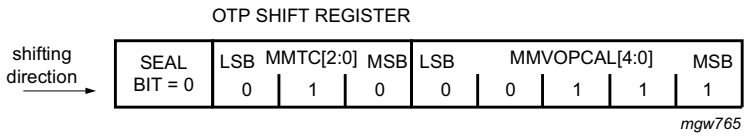


Fig 54. Shift register contents after example sequence, see Table 40

19.1.7 Programming flow

Programming is achieved while in CALMM mode and with the application of the programming voltages. As mentioned previously, the data for programming the OTP cell is contained in the corresponding shift register cell. In order to program the corresponding OTP cell, the shift register cell must be loaded with a logic 1. If the shift register cell contains a logic 0, then no action takes place when the programming voltages are applied.

Once programmed, an OTP cell cannot be de-programmed. An already programmed cell, i.e. an OTP cell containing a logic 1, must not be reprogrammed.

During programming, a substantial current flows in the V_{LCDIN} pin. For this reason, it is recommended to program only one OTP cell at a time by filling all but one shift register cells with logic 0.[2]

The programming specification refers to the voltages at the chip pins, contact resistance must therefore be considered by the user.

An example sequence of commands and data for OTP programming is given in Table 41. It is assumed that the PCF8811 has just been reset.

The order for programming cells is not significant. However, NXP Semiconductors recommends that the seal bit is programmed last. Once this bit has been programmed and the CALMM mode is exited, it is not possible to reenter the CALMM mode.

Table 41. Sequence for filling the shift register; example 2

X = value without meaning.

Step	Pin			Command byte								Action
	EXT	D/$\overline{C}$	R/$\overline{W}$/$\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	X	0	0	1	1	1	0	0	0	0	1	exit power-save
2	-	-	-	-	-	-	-	-	-	-	-	wait 5 ms for refresh to take effect
3	X	0	0	1	0	1	0	1	0	0	1	reenter power-down (DON = 0)
4	X	0	0	1	0	0	0	0	0	1	0	enter CALMM mode
5	X	0	0	1	X	X	X	X	X	X	1	shift in data; MMVOPCAL[4] is first bit
6	X	0	0	1	X	X	X	X	X	X	1	MMVOPCAL[3]
7	X	0	0	1	X	X	X	X	X	X	1	MMVOPCAL[2]
9	X	0	0	1	X	X	X	X	X	X	0	MMVOPCAL[1]
10	X	0	0	1	X	X	X	X	X	X	0	MMVOPCAL[0]
11	X	0	0	1	X	X	X	X	X	X	0	MMTC[2]
12	X	0	0	1	X	X	X	X	X	X	1	MMTC[1]
13	X	0	0	1	X	X	X	X	X	X	0	MMTC[0]

2. The examples in Table 40 and Table 41 are not in line with this recommendation since more than one cell is set to 1 at a time.

Table 41. Sequence for filling the shift register; example 2 *…continued*

X = value without meaning.

Step	Pin			Command byte								Action
	EXT	D/$\overline{C}$	R/$\overline{W}$/$\overline{WR}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
14	X	0	0	1	X	X	X	X	X	X	0	seal bit
15	-	-	-	-	-	-	-	-	-	-	-	apply programming voltage at pins $V_{OTPPROG}$ and V_{LCDIN}, see Section 19.1.8
Repeat steps 5 to 14 (9 bits, see Section 19.1.4) for each bit which must be programmed to 1; exit CALMM mode												
16	-	-	-	-	-	-	-	-	-	-	-	apply external reset

19.1.8 Programming specification

Table 42. Programming specification

See Figure 55.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{OTPPROG}$	voltage applied to pin $V_{OTPPROG}$ relative to V_{SS1}	programming active	[1]	11	11.5	12	V
		programming inactive	[1]	V_{SS} − 0.2	0	V_{SS} + 0.2	V
V_{LCDIN}	voltage applied to pin V_{LCDIN} relative to V_{SS1}	programming active	[1][2]	9	9.5	10	V
		programming inactive	[1][2]	V_{DD2} − 0.2	V_{DD2}	4.5	V
I_{LCDIN}	current drawn by V_{LCDIN} during programming	when programming a single bit to logic 1		-	850	1000	μA
$I_{VOTPPROG}$	current drawn by $V_{OTPPROG}$ during programming			-	100	200	μA
$T_{amb(PROG)}$	ambient temperature during programming			0	25	40	°C
$t_{SU;SCLK}$	set-up time of internal data after last clock			1	-	-	μs
$t_{HD;SCLK}$	hold time of internal data before next clock			1	-	-	μs
$t_{SU;VOTPPROG}$	set-up time of $V_{OTPPROG}$ prior to programming			1	-	10	μs
$t_{HD;VOTPPROG}$	hold time of $V_{OTPPROG}$ after programming			1	-	10	ms
t_{PW}	pulse width of programming voltage			100	120	200	ms

[1] The voltage drop across the ITO track and zebra connector must be taken into account to guarantee a sufficiently high voltage at the chip pins.

[2] The power-down mode (DON = 0 and DAL = 1) and CALMM mode must be active while the V_{LCDIN} pin is being driven.

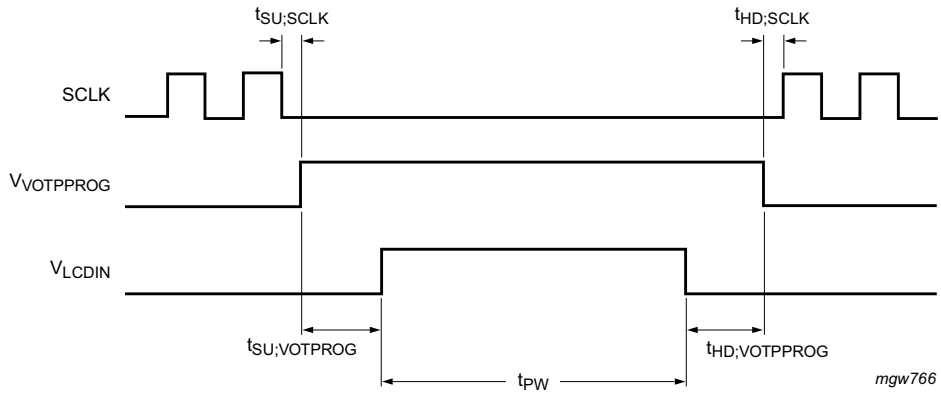


Fig 55. Programming waveforms

20. Package outline

Not applicable.

21. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

22. Packing information

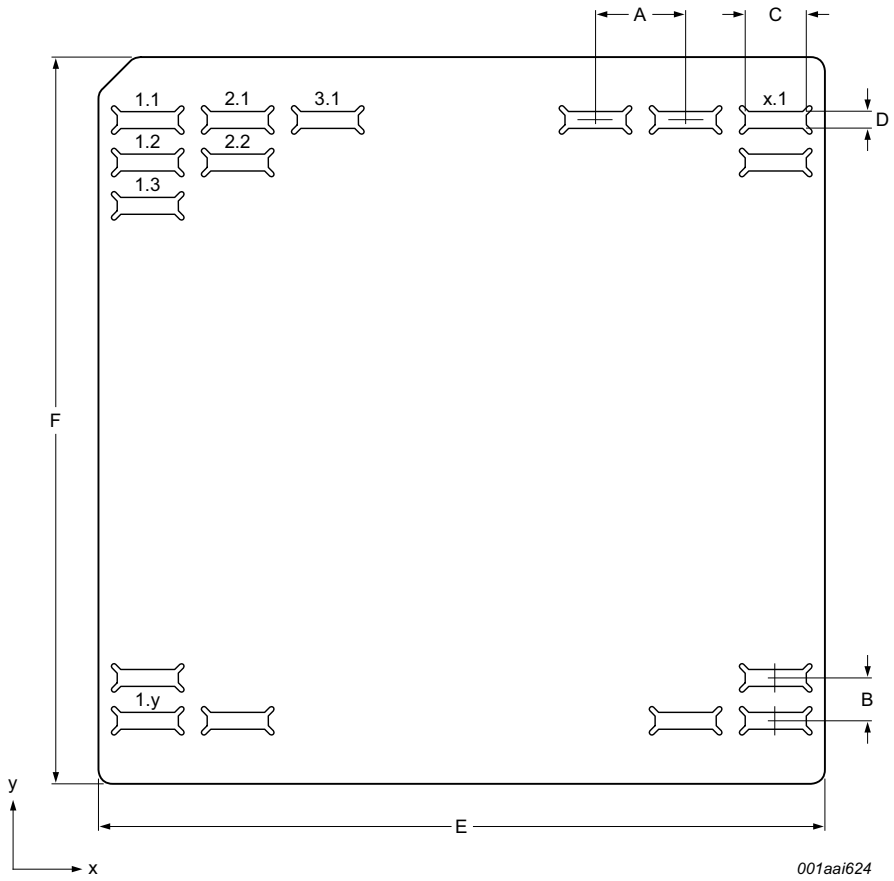


Fig 56. Tray details

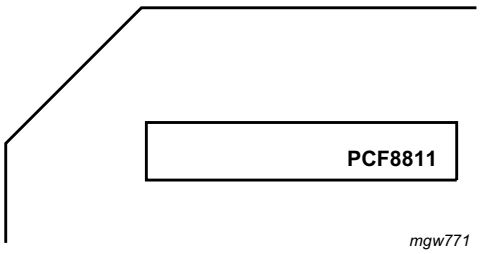


Fig 57. Tray alignment

Table 43. Tray dimensions

See Figure 56.

Symbol	Description	Value
A	pocket pitch in x direction	20.12 mm
B	pocket pitch in y direction	4.09 mm
C	pocket width in x direction	12.55 mm
D	pocket width in y direction	2.41 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
x	number of pockets, x direction	2
y	number of pockets, y direction	11

The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pin location diagram (Figure 2) for the orientation and position of the type name on the die surface.

23. Appendix

23.1 LCD graphic driver selection

Table 44. Selection of LCD graphic drivers

Type name	Max display resolution rows × col.	Multiplex rates	V_{DD1} (V)	V_{DD2} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)
PCA8539DUG	18 × 100	1:12, 1:18	2.5 to 5.5	2.5 to 5.5	4 to 16	45 to 360[1]	Y	Y	–40 to 105
PCF8539DUG	18 × 100	1:12, 1:18	2.5 to 5.5	2.5 to 5.5	4 to 16	45 to 360[1]	Y	Y	–40 to 85
PCF8531U	34 × 128 or 33 × 128 plus 128 icons	1:17, 1:26, 1:34	1.8 to 5.5	2.5 to 4.5	4 to 9	66	Y	Y	–40 to 85
PCF8811U	80 × 128 or 79 × 129 plus 128 icons	1:16 to 1:80 in steps of 8	2 to 3.3	1.8 to 3.3	3 to 9	30 to 60[1]	Y	Y	–40 to 85

[1] Can be selected by command.

24. Abbreviations

Table 45. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
COG	Chip-On-Glass
DDRAM	Double Data Random Access Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
HV	High Voltage
IC	Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MRA	Multiple Row Addressing
MSB	Most Significant Bit
MPU	MicroProcessing Unit
OTP	One Time Programmable
RAM	Random Access Memory
SPI	Serial Peripheral Interface
TC	Temperature Coefficient
TCP	Tape Carrier Packages

25. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN11267 —** EMC and system level ESD design guidelines for LCD drivers

[3] **AN10706 —** Handling bare die

[4] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **UM10569 —** Store and transport requirements

[11] **UM10204 —** I^2C-bus specification and user manual

26. Revision history

Table 46. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8811 v.6	20150210	Product data sheet	-	PCF8811 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Fixed typos • Enhanced description of DS0, see Section 7.1.9			
PCF8811 v.5	20100629	Product data sheet	-	PCF8811 v.4
PCF8811 v.4	20080627	Product data sheet	-	PCF8811 v.3
PCF8811 v.3	20040517	Product specification	-	PCF8811 v.2
PCF8811 v.2	20021204	Product specification	-	PCF8811 v.1
PCF8811 v.1	20020814	Product specification	-	-

27. Legal information

27.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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29. Tables

Table 1. Ordering information 2
Table 2. Pin description 5
Table 3. Bump and pad dimensions 7
Table 4. Alignment marker position[1] 7
Table 5. Bump locations 7
Table 6. Device recognition 18
Table 7. Command set selection 18
Table 8. Interface selection 18
Table 9. 6800 series parallel interface functions 28
Table 10. I^2C slave address byte 35
Table 11. Co and D/$\overline{C}$ definitions 36
Table 12. Instruction set[1] 41
Table 13. Common commands 44
Table 14. Power control register[1] 44
Table 15. Power-save mode (PSM), OS, DON, DAL and E combinations[1] 45
Table 16. Read status byte 45
Table 17. Multiplication settings 45
Table 18. Specific basic commands 45
Table 19. Specific extended commands 45
Table 20. Frame rate frequency 46
Table 21. Temperature coefficient[1] 46
Table 22. Multiplication settings 46
Table 23. RAM X/Y address range 49
Table 24. Bias levels for MRA driving method 52
Table 25. Relationship between multiplex rates and bias setting variables without icon row 52
Table 26. Relationship between multiplex rates and bias setting variables with the icon row (only extended command set) 53
Table 27. Example values of V_{PR}, V_{OP} and V_{OFF} for V_{LCD} = 6 V 54
Table 28. Parameters of V_{LCD} for the basic and extended command set 55
Table 29. ROM look-up table with values of V_{OFF}, V_{PR}, V_{OP} and V_{LCD} 56
Table 30. Limiting values[1] 63
Table 31. Static characteristics 64
Table 32. Dynamic characteristics[1] 66
Table 33. Parallel interface (6800 series) timing characteristics 66
Table 34. Serial interface timing characteristics[1] 68
Table 35. I^2C-bus characteristics; F/S-mode 71
Table 36. I^2C-bus characteristics; Hs-mode 72
Table 37. V_{OS}/MMVOPCAL values in two's complement notation 76
Table 38. Seal bit definition 77
Table 39. Additional interface commands 78
Table 40. Sequence for filling the shift register; example 1 79
Table 41. Sequence for filling the shift register; example 2 80
Table 42. Programming specification 81
Table 43. Tray dimensions 84
Table 44. Selection of LCD graphic drivers 85
Table 45. Abbreviations 86
Table 46. Revision history 88

30. Figures

Fig 1. Block diagram of PCF8811 3
Fig 2. Pin configuration for PCF8811 4
Fig 3. Chip dimensions 6
Fig 4. Alignment markers 7
Fig 5. DDRAM to display mapping 22
Fig 6. Sequence of writing data bytes into the RAM (basic command set) 23
Fig 7. Sequence of writing data bytes into the RAM with horizontal addressing; V = 0 (extended command set) 24
Fig 8. Sequence of writing data bytes into the RAM with vertical addressing; V = 1 (extended command set) 24
Fig 9. RAM byte organization, if DOR = 0 (extended command set) 25
Fig 10. RAM byte organization, if DOR = 1 (extended command set) 25
Fig 11. RAM format addressing; MX = 1 (both command sets) 26
Fig 12. RAM format addressing; MX = 0 (both command sets) 26
Fig 13. RAM format addressing; MY = 1 (both command sets) 27
Fig 14. RAM format addressing; MY = 0 (both command sets) 27
Fig 15. Serial bus protocol: transmission of 1 byte 29
Fig 16. Serial bus protocol: transmission of several bytes 29
Fig 17. Transmission of several bytes 29
Fig 18. Transmission interrupted by $\overline{SCE}$ 30
Fig 19. Read mode SPI 3-line and 4-line 30
Fig 20. Serial data stream; write mode 31
Fig 21. Write mode: a control bit followed by a transmission byte 32
Fig 22. Write mode: transmission of several bytes 32
Fig 23. Write mode: interrupted by reset ($\overline{RES}$) 32
Fig 24. Read mode: serial interface 3-line 33
Fig 25. System configuration 34
Fig 26. Bit transfer 34
Fig 27. Definition of START and STOP conditions 34
Fig 28. Acknowledge on the I^2C-bus 35
Fig 29. I^2C-bus protocol 36
Fig 30. Control byte format 36
Fig 31. Data transfer format in Hs-mode 37
Fig 32. Data transfer timing format in F/S-mode and Hs-mode 38
Fig 33. Master transmits in Hs-mode to slave receiver; write mode 39
Fig 34. Master receives from slave transmitter (status register is read); read mode 39
Fig 35. Programming the L[6:0] address and C[6:0] address when MY = 0 50
Fig 36. Bias levels for an MRA system with p = 8 and G_{max} = F 51
Fig 37. Setting of V_{OP} in the basic and extended command set 54
Fig 38. V_{LCD} programming of the PCF8811 59
Fig 39. Temperature coefficients 60
Fig 40. Device protection diagrams 61
Fig 41. Parallel interface timing; 6800 series 67
Fig 42. 3-line serial interface timing 69
Fig 43. 4-line serial interface timing 69
Fig 44. Serial interface timing; SPI 3-line or 4-line (read mode) 70
Fig 45. Serial interface timing; 3-line serial interface (read mode) 70
Fig 46. I^2C-bus timing diagram (F/S-mode) 71
Fig 47. I^2C-bus timing diagram (Hs-mode) 73
Fig 48. Reset timing 73
Fig 49. Application diagram: internal charge pump and a single supply 74
Fig 50. Application diagram: internal charge pump and two separate supplies (V_{DD1} and V_{DD2}) 74
Fig 51. Application diagram: external high voltage 75
Fig 52. V_{LCD} calibration 76
Fig 53. Basic OTP architecture 78
Fig 54. Shift register contents after example sequence, see Table 40 80
Fig 55. Programming waveforms 82
Fig 56. Tray details 83
Fig 57. Tray alignment 83

31. Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Ordering information 2
5 Block diagram 3
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 5
6.2.1 Tie-off pins 6
6.2.2 Bare die information 6
7 Functional description 17
7.1 Pin functions 17
7.1.1 R0 to R80: row driver outputs 17
7.1.2 C0 to C127: column driver signals 17
7.1.3 V_{SS1} and V_{SS2}: negative power supply rails . . 17
7.1.4 V_{DD1} to V_{DD3}: positive power supply rails 17
7.1.5 $V_{OTPPROG}$: OTP power supply 17
7.1.6 V_{LCDOUT}, V_{LCDIN}, and $V_{LCDSENSE}$: LCD power supply 17
7.1.7 T1 to T5: test pins 17
7.1.8 MF2 to MF0 18
7.1.9 DS0 18
7.1.10 V_{OS4} to V_{OS0} 18
7.1.11 EXT: extended command set 18
7.1.12 PS0, PS1, and PS2 18
7.1.13 D/$\overline{C}$ 18
7.1.14 R/$\overline{W}$/$\overline{WR}$ 19
7.1.15 E/$\overline{RD}$ 19
7.1.16 SCLH/$\overline{SCE}$ 19
7.1.17 SDAH 19
7.1.18 SDAHOUT 19
7.1.19 DB7 to DB0 19
7.1.19.1 DB7 to DB0 (parallel interface) 19
7.1.19.2 DB7, DB6 and DB5 (serial interface) 19
7.1.19.3 DB3 and DB2 (I^2C-bus interface) 20
7.1.20 $\overline{OSC}$: oscillator 20
7.1.21 $\overline{RES}$: reset 20
7.2 Block diagram functions 20
7.2.1 Address counter 20
7.2.2 Display data RAM 20
7.2.3 Timing generator 20
7.2.4 Display address counter 20
7.2.5 Display status 21
7.2.6 LCD row and column drivers 21
8 Addressing 22
8.1 Display data RAM structure 23
8.1.1 Basic command set 23
8.1.2 Extended command set 23
8.1.2.1 Horizontal/vertical addressing 23
8.1.2.2 Data order 25
8.1.2.3 Features available in both command sets . . . 25
9 Parallel interface 28
9.1 6800 series parallel interface 28
10 Serial interfacing (SPI and serial interface) . 28
10.1 Serial peripheral interface lines 28
10.1.1 Write mode 28
10.1.2 Read mode (only extended command set) . . 30
10.2 Serial interface (3-line) 30
10.2.1 Write mode 31
10.2.2 Read mode (only extended command set) . . 32
11 I^2C-bus interface 33
11.1 Characteristics of the I^2C-bus 33
11.1.1 System configuration 33
11.1.2 Bit transfer 34
11.1.3 START and STOP conditions 34
11.1.4 Acknowledge 35
11.2 I^2C-bus protocol 35
11.3 I^2C-bus Hs-mode protocol 37
11.4 Command decoder 40
12 Instructions 40
12.1 Instruction set commands 44
12.1.1 Common instructions of the basic and extended command set 44
12.1.2 Specific commands of the basic command set 45
12.1.3 Specific commands of the extended command set 45
12.2 Initialization 47
12.3 Reset function 47
12.3.1 Basic command set 47
12.3.2 Extended command set 47
12.4 Power-save mode 48
12.5 Display control 48
12.5.1 Bit MX 48
12.5.2 Bit MY 49
12.6 Set Y address of RAM 49
12.7 Set X address of RAM 49
12.8 Set display start line 49
12.9 Bias levels 51
12.10 Set V_{OP} value 53
12.10.1 Basic command set 54
12.10.2 Extended command set 59
12.11 Temperature control 60

continued >>

13 Internal circuitry 61
14 Safety notes 62
15 Limiting values 63
16 Static characteristics 64
17 Dynamic characteristics 66
17.1 Parallel interface timing characteristics 66
17.2 Serial interface timing characteristics 68
17.3 I^2C-bus interface timing characteristics 71
18 Application information 74
19 Support information 75
19.1 Module maker programming 75
19.1.1 V_{LCD} calibration 75
19.1.2 Temperature coefficient selection 76
19.1.3 Seal bit 77
19.1.4 OTP architecture 77
19.1.5 Interface commands 78
19.1.5.1 CALMM 78
19.1.5.2 Refresh 79
19.1.6 Example sequence for filling the shift register 79
19.1.7 Programming flow 80
19.1.8 Programming specification 81
20 Package outline 82
21 Handling information 82
22 Packing information 83
23 Appendix 85
23.1 LCD graphic driver selection 85
24 Abbreviations 86
25 References 87
26 Revision history 88
27 Legal information 89
27.1 Data sheet status 89
27.2 Definitions 89
27.3 Disclaimers 89
27.4 Trademarks 90
28 Contact information 90
29 Tables 91
30 Figures 92
31 Contents 93

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