

PESD5V0U2BMB

Ultra low capacitance bidirectional double ESD protection array

5 December 2018

Product data sheet

1. General description

Ultra low capacitance bidirectional double ElectroStatic Discharge (ESD) protection array designed to protect up to two signal lines from the damage caused by ESD and other transients. The device is housed in a leadless ultra small SOT883B (DFN1006B-3) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- · ESD protection of up to two lines
- Ultra low diode capacitance: C_d = 2.9 pF
- Ultra low leakage current: I_{RM} = 5 nA
- AEC-Q101 qualified
- ESD protection up to 10 kV
- IEC 61000-4-2; level 4 (ESD)

3. Applications

- Computers and peripherals
- · Audio and video equipment
- · Cellular handsets and accessories
- · Communication systems
- · Portable electronics
- · SIM card protection
- · High-speed data lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C	-	-	5	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	-	2.9	3.5	pF



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	1	к1
2	K2	cathode (diode 2)] 3	K2 K1 N CC
3	CC	common cathode	Transparent top view DFN1006B-3	006aab331
			(SOT883B)	

6. Ordering information

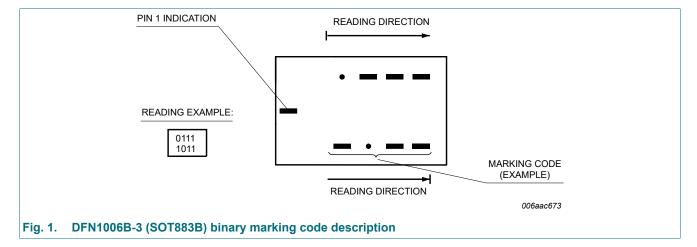
Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PESD5V0U2BMB		plastic, leadless ultra small plastic package; 3 solder lands; 0.35 mm pitch; 1.0 mm x 0.6 mm x 0.37 mm body	SOT883B		

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0U2BMB	0001 1010



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1] [2]	-	1.5	А
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximu	ım ratings		<u>'</u>	•		
V _{ESD}	electrostatic discharge	IEC 61000-4-2 (contact discharge)	[3] [2]	-	10	kV
	voltage	MIL-STD-883 (human body model)		-	8	kV
		machine model	[2]	-	400	V

^[1] Device stressed with ten non-repetitive current pulses (8/20 μs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321).

- [2] Measured from pin 1 or 2 to pin 3.
- [3] Device stressed with ten non-repetitive ESD pulses.

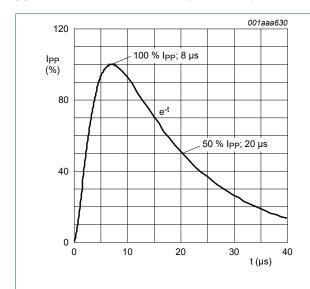


Fig. 2. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

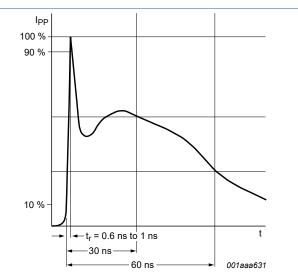


Fig. 3. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	5	V
V_{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C		5.5	6.5	9.5	V
I _{RM}	reverse leakage current	V _{RWM} = 5 V; T _{amb} = 25 °C		-	5	100	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	2.9	3.5	pF
		f = 1 MHz; V _R = 5 V; T _{amb} = 25 °C		-	1.9	-	pF
V _{CL}	clamping voltage	I _{PP} = 1 A; T _{amb} = 25 °C	[1] [2]	-	-	10	V
		I _{PPM} = 1.5 A; T _{amb} = 25 °C	[1] [2]	-	-	12	V
R _{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[3]	-	0.6	-	Ω

- [1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.
- [2] Measured from pin 1 or 2 to pin 3.
- [3] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

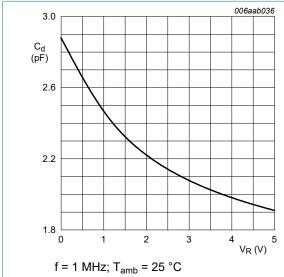
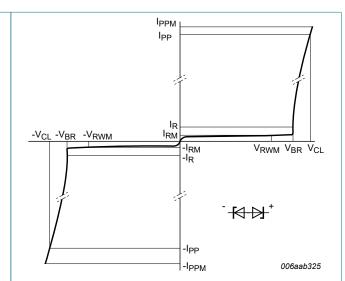
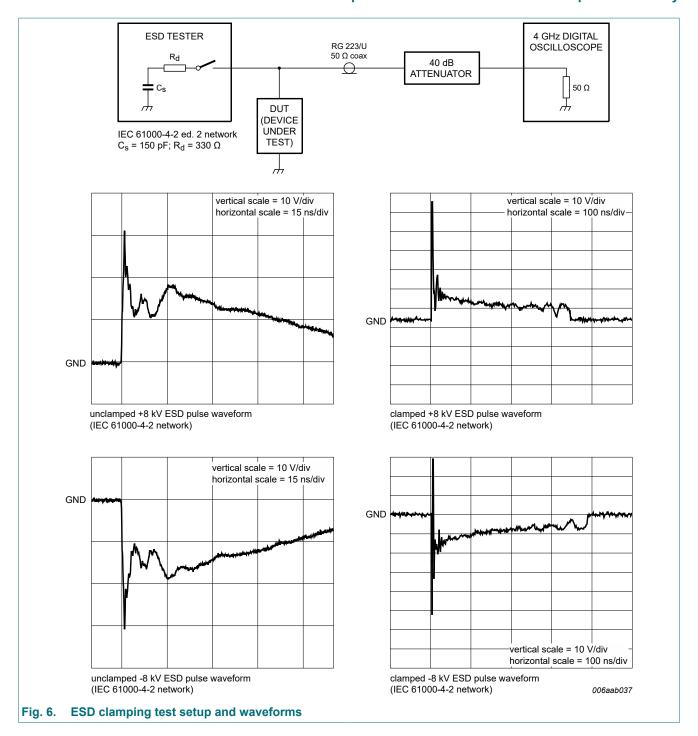


Fig. 4. Diode capacitance as a function of reverse voltage; typical values

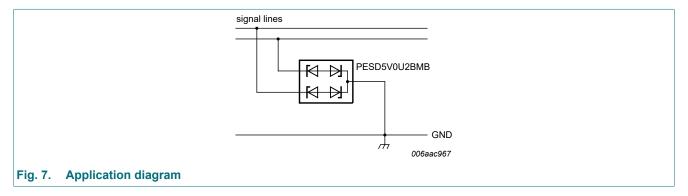


ig. 5. V-I characteristics for a bidirectional ESD protection diode



10. Application information

The device is designed for protection of up to two bidirectional data or signal lines from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative, with respect to ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

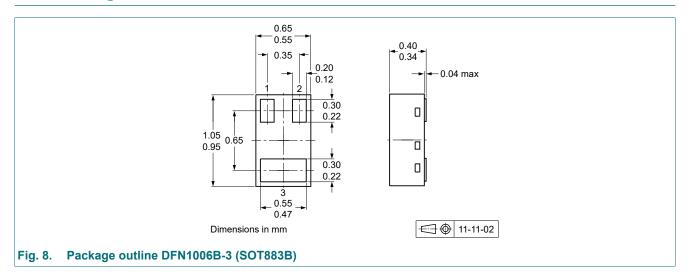
- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

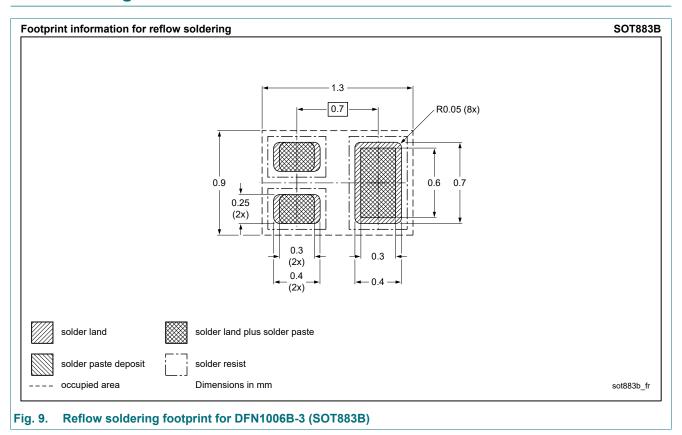
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



13. Soldering



14. Revision history

Table 7. Revision history

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Data sheet ID	Release date	Data sheet status	Change notice	Supersedes		
PESD5V0U2BMB v.2	20181205	Product data sheet	-	PESD5V0U2BMB v.1		
Modifications:	•	Legal texts have been adapted to the new company name where appropriate. The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.				
PESD5V0U2BMB v.1	20120313	Product data sheet	-	-		

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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