



PMK50XP

P-channel TrenchMOS extremely low level FET

Rev. 02 — 28 April 2010

Product data sheet

1. Product profile

1.1 General description

Extremely low level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance

1.3 Applications

- Battery management
- Load switching

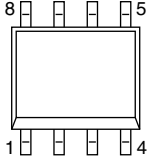
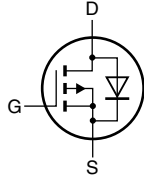
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	-20	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = -4.5\text{ V}$; see Figure 1 ; see Figure 3	-	-	-7.9	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 2	-	-	5	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$; $I_D = -2.8\text{ A}$; $T_j = 25\text{ °C}$; see Figure 9 ; see Figure 10	-	40	50	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = -4.5\text{ V}$; $I_D = -4.7\text{ A}$; $V_{DS} = -10\text{ V}$; see Figure 11 ; see Figure 12	-	1.3	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT96-1 (SO8)</p>	 <p>003aaa671</p>
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

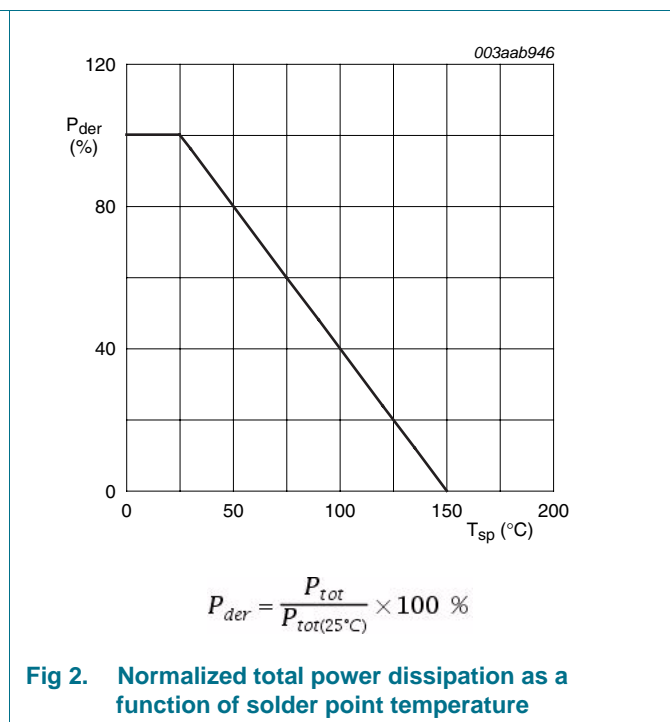
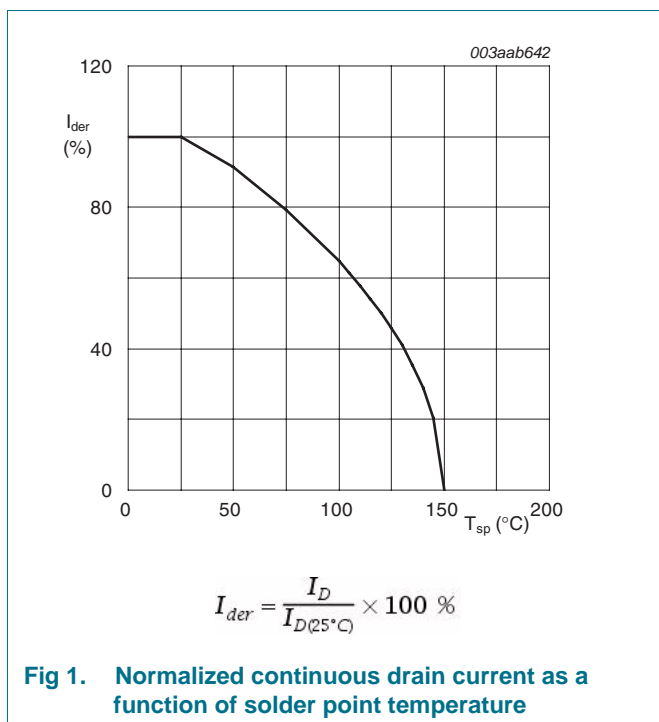
Type number	Package		Version
	Name	Description	
PMK50XP	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

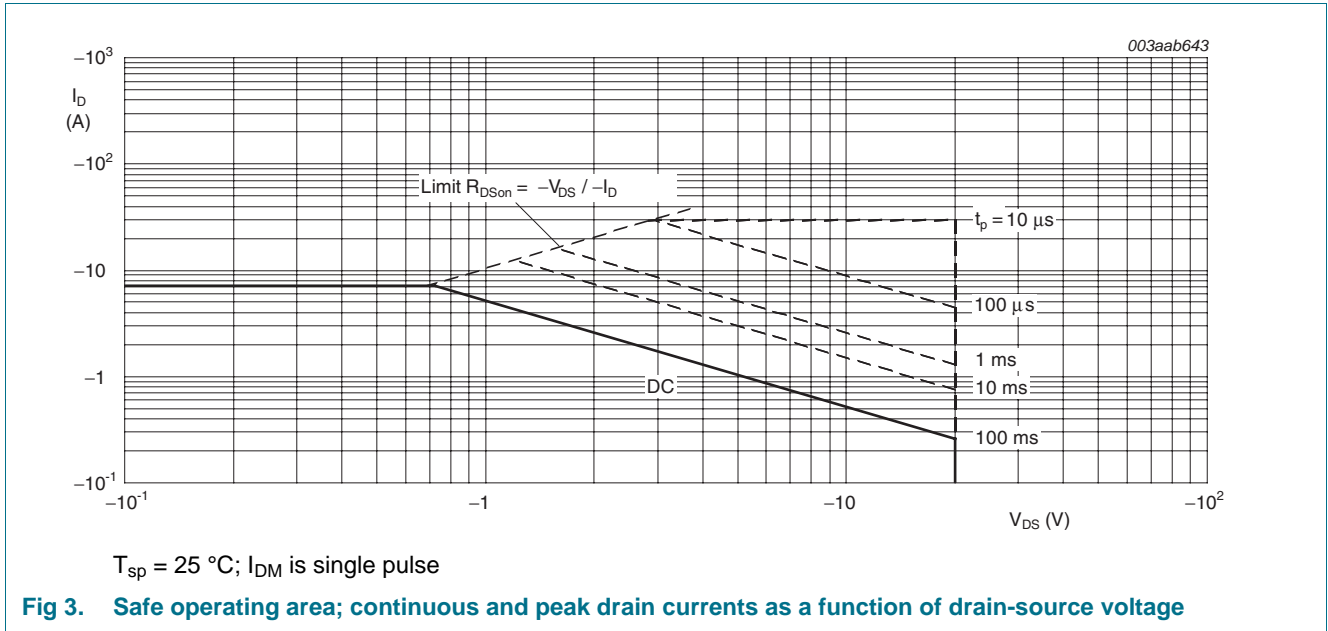
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C	-	-	-20	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 150 °C; R _{GS} = 20 kΩ	-	-	-20	V
V _{GS}	gate-source voltage		-12	-	12	V
I _D	drain current	T _{sp} = 25 °C; V _{GS} = -4.5 V; see Figure 1 ; see Figure 3	-	-	-7.9	A
		T _{sp} = 100 °C; V _{GS} = -4.5 V; see Figure 1	-	-	-5	A
I _{DM}	peak drain current	T _{sp} = 25 °C; t _p ≤ 10 μs; pulsed; see Figure 3	-	-	-31.6	A
P _{tot}	total power dissipation	T _{sp} = 25 °C; see Figure 2	-	-	5	W
T _{stg}	storage temperature		-55	-	150	°C
T _j	junction temperature		-55	-	150	°C
Source-drain diode						
I _S	source current	T _{sp} = 25 °C	-	-	-4.1	A
I _{SM}	peak source current	T _{sp} = 25 °C; t _p ≤ 10 μs; pulsed	-	-	-16.4	A

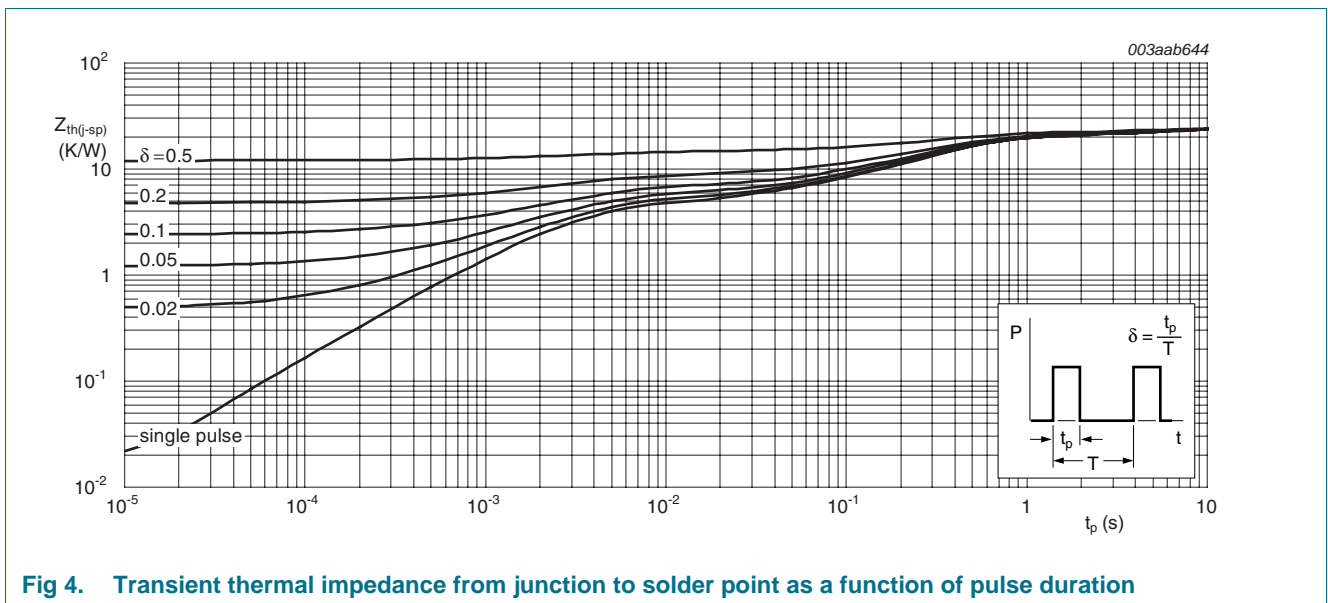




5. Thermal characteristics

Table 5. Thermal characteristics

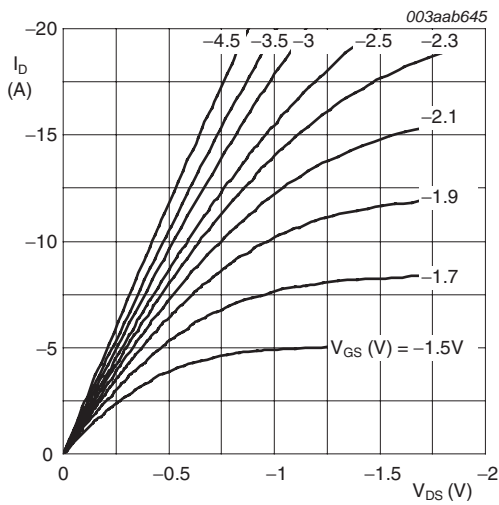
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	25	K/W



6. Characteristics

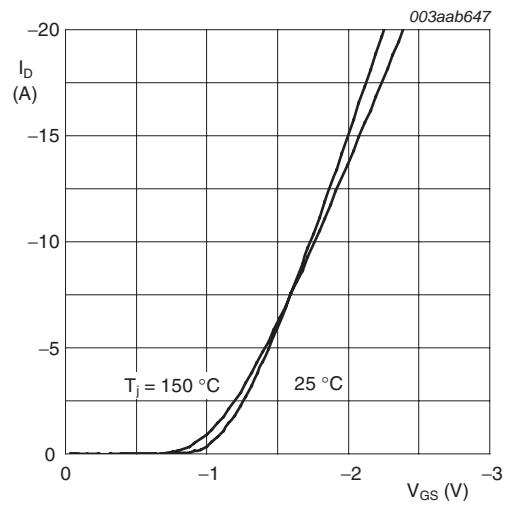
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ\text{C}$	-18	-	-	V
		$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	-	-	-1.1	V
		$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	-0.35	-	-	V
		$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 7 ; see Figure 8	-0.55	-0.75	-0.95	V
I_{DSS}	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 70 \text{ }^\circ\text{C}$	-	-	-5	μA
I_{GSS}	gate leakage current	$V_{GS} = 12 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	-	-10	-100	nA
		$V_{GS} = -12 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	-	-10	-100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -2.5 V; I_D = -2.3 A; T_j = 25 \text{ }^\circ\text{C};$ see Figure 9 ; see Figure 10	-	56	70	m Ω
		$V_{GS} = -4.5 V; I_D = -2.8 A; T_j = 150 \text{ }^\circ\text{C};$ see Figure 9 ; see Figure 10	-	64	80	m Ω
		$V_{GS} = -4.5 V; I_D = -2.8 A; T_j = 25 \text{ }^\circ\text{C};$ see Figure 9 ; see Figure 10	-	40	50	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = -4.7 A; V_{DS} = -10 V; V_{GS} = -4.5 V;$ see Figure 11 ; see Figure 12	-	10	-	nC
Q_{GS}	gate-source charge		-	2.2	-	nC
Q_{GD}	gate-drain charge		-	1.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = -4.7 A; V_{DS} = -10 V;$ see Figure 11 ; see Figure 12	-	-1.6	-	V
C_{iss}	input capacitance	$V_{DS} = -20 V; V_{GS} = 0 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	1020	-	pF
C_{oss}	output capacitance		-	140	-	pF
C_{rss}	reverse transfer capacitance		-	100	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 V; R_L = 10 \Omega; V_{GS} = -4.5 V;$ $R_{G(ext)} = 6 \Omega$	-	8.5	-	ns
t_r	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
t_f	fall time		-	35	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -1.7 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ\text{C};$ see Figure 14	-	-0.77	-1.2	V



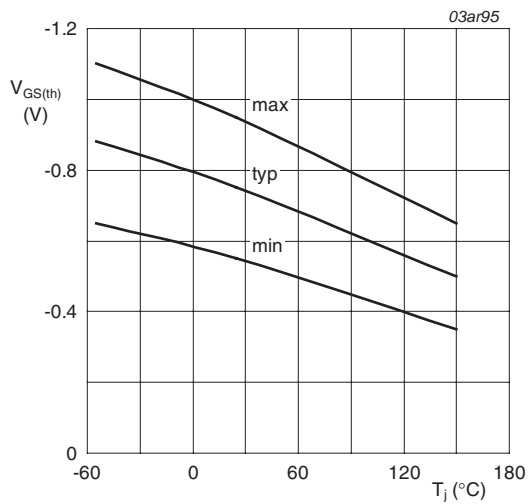
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



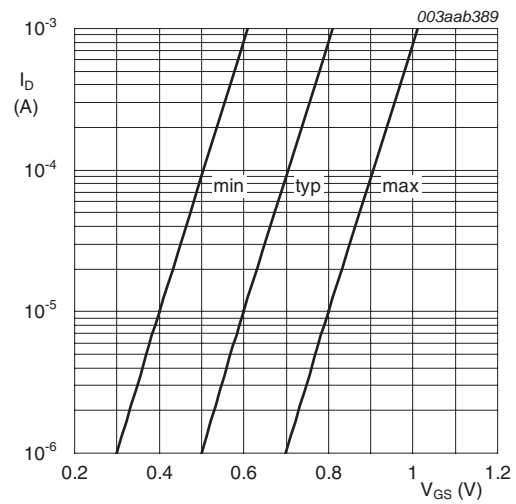
$V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



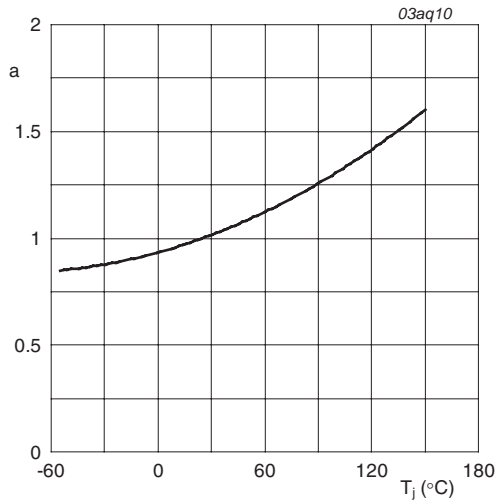
$I_D = -0.25\text{ mA}; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



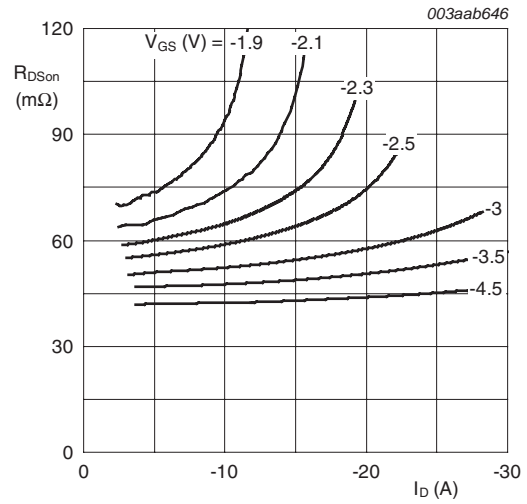
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = -5\text{ V}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



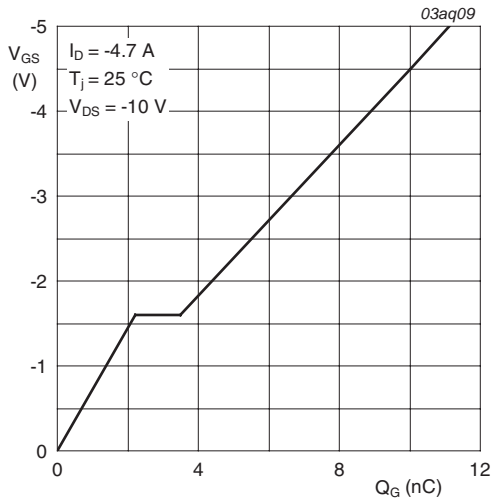
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



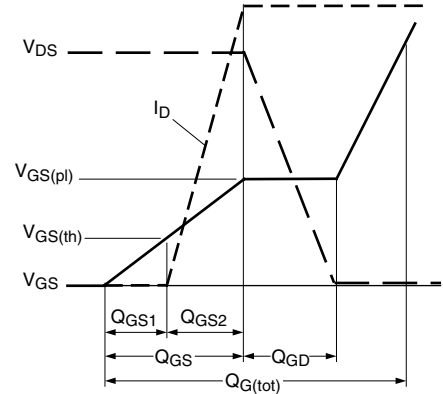
$T_j = 25^\circ C$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values



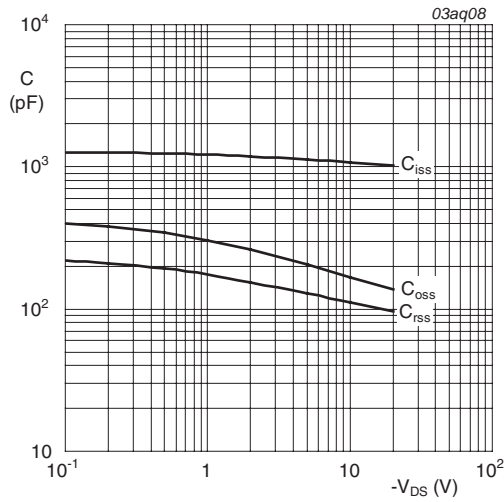
$I_D = -4.7 A; T_j = 25^\circ C; V_{DS} = -10 V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



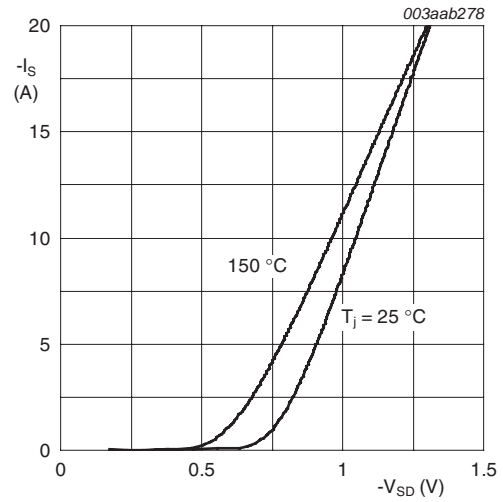
003aaa508

Fig 12. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig 14. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

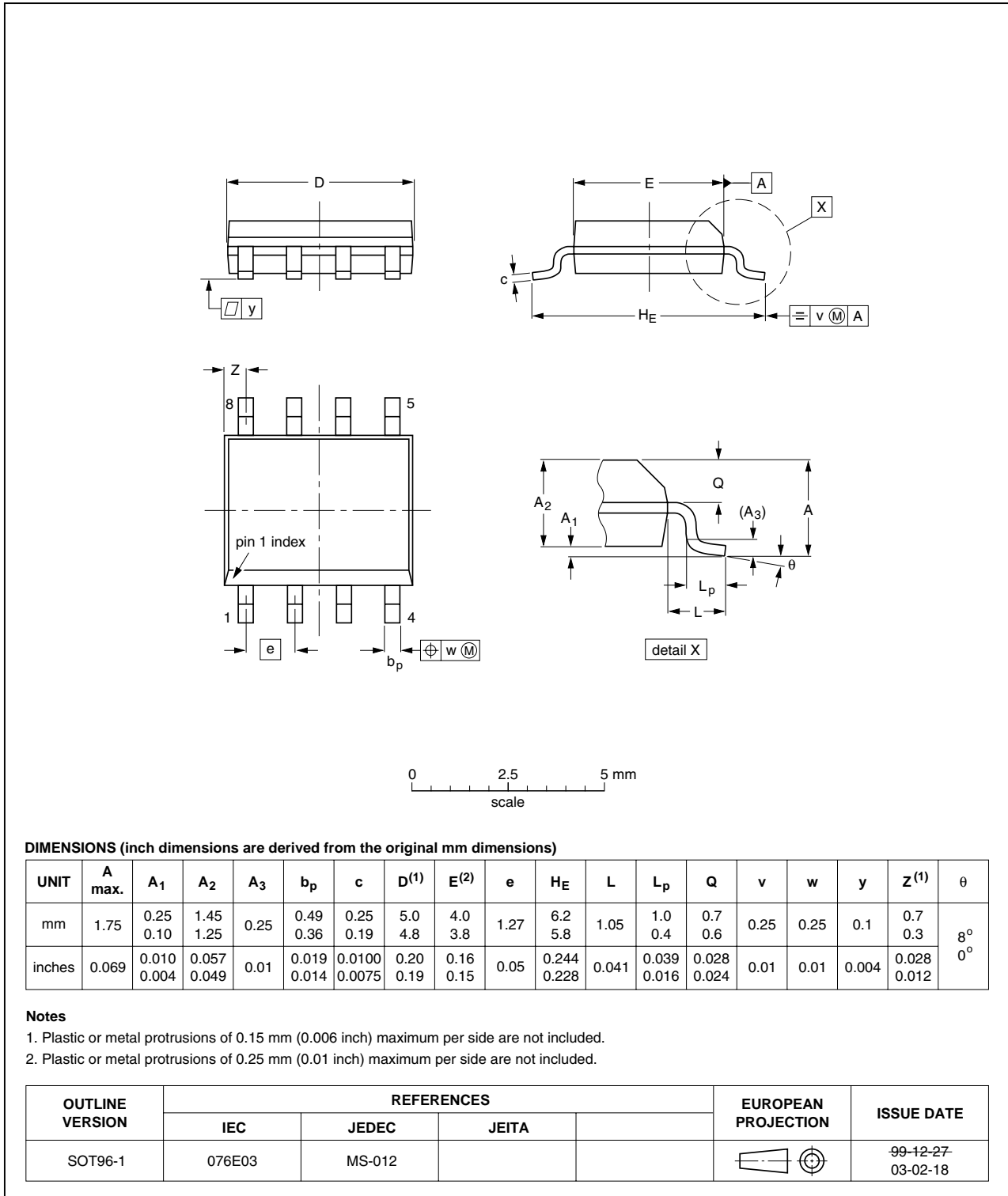


Fig 15. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMK50XP_2	20100428	Product data sheet	-	PMK50XP_1
Modifications:	• Various changes to content.			
PMK50XP_1	20070917	Product data sheet	-	-

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9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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