PTN38003A

Multi-protocol USB3.2 and DisplayPort linear redriver

Rev. 2.1 — 8 December 2021 Product data sheet

1 General description

PTN38003A is a high-performance USB3.2/DisplayPort multi-protocol linear redriver that is optimized for USB3.2 and DisplayPort applications on either the downstream facing port (DFP) or upstream facing port (UFP) application.

PTN38003A addresses high-speed signal quality enhancement requirements for implementation of USB Type-C interface in a platform that supports the USB Type-C, VESA DisplayPort Alternate Mode standards. This device also implements the snooping monitor of the sideband signals from DP mode (AUX) to optimize the configuration, power saving mode and performance.

The device provides programmable linear equalization, output swing linearity control by pin strapping or I^2C control to improve signal integrity and enable channel extension by reducing inter-symbol interference (ISI). DisplayPort AUX snooping is performed to follow relevant DisplayPort source-sink AUX transactions and configure the redriver to meet link requirements.

For USB operation, PTN38003A has built-in advanced power management capability that enables significant power saving under USB3.2 low power modes (U2/U3). It detects LFPS (Low Frequency Periodic Signaling)/LBPM (LFPS Based PWM Message) signaling to configure the operation (USB3.2 Gen 1/Gen 2 & x1/x2) and link electrical conditions and it activates/deactivates internal circuitry and logic dynamically. The device performs these actions without host software intervention and conserves power. The host processor keeps PTN38003A in deep power saving or USB mode until Alternate Mode has been entered.

The device is tailored to support USB3.2 electrical idle, receiver detection and power saving modes. It maintains two separate input signal detectors – loss of high-speed signal (LOS) and USB LFPS detectors with built-in hysteresis.

For DisplayPort (DP) operation, PTN38003A monitors the AUX transactions and adjusts the DisplayPort channel setting during DP Link initialization and training.

PTN38003A is powered from a 1.8 V supply. It is available in a small high performance HWFLGA36 package.

2 Features and benefits

- Flexible multi-protocol linear redriver supports three signaling combinations specified in USB Type-C and VESA specifications
  - Mode 0: Deep Power saving
  - Mode 1: USB3.2 Gen1x1/Gen1x2/Gen2x1/Gen2x2
  - Mode 2: USB3.2 + DP 2-Lane + AUX snooping
  - Mode 3: DP 4-Lane + AUX snooping
- Supports USB 3.2 Gen1x1, Gen 1x2, Gen2x1, Gen2x2 (5 Gbps and 10 Gbps)
  - I^2C register based Flat gain control
  - Peaking gain of +12.1 dB at 5 GHz
  - Output linearity control: 500 mVppd to 950 mVppd
- Support DP2.0 link rates at 1.62 Gbps (RBR), 2.7 Gbps (HBR), 5.4 Gbps (HBR2), 8.1 Gbps (HBR3),10 Gbps (UHBR10), 13.5 Gbps (UHBR13.5), 20 Gbps (UHBR20)
  - DP AUX monitoring during DP link training to control DP channel
  - I^2C register based Flat gain control
  - Peaking gain of 10.2 dB at 4.05 GHz, 20 dB at 10 GHz
  - Output linearity control: 500 mVppd to 950 mVppd
- Compliant to DisplayPort, USB3.2 standard and USB Type-C Alternate Mode interoperability testing
  - Implements USB Type-C Safe state conditions on all connector facing pins
- Configurable via I^2C interface with a configurable address pin
- Integrated termination resistors provide impedance matching on both transmit and receive sides
- Supports maximum voltage limit ($V_{voltage\_jump}$) to align to the latest USB3 specification and computing platform capabilities
- Autonomous Orientation detection of USB Type-C device connection
- RX equalizers on all high-speed inputs to compensate for signal attenuation
- Automatic receiver termination detection in USB mode
- Good linearity over the frequency band (50 MHz to 10.3 GHz) and voltage dynamic range
- Excellent Differential return loss performance: < -16 dB up to 10.3 GHz
- Flow-through pin-out to ease PCB layout and minimize crosstalk effects
  - Very low crosstalk: DDNEXT < -50 dB up to 10.3 GHz
- Low active current consumption for output swing linearity control of 950 mVppd
  - USB3.2 Gen2x2 or Gen1x2 (Mode 1) active power: 250 mA (typ)
  - USB3.2 Gen2x1 or Gen1x1 (Mode 1) active power: 125 mA (typ)
  - 1-lane DP HBR3/UHBR10/UHBR13.5/UHBR20 (Mode 2 or 3): 62 mA (typ)
  - 2-lane DP HBR3/UHBR10/UHBR13.5/UHBR20 (Mode 2 or 3): 125 mA (typ)
  - 4-lane DP only HBR3/UHBR10/UHBR13.5/UHBR20 (Mode 3): 250 mA (typ)
- Power–saving states:
  - USB3.2 (Mode 1)
    - 0.22 mA (typ) when 2 lanes are enabled in USB3 U2/U3 states
    - 0.11 mA (typ) when 1 lane is enabled in USB3 U2/U3 states
    - 0.11 mA (typ) only Rx detection is enabled on 1 lane when no connection detected (USB Rx detection enabled)
  - DisplayPort sleep D3 mode (Mode 3): 3.2 mA (typ)
  - 10 µA (typ) when in deep power saving state

- Hot Plug capable:
  - Support Type-C plug connection through PD controller
- Power Supply 1.7 V to 1.9 V
- Small high performance HWFLGA36 package
- ESD HBM 1.5 kV, CDM 1 kV
- Operating temperature range -20 °C to +85 °C

3 Applications

- For USB Type-C host/source application
  - Smartphones and tablets
  - Notebooks, AIO and desktop computers
  - Hub or dock devices
- For USB Type-C device/sink application
  - Docking stations
  - Display units

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PTN38003AEW	3A	HWFLGA36	plastic thermal enhanced very very thin fine-pitch land grid array package	SOT1948-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN38003AEW	PTN38003AEWY	HWFLGA36	reel dry pack, SMD, 13" Q1	7000	T_{amb} = -20 °C to 85 °C

5 Block diagram

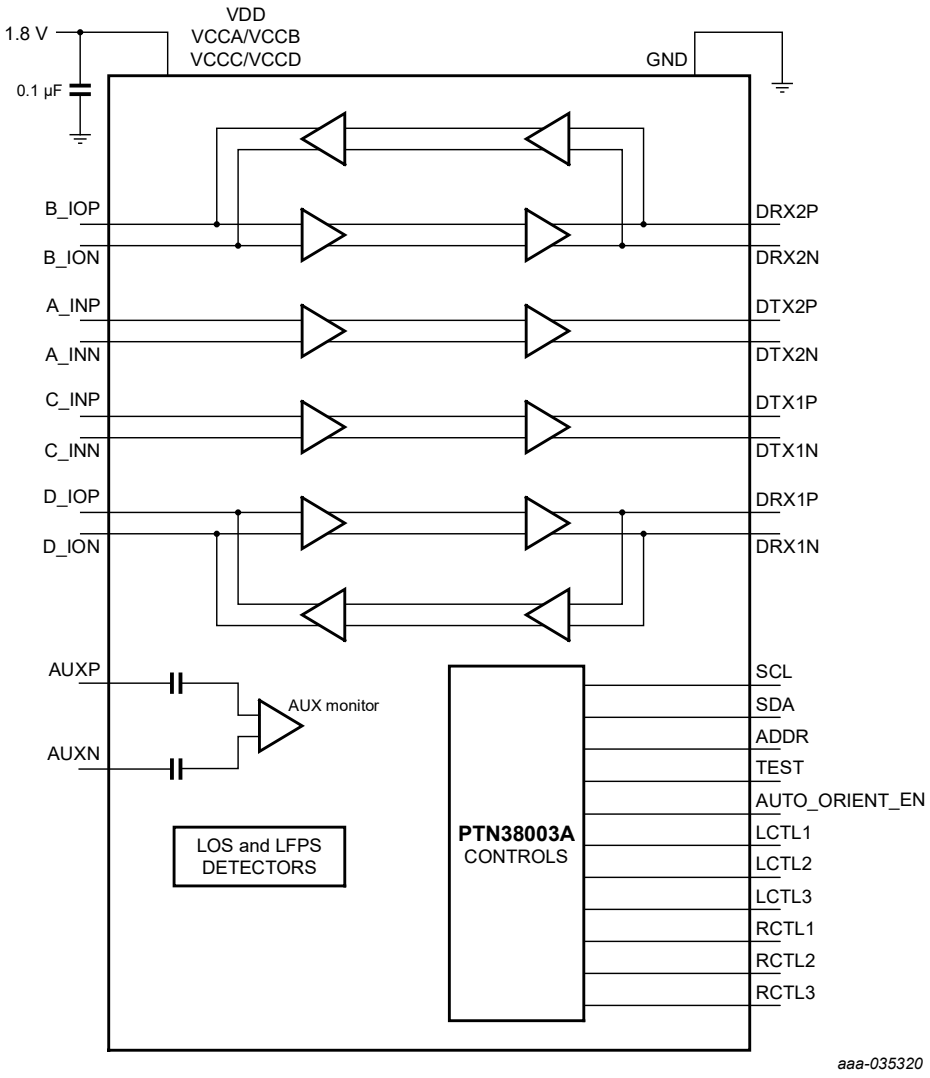


Figure 1. Block diagram

6 Pinning information

6.1 Pinning

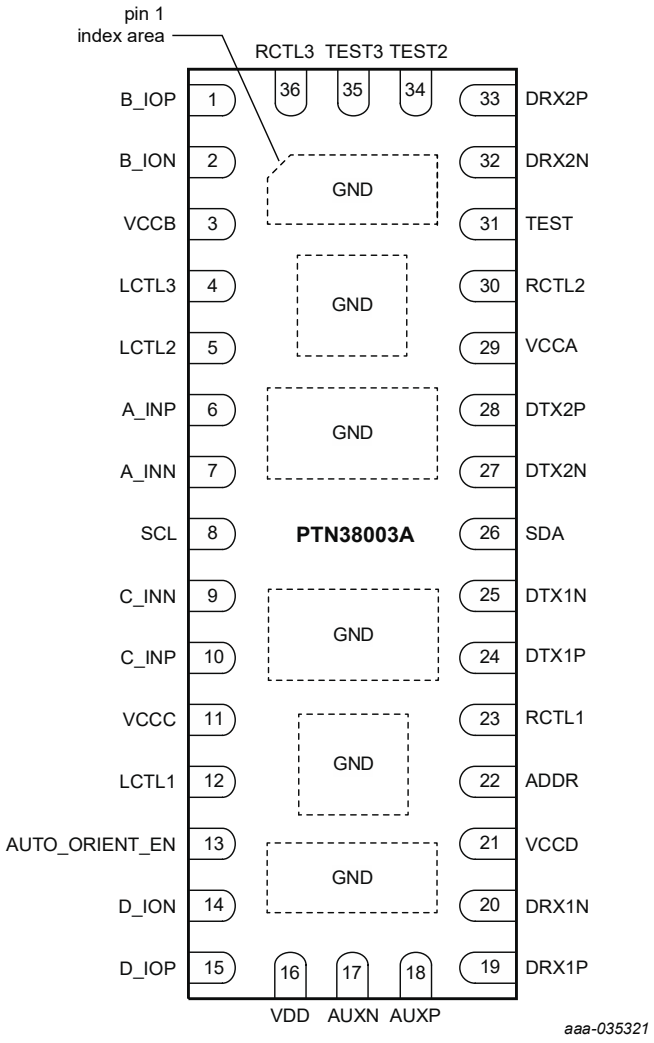


Figure 2. PTN38003A pinning (transparent top view)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
1	B_IOP	Self-biasing differential input/output	Differential signal high-speed input/output. B_IOP makes a differential pair with B_ION. The associated output/input pair is DRX2P and DRX2N. The I/O configuration is controlled by mode setting
2	B_ION		

Table 3. Pin description...*continued*

Symbol	Pin	Type	Description
3	VCCB	Power pins for high-speed paths	These dedicated power pins for high-speed differential pairs provide good signal integrity and isolation
11	VCCC		
21	VCCD		
29	VCCA		
4	LCTL3	Ternary Input	Ternary Input for controlling Output Swing Linearity on the downstream side of the redriver. Please refer to Table 10 for details
12	LCTL1	Ternary input	LCTL1 and LCTL2 are EQ Peaking Gain setting pins for inputs on upstream side of the redriver. Please refer to Table 8 for details
5	LCTL2		
6	A_INP	Self-biasing differential input	Differential signal from high-speed RX path. A_INP makes a differential pair with A_INN. The associated TX output pair is DTX2P and DTX2N
7	A_INN		
8	SCL	Open Drain input	When operating in I^2C mode, this pin is slave I^2C clock pin, and external pull-up resistor to I^2C supply (1.8 V or 3.3 V) is required
9	C_INN	Self-biasing differential input	Differential signal from high-speed RX path. C_INP makes a differential pair with C_INN. The associated TX output pair is DTX1P and DTX1N
10	C_INP		
13	AUTO_ ORIENT_EN	Binary input	Input for Auto Orientation Detection Enable: • If the pin input is HIGH, Autonomous orientation detection of USB-C connection is enabled • If this pin is LOW, Autonomous orientation detection of USB-C connection is disabled The pin can be either strapped in the application or connected to host processor. The pin is sampled at POR for initiating orientation detection process. This pin has a weak internal pulldown resistor (2 MΩ typ) to GND.
14	D_ION	Self-biasing differential input/output	Differential signal high-speed input/output. D_IOP makes a differential pair with D_ION. The associated output/ input pair is DRX1P and DRX1N. The I/O configuration is controlled by mode setting
15	D_IOP		
16	VDD	Power	1.8 V Supply for I^2C, AUX snooping and digital blocks
17	AUXN	Input	DP AUX channel snooping input
18	AUXP		
19	DRX1P	Self-biasing differential input/output	Differential signal high-speed input/output. DRX1P makes a differential pair with DRX1N. The associated output/ input pair is D_IOP and D_ION. The I/O configuration is controlled by mode setting
20	DRX1N		
22	ADDR	Quaternary Input	I^2C slave address selection pin in I^2C mode
23	RCTL1	Ternary input	RCTL1 and RCTL2 are EQ Peaking Gain setting pins for inputs on downstream side of the redriver. Please refer to Table 8 for details
30	RCTL2		

Table 3. Pin description...*continued*

Symbol	Pin	Type	Description
24	DTX1P	Self-biasing differential output	Differential signal of high-speed TX path. DTX1P makes a differential pair with DTX1N. The associated RX input pair is C_INP and C_INN
25	DTX1N		
26	SDA	Binary open drain input/ output	When PTN38003A is operating in I^2C mode, this pin is slave I^2C Data pin, and external pull-up resistor to I^2C supply (1.8 V or 3.3 V) is required
27	DTX2N	Self-biasing differential output	Differential signal of high-speed TX path. DTX2P makes a differential pair with DTX2N. The associated RX input pair is A_INP and A_INN
28	DTX2P		
31	TEST	Reserved Test pin	Reserved for test purpose only. Must be connected to GND in the system application
32	DRX2N	Self-biasing differential input/output	Differential signal high-speed input/output. DRX2P makes a differential pair with DRX2N. The associated output/ input pair is B_IOP and B_ION. The I/O configuration is controlled by mode setting
33	DRX2P		
34	TEST2	Reserved	These pins are left open/unconnected
35	TEST3		
36	RCTL3	Ternary input	Ternary input for controlling Output Swing Linearity on the upstream side of the redriver. Please refer to Table 10 for details
Center pads	GND		These 6 center pads must be connected to GND plane for both electrical grounding and thermal relief

7 Functional description

7.1 USB3.2 operation

PTN38003A supports USB3.2 Redriver operation at Gen1 (5 Gbps) and Gen2 (10 Gbps) data rates. The receive equalization – peaking gain and output linearity control are configured either via I^2C register settings or pin strapping.

PTN38003A has implemented an advanced power management scheme that operates in tune with USB Bus electrical condition. Though the device does not decode USB power management commands (related to USB3 U1/U2/U3 transitions) exchanged between USB Host and Peripheral/Device, it relies on bus electrical conditions and control pins/ register settings to decide to be in one of the following states:

- Active state wherein device is fully operational. In this state, USB connection exists and the Receive Termination remains active.
- Power-saving state wherein some portions of the TX and RX channels are kept enabled. In this state, LOS detector, LFPS/LBPM detection and/or Receive termination detection circuitry are active. Based on USB connection, there are two possibilities,
  - No USB connection (also called Rx-detect state)
    - Receive Termination detection circuitry keeps polling periodically
    - RX and TX signal paths (including LOS detector) are not enabled
    - Receive Termination is not active
  - When USB connection exists and when the link is in USB U2/U3 mode,
    - Receive Termination detection circuitry keeps polling periodically
    - RX and TX signal paths are not enabled; LOS detector is disabled, and LFPS detector is enabled.
    - Receive Termination is active

7.2 DisplayPort operation

PTN38003A supports DisplayPort v1.4/2.0 operation seamlessly at 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, 8.1 Gbps, 10 Gbps, 13.5 Gbps, and 20 Gbps with receiver equalization and linearity control.

The DisplayPort mode is selected only when DP alternate mode has been entered by the host controller. The DisplayPort source can activate power down via AUX command. DP spec supports two modes – D0/active or D3/Low power mode. In D0 mode, the linear redriver data path is active depending on the state of the DP link. In D3 mode, the AUX snooping logic is active while high-speed path is disabled resulting in lower current consumption.

The DisplayPort lane count is configured during DisplayPort link training phase based on AUX communication exchanges between source and sink.

PTN38003A performs equalization control for DP signals, and can be configured by LCTL[3:1] and RCTL[3:1] settings through either I^2C or pin strapping.

PTN38003A uses lane count information for configuring the transmitters and receivers. It is possible that only a subset of lanes gets selected during DP Link training and remaining lanes are not active. Depending on the number of lanes selected, PTN38003A is configured to operate with the selected lane count thereby saving power consumption on unused lanes.

7.2.1 AUX monitoring and configuration

PTN38003A monitors DP AUX communication exchanges that occur between DP source and DP sink. It detects AUX communication involving DPCD register controls – Lane count, sleep, wake and configures its operation suitably. AUX monitor function is enabled when operating mode is set to Mode 2 (USB+DP 2-Lane) or 3 (DP 4-Lane), and is disabled in other mode settings.

The list of DPCD registers (with only the relevant bit fields) supported are as follows:

- LANE_COUNT_SET
- SET POWER
- Other DPCD registers and I^2C over AUX transactions are not decoded

Input receive equalization is determined by LCTL[2:1] pins, and output linearity is controlled by LCTL3.

All lanes of DP redriver can be configured separately on a per lane basis using I^2C. When the Lane-Count is set via AUX, then the legal values are 1,2,4. If AUX tries to set it to 0, PTN38003A ignores it, and continues with the last known legal value. When the Lane-Count is set via I^2C, then the legal values are 0,1,2,4. If I^2C sets it to 0, PTN38003A disables all the lanes.

- Operational Mode = 0/1, DP Lane count = 0
- Operational Mode = 2, DP Lane count = 1 or 2
- Operational Mode = 3, DP lane count = 1, 2 or 4

7.3 Signal detectors

PTN38003A implements two types of signal detectors:

- LFPS detector: This is used in detect LFPS signaling on high speed data path. This is implemented only on lanes wherein USB data flows.
- Loss of (High-speed) Signal detector (LOS detector): This is meant for detecting both presence and absence of high-speed signal at the input pins over all protocols - USB and DP. The LOS detection is used to enter and exit from low power states.

Based on LOS detector output, PTN38003A turns off certain portions of the internal circuitry and optimizes current consumption under various modes: USB (U2/U3), DP (D3 mode), and especially under electrical idle conditions.

7.4 Linear redriver controls

PTN38003A allows for programming of linear redriver functions – equalizer and linearity on a per channel basis. Since the USB3.2 and DisplayPort input channels support different maximum data rates, the corresponding input equalization on those paths need to be tuned accordingly.

Each linear redriver channel path has individual control of

- Flat gain can be controlled via I^2C register for all the high speed data paths
- Peaking gain referenced to the maximum data rate (or Nyquist channel) in that channel
- Output Linear Swing is set up based on selected input source signal amplitude and pre-emphasis and considering channel attenuation

7.5 USB Type-C DFP receptacle application

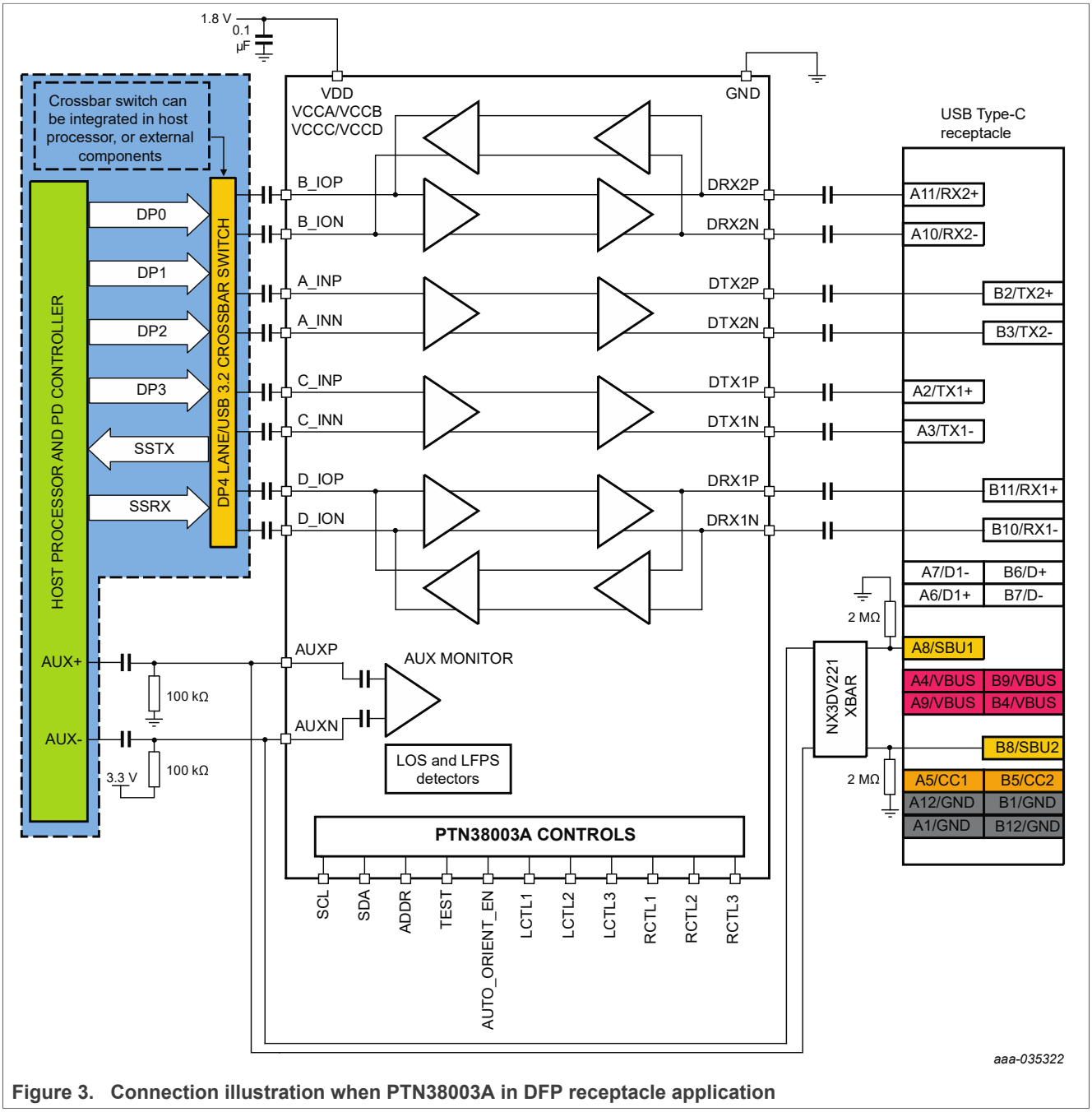


Figure 3. Connection illustration when PTN38003A in DFP receptacle application

Refer to Figure 3 for using PTN38003A in USB Type-C DFP receptacle application. In this configuration, upstream side of PTN38003A is connected to host processor and downstream side is connected to Type-C receptacle.

Each pin on the downstream side of PTN38003A connecting to the Type-C connector has specific input/output configuration, and must match the signal assignments on the upstream side accordingly. Table 4 shows the downstream pin connection facing the Type-C receptacle.

Table 4. Downstream pin connection to Type-C receptacle in DFP application

PTN38003A pins		USB Type-C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
33	DRX2P	A11	RX2+
32	DRX2N	A10	RX2-
27	DTX2N	B3	TX2-
28	DTX2P	B2	TX2+
24	DTX1P	A2	TX1+
25	DTX1N	A3	TX1-
20	DRX1N	B10	RX1-
19	DRX1P	B11	RX1+
18	AUXP		Input of SBU XBAR
17	AUXN		Input of SBU XBAR

The upstream pins of PTN38003A are connected to the host processor, with specific functions assigned to each differential signal. For each pin assignment configuration below, PTN38003A controls which transmitters or receivers to turn on or turn off, and operating in USB3.2 or DP mode according to the mode setting.

Table 5. Upstream pin connection to host processor in DFP receptacle application

PTN38003A pins		Host processor signal names							
Symbol	**Pin name**	**USB3.2**		**USB3.2 Gen1/2 x1**		**USB3 + 2-Lane DP**		**4-Lane DP**	
		Normal	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**
14	D_ION	SSRX1-	SSRX2-	SSRX-		SSRX-	ML0-	ML3-	ML0-
15	D_IOP	SSRX1+	SSRX2+	SSRX+		SSRX+	ML0+	ML3+	ML0+
10	C_INP	SSTX1+	SSTX2+	SSTX+		SSTX+	ML1+	ML2-	ML1+
9	C_INN	SSTX1-	SSTX2-	SSTX-		SSTX-	ML1-	ML2+	ML1-
6	A_INP	SSTX2+	SSTX1+		SSTX+	ML1+	SSTX+	ML1+	ML2+
7	A_INN	SSTX2-	SSTX1-		SSTX-	ML1-	SSTX-	ML1-	ML2-
1	B_IOP	SSRX2+	SSRX1+		SSRX+	ML0+	SSRX+	ML0+	ML3+
2	B_ION	SSRX2-	SSRX1-		SSRX-	ML0-	SSRX-	ML0-	ML3-

7.6 USB Type-C UFP receptacle application

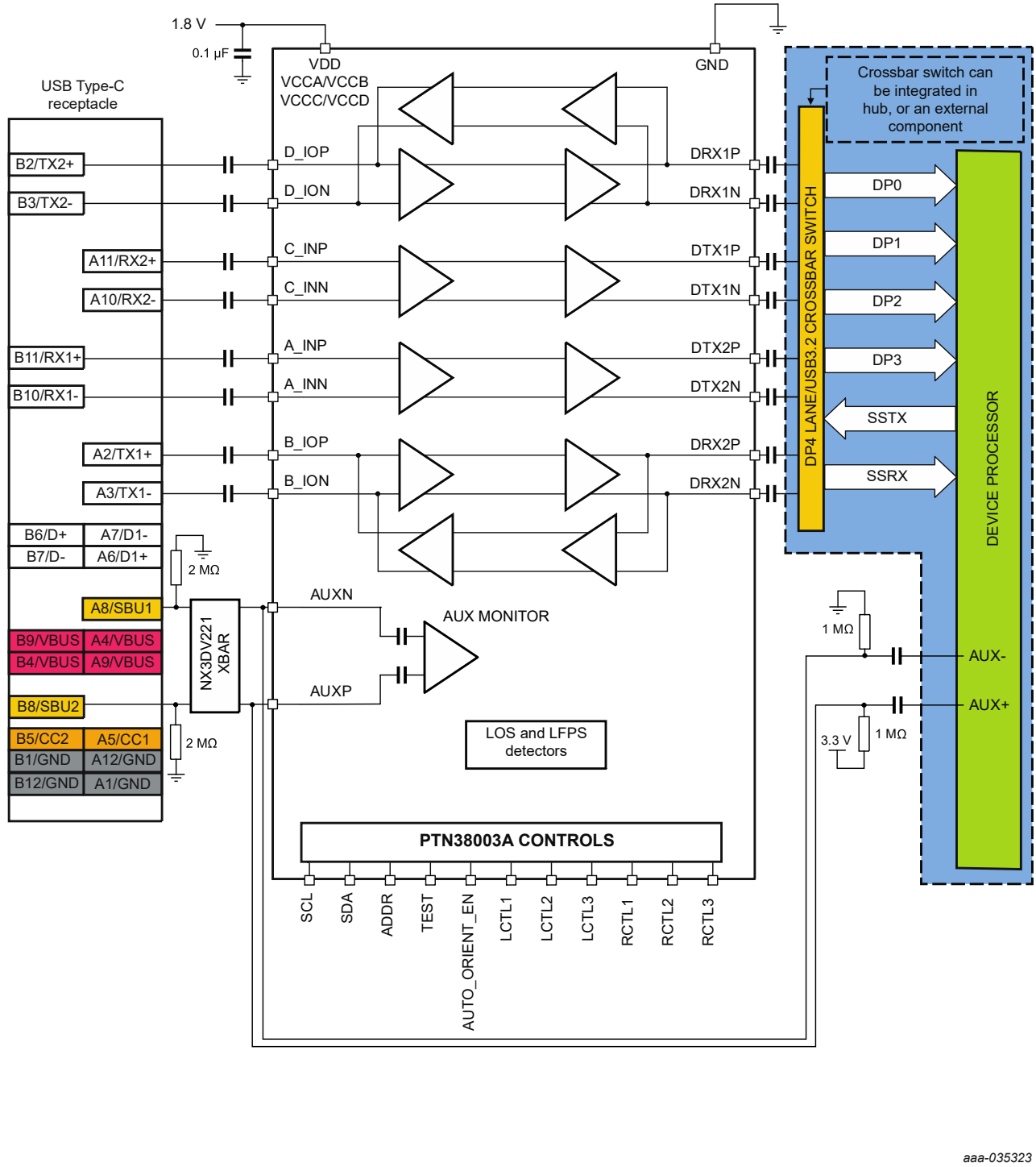


Figure 4. Connection illustration when PTN38003A in UFP receptacle application

Refer to Figure 4 for using PTN38003A in USB Type-C UFP receptacle application. In this configuration, downstream side of PTN38003A is connected to device processor while the upstream side is connected to Type-C receptacle.

Each pin on the upstream side of PTN38003A connecting to the Type-C connector has specific input/output configuration, and must match the signal assignments on the downstream side accordingly. Table 6 shows the upstream pin connection facing the Type-C receptacle.

Table 6. Upstream pin connection to Type-C receptacle in UFP application

PTN38003A pins		USB Type-C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
14	D_IOP	B2	TX2+
15	D_ION	B3	TX2-
9	C_INN	A10	RX2-
10	C_INP	A11	RX2+
6	A_INP	B11	RX1+
7	A_INN	B10	RX1-
1	B_IOP	A2	TX1+
2	B_ION	A3	TX1-
18	AUXP		Output of SBU XBAR
17	AUXN		Output of SBU XBAR

The downstream pins of PTN38003A are connected to the device processor, with specific functions assigned to each differential signal. For each pin assignment configuration below, PTN38003A controls which transmitters or receivers to turn on or turn off, and operating in USB3.2 or DisplayPort mode according to the mode setting.

Table 7. Downstream pin connection to device processor in UFP receptacle application

PTN38003A pins		Device processor signal names							
Symbol	**Pin name**	**USB3.2 Gen 1/2 X2**		**USB3.2 Gen 1/2 X1**		**USB3 & DP 2-Lane**		**DP 4-Lane**	
		Normal	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**
20	DRX1N	SSTX2-	SSTX1-		SSTX-	ML0-	SSTX-	ML0-	ML3-
19	DRX1P	SSTX2+	SSTX1+		SSTX+	ML0+	SSTX+	ML0+	ML3+
24	DTX1P	SSRX2+	SSRX1+		SSRX+	ML1+	SSRX+	ML1+	ML2+
25	DTX1N	SSRX2-	SSRX1-		SSRX-	ML1-	SSRX-	ML1-	ML2-
28	DTX2P	SSRX1+	SSRX2+	SSRX+		SSRX+	ML1+	ML2+	ML1+
27	DTX2N	SSRX1-	SSRX2-	SSRX-		SSRX-	ML1-	ML2-	ML1-
33	DRX2P	SSTX1+	SSTX2+	SSTX+		SSTX+	ML0+	ML3+	ML0+
32	DRX2N	SSTX1-	SSTX2-	SSTX-		SSTX-	ML0-	ML3-	ML0-

7.7 Control and programmability

7.7.1 Power-on operational mode

After POR initialization, if AUTO_ORIENT_EN pin is LOW, the chip is put into deep power saving state. In the deep power saving state, PTN38003A line drivers and input receive paths are terminated to ground with hi-ohmic resistors. If AUTO_ORIENT_EN pin is HIGH, then the device goes into USB mode of operation.

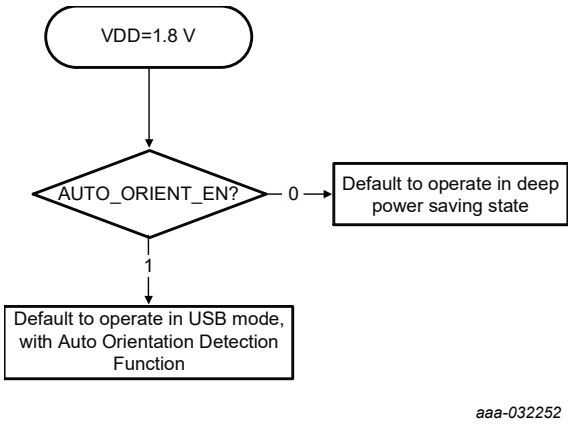


Figure 5. AUTO_ORIENT_EN control flow diagram

7.7.2 Auto Orientation Detection feature

PTN38003A is designed to detect the plug-in orientation autonomously based on SuperSpeed USB characteristics. This function may not work properly if SuperSpeed USB interface is not enabled in the host's or device's operation mode. Refer to Figure 6 for overall operating settings, and details are explained below.

Auto orientation detection feature is enabled through either setting AUTO_ORIENT_EN pin to high at power on reset, or through setting I^2C register 0x04 bit 7 to 1. When auto orientation detection is enabled through AUTO_ORIENT_EN pin at power on reset, PTN38003A transitions to USB mode by default, and the auto orientation detection process is executed without any firmware intervention. After the orientation is determined, "orientation" bit (register 0x04 bit 4) is updated, with "orientation done" bit (register 0x04 bit 6) set to 1. Since there is no way to indicate DFP or UFP application mode at power up reset when the detection process is executed, reporting of orientation is based on DFP application use case. At the same time, LCTLx and RCTLx pin values are used to configure USB upstream and downstream channel conditions.

If this feature is not enabled at power on reset, it can be enabled separately through I^2C register 0x04 bit 7 when the device is programmed to operate in USB only mode (register 0x04 bit [2:0] = 001). In addition, DFP or UFP application mode can be programmed in register 0x04 bit 5. When auto orientation detection process is completed, valid orientation will be reported in register 0x04 bit 4, based on the DFP or UFP application programmed information, with "orientation done" bit (register 0x04 bit 6) set to 1. USB's upstream and downstream channel conditions are also applied based on LCTLx and RCTLx values in register 0x10 through 0x13.

The auto orientation detection process is executed only once using either one of two methods mentioned above. After the orientation is found (register 0x04 bit 6 is set to 1),

setting register 0x04 bit 7 to 1 will not re-initiate the auto orientation detection procedure, as long as the mode bits (register 0x04 bit [2:0]) are not set to Deep Power Saving mode (000). I^2C controller may further configure PTN38003A to other operating modes (DP 2-Lane+USB, DP 4-Lane) with a different orientation if necessary, and correct pin configuration will be adjusted accordingly. Setting the mode bits (register 0x04 bit [2:0]) to Deep Power Saving mode (000) before the orientation done bit is set to 1 will result in aborting the auto orientation detection process.

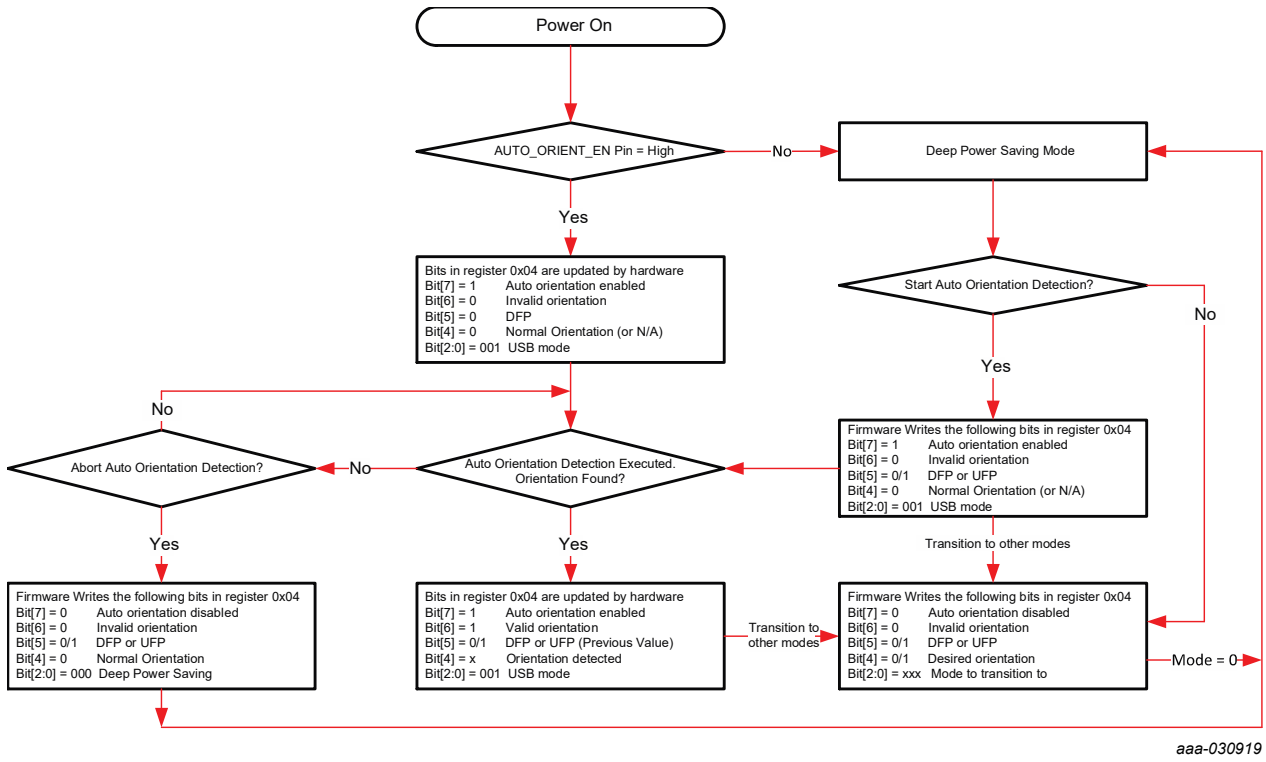


Figure 6. Auto-orientation flowchart

7.7.3 Mode transitions

The mode transitions follow USB safe state transition requirements of USB Type-C cable and connection specification, USB Power Delivery and Alternate Mode specifications. Figure 7 illustrates the various functional modes and deep power saving state transitions.

In Deep Power Saving mode, all high-speed pins are put in USB Safe state. The AUX snooping function is disabled. When a valid Type-C cable is connected, the host PD controller could place PTN38003A in USB3 mode (mode 1). Once DP Alternate Mode is negotiated, PTN38003A adheres the USB safe state requirements before making the mode transition.

The user can configure the device to transition between different modes at any time. When transitioning from Mode 1 to Mode 2, the USB3 connectivity is left undisturbed and DP 2-Lane + AUX functionality is included and when transitioning from Mode 2 to Mode 1, USB3 connectivity is left undisturbed while disabling the DP redriver functionality. While in Mode 1, USB's non-config lane is held in USB safe state. It is possible to transition from DP 4-Lane to USB only without entering Deep Power Saving, or vice versa. PTN38003A takes care of transition to USB Safe state internally.

The orientation is assumed to be fixed in Figure 7, because a change in orientation requires a disconnect event which requires a return to USB Safe state.

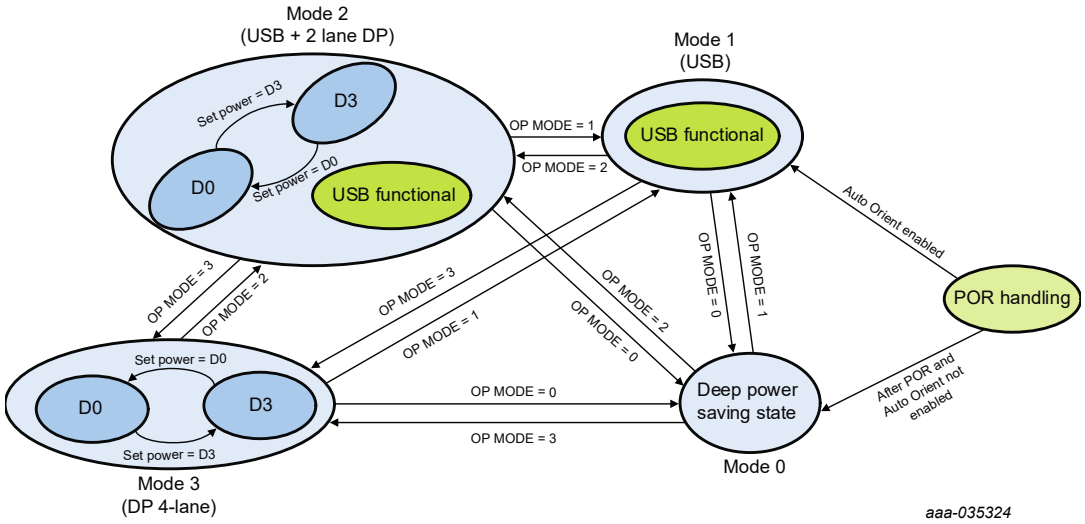


Figure 7. Mode transition state diagram

7.7.4 Channel settings for USB3.2 and DP Modes

The ternary channel condition inputs LCTL1, LCTL2, LCTL3, RCTL1, RCTL2, RCTL3 are enabled and sampled at POR. The detected values from these ternary inputs are used to initialize the I^2C registers. After entering via I^2C interface, changes to the ternary channel conditions are ignored and subsequent writes of I^2C values overwrite the sampled ternary inputs. Once the ternary inputs have been sampled during mode detection, there will be no mechanism to re-initialize the I^2C registers to the sampled values except via an I^2C write. When a software reset is issued, I^2C register values get reset to the stored value of the ternary inputs sampled at power-up.

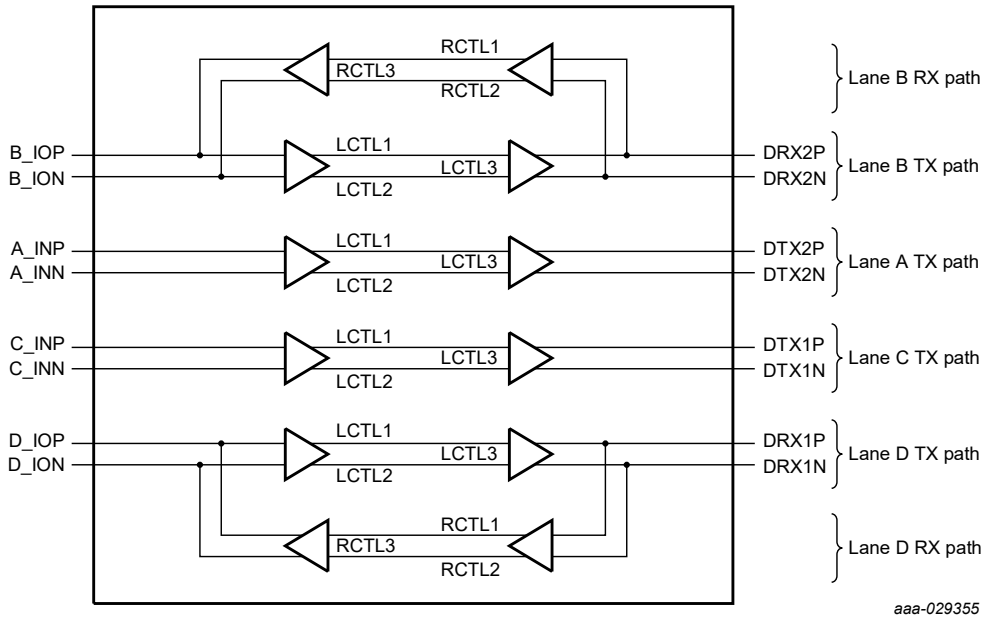


Figure 8. LCTL/RCTL signals to corresponding transmitter or receiver

Table 8 will be expanded to cover gain values at different link rates for each of the protocols - USB and DP.

Table 8. LCTL[2:1] and RCTL[2:1] Channel configurations: Flat gain = 0

Peaking Gain is the equalization gain at specific frequency relative to gain at 100 MHz and for Flat Gain (FG) = 0

I^2C register value <3:0>	LCTL2/ RCTL2	LCTL1/ RCTL1	Unit	Gain at 100 MHz (as reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5.0 GHz	6.75 GHz	10 GHz
0000	LOW	OPEN	dB	0.5	-0.2	-0.4	-0.1	-0.1	0.1	0.5	1.0	2.0
0001	OPEN	LOW	dB	0.5	-0.1	-0.3	0.0	0.1	0.4	0.8	1.5	2.8
0010			dB	0.5	0.0	-0.2	0.2	0.3	0.7	1.2	2.0	3.8
0011	HIGH	HIGH	dB	0.5	0.1	0.0	0.6	0.7	1.3	1.9	3.0	5.4
0100			dB	0.5	0.3	0.1	0.9	0.9	1.6	2.4	3.6	6.4
0101	HIGH	OPEN	dB	0.5	0.6	0.5	1.5	1.6	2.6	3.5	5.1	8.4
0110			dB	0.6	0.7	0.8	1.8	2.0	3.1	4.1	5.9	9.5
0111	HIGH	LOW	dB	0.6	1.1	1.3	2.6	2.8	4.2	5.4	7.5	11.6
1000			dB	0.6	1.5	1.8	3.4	3.6	5.3	6.6	9.0	13.4
1001	OPEN	HIGH	dB	0.6	1.7	2.0	3.7	4.0	5.7	7.2	9.7	14.2
1010			dB	0.6	2.0	2.4	4.4	4.7	6.7	8.2	10.9	15.6
1011	LOW	HIGH	dB	0.6	2.4	2.8	5.0	5.3	7.4	9.1	11.9	16.8
1100			dB	0.6	2.6	3.2	5.4	5.7	8.0	9.7	12.7	17.5
1101	OPEN	OPEN	dB	0.7	2.9	3.7	5.9	6.2	8.6	10.4	13.6	18.4
1110			dB	0.7	2.9	3.7	5.9	6.2	8.6	10.5	13.6	18.4
1111	LOW	LOW	dB	0.7	2.9	3.7	5.9	6.2	8.6	10.5	13.6	18.4

Table 9. LCTL[2:1] and RCTL[2:1] Channel configurations: Flat gain = 1

Peaking Gain is the equalization gain at specific frequency relative to gain at 100 MHz and for Flat Gain (FG) = 1

I^2C register value <3:0>	LCTL2/ RCTL2	LCTL1/ RCTL1	Unit	Gain at 100 MHz (as reference)	0.81 GHz	1.35 GHz	2.5 GHz	2.7 GHz	4.05 GHz	5.0 GHz	6.75 GHz	10 GHz
0000	LOW	OPEN	dB	-1.1	-0.1	-0.2	0.5	0.6	1.3	1.9	2.6	3.8
0001	OPEN	LOW	dB	-1.1	0.0	-0.1	0.7	0.8	1.6	2.2	3.1	4.6
0010			dB	-1.1	0.1	0.0	1.0	1.1	1.9	2.7	3.7	5.6
0011	HIGH	HIGH	dB	-1.1	0.3	0.2	1.4	1.6	2.6	3.4	4.7	7.2
0100			dB	-1.1	0.5	0.4	1.7	1.9	3.0	4.0	5.4	8.1
0101	HIGH	OPEN	dB	-1.1	0.9	1.0	2.5	2.7	4.0	5.1	6.9	10.2
0110			dB	-1.0	1.1	1.3	2.9	3.1	4.6	5.8	7.7	11.3
0111	HIGH	LOW	dB	-1.0	1.6	2.0	3.8	4.0	5.8	7.1	9.3	13.3
1000			dB	-1.0	2.0	2.5	4.6	4.9	6.9	8.3	10.7	15.1
1001	OPEN	HIGH	dB	-1.0	2.3	2.8	5.0	5.3	7.4	8.9	11.4	15.9
1010			dB	-1.0	2.7	3.3	5.8	6.1	8.3	9.9	12.6	17.3
1011	LOW	HIGH	dB	-1.0	3.1	3.8	6.4	6.7	9.1	10.8	13.6	18.4
1100			dB	-0.9	3.3	4.2	6.8	7.1	9.6	11.4	14.3	19.1
1101	OPEN	OPEN	dB	-0.9	3.7	4.7	7.3	7.7	10.2	12.1	15.2	20
1110			dB	-0.9	3.7	4.7	7.3	7.7	10.2	12.1	15.2	20
1111	LOW	LOW	dB	-0.9	3.7	4.7	7.3	7.7	10.2	12.1	15.2	20

Table 10. LCTL3/RCTL3 channel configuration

I^2C Register Value	LCTL3	RCTL3	Output Swing Linearity
0			500 mV_{ppd}
1	OPEN	OPEN	650 mV_{ppd}
2	LOW	LOW	800 mV_{ppd}
3	HIGH	HIGH	950 mV_{ppd}

7.7.5 I^2C configurability

PTN38003A has an I^2C register interface that enables system integrator to program register settings suitable as per application needs. After power on reset, the device reads the ADDR pin for determining the I^2C Slave Address. PTN38003A provides up to four I^2C Slave address combinations based on quaternary pin (ADDR) setting, and they are summarized in Table 11.

Table 11. I^2C slave address options

ADDR pin state	7-bit I^2C slave address	8-bit I^2C address							
Connected to 1.8 V supply directly	011-0011 (0x33)	0	1	1	0	0	1	1	R/W
Connected to 1.8 V with 56 kΩ (±10 %) pull-up resistor	011-0010 (0x32)	0	1	1	0	0	1	0	R/W
Connect to 1.8 V with 200 kΩ (±10 %) pull-up resistor	011-0001 (0x31)	0	1	1	0	0	0	1	R/W
Connected to GND directly	011-0000 (0x30)	0	1	1	0	0	0	0	R/W

7.7.6 I²C registers

The system integrator must program the registers of the device for proper operation. Further, it is expected that the system integrator performs I²C configuration after power-up and before data transport is initiated over the link. If such an operation is attempted during normal operation, the device may not behave as specified.

Table 12. I²C registers and description

Register offset	Register name	Bits	POR default value	Description
0x00 Read Only	Chip ID	7:0	b'00001011	Chip ID Number
0x01 Read Only	Chip Revision	7:4	b'1010	Chip base layer version
		3:0	b'0001	Chip metal layer version
0x02	Reserved	7:0	b'0000 0000	
0x03	Flat gain control			Flat gain control setting for each high speed data path. The gain is specified at 100 MHz
		7:6	b'00	Write '0' only. Read is don't care
		5	b'0	Lane B Rx path (Figure 8) flat gain control 0 = flat gain of +0.7 dB, 1 = flat gain of -0.7 dB
		4	b'0	Lane D Rx path flat gain control 0 = flat gain of +0.7 dB, 1 = flat gain of -0.7 dB
		3	b'0	Lane B Tx path (Figure 8) flat gain control 0 = flat gain of +0.7 dB, 1 = flat gain of -0.7 dB
		2	b'0	Lane A Tx path flat gain control 0 = flat gain of +0.7 dB, 1 = flat gain of -0.7 dB
		1	b'0	Lane C Tx path flat gain control 0 = flat gain of +0.7 dB, 1 = flat gain of -0.7 dB
		0	b'0	Lane D Tx path downstream flat gain control 0 = flat gain of +0.7 dB, 1 = flat gain of -0.7 dB

Table 12. I^2C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
0x04 Read/Write	Mode control	7	AUTO_ ORIENT_EN pin value	Auto orientation enable bit is used to select Auto orientation option • 1 = Enable • 0 = Disable or abort an ongoing auto orientation detection process
		6	b'0	Orientation done bit • When 0, 'Plug orientation control' bit (bit 4) is not valid • When 1, then it conveys 'Plug orientation control' bit (bit 4) is valid. This bit is cleared when Auto orientation enable (bit 7) is cleared by host, and it is not valid when bit 7 is '0'. Writes to this bit do not have any effect.
		5	b'0	DFP or UFP configuration • 0: DFP configuration • 1: UFP configuration
		4	b'0	Plug orientation control. This orientation condition applies to high-speed TX/RX configuration • 0: normal plug orientation of Type-C connection • 1: reverse plug orientation of Type-C connection This bit is to be written/read by the host or it can get updated automatically whenever ‘Auto orientation enable’ option is selected by setting bit 7 to ‘1'. If bit 7 is ‘1’, then the bit value is valid only when ‘Orientation done’ bit (bit 6) is ‘1’. The host shall not write this bit while bit[7] = 1. Overriding the orientation selection is possible only when bit 7 is cleared.
		3	b'0	AUX snooping polarity control bit • When 0, AUXP/AUXN signal polarities follow pin naming: – Pin 18 = AUXP – Pin 17 = AUXN • When 1, AUXP/AUXN signal polarities are reverse of the pin naming: – Pin 17 = AUXP – Pin 18 = AUXN
		2:0	b'000	Operational mode of the device. Refer to Section 7.7.3 for mode transition requirement • 0: Deep power saving state • 1: USB3.2 • 2: USB3.2 and 2-lane DP • 3: 4-lane DP • 4-7 Reserved

Table 12. I^2C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
0x05 Read/Write	Device control	7:1	b'0001010	Reserved
		0	b'0	Device Reset bit. This is a self-clearing bit, and reading this register will always return 0. • Writing a '1' to this register will soft reset the device including I^2C register contents and internal digital logic states, while the chip continuing to operate under I^2C mode. • Writing a '0' does not have any effect.
0x06 Read/Write	DP link control and status	7:5	b'000	Write '0' only. Read is don't care
		4	b'0	DisplayPort Power saving mode selection on all DP lanes. • 0: Normal/Active mode • 1: D3 Power saving mode This field may be modified thru I^2C write or AUX monitor function. When corresponding DPCD register changes are detected via AUX monitor, this field will be updated.
		3:2	b'00	DisplayPort operating lane count • 0: 0 DP Lane • 1: 1 DP Lane • 2: 2 DP lanes • 3: 4 DP lanes This field may be modified thru I^2C write or AUX monitor function. When corresponding DPCD register changes are detected via AUX monitor, this field will be updated.
		1:0	b'00	DP Link rate • 0: 1.62 Gbps (RBR) • 1: 2.7 Gbps (HBR) • 2: 5.4 Gbps (HBR2) • 3: 8.1 Gbps (HBR3) The field may be modified through I^2C write or AUX monitor function. When corresponding DPCD register changes are detected via AUX monitor, this field will be updated.
0x07 Read/Write	DP Lane 0 Control_1 Register	7:4	b'00	Write '0' only. Read is don't care
		3:0	LCTL1, LCTL2	DP Lane 0 link Equalization gain. Refer to Peaking gain tables - Table 8 and Table 9 in Section 7.7.4 for more details.
0x08 Read/Write	DP Lane 0 Control_2 Register	7:2	b'0000 00	Write '0' only. Read is don't care
		1:0	LCTL3	DP Lane 0 output signal swing linearity • 0: 500 mVppd • 1: 650 mVppd • 2: 800 mVppd • 3: 950 mVppd

Table 12. I^2C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
0x09 Read/Write	DP Lane 1 Control_1 Register	7:4	b'0000	Write '0' only. Read is don't care
		3:0	LCTL1, LCTL2	DP Lane 1 link Equalization gain. Refer to Peaking gain tables - Table 8 and Table 9 in Section 7.7.4 for more details.
0x0A Read/Write	DP Lane 1 Control_2 Register	7:2	b'0000 00	Write '0' only. Read is don't care
		1:0	LCTL3	DP Lane 1 output signal swing linearity • 0: 500 mVppd • 1: 650 mVppd • 2: 800 mVppd • 3: 950 mVppd
0x0B Read/Write	DP Lane 2 Control_1 Register	7:4	b'0000	Write '0' only. Read is don't care
		3:0	LCTL1, LCTL2	DP Lane 2 link Equalization gain. Refer to Peaking gain tables - Table 8 and Table 9 in Section 7.7.4 for more details.
0x0C Read/Write	DP Lane 2 Control_2 Register	7:2	b'0000 00	Write '0' only. Read is don't care
		1:0	LCTL3	DP Lane 2 output signal swing linearity • 0: 500 mVppd • 1: 650 mVppd • 2: 800 mVppd • 3: 950 mVppd
0x0D Read/Write	DP Lane 3 Control_1 Register	7:4	b'0000	Write '0' only. Read is don't care
		3:0	LCTL1, LCTL2	DP Lane 3 link Equalization gain. Refer to Peaking gain tables - Table 8 and Table 9 in Section 7.7.4 for more details.
0x0E Read/Write	DP Lane 3 Control_2 Register	7:2	b'0000 00	Write '0' only. Read is don't care
		1:0	LCTL3	DP Lane 3 output signal swing linearity • 0: 500 mVppd • 1: 650 mVppd • 2: 800 mVppd • 3: 950 mVppd
0x0F Read/Write	LOS detector threshold	7	0	LFPS detection disable in U2/U3 state in USB3 operation. This bit can be set/changed only during Deep Power saving mode. 0: LFPS detector is used in U2/U3 state to transition back to U0 state 1: LFPS detector is not used to transition from U2/U3 state to U0 state
		6	0	LOS detector disable in USB3 operation. This bit can be set/changed only during Deep Power saving mode. 0: LOS detector is enabled 1: LOS detector is disabled

Table 12. I^2C registers and description*...continued*

Register offset	Register name	Bits	POR default value	Description
		5:4	b'00	Chip upstream (B_IO, A_IN, C_IN, and D_IO) side LOS detector threshold setting • 0: 45 mV (default/POR) • 1: 60 mV • 2: 70 mV • 3: 80 mV • Other values are reserved The setting is applicable for operational modes (USB3.2 and DP). It is used as a signal threshold reference for low power state management
		3:2	b'00	USB3 power saving mode (U2/U3) and compliance mode select. This function is only valid when bit 6 is set to 1. When entering USB mode, PTN38003A is in U0 state. System can write this bit to enter Power saving mode (U2/U3) or compliance mode. These bits are updated to 00 after PTN38003A exits power saving mode (U2/U3) to active mode (U0), or compliance mode to active mode (U0). 00: Active state (U0) 01: Power saving state (U2/U3) 10: Compliance mode 11: Transition from power saving state (U2/U3) to active state (U0)
		1:0	b'00	Chip downstream (DRX1 and DRX2) side LOS detector threshold setting. • 0: 45 mV (default/POR) • 1: 60 mV • 2: 70 mV • 3: 80 mV • Other values are reserved The setting is applicable for USB3.2 mode. It is used as a signal threshold reference for low power state management
0x10	USB_Downstream_RX_ Control	7:4	b'0000	Write '0' only. Read is don't care
		3:0	RCTL1, RCTL2	USB3.2 Mode downstream (DRX2 and DRX1) side link Equalization gain. Refer to Peaking gain tables - Table 8 and Table 9 in Section 7.7.4 for more details.
0x11 Read/Write	USB_Upstream_TX_ Control	7:2	b'0000 00	Write '0' only. Read is don't care
		1:0	RCTL3	USB3.2 Mode upstream (B_IO and D_IO) side link output signal swing linearity • 0: 500 mVppd • 1: 650 mVppd • 2: 800 mVppd • 3: 950 mVppd

Table 12. I²C registers and description...*continued*

Register offset	Register name	Bits	POR default value	Description
0x12 Read/Write	USB_Upstream_ RX_ Control	7:4	b'0000	Write '0' only. Read is don't care
		3:0	LCTL1, LCTL2	USB3.2 Mode upstream (A_IN and C_IO) side link Equalization gain. Refer to Peaking gain tables - Table 8 and Table 9 in Section 7.7.4 for more details.
0x13 Read/Write	USB_Downstream_TX_ Control	7:2	b'0000 00	Write '0' only. Read is don't care
		1:0	LCTL3	USB3.2 Mode downstream (DTX2 and DTX1) side link output signal swing linearity • 0: 500 mVppd • 1: 650 mVppd • 2: 800 mVppd • 3: 950 mVppd
0x14 to 0xFF	Reserved			Reserved for NXP Internal use only; Do not write to these registers

7.7.7 I²C read/write operations

PTN38003A supports programming of the registers through the I²C interface. Reading/writing the registers must be done according to protocols defined in the UM10204, "I²C - bus specification and user manual"; NXP Semiconductors, Revision 06 April 4, 2014 [4]

PTN38003A supports programming of the registers through the I²C interface. Reading/writing the registers must be done according to the following sequences.

The read sequence contains two phases:

- Command phase
- Data phase

7.7.7.1 Single byte register reads/writes

The command phase is an I²C write to PTN38003A that contains a single data byte. The LS bit indicates if the command that is being executed will read or write data from/to the device. The other 7 bits are the device slave address. The single data byte followed is the register offset that is used to indicate which register address is being accessed (read or written). The data phase is a second I²C transaction that starts with 7-bit slave address, with LS bit set to 1 indicating a read operation, followed by an 8-bit data read back from the device register address.

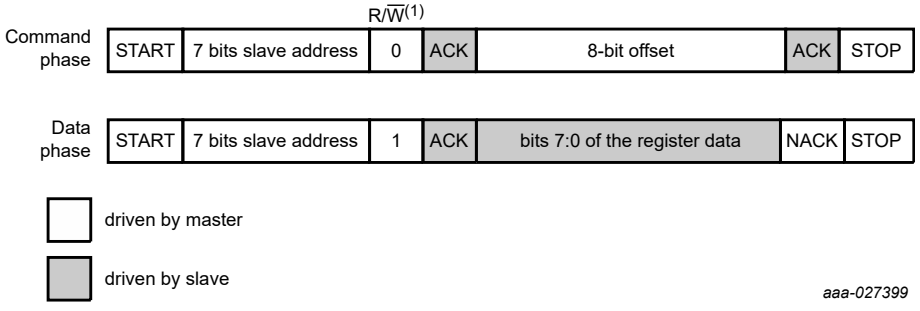


Figure 9. I²C read sequence

(1) R/$\overline{W}$ = read/write bit. 0b = I^{2}C write; 1b = I^{2}C read

The write sequence starts with 7-bit slave address, with LS bit set to 0 indicating a write access. The next byte is the register offset that is used to indicate which device register address is being written to. The last byte is the 8-bit register data that will be written to the device register address.

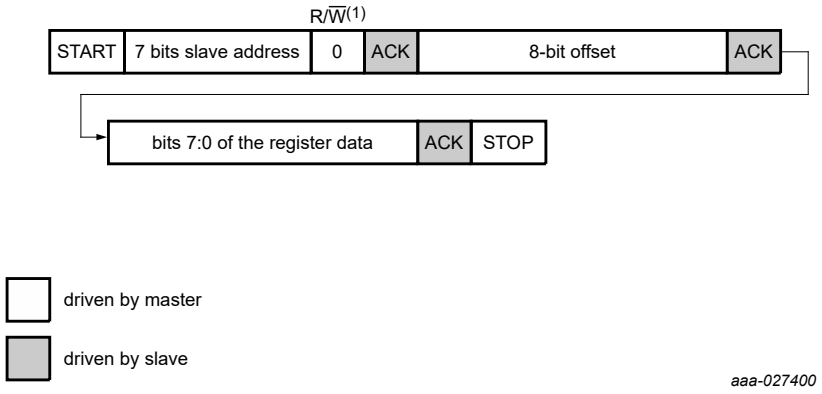


Figure 10. I^{2}C write sequence

(1) R/$\overline{W}$ = read/write bit. 0b = I^{2}C write; 1b = I^{2}C read

7.7.7.2 Multi-byte register reads/writes

Reading one or more registers

The slave recognizes the following procedure as a request to read one or more registers:

1. Master asserts START condition or repeated-START condition
2. Master addresses PTN38003A's slave address with R/W bit set as "Write"
3. Slave acknowledges the request by asserting ACK
4. Master writes the desired starting register address
5. Slave acknowledges the register address with ACK, even if the register address is not part of the defined register map
6. Master issues a repeated-START condition
7. Master addresses PTN38003A's slave address with R/W bit set as "Read"
8. In the following clock pulses, the slave clocks out the value of the requested register
9. If master wishes to read the next consecutive register, it issues an ACK and then provides another set of clock pulses, whereby the slave supplies the value of the next register. As long as the master continues to issue ACK and supplies additional clock pulses, the slave continues to supply the value of consecutive registers. If the master attempts to read consecutive registers that do not exist in the defined register space the slave returns undefined data value of 0xFF
10. When the master does not wish to read additional consecutive registers, it supplies a NACK in response to the final register value it wishes to read and then issues a STOP or repeated-START condition.

Figure 11 provides an illustrative example where the master chooses to read from two consecutive registers starting with register "R".

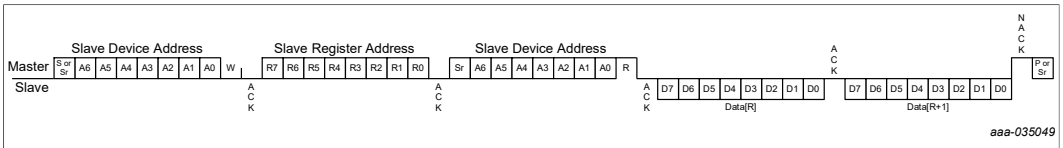


Figure 11. Reading one or more consecutive registers

Writing one or more registers

The slave recognizes the following procedure as a request to write to one or more registers.

1. Master asserts START condition or repeated-START condition
2. Master addresses PTN38003A's slave address with R/W bit set as "Write"
3. Slave acknowledges the request by asserting ACK
4. Master writes the desired starting register address
5. Slave acknowledges the register address with ACK, even if register address is not part of the defined register map
6. Master writes the data for that register address. Slave updates the value of that register once all 8 bits of data have been written
7. Slave acknowledges the data with ACK
8. If the master wishes to write to the next consecutive register address, it supplies another data byte, which the slave ACKs. The master continues writing data bytes for consecutive registers. If the master writes to more consecutive registers than exist in the register map, the slave discards the extra data bytes, but ACKs each byte. When the master finishes writing the desired register(s), it issues either a STOP condition or a repeated-START condition
   Figure 12 provides an illustrative example where the master chooses to write to three consecutive registers starting with register "R".

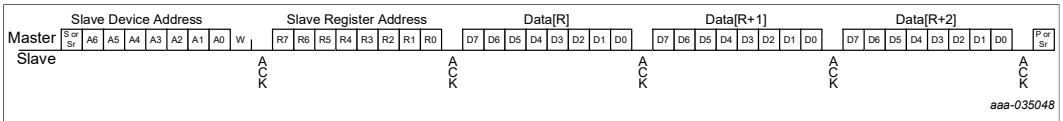


Figure 12. Writing one or more consecutive registers

8 Limiting values

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

In accordance with the Absolute Maximum Rating System (IEC 60134).

Table 13. Limiting values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{DD}[1]	Supply voltage	1.8 V digital supply voltage	-0.5		+2.2	V	LTC-VOL-PRIO1-001
V_{CCXX}[1]	Supply voltage for high-speed lanes	VCCA, VCCB, VCCC, VCCD	-0.5		+2.2	V	LTC-VOL-PRIO1-002
V_I[1]	Input voltage	AUTO_ORIENT_EN, SCL, SDA, LCTL1, LCTL2, LCTL3, RCTL1, RCTL2, RCTL3, ADDR AUXP/N pins	-0.5		+3.6	V	LTC-VOL-PRIO1-005
		High-speed pins	-0.5		+2.5	V	LTC-VOL-PRIO1-006
T_{stg}	Storage temperature		-65		+150	°C	LTC-TMP-PRIO1-007
V_{esd}	Electrostatic discharge	HBM[2] for High-speed and AUX/LS pins	1500			V	LTC-VOL-PRIO1-008
		HBM for other control pins	1500			V	LTC-VOL-PRIO1-009
		CDM[3] for High-speed and AUX /LS pins	1000			V	LTC-VOL-PRIO1-010
		CDM for other control pins	1000			V	LTC-VOL-PRIO1-011
$R_{th(j-a)}$	Thermal resistance from junction to ambient environment	JEDEC still air test environment		40.6		°C/W	LTC-RES-PRIO2-012
$R_{th(j-c)}$	Thermal resistance from junction to case			16.8		°C/W	LTC-RES-PRIO2-013
$R_{th(j-b)}$	Thermal resistance from junction to board	FR4 PCB material and with center pad soldered with recommended solder pad structure		19.7		°C/W	LTC-RES-PRIO2-014

[1] All voltage values, except differential voltages, are with respect to network ground terminal.
[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model – Component level; Electrostatic Discharge Association, Rome, NY, USA.
[3] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model – Component level; Electrostatic Discharge Association, Rome, NY, USA

9 Recommended operating conditions

Over operating free-air temperature range (unless otherwise noted). Typical values are specified for 1.8 V and 25 °C operating temperature.

Table 14. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{DD}	Supply voltage	1.8 V Digital Supply voltage	1.7	1.8	1.9	V	ROC-VOL-PRIO1-001
V_{CC}	Supply voltage for high-speed lanes	VCCA, VCCB, VCCC, VCCD	1.7	1.8	1.9	V	ROC-VOL-PRIO1-002
V_I	Input voltage	AUTO_ORIENT_EN, SCL, SDA, LCTL1, LCTL2, LCTL3, RCTL1, RCTL2, RCTL3, AUXP/N pins	-0.3		+3.6	V	ROC-VOL-PRIO1-003
		ADDR pin (in I^2C mode)	-0.3		V_{DD}	V	ROC-VOL-PRIO1-004
		High-speed Data pins	-0.3		V_{CC}+0.3	V	ROC-VOL-PRIO1-005
V_{SYS}	Power supply voltage for control signals		1.7		3.6	V	ROC-VOL-PRIO1-006
	Power supply voltage for I^2C signals		1.08		3.6	V	ROC-VOL-PRIO1-007
T_{amb}	Ambient temperature	Operating in free air	-20	-	+85	°C	ROC-TMP-PRIO1-008

10 Characteristics

10.1 Device characteristics

Table 15. Device characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{GND_VCC} noise	Noise voltage from DUT (50 Hz to 1 MHz) GND noise/bounce with VCC as the reference point	DUT only and No bypass cap during testing Test recommendations: Battery powered DUT with VCC pin as the reference power plan and measure the GND pin ground bounce. Measured by power rail probe		18		mVpp	DEV-VOL-PRIO2-001
	Noise voltage (1 MHz to 10 MHz)			18		mVpp	DEV-VOL-PRIO2-002
	Noise voltage (10 MHz to 5 GHz)				10	mVpp	DEV-VOL-PRIO1-003
CMRR	Common Mode Rejection Ratio Δ(Vcm,rx)/Δ(Vout_diff)	10 MHz to 1 GHz		30		dB	DEV-DB-PRIO2-004
PSRR	Power Supply Rejection Ratio Δ(VCC)/Δ(Vout_diff)	10 MHz to 200 MHz		41		dB	DEV-DB-PRIO2-005
$t_{Startup}$	Start-up time	Between supply voltage exceeding 1.4 V until sampling of control pins	-		3	ms	DEV-TIM-PRIO1-006
$t_{Startup\_USB}$	USB start-up time	Time between configuration in USB operating mode until automatic receive detection is active	-		5	ms	DEV-TIM-PRIO1-007
$t_{S(EN-DIS)}$	Enable to Disable settling time (Deep power saving mode)	Power down control change until Deep Power Saving mode is entered. Device is supplied with valid supply voltage	-		1	ms	DEV-TIM-PRIO1-008
T_{mode_rcfg}	Mode control Reconfiguration time	Mode control configuration change			0.5	ms	DEV-TIM-PRIO1-010
t_{PD}	Differential Propagation Delay	Differential propagation delay between 50 % level at input and output of SuperSpeed pins		70	90	ps	DEV-TIM-PRIO1-011
t_{idle}	Idle Time	Time to wait before getting into power saving U2/U3 state (in USB Mode), D3 state (in DP)		300	400	ms	DEV-TIM-PRIO1-012

Table 15. Device characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
$t_{ps-exit}$	Power Saving Exit Time	Time for exiting from Power saving U2/U3 state and get into Active state in USB3.2 mode, D0 (in DP)			115	µs	DEV-TIM-PRIO1-013
Gp	Peaking gain (compensation at 10 GHz, 5 GHz and 4.05 GHz, relative to gain at 100 MHz; sinusoidal input of 100 mVppd)	xCTL[2:1] = Hi-Z: Hi-Z at 10 GHz (Table 9)		20		dB	DEV-DB-PRIO2-016
		xCTL[2:1] = Hi-Z: Hi-Z at 5.0 GHz (Table 9)		12.1		dB	DEV-DB-PRIO2-017
		xCTL[2:1] = Hi-Z: Hi-Z at 4.05 GHz (Table 9)		10.2		dB	DEV-DB-PRIO2-018
Gp,var	Peaking gain variations over Gp at 10 GHz		-2.3	-	+2.3	dB	DEV-DB-PRIO1-019
Gf	Flat gain at 100 MHz	positive flat gain setting		+0.7		dB	DEV-DB-PRIO2-020
		negative flat gain setting		-0.7		dB	DEV-DB-PRIO2-021
Gf,var	Flat gain variations over Gf at 100 MHz		-1.2	-	+1.2	dB	DEV-DB-PRIO1-022
OLS_{100M}	Output swing linearity (-1 dB compression point) at 100 MHz	xCTL3 = I^2C (based on I^2C register settings)		500		mVppd	DEV-VOL-PRIO2-023
		xCTL3 = Open		650		mVppd	DEV-VOL-PRIO2-024
		xCTL3 = 0		800		mVppd	DEV-VOL-PRIO2-025
		xCTL3 = 1		950		mVppd	DEV-VOL-PRIO2-026
OLS_{5G}	Output swing linearity (-1 dB compression point) at 5 GHz	xCTL3 = I^2C (based on I^2C register settings)		500		mVppd	DEV-VOL-PRIO2-027
		xCTL3 = Open (Table 10)		650		mVppd	DEV-VOL-PRIO2-028
		xCTL3 = 0 (Table 10)		800		mVppd	DEV-VOL-PRIO2-029
		xCTL3 = 1 (Table 10)		950		mVppd	DEV-VOL-PRIO2-030
OLS_{10G}	Output swing linearity (-1 dB compression point) at 10.3 GHz	xCTL3 = I^2C (based on I^2C register settings)		500		mVppd	DEV-VOL-PRIO2-031
		xCTL3 = Open (Table 10)		650		mVppd	DEV-VOL-PRIO2-032
		xCTL3 = 0 (Table 10)		800		mVppd	DEV-VOL-PRIO2-033
		xCTL3 = 1 (Table 10)		950		mVppd	DEV-VOL-PRIO2-034
V_{noise_in}	Input referred noise	100 MHz to 15 GHz; Peaking gain of 9.9 dB (at 5 GHz) and OS 950 mVppd		0.8		mV_{rms}	DEV-VOL-PRIO2-035
V_{noise_out}	Output referred noise	100 MHz to 15 GHz; Peaking gain of 9.9 dB (at 5 GHz) and OS 950 mVppd		2.0		mV_{rms}	DEV-VOL-PRIO2-037

Table 15. Device characteristics*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{LOS}	(I^2C configured) LOS threshold level	LOS threshold 3; I^2C 0X0F byte [5:4] or [1:0]		80		mVppd	DEV-VOL-PRIO2-039
		LOS threshold 2; I^2C 0X0F byte [5:4] or [1:0]		70		mVppd	DEV-VOL-PRIO2-040
		LOS threshold 1; I^2C 0X0F byte [5:4] or [1:0]		60		mVppd	DEV-VOL-PRIO2-041
		LOS threshold 0; I^2C 0X0F byte [5:4] or [1:0]		45		mVppd	DEV-VOL-PRIO2-042
V_{LFPS}	LFPS threshold level		100	180	300	mVppd	DEV-VOL-PRIO1-043
I_{DD}	Supply current All 4 channels active, Mode 2/3/4/5	Output swing linearity selection of 950 mVppd		250	270	mA	DEV-CUR-PRIO1-044
		Output swing linearity selection of 800 mVppd		225	260	mA	DEV-CUR-PRIO1-045
		Output swing linearity selection of 650 mVppd		200	240	mA	DEV-CUR-PRIO1-046
		Output swing linearity selection of 500 mVppd		190	230	mA	DEV-CUR-PRIO1-047
	Supply current 2 channels USB 3.2 active, Mode 1	Output swing linearity selection of 950 mVppd		125	140	mA	DEV-CUR-PRIO1-048
		Output swing linearity selection of 800 mVppd		110	130	mA	DEV-CUR-PRIO1-049
		Output swing linearity selection of 650 mVppd		115	120	mA	DEV-CUR-PRIO1-050
		Output swing linearity selection of 500 mVppd		100	120	mA	DEV-CUR-PRIO1-051
	Supply current 1 lane/channel DP active, Mode 3	Output swing linearity selection of 950 mVppd		62	75	mA	DEV-CUR-PRIO1-052
		Output swing linearity selection of 800 mVppd		57	70	mA	DEV-CUR-PRIO1-053
		Output swing linearity selection of 650 mVppd		52	65	mA	DEV-CUR-PRIO1-054
		Output swing linearity selection of 500 mVppd		47	60	mA	DEV-CUR-PRIO1-055
	Supply current	Power saving mode (USB U2/ U3 modes)		0.22[1]		mA	DEV-CUR-PRIO2-056
				0.11[2]		mA	DEV-CUR-PRIO2-057
		Power saving mode (No Connection mode)		0.11[3]		mA	DEV-CUR-PRIO1-058
		Power saving mode (DP D3 mode, no USB)		3.2 [4]		mA	DEV-CUR-PRIO2-059
		Deep Power saving state (mode 0)		10		µA	DEV-CUR-PRIO2-060

Table 15. Device characteristics...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
DDNEXT1	Near end cross talk for adjacent high-speed channels (between TX and RX channels within the same USB3.2 lanes)	at 10.3 GHz between DTX1 and DRX1 channels; Between DTX2 and DRX2; Between B_IO and A_INN; Between D_IO and C_INN		-60		dB	DEV-DB-PRIO2-063
DDNEXT2	Near end cross talk for adjacent high speed -channels (between TX and RX channels from different USB3.2 lanes)	at 10.3 GHz between DTX1 and DRX2 channels; Between DTX2 and DRX1; Between B_IO and C_IN Between D_IO and A_IN		-55		dB	DEV-DB-PRIO2-064
$Xtak_{oo}$	The crosstalk between two output drivers for far end crosstalk analysis. (between any two DP lane/channels, two USB3.2 TX channels or two USB3.2 RX channels)	at 10.3 GHz For DP 4-Lane Mode, between any two channels among DRX1, DRX2, DTX1 and DTX2. For X2 USB3.2 Mode, between D_IO and B_IO		-34		dB	DEV-DB-PRIO2-065

[1] When both lanes are active
[2] When one lane is active. Only LFPS detector is enabled.
[3] Only Rx detection is enabled.
[4] When both LOS detector is enabled on Lane #0 and AUX transaction processing is enabled.

Note: *One lane for USB3.2 means One TX/RX pair (channels); for DisplayPort, one lane means one differential pair (channel)*

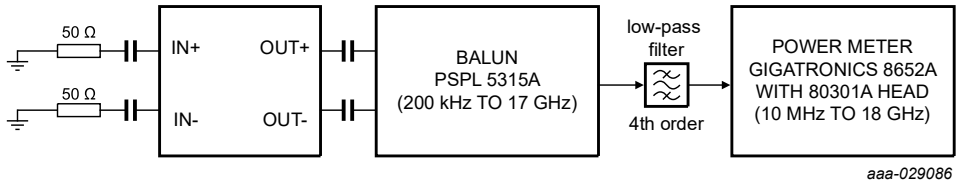


Figure 13. Noise test configuration

10.2 Input AC/DC characteristics

Table 16. Input AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
$C_{ac\_coupling}$	AC coupling capacitance		75		265	nF	INC-CAP-PRIO1-001
$C_{RX\_ac\_coupling}$	RX AC coupling capacitance		297		363	nF	INC-CAP-PRIO1-002
$T_{Discharge}$	Discharge time				250	ms	INC-TIM-PRIO1-003
$R_{in\text{-}DC}$	Input DC common mode impedance		21		34	Ω	INC-RES-PRIO1-004
$V_{RX\text{-}CM\text{-}AC\text{-}PP}$	RX AC common mode voltage tolerance for USB3.2	A single tone test at 120 MHz is deemed to be an adequate stress test			300	mVpp	INC-VOL-PRIO1-005
$V_{RX\text{-}CM\text{-}PP1}$	RX AC common mode voltage tolerance for DisplayPort application	A single tone test at 400 MHz is deemed to be an adequate stress test			100	mVpp	INC-VOL-PRIO1-006
$R_{IN\text{-}DIFF\text{-}DC}$	DC Differential Impedance		90		131	Ω	INC-RES-PRIO1-007
$V_{IP\text{-}DC\text{-}CM}$	DC biasing/common mode voltage	Biasing on all SuperSpeed pins		1.8		V	INC-VOL-PRIO2-008
$V_{voltage\_jump}$	Maximum voltage jump on left side pins (Axx, Bxx, cxx, Dxx) measured before AC coupling capacitors	Applicable during power-on/power-off, transition from low power to active state and vice versa	-0.3		1	V	INC-VOL-PRIO1-009
$Z_{IN\text{-}NO\text{-}POWER\text{-}DC\text{-}POS}$	DC input high impedance; VDD>0 during Reset or power down	RX low frequency CM impedance with the RX termination is not powered. Defined at the transmitter side of the AC capacitor as min(Δ_V/Δ_I) upon application of positive Tx step of any size up to +500mV from steady state	10			kΩ	INC-RES-PRIO1-010
$Z_{IN\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	USB DC Input High Impedance	USB DC common-mode input impedance when output of redriver is not terminated and V_{DD} between 1.7 V and 1.9 V. USB3.x controller should stop doing RX Detection before V_{DD} is powered down to avoid detection of low-ohmic RX input termination	25			kΩ	INC-RES-PRIO1-011

Table 16. Input AC/DC characteristics*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
$V_{RX\text{-}DIFF\text{-}PP}$	USB Input voltage (peak to peak differential signal)		45		1200	mVppd	INC-VOL-PRIO1-012
	DisplayPort Input voltage (peak to peak differential signal)		45		1400	mVppd	INC-VOL-PRIO1-013
$RL_{DD11,\ IN}$	Input differential mode Return Loss	100 MHz to 10.3 GHz		15		dB	INC-DB-PRIO2-014
$RL_{CC11,\ IN}$	Input common mode Return Loss	100 MHz to 10.3 GHz		12		dB	INC-DB-PRIO2-015

10.3 Output AC/DC characteristics

Table 17. Output AC/DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
R_{OP-DC}	Output DC common mode Impedance		21		34	Ω	OUC-RES-PRIO1-001
$R_{OP-DIFF-DC}$	Output Differential Impedance		89		131	Ω	OUC-RES-PRIO1-002
$V_{OP-DC-CM}$	DC biasing/common mode voltage	Output swing linearity selection of 950 mVppd		1.2		V	OUC-VOL-PRIO2-003
		Output swing linearity selection of 800 mVppd		1.3		V	OUC-VOL-PRIO2-004
		Output swing linearity selection of 650 mVppd		1.4		V	OUC-VOL-PRIO2-005
		Output swing linearity selection of 500 mVppd		1.5		V	OUC-VOL-PRIO2-006
$V_{TX-CM-AC-PP\_ACTIVE}$	Output AC Common mode output voltage in active state	Device input fed with differential signal			20	mVpp	OUC-VOL-PRIO1-007
$V_{TX-IDLE-DIFF-AC-pp}$	Output AC differential output voltage	When link is in electrical idle			10	mVppd	OUC-VOL-PRIO1-008
$V_{voltage\_jump}$	Maximum voltage jump on right side pins (DTXyy, DRXyy) measured after AC coupling capacitors	Applicable during power-on/power-off, transition from low power to active state and vice versa	-0.3		1	V	OUC-VOL-PRIO1-009
V_{DETECT}	Voltage change allowed during USB receiver detection	Positive voltage swing to sense the receiver termination detection			600	mV	OUC-VOL-PRIO1-010
$RL_{DD11, OP}$	Output differential mode Return Loss	100 MHz to 10.3 GHz		18		dB	OUC-DB-PRIO2-011
$RL_{CC11, OP}$	Output common mode Return Loss	100 MHz to 10.3 GHz		12		dB	OUC-DB-PRIO2-012

10.4 AUX snooping monitor characteristics

Table 18. AUX monitor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_I	Bias Voltage at the pin	AUXP/AUXN pins	0		3.6	V	AUX-VOL-PRIO1-001
r_{AUX}	AUX bit rate			1		Mbps	AUX-FRQ-PRIO2-002
$V_{AUX\text{-}AC\text{-}DIFF\text{-}pp}$	AUX AC differential peak-to-peak	AUXP/AUXN pins	0.27		1.38	V_{ppd}	AUX-VOL-PRIO1-003
I_{IL}	Leakage current at the pin	Pin voltage 3.6 V			+19	µA	AUX-CUR-PRIO1-004
I_{bck}	Back current sunk from pin to powered down supply	V_{DD} =0, Pin voltage = 3.6 V			+27	µA	AUX-CUR-PRIO1-005
Z_{in}	AUX monitor differential input impedance	Over frequency range of interest DC to 50 MHz		1		MΩ	AUX-RES-PRIO2-006
C_{Aux}	AUX AC coupling capacitance		75		200	nF	AUX-CAP-PRIO1-007

All S-parameter measurements are with respect to 100Ω differential impedance reference and 50Ω single-ended impedance reference.

10.5 Control characteristics for AUTO_ORIENT_EN pin

Table 19. Binary control input characteristics (external system voltage V_{SYS} = 1.7 V to 3.6 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{IH}	High level voltage		0.7*V_{DD}		V_{SYS}	V	BIN-VOL-PRIO1-001
V_{IL}	Low level voltage				0.3*V_{DD}	V	BIN-VOL-PRIO1-002
I_{IL}	Leakage current at the pin	V_{DD} = 1.8 V, pin voltage = 3.6 V			+14	µA	BIN-CUR-PRIO1-003
		V_{DD} = 1.8 V, pin voltage = 1.8 V			+1.5	µA	BIN-CUR-PRIO1-004
I_{bck}	Back current sunk from pin to powered down supply	V_{DD} = 0, V_{SYS} = 3.6 V			+24	µA	BIN-CUR-PRIO1-005
C_{pin}	Maximum allowed capacitance at the pin				10	pF	BIN-CAP-PRIO1-006

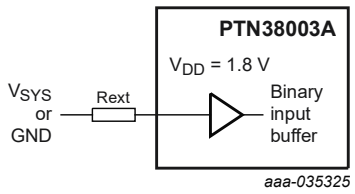


Figure 14. Binary input buffer setting

10.6 Ternary control characteristics for LCTL[1, 2, 3] and RCTL[1, 2, 3] pins

Table 20. Ternary control input characteristics (external system voltage V_{SYS}= 1.7 V to 3.6 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{IH}	High level voltage	External pull-up 1kΩ resistor to V_{SYS}	0.8*V_{DD}		V_{SYS}	V	TER-VOL-PRIO1-001
V_{IM}	Unconnected or open condition		0.35*V_{DD}		0.45*V_{DD}	V	TER-VOL-PRIO1-002
V_{IL}	Low level voltage	External pull-down 1kΩ resistor to GND			0.15*V_{DD}	V	TER-VOL-PRIO1-003
I_{IL}	Leakage current when pin is not active	VDD = 1.8 V, pull-up resistor connected to V_{SYS} = 3.6 V			15	µA	TER-CUR-PRIO1-004
		VDD = 1.8 V, pull-up resistor connected to V_{SYS} = 1.8 V			1	µA	TER-CUR-PRIO1-005
	Leakage current when pin is active	VDD = 1.8 V, pull-up resistor connected to V_{SYS} = 3.6 V			80	µA	TER-CUR-PRIO1-006
		VDD = 1.8 V, pull-up resistor connected to V_{SYS} = 1.8 V	-25		35	µA	TER-CUR-PRIO1-007
I_{bck}	Back current sunk from pin to powered down supply	V_{DD} = 0, V_{SYS} = 3.6 V			20	µA	TER-CUR-PRIO1-008
R_{pu}	Internal pull-up resistance			120		kΩ	TER-RES-PRIO2-009
R_{pd}	Internal pull-down resistance			80		kΩ	TER-RES-PRIO2-010
C_{pin}	Maximum allowed capacitance at the pin				10	pF	TER-CAP-PRIO1-011

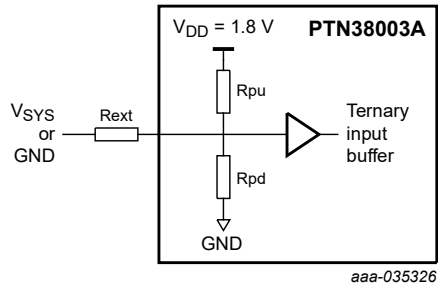


Figure 15. Ternary input buffer setting

10.7 Quaternary control characteristics for ADDR pin

Table 21. Ternary control input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
V_{IH1}	High level voltage	Pin connected to V_{DD}	0.9*V_{DD}		V_{DD}+0.3	V	QAT-VOL-PRIO1-001
V_{IH2}	High level voltage	R_{ext} = 56 kΩ (10 % resistor) pull-up to V_{DD}	0.575*V_{DD}		0.725*V_{DD}	V	QAT-VOL-PRIO1-002
V_{IM}	Voltage at unconnected/ open condition	R_{ext} = 200 kΩ (10 % resistor) pull-up to V_{DD}	0.275*V_{DD}		0.425*V_{DD}	V	QAT-VOL-PRIO1-003
V_{IL}	Low level voltage	Pin connected to GND			0.1*V_{DD}	V	QAT-VOL-PRIO1-004
I_{IL}	Leakage current at the pin	Pin voltage = 3.6 V			20	µA	QAT-CUR-PRIO1-005
I_{bck}	Back current sunk from pin to powered down supply	V_{DD} = 0; Pin voltage = 3.6 V			20	µA	QAT-CUR-PRIO1-006
R_{pd}	Internal pull-down resistance			105		kΩ	QAT-RES-PRIO2-007
C_{pin}	Maximum allowed capacitance at the pin				10	pF	QAT-CAP-PRIO1-008

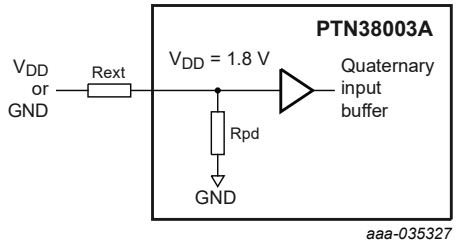


Figure 16. Quaternary input buffer setting

10.8 I^2C AC/DC characteristics

Table 22. I^2C interface- AC/DC characteristics for SCL and SDA pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
F_{I2C}	I^2C Clock frequency		0		1000	kHz	SER-FRQ-PRIO1-001
V_{IH}	HIGH-level Input voltage		1.19		3.6	V	SER-VOL-PRIO1-002
V_{IL}	LOW-level Input voltage				0.57	V	SER-VOL-PRIO1-003
V_{hys}	Hysteresis of Schmitt trigger inputs	V_{pullup} < 3.6 V	0.095			V	SER-VOL-PRIO1-004
V_{OL}	LOW-level output voltage at 2 mA sink current	V_{pullup} < 3.6 V	0		0.4	V	SER-VOL-PRIO1-005
I_{OL}	LOW-level output current	VOL = 0.4 V; Standard and Fast modes	3			mA	SER-CUR-PRIO1-006
		VOL = 0.4 V; Fast mode plus	20			mA	SER-CUR-PRIO1-007
		VOL = 0.6 V; Fast mode	6			mA	SER-CUR-PRIO1-008
I_{IL}	LOW-level input current	Pin voltage - 0.1* V_{pullup} to 0.9*$V_{pullup, max}$	-10		10	µA	SER-CUR-PRIO1-009
C_I	Capacitance of I/O pin				10	pF	SER-CAP-PRIO1-010
$t_{HD,STA}$	Hold time (repeated) START condition	Fast mode plus; After this period, the first clock pulse is generated	0.26			µs	SER-TIM-PRIO1-011
t_{LOW}	LOW period of I^2C clock	Fast mode plus	0.5			µs	SER-TIM-PRIO1-012
t_{HIGH}	HIGH period of I^2C clock	Fast mode plus	0.26			µs	SER-TIM-PRIO1-013
$T_{SU,STA}$	Setup time (repeated) START condition	Fast mode plus	0.26			µs	SER-TIM-PRIO1-014
$T_{HD,DAT}$	Data Hold time	Fast mode plus	0			µs	SER-TIM-PRIO1-015
$T_{SU,DAT}$	Data Setup time	Fast mode plus	50			ns	SER-TIM-PRIO1-016
T_r	Rise time of I^2C_SCL and I^2C_SDA signals	Fast mode plus	-		120	ns	SER-TIM-PRIO1-017
T_f	Fall time of I^2C_SCL and I^2C_SDA signals	Fast mode plus	-		120	ns	SER-TIM-PRIO1-018
$T_{SU,STO}$	Setup time for STOP condition	Fast mode plus	0.26			µs	SER-TIM-PRIO1-019
t_{BUF}	Bus free time between STOP and START condition	Fast mode plus	0.5			µs	SER-TIM-PRIO1-020
$t_{VD,DAT}$	Data valid time	Fast mode plus			0.45	µs	SER-TIM-PRIO1-021

Table 22. I^2C interface- AC/DC characteristics for SCL and SDA pins*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Unique Identifier
$t_{VD,ACK}$	Data valid acknowledge time	Fast mode plus			0.45	µs	SER-TIM-PRIO1-022
t_{SP}	Pulse width of spikes that must be suppressed by input filter		0		50	ns	SER-TIM-PRIO1-023

Note: V_{pullup} is external pull-up voltage on SCL and SDA pins. The voltage can be up to 3.3 V from another power supply.

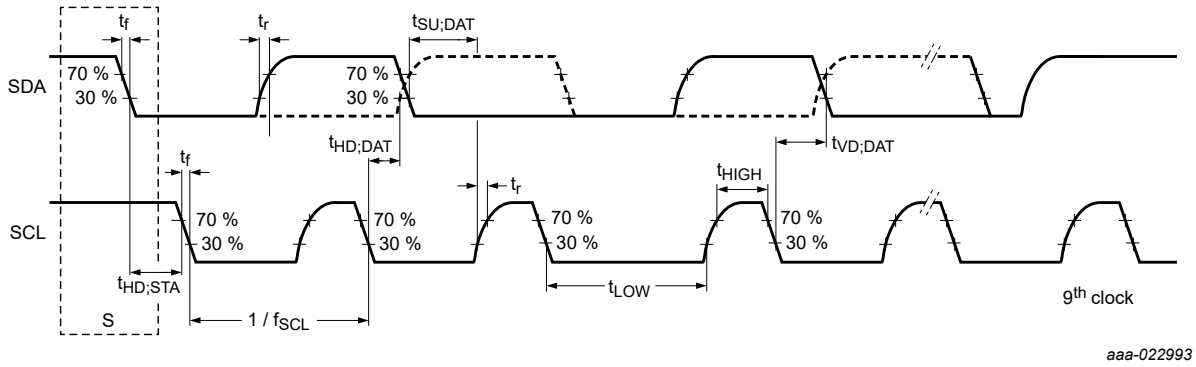


Figure 17. I^2C-bus timing diagram

11 Package outline

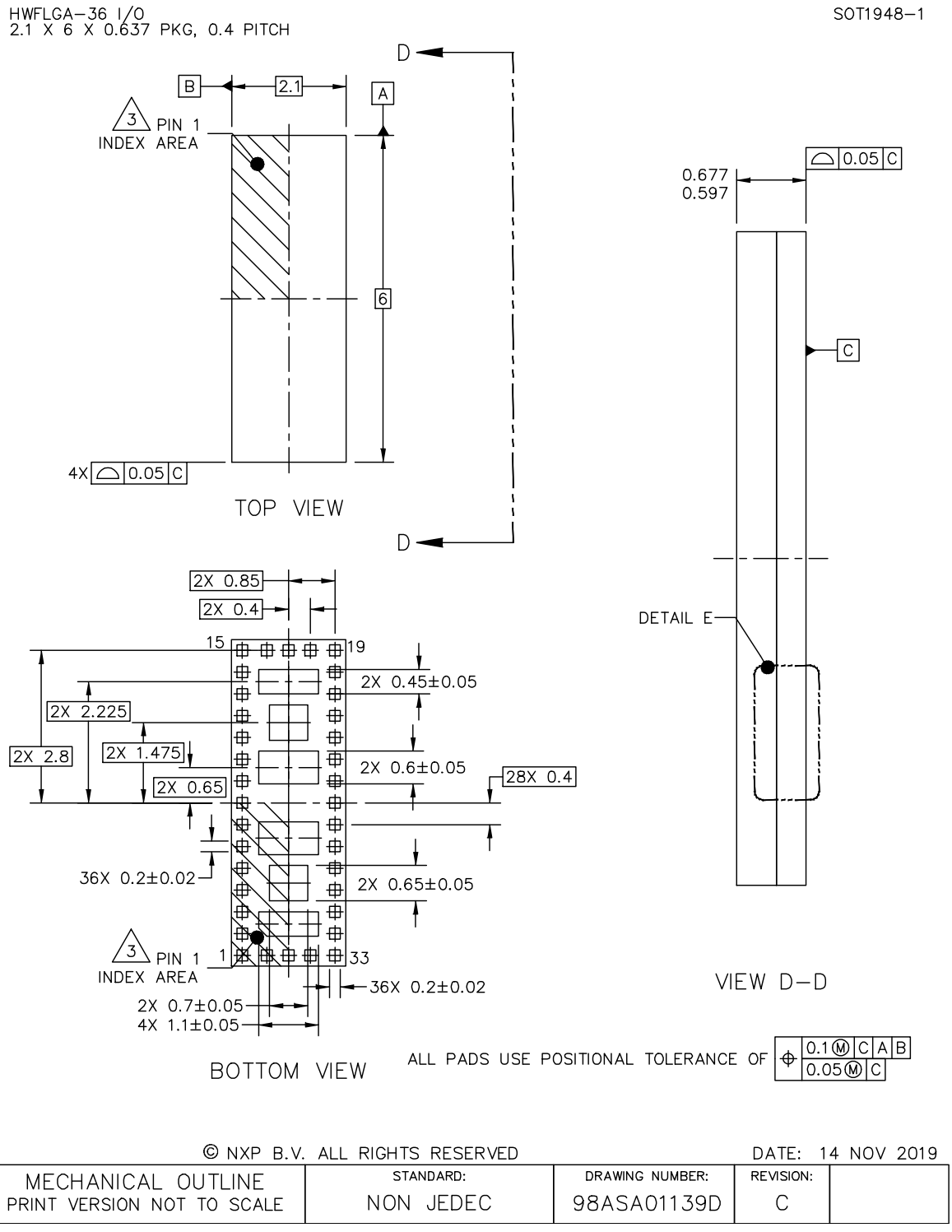


Figure 18. Package outline SOT1948-1

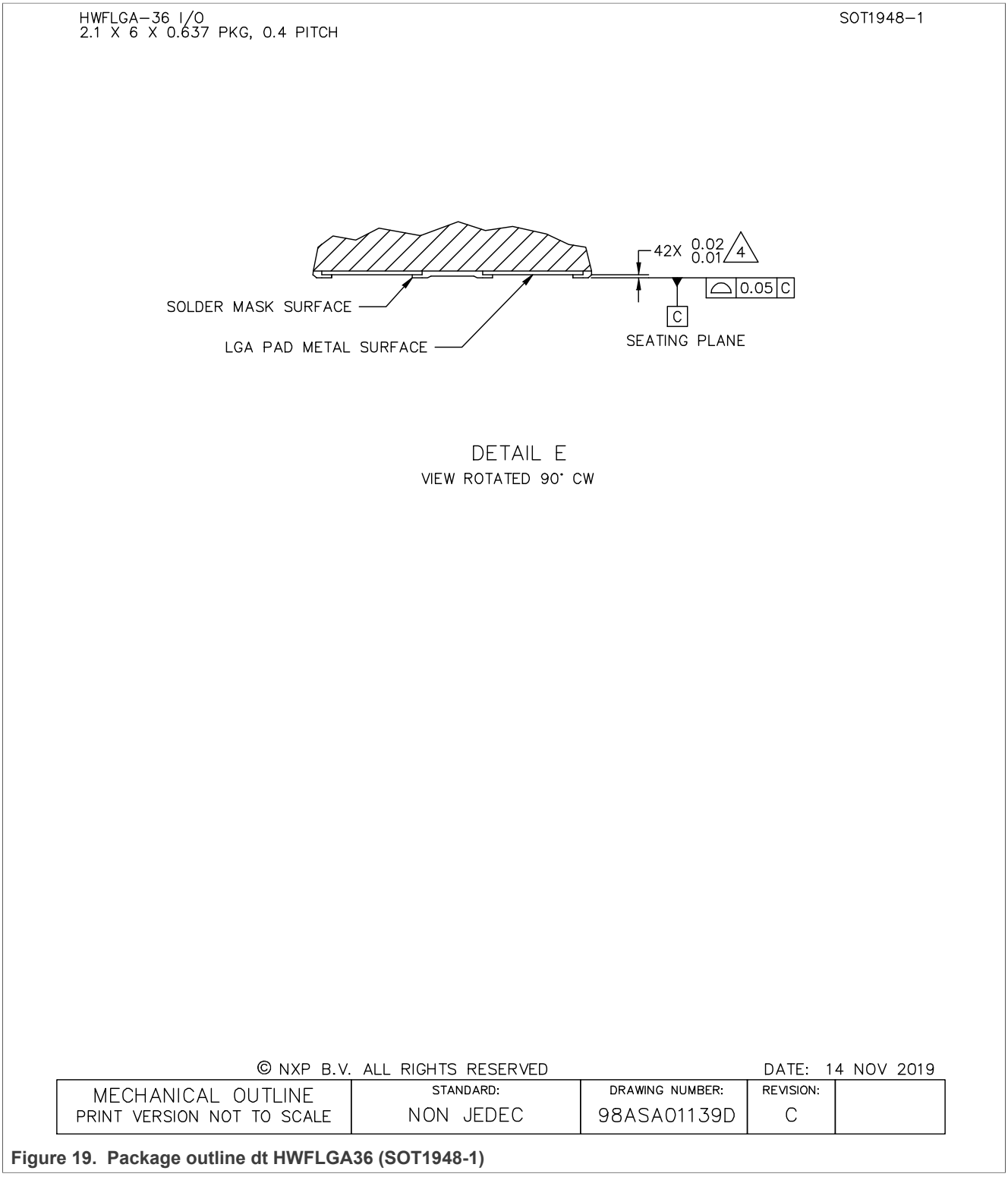


Figure 19. Package outline dt HWFLGA36 (SOT1948-1)

Figure 20. Package outline note HWFLGA36 (SOT1948-1)

12 Packing information

12.1 SOT1948-1; HWFLGA36; reel dry pack, SMD, 13" Q1 standard product orientation ordering code (12NC) ending 019

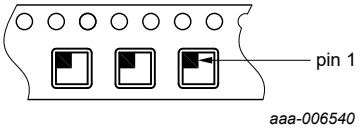
12.1.1 Dimensions and quantities

Table 23. Dimensions and quantities

Reel dimensions d × w (mm)[1]	SPQ/PQ (pcs)[2]	Reels per box
330 × 12	7000	1

[1] d = reel diameter; w = tape width.
[2] Packing quantity dependent on specific product type. View ordering and availability details at NXP order portal, or contact your local NXP representative.

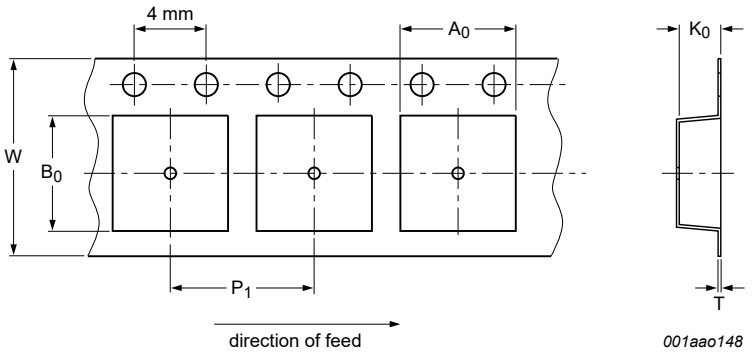
12.1.2 Product orientation



Pin 1 is in quadrant 1.

Figure 21. Product orientation in carrier tape

12.1.3 Carrier tape dimensions



Not drawn to scale.

Figure 22. Carrier tape dimensions

Table 24. Carrier tape dimensions

In accordance with IEC 60286-3/EIA-481.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
2.30 ± 0.05	6.30 ± 0.05	0.85 +.1/-.05	0.30 ± 0.05	8 ± 0.1	12 +0.3/-0.1

13 Soldering

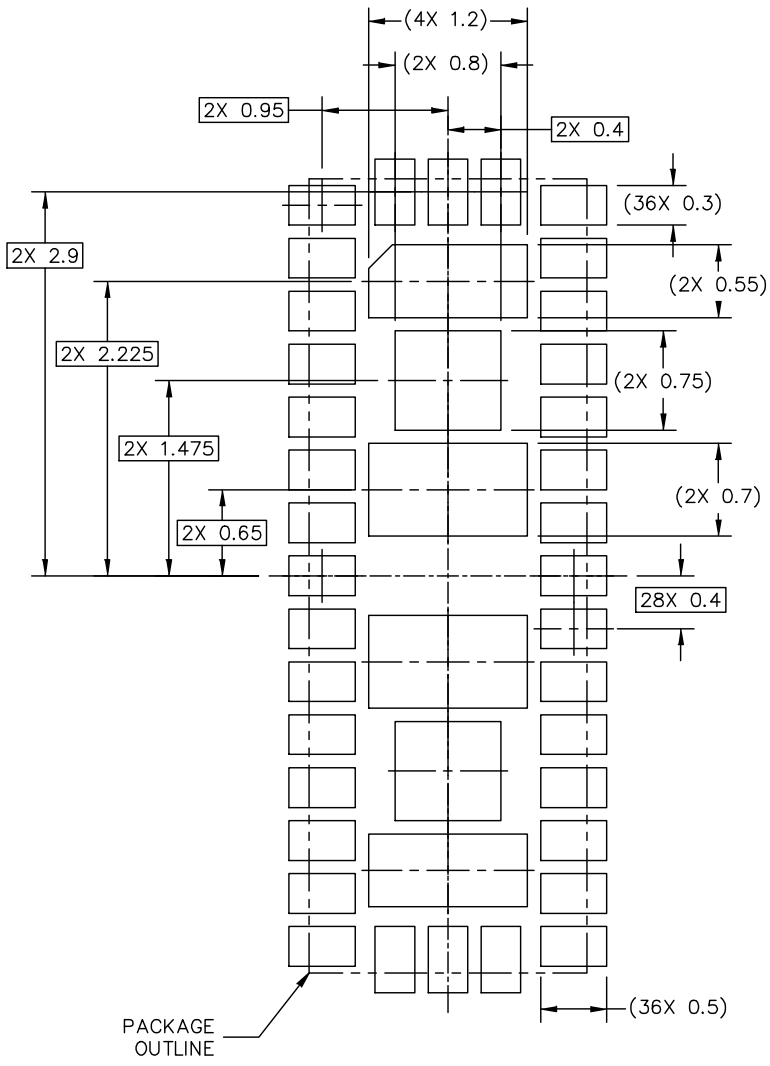


Figure 23. Reflow soldering footprint for SOT1948-1

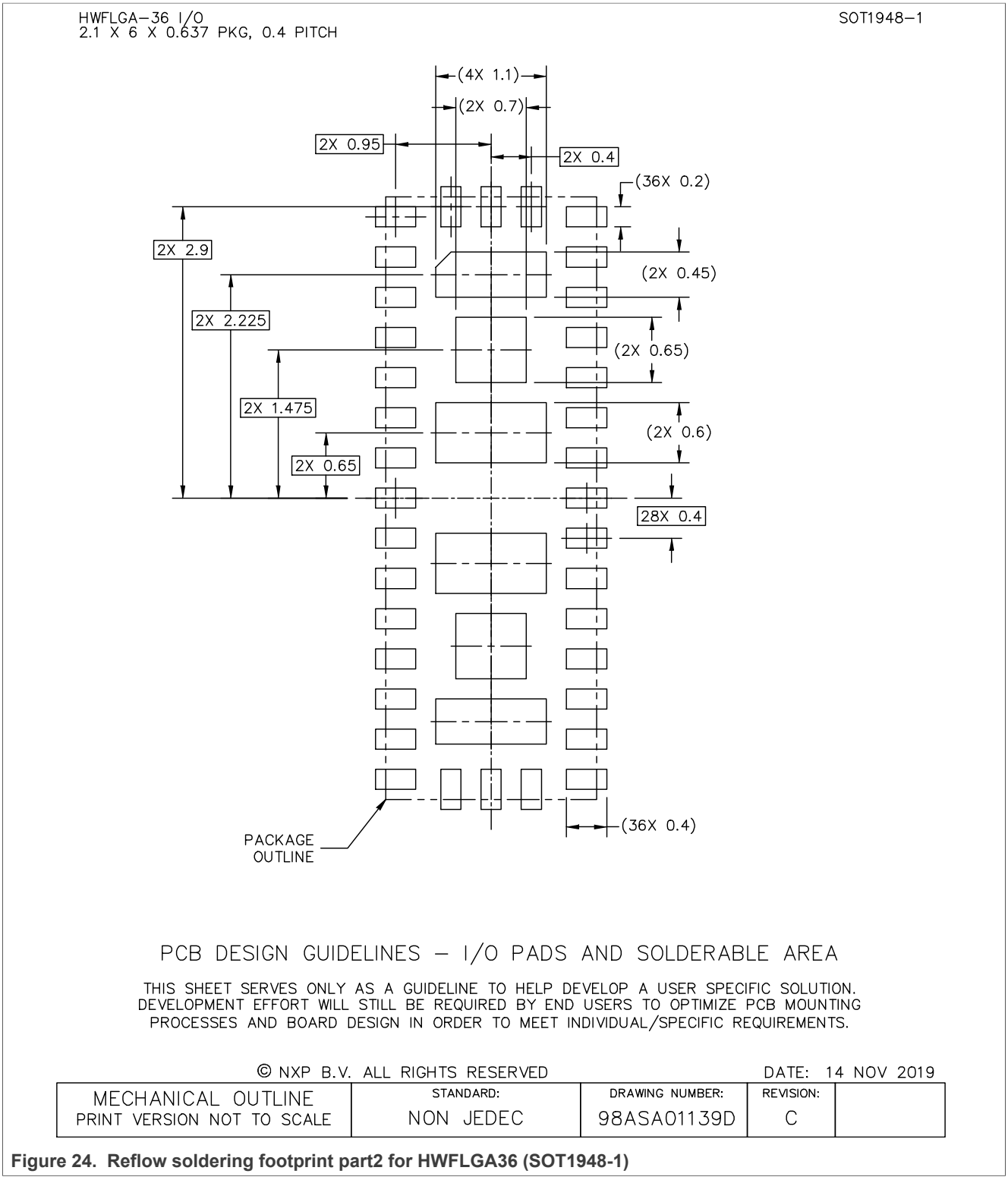


Figure 24. Reflow soldering footprint part2 for HWFLGA36 (SOT1948-1)

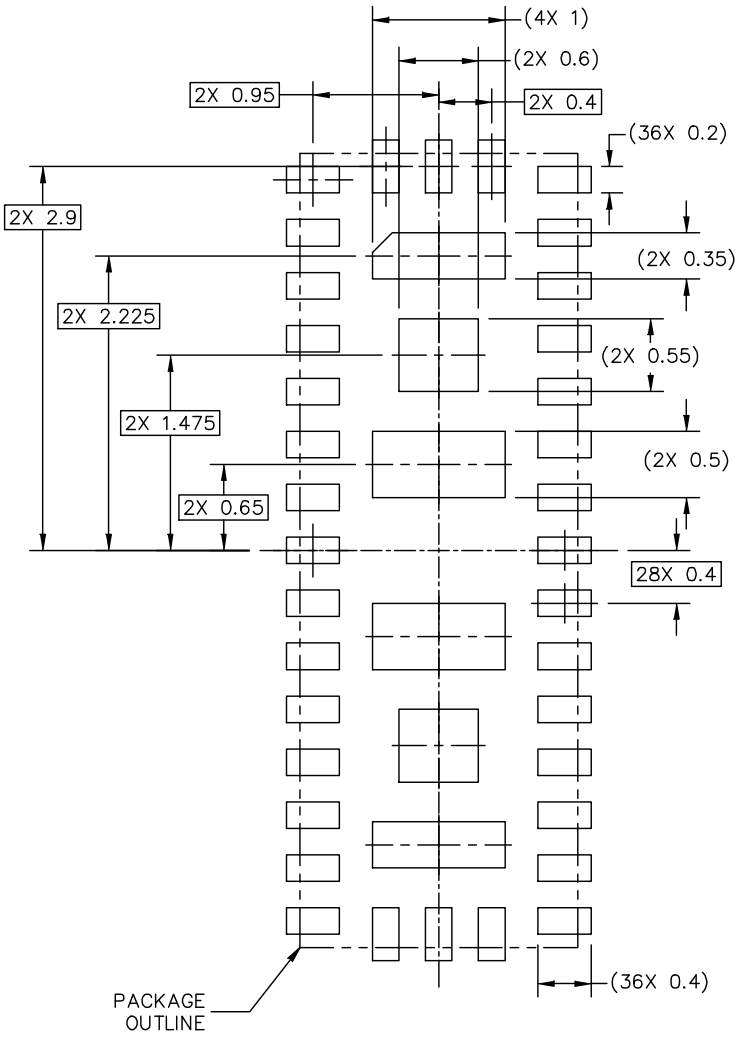


Figure 25. Reflow soldering footprint part3 for HWFLGA36 (SOT1948-1)

14 Abbreviations

Table 25. Abbreviations

Acronym	Description
CDM	Charged Device Model
USB4	Converged IO specification (aka USB4)
DFP	Downstream Facing Port
DP	DisplayPort
Gbps	Gigabits per second
HBM	Human Body Model
LBPM	LFPS Based PWM Message
LFPS	Low Frequency Periodic Signaling
LPM	Link Power Management
NC	No Connect
Rx	Receiver
SI	Signal Integrity
TX	Transmitter
UFP	Upstream Facing Port
USB	Universal Serial Bus

15 References

[1] USB3.2 Specification, Revision 1.0, Sep 22, 2017

[2] VESA DisplayPort v1.4a, Apr 19, 2018 (with the addition of additional data rates - 10/13.5/20 Gbps from DisplayPort v2.0 specification

[3] UM10204, "I^2C-bus specification and user manual"; NXP Semiconductors, Rev 6, April 4, 2014

16 Revision history

Table 26. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
PTN38003A v2.1	20211208	Product data sheet	-	-
Modifications:	• Section 7.7.6: Corrected description for 0x0F bits [5:4] and [1:0]			
PTN38003A v2.0	20211022	Product data sheet	202110005I	-
Modifications:	• Changed "DP1.4" to "DisplayPort" throughout • Updated with DP2.0 link rates • Table 8, Table 9: Added 6.75 GHz and 10 GHz data for UHBR20			
PTN38003A v1.0	20210607	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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