SA58672

3.0 W mono class-D audio amplifier

Rev. 04 — 8 June 2009 **Product data sheet**

1. General description

The SA58672 is a mono, filter-free class-D audio amplifier which is available in a 9 bump WLCSP (Wafer Level Chip-Size Package) and 10-terminal HVSON packages.

The SA58672 features shutdown control. Improved immunity to noise and RF rectification is increased by high PSRR and differential circuit topology. Fast start-up time and very small WLCSP package makes it an ideal choice for both cellular handsets and PDAs.

The SA58672 delivers 1.7 W at 5 V and 800 mW at 3.6 V into 8 Ω. It delivers 3.0 W at 5 V and 1.6 W at 3.6 V into 4 Ω. The maximum power efficiency is excellent at 90 % into 8 Ω and 84 % to 88 % into 4 Ω. The SA58672 provides thermal and short-circuit shutdown protection.

2. Features

- Output power
  - 3.0 W into 4 Ω at 5 V
  - 1.6 W into 4 Ω at 3.6 V
  - 1.7 W into 8 Ω at 5 V
  - 800 mW into 8 Ω at 3.6 V
- Power supply range: 2.0 V to 5.5 V
- Shutdown control
- High SVRR: –77 dB at 217 Hz
- Fast start-up time: 7.0 ms
- Low supply current
- Low shutdown current
- Short-circuit and thermal protection
- Space savings with 1.66 mm × 1.71 mm × 0.6 mm 9 bump WLCSP package
- Low junction to ambient thermal resistance of 100 K/W with adequate heat sinking of WLCSP
- Enhanced power dissipation with 3.0 mm × 3.0 mm × 0.85 mm HVSON10 package

3. Applications

- Wireless and cellular handsets and PDAs
- Portable DVD player
- USB speakers
- Notebook PC
- Portable radio and gaming
- Educational toys

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SA58672TK	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 × 3 × 0.85 mm	SOT650-1
SA58672UK	WLCSP9	wafer level chip-size package; 9 bumps; 1.66 × 1.71 × 0.6 mm	SA58672UK

5. Block diagram

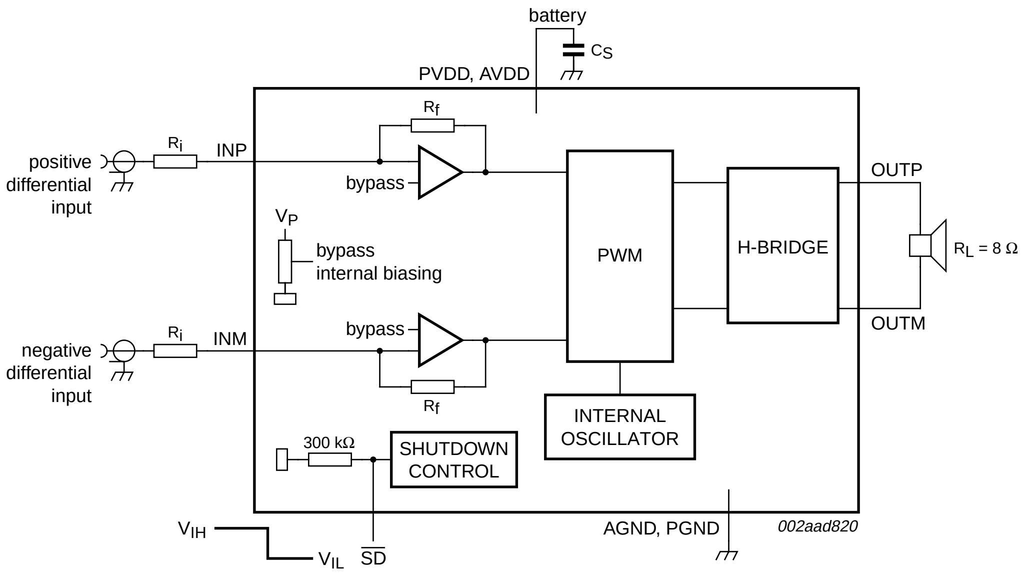
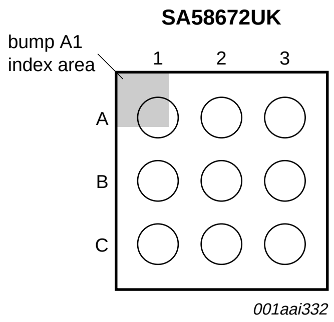


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration for WLCSP9

	1	2	3
A	INP	AGND	OUTM
B	AVDD	PVDD	PGND
C	INM	$\overline{SD}$	OUTP

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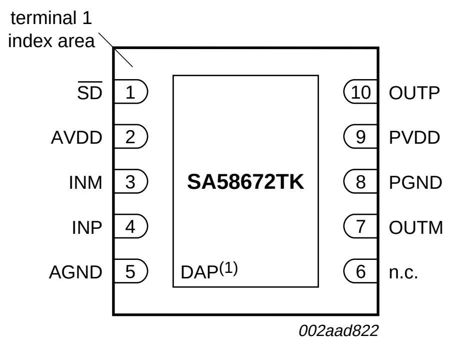
Transparent top view

Fig 3. Ball mapping for WLCSP9



Transparent top view

(1) Exposed Die Attach Paddle (DAP).

Fig 4. Pin configuration for HVSON10

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	WLCSP9	HVSON10	
INP	A1	4	channel positive input
AVDD	B1	2	analog supply voltage (level same as PVDD)
INM	C1	3	channel negative input
AGND	A2	5	analog ground
PVDD	B2	9	power supply voltage (level same as AVDD)
$\overline{SD}$	C2	1	channel shutdown input (active LOW)
OUTM	A3	7	channel negative output
PGND	B3	8	power ground
OUTP	C3	10	channel positive output
n.c.	-	6	not connected
DAP	-	(DAP)	exposed die attach paddle; connect to ground plane heat spreader

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	Active mode	–0.3	+6.0	V
		Shutdown mode	–0.3	+7.0	V
V_I	input voltage	pin $\overline{SD}$	GND	V_{DD}	V
		other pins	–0.3	V_{DD} + 0.3	V
P	power dissipation	WLCSP9; derating factor 10 mW/K			
		T_{amb} = 25 °C	-	1250	mW
		T_{amb} = 75 °C	-	750	mW
		T_{amb} = 85 °C	-	650	mW
		HVSON10; derating factor 25 mW/K			
		T_{amb} = 25 °C	-	3.12	W
		T_{amb} = 75 °C	-	1.87	W
		T_{amb} = 85 °C	-	1.62	W
T_{amb}	ambient temperature	operating in free air	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C
T_{stg}	storage temperature		–65	+150	°C
V_{ESD}	electrostatic discharge voltage	human body model	±2500	-	V
		machine model	±100	-	V
		charged-device model	±750	-	V

8. Static characteristics

Table 4. Static characteristics

T_{amb} = 25 °C, unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		2.0	-	5.5	V
$\|V_{O(offset)}\|$	output offset voltage	measured differentially; inputs AC grounded; G_v = 6 dB; V_{DD} = 2.0 V to 5.5 V	-	5	25	mV
PSRR	power supply rejection ratio	V_{DD} = 2.0 V to 5.5 V	-	–93	–70	dB
$V_{i(cm)}$	common-mode input voltage	V_{DD} = 2.0 V to 5.5 V	0.5	-	V_{DD} – 0.8	V
CMRR	common mode rejection ratio	inputs are shorted together; V_{DD} = 2.0 V to 5.5 V	-	–69	–50	dB
I_{IH}	HIGH-level input current	V_{DD} = 5.5 V; V_I = V_{DD}	-	-	50	μA
I_{IL}	LOW-level input current	V_{DD} = 5.5 V; V_I = 0 V	-	-	5	μA
I_{DD}	supply current	V_{DD} = 5.5 V; no load	-	3.4	4.2	mA
		V_{DD} = 5.0 V; no load		3.2	4.0	mA
		V_{DD} = 3.6 V; no load	-	2.6	3.4	mA
		V_{DD} = 2.5 V; no load	-	2.2	3.0	mA
$I_{DD(sd)}$	shutdown mode supply current	no input signal; V_{SD} = GND	-	10	1000	nA
V_{SD}	voltage on pin $\overline{SD}$	device ON	1.3	-	V_{DD}	V
		device OFF	GND	-	0.35	V
Z_i	input impedance	V_{DD} = 2.0 V to 5.5 V	260	300	340	kΩ
R_{DSon}	drain-source on-state resistance	static; V_{DD} = 5.5 V	-	430	-	mΩ
		static; V_{DD} = 3.6 V	-	475	-	mΩ
		static; V_{DD} = 2.5 V	-	550	-	mΩ
$Z_{o(sd)}$	shutdown mode output impedance	V_{SD} = 0.35 V	-	2	-	kΩ
f_{sw}	switching frequency	V_{DD} = 2.5 V to 5.5 V	250	300	350	kHz
$G_{v(cl)}$	closed-loop voltage gain	V_{DD} = 2.0 V to 5.5 V; R_i in kΩ	260 kΩ / R_i	300 kΩ / R_i	340 kΩ / R_i	V/V

[1] V_{DD} is the supply voltage on pin PVDD and pin AVDD.
GND is the ground supply voltage on pin PGND and pin AGND.

9. Dynamic characteristics

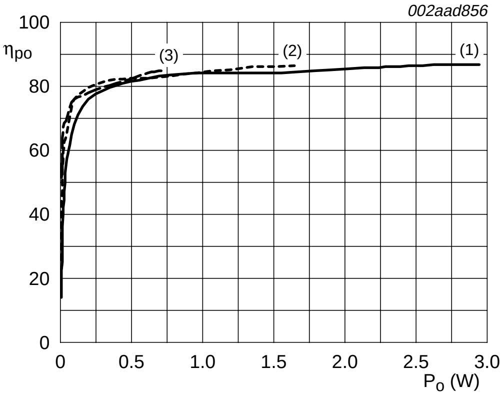
Table 5. Dynamic characteristics

T_{amb} = 25 °C; R_L = 8 Ω; unless otherwise specified[1].

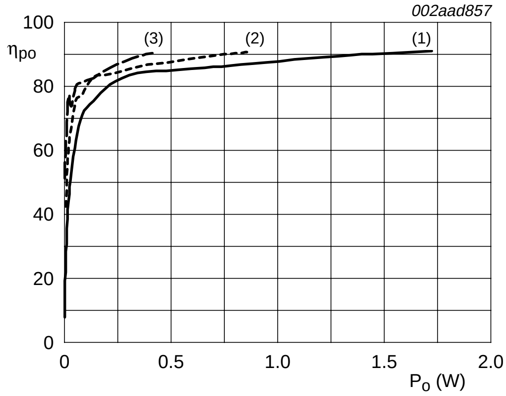
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	output power	f = 1 kHz; THD+N = 10 %				
		R_L = 8 Ω; V_{DD} = 5.0 V	-	1.7	-	W
		R_L = 8 Ω; V_{DD} = 3.6 V	-	800	-	mW
		R_L = 4 Ω; V_{DD} = 5.0 V	-	3.0	-	W
		R_L = 4 Ω; V_{DD} = 3.6 V	-	1.6	-	W
		f = 1 kHz; THD+N = 1 %				
		R_L = 8 Ω; V_{DD} = 5.0 V	-	1.6	-	W
		R_L = 8 Ω; V_{DD} = 3.6 V	-	0.75	-	W
		R_L = 4 Ω; V_{DD} = 5.0 V	-	2.4	-	W
		R_L = 4 Ω; V_{DD} = 3.6 V	-	1.2	-	W
THD+N	total harmonic distortion-plus-noise	V_{DD} = 5 V; G_v = 6 dB; R_L = 8 Ω; f = 1 kHz; P_o = 1 W	-	0.08	-	%
		V_{DD} = 3 V; R_L = 3 Ω; P_o = 1 W	-	3	-	%
η_{po}	output power efficiency	$P_{o(RMS)}$ = 2.0 W; R_L = 4 Ω	-	85	-	%
		$P_{o(RMS)}$ = 1.3 W; R_L = 8 Ω	-	90	-	%
SVRR	supply voltage ripple rejection	G_v = 6 dB; f = 217 Hz				
		V_{DD} = 5.0 V	-	–77	-	dB
		V_{DD} = 3.6 V	-	–73	-	dB
CMRR	common mode rejection ratio	V_{DD} = 5 V; G_v = 6 dB; f = 217 Hz	-	–69	-	dB
$t_{d(sd-startup)}$	delay time from shutdown to start-up	V_{DD} = 3.6 V	-	7.0	-	ms
$V_{n(o)}$	output noise voltage	V_{DD} = 3.6 V; f = 20 Hz to 20 kHz; inputs are AC grounded				
		no weighting	-	35	-	μV
		A weighting	-	27	-	μV

[1] V_{DD} is the supply voltage on pins PVDD and pin AVDD.

10. Typical characterization curves



a. $R_L = 2 \times 15\ \mu H + 4.11\ \Omega$



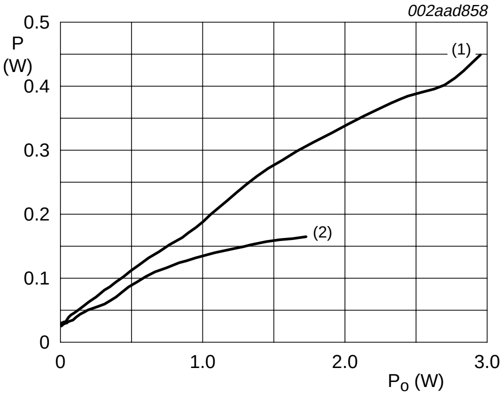
b. $R_L = 2 \times 15\ \mu H + 8.03\ \Omega$

(1) $V_{DD} = 5.0$ V.

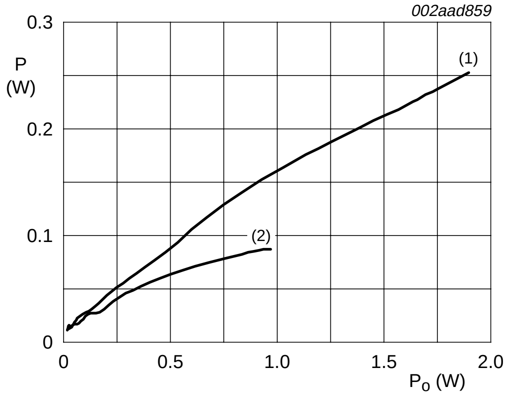
(2) $V_{DD} = 3.6$ V.

(3) $V_{DD} = 2.5$ V.

Fig 5. Output power efficiency as a function of output power



a. $V_{DD} = 5.0$ V

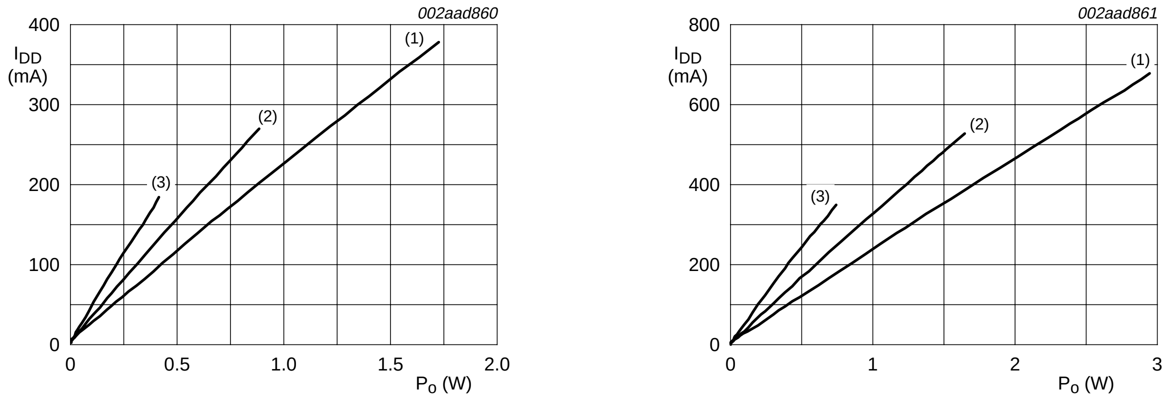


b. $V_{DD} = 3.6$ V

(1) $R_L = 2 \times 15\ \mu H + 4.11\ \Omega$.

(2) $R_L = 2 \times 15\ \mu H + 8.03\ \Omega$.

Fig 6. Power dissipation as a function of output power



a. $R_L = 2 \times 15\ \mu H + 8.03\ \Omega$

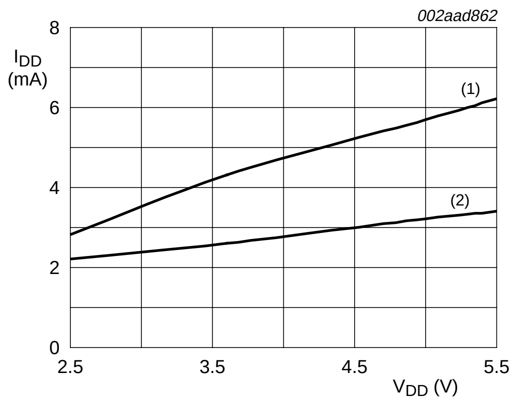
b. $R_L = 2 \times 15\ \mu H + 4.11\ \Omega$

(1) $V_{DD} = 5.0$ V.

(2) $V_{DD} = 3.6$ V.

(3) $V_{DD} = 2.5$ V.

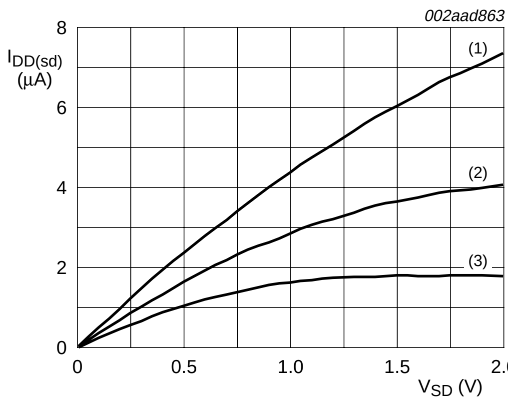
Fig 7. Supply current as a function of output power



(1) With ferrite bead + 1 nF capacitor on outputs; $R_L = 2 \times 15\ \mu H + 8.03\ \Omega$.

(2) Without ferrite beads + 1 nF capacitor on outputs; $R_L = 2 \times 15\ \mu H + 8.03\ \Omega$ or no load.

Fig 8. Supply current as a function of supply voltage

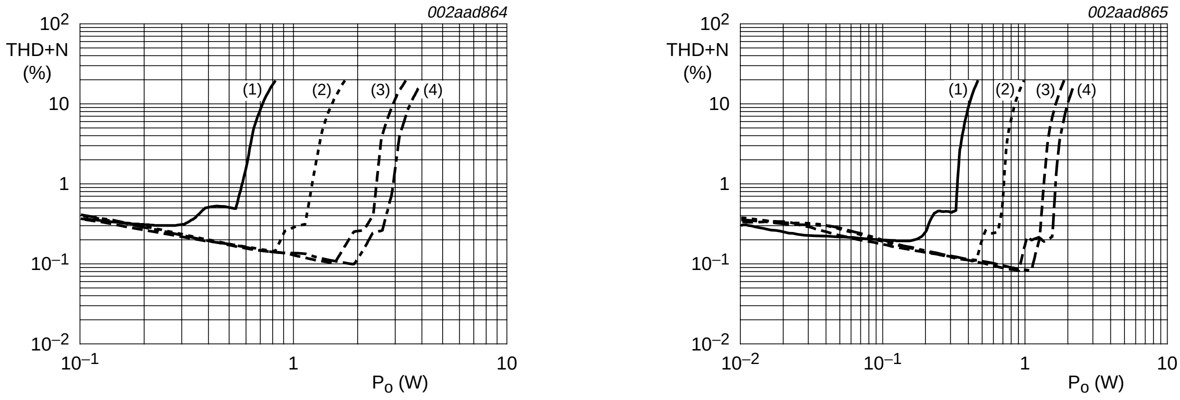


(1) $V_{DD} = 5.0$ V.

(2) $V_{DD} = 3.6$ V.

(3) $V_{DD} = 2.5$ V.

Fig 9. Shutdown mode supply current as a function of shutdown voltage



a. $R_L = 2 \times 15\ \mu H + 4\ \Omega$; A-weighting THD+N filter

b. $R_L = 2 \times 15\ \mu H + 8\ \Omega$; A-weighting THD+N filter

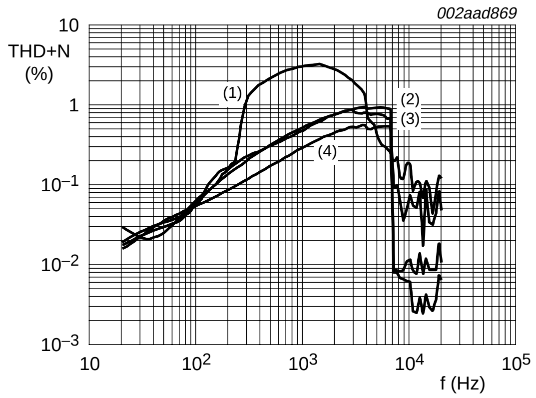
(1) $V_{DD} = 2.5$ V.

(2) $V_{DD} = 3.6$ V.

(3) $V_{DD} = 5.0$ V.

(4) $V_{DD} = 5.5$ V.

Fig 10. Total harmonic distortion-plus-noise as a function of output power



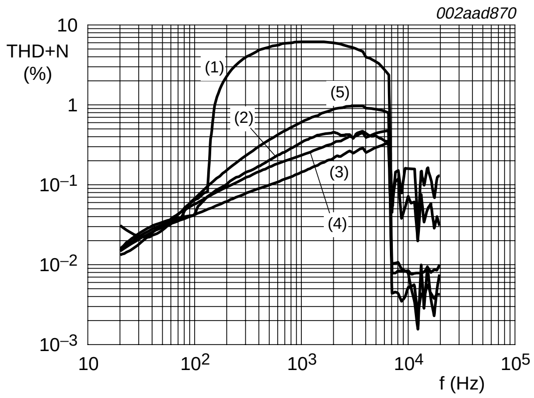
(1) V_O = 4 dBV.

(2) V_O = 3.5 dBV.

(3) V_O = 0 dBV.

(4) V_O = −10 dBV.

a. V_{DD} = 2.5 V



(1) V_O = 8 dBV.

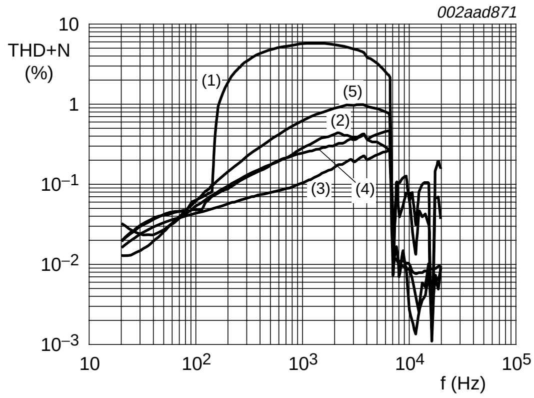
(2) V_O = 7 dBV.

(3) V_O = 5 dBV.

(4) V_O = 0 dBV.

(5) V_O = −10 dBV.

b. V_{DD} = 3.6 V



(1) V_O = 11 dBV.

(2) V_O = 10 dBV.

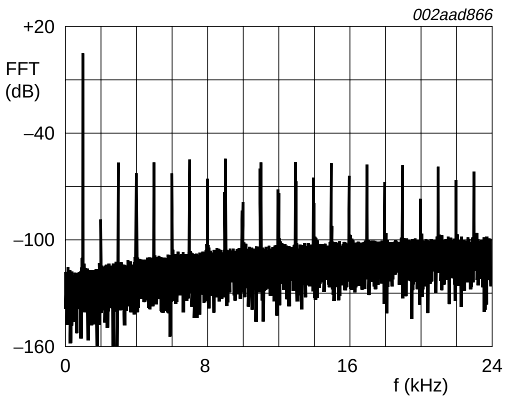
(3) V_O = 8 dBV.

(4) V_O = 0 dBV.

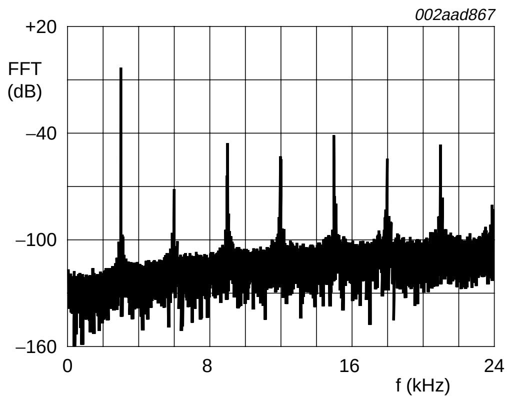
(5) V_O = −10 dBV.

c. V_{DD} = 5.0 V

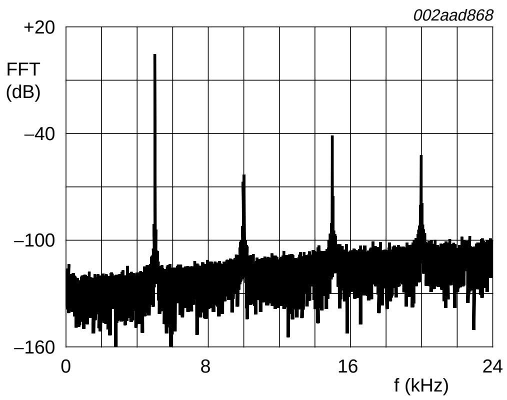
Fig 11. Total harmonic distortion-plus-noise as a function of frequency; $R_L = 2 \times 15\ \mu H + 4\ \Omega$; G_v = 6 dB; A-weighting THD+N filter



a. f_i = 1 kHz

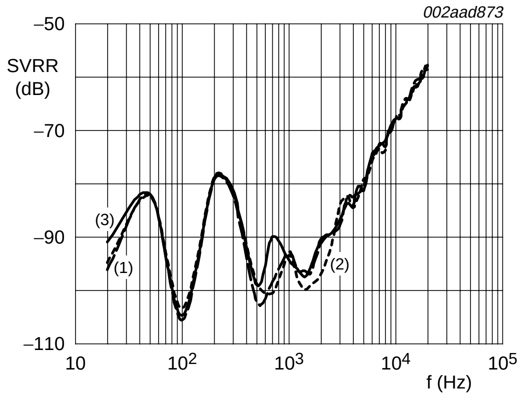


b. f_i = 3 kHz

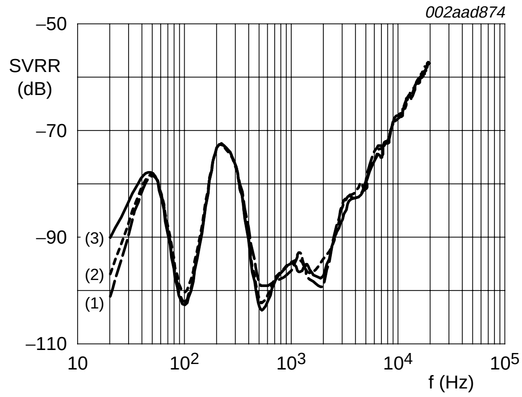


c. f_i = 5 kHz

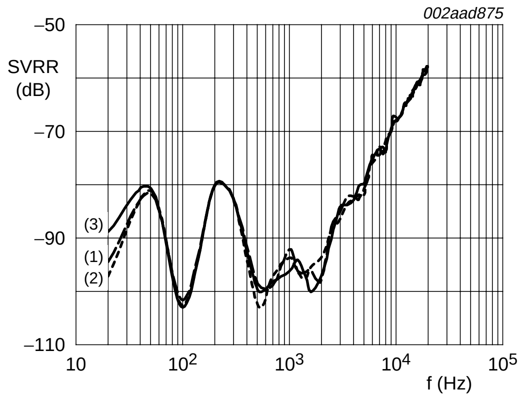
Fig 12. FFT spectrum as a function of frequency; V_{DD} = 3.6 V; V_O = 6 dBV; $R_L = 2 \times 15\ \mu H + 4\ \Omega$



a. R_L = 2 × 15 µH + 4.11 Ω; inputs AC grounded; C_i = 1 µF



b. R_L = 2 × 15 µH + 8.03 Ω; inputs AC grounded; C_i = 1 µF



c. R_L = 2 × 15 µH + 8.03 Ω; inputs floating

(1) V_{DD} = 5.0 V.

(2) V_{DD} = 3.6 V.

(3) V_{DD} = 2.5 V.

Fig 13. Supply voltage ripple rejection as a function of frequency; $G_{v(cl)}$ = 2 V/V

11. Application information

11.1 Power supply decoupling considerations

The SA58672 is a mono class-D audio amplifier that requires proper power supply decoupling to ensure the rated performance for THD+N and power efficiency. To decouple high frequency transients, power supply spikes and digital noise on the power bus line, a low Equivalent Series Resistance (ESR) capacitor, of typically 1 μF is placed as close as possible to the PVDD terminals of the device. It is important to place the decoupling capacitor at the power pins of the device because any resistance or inductance in the PCB trace between the device and the capacitor can cause a loss in efficiency. Additional decoupling using a larger capacitor, 4.7 μF or greater may be done on the power supply connection on the PCB to filter low frequency signals. Usually this is not required due to high PSRR of the device.

11.2 Voltage gain

The SA58672 is comprised of an analog amplifier stage and a comparator stage. The output of the analog amplifier stage is compared with the periodic ramp signal from the sawtooth ramp generator. The resulting output of the comparator is a Pulse Width Modulated (PWM) signal. The final stage is a power NMOS and PMOS H-bridge that converts the PWM into a high power output signal capable of driving low-impedance loads.

The input resistor, R_i sets the gain of the amplifier according to Equation 1:

$$Gain = \frac{2(150\ k\Omega)}{R_i} \tag{1}$$

11.3 Input capacitor selection

The SA58672 does not require input coupling capacitors when used with a differential audio source that is biased from 0.5 V to V_{DD} − 0.8 V. In other words, the input signal must be biased within the common-mode input voltage range. If high-pass filtering is required or if it is driven using a single-ended source, input coupling capacitors are required.

The 3 dB cut-off frequency created by the input coupling capacitor and the input resistors is calculated by Equation 2:

$$f_{-3dB} = \frac{1}{2\pi \times R_i \times C_i} \tag{2}$$

Using an input resistor of 150 kΩ, the gain is set to 2 V/V. At this gain setting, for input capacitor values from 220 nF to 2.2 μF, the 3 dB cut-off frequency may be set between 22 Hz and 220 Hz. Since the values of the input coupling capacitor and the input resistor affects the low frequency performance of the audio amplifier, it is important to consider in the system design. Small speakers in wireless and cellular phones usually do not respond well to low frequency signals. Their low frequency response may be only 600 Hz; typically 1 kHz. Thus, the 3 dB cut-off frequency should be increased to block the low frequency signals to the speakers.

For a required 3 dB cut-off frequency, Equation 3 is used to determine C_i:

$$C_i = \frac{1}{2\pi \times R_i \times f_{-3dB}} \quad (3)$$

The input signal may be DC-coupled, but not using input coupling capacitors may increase the output offset voltage.

11.4 PCB layout considerations

The component location is very important for performance of the SA58672. Place all external components very close to the device. Placing decoupling capacitors directly at the power supply pins increases efficiency because the resistance and inductance in the trace between the device power supply pins and the decoupling capacitor causes a loss in power efficiency.

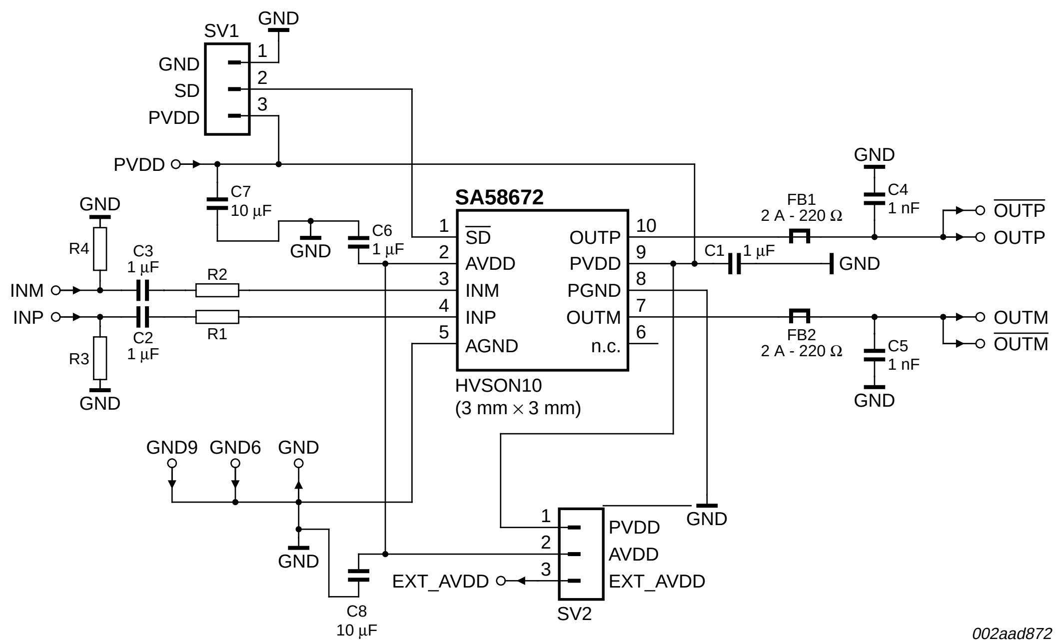
The trace width and routing are also very important for power output and noise considerations.

For high current terminals (PVDD, PGND and audio output), the trace widths should be maximized to ensure proper performance and output power. Use at least 500 μm wide traces.

For the input pins (INP, INM), the traces must be symmetrical and run side-by-side to maximize common-mode cancellation.

11.5 Evaluation demo board

The SA58672 evaluation demo board schematic is shown in Figure 14. An evaluation demo board is available and it may be used for either differential or single-ended (SE) input configuration. A component position on the PCB is provided to AC ground one of the inputs using a 0 Ω chip resistor. When driving SE, the undriven input must be at the same DC level as driven input. If the input is driven from an iPOD or MP3 player, the undriven input is AC grounded; however, if driven from a CODEC, the undriven input is AC decoupled to the same level as the CODEC output. Usually, a V_{ref} is provided on the CODEC.



R3 and R4 are not populated for differential input drive. For single-ended input drive, either R3 or R4 are shorted to ground using a 0 Ω resistor (i.e., one input is AC grounded and the other is driven with the input signal).

Fig 14. SA58672 evaluation demo board schematic

11.6 Filter-free operation and ferrite bead filters

A ferrite bead low-pass filter can be used to reduce radio frequency emissions in applications that have circuits sensitive to greater than 1 MHz. A ferrite bead low-pass filter functions well for amplifiers that must pass FCC unintentional radiation requirements at greater than 30 MHz. Choose a bead with high-impedance at high frequencies and very low-impedance at low frequencies. In order to prevent distortion of the output signal, select a ferrite bead with adequate current rating.

Ferrite bead sources are:

- TDK MPZ1608S221A: 220 Ω at 100 MHz; 3 A peak max current; 0.04 Ω DC resistance.
- KOA CZP2AFTTD221P: 220 Ω at 100 MHz; 2 A peak max current; 0.05 Ω DC resistance.
- Murata BLM21PG221SN1: 220 Ω at 100 MHz; 2 A peak max current; 0.05 Ω DC resistance.

The DC resistance should be as low as possible and the maximum current must exceed at least 1 A. Impedance of 220 Ω at 100 MHz is common spec, but 600 Ω and 1 kΩ ferrite beads may be used. Generally, the current rating decreases with increasing impedance at 100 MHz. However, larger impedance at 100 MHz allows for a smaller, shunt capacitor that will reduce the quiescent load current; this is important for battery operated applications.

For applications in which there are circuits that are EMI sensitive to low frequency (< 1 MHz) and there are long leads from amplifier to speaker, it may be necessary to use an LC output filter.

11.7 Efficiency and thermal considerations

The maximum ambient operating temperature depends on the heat transferring ability of the heat spreader on the PCB layout. In Table 3 "Limiting values", power dissipation, the power derating factor is given as 10 mW/K. The device thermal resistance, $R_{th(j-a)}$ is the reciprocal of the power derating factor. Convert the power derating factor to $R_{th(j-a)}$ by Equation 4:

$$R_{th(j\text{-}a)} = \frac{1}{derating\ factor} = \frac{1}{0.01} = 100\ K/W \quad (4)$$

For a maximum allowable junction temperature, T_j = 150 °C and $R_{th(j-a)}$ = 100 K/W and a maximum device dissipation of 0.84 W (420 mW per channel) and for 1.7 W per channel output power, 4 Ω load, 5 V supply, the maximum ambient temperature is calculated using Equation 5:

$$T_{amb(max)} = T_{j(max)} - (R_{th(j\text{-}a)} \times P_{max}) = 150 - (100 \times 0.84) = 66\ °C \quad (5)$$

The maximum ambient temperature is 66 °C at maximum power dissipation for 5 V supply and 4 Ω load. If the junction temperature of the SA58672 rises above 150 °C, the thermal protection circuitry turns the device off; this prevents damage to the IC. Using speakers greater than 4 Ω further enhances thermal performance and battery lifetime by reducing the output load current and increasing amplifier efficiency.

11.8 Additional thermal information

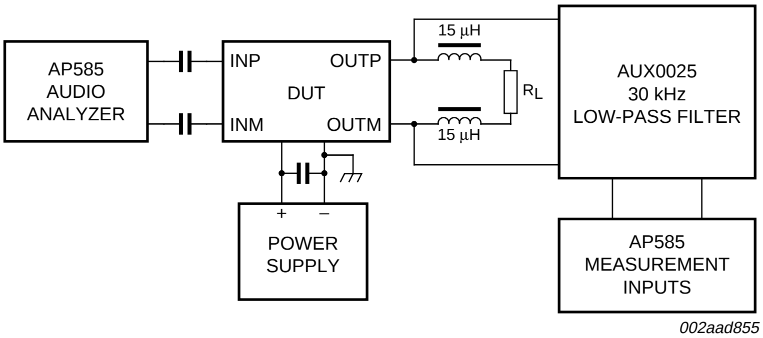
The SA58672 9 bump WLCSP package ground bumps are soldered directly to the PCB heat spreader. By the use of thermal vias, the bumps may be soldered directly to a ground plane or special heat sinking layer designed into the PCB. The thickness and area of the heat spreader may be maximized to optimize heat transfer and achieve lower package thermal resistance.

The SA58672 HVSON10 package has an exposed Die Attach Paddle (DAP), which is soldered directly to the PCB heat spreader to provide enhanced heat transfer and achieve lowest package thermal resistance.

12. Test information

12.1 Test setup for typical characterization curves

The SA58672 demo board shown in Figure 14 and the APA (Audio Precision Analyzer) are used to provide the characterization curves. The test setup diagram in Figure 15 shows the setup details. The output load configuration is comprised of 2 × 15 μH power inductors and precision power load resistor. This passive load emulates a small, low power speaker; it facilitates efficiency measurements. A speaker may be substituted for the passive load to yield similar results.

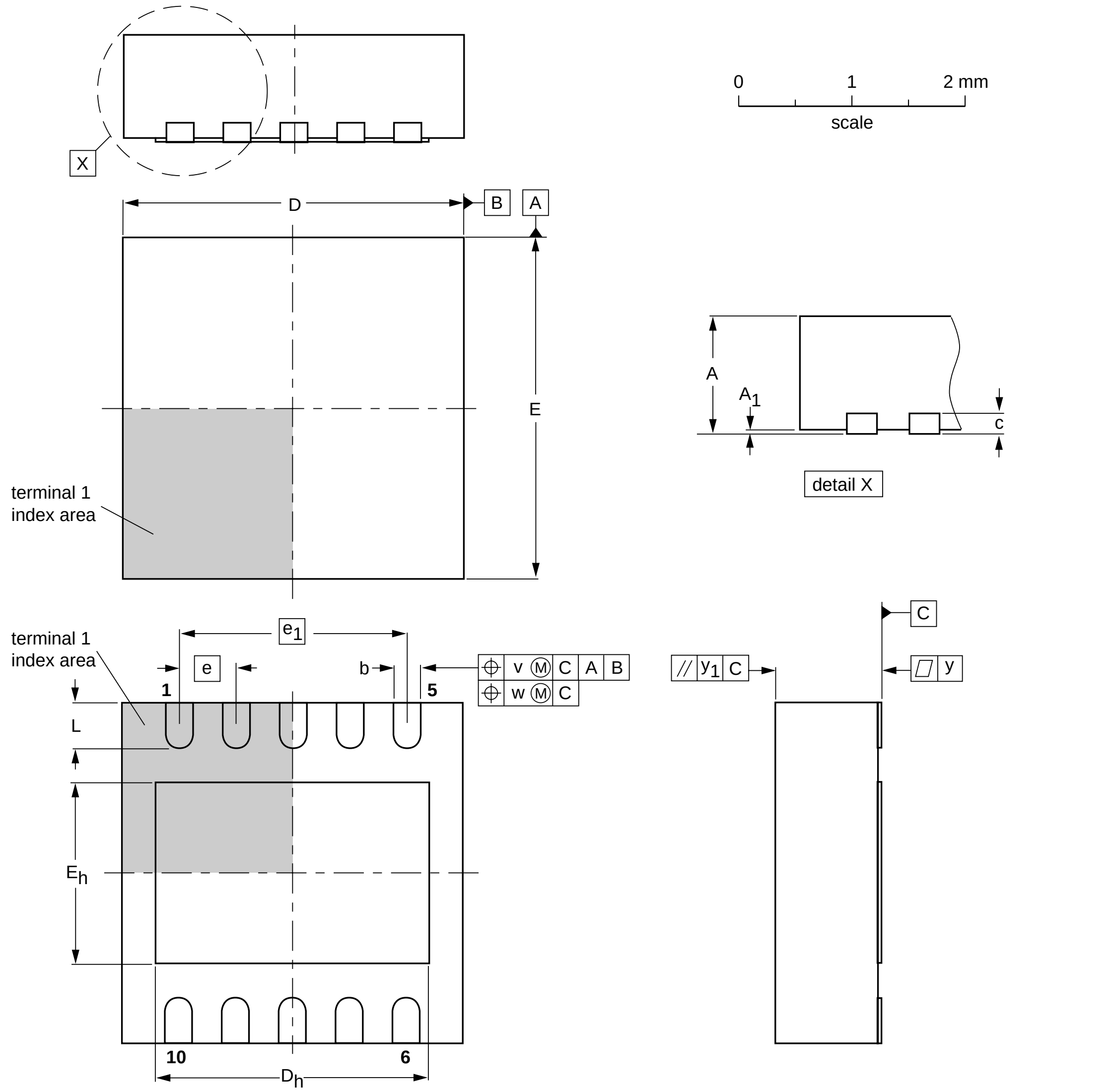


(1) DUT is the SA58672 evaluation demo board.

Fig 15. SA58672 test setup block diagram

13. Package outline

HVSON10: plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 x 3 x 0.85 mm **SOT650-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	2.55 2.15	3.1 2.9	1.75 1.45	0.5	2	0.55 0.30	0.1	0.05	0.05	0.1

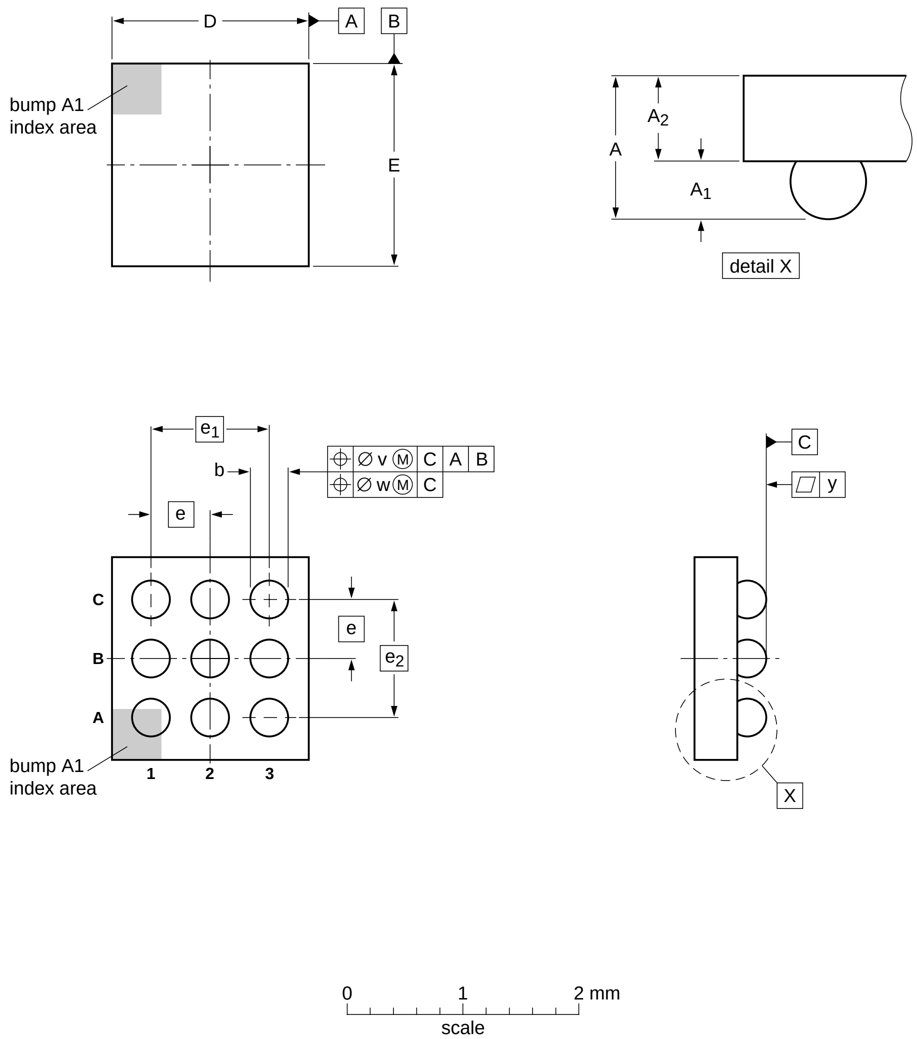
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT650-1	- - -	MO-229	- - -			~~01-01-22~~ 02-02-08

Fig 16. Package outline SOT650-1 (HVSON10)

WLCSP9: wafer level chip-size package; 9 bumps; 1.66 x 1.71 x 0.6 mm **SA58672UK**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	0.64	0.26 0.22	0.38 0.34	0.34 0.30	1.69 1.63	1.74 1.68	0.5	1	1	0.15	0.05	0.08

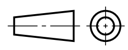
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SA58672UK						08-06-12

Fig 17. Package outline WLCSP9

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 6 and 7

Table 6. SnPb eutectic process (from J-STD-020C)

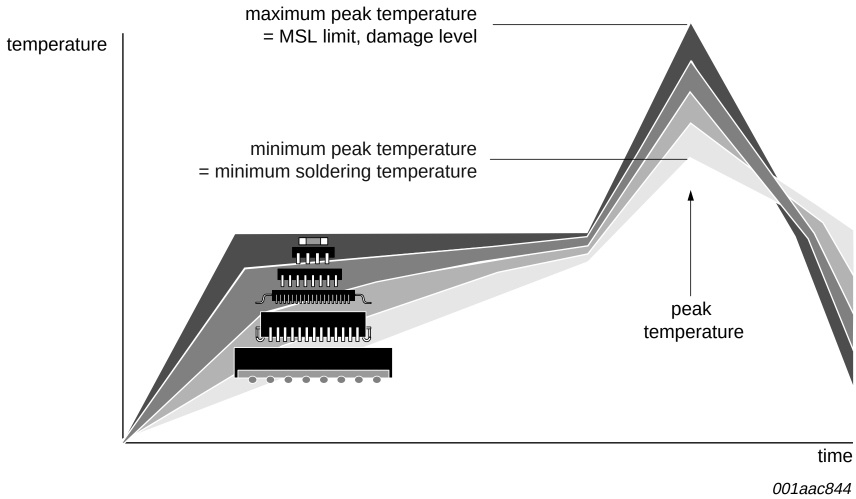
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Soldering of WLCSP packages

15.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 “Wafer Level Chip Scale Package”* and in application note *AN10365 “Surface mount reflow soldering description”*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

15.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a PbSn process, thus reducing the process window

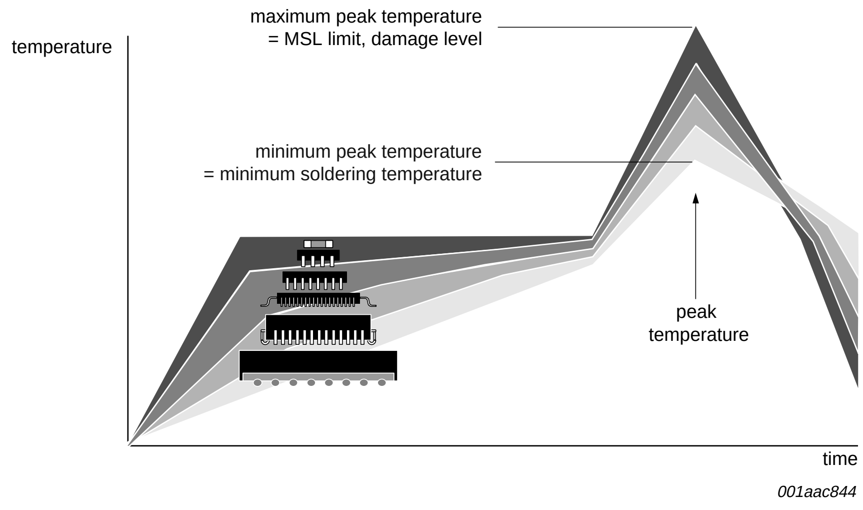
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8.

Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

15.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate

- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

15.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

15.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

15.3.4 Cleaning

Cleaning can be done after reflow soldering.

16. Abbreviations

Table 9. Abbreviations

Acronym	Description
APA	Audio Precision Analyzer
CODEC	compressor-decompressor
DAP	Die Attach Paddle
DUT	Device Under Test
DVD	Digital Video Disc
EMI	ElectroMagnetic Interference
ESR	Equivalent Series Resistance
FCC	Federal Communications Commission
FFT	Fast Fourier Transform
IC	Integrated Circuit

Table 9. Abbreviations *…continued*

Acronym	Description
LC	inductor-capacitor filter
LSB	Least Significant Bit
MP3	MPEG-1 audio layer 3
MSB	Most Significant Bit
PC	Personal Computer
PCB	Printed-Circuit Board
PDA	Personal Digital Assistant
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulator
RF	Radio Frequency
USB	Universal Serial Bus
WLCSP	Wafer Level Chip-Size Package

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA58672_4	20090608	Product data sheet	-	SA58672_3
Modifications:	• Table 3 "Limiting values": – Symbol changed from "V_{esd}" to "V_{ESD}" – V_{ESD} Min value for human body model changed from "±2000 V" to "±2500 V" – V_{ESD} Min value for machine model changed from "±200 V" to "±100 V" – Added V_{ESD} charged-device model specification			
SA58672_3	20090421	Product data sheet	-	SA58672_2
SA58672_2	20090223	Product data sheet	-	SA58672_1
SA58672_1	20080710	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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