# SSL5511T

## Greenchip controller for LED lighting with DIM pin

Rev. 2 — 30 June 2014 Product data sheet

## 1. General description

The SSL5511T is an offline dimmable controller IC, intended to drive dimmable LEDs in general lighting applications, like remote-controlled luminaires and smart lamps.

The main benefits of this IC include:

- Dim level control with either an analog or a digital control input
- Selectable modes for high power factor or low ripple, allowing a wide LED power range
- Large dimming range
- Single stage topology for small PCB footprint
- Ease of design-in
- Integrated start-up JFET
- Low electronic Bill Of Material (BOM)
- Various converter topologies supported

The IC drives an external switch for easy power scaling. It has been designed to start up directly from the High-Voltage (HV) supply by an internal high-voltage current source. Flyback, buck and buck-boost circuit topologies are supported. Primary side sensing provides accurate output current control.

The IC can detect analog signals (according to IEC60929 annex E) or digital control signals and translate them to a continuous LED current in multiple ways. It can operate in three switching modes at two switching frequency ranges. It offers tradeoffs between the output current ripple, the mains current Total Harmonic Distortion (THD) and the application size. The IC incorporates all required protection features.

## 2. Features and benefits

- LED controller IC for driving strings of LEDs or high-voltage LEDs from rectified mains
- High-efficiency switch mode buck, flyback or buck-boost controller driving an external power FET
  - Two maximum switching frequencies for highest efficiency or smallest application size
  - Zero current switching at switch turn-on
  - Zero voltage or valley switching at switch turn-on
  - Selectable low THD or low LED current ripple modes
- Analog IEC60929 input or digital control input for dimming
- Continuous (analog) regulation of LED current in both the dimming control modes
- Dim curve selection based on the control input type
- No binning on LED forward voltage required
- LED current accuracy within ±4 % across variations in components and conditions
- Built-in Protections:
  - UnderVoltage LockOut (UVLO)
  - Leading Edge Blanking (LEB)
  - OverCurrent Protection (OCP)
  - Internal OverTemperature Protection (OTP)
  - Brownout protection
  - Output Short Protection (OSP)
  - Output open OverVoltage Protection (OVP)
  - Mains synchronization loss protection
- Low component count LED driver solution
- Compatible with wall switches with built-in indication light during standby(
- IC lifetime matches or surpasses LED lamp lifetime

## 3. Applications

- Compact mains connected, remote-controlled LED lamps with accurate, dimmable current output for single or universal mains voltages, including 100 V (AC), 120 V (AC) and 230 V (AC). External components determine the power level. The power level ranges from 4 W to over 25 W. Applications fit in common form factors like PAR, GU10, A19, and the candle form factor.

# 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 8.8 | - | 32 | V |
| $f_{sw}$ | switching frequency | low-frequency mode; undimmed | | | | |
| | | 50 Hz mains | 55 | 60 | 65 | kHz |
| | | 60 Hz mains | 66 | 72 | 78 | kHz |
| | | high-frequency mode; undimmed | | | | |
| | | 50 Hz mains | 84 | 91 | 98 | kHz |
| | | 60 Hz mains | 101 | 109 | 117 | kHz |
| $I_{CC}$ | supply current | normal operation | - | 2.25 | - | mA |
| $V_{I(DRAIN)}$ | input voltage on pin DRAIN | not repetitive | - | - | 700 | V |
| $V_{o(PWRDRV)}$ | output voltage on pin PWRDRV | high level | - | 10.7 | - | V |

# 5. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| SSL5511T | SO8 | plastic small package outline body; 8 leads; body width 3.9 mm | SOT96-1 |

# 6. Block diagram

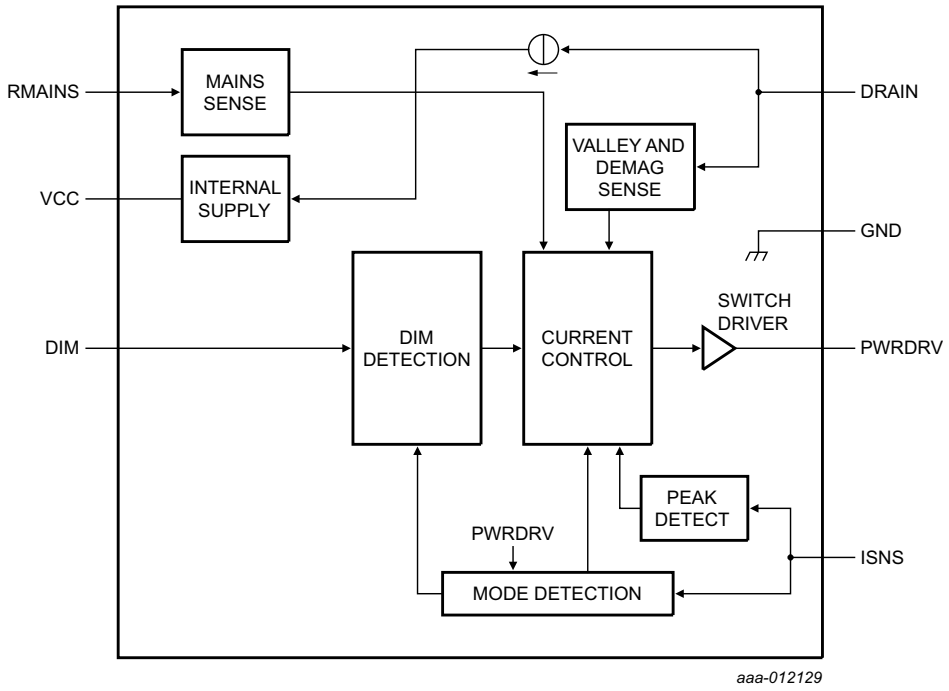



**Fig 1. SSL5511T block diagram**

# 7. Pinning information

## 7.1 Pinning

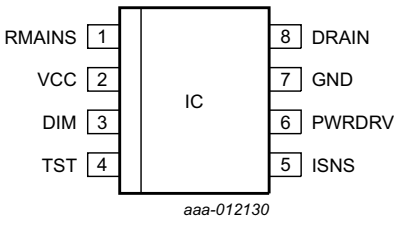



**Fig 2. SSL5511T pinning diagram**

### 7.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| RMAINS | 1 | mains detection input |
| VCC | 2 | IC supply input/output |
| DIM | 3 | dim-level control input |
| TST | 4 | IC test pin, to be connected to ground in application |
| ISNS | 5 | peak current sense input |
| PWRDRV | 6 | external MOSFET gate driver output |
| GND | 7 | ground |
| DRAIN | 8 | external MOSFET drain sense input |

## 8. Functional description

### 8.1 Pin functionality

#### 8.1.1 Pin RMAINS

The RMAINS pin takes in a current representing the rectified mains voltage via the external RMAINS resistors. The low ohmic input results in current always flowing, causing the voltage on the RMAINS pin to remain below the maximum $V_{i(RMAINS)}$ at any time. The information about the mains voltage is used to shape the output current waveform in LTHD modes. It is also used for internal timing synchronizations, making it essential for the low-ripple applications. Some filtering may be required outside the IC to eliminate incoming noise.

If the pin does not receive a rectified mains signal, the mains synchronization loss protection is triggered.

#### 8.1.2 Pin VCC

At power-up, the VCC pin and its capacitor are charged using the internal HV current source from the DRAIN pin. Once $V_{CC}$ has reached $V_{CC(startup)}$, switching starts and $V_{CC}$ supply is generated from the auxiliary winding. If $V_{CC}$ exceeds $V_{ovp(VCC)}$ due to, for example, a disconnected output, OVP is triggered. If $V_{CC}$ drops to $V_{CC(low)}$, the internal HV current source is enabled. If $V_{CC}$ drops to below $V_{CC(stop)}$, UVLO protection is triggered.

Do not use the VCC pin to power additional circuitry outside the IC because no additional current budget is guaranteed. An additional $V_{CC}$ load can affect product performance.

To support wall switches that include an indicator light, a predetermined current ($I_{CC}$) is pulled from the supply during a limited window of the VCC voltage (see condition 2 of $I_{CC}$ in Table 7).

#### 8.1.3 Pin DIM

The DIM pin is the dimming level control pin. It also acts as the on/off control pin. It accepts both an analog voltage signal and a digital control signal as input. The type of input signal is automatically detected and the input is then translated into a target output current level (see Section 8.2.6).

### 8.1.4 Pin ISNS

The ISNS pin senses the voltage across the sense resistor, $R_{SNS}$, generated by the inductor current flowing through the external MOSFET and this resistor (see Figure 3).

Optionally, a mode definition resistor is present between the pin and the current sense resistor. At start-up, the mode resistor is measured using a current which is sourced out of the pin.

### 8.1.5 Pin PWRDRV

The SSL5511T is equipped with a driver that controls an external MOSFET. The voltage on the driver output pin is increased towards the maximum $V_{o(PWRDRV)}$ to open the switch during the first cycle (t0 to t1; see Figure 4). It is pulled to ground from the start of the secondary stroke until the next cycle starts (t1 to t00). During the transition from low to high and back, the switching slope is controlled, limiting the high-frequency radiation.

### 8.1.6 Pin DRAIN

The DRAIN pin is used to derive energy to charge the VCC pin at start-up and after switching is stopped because of a triggered protection. The signal at the DRAIN pin is also used to detect demagnetization and to determine the valley of the ringing voltage for starting the primary stroke.

## 8.2 Converter operation

### 8.2.1 Available modes

The SSL5511T incorporates various built-in operation modes which can be selected in the application using a maximum of two external resistors. At start-up, the value of these resistors is detected and the corresponding operation mode is set.

The mode resistor at the PWRDRV ($R_{TF}$) is connected to ground. The mode resistor at the ISNS pin ($R_{CTL}$)is connected between the pin and the external MOSFET source (see Figure 3).

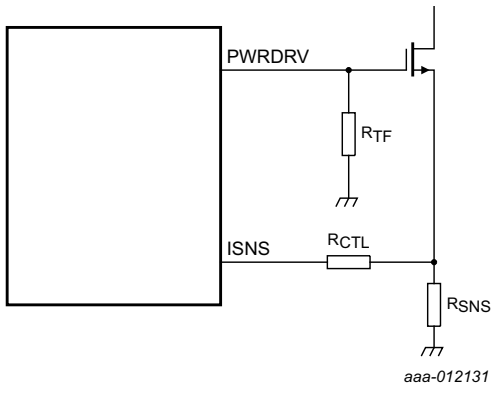



**Fig 3. Mode resistor connections**

Table 4 gives an overview of the available modes.

**Table 4. Available modes**

| Parameter | How to set | Options | Mode resistor value |
|---|---|---|---|
| topology and frequency | $R_{TF}$ on pin PWRDRV | flyback or buck-boost; HF mode | ∞ |
| | | buck; HF mode | 56 kΩ |
| | | buck; LF mode | 33 kΩ |
| | | flyback or buck-boost; LF mode | 15 kΩ |
| control mode | $R_{CTL}$ on pin ISNS | low ripple (PF < 0.7) | 0 kΩ to 0.5 kΩ or 3.3 kΩ |
| | | eco-LTHD (PF ~ 0.75) | 1.5 kΩ |
| | | LTHD (PF > 0.9) | 5.6 kΩ |

### 8.2.2 Switching scheme

The converter in the SSL5511T is a Discontinuous Conduction Mode (DCM), peak current controlled system. When the output current control system requires a new switching cycle and the inductor current is zero, the external MOSFET is turned on at the next detected valley (see Section 8.2.3). The inductor current increases until a maximum, defined by the regulation loop, is reached and the MOSFET is switched off. The inductor current reduces again. When the inductor current reaches zero, it is detected at the DRAIN pin. The detection enables the control system to regulate to an accurate average value of the LED current.

The maximum switching frequency can be set at two rates (see Section 8.2.1).

Three options are available which determine how the controller adjusts the maximum inductor peak current over the mains cycle. The result is either an optimal input current shape (optimized power factor and THD), a minimal LED current ripple, or an intermediate solution (eco-LTHD mode).

### 8.2.3 Valley detection

A new cycle is started when the primary switch is switched on (see Figure 4). At a certain time (t1), the switch is turned off and the secondary stroke starts. After the secondary stroke (t3), the drain voltage shows oscillation or ringing. Circuitry at the DRAIN pin senses when the voltage on the drain of the switch has reached its lowest value (valley) during each oscillation. When the control loop requires the next cycle, it is started the next time a valley occurs. As a result, the capacitive switching losses reduce significantly. For successful valley detection, the frequency and amplitude of the drain voltage ringing must cause the slope of the ringing voltage to exceed the detection limit $(dV/dt)_{vrec}$ for at least $t_{d(vrec\text{-}swon)}$.

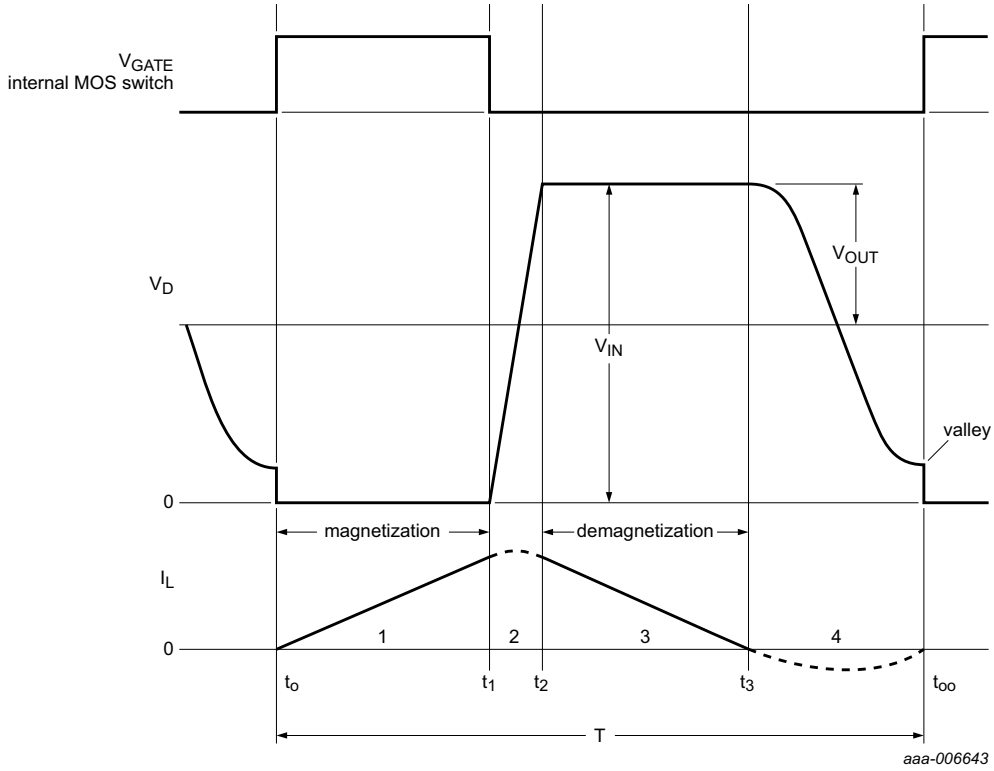



**Fig 4. Buck waveforms and valley detection**

### 8.2.4 Output current settings

The IC regulates the output LED current with great accuracy over line, load and component variations. The user can set the full-scale (100 %) value of the LED current. Choose a current sense resistor value according to Equation 1:

$$I_{LED} = \frac{V_{reg}}{R_{SNS}} \times N \quad (1)$$

Where:

- $V_{reg}$ is the set point of the internal regulation loop: 117 mV for LTHD buck-boost/flyback, 234 mV for LTHD buck and low ripple buck-boost/flyback, and 469 mV for low-ripple buck
- $R_{SNS}$ is the sense resistor on pin ISNS (see Figure 3)
- N is the transformer ratio

The IC regulates the output current by controlling the current sense threshold voltage $V_{th(ISNS)}$, the number of switching cycles per (half-)mains period, and, if necessary, the switching frequency, depending on the mode of operation.

### 8.2.5 Preventing Continuous Conduction Mode (CCM)

To enable application design without having to include margins to ensure DCM operation, a CCM-prevention feature has been built in. The IC monitors the time gap between the end of the secondary stroke and the start of the next cycle. If this time becomes shorter than a predetermined idle time of about 1.8 μs, the controller reduces the switching frequency.

### 8.2.6 Dimming support

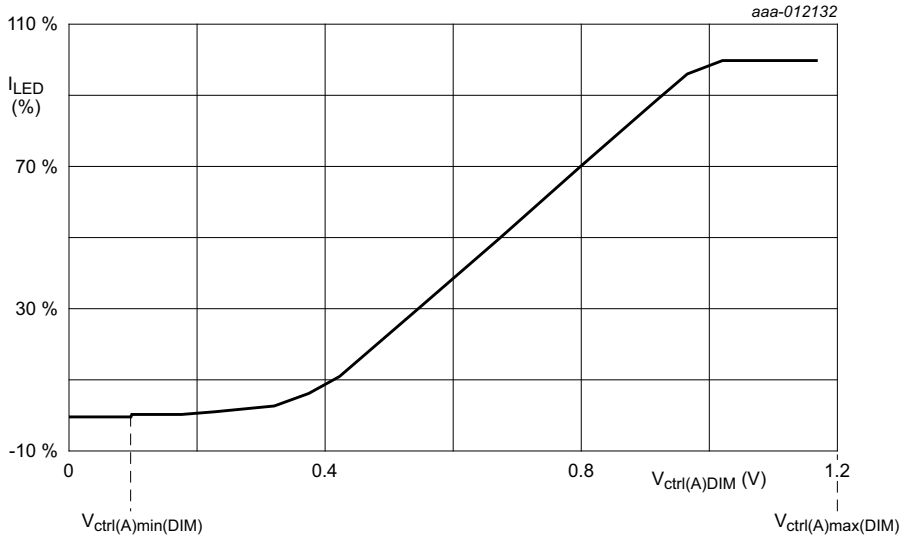
The SSL5511T accepts one of two different types of control signals on the DIM pin, either an analog voltage signal or a digital control signal. The type of the dimming control is detected during start-up. If digital switching occurs on the DIM pin, or if a voltage above the analog dimming input range ($V_{ctrl(A)DIM}$) is present on the pin, digital dimming control is detected. If a voltage within the analog range ($V_{ctrl(A)DIM}$) is present on the pin, then analog dimming control is detected. If the input remains low (below the analog dimming range), the target output current level is set to zero, and standby mode is entered. Dim mode selection is then postponed until one of the above detection conditions is met. Once the dimming type is detected, it is set fixed until power-down. During operation in either analog or digital dimming mode, the measurement of the DIM pin is done once in every full mains cycle. For both dimming control types, the output current regulation remains analog.

- Analog Input Dimming Control (AIDC):

  In this mode, an input voltage within the analog range ($V_{ctrl(A)DIM}$) is accepted on the DIM pin and translated to a target output current level. Figure 5 shows the plotting of the dimming percentage of the output current against the input voltage. The smooth tail of the curve matches human eye light sensitivity. The minimum output current level as a ratio of the full-scale current is $I_{LEDlow}/I_{LED100}$. If the input voltage drops to below the analog range by more than the built-in hysteresis ($V_{hys(low)DIM}$), the output current is set to zero. The IC enters standby mode. Some filtering may be required outside the IC to eliminate incoming noise.

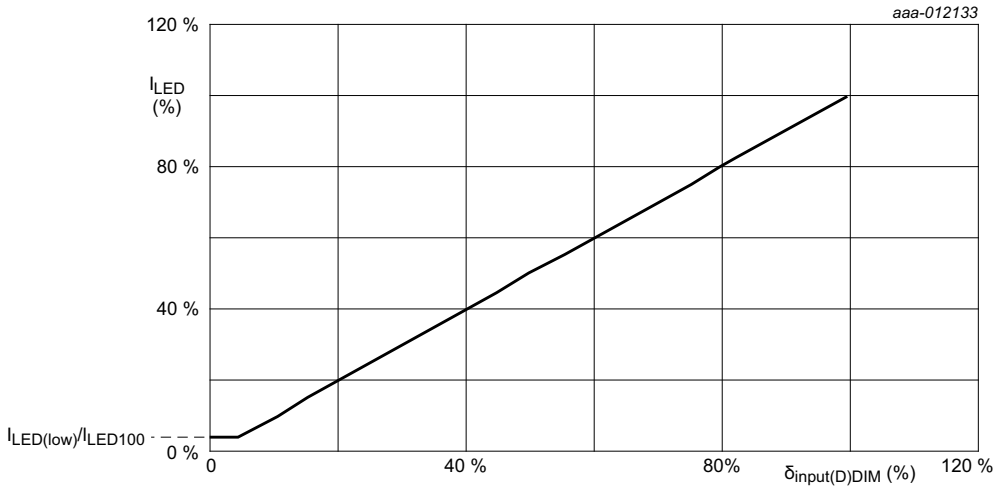
- Digital Input Dimming Control (DIDC):

  A digital signal of a frequency within the range $f_{i(DIM)}$, and levels satisfying the thresholds $V_{th(L)DIM}$ and $V_{th(H)DIM}$ are accepted and translated to a target LED current level. The dimming percentage of the output current equals the duty cycle of the input signal (expressed as a percentage; see Figure 6). The minimum output current level as a ratio of the full-scale current is $I_{LEDlow}/I_{LED100}$. If the input signal is low for longer than $t_{det(stb)DIM}$ in the measurement window, the output current is set to zero. The IC enters standby mode.




(1) See $I_{LEDlow}/I_{LED100}$, analog dimming control in Table 7.

**Fig 5. LED current ratio as a function of analog control voltage**




(1) See $I_{LEDlow}/I_{LED100}$, digital dimming control in Table 7.

**Fig 6. Output current as a function of digital dimming input duty cycle**

## 8.3 Protections

The IC incorporates the following protections:

- UnderVoltage LockOut (UVLO
- OverCurrent Protection (OCP)
- Brownout Protection
- Output Short Protection (OSP)
- Output open OverVoltage Protection (OVP)
- Internal OverTemperature Protection (OTP)
- Mains synchronization loss protection
- Leading Edge Blanking (LEB)

Output open OVP is a latched protection. Power-off cycling is required to exit the latched state. All other protections are not latched and lead to a safe restart of the converter.

### 8.3.1 UnderVoltage LockOut (UVLO)

When the voltage on the VCC pin drops to below the value of $V_{CC(stop)}$, the IC stops switching. The internal HV current source is enabled. Once $V_{CC}$ has increased to $V_{CC(startup)}$, the IC restarts a minimum of 1 s back-off time.

### 8.3.2 OverCurrent Protection (OCP)

The SSL5511T contains a highly accurate peak current detector. It triggers when the voltage at pin ISNS reaches $V_{th(ISNS)}$. The circuit is activated after the leading edge blanking time ($t_{leb}$). There is a propagation delay between the peak current detection and the switch actually switching off. Due to this delay, the actual peak current is slightly higher than the peak current level set by the current sense resistor. The control loop compensates for this difference ensuring output current accuracy.

### 8.3.3 Brownout protection

The brownout protection is designed to limit the switch-on time in case of low input voltage. Because of the built-in peak current control, the input current otherwise slowly increases while no power is transferred to the output in a flyback configuration. The SSL5511T includes a maximum on-time of the switch $t_{on(high)}$.

### 8.3.4 Output short protection (OSP)

During the secondary stroke (switch-off time), if a valley is not detected within the off-time limit ($t_{off(high)}$), the output voltage is typically less than the minimum limit allowed in the application. This condition can occur either during start-up or due to a short. A timer is started when $t_{off(high)}$ is detected. It is only stopped if a valid valley-detection occurs in one of the subsequent cycles. If no valley is detected for $t_{det(sc)}$, it is concluded that a real short-circuit exists and not a temporary start-up situation. The IC enters standby mode and tries to restart after a minimum of 9 s back-off time.

### 8.3.5 Output open OverVoltage Protection (OVP)

The result of an output open situation is that no power is delivered to the output, causing $V_{CC}$ to exceed $V_{CC(max)}$. Upon detection of this event, the IC enters the standby mode. As long as mains voltage is present, the IC does not restart.

### 8.3.6 Internal OverTemperature Protection (OTP)

When the internal OTP function is triggered, the converter stops operating. This function is triggered at $T_{th(act)otp}$. The Overtemperature protection is an auto-restart protection. The IC restarts when the IC temperature drops to below $T_{th(rel)otp}$.

### 8.3.7 Mains synchronization loss protection

When the input current at the RMAINS pin fails to cross the "zero crossing detection" value of $I_{i(RMAINS)}$, no mains cycles are detected. If this situation persists for a time $t_{d(mld)}$, the IC stops switching. Once a valid mains signal is available again, the IC restarts.

### 8.3.8 Leading Edge Blanking (LEB)

A blanking time is implemented after switch-on to prevent premature detection of inductor peak current. At the opening of the MOSFET switch, a short current spike can occur because of the capacitive discharge of voltage over the drain and source. During the leading edge blanking time ($t_{leb}$), detection is disabled. So spikes are disregarded.

# 9. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| $P_{tot}$ | total power dissipation | SO8 package | - | 0.6 | W |
| $T_{amb}$ | ambient temperature | | –40 | +125 | °C |
| $T_j$ | junction temperature | | –40 | +190 | °C |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| SR | slew rate | pin DRAIN | –10 | +10 | V/ns |
| **Pin voltages and currents** | | | | | |
| $V_{CC}$ | supply voltage | | –0.4 | +34 | V |
| $V_{i(RMAINS)}$ | input voltage on pin RMAINS | current limited | –0.4 | +5.2 | V |
| $I_{i(RMAINS)}$ | input current on pin RMAINS | at $V_{RMAINS}$ = 5.2 V | 0 | 2.5 | mA |
| $V_{i(ISNS)}$ | input voltage on pin ISNS | | –0.4 | +5.2 | V |
| $V_{i(DRAIN)}$ | input voltage on pin DRAIN | during mains surge; not repetitive | –0.4 | +700 | V |
| $V_{ESD}$ | electrostatic discharge voltage | human body model [1] | | | |
| | | all pins except pin DRAIN | –2000 | +2000 | V |
| | | pin DRAIN | –1000 | +1000 | V |
| | | charged device model [2] | –500 | +500 | V |

[1] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Charged device model: equivalent to charging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

# 10. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; PCB: 2 cm × 3 cm; 2-layer; 35 μm Cu/layer | 159 | K/W |
| | | in free air; PCB: JEDEC 2s2p | 89 | K/W |
| $\Psi_{j-top}$ | thermal characterization parameter from junction to top of package | top package temperature measured at the warmest top of the case point | 0.49 | K/W |

# 11. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **High voltage** | | | | | | |
| $V_{I(DRAIN)}$ | input voltage on pin DRAIN | [1] | - | - | 675 | V |
| $I_{i(DRAIN)}$ | input current on pin DRAIN | JFET on strong; $V_{DRAIN}$ = 675 V; $V_{CC}$ = 17 V | 4 | 5.5 | 7 | mA |
| | | JFET off; $V_{DRAIN}$ = 675 V; $V_{CC}$ = 20 V | - | - | 15 | µA |
| | | JFET on weak; $V_{DRAIN}$ = 675 V; $V_{CC}$ < 4 V | 500 | 550 | 600 | µA |
| **Supply** | | | | | | |
| $V_{CC(startup)}$ | start-up supply voltage | | 17.5 | 18.5 | 19.5 | V |
| $V_{CC(low)}$ | low supply voltage | pin VCC | 11.2 | 11.8 | 12.4 | V |
| $V_{CC(stop)}$ | stop supply voltage | | 8.8 | 9.3 | 9.8 | V |
| $V_{CC(hys)}$ | hysteresis of supply voltage | between $V_{startup}$ and $V_{stop}$ | 8.5 | 9.1 | 9.7 | V |
| $V_{ovp(VCC)}$ | overvoltage protection voltage on pin VCC | | 28 | 30 | 32 | V |
| $I_{CC}$ | supply current | pin DRAIN; $V_{CC}$ < 4 V; standby mode | - | 0.1 | 0.2 | mA |
| | | pin DRAIN; 4 V < $V_{CC}$ < $V_{CC(low)}$; standby mode | 1 | 1.25 | 1.5 | mA |
| | | pin DRAIN; $V_{CC}$ > $V_{CC(low)}$; standby mode | - | 0.2 | - | mA |
| | | pin VCC; normal operation, excluding drive currents to PWRDRV | - | 2.25 | - | mA |
| **Current regulator and protection** | | | | | | |
| $f_{sw}$ | switching frequency | low-frequency mode; undimmed | | | | |
| | | 50 Hz mains | 55 | 60 | 65 | kHz |
| | | 60 Hz mains | 66 | 72 | 78 | kHz |
| | | high-frequency mode; undimmed | | | | |
| | | 50 Hz mains | 84 | 91 | 98 | kHz |
| | | 60 Hz mains | 101 | 109 | 117 | kHz |
| $V_{th(high)ISNS}$ | high threshold voltage on pin ISNS | at peak current | 1.195 | 1.24 | 1.285 | V |
| $V_{th(low)ISNS}$ | low threshold voltage on pin ISNS | (eco-)LTHD mode; at peak current | 0.75 | 0.78 | 0.81 | V |
| | | low-ripple mode | 0.33 | 0.35 | 0.37 | V |
| $t_{leb}$ | leading edge blanking time | | - | 600 | - | ns |

**Table 7. Characteristics** *…continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Valley detection** | | | | | | |
| $(\Delta V/\Delta t)_{vrec}$ | valley recognition voltage change with time negative slope | voltage ringing on pin DRAIN | −26 | −16 | −6 | V/µs |
| $t_{d(vrec\text{-}swon)}$ | valley recognition to switch-on delay time | | - | 100 | - | ns |
| **Brownout protection** | | | | | | |
| $t_{on(high)}$ | high on-time | low-frequency mode | | | | |
| | | 50 Hz mains | 13.2 | 14.4 | 15.6 | µs |
| | | 60 Hz mains | 11.0 | 12.0 | 13.0 | µs |
| | | high-frequency mode | | | | |
| | | 50 Hz mains | 8.8 | 9.6 | 10.4 | µs |
| | | 60 Hz mains | 8.3 | 9.0 | 9.7 | µs |
| **Output short protection** | | | | | | |
| $t_{off(high)}$ | high off-time | | 32 | 40 | 48 | µs |
| $t_{det(sc)}$ | short-circuit detection time | 50 Hz mains | 10 | - | 20 | ms |
| | | 60 Hz mains | 8.3 | - | 16.7 | ms |
| **Temperature protections** | | | | | | |
| $T_{th(act)otp}$ | overtemperature protection activation threshold temperature | on-chip | 160 | 175 | 190 | °C |
| $T_{th(rel)otp}$ | overtemperature protection release threshold temperature | on-chip | 90 | 102 | 114 | °C |
| **Pin PWRDRV** | | | | | | |
| $V_{o(PWRDRV)}$ | output voltage on pin PWRDRV | high level | | | | |
| | | $V_{VCC} > V_{CC(low)}$ | - | 10.7 | - | V |
| | | $V_{VCC} = V_{CC(stop)}$ | - | 8.5 | - | V |
| $I_{source(PWRDRV)}$ | source current on pin PWRDRV | 20 µs maximum; $V_{PWRDRV}$ = 2 V | - | 360 | - | mA |
| $I_{sink(PWRDRV)}$ | sink current on pin PWRDRV | 20 µs maximum; $V_{PWRDRV}$ = 10 V | - | 900 | - | mA |
| | | 20 µs maximum; $V_{PWRDRV}$ = 2 V | - | 260 | - | mA |
| **Pin DIM** | | | | | | |
| $V_{ctrl(A)DIM}$ | analog control voltage on pin DIM | | 0.1 | - | 1.2 | V |
| $V_{hys(low)DIM}$ | low hysteresis voltage on pin DIM | analog dimming control | - | −20 | - | mV |
| $V_{th(L)DIM}$ | LOW-level threshold voltage on pin DIM | digital dimming control | 0.30 | 0.40 | 0.50 | V |
| $V_{th(H)DIM}$ | HIGH-level threshold voltage on pin DIM | digital dimming control | 1.25 | 1.50 | 1.75 | V |
| $f_{i(DIM)}$ | input frequency on pin DIM | digital dimming control | 0.1 | - | 10 | kHz |
| $I_{offset(DIM)}$ | offset current on pin DIM | | −7 | −11 | −15 | µA |

**Table 7. Characteristics** *…continued*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LED(low)}/I_{LED100}$ | low LED current ratio | analog dimming control | [2] | - | 0.008 | - | |
| | | digital dimming control; $f_{i(DIM)} < 3$ kHz | [2] | - | 0.001 | - | |
| | | digital dimming control; 3 kHz < $f_{i(DIM)} < 10$ kHz | [2] | 0.001 | - | 0.004 | |
| | | digital dimming control; $f_{i(DIM)} = 10$ kHz | [2] | - | 0.004 | - | |
| $t_{det(stb)DIM}$ | standby detection time on pin DIM | digital dimming control | | - | 10 | - | ms |
| **Pin RMAINS** | | | | | | | |
| $I_{i(RMAINS)}$ | input current on pin RMAINS | at top of mains sine wave | | 324 | 360 | 396 | µA |
| | | for zero cross detection | | 18 | 22.5 | 27 | µA |
| $t_{d(mld)}$ | mains loss detection delay time | 50 Hz mains | | - | 60 | - | ms |
| | | 60 Hz mains | | - | 50 | - | ms |
| $I_{sink(RMAINS)}$ | sink current on pin RMAINS | $V_{i(RMAINS)} = 4$ V | | 400 | - | - | µA |

[1] The peak voltage on pin DRAIN occurs each switching cycle, based 25,000 hours device lifetime.

[2] Actual LED current values are lower due to the IC supply current.

## 12. Application information

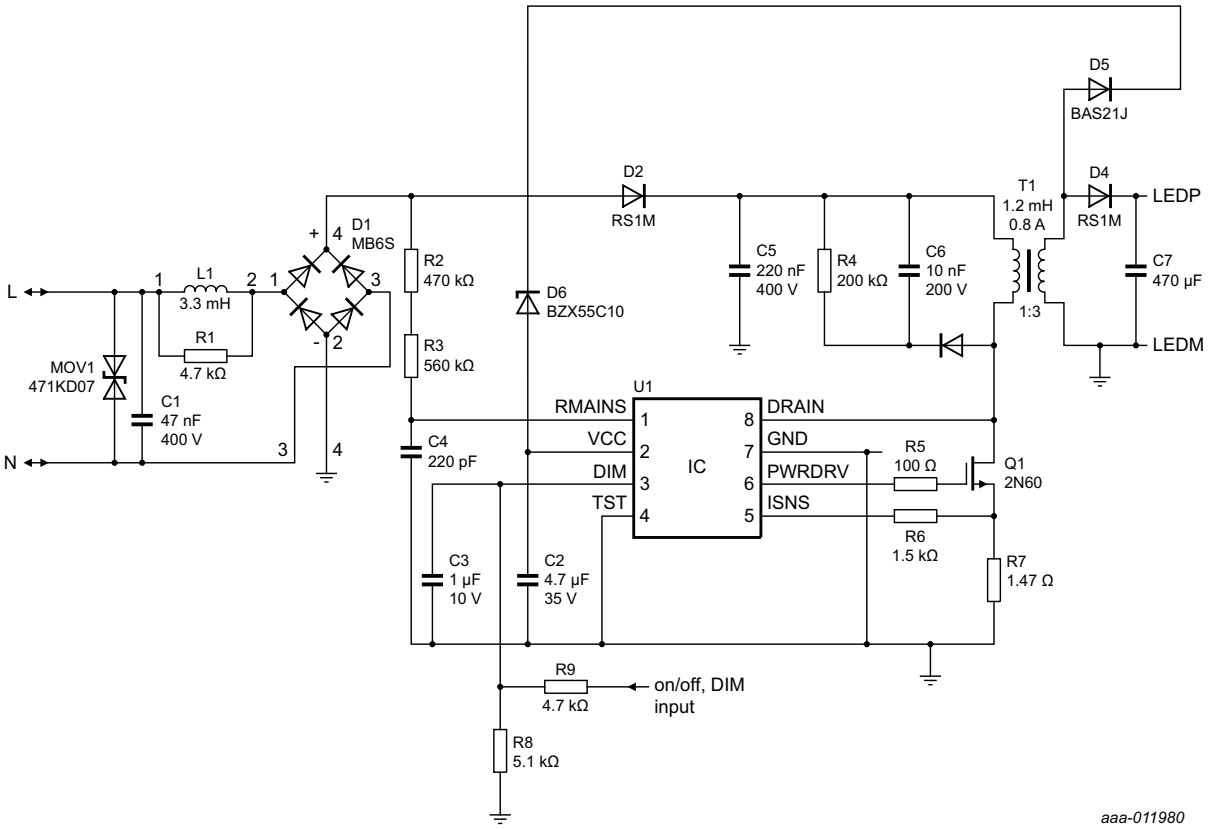
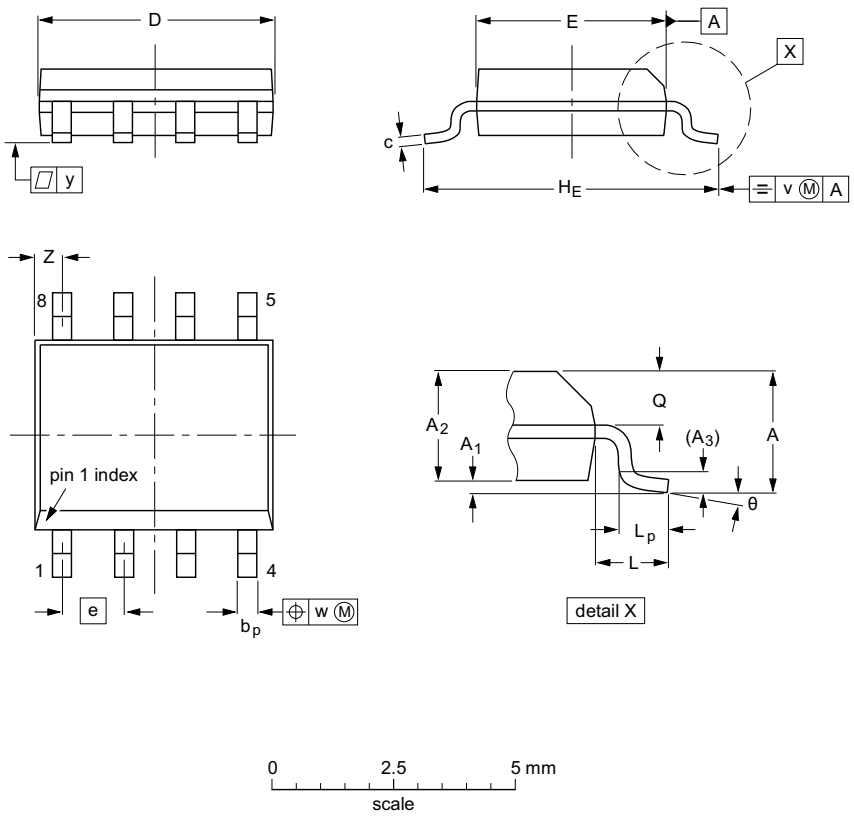



**Fig 7. SSL5511T flyback configuration; LTHD; input = 230 V (AC); output = 35 V/200 mA**

# 13. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 8. Package outline SOT96-1 (SO8)**

# 14. Revision history

**Table 8. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| SSL5511T v.2 | 20140630 | Product data sheet | - | SSL5511T v.1 |
| Modifications: | • Data sheet status has changed from Preliminary to Product.<br>• Text and graphics updated throughout the document. | | | |
| SSL5511T v.1 | 20140527 | Preliminary data sheet | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 17. Contents


**1 General description . . . . . 1**
**2 Features and benefits . . . . . 2**
**3 Applications . . . . . 2**
**4 Quick reference data . . . . . 3**
**5 Ordering information . . . . . 3**
**6 Block diagram . . . . . 4**
**7 Pinning information . . . . . 4**
7.1 Pinning . . . . . 4
7.2 Pin description . . . . . 5
**8 Functional description . . . . . 5**
8.1 Pin functionality . . . . . 5
8.1.1 Pin RMAINS . . . . . 5
8.1.2 Pin VCC . . . . . 5
8.1.3 Pin DIM . . . . . 5
8.1.4 Pin ISNS . . . . . 6
8.1.5 Pin PWRDRV . . . . . 6
8.1.6 Pin DRAIN . . . . . 6
8.2 Converter operation . . . . . 6
8.2.1 Available modes . . . . . 6
8.2.2 Switching scheme . . . . . 7
8.2.3 Valley detection . . . . . 7
8.2.4 Output current settings . . . . . 8
8.2.5 Preventing Continuous Conduction Mode (CCM) . . . . . 9
8.2.6 Dimming support . . . . . 9
8.3 Protections . . . . . 11
8.3.1 UnderVoltage LockOut (UVLO) . . . . . 11
8.3.2 OverCurrent Protection (OCP) . . . . . 11
8.3.3 Brownout protection . . . . . 11
8.3.4 Output short protection (OSP) . . . . . 11
8.3.5 Output open OverVoltage Protection (OVP) . . 11
8.3.6 Internal OverTemperature Protection (OTP) . . 12
8.3.7 Mains synchronization loss protection . . . . . 12
8.3.8 Leading Edge Blanking (LEB) . . . . . 12
**9 Limiting values . . . . . 13**
**10 Thermal characteristics . . . . . 13**
**11 Characteristics . . . . . 14**
**12 Application information . . . . . 17**
**13 Package outline . . . . . 18**
**14 Revision history . . . . . 19**
**15 Legal information . . . . . 20**
15.1 Data sheet status . . . . . 20
15.2 Definitions . . . . . 20
15.3 Disclaimers . . . . . 20
15.4 Trademarks . . . . . 21
**16 Contact information . . . . . 21**
**17 Contents . . . . . 22**




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