QorIQ T1023 Reference Design Board User Guide

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freescale™

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Chapter 1
Overview

The T1023 Reference design board (T1023RDB) is a system featuring QorIQ advanced multicore processor. It combines two 64-bit ISA Power Architecture processor cores with high-performance data path acceleration and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and military/aerospace application.

This low-cost, high-performance system solution consists of a Printed circuit board (PCB) assembly and a software Board support package (BSP). This BSP enables the fastest possible time-to-market for development or integration of applications including multi-service branch office router, security appliance/UTM and enterprise wireless access point. This document describes the hardware features of the board including specifications, block diagram, connectors, interfaces, and hardware straps. It also describes the board settings and physical connections needed to boot the RDB. Revision history lists the changes to this document.

When you finish reading this document, you should be familiar with:

- Board layout and its interfaces
- Board configuration options

This document is applicable for PCBA version **700-28530 Rev D** and Schematics version **SCH-28530 Rev D**.

1.1 Related documentation

The table below lists and explains the additional documents that you can refer to, for more information about T1023RDB.

Some of the documents listed below may be available only under a Non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1-1. Useful references

Document	Description
QorIQ T1023 Integrated Processor Reference Manual	Provides a detail description on T1023 QorIQ multicore processor, and on some of its features like memory map, serial interfaces, power supply, chip features, and clock information.
QorIQ T1023, T1013 Data Sheet	Provides specific data regarding AC, DC electrical specifications, thermal characteristics, and pin assignments, as well as other design considerations.

1.2 Acronyms and abbreviations

The table below lists and explains the acronyms and abbreviations used in this document.

Table 1-2. Acronyms and abbreviations

Usage	Description
COP	Common On-chip Processor
CPC	CoreNet Platform Cache
CPLD	Complex Programmable Logic Device
DIMM	Dual In-Line Memory Module
DIP	Dual In-Line Package
DIU	Display Interface Unit
DMA	Direct Memory Access
DPAA	Data Path Acceleration Architecture
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
EC	Ethernet Controllers
EDC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Ethernet Management Interfaces
eMMC	embedded MultiMediaCard
eSDHC	enhanced Secure Digital Host Controller
eSPI	enhanced Serial Peripheral Interface
FET	Field Effect Transistor
HDLC	High-level Data Link Control
I2C	Inter-Integrated Circuit
IFC	Integrated Flash Controller
JTAG	Joint Test Action Group

Table continues on the next page...

Table 1-2. Acronyms and abbreviations (continued)

Usage	Description
MPIC	Multicore Programmable Interrupt Controller
PCIe/PEX	PCI Express
PLD	Programmable Logic Device
POR	Power On Reset
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDRAM	Synchronous Dynamic Random-Access Memory
SDHC	Secure Digital High Capacity
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SPI	Serial Peripheral Interface
SYSCLK	System Clock
TDM	Time-Division Multiplexing
UART	Universal Asynchronous Receiver/Transmitter
VCC	Voltage for Circuit
VTT	Voltage for Terminal

1.3 T1023RDB board features

The T1023RDB board features are as follows:

- T1023RDB runs at default core frequency 1.2 GHz, platform clock 400 MHz, DDR4 1600 MT/s.
- Memory subsystem:
  - 2 GB unbuffered DDR4 SDRAM discrete devices (32-bit bus)
  - 128 MB NOR flash single-chip memory
  - 512 MB NAND flash memory
  - 256 Kbit M24256 I2C EEPROM
  - 64 MB SPI memory
  - 8 GB eMMC 4.51
  - SD/MMC connector to interface with the SD memory card
- Interfaces
  - PCIe:
    - Lane A: x1 mini-PCIe slot
    - Lane C: x1 mini-PCIe slot
  - 10/100/1000 BaseT Ethernet ports:
    - EC1, RGMII: one 10/100/1000 port with RTL8211FS PHY

        - Lane B: 2.5G SGMII port with AQR105 PHY
        - Lane D: 1G SGMII port with RTL8211FS PHY
    - USB 2.0 port:
        - X1 USB2.0 port: connect to a type-A conector
    - UART interface:
        - UART interface: supports one UART at default 115200 Baud rate for console display
        - RJ-45 connector is used for the UART port
- Board connectors:
    - JTAG/COP for T1023 debugging
    - Push button for Board Reset
    - Remote Reset Header
- Real-time clock on I2C bus
- Boot Source Selection:
    - Supports NOR/SD/NAND/SPI boot by the selection of the dip switches

NOTE

Boot from eMMC will be supported in the next SDK release.

- PoE:
    - The power is enabled by default for all the boards. Turn off the power of one PCIe card, if the external PoE power is not enough.
- PCB
    - 6-layer routing (4-layer signals, 2-layer power and ground)

The below figure shows the T1023RDB-PC block diagram.

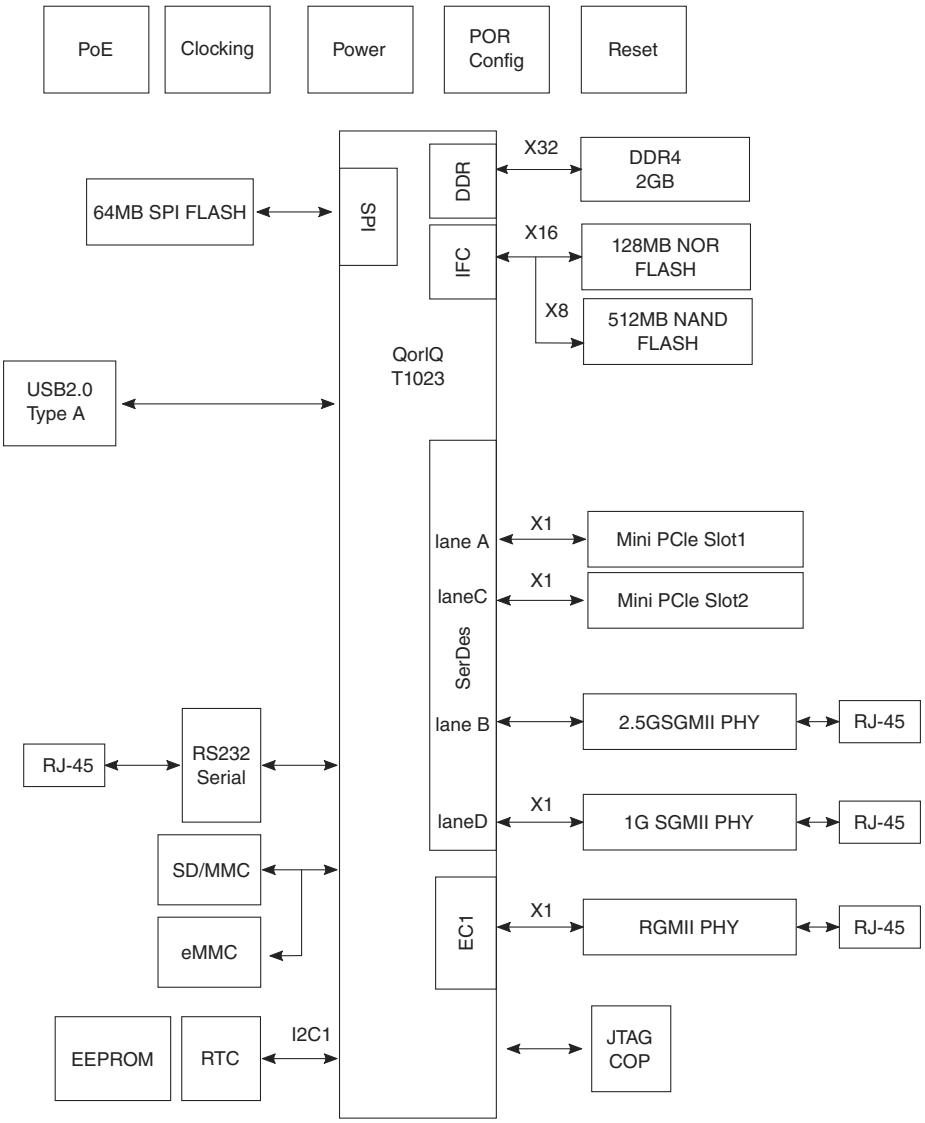


Figure 1-1. Block diagram

1.4 Specifications

The table below lists the specifications of the T1023RDB-PC.

Table 1-3. RDB specifications

Characteristics	Specifications
Chassis Power requirements	Maximum 60 W 12 V AC adapter
Chassis Power requirements	25.5 W If POE is present
Communication processor	T1023 cores running at 1400 MHz
Operating temperature	0 °C to 70 °C (room temperature)
Storage temperature	–25 °C to 85 °C

Table continues on the next page...

Table 1-3. RDB specifications (continued)

Characteristics	Specifications
Relative humidity	5% to 90% (noncondensing)
PCB dimensions: Length Width Thickness	8504 mil (216 mm) 6692 mil (170 mm) 62 mil

1.5 T1023RDB-PC board drawings

The below figure shows the T1023RDB-PC board diagram. The board is 216 mm x 170 mm (8504 mil x 6692 mil).

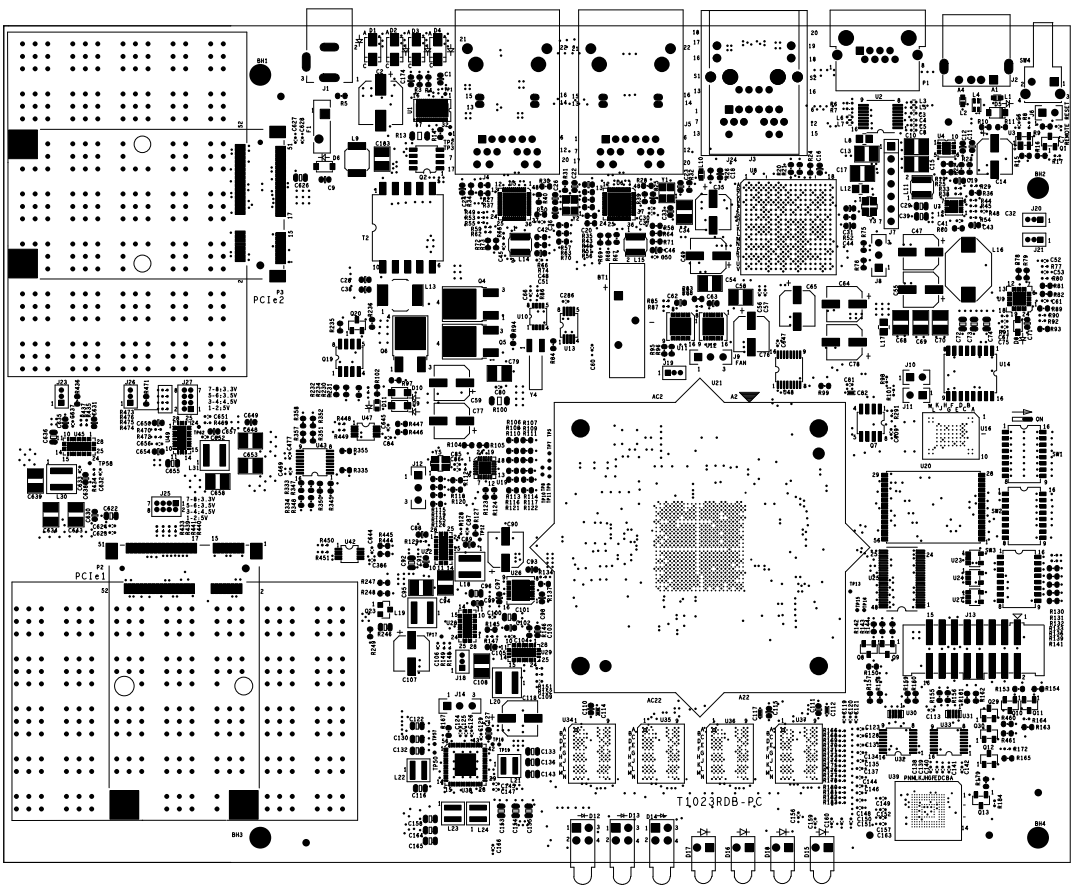


Figure 1-2. T1023RDB-PC board diagram

Chapter 2
Architecture

This chapter explains the architecture of T1023RDB:

- Processor
- Power
- Reset
- Clocks
- Memory interface
- Termination
- SerDes interfaces (PCIe/SGMII/SATA)
- Ethernet controllers
- EC1 10/100/1000 BaseT interface (ETH1)
- SerDes lane D 10/100/1000 BaseT interface (ETH2)
- SerDes lane B 2.5G BaseT interface (ETH3)
- Ethernet management
- Ethernet ports
- I2C
- IFC
- eSPI interface
- eSDHC interface
- GPIO interface
- Interrupts
- USB interface
- RS-232
- POR configuration
- JTAG/COP port
- DMA
- Connectors, Headers, Push buttons, and LEDs
- Switch settings

2.1 Processor

The T1023RDB supports many features of the T1023 processor, as detailed in the following sections. The boards and the supporting hardware are all identical, but the ability to use various features depends on the device installed.

2.2 Power

The power supply system of the T1023RDB systems uses external power adaptor +12 V for the RDB board. The rated power is 60 W.

- **PoE Power Supply** - Linear Technical LTC4269 on board is used for Power over Ethernet function. It is compliant to the 802.3 at standard and can supply 22.5 W power for the board. LTC4269 is sourced from the ETH3 ethernet port. Mini-PCIe slot and SGMII PHY, AQR105 and USB regulators can be turned off by resetting jumpers, once the PoE power is not enough. DCDC provides power these devices. For more details, see Connectors, Headers, Push buttons, and LEDs.
- **CPU VDD (DCDC_1V0)** - The CPU core voltage `DCDC_1V0` rail is sourced from a Linear switching regulator. The device used on the RDB is the LT8612. `DCDC_1V0` = 1.0 V.
- **AVDD For Core PLL, Platform, SerDes** - All these pins are sourced from VR500 SW2 output `VR500_1V8`, and RC filter is used for each pin. Voltage is 1.8 V.
- **DDR** - The memory interface power (VPP, VTT, GVDD, and VREF) are sourced from VR500. VR500_2V5 for VPP = 2.5 V, VR500_VTT for VTT = 0.6 V, VR500_1V2 for GVDD = 1.2 V, and VR500_VREF for VREF = 0.6 V.
- **SerDes** - The SerDes Receiver power S1VDD is sourced from a Linear regulator LT3021. The SerDes Transmitter and PLL power X1VDD is sourced from the VR500. LDO_1V0 for S1VDD = 1.0 V; VR500_1V35 for X1VDD = 1.35 V.
- **eSPI, SDHC_WP, SDHC_CD (CVDD)** - Each of these rails are sourced from the VR500 SW2. VR500_1V8 for CVDD = 1.8 V.
- **SD/MMC (EVDD)** - EVDD can be selected between 1.8 V (VR500_1V8) and 3.3 V (DCDC2_3V3), T1023 pin SDHC_VS is used to enable the selected rail. This pin is pull down to select 3.3 V when it is set high, EVDD will be switched to 1.8 V rail.
- **IFC, GPIO, JTAG IO, System Control (OVDD)** - This rail is sourced from the VR500 SW2. VR500_1V8 for OVDD = 1.8 V.
- **I2C, UART (DVDD)** - I2C and UART interface is operated in 3.3 V level, and are sourced directly from the always on regulator LT8612 (U29), DCDC2_3V3 rail.
- **Ethernet Interface, EMI1 EMI2 (LVDD/TVDD)** - The LVDD rail is used for the TSEC I/O and is configured for 1.8 V operation. The rail is sourced from VR500 SW2, rail is VR500_1V8. TVDD for EMI2 is 1.2 V and sourced from a linear regulator LT3021, rail is LDO_1V2.

- **Mini-PCIe (1.5 V, 3.3 V and PA for QCA card)** - The +1.5 V rail is used by the mini-PCIe slot and is sourced by VR500, rail name is VR500_1V5. The Mini-PCIe 1 (P2) 3.3 V is sourced from regulator LT8612(U29), DCDC2_3V3. The Mini-PCIe 2(P3) 3.3 V is sourced from another regulator LT8612 (U28). Each PA card is sourced from a LT8612(U45 and U49) regulator. Each type of card has different PA voltage. Hence, each DCDC can be adjusted to the four kind of output voltages, that is 3.3 V,3.5 V, 4.5 V,and 5 V. For more details, see Connectors, Headers, Push buttons, and LEDs
- **AQR105 (0.85 V, 1.2 V, 2.1 V, 2.5 V)** - 0.85 V is sourced from part LTC3605A, rail is DCDC_V85; 1.2 V is sourced from part LT3021, rail is LDO_1V2; 2.1 V is sourced from another LT3021 part, rail is LDO_2V1; 2.5 V is sourced from the VR500_2V5 rail.

The following figure shows the board power structure and the current consumption. All the values marked are the maximum values from the datasheet and are only for reference.

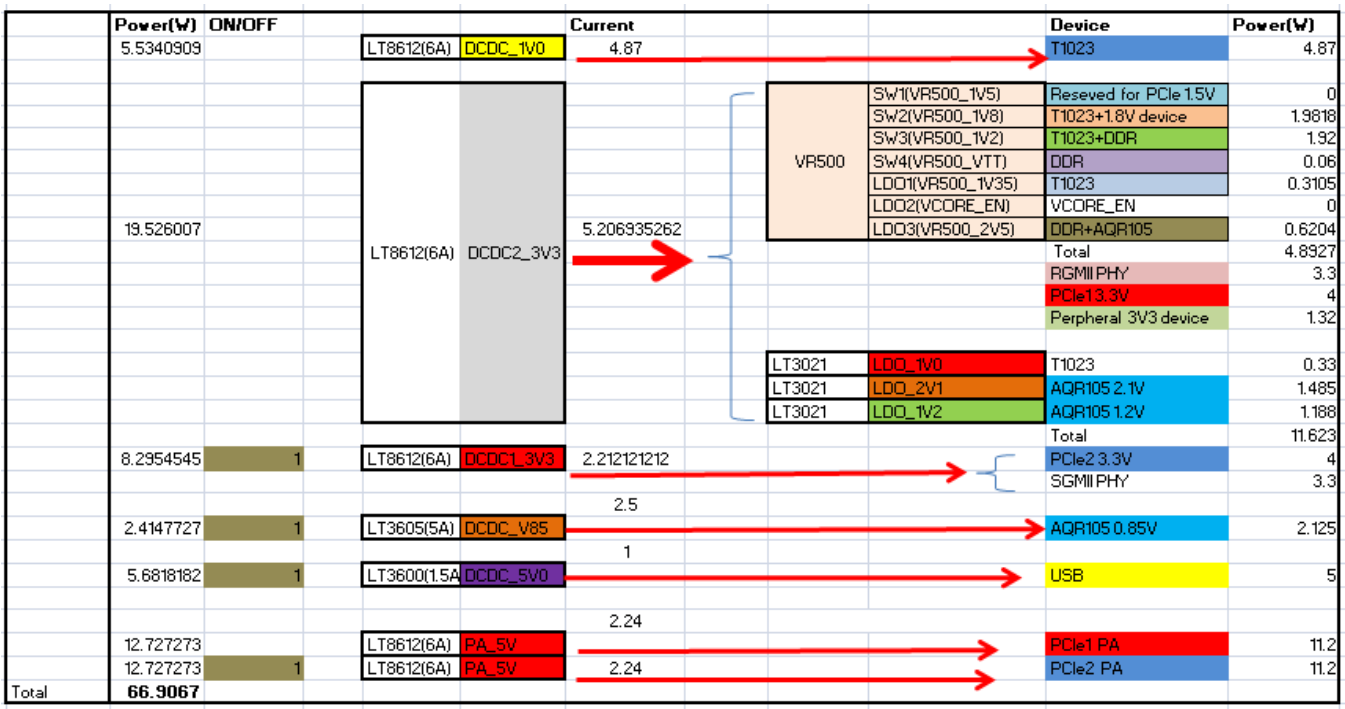


Figure 2-1. Power block

2.3 Reset

All resets on the board are handled by the reset switch SW4. Power-on Reset is initiated by pressing the switch SW4. Software is also capable of initiating a reset by asserting the RESET_REQ line from the processor.

2.4 Clocks

The T1023 board uses single source clocking mode. The clock generator channel provides 100 MHz to the system differential clock input. The Ethernet controller clock is sourced from the RTL8211 PHY.

2.5 Memory interface

The memory interface on the RDB is configured as DDR4 and is implemented as a single bank discrete chips (x8). ECC is not supported on the design. The memory size supported on the board is shown below.

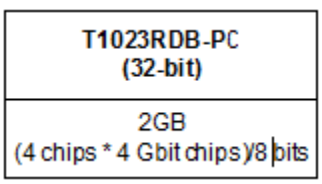


Figure 2-2. Memory interface

The PCB design is capable of running up to a clock rate of 800 MHz (1600 MT/s data rate). The DDR4 interface uses the SSTL driver/receiver and 1.2 V power. A VREF, 1.2V/2 is needed for all SSTL receivers in the DDR4 interface. A VPP 2.5 V is need for DDR4 which is used for activating power supply. For details on DDR4 timing design and termination, see *Application Note AN3940- Hardware and Layout Design Considerations for DDR3 Memory Interfaces*. Signal integrity test results show this design does not require serialing resistors (Series resistor (SR) and Termination resistor (TR)) for the discrete DDR4 devices used. DDR4 supports on-die termination; the DDR4 chips and T1023 are connected directly. The 1.2 V, VREF, VTT, and VPP are powered from a PMIC VR500 output.

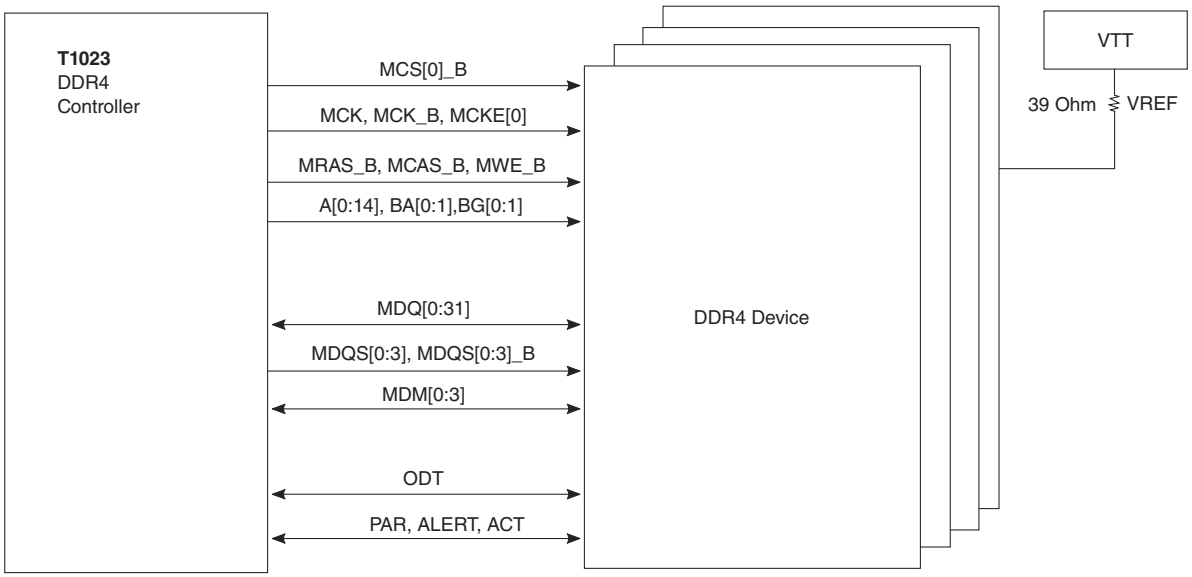


Figure 2-3. DDR4 SDRAM connection

NOTE

DQ swap across nibbles is not allowed.

2.6 Termination

The DDR4 address, control, and command signals are terminated to the VTT rail through 39 Ohm resistor.

2.7 SerDes interfaces (PCIe/SGMII/SATA)

T1023 processor supports the SGMII, 2.5G SGMII and PCI Express high-speed I/O interface standards. The table below details the SerDes connections.

Table 2-1. SerDes1 connectivity

SerDes Lane	Mode	Connected to	Comment
Lane A	PCI Express 1	Mini-PCIe slot	Used for WLAN type cards
Lane C	PCI Express 2	Mini-PCIe slot	Used for WLAN type cards
Lane B	2.5G SGMII	AQR105 PHY	
Lane D	1G SGMII	Realtek SGMII PHY	

2.7.1 PCI Express support

On the RDB, lanes A and C are configured as two independent x1 PCI Express interfaces. These interfaces are compliant with the PCI Express Base Specification Revision 2.0. The physical layer of the PCI Express interface operates at a transmission rate of 3.125 Gbaud (data rate of 2.5 Gbit/s) per lane. The theoretical unidirectional peak bandwidth is 2.5 Gbit/s per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 5 Gbit/s per lane. It supports Root complex (RC) and End point (EP) configurations.

2.7.2 SGMII support

On the T1023RDB-PC, lane B of SerDes are used in 2.5G SGMII mode and lane D are in 1G SGMII mode. The Serial gigabit media independent interface (SGMII) is a high-speed interface linking the Ethernet controller with an Ethernet PHY. SGMII uses differential signalling for electrical robustness. Only four signals are required: receive data and its inverse, and send data and its inverse.

2.7.3 SerDes clock

The clocking for the SerDes interface is 100 MHz for SerDes PLL1 and 125 MHz for SerDes PLL2, both are provided by the 5P49V5901A616NLGI clock chip.

2.8 EC1 10/100/1000 BaseT interface (ETH1)

EC1 is set to operate in RGMII mode. It connects to a Realtek RGMII PHY (RTL8211FS), as shown in the below figure.

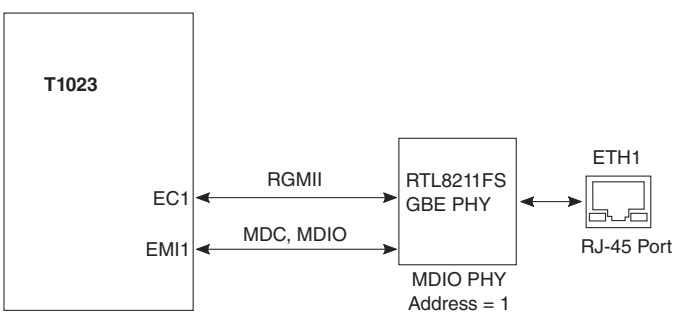


Figure 2-4. RGMII interface connection

2.9 SerDes lane D 10/100/1000 BaseT interface (ETH2)

SerDes lane D is set to operate in SGMII and is directly connected to the RealTek SGMII PHY(RTL8211FS), as shown in the below figure.

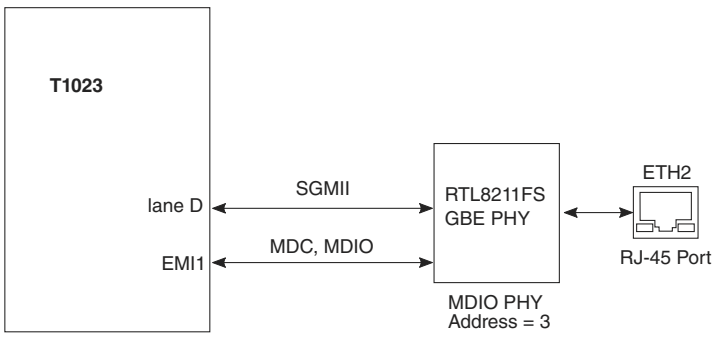


Figure 2-5. SGMII interface connection

2.10 SerDes lane B 2.5G BaseT interface (ETH3)

SerDes lane B is set to operate in 2.5G SGMII and is directly connected to the AQR105 PHY, as shown in the below figure.

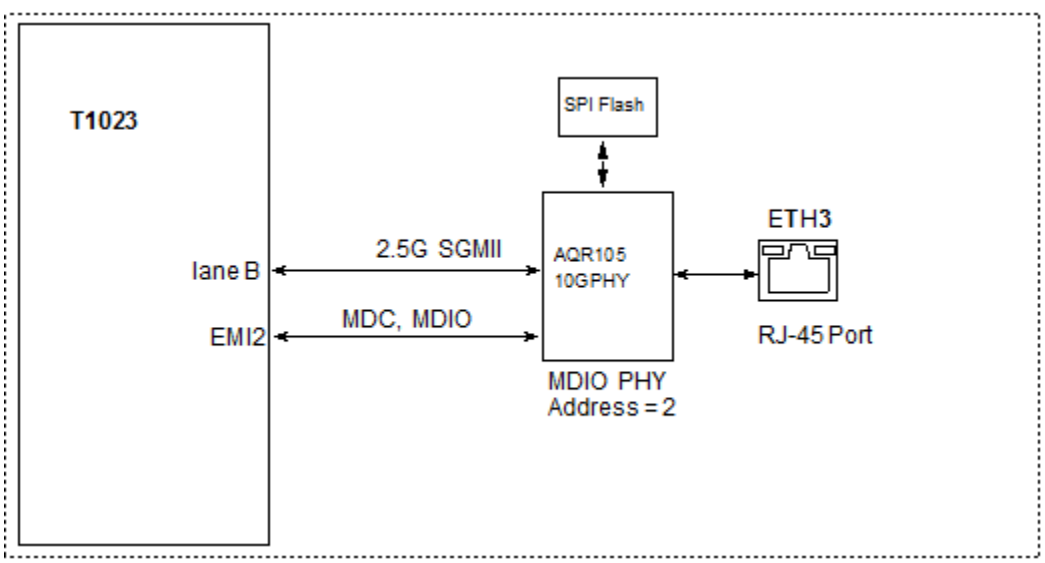


Figure 2-6. SGMII interface connection

2.11 Ethernet management

The table below details how the MDC and MDIO connections are made on the RDB.

Table 2-2. MDC/MDIO connectivity

Device	PHY address
EC1/RGMII PHY	00001
AQR105 PHY	00010
SGMII PHY	00011

2.12 Ethernet ports

The figure below shows how the Ethernet ports are connected on the backside of the RDB chassis. ETH3 (PoE) port is same as the PoE power port.

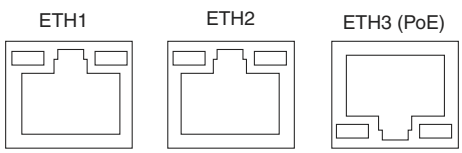


Figure 2-7. Ethernet port connection

2.13 I2C

The T1023 device has two I2C controllers. On the RDB, the I2C buses are connected as shown below. The M24256 serial EEPROM can be used to store configuration registers' values.

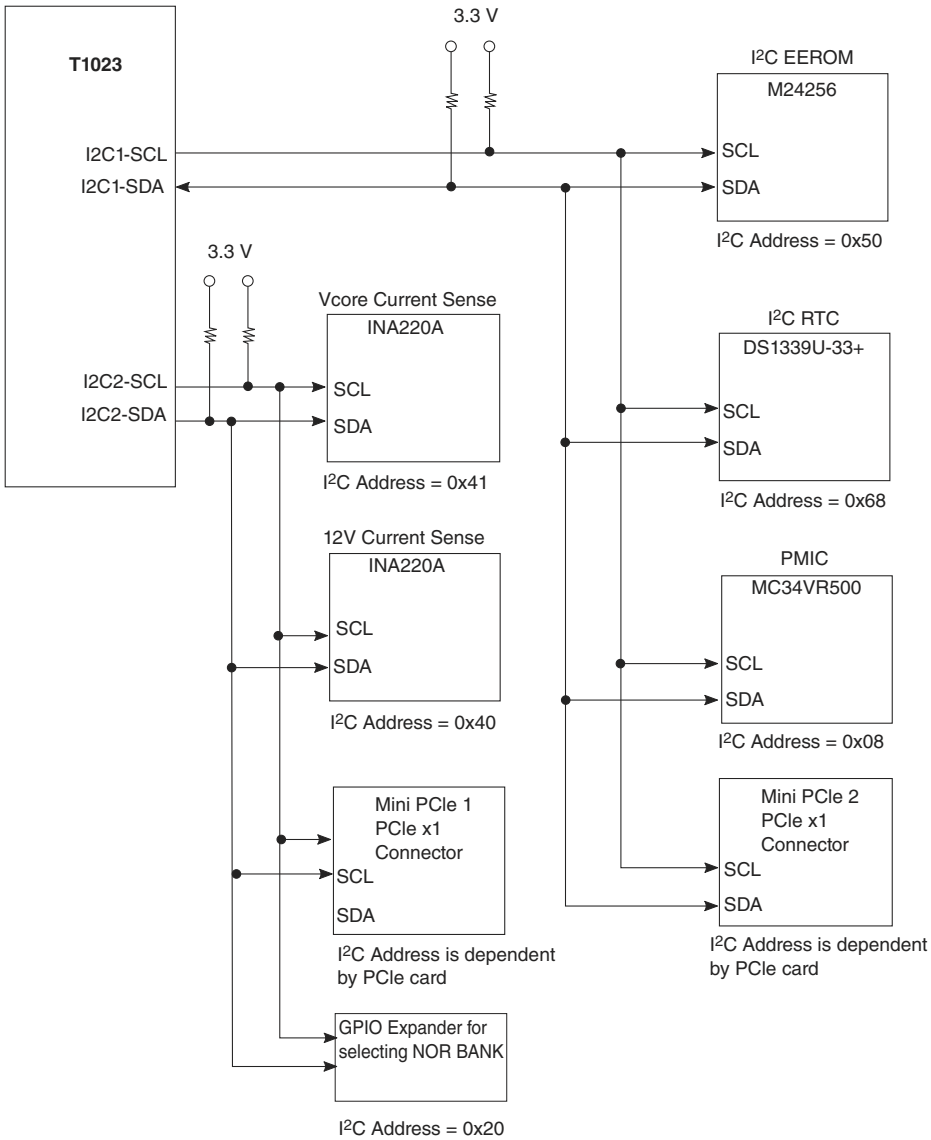


Figure 2-8. I2C subsystem

The table below shows all the I2C device and address information on T1023RDB-PC.

Table 2-3. I2C Bus connections

I2C Bus	I2C Address	Manufacturer	Device	Comment
I2C1	0x50	ST Microelectronics	M24256	Stores configuration register's value
I2C1	0x68	Dallas	DS1339U-33+	Real time clock
I2C1	0x08	Freescale	MC34VR500	PMIC
I2C1			Mini PCIe 2 PCIe x1 Connector	I2C address is dependent on PCIe card
I2C2	0x41	Linear	INA220A	core current measurement

Table continues on the next page...

Table 2-3. I2C Bus connections (continued)

I2C Bus	I2C Address	Manufacturer	Device	Comment
I2C2	0x40	Linear	INA220A	12 V current measurement
I2C2		Linear	Mini PCIe 1 PCIe x1 Connector	I2C address is dependent on PCIe card
I2C2	0x20	NXP	PCA6408APW	GPIO expander for selecting NOR bank

2.14 IFC

The Integrated flash controller (IFC) is used to access the external NAND flash and NOR flash. To interface with the standard memory device, an address latch is needed on the upper address bits since they are multiplexed with the data bus. The IFC_AVD is used as the latching signal. The following modules are connected to the IFC:

- 128 MB NOR flash memory
- 512 MB NAND flash memory

NOTE

Silicon IFC_NOR 28 bit addressing mode is not functional with Asynchronous non-ADM NOR. For more details, see *A-009138: IFC_NOR 28/25 addressing mode is not functional for T1023 with Asynchronous, Non-ADM NOR* errata document.

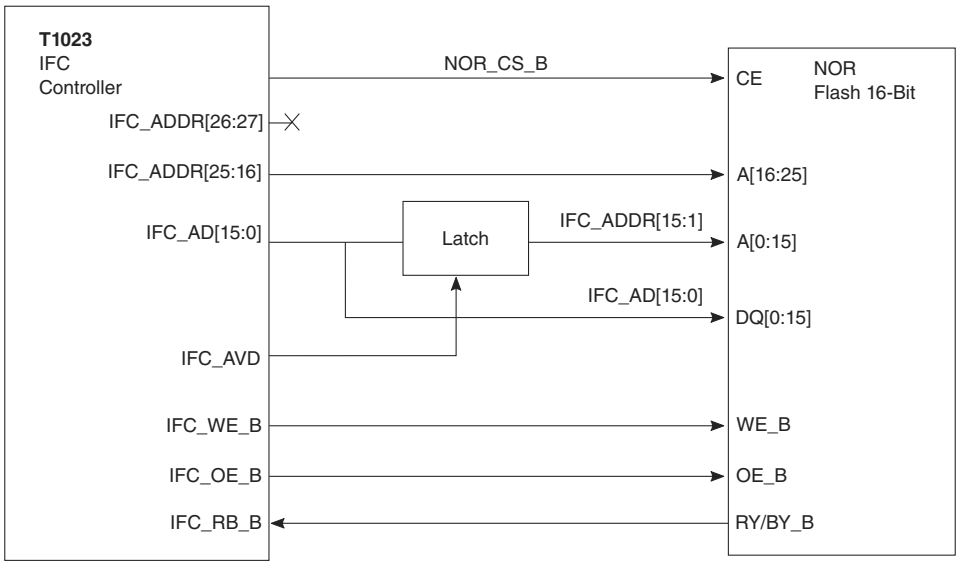
2.14.1 NOR flash memory

T1023RDB-PC provides 128 MB of NOR flash memory. The flash memory used is configured in a 16-bit port size. The NOR flash memory is divided in to 8 banks. By default, only bank0 and bank4 are supported to swap in U-Boot by using the following commands:

```
switch bank0

switch bank4
```

The below figure shows the hardware connections for the flash memory.

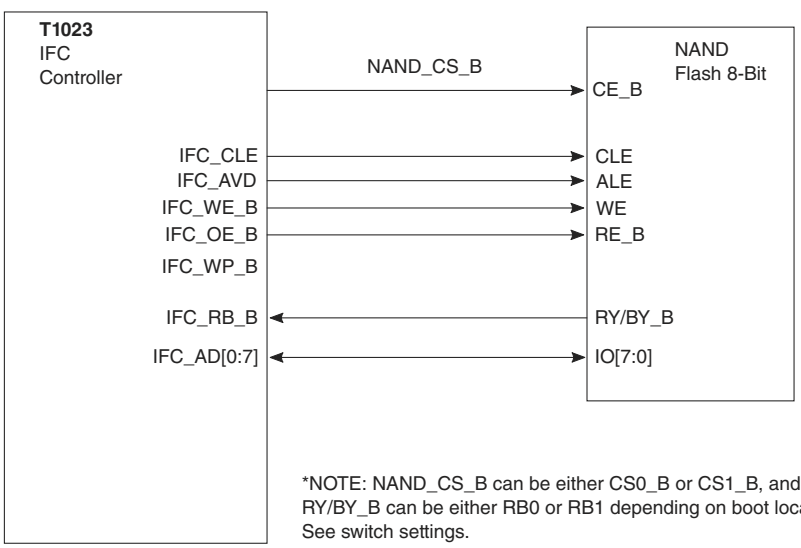


*NOTE: NOR_CS_B can be either CS0_B or CS1_B, and RY/BY_B can be either RB0 or RB1 depending on boot location. See switch settings.

Figure 2-9. NOR flash memory connection

2.14.2 NAND flash memory

The T1023 device has native support for NAND flash memory through its NAND Flash control machine (FCM). The T1023RDB-PC implements an 8-bit NAND flash with 512 MB in size. The figure below shows the NAND flash memory connection.



*NOTE: NAND_CS_B can be either CS0_B or CS1_B, and RY/BY_B can be either RB0 or RB1 depending on boot location. See switch settings.

Figure 2-10. NAND flash memory connection

The table below summarizes the IFC connectivity.

Table 2-4. IFC connectivity

IFC chip select	Manufacturer	Device	Comment
IFC_CS0 or IFC_CS1 assignment dependent on SW3[4]	Spansion	S29GL01GS11TFIV10	NOR flash memory 128 MB (16-bit)
IFC_CS0 or IFC_CS1 assignment dependent on SW3[4]	Spansion	S34MS04G200BHI000	NAND flash 512 MB (8-bit)

2.15 eSPI interface

The eSPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The T1023 device has the ability to boot from a SPI serial flash device in addition to supporting other peripheral devices conforming to the SPI standard.

On the T1023RDB, a Spansion SPI flash memory is supported. The table below details the eSPI connection.

Table 2-5. eSPI connection

eSPI chip select	Manufacturer	Part #	Comment
SPI_Flash_CS0_N	Spansion	S25FL512SAGMFI010	64 MB Spansion SPI flash (default)

2.16 eSDHC interface

The enhanced SD host controller (eSDHC) provides an interface between host system and SD/MMC cards. The Secure digital (SD) card is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in emerging audio and video consumer electronic devices. Booting from eSDHC interface is supported through on-chip ROM of processor.

On the T1023RDB, SD/MMC and eMMC are both supported, as shown in the below figure. The SW3[3] and GPIO1_14 are used to switch between eMMC and SD/MMC card. Use the U-Boot commands `switch sd` or `switch emmc` to switch SD/MMC card and eMMC.

NOTE

Boot from eMMC will be supported in the next SDK release.

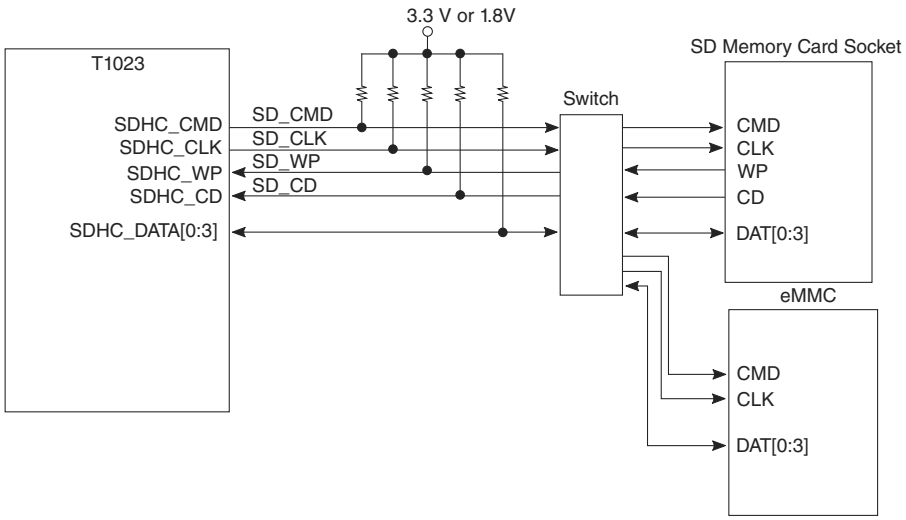


Figure 2-11. SD memory card/eMMC connection

2.17 GPIO interface

The table below lists the GPIO pin usage on the RDB platform.

Table 2-6. GPIO pin usage

GPIO	Input/Output	Signal name	Comment
GPIO1_14	output	GPIO1_14_eMMC_SEL_n	0: Select eMMC; 1: Select SD/MMC card
GPIO3_04	input		Board version identifying bit 1; Rev B= 0, Rev C= 0, Rev D= 1, Rev E= 1
GPIO3_05	input		Board version identifying bit 0; Rev B= 0, Rev C= 1, Rev D= 0, Rev E= 1
PCIe 2 card wake	GPIO3_02	GPIO3_2_WAKE_L	

2.18 Interrupts

The figure below shows the external interrupts to the T1023.

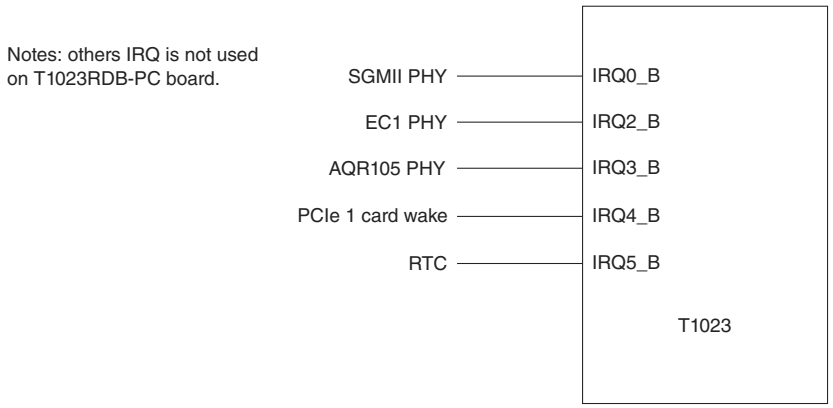


Figure 2-12. T1023 interrupts

The table below details how the interrupts are connected on the RDB platform.

Table 2-7. Interrupts

Name	Connection	Note
IRQ0	SGMII PHY RTL8211FS	On-board Pull-up
IRQ2	EC1 RGMII PHY	On-board Pull-up
IRQ3	AQR105 PHY	On-board Pull-up
IRQ4	PCIe 1 card wake	On-board Pull-up
IRQ5	RTC	On-board Pull-up

2.19 USB interface

On T1023RDB-PC, there is one USB interface and the USB PHY is integrated in the T1023 device.

The board features are:

- Complies with USB Specification Rev 2.0
- High-speed (480 MB/s), full-speed (12 MB/s) and low-speed (1.5 MB/s) operation, low speed is only supported in host mode
- On-chip USB 2.0, full-speed/high-speed PHY with UTMI
- Support operation as a standalone USB host controller
- Support operation as a standalone USB device
- One Type A USB connector

The figure below shows how the USB connectivity is implemented on the RDB.

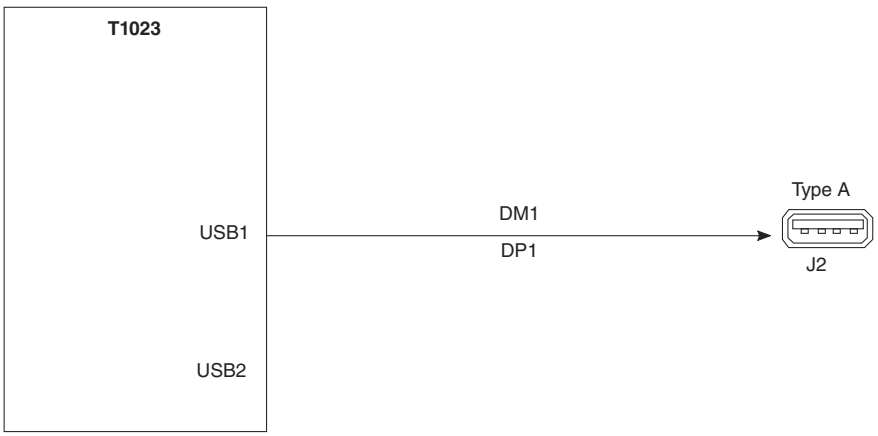


Figure 2-13. USB interface

2.20 RS-232

The T1023 device has two UART controllers and only UART1 is used on the board.The RS-232 interface provides an RS-232 standard interconnection between the card and an external host. The serial connection is configured to run at 115.2 KB/s.

UART supports:

- Full-duplex operation
- Software-programmable baud generators
  - Divide the platform clock/2 by 1 to (2^16 -1)
  - Generate a 16x clock for the transmitter and receiver engines
- Clear-to-send (CTS) and Ready-to-send (RTS) modem control functions
- Software-selectable serial interface data format that includes:
  - Data length
  - Parity
  - 1/1.5/2 STOP bit
  - Baud rate
- Overrun, parity, and framing error detection

The UART1 are routed to a RJ-45 connectors P1, as shown in the below figure.

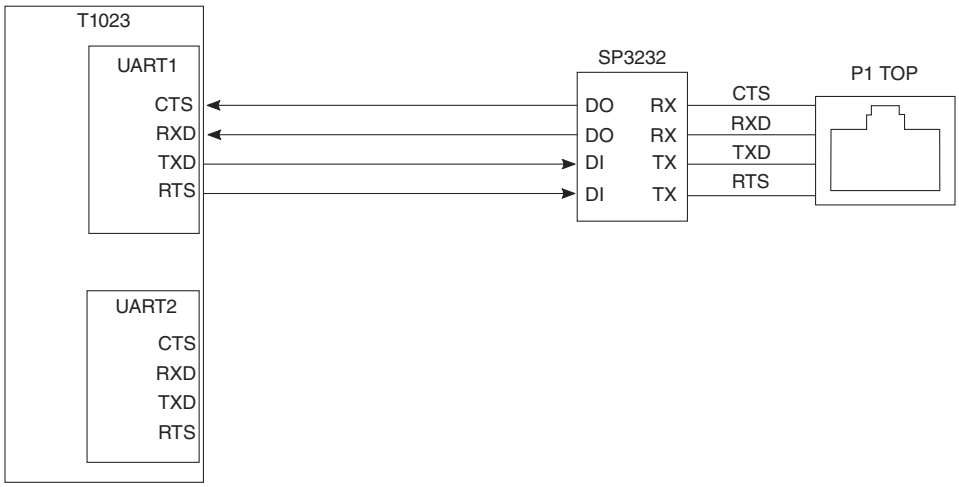


Figure 2-14. RS-232 ports connection

The below table shows the connection settings for the UART RJ-45 connector to the DB9 female cable connection.

Table 2-8. RJ45 to DB9 connection settings

RJ-45 pin number	RS-232 signal	DB9 female pin number
1	RTS	8
2	NC	
3	TXD	2
4	GND	5
5	GND	5
6	RXD	3
7	NC	
8	CTS	7

2.21 POR configuration

The POR configuration is based on switch setting. When Power-on reset (POR) is asserted, the RCW source POR configuration input are sampled to determine the configuration source. Then the device starts loading the RCW data. Negate the POR when the required assertion or hold time is met (the minimum value is 1 ms). On this board, MAX811 asserts the POR for 110 ms.

2.22 JTAG/COP port

The JTAG connection is provided by a direct connection to the appropriate header connector. The Common on-chip processor (COP) is part of the T1023 processor's JTAG module, and it is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the Ethernet port, USB port, parallel port, or RS-232. A setup using a USB port emulator is shown in the below figure.

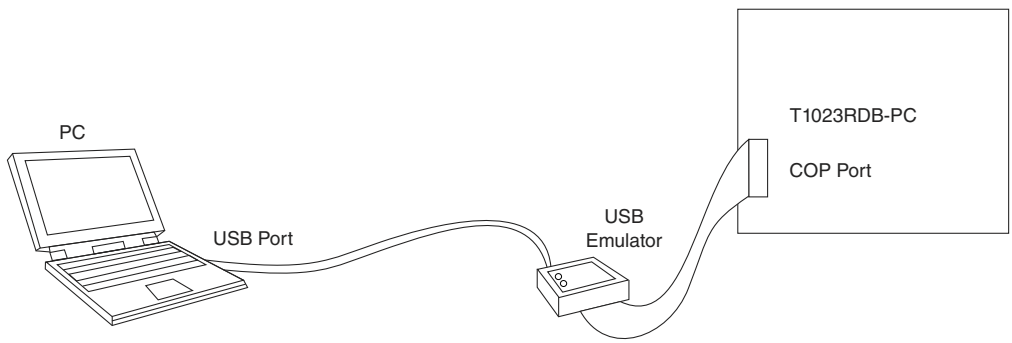


Figure 2-15. USB port emulator setup

The 16-pin generic header connector carries the COP/JTAG signals and connect T1023 using level shift and the additional signals for system debugging. The pin-out of this connector is shown in the below figure.

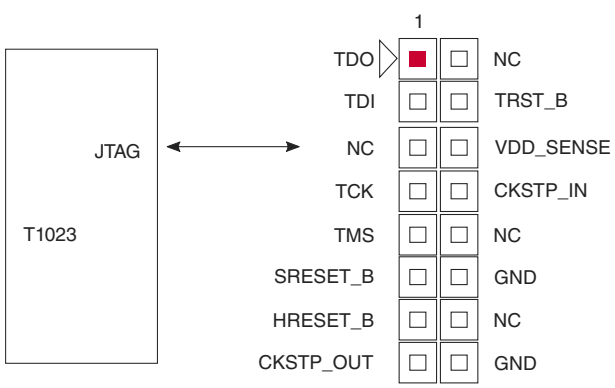


Figure 2-16. RDB COP connector

The table below displays the connections made from the T1023RDB COP connector.

Table 2-9. T1023RDB COP connector

Pin number	Signal name	Connection
1	TDO	Connected directly between the processor and JTAG/COP connector.
2	NC	Not connected.
3	TDI	Connected directly between the processor and JTAG/COP connector.

Table continues on the next page...

Table 2-9. T1023RDB COP connector (continued)

Pin number	Signal name	Connection
4	TRST	Connected between the processor and JTAG/COP connector.
5	NC	Not connected.
6	VDD_SENSE	Pulled to 3.3 V using a 10 Ohm resistor.
7	TCK	Connected directly between the processor and JTAG/COP connector.
8	CKSTP_IN	Connected directly between the processor and JTAG/COP connector.
9	TMS	Connected directly between the processor and JTAG/COP connector.
10	NC	Not connected.
11	SRESET	Connected between the processor and JTAG/COP connector.
12	GND	Connected to ground.
13	HRESET	Connected between the processor and JTAG/COP connector.
14	NC	Not connected.
15	CKSTP_OUT	Connected directly between the processor and JTAG/COP connector.
16	GND	Connected to ground.

NOTE

J28 should be uninstalled while using JTAG at blank NOR boot mode.

2.23 DMA

The DMA function itself is not utilized on the RDB platform. All the DMA pins are multiplex with the SDHC pins.

2.24 Connectors, Headers, Push buttons, and LEDs

This section explains:

- Connectors
- Headers
- Push buttons
- LEDs

2.24.1 Connectors

The below table lists the various connectors on the T1023RDB platform.

Table 2-10. Connectors on T1023RDB platform

Reference designators	Used for	Notes
J16	SD/MMC Card	SD/MMC card socket
J2	USB_Type A	USB1 internal UTMI PHY
P1	UART port	UART 1
J4	ETH1	EC1 RGMII PHY
J5	ETH2	SGMII PHY
J3	ETH3	2.5G SGMII PHY
P2	mini-PCIe 1	WiFi card
P3	mini-PCIe 2	WiFi card

The board contains an RTC that requires a battery in order to maintain the data inside the RTC. The battery holder (BT1) accommodates a CR-2032. The below figure shows how to insert a battery.

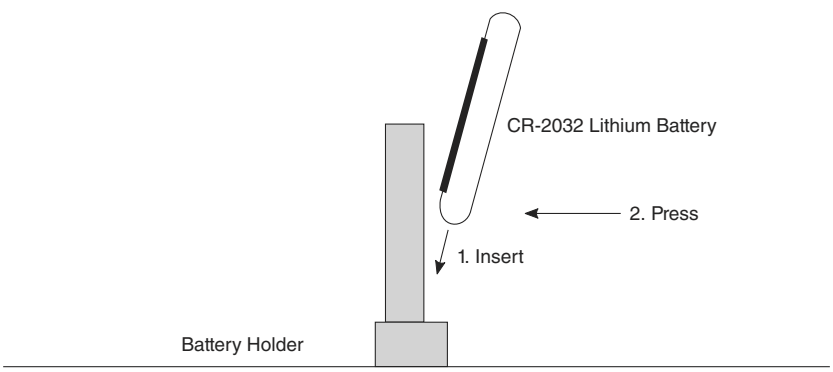


Figure 2-17. Battery installation

2.24.2 Headers

The below table lists the various headers on the T1023RDB platform.

Table 2-11. Headers on T1023RDB platform

Reference designators	Used for	Setting
J9	Fan Header	For socket fan
J6	Remote RESET	Connect cable to chassis
J1	JTAG/COP	Used for PowerPC JTAG

Table continues on the next page...

Table 2-11. Headers on T1023RDB platform (continued)

Reference designators	Used for	Setting
J18	DCDC1_3V3	1-2: Turn OFF PCIe 2 and ETH2 3.3 V power, if 12 V adapter is not present. [Default] 2-3: Always ON
J19	LDO_2V1	1-2: Turn OFF AQR105 2.1 V power, if 12 V adapter is not present. 2-3: Always ON [Default]
J20	DCDC_5V0	1-2: Turn OFF USB power, if 12 V adapter is not present. 2-3: Always ON [Default]
J21	DCDC_V85	1-2 Turn OFF AQR105 PHY power supply, if 12 V adapter is not present. 2-3: Always ON [Default]
J23	VPA	1-2: Always turned ON for PCIe1 card PA power [Default] 2-3: Turn OFF PCIe 1 card PA power
J26	VPA_PCIE2	2-3: Turn OFF PCIe 2 PA power, if 12 V adapter not present. 1-2 Always ON [Default]
J25	PCIe1 PA power setting	1-2: 5 V, CUS239 [Default] 3-4: 4.5 V, CUS260 5-6: 3.5 V, CUS238 7-8: 3.3 V, CUS240
J27	PCIe2 PA power setting	1-2: 5 V, CUS239 [Default] 3-4: 4.5 V, CUS260 5-6: 3.5 V, CUS238 7-8: 3.3 V, CUS240
J28	JTAG TRST	By default it is installed; but needs to uninstall it for JTAG connectivity, when board is set to NOR boot and RCW is not programmed to NOR.

2.24.3 Push buttons

The following table describes how the push buttons are used on the T1023RDB platform.

Table 2-12. Push buttons on T1023RDB platform

Reference designators	Used for	Notes
SW4	Reset	Used for resetting the whole board

2.24.4 LEDs

The below table lists all the LEDs on the T1023RDB front plate.

Table 2-13. LEDs on the T1023RDB front plate

Description	Reference designators	Color for	LED ON	LED OFF
12 V Power	D11	Green	12 V Power ON	12 V Power OFF
3.3 V Power	D15	Green	3.3 V Power ON	3.3 V Power OFF
Status	D18	Yellow	LED is always ON, the board boot fails	LED is turned ON for less than 1 second at power ON and then OFF. The board boots normally.

2.25 Switch settings

The RDB has user selectable switches for evaluating different frequency and boot options for the T1023 device.

2.25.1 T1023RDB-PC RCW source configuration (using switches)

The below table lists options for RCW source configuration.

Table 2-14. T1023RDB-PC RCW source configuration options

SW1[1:8], SW2[1]	cfg_rcw_src[0:8]	RCW source	Remark
ON ON ON OFF ON OFF OFF OFF, OFF	000101111	16-bit NOR, provides up to 28b addressability	For NOR flash boot, except the RCW source settings, also set SW3.4 to ON to assign CS0 and RB0 to NOR flash.
ON ON OFF ON ON ON ON ON, ON	001000000	SD/MMC	
ON ON OFF ON ON ON OFF ON, OFF	001000101	SPI 24-bit addressing	
OFF ON ON ON ON ON OFF ON, ON	100000101	8-bit NAND, 2 KB page, 64 pages/block	For NAND flash boot, except the RCW source settings, also set SW3.4 to OFF to assign CS0 and RB0 to NAND.

2.25.2 Switches configuration options

The below table lists all configuration options of the switches (SW2-4) that are available on the board.

Table 2-15. Switches configuration options

Switch	Signal name	Reset configuration name	Function	Default
SW1[1:8] SW2[1]	IFC_AD[8:15] IFC_CLE	cfg_rcw_src[0:8]	See QorIQ T1024 Reference Manual Rev. A, Table 4-21 RCW source encodings	000101111 NOR Boot
SW2[2]	IFC_TE	cfg_ifc_te	IFC extenal transceiver enable polarity select. set bit 0 to drive logic 1 for TE assertion; set bit 1 to drive logic 0 for TE assertion	1
SW2[3]	IFC_A18	cfg_pll_config_sel_b	This pin must be pull high during power on reset	1
SW2[4]	IFC_A19	cfg_por_ainit	Unused	1
SW2[5]	IFC_A16	cfg_svr0		1
SW2[6]	IFC_A17	cfg_svr1		1
SW2[7]	unused			
SW2[8]	IFC_AVD	cfg_rsp_dis	Unused, default set bit to 1	1
SW3[1]	IFC_OE_N	cfg_eng_use1	Set system clock input type. Set 0 for differential clock; set 1 for single clcok	1
SW3[2]	IFC_WP_N	cfg_eng_use2	Unused	1
SW3[3]	GPIO1_14_eMMC_SEL_n		SD/eMMC selection	0 eMMC selected
SW3[4]	NAND_BOOT_SEL		Switch CS/RB between NOR and NAND, if boot source is changed. NOR/NAND boot selection	0 NOR boot CS0/RB0 to NOR
SW3[5]	IFC_A25_INVERT		Set 1 to invert the IFC address A25	0
SW3[6]	IFC_A24_INVERT		Set 1 to invert the IFC address A24	0
SW3[7]	IFC_A23_INVERT		Set 1 to invert the IFC address A23	0
SW3[8]	TEST_SEL_N		Set 0 enable single core; set 1 enable dual core	1

NOTE

Switch ON: 0; Switch OFF: 1

Appendix A
Revision history

The below table summarizes the revisions to this document.

Table A-1. Revision history

Revision	Date	Topic cross-reference	Change description
Rev 0	08/2015		Initial Public Release.

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