DATA SHEET

TDA8002C
IC card interface

Product specification
Supersedes data of 1999 Feb 24
File under Integrated Circuits, IC02

1999 Oct 12

Philips
Semiconductors

PHILIPS

FEATURES

- Single supply voltage interface (3.3 or 5 V environment)
- Low-power sleep mode
- Three specific protected half-duplex bidirectional buffered I/O lines
- V_{CC} regulation 5 V ±5% or 3 V ±5%, I_{CC} < 55 mA for V_{DD} = 3.0 to 6.5 V, with controlled rise and fall times
- Thermal and short-circuit protections with current limitations
- Automatic ISO 7816 activation and deactivation sequences
- Enhanced ESD protections on card side (>6 kV)
- Clock generation for the card up to 12 MHz with synchronous frequency changes
- Clock generation up to 20 MHz (external clock)
- Synchronous and asynchronous cards (memory and smart cards)
- ISO 7816, GSM11.11 compatibility and EMV (Europay, MasterCard® and Visa) compliant
- Step-up converter for V_{CC} generation
- Supply supervisor for spikes elimination and emergency deactivation
- Chip select input for easy use of several TDA8002Cs in parallel.

APPLICATIONS

IC card readers for:

- GSM applications
- Banking
- Electronic payment
- Identification
- Pay TV
- Road tolling.

GENERAL DESCRIPTION

The TDA8002C is a complete low-power analog interface for asynchronous and synchronous cards. It can be placed between the card and the microcontroller. It performs all supply, protection and control functions. It is directly compatible with ISO 7816, GSM11.11 and EMV specifications.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	MARKING	NAME	DESCRIPTION	VERSION
TDA8002CT/A/C1	TDA8002CT/A	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA8002CT/B/C1	TDA8002CT/B			
TDA8002CT/C/C1	TDA8002CT/C			
TDA8002CG/C1	TDA8002C	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		3.0	–	6.5	V
$I_{DD(lp)}$	supply current	low-power	–	–	150	µA
$I_{DD(idle)}$	supply current	Idle mode; f_{CLKOUT} = 10 MHz	–	–	5	mA
$I_{DD(active)}$	supply current	active mode; $V_{CC(O)}$ = 5 V; f_{CLKOUT} = 10 MHz				
		f_{CLK} = LOW; I_{CC} = 100 µA	–	–	8	mA
		f_{CLK} = 5 MHz; I_{CC} = 10 mA	–	–	50	mA
		f_{CLK} = 5 MHz; I_{CC} = 55 mA	–	–	140	mA
		active mode; $V_{CC(O)}$ = 3 V; f_{CLKOUT} = 10 MHz				
		f_{CLK} = LOW; I_{CC} = 100 µA	–	–	8	mA
		f_{CLK} = 5 MHz; I_{CC} = 10 mA	–	–	50	mA
		f_{CLK} = 5 MHz; I_{CC} = 55 mA	–	–	140	mA
Card supply						
$V_{CC(O)}$	output voltage	active mode for V_{CC} = 5 V				
		I_{CC} < 55 mA; DC load	4.6	–	5.4	V
		I_{CC} = 40 nAs; AC load	4.6	–	5.4	V
		active mode for V_{CC} = 3 V				
		I_{CC} < 55 mA; DC load	2.76	–	3.24	V
		I_{CC} = 40 nAs; AC load	2.76	–	3.24	V
General						
f_{CLK}	card clock frequency		0	–	12	MHz
t_{de}	deactivation sequence duration		60	80	100	µs
P_{tot}	continuous total power dissipation					
	TDA8002CT/x	T_{amb} = –25 to +85 °C	–	–	0.56	W
	TDA8002CG	T_{amb} = –25 to +85 °C	–	–	0.46	W
T_{amb}	ambient temperature		–25	–	+85	°C

BLOCK DIAGRAM

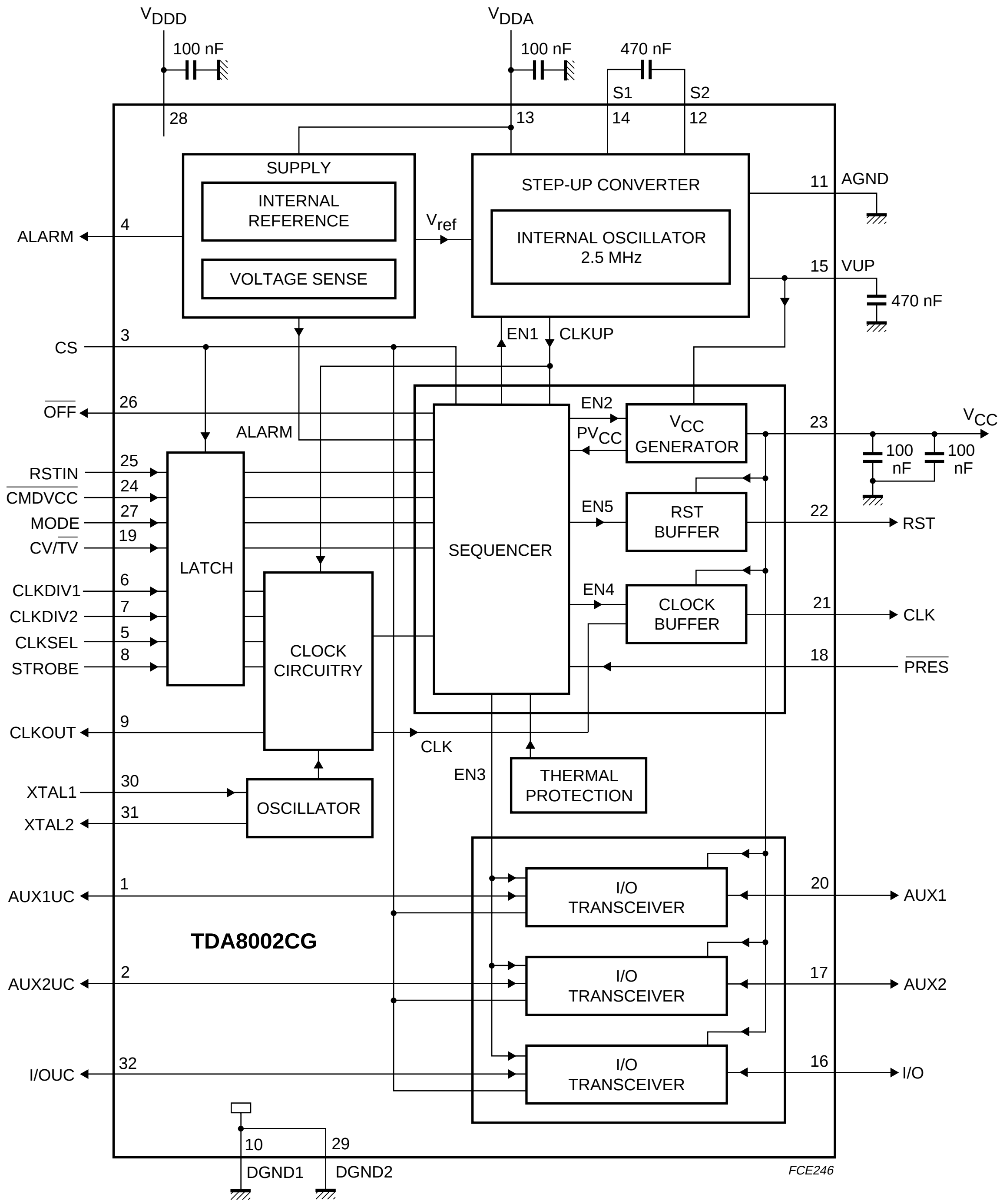


Fig.1 Block diagram.

PINNING

SYMBOL	PIN				I/O	DESCRIPTION
	TYPE CT/A	TYPE CT/B	TYPE CT/C	TYPE CG		
XTAL1	1	1	1	30	I	crystal connection or input for external clock
XTAL2	2	2	2	31	O	crystal connection
I/OUC	3	3	3	32	I/O	data I/O line to and from microcontroller
AUX1UC	4	4	4	1	I/O	auxiliary line 1 to and from microcontroller for synchronous applications
AUX2UC	5	–	–	2	I/O	auxiliary line 2 to and from microcontroller for synchronous applications
CS	–	5	5	3	I	chip select control input for enabling pins I/OUC, AUX1UC, AUX2UC, CLKSEL, CLKDIV1, CLKDIV2, STROBE, CV/$\overline{\text{TV}}$, $\overline{\text{CMDVCC}}$, RSTIN, $\overline{\text{OFF}}$ and MODE; note 1
ALARM	6	6	6	4	O	open drain PMOS reset output for microcontroller (active HIGH)
CLKSEL	7	7	7	5	I	control input signal for CLK (LOW = XTAL oscillator; HIGH = STROBE input)
CLKDIV1	8	8	8	6	I	control input with CLKDIV2 for choosing CLK frequency
CLKDIV2	9	9	9	7	I	control input with CLKDIV1 for choosing CLK frequency
STROBE	10	10	10	8	I	external clock input for synchronous applications
CLKOUT	11	11	11	9	O	clock output (see Table 1)
DGND1	12	12	12	10	supply	digital ground 1
AGND	13	13	13	11	supply	analog ground
S2	14	14	14	12	I/O	capacitance connection for voltage doubler
V_{DDA}	15	15	15	13	supply	analog supply voltage
S1	16	16	16	14	I/O	capacitance connection for voltage doubler
VUP	17	17	17	15	I/O	output of voltage doubler
I/O	18	18	18	16	I/O	data I/O line to and from card
AUX2	19	–	–	17	I/O	auxiliary I/O line to and from card
$\overline{\text{PRES}}$	20	19	19	18	I	card input presence contact (active LOW)
PRES	–	20	–	–	I	active HIGH card input presence contact
CV/$\overline{\text{TV}}$	–	–	20	19	I	card voltage selection input line (high = 5 V, low = 3 V); note 1
AUX1	21	21	21	20	I/O	auxiliary I/O line to and from card
CLK	22	22	22	21	O	clock to card output (C3I) (see Table 1)
RST	23	23	23	22	O	card reset output (C2I)
V_{CC}	24	24	24	23	O	supply for card (C1I)
$\overline{\text{CMDVCC}}$	25	25	25	24	I	start activation sequence input from microcontroller (active LOW)
RSTIN	26	26	26	25	I	card reset input from microcontroller
$\overline{\text{OFF}}$	27	27	27	26	O	open-drain NMOS interrupt output to microcontroller (active LOW)

SYMBOL	PIN				I/O	DESCRIPTION
	TYPE CT/A	TYPE CT/B	TYPE CT/C	TYPE CG		
MODE	28	28	28	27	I	operating mode selection input (HIGH = normal; LOW = sleep)
V_{DDD}	–	–	–	28	supply	digital supply voltage
DGND2	–	–	–	29	supply	digital ground 2

Note

1. A pull-up resistor of 100 kΩ connected to V_{DD} is integrated.

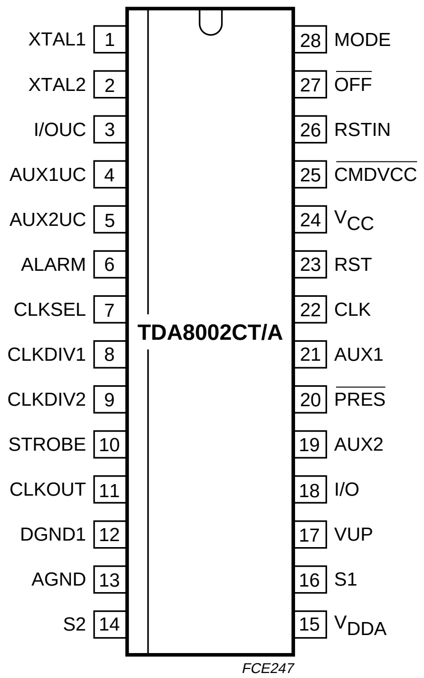


Fig.2 Pin configuration (TDA8002CT/A).

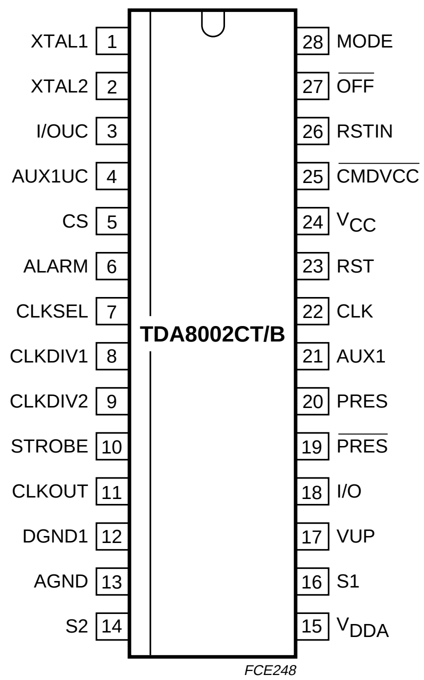


Fig.3 Pin configuration (TDA8002CT/B).

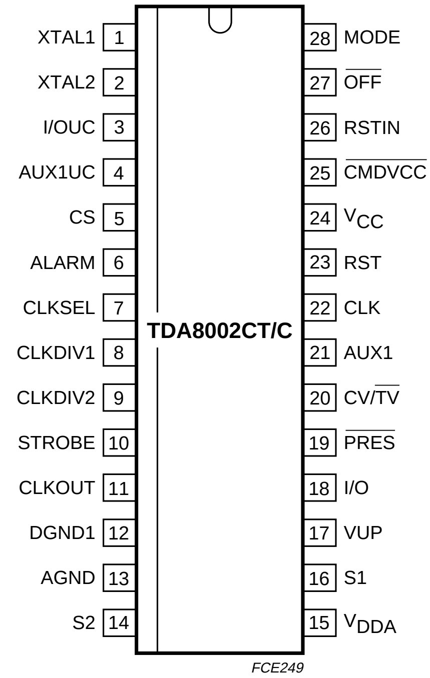


Fig.4 Pin configuration (TDA8002CT/C).

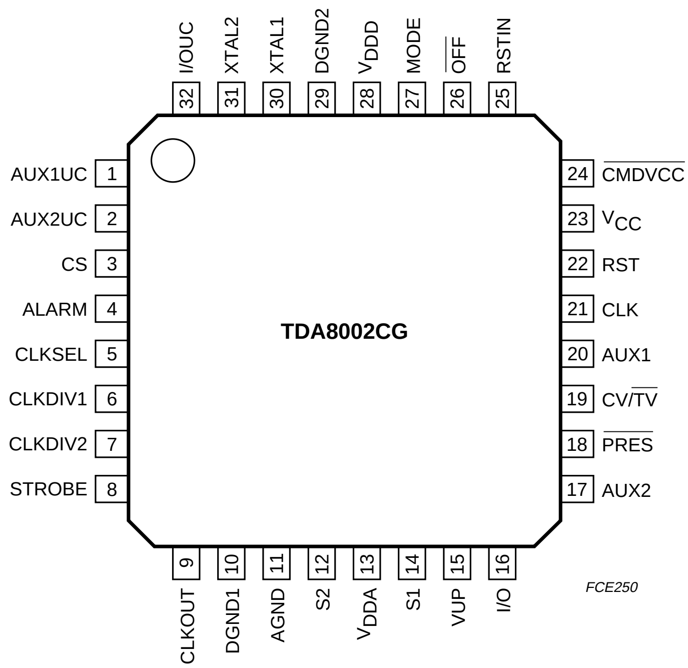


Fig.5 Pin configuration (TDA8002CG).

FUNCTIONAL DESCRIPTION

Power supply

The supply pins for the chip are V_{DDA}, V_{DDD}, AGND, DGND1 and DGND2. V_{DDA} and V_{DDD} (i.e. V_{DD}) should be in the range of 3.0 to 6.5 V. All card contacts remain inactive during power-up or power-down.

On power-up, the logic is reset by an internal signal. The sequencer is not activated until V_{DD} reaches $V_{th2} + V_{hys2}$ (see Fig.6). When V_{DD} falls below V_{th2}, an automatic deactivation sequence of the contacts is performed.

Chip selection

The chip select pin (CS) allows the use of several TDA8002Cs in parallel.

When CS is HIGH, the pins RSTN, $\overline{\text{CMDVCC}}$, MODE, CV/$\overline{\text{TV}}$, CLKDIV1, CLKDIV2, CLKSEL and STROBE control the chip, pins I/OUC, AUX1UC and AUX2UC are the copy of I/O, AUX1 and AUX2 when enabled (with integrated 20 kΩ pull-up resistors connected to V_{DD}) and $\overline{\text{OFF}}$ is enabled.

When CS goes LOW, the levels on pins RSTIN, $\overline{\text{CMDVCC}}$, MODE, CV/$\overline{\text{TV}}$, CLKDIV1, CLKDIV2 and STROBE are internally latched, I/OUC, AUX1UC and AUX2UC go to high-impedance with respect to I/O, AUX1 and AUX2 (with integrated 100 kΩ pull-up resistors connected to V_{DD}) and $\overline{\text{OFF}}$ is high-impedance.

Supply voltage supervisor (V_{DD})

This block surveys the V_{DD} supply. A defined retriggerable pulse of 10 ms minimum (t_W) is delivered on the ALARM output during power-up or power-down of V_{DD} (see Fig.6). This signal is also used for eliminating the spikes on card contacts during power-up or power-down.

When V_{DD} reaches $V_{th2} + V_{hys2}$, an internal delay (t_W) is started. The ALARM output is active until this delay has expired. When V_{DD} falls below V_{th2}, ALARM is activated and a deactivation sequence of the contacts is performed.

Clock circuitry

The TDA8002C supports both synchronous and asynchronous cards. There are three methods to clock the circuitry:

- Apply a clock signal to pin STROBE
- Use of an internal RC oscillator
- Use of a quartz oscillator which should be connected between pins XTAL1 and XTAL2 or an external clock applied on XTAL1.

When CLKSEL is HIGH, the clock should be applied to the STROBE pin. When CLKSEL is LOW, the internal oscillators is used.

When an internal clock is used, the clock output is available on pin CLKOUT. The RC oscillator is selected by making CLKDIV1 HIGH and CLKDIV2 LOW. The clock output to the card is available on pin CLK. The frequency of the card clock can be the input frequency divided by 2 or 4, STOP low or 1.25 MHz, depending on the states of CLKDIV1 or CLKDIV2 (see Table 1).

When STROBE is used for entering the clock to a synchronous card, STROBE should remain stable during activation sequence otherwise the first pulse may be omitted.

Do not change CLKSEL during activation. When in low-power (sleep) mode, the internal oscillator frequency which is available on pin CLKOUT is lowered to approximately 16 kHz for power economy purposes.

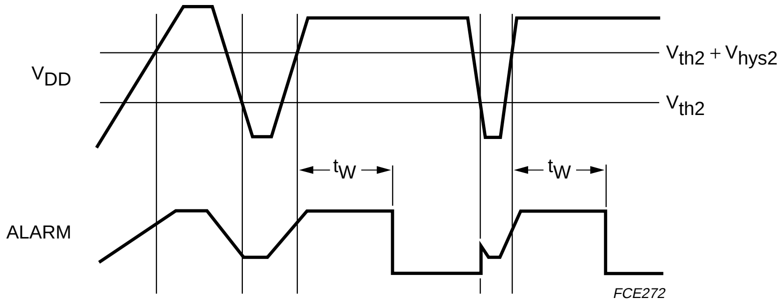


Fig.6 ALARM as a function of V_{DD} (t_W pulse width minimum of 10 ms).

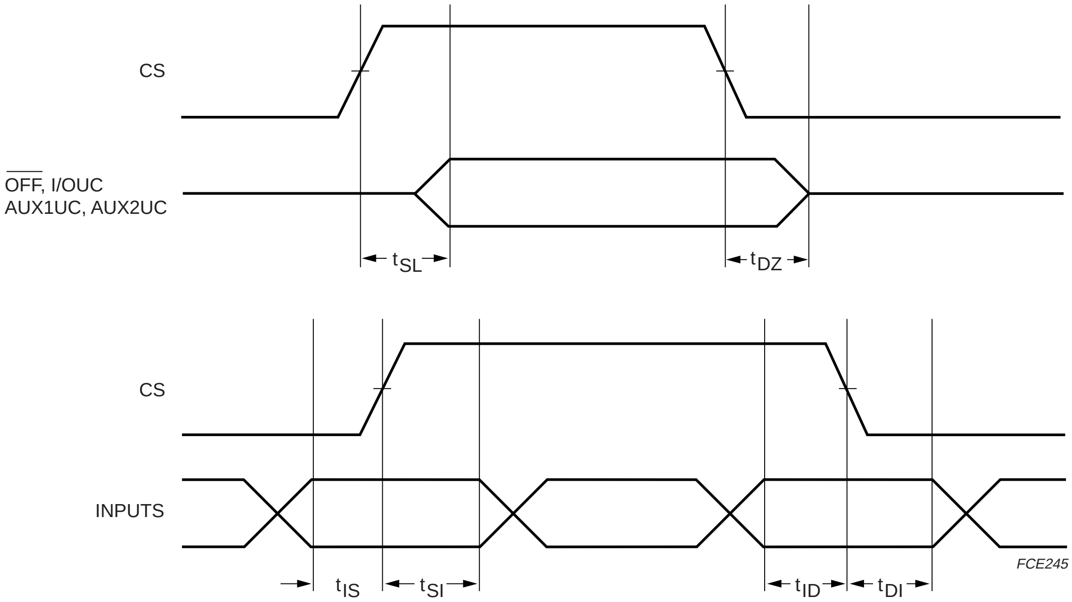


Fig.7 Chip select.

Table 1 Clock circuitry definition

MODE	CLKSEL	CLKDIV1	CLKDIV2	FREQUENCY OF CLK	FREQUENCY OF CLKOUT
HIGH	LOW	HIGH	LOW	$\frac{1}{2}f_{int}$	$\frac{1}{2}f_{int}$
HIGH	LOW	LOW	LOW	$\frac{1}{4}f_{xtal}$	f_{xtal}
HIGH	LOW	LOW	HIGH	$\frac{1}{2}f_{xtal}$	f_{xtal}
HIGH	LOW	HIGH	HIGH	STOP low	f_{xtal}
HIGH	HIGH	X(1)	X(1)	STROBE	f_{xtal}
LOW(2)	X(1)	X(1)	X(1)	STOP low	$\frac{1}{2}f_{int}$(3)

Notes

1. X = don't care.
2. In low-power mode.
3. f_{int} = 32 kHz in low-power mode.

I/O circuitry

The three I/O transceivers are identical. The state is HIGH for all I/O pins (i.e. I/O, I/OUC, AUX1, AUX1UC, AUX2 and AUX2UC). Pin I/O is referenced to V_{CC} and pin I/OUC to V_{DD}, thus ensuring proper operation in the event that $V_{CC} \neq V_{DD}$.

The first side on which a falling edge is detected becomes a master (input). An anti-latch circuitry first disables the detection of the falling edge on the other side, which becomes slave (output), see Fig.8.

After a delay time t_d (between 50 and 400 ns), the logic 0 present on the master side is transferred on the slave side.

When the input is back to HIGH level, a current booster is turned on during the delay t_d on the output side and then both sides are back to their idle state, ready to detect the next logic 0 on any side.

In the event of a conflict, both lines may remain LOW until the software enables the lines to be HIGH. The anti-latch circuitry ensures that the lines do not remain LOW if both sides return HIGH, regardless of the prior conditions. The maximum frequency on the lines is approximately 200 kHz.

When CS is HIGH, I/OUC, AUX1UC and AUX2UC are internally pulled-up to V_{DD} with 20 kΩ resistors. When CS is LOW, I/OUC, AUX1UC and AUX2UC are permanently HIGH (with integrated 100 kΩ pull-up resistors connected to V_{DD}).

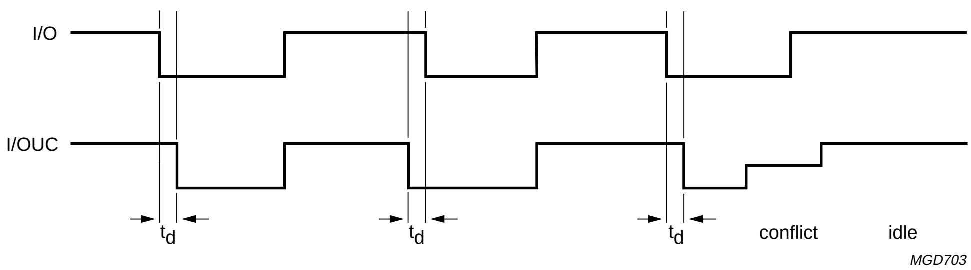


Fig.8 Master and slave signals.

Logic circuitry

After power-up, the circuit has six possible states of operation. Figure 9 shows the state diagram.

IDLE MODE

After reset, the circuit enters the idle mode. A minimum number of functions in the circuit are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- I/OUC, AUX1UC and AUX2UC are high-impedance
- Oscillator (XTAL) runs, delivering CLKOUT
- Voltage supervisor is active.

LOW-POWER MODE

When pin MODE goes LOW, the circuit enters the low-power (sleep) mode. As long as pin MODE is LOW no activation is possible.

If pin MODE goes LOW in the active mode, a normal deactivation sequence is performed before entering the low-power mode. When pin MODE goes HIGH, the circuit enters the normal operating mode after a delay of at least 6 ms (96 cycles of CLKOUT). During this time the CLKOUT remains at 16 kHz.

- All card contacts are inactive
- Oscillator (XTAL) does not operate
- The V_{DD} supervisor, ALARM output, card presence detection and $\overline{OFF}$ output remain functional
- Internal oscillator is slowed to 32 kHz, providing 16 kHz on CLKOUT.

ACTIVE MODE

When the activation sequence is completed, the TDA8002C will be in the active mode. Data is exchanged between the card and the microcontroller via the I/O lines.

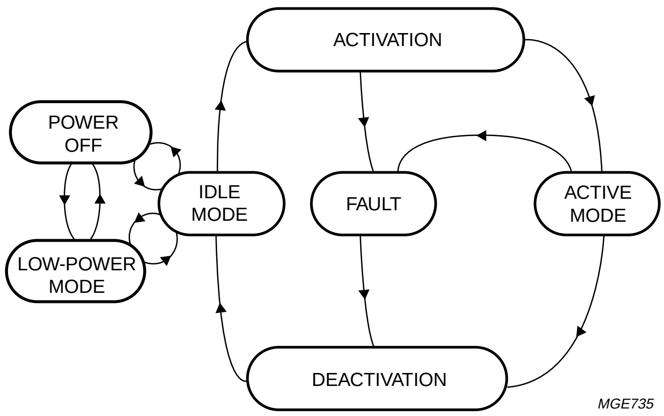


Fig.9 State diagram.

ACTIVATION SEQUENCE

From Idle mode, the circuit enters the activation mode when the microcontroller sets the $\overline{\text{CMDVCC}}$ line LOW or sets the MODE line HIGH when the $\overline{\text{CMDVCC}}$ line is already LOW. The internal circuitry is then activated, the internal clock is activated and an activation sequence is executed. When RST is enabled it becomes the inverse of RSTIN.

Figures 10 to 12 illustrate the activation sequence as follows:

1. Step-up converter is started ($t_1 \approx t_0$)
2. V_{CC} rises from 0 to 3 or 5 V ($t_2 = t_1 + 1\frac{1}{2}T$) (according to the state on pin CV/$\overline{\text{TV}}$)
3. I/O, AUX1 and AUX2 are enabled and CLK is enabled ($t_3 = t_1 + 4T$); I/O, AUX1 and AUX2 were forced LOW until this time
4. CLK is set by setting RSTIN to HIGH (t_4)
5. RST is enabled ($t_5 = t_1 + 7T$); after t_5, RSTIN has no further action on CLK, but is only controlling RST.

The value of V_{CC} (5 or 3 V) must be selected by the level on pin CV/$\overline{\text{TV}}$ before the activation sequence.

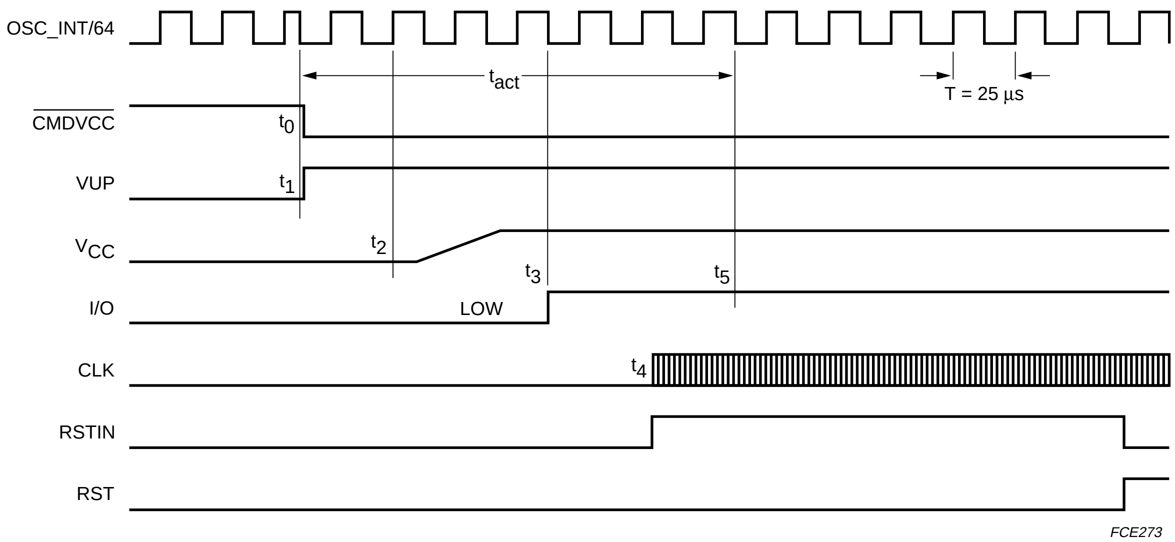


Fig.10 Activation sequence using RSTIN and $\overline{\text{CMDVCC}}$.

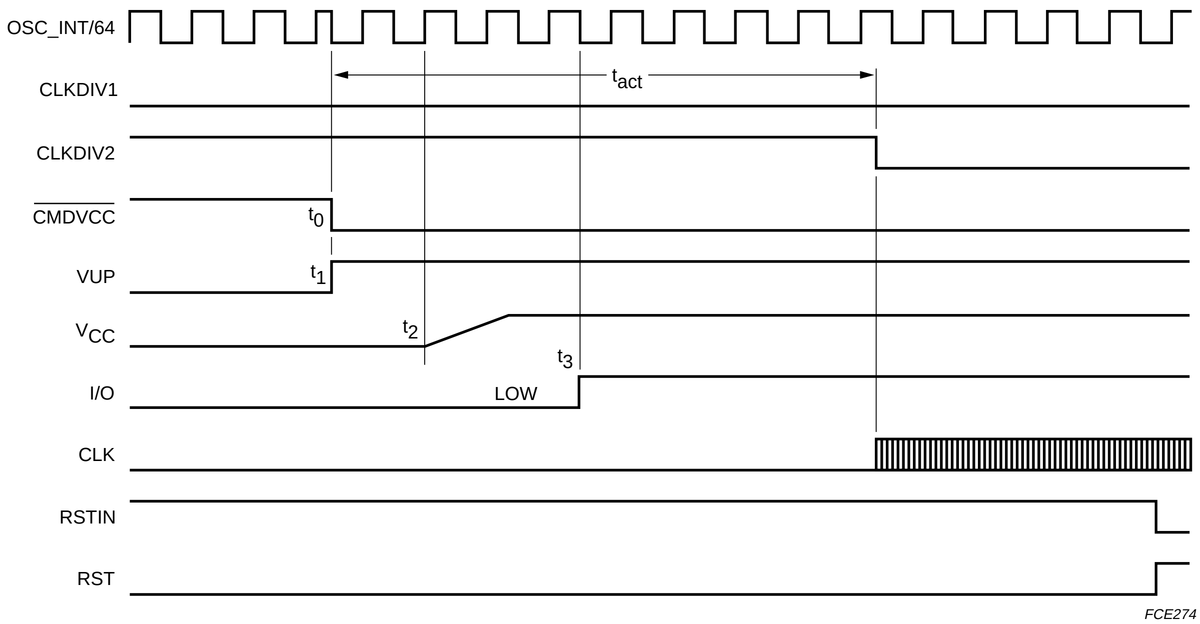


Fig.11 Activation sequence using $\overline{CMDVCC}$, CLKDIV1 and CLKDIV2 signals to enable CLK.

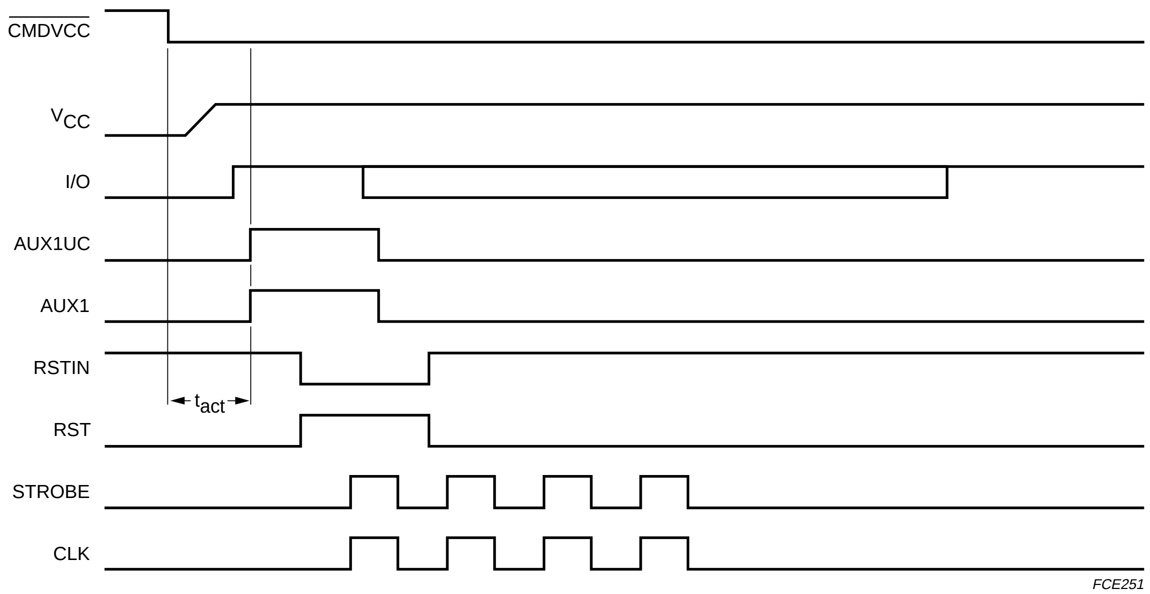


Fig.12 Activation sequence for synchronous application.

DEACTIVATION SEQUENCE

When a session is completed, the microcontroller sets the $\overline{CMDVCC}$ line to HIGH state or MODE line to LOW state. The circuit then executes an automatic deactivation sequence by counting the sequencer down and thus end in the Idle mode.

Figures 13 and 14 illustrate the deactivation sequence as follows:

1. RST goes LOW ($t_{11} \approx t_{10}$)
2. CLK is stopped ($t_{12} = t_{11} + \frac{1}{2}T$)
3. I/O, AUX1 and AUX2 fall to zero ($t_{13} = t_{11} + T$)
4. V_{CC} falls to zero ($t_{14} = t_{11} + 1\frac{1}{2}T$); a special circuit ensures that I/O remains below V_{CC} during the falling slope of V_{CC}
5. VUP falls ($t_{15} = t_{11} + 5T$).

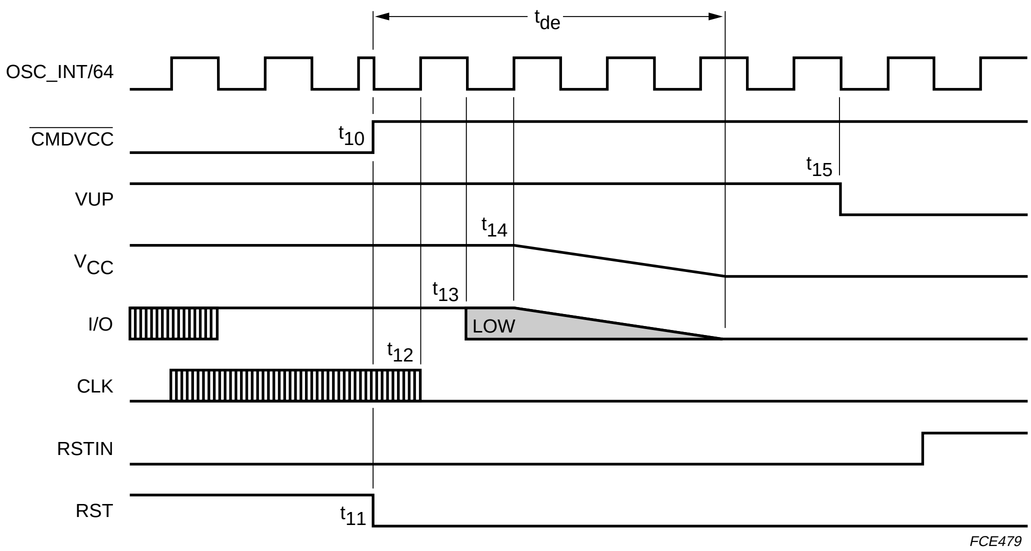


Fig.13 Deactivation sequence

Fault detection

The following fault conditions are monitored by the circuit:

- Short-circuit or high current on V_{CC}
- Removing card during transaction
- V_{DD} dropping
- Overheating.

When one or more of these faults are detected, the circuit pulls the interrupt line $\overline{OFF}$ to its active LOW state and a deactivation sequence is initiated. In the event that the card is present the interrupt line $\overline{OFF}$ is set to HIGH state when the microcontroller has reset the $\overline{CMDVCC}$ line HIGH (after completion of the deactivation sequence). In the event that the card is not present $\overline{OFF}$ remains LOW.

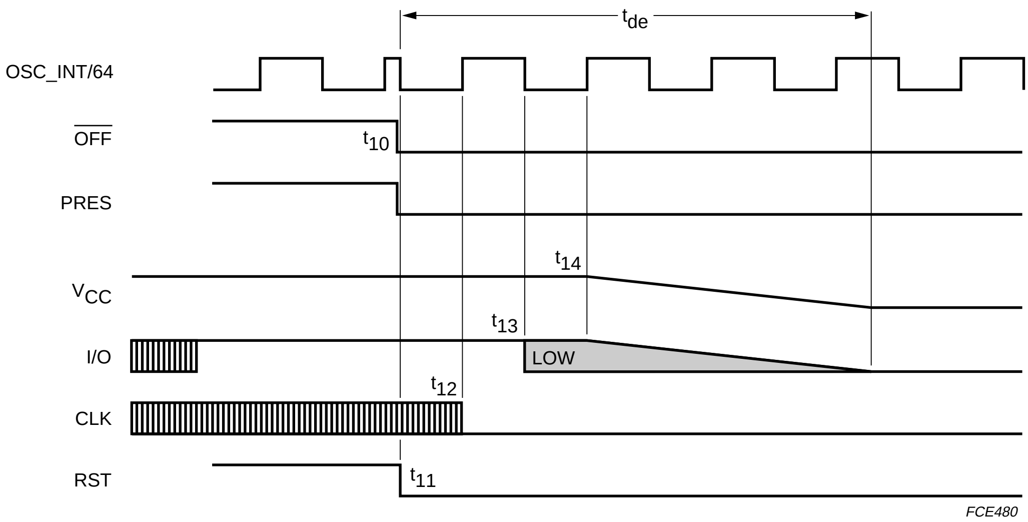


Fig.14 Emergency deactivation sequence.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–0.3	+6.5	V
V_{DDA}	analog supply voltage		–0.3	+6.5	V
V_{CC}	card supply voltage pins; XTAL1, XTAL2, ALARM, CS, MODE, RSTIN, CLKSEL, AUX2UC, AUX1UC, CLKDIV1, CLKDIV2, CLKOUT, STROBE, $\overline{\text{CMDVCC}}$, CV/$\overline{\text{TV}}$ and $\overline{\text{OFF}}$		–0.3	+6.5	V
$V_{i(card)}$	input voltage on card contact pins; I/O, AUX2, $\overline{\text{PRES}}$, PRES, AUX1, CLK, RST and V_{CC}		–0.3	+6.5	V
V_{es}	electrostatic handling voltage				
	on pins I/O, AUX2, $\overline{\text{PRES}}$, PRES, AUX1, CLK, RST and V_{CC}		–6	+6	kV
	on all other pins		–2	+2	kV
T_{stg}	storage temperature		–55	+125	°C
P_{tot}	continuous total power dissipation				
	TDA8002CT/x	T_{amb} = –25 to +85 °C	–	0.56	W
	TDA8002CG	T_{amb} = –25 to +85 °C	–	0.46	W
T_{amb}	ambient temperature		–25	+85	°C
T_j	junction temperature		–	150	°C

Note

1. Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM 1500 Ω, 100 pF) 3 positive pulses and 3 negative pulses on each pin with respect to ground.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SOT136-1		70	K/W
	SOT401-1		91	K/W

CHARACTERISTICS

V_{DD} = 3.3 V; T_{amb} = 25 °C; f_{xtal} = 10 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		3	–	6.5	V
$I_{DD(lp)}$	supply current	low-power mode	–	–	150	µA
$I_{DD(idle)}$	supply current	Idle mode; f_{CLKOUT} = 10 MHz	–	–	5	mA
$I_{DD(active)}$	supply current	active mode; $V_{CC(O)}$ = 5 V; f_{CLKOUT} = 10 MHz				
		f_{CLK} = LOW; I_{CC} = 100 µA	–	–	8	mA
		f_{CLK} = 5 MHz; I_{CC} = 10 mA	–	–	50	mA
		f_{CLK} = 5 MHz; I_{CC} = 55 mA	–	–	140	mA
		active mode; $V_{CC(O)}$ = 3 V; f_{CLKOUT} = 10 MHz				
		f_{CLK} = LOW; I_{CC} = 100 µA	–	–	8	mA
		f_{CLK} = 5 MHz; I_{CC} = 10 mA	–	–	50	mA
		f_{CLK} = 5 MHz; I_{CC} = 55 mA	–	–	140	mA
V_{th2}	threshold voltage on V_{DD} for voltage supervisor	falling	2.2	–	2.4	V
V_{hys2}	hysteresis on V_{th2}		50	100	150	mV
Card supply						
$V_{CC(O)}$	output voltage	Idle mode	–	–	0.3	V
		active mode				
		V_{CC} = 5 V; I_{CC} < 55 mA; DC load	4.6	–	5.4	V
		I_{CC} = 40 nAs; AC load	4.6	–	5.4	V
		V_{CC} = 3 V; I_{CC} < 55 mA; DC load	2.76	–	3.24	V
		I_{CC} = 24 nAs; AC load	2.76	–	3.24	V
$I_{CC(O)}$	output current	$V_{CC(O)}$ = from 0 to 5 or 3 V	–	–	55	mA
		V_{CC} short-circuited to ground	–	200	–	mA
SR	slew rate	rising or falling slope	0.10	0.15	0.20	V/µs
Crystal connections (XTAL1 and XTAL2)						
C_{ext}	external capacitors	note 1	–	15	–	pF
f_{xtal}	resonance frequency	note 2	2	–	24	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data lines						
GENERAL						
$t_{d(edge)}$	delay between falling edge of I/O, AUX1, AUX2, I/OUC, AUX1UC and AUX2UC		–	–	1	μs
t_r, t_f	rise and fall times	$C_i = C_o = 30$ pF	–	–	0.5	μs
$f_{I/O(max)}$	maximum frequency on data lines		–	–	200	kHz
DATA LINES I/O, AUX1 AND AUX2 (WITH 10 kΩ PULL-UP RESISTOR CONNECTED TO V_{CC})						
V_o	output voltage	Idle and low-power modes	0	–	0.3	V
V_{OH}	HIGH-level output voltage on data lines	$I_{OH} = -20$ μA	$0.8V_{CC}$	–	V_{CC}	V
V_{OL}	LOW-level output voltage on data lines	$I_{I/O} = 1$ mA	–	–	0.4	V
V_{IH}	HIGH-level input voltage on data lines		$0.6V_{CC}$	–	V_{CC}	V
V_{IL}	LOW-level input voltage on data lines		0	–	0.5	V
V_{idle}	voltage on data lines outside a session		–	–	0.4	V
R_{pu}	internal pull-up resistance between data lines and V_{CC}		8	10	12	kΩ
I_{edge}	current from data lines when active pull-up is active		–	1	–	mA
I_{IL}	LOW-level input current on data lines	$V_{IL} = 0.4$ V	–	–	–600	μA
I_{IH}	HIGH-level input current on data lines	$V_{IH} = V_{CC}$	–	–	10	μA
DATA LINES I/OUC, AUX1UC AND AUX2UC (WITH 20 kΩ PULL-UP RESISTOR CONNECTED TO V_{DD} WHEN CS IS HIGH AND 100 kΩ WHEN CS IS LOW)						
V_{OH}	HIGH-level output voltage on data lines	$I_{OH} = -20$ μA	$V_{DD} - 1$	–	$V_{DD} + 0.2$	V
V_{OL}	LOW-level output voltage on data lines	$I_{I/OUC} = 1$ mA	–	–	0.4	V
V_{IH}	HIGH-level input voltage on data lines		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW-level input voltage on data lines		0	–	$0.3V_{DD}$	V
Z_{idle}	impedance on data lines outside a session		10	–	–	MΩ
ALARM and $\overline{OFF}$ when connected (open-drain outputs)						
$I_{OH(OFF)}$	HIGH-level output current on pin $\overline{OFF}$	$V_{OH(OFF)} = 5$ V	–	–	5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{OL(OFF)}$	LOW-level output voltage on pin $\overline{OFF}$	$I_{OL(OFF)}$ = 2 mA	–	–	0.4	V
$I_{OL(ALARM)}$	LOW-level output current on pin ALARM	$V_{OL(ALARM)}$ = 0 V	–	–	–5	μA
$V_{OH(ALARM)}$	HIGH-level output voltage on pin ALARM	$I_{OH(ALARM)}$ = –2 mA	V_{DD} – 1	–	–	V
t_W	ALARM pulse width		6	–	20	ms
Clock output (CLKOUT; powered from V_{DD})						
f_{CLKOUT}	frequency on CLKOUT		0	–	20	MHz
		low power	–	16	–	kHz
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{DD} – 0.5	–	–	V
t_r, t_f	rise and fall times	C_L = 15 pF; notes 3 and 4	–	–	8	ns
δ	duty factor	C_L = 15 pF; notes 3 and 4	40	–	60	%
Internal oscillator						
f_{int}	frequency of internal oscillator	active mode	2	2.5	3	MHz
		sleep mode	–	32	–	kHz
Card reset output (RST)						
$V_{O(inact)}$	output voltage	inactive modes	0	–	0.3	V
$t_{d(RST)}$	delay between RSTIN and RST	RST enabled	–	–	100	ns
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 μA	V_{CC} – 0.5	–	V_{CC}	V
t_r, t_f	rise and fall times	C_L = 30 pF	–	–	0.5	ns
Card clock output (CLK)						
$V_{O(inact)}$	output voltage	inactive modes	0	–	0.3	V
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –50 μA	V_{CC} – 0.5	–	V_{CC}	V
t_r, t_f	rise and fall times	C_L = 30 pF; note 3	–	–	8	ns
δ	duty factor	C_L = 30 pF; note 3	45	–	55	%
SR	slew rate (rise and fall)		0.2	–	–	V/ns
Strobe input (STROBE)						
f_{STROBE}	frequency on STROBE		0	–	10	MHz
V_{IL}	LOW-level input voltage		0	–	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	–	V_{DD}	V
Logic inputs (CLKSEL, CLKDIV1, CLKDIV2, MODE, $\overline{CMDVCC}$ and RSTIN); note 5						
V_{IL}	LOW-level input voltage		0	–	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	–	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOGIC INPUTS (CV/$\overline{TV}$ AND CS) (INTEGRATED 10 kΩ PULL-UP RESISTOR CONNECTED TO V_{DD}); note 5						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
Logic inputs $\overline{PRES}$ and PRES; note 5						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$I_{IL(PRES)}$	LOW-level input current on pin $\overline{PRES}$	V_{OL} = 0 V	–	–	–10	µA
$I_{IH(PRES)}$	HIGH-level input current on pin $\overline{PRES}$		–	–	10	µA
Protections						
T_{sd}	shut-down local temperature		–	135	–	°C
$I_{CC(sd)}$	shut-down current at V_{CC}		–	–	90	mA
Timing						
t_{act}	activation sequence duration	guaranteed by design; see Fig.12	–	180	220	µs
t_{de}	deactivation sequence duration	guaranteed by design; see Fig.14	50	70	100	µs
t_3	start of the window for sending CLK to the card	see Figs 10 and 11	–	–	130	µs
t_5	end of the window for sending CLK to the card	see Fig.11	150	–	–	µs
t_{IS}	time from input to select		100	–	–	ns
t_{SI}	time from select to input		1000	–	–	ns
t_{ID}	time from input to deselect		1000	–	–	ns
t_{DI}	time from deselect to input		100	–	–	ns
t_{SL}	time from select to low impedance		–	–	40	ns
t_{DZ}	time from deselect to high impedance	pull-up resistor at pin $\overline{OFF}$ = 10 kΩ; 1 device	–	–	6	ns
		2 devices in parallel	–	–	3	ns
$t_{r(max)}$	maximum rise time on pin CS		–	–	100	ns
$t_{f(max)}$	maximum fall time on pin CS		–	–	100	ns

Notes

1. It may be necessary to connect capacitors from XTAL1 and XTAL2 to ground depending on the choice of crystal or resonator.
2. When the oscillator is stopped in mode 1, XTAL1 is set to HIGH.
3. The transition time and duty cycle definitions are shown in Fig.15; $\delta = \frac{t_1}{t_1 + t_2}$
4. CLKOUT transition time and duty cycle do not need to be tested.
5. $\overline{\text{PRES}}$ and $\overline{\text{CMDVCC}}$ are active LOW; RSTIN, PRES and CS are active HIGH.

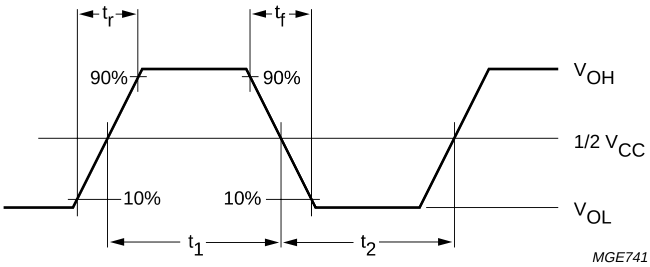
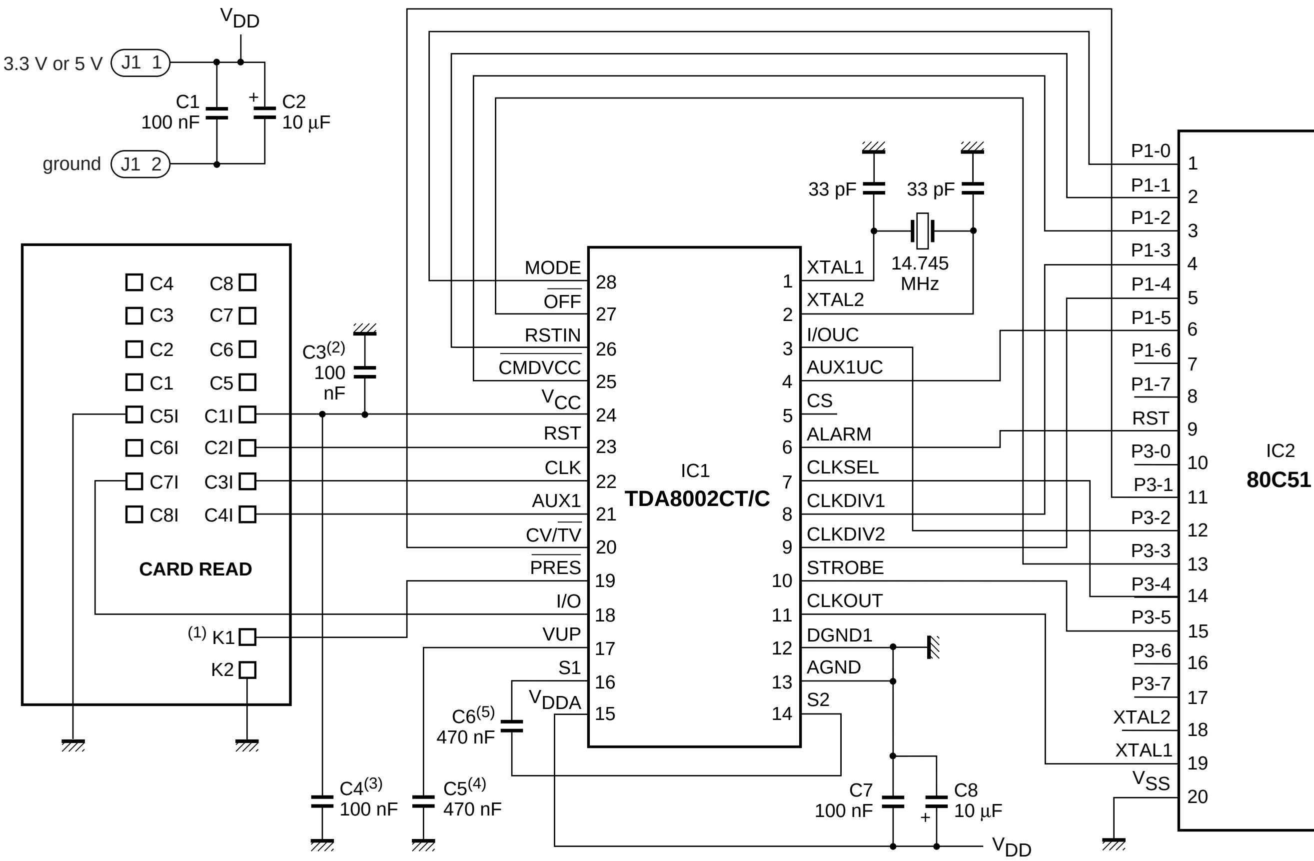


Fig.15 Definition of transition times.



TDA8002C should be placed as close as possible to the card reader.

(1) Contact normally open.

(2) C3 close to pin V_{CC} of TDA8002C.

(3) C4 close to C1 contact of card reader.

(4) C5 close to VUP pin of TDA8002C.

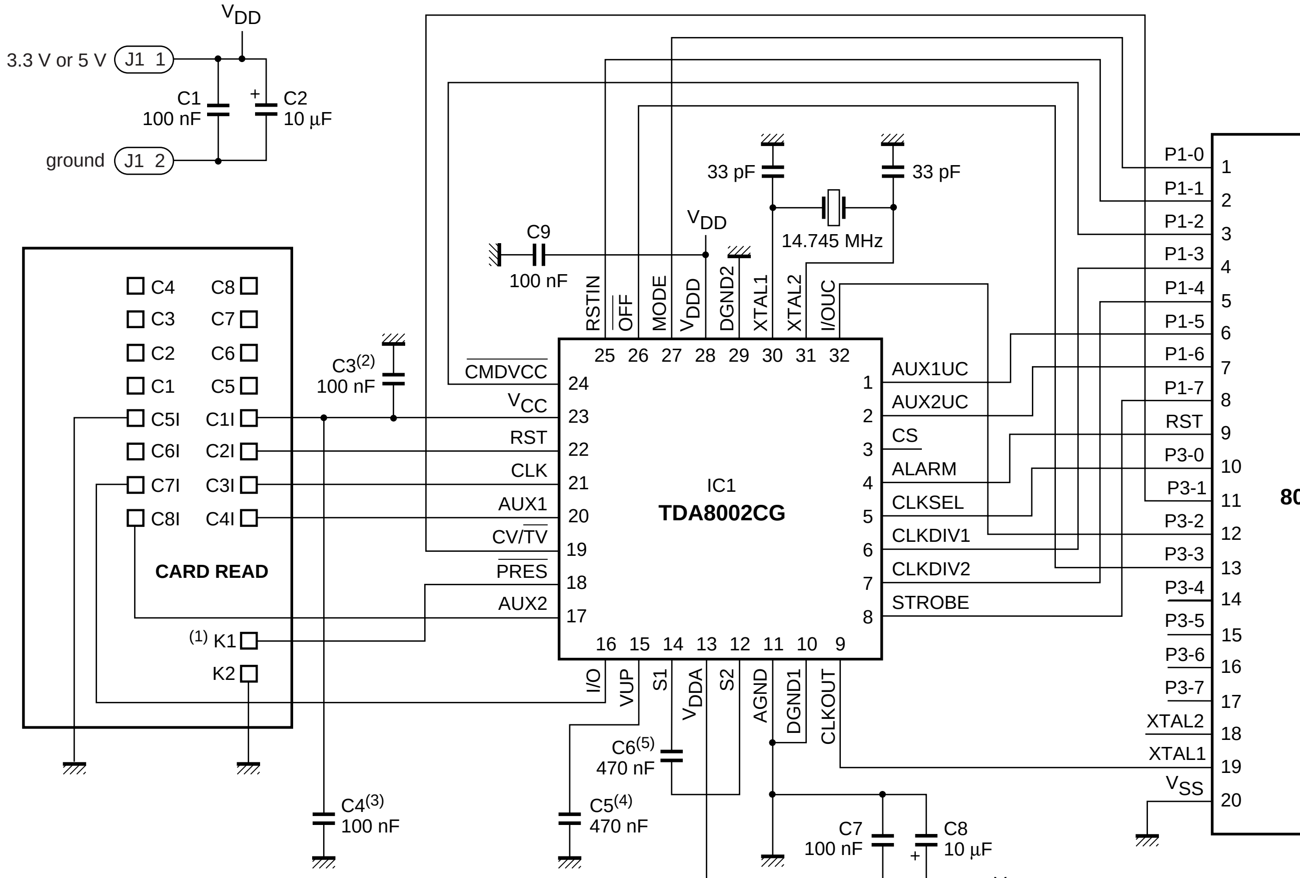
(5) C6 as close as possible to pins S1 and S2.

CLK line may be shielded with respect to other lines.

Decoupling capacitors C7 and C8 may be placed as close as possible to pin V_{DDA}.

A good ground plane is recommended.

Fig.16 Application diagram.



TDA8002C should be placed as close as possible to the card reader.

(1) Contact normally open.

(2) C3 close to pin V_{CC} of TDA8002C.

(3) C4 close to C1 contact of card reader.

(4) C5 close to VUP pin of TDA8002C.

(5) C6 as close as possible to pins S1 and S2.

CLK line may be shielded with respect to other lines.

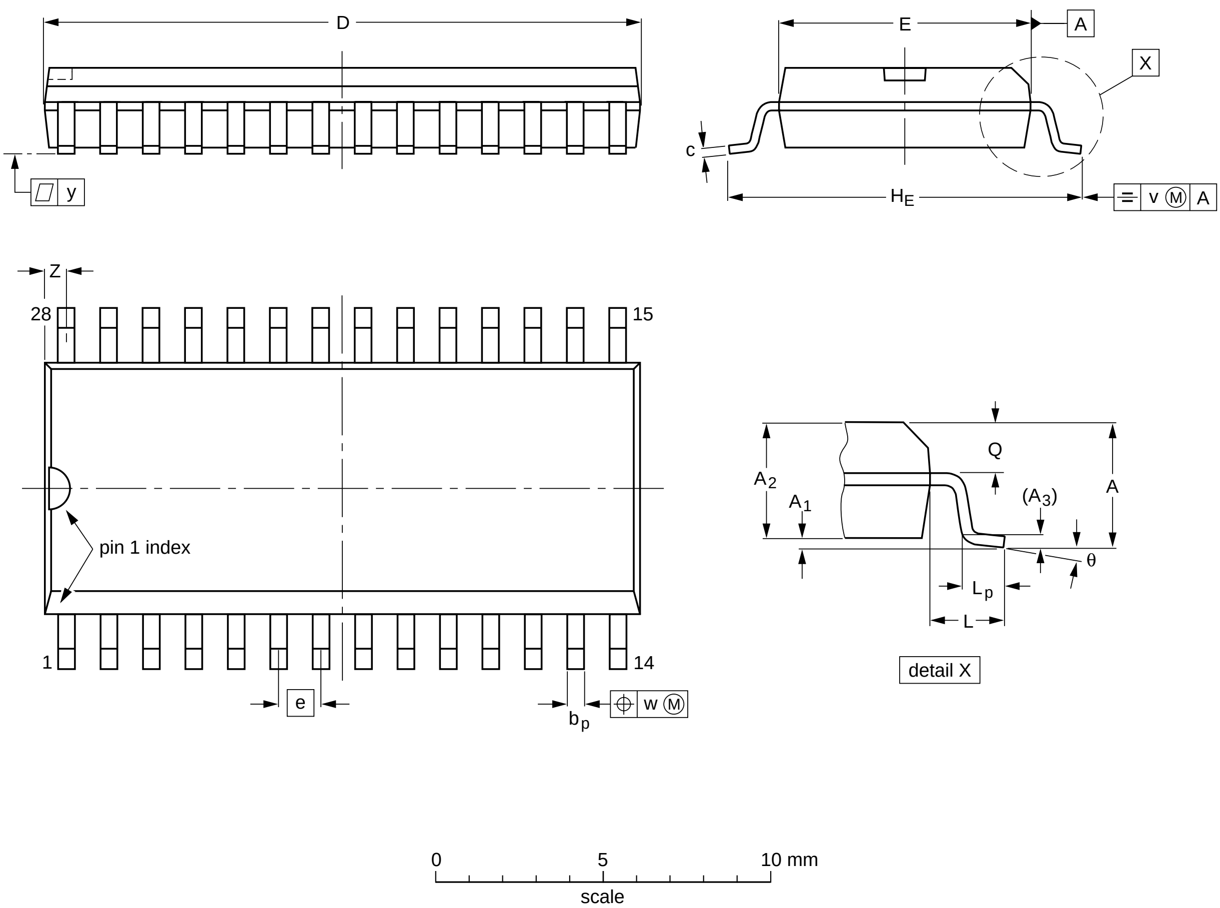
Decoupling capacitors C7, C8 and C9 may be placed as close as possible to pin V_{DDA} a

A good ground plane is recommended.

Fig.17 Application diagram (for more details, see *“Application note AN98054”*).

PACKAGE OUTLINES

SO28: plastic small outline package; 28 leads; body width 7.5 mm — SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

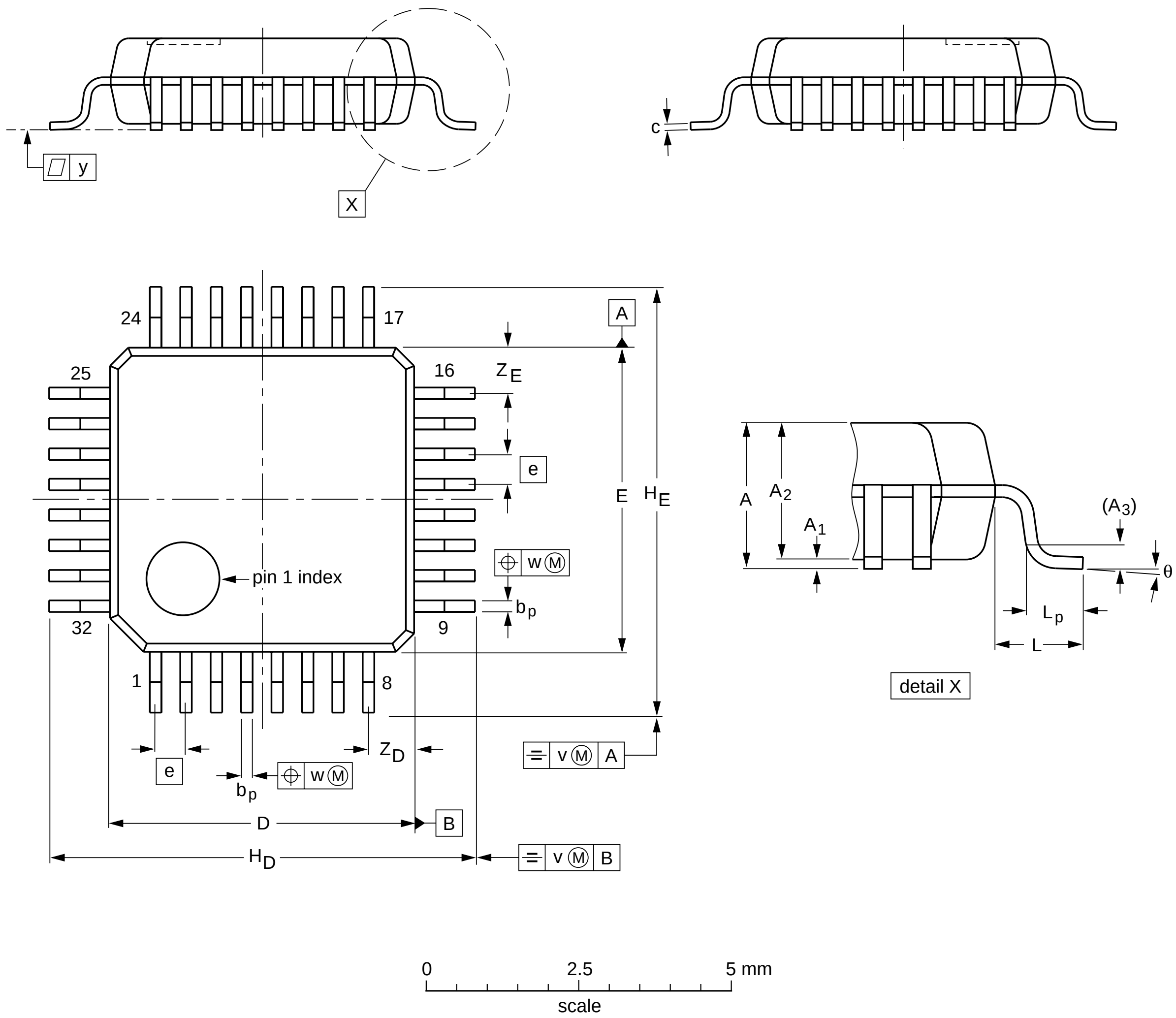
UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(1)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 545004/25/03/pp28 Date of release: 1999 Oct 12 Document order number: 9397 750 06149