TDF8546

I²C-bus controlled 4 × 45 W best efficiency amplifier

Rev. 8 — 27 September 2013 Product short data sheet

1. General description

The TDF8546 is one of a new generation of complementary quad Bridge-Tied Load (BTL) audio power amplifiers intended for automotive applications. It has a best efficiency mode with full I²C-bus controlled diagnostics, including start-up diagnostics. The TDF8546 can operate at a battery voltage as low as 6 V making this amplifier suitable for stop/start-car operation.

The new best efficiency principle uses a patented switch technique which reduces switching distortion. To reduce power dissipation, the new best efficiency principle uses the audio information on all four channels instead of only the front or rear signals. Dissipation is more than 65 % less than standard BTL when used for front and rear correlated audio signals. Dissipation is 35 % less than standard BTL when used for uncorrelated (delayed) audio signals between front and rear. It is 17 % less for uncorrelated audio signals when the front or rear information is used.

The amplifier uses a complementary DMOS output stage in a Silicon-On-Insulator (SOI) based BCD process. The DMOS output stage ensures a high-power output signal with perfect sound quality. The SOI-based BCD process ensures a robust amplifier, where latch-up cannot occur, with good separation between the four independent channels, with every component isolated and without substrate currents.

2. Features and benefits

- Stop/start-car prepared: keeps operating without audible disturbance during engine start at a battery voltage as low as 6 V
- New best efficiency mode with patented low switching distortion
- Extreme best efficiency mode (uses information from 4 channels) with 17 % less dissipation for uncorrelated signals compared to 2-channel best efficiency mode.
- Operates in either legacy (non-I²C-bus) or I²C-bus modes (3.3 V and 5 V compliant)
- Four hardware-programmable I²C-bus addresses
- Can drive 2 Ω and 4 Ω loads
- Speaker fault detection
- Start-up diagnostics with load detection: open, short, present; filtered for door-slam and chatter relays
- AC load (tweeter) detection with low and high current mode
- Gain select after start-up without audible disturbance
- Independent selectable soft mute of front and rear channels
- Programmable gain (26 dB and 16 dB), independently programmable for the front and rear channels

- Line driver mode supports engine start at a battery voltage as low as 6 V (16 dB and mid-tap voltage 0.25 × V_P)
- Programmable clip detect: 2 %, 5 % or 10 %
- Programmable thermal pre-warning
- Pin STB can be programmed/multiplexed with second-clip detect
- Clip information of each channel can be directed separately to pin DIAG or pin STB
- Independent enabling of thermal-, clip- or load fault information (short across the load or to V_P or to ground) on pin DIAG
- Loss-of-ground and open V_P safe (minimum series resistance required)
- All amplifier outputs short-circuit proof to ground, supply voltage and across the load (channel independent)
- All pins short-circuit proof to ground
- Temperature controlled gain reduction to prevent audio holes at high junction temperatures
- Programmable low battery voltage detection to enable 7.5 V or 6 V minimum battery voltage operation
- Overvoltage protection (load-dump safe up to V_P = 50 V) with overvoltage pre-warning at 16 V
- Offset detection

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{P(oper)}$	operating supply voltage	R_L = 4 Ω	6	14.4	18	V
I_q	quiescent current	no load	-	260	350	mA
		no load; V_P = 7 V	-	190	-	mA
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; maximum power; V_i = 2 V RMS square wave	37	40	-	W
		R_L = 4 Ω; V_P = 15.2 V; maximum power; V_i = 2 V RMS square wave	41	45	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %	18	20	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %	23	25	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 10 %	40	44	-	W
		R_L = 2 Ω; V_P = 14.4 V; maximum power; V_i = 2 V RMS square wave	58	64	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f_i = 1 kHz; R_L = 4 Ω; BTL mode	-	0.01	0.1	%
		P_o = 4 W; f_i = 1 kHz; R_L = 4 Ω; best efficiency mode	-	0.03	-	%
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz; R_S = 1 kΩ				
		amplifier mode	-	43	65	μV
		line driver mode	-	25	33	μV

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4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDF8546J	DBS27P	plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm)	SOT827-1
TDF8546TH	HSOP36	plastic, heatsink small outline package; 36 leads; low stand-off height	SOT851-1
TDF8546JS	DBSMS27P	plastic dual bent surface mounted SIL power package; 27 leads	SOT1154-1

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5. Pinning information

5.1 Pinning

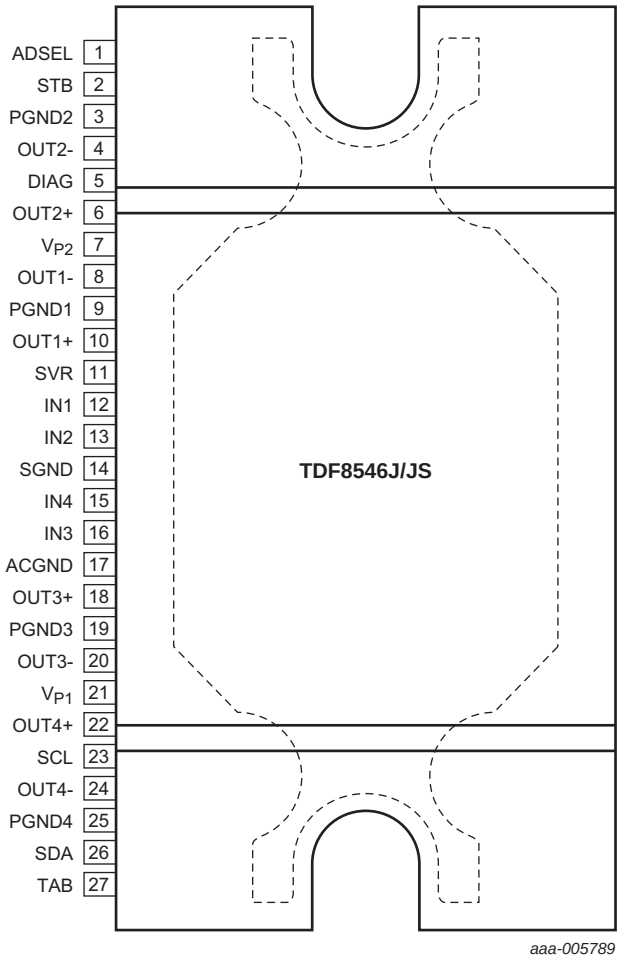

Fig 1. Pin configuration of TDF8546J/JS (packages DBS27P and DBSMS27P)

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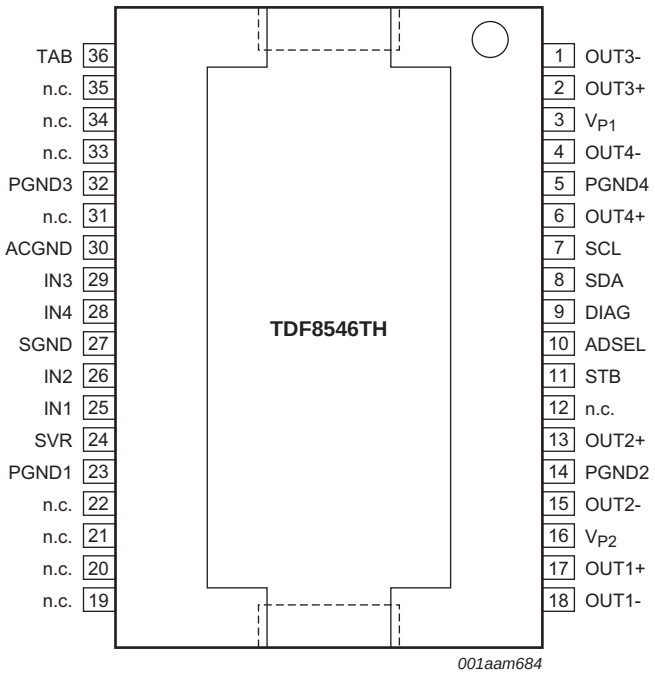

Fig 2. Pin configuration TDF8546TH

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5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TDF8546J/JS	TDF8546TH	
ADSEL	1	10	I²C-bus address select
STB	2	11	Standby (I²C-bus mode) or mode pin (legacy mode) programmable second clip indicator
PGND2	3	14	channel 2 power ground
OUT2−	4	15	channel 2 negative output (right rear)
DIAG	5	9	diagnostic and clip detection output
OUT2+	6	13	channel 2 positive output (right rear)
V_{P2}	7	16	power supply voltage 2
OUT1−	8	18	channel 1 negative output (right front)
PGND1	9	23	channel 1 power ground
OUT1+	10	17	channel 1 positive output (right front)
SVR	11	24	half supply voltage filter capacitor
IN1	12	25	channel 1 input
IN2	13	26	channel 2 input
SGND	14	27	signal ground
IN4	15	28	channel 4 input
IN3	16	29	channel 3 input
ACGND	17	30	AC ground
OUT3+	18	2	channel 3 positive output (left front)
PGND3	19	32	channel 3 power ground
OUT3−	20	1	channel 3 negative output (left front)
V_{P1}	21	3	power supply voltage 1
OUT4+	22	6	channel 4 positive output (left rear)
SCL	23	7	I²C-bus clock input
OUT4−	24	4	channel 4 negative output (left rear)
PGND4	25	5	channel 4 power ground
SDA	26	8	I²C-bus data input and output
TAB	27	36	heatsink connection; must be connected to ground
n.c.	-	12, 19, 20, 21, 22, 31, 33, 34, 35	not connected

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6. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
DBS27/DBSMS27P				
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		40	K/W
HSOP36				
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		35	K/W

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7. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage behavior						
$V_{P(oper)}$	operating supply voltage	R_L = 4 Ω	6	14.4	18	V
		R_L = 2 Ω	6	14.4	16	V
I_q	quiescent current	no load	-	260	350	mA
		no load; V_P = 7 V	-	190	-	mA
I_{off}	off-state current	V_{STB} = 0.4 V	-	4	10	μA
V_O	output voltage	DC				
		amplifier on; high gain/low gain mode	6.6	7.1	7.6	V
		line driver mode; IB4[D2] = 0; IB3[D5:D6] = 1	3.0	3.4	3.8	V
$V_{P(low)(mute)}$	low supply voltage mute	rising supply voltage				
		IB4[D0] = 1	7.0	7.7	8.1	V
		IB4[D0] = 0	5.4	5.7	6.2	V
		falling supply voltage				
		IB4[D0] = 1	6.5	7.2	7.7	V
		IB4[D0] = 0	5.2	5.5	5.9	V
$\Delta V_{P(low)(mute)}$	low supply voltage mute hysteresis	IB4[D0] = 1	0.1	0.5	0.8	V
		IB4[D0] = 0	0.1	0.3	0.7	V
$V_{P(ovp)pwarn}$	pre-warning overvoltage protection supply voltage	rising supply voltage	15.2	16	16.9	V
		falling supply voltage	14.4	15.2	16.2	V
		hysteresis	-	0.8	-	V
$V_{th(ovp)}$	overvoltage protection threshold voltage	rising supply voltage	18	20	22	V
V_{POR}	power-on reset voltage	falling supply voltage	-	3.1	4.5	V
$V_{O(offset)}$	output offset voltage	amplifier on	−75	0	+75	mV
		amplifier mute	−25	0	+25	mV
		line driver mode	−45	0	+45	mV

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Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Mode select and second clip detection: pin STB							
V_{STB}	voltage on pin STB	off-by mode selected					
		I²C-bus mode		-	-	0.8	V
		legacy mode (I²C-bus mode off)		-	-	0.8	V
		mute selected					
		legacy mode (I²C-bus mode off)		2.5	-	4.5	V
		operating mode selected					
		I²C-bus mode		2.5	-	V_P	V
		legacy mode (I²C-bus mode off)		5.9	-	V_P	V
		low voltage on pin STB when pulled LOW during clipping; clip detection on STB active	[1]				
		I_{STB} = 150 µA		5.6	5.9	6.5	V
		I_{STB} = 500 µA		6.1	-	7.4	V
I_{STB}	current on pin STB	0 V < V_{STB} < 8.5 V; clip detection not active	[1]	-	5	30	µA
Start-up/shut-down/mute timing							
t_{wake}	wake-up time	time after wake-up via pin STB before first I²C-bus transmission is recognized;		-	300	500	µs
$I_{LO(SVR)}$	output leakage current on pin SVR			-	-	5	µA
$t_{d(mute_off)}$	mute off delay time	time from amplifier start to 10 % of output signal; I_{LO} = 0 µA	[2]				
		I²C-bus mode; with I_{LO} = 5 µA → +15 ms; no DC-load (IB1[D1] = 0);		-	430	650	ms
		legacy mode; with I_{LO} = 5 µA → +20 ms; V_{STB} = 7 V; R_{ADSEL} = 0 Ω;		-	430	650	ms
t_{amp_on}	amplifier on time	time from amplifier start to amplifier on; 90 % of output signal; I_{LO} = 0 µA	[2]				
		I²C-bus mode; with I_{LO} = 5 µA → +30 ms; no DC-load (IB1[D1] = 0);		-	550	800	ms
		legacy mode; with I_{LO} = 5 µA → +20 ms; V_{STB} = 7 V; R_{ADSEL} = 0 Ω;		-	550	800	ms

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Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{off}	amplifier switch-off time	time to DC output voltage < 0.1 V; I_{LO} = 0 μA [2]				
		I²C-bus mode; with I_{LO} = 5 μA → +0 ms;	250	500	750	ms
		via pin STB; (IB4[D6] = 0); with I_{LO} = 5 μA → +0 ms;	250	500	750	ms
$t_{d(mute-on)}$	delay time from mute to on	from 10 % to 90 % of output signal; V_i = 50 mV; I²C-bus mode (IB2[D1, D2] = 1 to 0) or IB2(D0 = 1 to 0) or legacy mode (V_{STB} = 3 V to 7 V);	5	15	40	ms
$t_{d(soft_mute)}$	soft mute delay time	from 90 % to 10 % of output signal; V_i = 50 mV; I²C-bus mode (IB2[D1, D2] = 0 to 1) or legacy mode (V_{STB} = 7 V to 3 V);	5	15	40	ms
$t_{d(fast_mute)}$	fast mute delay time	from 90 % to 10 % of output signal; V_i = 50 mV; I²C-bus mode (IB2[D0] = 0 to 1, or V_{STB} from > 5.9 V to < 0.8 V in 1 μs;	-	0.4	1	ms
$t_{(start-Vo(off))}$	engine start to output off time	V_P from 14.4 V to 5 V in 1.5 ms; V_o < 0.5 V;	-	0.1	1	ms
$t_{(start-SVRoff)}$	engine start to SVR off time	V_P from 14.4 V to 5 V in 1.5 ms; V_{SVR} < 0.7 V;	-	40	75	ms
I²C-bus interface [3]						
V_{IL}	LOW-level input voltage	pins SCL and SDA	-	-	1.5	V
V_{IH}	HIGH-level input voltage	pins SCL and SDA	2.3		5.5	V
V_{OL}	LOW-level output voltage	pin SDA; I_L = 5 mA	-	-	0.4	V
f_{SCL}	SCL clock frequency		-	400	-	kHz
V_{ADSEL}	voltage on pin ADSEL	I²C-bus address A[6:0] = 1101 101				
		$Rseries_{ADSEL}$ = 0 Ω	4	5	11	V
		$Rseries_{ADSEL}$ = 100 kΩ	-	-	V_P	V
$I_{I(ADSEL)}$	input current on pin ADSEL	V_{STB} = 5 V; V_{ADSEL} = 5 V	-	2	10	μA
R_{ADSEL}	resistance on pin ADSEL	I²C-bus address A[6:0] = 1101 110	99	100	101	kΩ
		I²C-bus address A[6:0] = 1101 111	29.7	30	30.3	kΩ
		I²C-bus address A[6:0] = 1101 010	9.9	10	10.1	kΩ
		legacy mode	-	-	0.47	kΩ
$V_{P(latch)}$	latch supply voltage	does not react to address selection changes	-	-	6	V
Start-up diagnostics						

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Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{sudiag}	start-up diagnostic time	from start-up diagnostic command via I²C-bus until completion of start-up diagnostic; V_O + < 0.1 V; V_O − < 0.1 V (no load) IB1[D1] = 1;	50	130	250	ms
$t_{d(sudiag-on)}$	start-up diagnostic to on delay time	at 90 % of output signal; IB1[D0:D1] = 11;	-	680	-	ms
V_{offset}	offset voltage	start-up diagnostic offset voltage under no load condition	1.3	2	2.5	V
$R_{Ldet(sudiag)}$	start-up diagnostic load detection resistance	shorted load				
		high gain; IB3[D6:D5] = 00	-	-	0.5	Ω
		low gain; IB3[D6:D5] = 11	-	-	1.5	Ω
		normal load				
		high gain (IB3[D6:D5] = 00)	1.5	-	20	Ω
		low gain (IB3[D6:D5] = 11)	3.2	-	20	Ω
		line driver load	80	-	200	Ω
		open load	400	-	-	Ω
Amplifier diagnostics						
$V_{OL(DIAG)}$	LOW-level output voltage on pin DIAG	fault condition; I_{DIAG} = 1 mA	-	-	0.3	V
$V_{O(offset_det)}$	output voltage at offset detection		±1.0	±1.3	±2.0	V
THD_{clip}	total harmonic distortion clip detection level	V_P > 10 V				
		IB2[D7:D6] = 10	-	10	-	%
		IB2[D7:D6] = 01	-	5	-	%
		IB2[D7:D6] = 00	-	2	-	%
$T_{j(AV)(pwarn)}$	pre-warning average junction temperature	IB3[D4] = 0 or legacy mode	150	160	170	°C
		IB3[D4] = 1	125	135	145	°C
$T_{j(AV)(G(-0.5dB))}$	average junction temperature for 0.5 dB gain reduction	V_i = 0.05 V; best efficiency mode turns off when activated	-	175	-	°C
$\Delta G_{(th_fold)}$	gain reduction of thermal foldback	when all channels switch off	-	20	-	dB
I_o	output current	I²C-bus mode; IB5[D7] = 0; AC load bit set; peak current				
		IB4[D1] = 1	500	-	-	mA
		IB4[D1] = 0	275	-	-	mA
		I²C-bus mode; IB5[D7] = 0; AC load bit not set; peak current				
		IB4[D1] = 1	-	-	250	mA
		IB4[D1] = 0	-	-	100	mA

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Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier							
P_o	output power	R_L = 4 Ω; V_P = 14.4 V; THD = 0.5 %		18	20	-	W
		R_L = 4 Ω; V_P = 14.4 V; THD = 10 %		23	25	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 0.5 %		29	32	-	W
		R_L = 2 Ω; V_P = 14.4 V; THD = 10 %		40	44	-	W
$P_{o(max)}$	maximum output power	R_L = 4 Ω; V_P = 14.4 V; V_i = 2 V RMS square wave		37	40	-	W
		R_L = 4 Ω; V_P = 15.2 V; V_i = 2 V RMS square wave		41	45	-	W
		R_L = 2 Ω; V_P = 14.4 V; V_i = 2 V RMS square wave		58	64	-	W
THD	total harmonic distortion	P_o = 1 W to 12 W; f_i = 1 kHz; R_L = 4 Ω; BTL mode		-	0.01	0.1	%
		P_o = 1 W; f_i = 1 kHz; R_L = 4 Ω; V_P = 7 V; BTL and best efficiency mode		-	0.01	0.1	%
		P_o = 4 W; f_i = 1 kHz; R_L = 4 Ω; best efficiency mode		-	0.03	0.1	%
		P_o = 1 W to 12 W; f_i = 20 kHz; R_L = 4 Ω; best efficiency mode		-	0.3	0.4	%
		V_o = 1 V (RMS) and 4 V (RMS), f_i = 1 kHz; line driver mode		-	0.02	0.05	%
		P_o = 1 W to 12 W; f_i = 1 kHz; R_L = 4 Ω; low gain mode		-	0.01	0.1	%
α_{cs}	channel separation	best efficiency mode; R_S = 1 kΩ; R_{ACGND} = 250 Ω	[4]				
		f_i = 1 kHz		65	80	-	dB
		f_i = 10 kHz		55	65	-	dB
SVRR	supply voltage ripple rejection	f_i = 1 kHz; R_S = 1 kΩ; R_{ACGND} = 250 Ω; best efficiency mode; tested at V_P = 10.5 V	[4]	55	70	-	dB
CMRR	common mode rejection ratio	amplifier mode; V_{cm} = 0.3 V (p-p); f_i = 1 kHz to 3 kHz, R_S = 1 kΩ; R_{ACGND} = 250 Ω; best efficiency mode	[4]				
		common mode input to differential output ($V_{O(dif)}$ / $V_{I(cm)}$ + 26 dB)		55	65	-	dB
		common mode input to common mode output ($V_{O(cm)}$ / $V_{I(cm)}$ + 26 dB)		50	58	-	dB

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Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_P = 14.4 V; unless otherwise specified. Tested at T_{amb} = 25 °C; guaranteed for T_j = −40 °C to +150 °C; functionality is guaranteed for V_P < 10 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_o	output voltage variation	plop during switch-on and switch-off; best efficiency mode [5]				
		from off to mute and mute to off	-	-	7.5	mV
		from mute to on and on to mute (soft mute)	-	-	7.5	mV
		from off to on and on to off (start-up diagnostic enabled)	-	-	7.5	mV
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz (6th order); R_S = 1 kΩ				
		mute mode	-	15	23	μV
		line driver mode	-	25	33	μV
		amplifier mode; best efficiency mode	-	43	65	μV
		amplifier mode; best efficiency mode; R_S = 50 Ω	-	40	60	μV
$G_{v(amp)}$	voltage gain amplifier mode	single-ended in to differential out; best efficiency mode	25.5	26	26.5	dB
$G_{v(ld)}$	voltage gain line driver mode	single-ended in to differential out; best efficiency mode	15.5	16	16.5	dB
Z_i	input impedance	T_{amb} = −40 °C to +105 °C	38	62	105	kΩ
		T_{amb} = 0 °C to 105 °C	55	62	105	kΩ
α_{mute}	mute attenuation	$V_{o(on)}$ / $V_{o(mute)}$; V_i = 50 mV	80	92	-	dB
$V_{o(mute)(RMS)}$	RMS mute output voltage	V_i = 1 V RMS; filter 20 Hz to 22 kHz	-	16	29	μV
B_p	power bandwidth	−1 dB	-	20 to 20000	-	Hz
$C_{L(crit)}$	critical load capacitance	no oscillation; R_L between 2 Ω and open load; C_L from all outputs to GND	22	-	-	nF
Best efficiency mode control						
$V_{o(swoff)be}$	best efficiency switch-off output voltage	best efficiency switch open				
		4 Ω load selected; IB5[D4] = 1	-	0.9	-	V
		2 Ω load selected; IB5[D4] = 0	-	1.7	-	V
$R_{sw(be)}$	best efficiency switch resistance		-	1.0	-	Ω

[1] V_{STB} depends on the current into pin STB: minimum = (1429 Ω × I_{STB}) + 5.4 V, maximum = (3143 Ω × I_{STB}) + 5.6 V.

[2] The times are specified without leakage current. For a leakage current of 5 μA on pin SVR, the delta time is specified. If the capacitor value on pin SVR changes ± 30 %, the specified time also changes ± 30 %. The specified times include an ESR of 15 Ω for the capacitor on pin SVR.

[3] Standard I²C-bus specification: maximum LOW-level = 0.3V_{DD}, minimum HIGH-level = 0.7V_{DD}. To comply with 5 V and 3.3 V logic, V_{DD} = 5 V defines the maximum LOW-level and V_{DD} = 3.3 V defines the minimum HIGH-level.

[4] For optimum channel separation (α_{cs}), supply voltage ripple rejection (SVRR) and common mode rejection ratio (CMRR), a resistor $R_{ACGND} = \frac{R_S}{4}$ Ω must be in series with the ACGND capacitor.

[5] The plop-noise during amplifier switch-on and switch-off is measured using an ITU-R 2 k filter; see Figure 4.

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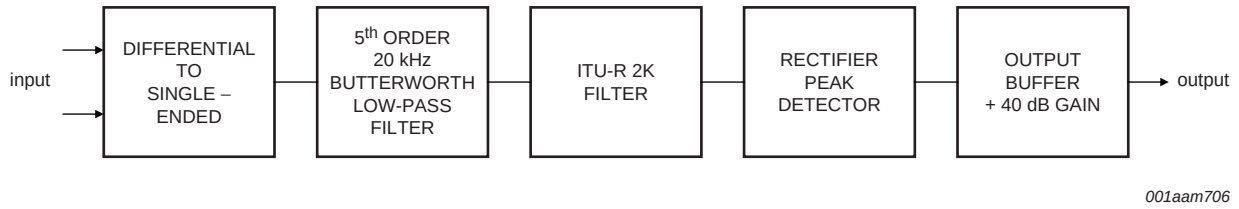
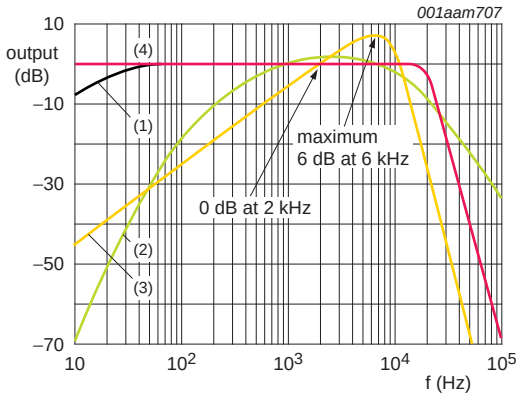


Fig 3. Location of ITU-R 2K filter



(1) 20 Hz.

(2) A-weighting.

(3) ITU-R average response meter.

(4) 20 kHz bandwidth limit.

Fig 4. Plop noise test using ITU-R 2K filter

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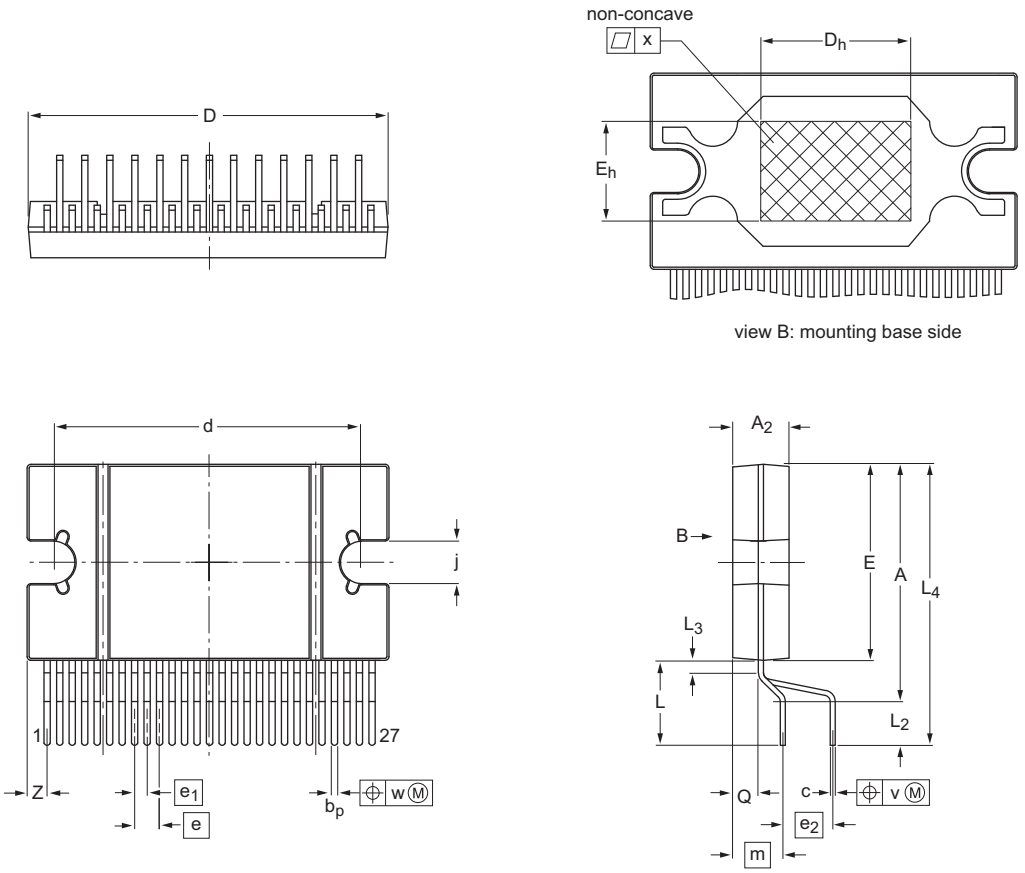
8. Package outline

DBS27P: plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm) **SOT827-1**



x	Z(1)
0.03	1.8
	1.2

Dimensions (mm are the original dimensions)

Unit		A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_2	L_3	L_4	m	Q	v	w
mm	max		4.6	0.60	0.5	29.2	24.8		15.9					3.55		3.9	1.15	22.9		2.1		
	nom	19						12		2	1	4	8	3.40	6.8				4		0.6	0.25
	min		4.4	0.45	0.3	28.8	24.4		15.5					3.25		3.1	0.85	22.1		1.8		

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot827-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT827-1						~~13-02-13~~ 13-05-30

Fig 5. Package outline SOT827-1 (DBS27P)

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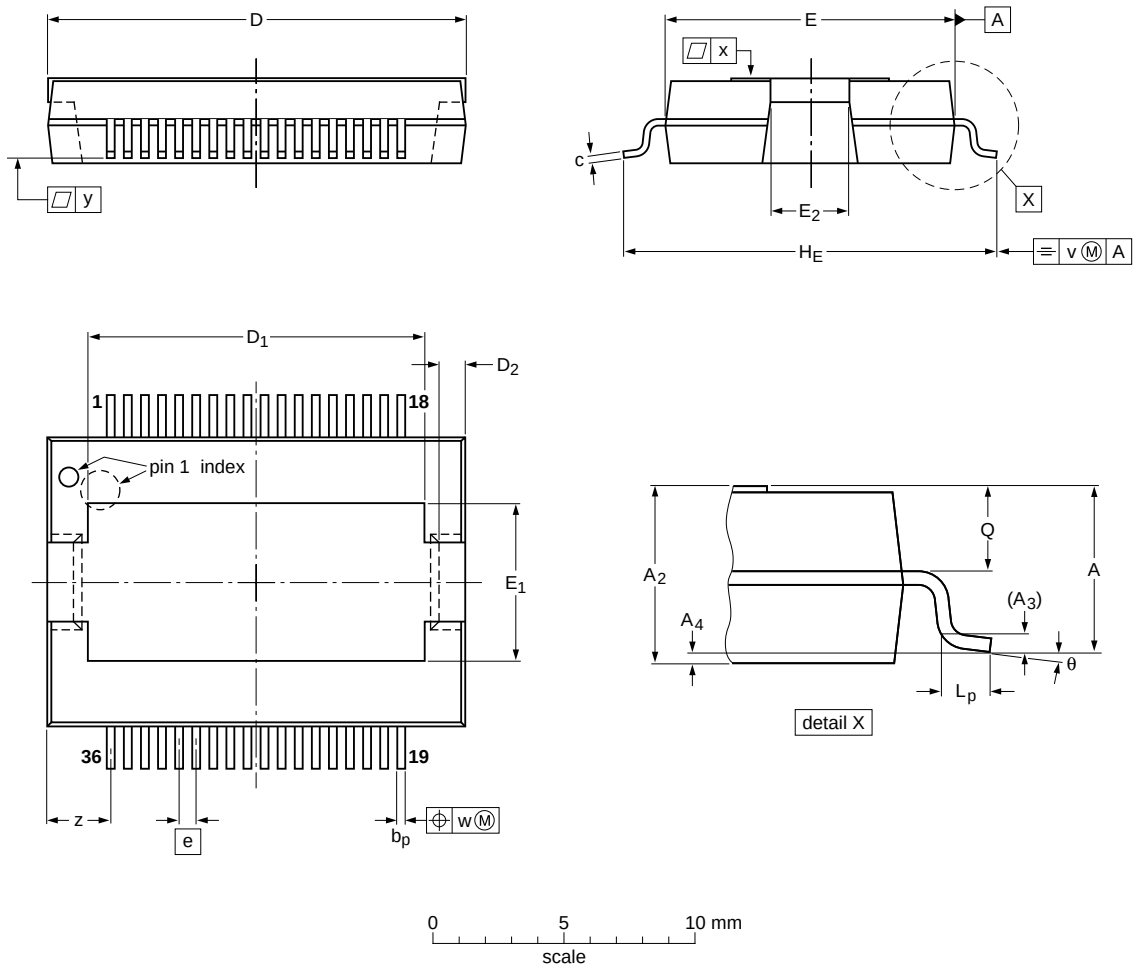
HSOP36: plastic, heatsink small outline package; 36 leads; low stand-off height **SOT851-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4[1]	b_p	c	D[2]	D_1	D_2	E[2]	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.4 3.3	0.35	+0.08 −0.04	0.38 0.25	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	0.65	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.12	0.03	0.07	2.55 2.20	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT851-1						~~04-03-09~~ 04-05-25

Fig 6. Package outline SOT851-1 (HSOP36)

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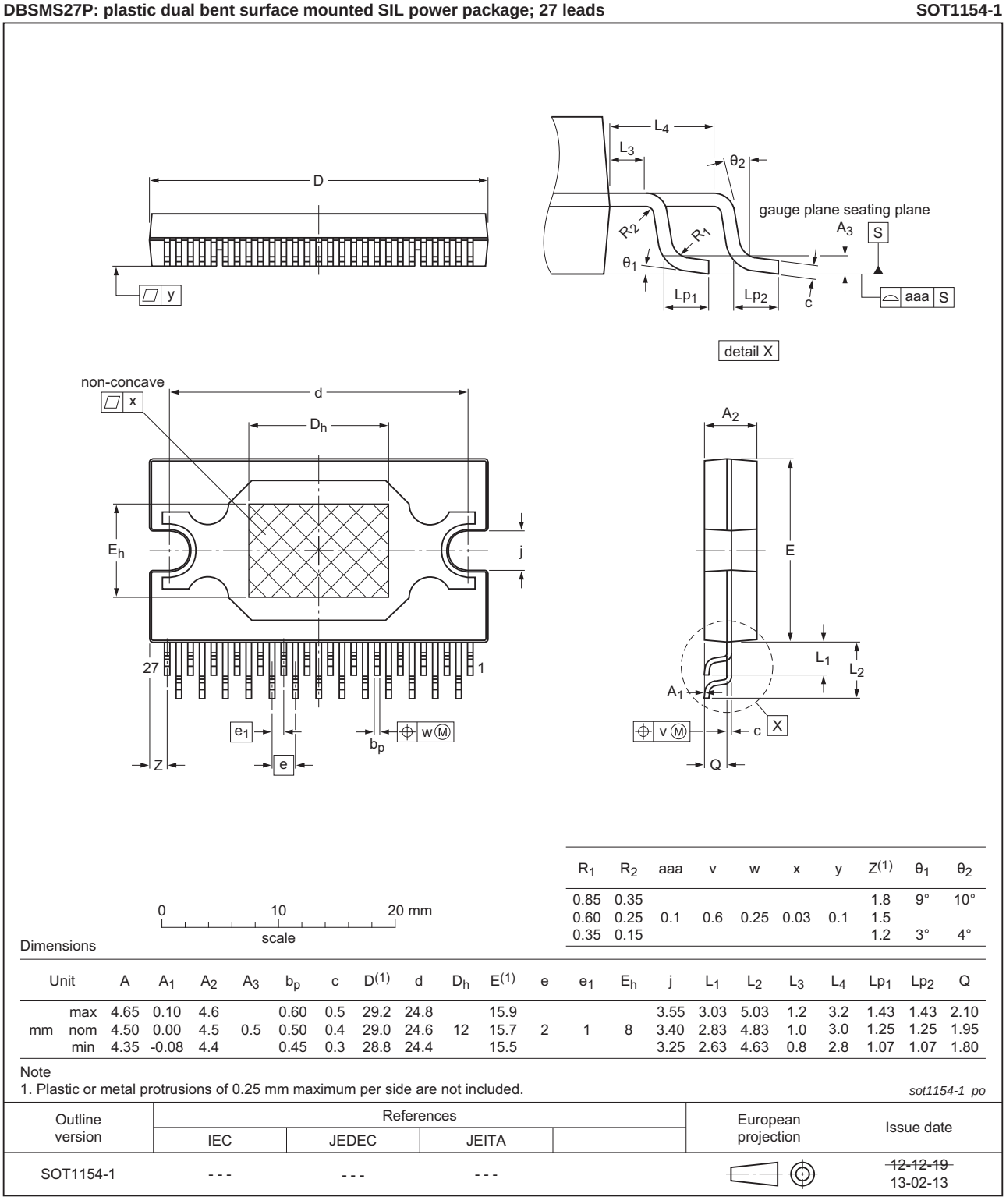
DBSMS27P: plastic dual bent surface mounted SIL power package; 27 leads **SOT1154-1**



R_1	R_2	aaa	v	w	x	y	$Z^{(1)}$	θ_1	θ_2
0.85	0.35						1.8	9°	10°
0.60	0.25	0.1	0.6	0.25	0.03	0.1	1.5		
0.35	0.15						1.2	3°	4°

Dimensions

Unit	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	E_h	j	L_1	L_2	L_3	L_4	Lp_1	Lp_2	Q
max	4.65	0.10	4.6		0.60	0.5	29.2	24.8		15.9				3.55	3.03	5.03	1.2	3.2	1.43	1.43	2.10
mm nom	4.50	0.00	4.5	0.5	0.50	0.4	29.0	24.6	12	15.7	2	1	8	3.40	2.83	4.83	1.0	3.0	1.25	1.25	1.95
min	4.35	-0.08	4.4		0.45	0.3	28.8	24.4		15.5				3.25	2.63	4.63	0.8	2.8	1.07	1.07	1.80

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1154-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1154-1	- - -	- - -	- - -			~~12-12-19~~ 13-02-13

Fig 7. Package outline SOT1154-1 (DBSMS27P)

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9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8546 v.8	20130927	Product short data sheet	-	-

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10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

1 General description 1
2 Features and benefits 1
3 Quick reference data 2
4 Ordering information 3
5 Pinning information 4
5.1 Pinning 4
5.2 Pin description 6
6 Thermal characteristics 7
7 Characteristics 8
8 Package outline 15
9 Revision history 18
10 Legal information 19
10.1 Data sheet status 19
10.2 Definitions 19
10.3 Disclaimers 19
10.4 Trademarks 20
11 Contact information 20
12 Contents 21

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